异构内存管理

部分相关论文分享

甄艳洁

- 层次架构
- DRAM作为PCM的小型缓冲
- Lazy-write

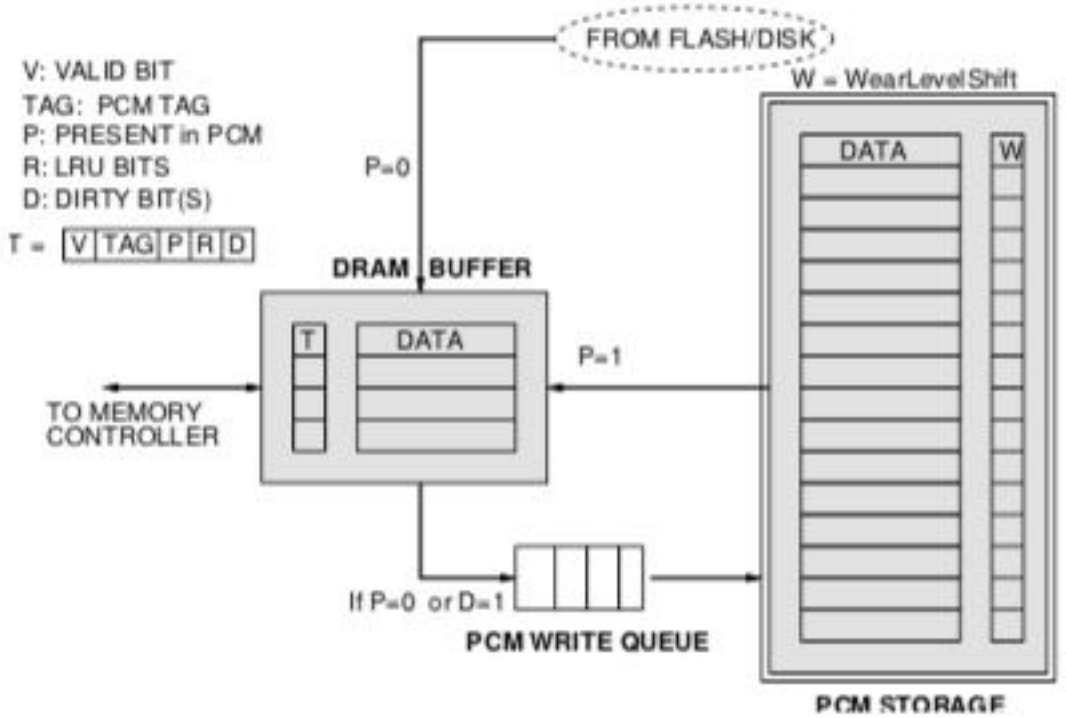

Figure 5: Lazy Write Organization

1. Scalable High Performance Main Memory System Using Phase-Change Memory Technology [ISCA 09]

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- DRAM作为PCM的小型缓冲
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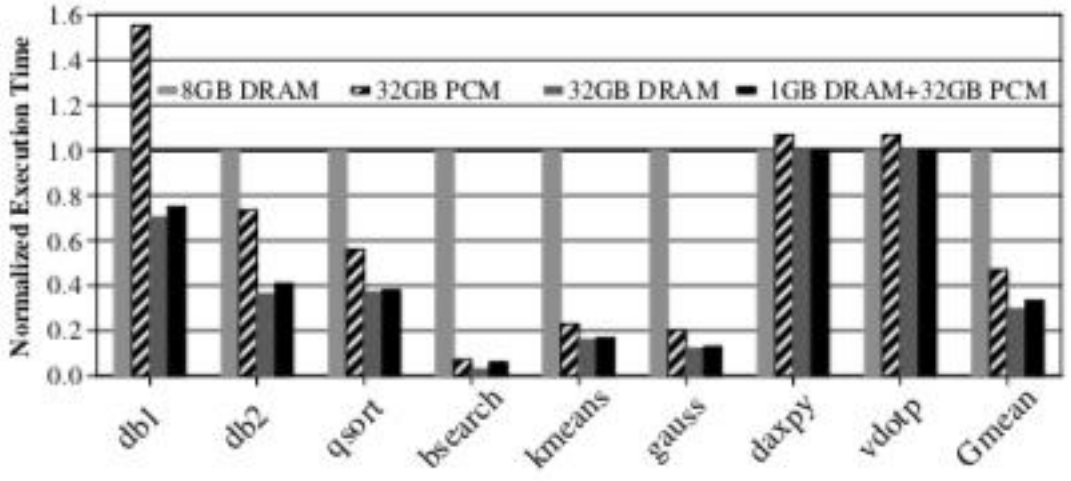
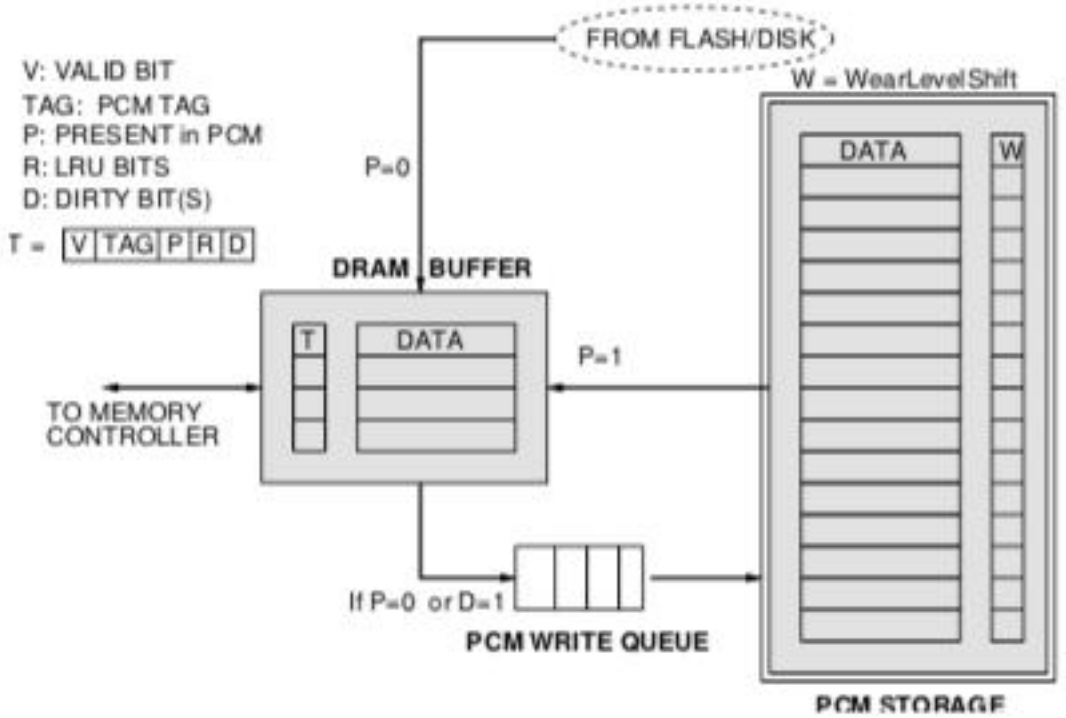


Figure 10: Execution time (normalized to 8GB DRAM).



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- Memory control 收集访问频次信息
- OS 实现页面置换（保证磨损均衡/性能）

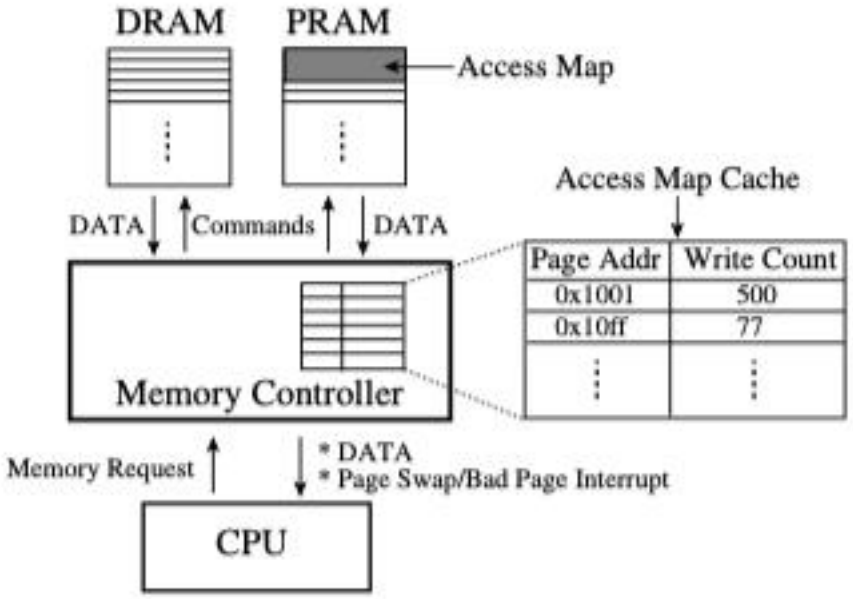

Figure 2: PDRAM Memory controller

1. PDRAM:A Hybird PRAM and DRAM Main Memory System [DAC 09]

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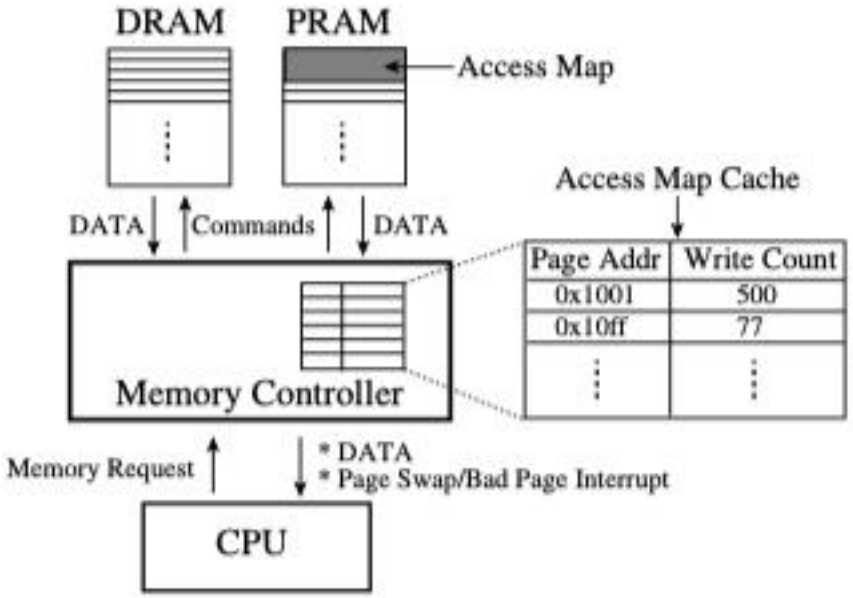

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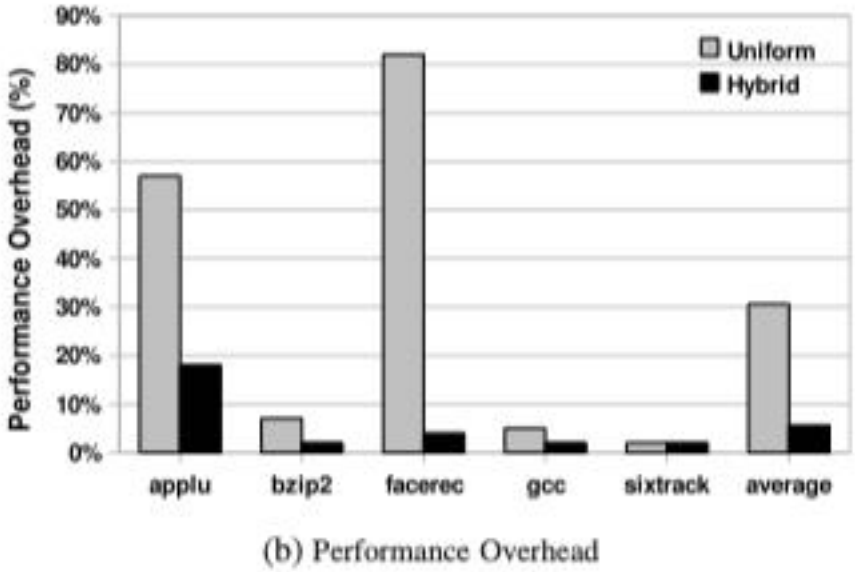


(b) Performance Overhead

Figure 3: Energy Savings and Performance Overhead Results

1. PDRAM:A Hybird PRAM and DRAM Main Memory System [DAC 09]

- DRAM/NVM分别拥有一个LRU队列
- NVM的队列记录读写次数（只记录top position）
- NVM队列头页面频次达到阈值迁移到DRAM
- 从disk读取页面到DRAM
- 可以大量减少VNM写操作

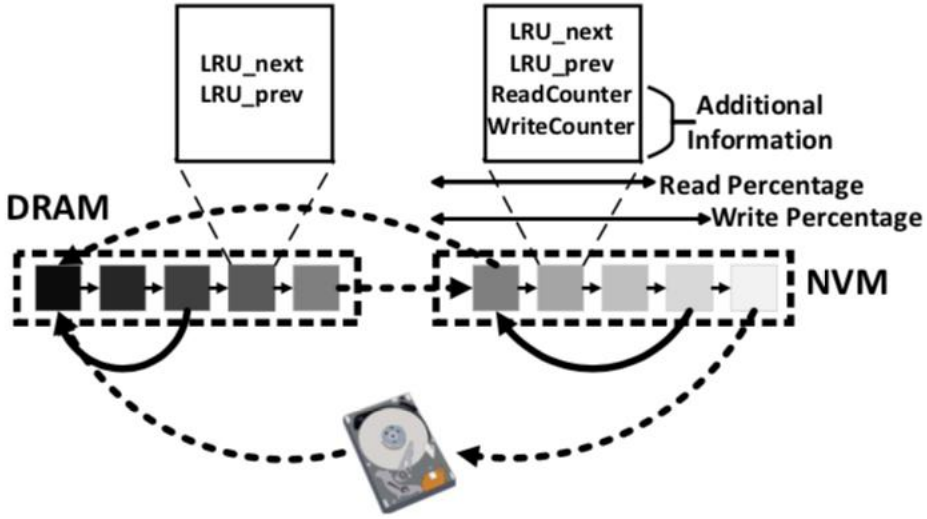
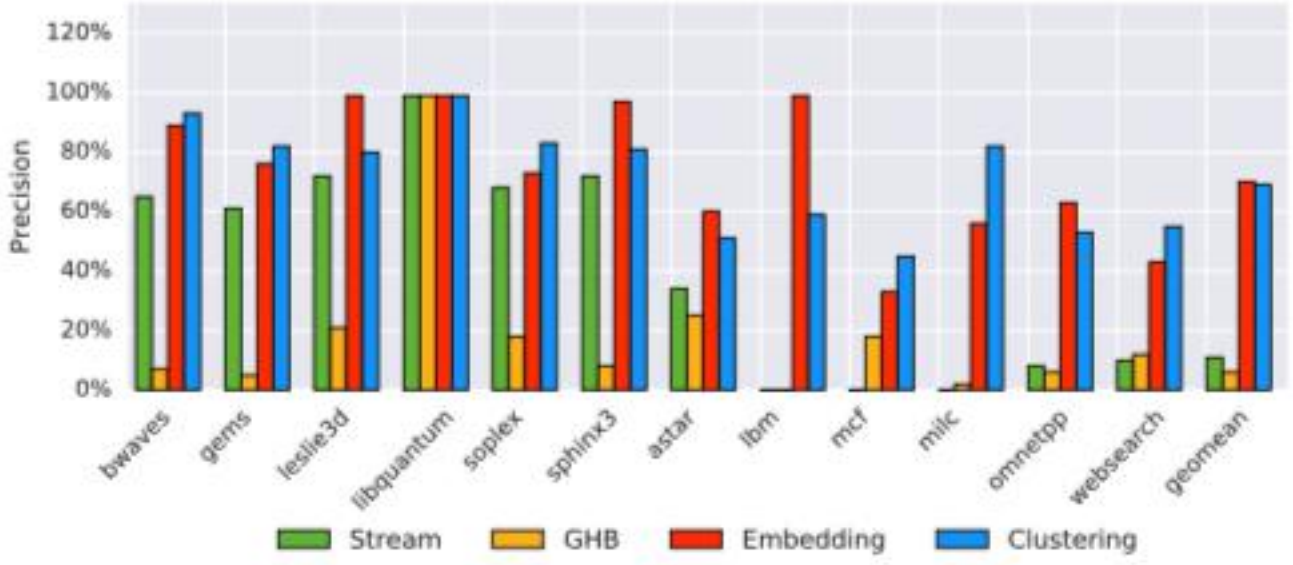


Fig. 3: Proposed Data Migration Scheme in a Hybrid Memory Architecture

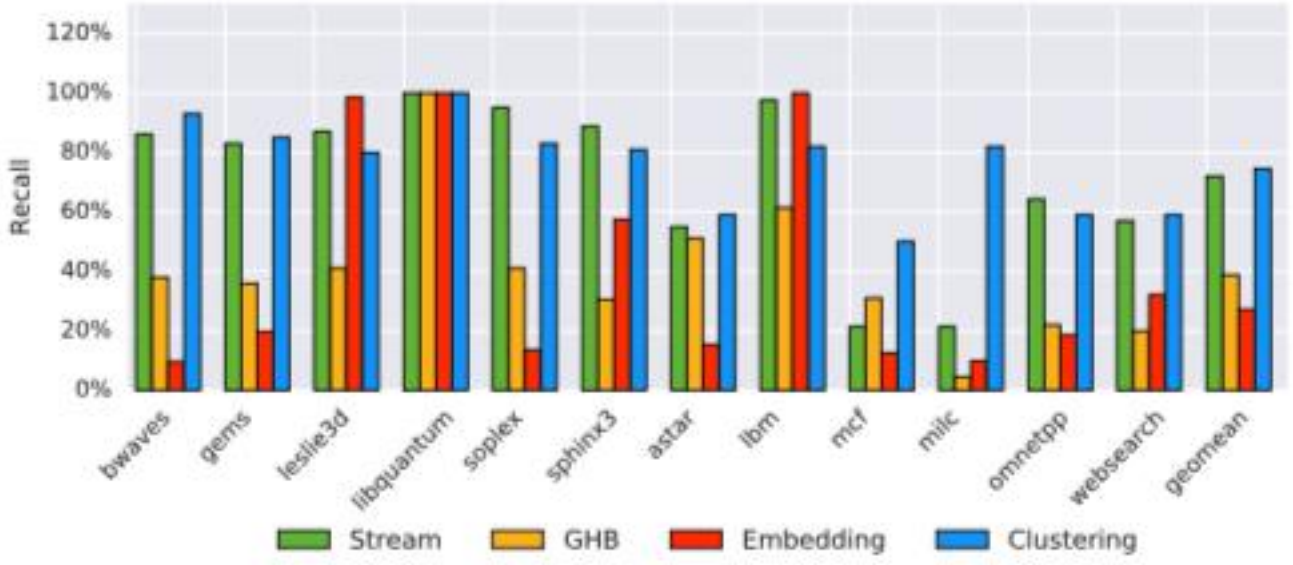
1. An Operating System Level Data Migration Scheme in Hybrid DRAM-NVM Memory Architecture **[DATE 16]**
2. Page Placement in Hybrid Memory Systems [ICS 11]

- 本文关注机器学习算法
- 无实际系统中的验证

- 使用pin采集数据
- 聚类&LSTM模型



(a) Precision



(b) Recall

1. Learning Memory Access Patterns **[ICML 18]**
2. Long Short Term Memory Based Hardware Prefetcher [MEMSYS 17]