Chenyang Zhou

New York, NY cz2791@columbia.edu 6692219195

chenyang-zhou chz05 My Website

Education

Columbia University *Aug 2023 – Dec 2024*
MS in Computer Science

- GPA: 3.6/4.0
- **Coursework:** Databases, Advanced Systems Programming, Embedded Systems, Cloud Computing & Big Data, Computer Networks, Artificial Intelligence.

University of California San Diego *Sept 2021 – June 2023*
BS in Computer Science

- GPA: 3.6/4.0
- **Coursework:** Computer Architecture, Advanced Processor Architecture Design Project, Programming Language, Computational Theory, Machine Learning, Algorithm, Math Statistics, Deep Learning, Parallel Computing, Operating System, Digital System, Software Engineering.

Research Interest

Computer Architecture, Data center Accelerators, Compilers.

Experiences

Research Assistant *New York, NY*
Columbia University *Feb 2024 – Dec 2024*

- Worked on a research project that submitted to conference ISCA 2025: Compiler-based simulation Infrastructure for multiple hardware Accelerators that advised by Professor Tanvir Ahmad Khan.

Teaching Assistant *New York, NY*
Columbia University *Sept 2023 – Dec 2024*

- Working as a Teaching Assistant for Computer Architecture, helping with grading and holding routine Office Hours.
- Understanding mantees' problems and helping them get unblocked by hands-on debugging and clear explanations.

Projects

Operating System Application (Java) *github.com/chz05/nachos*

- Designed and implemented logics for Nachos operating system to support multiprogramming, enabling the execution of multiple threads concurrently.
- The logics were proved to be correct through comparison with Java's Exchange library/package
- Implemented file system I/O interfaces in a multi-threaded scenario following documented semantics and specifications, to achieve processes' asynchronous file system access capabilities.
- Implemented UNIX-like exec, join, and exit commands for sub-process creation and orchestration.

Screaming bird (SystemVerilog/C) *screaming bird*

- Hardware/Software Co-design for Screaming bird (The frequency of voice input to control the movement of the flappy bird) in DE1-SoC board.
- Implement Software side to control the movement of bird and pipes and Hardware side to receive voice signal and display sprite graphs.

Advanced Processor Architecture Design (SystemVerilog/C) *github.com/chz05/project*

- Implemented and designed Victim Cache, Cache Set Dueling, Tournament Predictor and Out-of-order Execution in MIPS processor.

Awards and Honors

Provost Honors: 5 times in University of California San Diego.

Dean's List: 5 times in De Anza College (Cupertino, CA).

Technologies

Languages: C++, C, Java, Python, SQL, JavaScript, verilog, systemverilog

Technologies: MLIR, LLVM, Linux, Git, Docker