User's Manual

# μPD720201/μPD720202

## User's Manual: Hardware

## USB3.0 HOST CONTROLLER




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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

# PREFACE

**Readers**

This manual is intended for engineers who need to be familiar with the capability of the μPD720201/μPD720202 in order to develop application systems based on it.

**Purpose**

The purpose of this manual is to help users understand the hardware capabilities (listed below) of the μPD720201/μPD720202.

**Configuration**

This manual consists of the following chapters:

- Overview
- Pin function
- Register information
- Power management
- How to connect to external elements
- How to access external ROM
- FW download interface
- Battery charging function

**Guidance**

Readers of this manual should already have a general knowledge of electronics, logic circuits, and microcomputers.

**Notation**

This manual uses the following conventions:

| | |
|---|---|
| Data bit significance: | High-order bits on the left side;<br>low-order bits on the right side |
| Active low: | XXXXB (Pin and signal names are suffixed with B.) |
| **Note**: | Explanation of an indicated part of text |
| **Caution**: | Information requiring the user's special attention |
| **Remark**: | Supplementary information |
| Numerical value: | Binary ... xxxx or xxxxb<br>Decimal ... xxxx<br>Hexadecimal ... xxxxh |

**Related Document**

Use this manual in combination with the following document.
The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- μPD720201/μPD720202 Data Sheet: R19DS0047E

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μPD720201/μPD720202
ASSP (USB3.0 HOST CONTROLLER)

R19UH0078EJ0801
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# 1. Overview

The μPD720201 and μPD720202 are Renesas' third generation Universal Serial Bus 3.0 host controllers, which comply with Universal Serial Bus 3.0 Specification, and Intel's eXtensible Host Controller Interface (xHCI). These devices reduce power consumption and offer a smaller package footprint making them ideal for designers who wish to add the USB3.0 interface to mobile computing devices such as laptops and notebook computers.

The μPD720201 supports up to four USB3.0 SuperSpeed ports and the μPD720202 supports up to two USB3.0 SuperSpeed ports. The μPD720201 and μPD720202 use a PCI Express® Gen 2 system interface bus allowing system designers to easily add up to four (μPD720201) or two (μPD720202) USB3.0 SuperSpeed ports to systems containing the PCI Express bus interface. When connected to USB 3.0-compliant peripherals, the μPD720201 and μPD720202 can transfer information at clock speeds of up to 5 Gbps. The μPD720201 and μPD720202 and USB 3.0 standard are fully compliant and backward compatible with the previous USB2.0 standard. The new USB 3.0 standard supports data transfer speeds of up to ten times faster than those of the previous-generation USB2.0 standard, enabling quick and efficient transfers of large amounts of information.

## 1.1 Features

- Compliant with Universal Serial Bus 3.0 Specification Revision 1.0, which is released by USB Implementers Forum, Inc
  - Supports the following speed data rates: Low-Speed (1.5 Mbps) / Full-Speed (12 Mbps) / Hi-Speed (480 Mbps) / SuperSpeed (5 Gbps)
  - μPD720201 supports up to 4 downstream ports for all speeds
  - μPD720202 supports up to 2 downstream ports for all speeds
  - Supports all USB compliant data transfer types as follows; Control / Bulk / Interrupt / Isochronous transfer
- Compliant with Intel's eXtensible Host Controller Interface (xHCI) Specification Revision 1.0
  - Supports USB debugging capability on all SuperSpeed ports.
- Supports USB legacy function
- Compliant with PCI Express Base Specification Revision 2.0
- Supports Latency Tolerance Reporting ECN of PCI Express Specification
- Supports ExpressCard™ Standard Release1.0
- Supports PCI Express Card Electromechanical Specification Revision 2.0
- Supports PCI Bus Power Management Interface Specification Revision 1.2
- Supports USB Battery Charging Specification Revision 1.2 and other portable devices
  - DCP mode of BC 1.2
  - CDP mode of BC 1.2
  - China Mobile Phone Chargers
  - EU Mobile Phone Chargers
  - Apple iOS products
- Operational registers are direct-mapped to PCI memory space
- Supports Serial Peripheral Interface (SPI) type ROM for Firmware
- Supports Firmware Download Interface from system BIOS or system software
- System clock: 24 MHz crystal

- Small and low count pin package with improved signal pin assignment for efficient PCB layout
  - μPD720201 adopts 68pin QFN (8 x 8)
  - μPD720202 adopts 48pin QFN (7 x 7)
- 3.3 V and 1.05 V power supply

## 1.2 Applications

Desktop and Laptop computers, Tablet, Server, PCI Express Card / Express Card, Digital TV, Set-Top-Box, BD Player/Recorder, Media Player, Digital Audio systems, Projector, Multi Function Printer, Storage, Router, NAS, etc

## 1.3 Ordering Information

| Part Number | Package | Packing form | Operating temperature | Remark |
|---|---|---|---|---|
| μPD720201K8-701-BAC-A | 68-pin QFN (8 × 8) | Fraction (any vacancy in the tray and any free space in the carton) | 0 to 85 °C | Lead-free product |
| μPD720201K8-701-BAC-M1-A | | Full Carton (tray and Carton is packed with every product) | | |
| μPD720202K8-701-BAA-A | 48-pin QFN (7 x 7) | Fraction | | |
| μPD720202K8-701-BAA-M1-A | | Full Carton | | |
| μPD720201K8-711-BAC-A | 68-pin QFN (8 × 8) | Fraction | −40 to 85 °C | Lead-free product |
| μPD720201K8-711-BAC-M1-A | | Full Carton | | |
| μPD720202K8-711-BAA-A | 48-pin QFN (7 x 7) | Fraction | | |
| μPD720202K8-711-BAA-M1-A | | Full Carton | | |

**Note:** μPD720201K8-711-BAC-A & μPD720201K8-711-BAC-M1-A & μPD720202K8-711-BAA-A & μPD720202K8-711-BAA-M1-A should should use the FW Download function.
μPD720201K8-711-BAC-A & μPD720201K8-711-BAC-M1-A & μPD720202K8-711-BAA-A & μPD720202K8-711-BAA-M1-A should do not support the External ROM (Serial Peripheral Interface (SPI) type ROM).
μPD720201 & μPD720202 should download the firmware from the External ROM (-701 versions only) or by FW download function after Power on Reset.
Regarding External ROM & FW Download function, refer to “6.How to Access External ROM” & “7. FW Download Interface”.

## 1.4 Block Diagram

**Figure 1-1. μPD720201 Block Diagram**

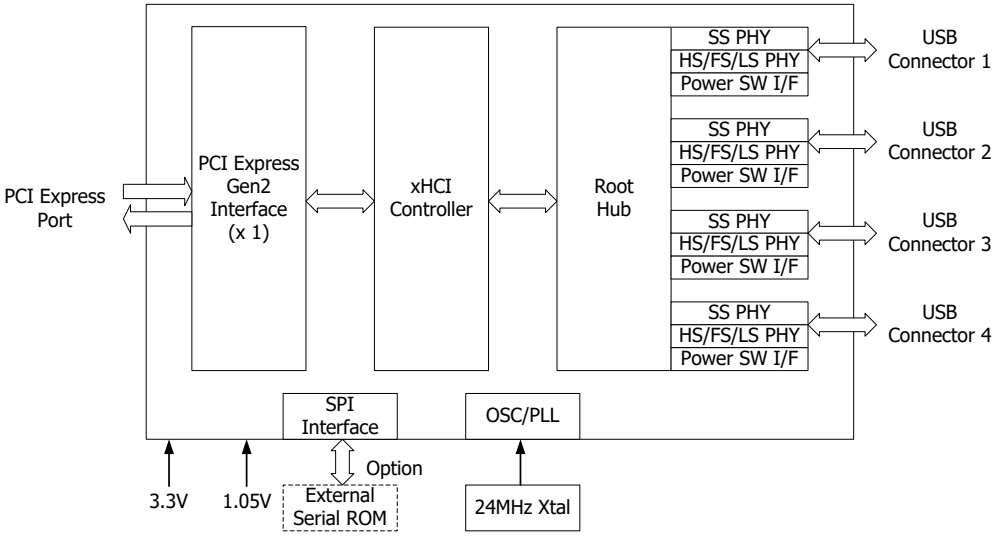
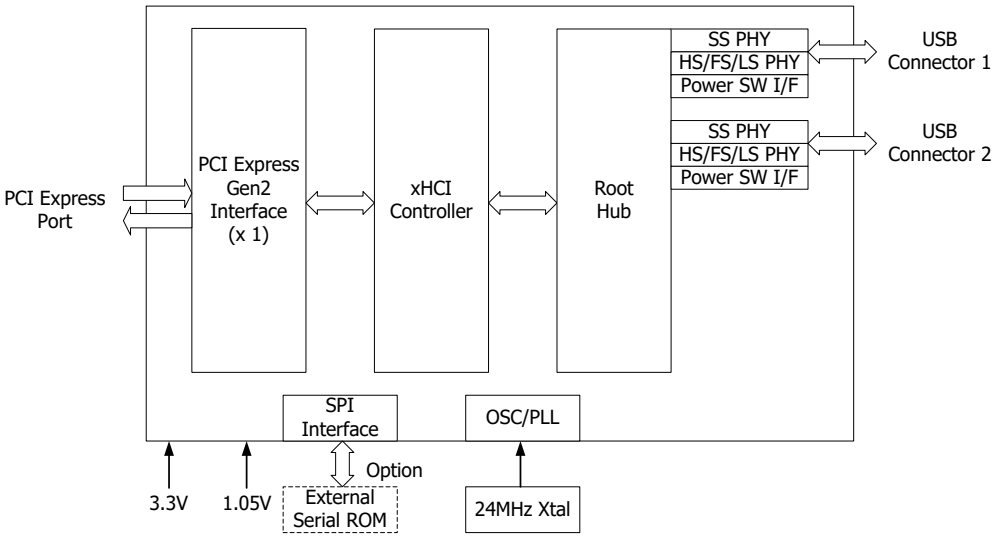



**Figure 1-2. μPD720202 Block Diagram**



| | |
|---|---|
| PCI Express Gen2 Interface | Complies with PCI Express Gen2 interface, with 1 lane. This block includes both the link and PHY layers. |
| xHCI Controller | Handles all support required for USB 3.0, SuperSpeed and Hi-/Full-/Low-Speed. This block includes the register interface from the system. |
| Root hub | Hub function in host controller. |
| SS PHY | For SuperSpeed Tx/Rx |
| HS/FS/LS PHY | For Hi-/Full-/Low-Speed Tx/Rx |
| Power SW I/F | Connected to external power switch for port power control and over current detection. |
| SPI Interface | Connected to external serial ROM. When system BIOS or system software does not support FW download function, the external serial ROM is required. |
| OSC | Internal oscillator block. |

## 1.5 Pin Configuration (TOP VIEW)

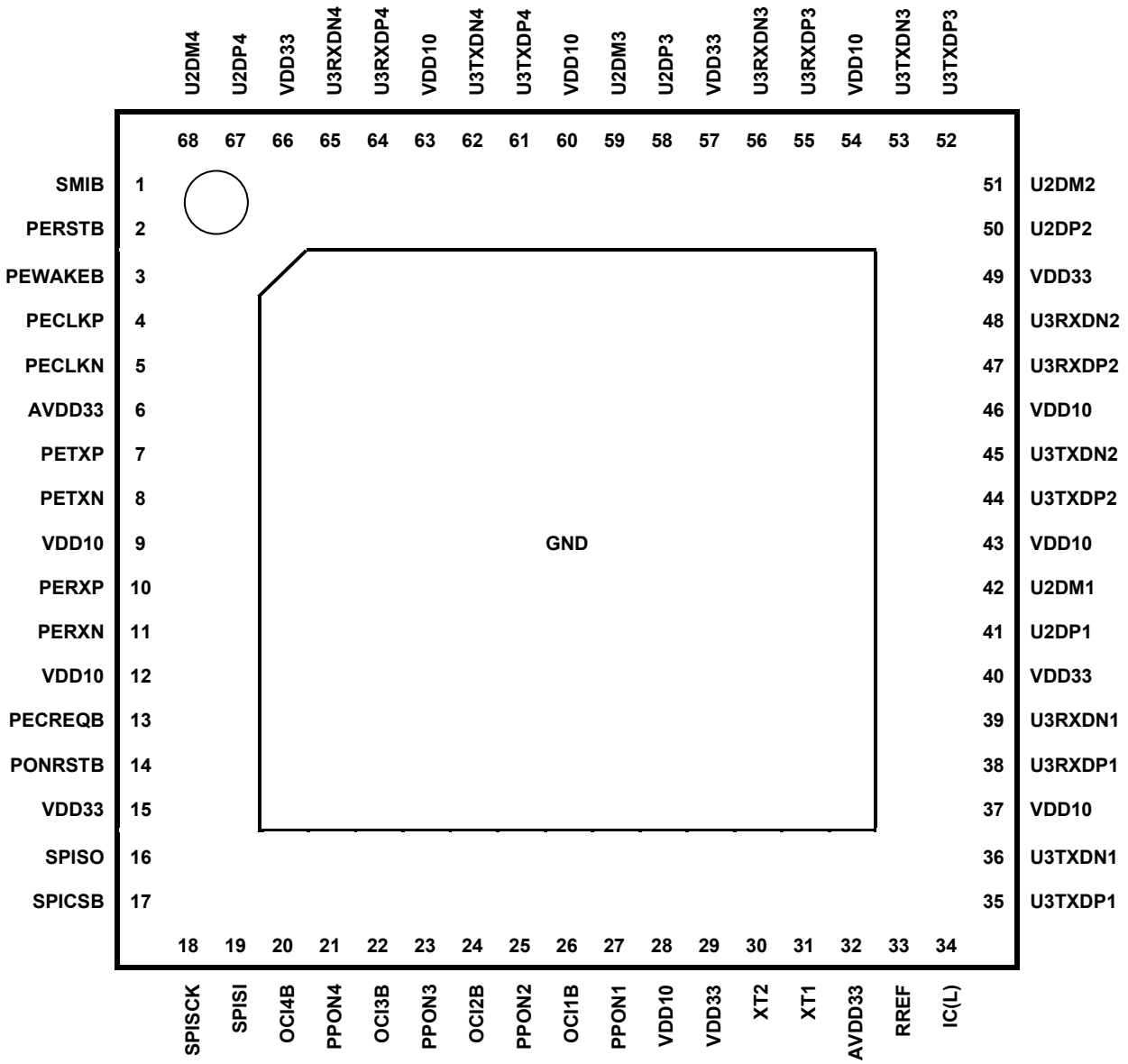
- **68-pin QFN (8 × 8)**
  μPD720201K8-701-BAC-A

  μPD720201K8-701-BAC-M1-A

  μPD720201K8-711-BAC-A

  μPD720201K8-711-BAC-M1-A

**Figure 1-3. Pin Configuration of μPD720201**



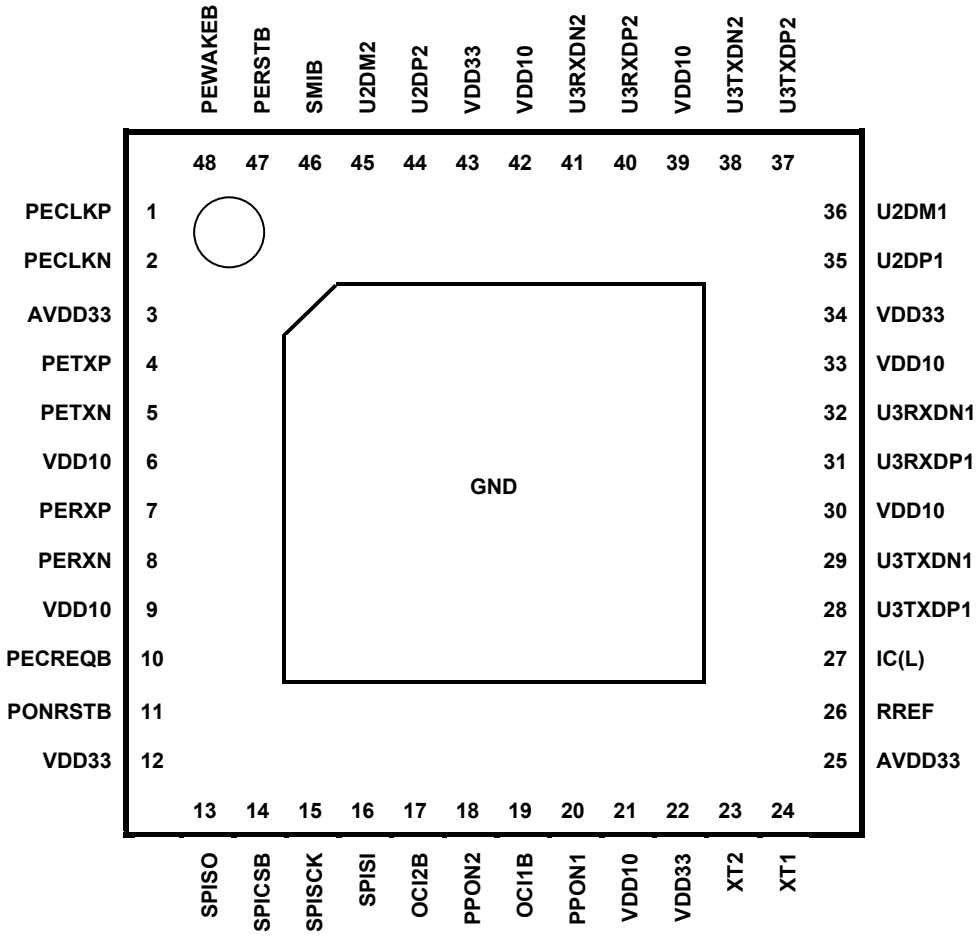
- **48-pin QFN (7 x 7)**
  μPD720202K8-701-BAA-A

  μPD720202K8-701-BAA-M1-A

  μPD720202K8-711-BAA-A

  μPD720202K8-711-BAA-M1-A

**Figure 1-4. Pin Configuration of μPD720202**



# 2. Pin Function

This section describes each pin functions.

## 2.1 Power supply

**Table 2-1. Power Supply**

| Pin Name | 720201 Pin No. | 720202 Pin No. | I/O Type | Function |
|---|---|---|---|---|
| VDD33 | 15, 29, 40, 49, 57, 66 | 12, 22, 34, 43 | Power | +3.3 V power supply |
| VDD10 | 9, 12, 28, 37, 43, 46, 54, 60, 63 | 6, 9, 21, 30, 33, 39, 42 | Power | +1.05 V power supply. |
| AVDD33 | 6, 32 | 3, 25 | Power | +3.3 V power supply for analog circuit. |
| GND | GND PAD | GND PAD | Power | Connect to ground. |
| IC(L) | 34 | 27 | I | Test pin. Connect to ground. |

## 2.2 Analog Signal

**Table 2-2. Analog Signal**

| Pin Name | 720201 Pin No. | 720202 Pin No. | I/O Type | Active Level | Function |
|---|---|---|---|---|---|
| RREF | 33 | 26 | USB2 | – | Reference resistor connection. |

## 2.3 System clock

**Table 2-3. System Clock**

| Pin Name | 720201 Pin No. | 720202 Pin No. | Type | Active Level | Function |
|---|---|---|---|---|---|
| XT1 | 31 | 24 | I (OSC) | – | Oscillator in<br>Connect to 24 MHz crystal. * |
| XT2 | 30 | 23 | O (OSC) | – | Oscillator out<br>Connect to 24 MHz crystal. * |

**Note 1:** An external modular oscillator cannot be used instead of a crystal, due to aggressive clock management in reduced power states.

### 2.3.1 System Interface signal

**Table 2-4. System Interface Signal**

| Pin Name | 720201 Pin No. | 720202 Pin No. | I/O Type | Active Level | Function |
|---|---|---|---|---|---|
| PONRSTB | 14 | 11 | I (3.3 V Schmitt Input) | Low | Power on reset signal. When supporting wakeup from D3cold, this signal should be pulled high with system auxiliary power supply. |
| SMIB | 1 | 46 | O (3.3 V Output) | Low | System management Interrupt signal. This is controlled with the USB Legacy Support Control/Status register. |

### 2.3.2 PCI Express Interface

**Table 2-5. PCI Express Interface**

| Pin Name | 720201 Pin No. | 720202 Pin No. | I/O Type | Active Level | Function |
|---|---|---|---|---|---|
| PECLKP | 4 | 1 | I (PCIE) | – | PCI Express 100 MHz Reference Clock. |
| PECLKN | 5 | 2 | I (PCIE) | – | PCI Express 100 MHz Reference Clock. |
| PETXP | 7 | 4 | O (PCIE) | – | PCI Express Transmit Data+. |
| PETXN | 8 | 5 | O (PCIE) | – | PCI Express Transmit Data-. |
| PERXP | 10 | 7 | I (PCIE) | – | PCI Express Receive Data+. |
| PERXN | 11 | 8 | I (PCIE) | – | PCI Express Receive Data-. |
| PERSTB | 2 | 47 | I (3.3 V Input) | Low | PCI Express “PERST#” signal. |
| PEWAKEB | 3 | 48 | O (Open Drain) | Low | PCI Express “WAKE#” signal. This signal is used for remote wakeup mechanism, and requests the recovery of power and reference clock input. |
| PECREQB | 13 | 10 | O (Open Drain) | Low | PCI Express “CLKREQ#” signal. This signal is used to request run/stop of reference clock. |

### 2.3.3 USB Interface

**Table 2-6. USB Interface**

| Pin Name | 720201 Pin No. | 720202 Pin No. | I/O Type | Active Level | Function |
|---|---|---|---|---|---|
| U3TXDP1 | 35 | 28 | O (USB3) | – | USB3.0 Transmit data D+ signal for SuperSpeed |
| U3TXDN1 | 36 | 29 | O (USB3) | – | USB3.0 Transmit data D- signal for SuperSpeed |
| U3RXDP1 | 38 | 31 | I (USB3) | – | USB3.0 Receive data D+ signal for SuperSpeed |
| U3RXDN1 | 39 | 32 | I (USB3) | – | USB3.0 Receive data D- signal for SuperSpeed |
| U2DP1 | 41 | 35 | I/O (USB2) | – | USB2.0 D+ signal for Hi-/Full-/Low-Speed |
| U2DM1 | 42 | 36 | I/O (USB2) | – | USB2.0 D– signal for Hi-/Full-/Low-Speed |
| OCI1B | 26 | 19 | I (3.3 V Input) | Low | Over-current status input signal.<br>0: Over-current condition is detected<br>1: No over-current condition is detected |
| PPON1 | 27 | 20 | O (3.3 V Output) | High | USB port power supply control signal.<br>0: Power supply OFF<br>1: Power supply ON |
| U3TXDP2 | 44 | 37 | O (USB3) | – | USB3.0 Transmit data D+ signal for SuperSpeed |
| U3TXDN2 | 45 | 38 | O (USB3) | – | USB3.0 Transmit data D- signal for SuperSpeed |
| U3RXDP2 | 47 | 40 | I (USB3) | – | USB3.0 Receive data D+ signal for SuperSpeed |
| U3RXDN2 | 48 | 41 | I (USB3) | – | USB3.0 Receive data D- signal for SuperSpeed |
| U2DP2 | 50 | 44 | I/O (USB2) | – | USB2.0 D+ signal for Hi-/Full-/Low-Speed |
| U2DM2 | 51 | 45 | I/O (USB2) | – | USB2.0 D– signal for Hi-/Full-/Low-Speed |
| OCI2B | 24 | 17 | I (3.3 V Input) | Low | Over-current status input signal.<br>0: Over-current condition is detected<br>1: No over-current condition is detected |
| PPON2 | 25 | 18 | O (3.3 V Output) | High | USB port power supply control signal.<br>0: Power supply OFF<br>1: Power supply ON |

| Pin Name | 720201 Pin No. | 720202 Pin No. | I/O Type | Active Level | Function |
|---|---|---|---|---|---|
| U3TXDP3 | 52 | – | O (USB3) | – | USB3.0 Transmit data D+ signal for SuperSpeed |
| U3TXDN3 | 53 | – | O (USB3) | – | USB3.0 Transmit data D- signal for SuperSpeed |
| U3RXDP3 | 55 | – | I (USB3) | – | USB3.0 Receive data D+ signal for SuperSpeed |
| U3RXDN3 | 56 | – | I (USB3) | – | USB3.0 Receive data D- signal for SuperSpeed |
| U2DP3 | 58 | – | I/O (USB2) | – | USB2.0 D+ signal for Hi-/Full-/Low-Speed |
| U2DM3 | 59 | – | I/O (USB2) | – | USB2.0 D– signal for Hi-/Full-/Low-Speed |
| OCI3B | 22 | – | I (3.3 V Input) | Low | Over-current status input signal.<br>0: Over-current condition is detected<br>1: No over-current condition is detected |
| PPON3 | 23 | – | O (3.3 V Output) | High | USB port power supply control signal.<br>0: Power supply OFF<br>1: Power supply ON |
| U3TXDP4 | 61 | – | O (USB3) | – | USB3.0 Transmit data D+ signal for SuperSpeed |
| U3TXDN4 | 62 | – | O (USB3) | – | USB3.0 Transmit data D- signal for SuperSpeed |
| U3RXDP4 | 64 | – | I (USB3) | – | USB3.0 Receive data D+ signal for SuperSpeed |
| U3RXDN4 | 65 | – | I (USB3) | – | USB3.0 Receive data D- signal for SuperSpeed |
| U2DP4 | 67 | – | I/O (USB2) | – | USB2.0 D+ signal for Hi-/Full-/Low-Speed |
| U2DM4 | 68 | – | I/O (USB2) | – | USB2.0 D– signal for Hi-/Full-/Low-Speed |
| OCI4B | 20 | – | I (3.3V Input) | Low | Over-current status input signal.<br>0: Over-current condition is detected<br>1: No over-current condition is detected |
| PPON4 | 21 | – | O (3.3V Output) | High | USB port power supply control signal.<br>0: Power supply OFF<br>1: Power supply ON |

**Note 1:** The SuperSpeed signals (U3TXDPx, U3TXDNx, U3RXDPx, U3RXDNx) and Hi-/Full-/Low-signals (U2DPx, U2DMx) of μPD720201 and μPD720202 shall be connected to the same USB connecter.

**Note 2:** The Timing of PPONx assertion is changed from μPD720200. The PPONx of μPD720200A, μPD720201 and μPD720202 are asserted after the software sets Max Device Slots Enable (MaxSlotsEn) field in Configure (CONFIG) register or Host Controller Reset (HCRST) flag in USBCMD register. On μPD720200, the PPON (2:1) are asserted immediately after the PCIe Reset.

### 2.3.4 SPI Interface

**Table 2-7. SPI Interface**

| Pin Name | 720201 Pin No. | 720202 Pin No. | Type | Active Level | Function |
|---|---|---|---|---|---|
| SPISCK | 18 | 15 | O (3.3 V output) | – | SPI serial flash ROM clock signal.<br>When the external serial ROM is not mounted, this signal should be pulled down through a pull-down resistor. |
| SPICSB | 17 | 14 | O (3.3 V output) | – | SPI serial flash ROM chip select signal.<br>When the external serial ROM is not mounted, this signal should be pulled down through a pull-down resistor. |
| SPISI | 19 | 16 | O (3.3 V output) | – | SPI serial flash ROM slave input signal.<br>When the external serial ROM is not mounted, this signal should be pulled down through a pull-down resistor. |
| SPISO | 16 | 13 | I (3.3 V Input) | – | SPI serial flash ROM slave output signal.<br>This signal should be pulled up through a pull-up resistor in all cases. |

# 3. Register Information

The μPD720201 and μPD720202 are implemented with the eXtensible Host Controller (xHCI) core that handles all speeds required for USB 3.0, SuperSpeed and Hi-/Full-/Low-Speed. The following sections show PCI configuration space and Memory Mapped I/O register information for the xHCI host controller. The number of valid ports is specified by "HCSPARAMS1" register in the Host Controller Capability Registers.

## 3.1 Register Attributes

The following notation is used to describe register access attributes.

**Table 3-1. Register and Register Bit-Field Types**

| Register Attribute | Description |
|---|---|
| HwInit | **Hardware Initialized:** Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial external ROM. Bits are read-only after initialization and may only be reset with a HCRST. |
| RO | **Read-only**: Register bits are read-only and cannot be altered by software. Register bits are permitted to be initialized by hardware and firmware mechanisms such as pin strapping or serial external ROM. |
| RWO | **Read-Write-once**: Register bits can be written only once after power up. After the first write, the bits become read only. |
| RW | **Read-Write**: Register bits are read-write and are permitted to be either Set or Cleared by software to the desired state. Note that individual bits in some read/write registers may be Read-Only. |
| RW1C | **Write-1-to-clear status**: Register bits indicate status when read. A set bit indicating a status event may be cleared by writing a '1'. Writing a '0' to RW1C bits has no effect. |
| RW1S | **Write-1-to-set status**: Register bits indicate status when read. A clear bit may be set by writing a '1'. Writing a '0' to RW1S bits has no effect. |
| RWS | **Sticky-Read-Write**: Register bits are read-write and are Set or Cleared by software to the desired state. Bits are only initialized or modified by hot reset. Where noted, registers that consume AUX power shall preserve sticky register values when AUX power consumption is enabled. In these cases, registers are not initialized or modified by hot, warm, or cold reset. |
| RW1CS | **Sticky-Write-1-to clear status**: Register bits indicate status when read. A set bit indicating a status event may be cleared by writing '1'. Writing a '0' to RW1CS bits has no effect. Bits are not initialized or modified by hot reset. Where noted, registers that consume AUX power shall preserve sticky register values when AUX power consumption is enabled. In these cases, registers are not initialized or modified by hot, warm, or cold reset. |
| Rsvd | **Reserved**: Reserved for future implementation. Rsvd registers or memory shall be treated as read-only by system software. Rsvd registers shall return '0' when read. Software shall ignore the value read from these bits. |

## 3.2 PCI Configuration Space

The configuration registers are accessed in order to set up hardware resources, device characteristics or operations, etc. in PCI Express. The following sections describe the PCI Configuration Space, which is the address space for the configuration registers. For more detailed description, see the **PCI Express Base Specification Revision 2.0.**

### 3.2.1 PCI Type 0 Configuration Space Header

**Table 3-2. PCI Type 0 Configuration Space Header**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| Device ID | | Vendor ID | | 00h |
| Status | | Command | | 04h |
| Class Code | | | Revision ID | 08h |
| BIST | Header Type | Latency Timer | Cache Line Size | 0Ch |
| Base Address Register #0 | | | | 10h |
| Base Address Register #1 | | | | 14h |
| Reserved | | | | 18h~28h |
| Subsystem ID | | Subsystem Vendor ID | | 2Ch |
| Reserved | | | | 30h |
| Reserved | | | Cap_Ptr | 34h |
| Reserved | | | | 38h |
| Max_Lat | Min_Gnt | Interrupt Pin | Interrupt Line | 3Ch |
| Reserved | | | | 40h~4Ch |
| PMC | | Next_Ptr | Cap_ID | 50h |
| Reserved | | PMSC | | 54h |
| Reserved | | | | 58h~5Ch |
| Reserved | | FLADJ | SBRN | 60h |
| Reserved | | | | 64h~6Ch |
| Reserved | FW Version | | Reserved | 6Ch |
| Message Control | | Next_Ptr | Cap_ID | 70h |
| MSI Address | | | | 74h |
| MSI Upper Address | | | | 78h |
| Reserved | | MSI Data | | 7Ch |
| MSI Mask Bits | | | | 80h |
| MSI Pending Bits | | | | 84h |
| Reserved | | | | 88h~8Ch |
| Message Control | | Next_Ptr | Cap_ID | 90h |
| Table Offset , Table BIR | | | | 94h |
| PBA Offset , PBA BIR | | | | 98h |
| Reserved | | | | 9Ch |
| PCI Express Capability | | Next_Ptr | Cap_ID | A0h |

| | | |
|---|---|---|
| Device Capability | | A4h |
| Device Status | Device Control | A8h |
| Link Capability | | ACh |
| Link Status | Link Control | B0h |
| Reserved | | B4h~C3h |
| Device Capability 2 | | C4h |
| Device Status 2 | Device Control 2 | C8h |
| Link Capability 2 | | CCh |
| Link Status 2 | Link Control 2 | D0h |
| Reserved | | D4h~DBh |
| PHY Control 0 | | DCh |
| PHY Control 1 | | E0h |
| PHY Control 2 | | E4h |
| Host Controller Configuration | | E8h |
| External ROM Information | | ECh |
| External ROM Configuration | | F0h |
| External ROM Write Control & Status | FW Download Control & Status | F4h |
| DATA 0 | | F8h |
| DATA 1 | | FCh |
| Advanced Error Reporting Enhanced Capability Header | | 100h |
| Uncorrectable Error Status Register | | 104h |
| Uncorrectable Error Mask Register | | 108h |
| Uncorrectable Error Severity Register | | 10Ch |
| Correctable Error Status Register | | 110h |
| Correctable Error Mask Register | | 114h |
| Advanced Error Capabilities and Control Register | | 118h |
| Header Log 1 | | 11Ch |
| Header Log2 | | 120h |
| Header Log3 | | 124h |
| Header Log4 | | 128h |
| Device Serial Number Enhanced Capability Header | | 140h |
| Serial Number Register (Lower DW) | | 144h |
| Serial Number Register (Upper DW) | | 148h |
| LTR Extended Capability Header | | 150h |
| Max No-Snoop Latency Register | Max Snoop Latency Register | 154h |

#### 3.2.1.1 Vendor ID Register

**Table 3-3. Vendor ID Register (Offset Address: 00h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Vendor ID | RO | 1912h | This is a 16-bit value. |

#### 3.2.1.2 Device ID Register

**Table 3-4. Device ID Register (Offset Address: 02h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Device ID | RO | 0014h (μPD720201)<br>0015h (μPD720202) | This is a 16-bit value. 0014h is assigned to μPD720201 and 0015h is assigned to μPD720202. |

#### 3.2.1.3 Command Register

**Table 3-5. Command Register (Offset Address: 04h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | I/O Space | RO | 0b | No support I/O space |
| 1 | Memory Space | RW | 0b | Controls response to memory access<br>0: Memory access disable<br>1: Memory access enable |
| 2 | Bus Master | RW | 0b | Controls the ability of a PCI Express Endpoint to issue Memory Read/Write Requests.<br>When Set, the PCI Express Function is allowed to issue Memory Requests. |
| 3 | Special Cycles | RO | 0b | Does not apply to PCI Express. |
| 4 | Memory Write and Invalidate Enable | RO | 0b | Does not apply to PCI Express. |
| 5 | VGA palette snoop | RO | 0b | Does not apply to PCI Express. |
| 6 | Parity Error response | RW | 0b | This bit controls the logging of poisoned TLPs in the Master Data Parity Error bit in the Status register. |
| 7 | Wait cycle control | RO | 0b | Does not apply to PCI Express. |
| 8 | SERR# enable | RW | 0b | When Set, this bit enables reporting of Non-fatal and Fatal errors detected by the Function to the Root Complex. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 9 | Fast back-to-back enable | RO | 0b | Does not apply to PCI Express. |
| 10 | Interrupt Disable | RW | 0b | Controls the ability of a PCI Express Function to generate INTx interrupts. When Set, Functions are prevented from asserting INTx interrupts. |
| 15 : 11 | Rsvd | - | - | Reserved. |

#### 3.2.1.4 Status Register

**Table 3-6. Status Register (Offset Address: 06h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 2 : 0 | Rsvd | - | - | Reserved. |
| 3 | Interrupt Status | RO | 0b | Shows Interrupt Status. When “Interrupt Disable” bit in PCI Command Register is set to 0b, the register shows the Interrupt Status. When “Interrupt Disable” is set to 1b; the register is invalid. |
| 4 | Capabilities List | RO | 1b | Indicates the presence of an Extended Capability list item. |
| 5 | 66 MHz capable | RO | 0b | Does not apply to PCI Express. |
| 6 | Rsvd | - | - | Reserved. |
| 7 | Fast back-to-back capable | RO | 0b | Does not apply to PCI Express. |
| 8 | Master Data Parity Error | RW1C | 0b | This bit is set if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs:<br>- Receive a Completion marked poisoned<br>- Poison a write Request.<br>If the Parity Error Response bit is 0b, this bit is never set. |
| 10 : 9 | DEVSEL timing | RO | 00b | Does not apply to PCI Express. |
| 11 | Signaled target abort | RW1C | 0b | This bit is set when a function completes a posted or non-posted request as a completer abort error. |
| 12 | Received target abort | RW1C | 0b | This bit is set when a requester receives a completion with completer abort completion status. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 13 | Received master abort | RW1C | 0b | This bit is set when a requester receives a completion with unsupported request completion status. |
| 14 | Signaled system error | RW1C | 0b | This bit is set when a function sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR# Enable bit in the Command register is 1b. |
| 15 | Detected parity error | RW1C | 0b | This bit is set by a function whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response bit in the Command register. |

#### 3.2.1.5 Revision ID Register

**Table 3-7. Revision ID Register (Offset Address: 08h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Revision ID | RO | 03h(μPD720201)<br>02h(μPD720202) | Revision ID. |

#### 3.2.1.6 Class Code Register

**Table 3-8. Class Code Register (Offset Address: 09h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Programming Interface | RO | 30h | USB3.0 host controller. |
| 15 : 8 | Sub Class | RO | 03h | Universal Serial Bus. |
| 23 : 16 | Base Class | RO | 0Ch | Serial Bus Controllers. |

#### 3.2.1.7 Cache Line Size Register

**Table 3-9. Cache Line Size Register (Offset Address: 0Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Cache Line Size | RW | 0h | Cache Line Size.<br>This field is implemented as a read-write field for legacy compatibility purposes but has no effect on this device behavior. |

#### 3.2.1.8 Latency Timer Register

**Table 3-10. Latency Timer Register (Offset Address: 0Dh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Latency Timer | RO | 0h | Does not apply to PCI Express. |

#### 3.2.1.9 Header Type Register

**Table 3-11. Header Type Register (Offset Address: 0Eh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Header Type | RO | 0h | Header Type 0. |

#### 3.2.1.10 BIST Register

**Table 3-12. BIST Register (Offset Address: 0Fh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | BIST | RO | 0h | BIST is not supported. |

#### 3.2.1.11 Base Address Register #0

**Table 3-13. Base Address Register #0 (Offset Address: 10h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Memory space Indicator | RO | 0b | Operational registers are mapped to main memory space. |
| 2 : 1 | Type | RO | 10b | Base register is 64bits wide and can be mapped anywhere in the 64-bit address space. |
| 3 | Prefetchable | RO | 0b | Prefetch is disabled. |
| 12 : 4 | Base address (LSB) | RO | 0h | Operational registers require 8Kbyte address space. |
| 31 : 13 | Base address (MSB) | RW | 0h | Indicates the high-order 19 bits of the base address in the Operational registers. |

#### 3.2.1.12 Base Address Register #1

**Table 3-14. Base Address Register #1 (Offset Address: 14h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Base address | RW | 0h | Indicates the high-order 32 bits of the base address in the Operational registers. |

#### 3.2.1.13 Subsystem Vendor ID Register

**Table 3-15. Subsystem Vendor ID Register (Offset Address: 2Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Subsystem Vendor ID | RWO | 0000h | This is written by BIOS or loaded from an External Serial Rom. After the first write, this register bits become read only.<br>This register is initialized to default value by the assertion of PONRSTB. |

#### 3.2.1.14 Subsystem ID Register

**Table 3-16. Subsystem ID Register (Offset Address: 2Eh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Subsystem ID | RWO | 0000h | This is written by BIOS or loaded from an External Serial ROM. After the first write, this register bits become read only.<br>This register is initialized to default value by the assertion of PONRSTB. |

#### 3.2.1.15 Capabilities Pointer Register

**Table 3-17. Capabilities Pointer Register (Offset Address: 34h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Capabilities Pointer | RO | 50h | Capability Pointer. |

#### 3.2.1.16 Interrupt Line Register

**Table 3-18. Interrupt Line Register (Offset Address: 3Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Interrupt Line | RW | 0h | Interrupt line's route |

#### 3.2.1.17 Interrupt Pin Register

**Table 3-19. Interrupt Pin Register (Offset Address: 3Dh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Interrupt Pin | RO | 01h | Routing to INTA# |

#### 3.2.1.18 Min_Gnt Register

**Table 3-20. Min_Gnt Register (Offset Address: 3Eh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Min_Gnt | RO | 0h | Does not apply PCI Express. |

#### 3.2.1.19 Max_LAT Register

**Table 3-21. Max_Lat Register (Offset Address: 3Fh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Max_Lat | RO | 0h | Does not apply PCI Express. |

#### 3.2.1.20 Serial Bus Release Number Register (SBRN)

This register contains the release of the Universal Serial Bus Specification with which this Universal Serial Bus Host Controller module is compliant.

**Table 3-22. SBRN Register (Offset Address: 60h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Serial Bus Specification Release Number | RO | 30h | Serial Bus Release Number Register. This register indicates the release number of the USB with which this controller is compliant. |

### 3.2.1.21 Frame Length Adjustment Register (FLADJ)

This register is the Auxiliary Power well. This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted for all USB buses implemented by an xHC. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system software (typically the BIOS). This register should only be modified when the HCHalted (HCH) bit in the USBSTS register is '1'. Changing the value of this register while the host controller is operating yield undefined results.

**Table 3-23. FLADJ Register (Offset Address: 61h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 5 : 0 | Frame Length Timing Value | RWS | 20h | Each decimal value change to this register corresponds to 16 Hi-Speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF microframe length) is equal to 59488 + value in this field. The default vale is decimal 32 (20h), which gives an SOF cycle time of 60000.<br>Frame Length / FLADJ Value<br>59488 / 0<br>…<br>59984 / 31<br>60000 / 32<br>…<br>60496 / 63 |
| 7 : 6 | Rsvd | - | - | Reserved. |

### 3.2.2 PCI Power Management Capabilities

#### 3.2.2.1 Capabilities List Register

**Table 3-24. Capabilities List Register (Offset Address: 50h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Cap_ID | RO | 01h | ID for PCI Power Management reg. |
| 15 : 0 | Next_Ptr | RO | 70h | Next Capability Pointer. |

#### 3.2.2.2 Power Management Capabilities Register (PMC)

**Table 3-25. PMC Register (Offset Address: 52h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 2 : 0 | Version | RO | 11b | Supports PCI Power Management Interface Specification release 1.2 |
| 3 | PME Clock | RO | 0b | Does not apply to PCI Express. |
| 4 | Rsvd | - | - | Reserved. |
| 5 | DSI | RO | 0b | Does not required Specific Initialization before the generic class device driver is able to use it. |
| 8 : 6 | Aux_Current | HwInit | 111b | Indicates current requirement.<br>If the AUXDET in HCConfigration register is ‘0b’, this field returns a value of “000b” when read.<br>If the AUXDET in HCConfiguration register is ‘1b’, following assignments apply:<br>Bit 3.3Vaux<br>8 7 6 Max. Current Required<br>1 1 1 375 mA<br>1 1 0 320 mA<br>1 0 1 270 mA<br>1 0 0 220 mA<br>0 1 1 160 mA<br>0 1 0 100 mA<br>0 0 1 55 mA<br>0 0 0 0 (self powerd) |
| 9 | D1_support | RO | 0b | No Support. |
| 10 | D2_support | RO | 0b | No Support. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 11 | PME_support | HwInit | X1001b | If the AUXDET in HCConfiguration register is set to '1b', bit 15 is set to '1'.<br>This 5-bit field indicates the power states in which the function may send PME Message. A value of 0b for any bit indicates that the function is not capable of sending the PME Message while in that power state.<br>PME Message can be sent from D0 and D3hot. |

### 3.2.2.3 Power Management Status / Control Register (PMSC)

**Table 3-26. PMSC Register (Offset Address: 54h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 1 : 0 | Power State | RW | 0b | This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below.<br>00b : D0<br>11b : D3<br>In case of transitioning from D0 to D3, Run/Stop in USBCMD register should be 0b, and HCHalted in USBSTS register is 1b.<br>If Run/Stop is 1b and HCHalted is 0b and Power State is set from D0 to D3, the behavior of μPD720201/ μPD720202 is undefined. |
| 2 | Rsvd | - | - | Reserved. |
| 3 | No_Soft_Reset | RO | 1b | This bit indicates that devices transitioning from D3hot to D0 do not perform an internal reset. Configuration Context is preserved. Upon transition from D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. |
| 7 : 4 | Rsvd | - | - | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 8 | PME Enable | RWS | 0b | A ‘1‘ enables the function to send PME Message. When ‘0‘, PME Message is disabled. |
| 12 : 9 | Data Select | RO | 0b | No support. |
| 14 : 13 | Data Scale | RO | 0b | No support. |
| 15 | PME Status | RW1CS | 0b | This bit is set when the function would send the PME message if enabled to do so. This bit is independent of the state of PME Enable bit.<br>Writing a ‘1’ to this bit will clear it and cause the function to stop sending PME message. Writing a ‘0’ has no effect. |

### 3.2.3 MSI Capabilities

#### 3.2.3.1 Capabilities List Register for MSI

**Table 3-27. Capabilities List Register (Offset Address: 70h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Cap_ID | RO | 05h | ID for MSI Capability reg. |
| 15 : 8 | Next_Ptr | RO | 90h | Pointer to the next capabilities list. |

#### 3.2.3.2 Message Control for MSI

**Table 3-28. Message Control Register (Offset Address: 72h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | MSI Enable | RW | 0b | If 1 and MSI-X Enable bit is 0, the function is permitted to use MSI. |
| 3 : 1 | Multiple Message Capable | RO | 11b | Supports 8 request vectors. |
| 6 : 4 | Multiple Message Enable | RW | 0b | System software writes to this field to indicate the number of allocated vectors. |
| 7 | 64bit address capable | RO | 1b | This is capable of sending 64bit message address. |
| 8 | Per-vector masking capable | RO | 0b | Does not support MSI per-vector masking. |
| 15 : 9 | Rsvd | - | - | Reserved. |

#### 3.2.3.3 Message Address for MSI

**Table 3-29. Message Address Register (Offset Address: 74h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 1 : 0 | Rsvd | - | - | Reserved. |
| 31 : 2 | MSI Address | RW | 0h | System-specified message address. |

#### 3.2.3.4 Message Upper Address for MSI

**Table 3-30. Message Upper Address Register (Offset Address: 78h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | MSI Upper Address | RW | 0h | System-specified message address. |

#### 3.2.3.5 Message Data for MSI

**Table 3-31. Message Data Register (Offset Address: 7Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | MSI Data | RW | 0h | System-specified message data. |

#### 3.2.3.6 Mask Bits for MSI

**Table 3-32. Mask Bits Register (Offset Address: 80h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | MSI Mask bits | RW | 0h | For each Mask bit that is set, the function is prohibited from sending the associated message. |

#### 3.2.3.7 Pending Bits for MSI

**Table 3-33. Pending Bits Register (Offset Address: 84h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | MSI Pending bits | RO | 0h | Does not support MSI Pending bits. |

### 3.2.4 MSI-X Capabilities

#### 3.2.4.1 Capabilities List Register for MSI-X

**Table 3-34. Capabilities List Register (Offset Address: 90h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Cap_ID | RO | 11h | ID for MSI-X Capability reg. |
| 15 : 8 | Next_Ptr | RO | A0h | Pointer to the next capabilities list. |

#### 3.2.4.2 Message Control for MSI-X

**Table 3-35. Message Control Register (Offset Address: 92h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 10 : 0 | Table Size | RO | 111b | MSI-X Table Size. This controller supports 8 entries. |
| 13 : 11 | Rsvd | - | - | Reserved. |
| 14 | Function Mask | RW | 0b | If 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states.<br>If 0, each vector's mask bit determines whether the vector is masked or not. |
| 15 | MSI-X Enable | RW | 0b | If 1 and the MSI Enable bit in the MSI Message Control register is 0, the function is permitted to use MSI-X. |

#### 3.2.4.3 Table Offset / Table BIR for MSI-X

**Table 3-36. Table Offset / Table BIR Register (Offset Address: 94h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Table Offset | RO | 1000h | Indicates that MSI-X table is located at BaseAddress + 1000h. |

#### 3.2.4.4 PBA Offset for MSI-X

**Table 3-37. Message Upper Address Register (Offset Address: 98h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | PBA Offset | RO | 1080h | Indicates that MSI-X table is located at BaseAddress + 1080h . |

### 3.2.5 PCI Express Extended Capabilities

#### 3.2.5.1 PCI Express Capabilities List Register

**Table 3-38. PCI Express Capabilities List Register (Offset Address: A0h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Cap_ID | RO | 10h | ID for PCI Express Capability reg. |
| 15 : 8 | Next_Ptr | RO | 0h | Pointer to the next capabilities list. |

#### 3.2.5.2 PCI Express Capabilities Register

**Table 3-39. PCI Express Capabilities Capability Register (Offset Address: A2h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Capability Version | RO | 10b | Indicates PCI-SIG defined PCI Express Capability structure version number. |
| 7 : 4 | Device / Port Type | RO | 0b | Indicates PCI Express Endpoint. |
| 8 | Slot Implemented | RO | 0b | This field is invalid for PCI Express Endpoint. |
| 13 : 9 | Interrupt Message Number | RO | 0b | Indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this capability structure. |
| 15 : 14 | Rsvd | - | - | Reserved. |

#### 3.2.5.3 Device Capabilities Register

**Table 3-40. Device Capabilities Register (Offset Address: A4h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 2 : 0 | Max_Payload_Size Supported | RO | 0b | Indicates the maximum payload size that the Function can support for TLPs. μPD720201/μPD720202 support 128bytes max payload size. |
| 4 : 3 | Phantom Functions Supported | RO | 0b | Does not support Phantom Functions. |
| 5 | Extended Tag Field Supported | RO | 0b | Indicates the maximum supported size of Tag field as a Requester.μPD720201/μPD720202 support 5-bit Tag field. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 8 : 6 | Endpoint L0s Acceptable Latency | RO | 111b | Indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. 111b is no limit. |
| 11 : 9 | Endpoint L1 Acceptable Latency | RO | 111b | Indicates the acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. 111b is no limit. |
| 14 : 12 | Rsvd | - | - | Reserved. |
| 15 | Role-Based Error Reporting | RO | 1b | Supports Error Reporting functionality. |
| 17 : 16 | Rsvd | - | - | Reserved. |
| 25 : 18 | Captured Slot Power Limit Value | RO | 0b | In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. |
| 27 : 26 | Captured Slot Power Limit Scale | RO | 0b | Specifies the scale used for the Slot Power Limit Value. |
| 28 | Function Level Reset Capability | RO | 0b | Optional Function Level Reset mechanism is not supported. |
| 31 : 29 | Rsvd | - | - | Reserved. |

#### 3.2.5.4 Device Control Register

**Table 3-41. Device Control Register (Offset Address: A8h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Correctable Error Reporting Enable | RW | 0b | This bit, in conjunction with other bits, controls sending ERR_COR Message. |
| 1 | Non-Fatal Error Reporting Enable | RW | 0b | This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages. |
| 2 | Fatal Error Reporting Enable | RW | 0b | This bit, in conjunction with other bits, controls sending ERR_FATAL Messages. |
| 3 | Unsupported Request Reporting Enable | RW | 0b | This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending Error Messages. |
| 4 | Enable Relaxed Ordering | RW | 1b | μPD720201/μPD720202 are permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 5 | Max_Payload_Size | RW | 0b | This field sets maximum TLP payload seize for μPD720201/μPD720202. |
| 8 | Extended Tag Field Enable | RO | 0b | Does not support this capability. |
| 9 | Phantom Function Enable | RO | 0b | Does not support this capability. |
| 10 | Auxiliary (AUX) Power PM Enable | RWS | 0b | When set this bit, enables a Function to draw AUX power independent of PME AUX power. |
| 11 | Enable No Snoop | RW | 1b | If this bit is Set, μPD720201/μPD720202 are permitted to Set the No snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. |
| 14 : 12 | Max_Read_Request_Size | RW | 010b | This field sets the maximum Read Request size for the Function as a Requester. |
| 15 | Initiate Function Level Reset | RW | 0b | A write of 1b initiates Function Level Reset to the Function. The value read by software from this bit is always 0b. |

### 3.2.5.5 Device Status Register

**Table 3-42. Device Status Register (Offset Address: AAh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Correctable Error Detected | RW1C | 0b | This bit indicates status of correctable errors detected. |
| 1 | Non-Fatal Error Detected | RW1C | 0b | This bit indicates status of Non-Fatal errors detected. |
| 2 | Fatal Error Detected | RW1C | 0b | This bit indicates status of Fatal errors detected. |
| 3 | Unsupported Request Detected | RW1C | 0b | This bit indicates that μPD720201/μPD720202 received an Unsupported Request. |
| 4 | AUX Power Detected | RO | HwInit | If the AUXDET bit in HCConfiguration register is set to 1b, this bit is set to1. |
| 5 | Transactions Pending | RO | 0b | When set, this bit indicates that μPD720201/μPD720202 has issued Non-Posted Requests that have not been completed. |
| 15 : 6 | Rsvd | - | - | Reserved |

### 3.2.5.6 Link Capabilities Register

**Table 3-43. Link Capabilities Register (Offset Address: ACh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Supported Link Speeds | RO | 10b | This field indicates the supported Link speeds of the associated Port. μPD720201/μPD720202 supports 5.0GT/s and 2.5GT/s Link speeds. |
| 9 : 4 | Maximum Link Width | RO | 1b | This field indicates the maximum Link width. μPD720201/μPD720201 supports 1Lane. |
| 11 : 10 | Active State Power Management(ASPM) Support | RO | 11b | This field indicates the level of ASPM supported on the given PCI Express Link. |
| 14 : 12 | L0s Exit Latency | RO | 110b | This field indicates the L0s exit latency for the given PCI Express Link. 110b indicates 2us-4us. |
| 17 : 15 | L1 Exit Latency | RO | 111b | This field indicates the L1 exit latency for the given PCI Express Link. 111b indicates more than 64us. |
| 18 | Clock Power Management | RO | 1b | 1b indicates that the component tolerates the removal of any reference clock via the " clock request"(CLKREQ#) mechanism when the Link is in the L1 states. |
| 21 : 19 | Rsvd | - | - | Reserved. |
| 31 : 24 | Port Number | RO | 0b | This field indicates the PCI Express Port number for the given PCI Express Link. |

### 3.2.5.7 Link Control Register

**Table 3-44. Link Control Register (Offset Address: B0h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 1 : 0 | Active State Power Management(ASPM) Control | RW | HwInit | This field controls the level of ASPM supported on the given PCI Express Link. If the PSEL bit in HCConfiguration register is set to 0b, default value is 11b.<br>00b : Disabled<br>01b : L0s Entry Enabled<br>10b : L1 Entry Enabled<br>11b : L0s and L1 Entry enabled |
| 2 | Rsvd | - | - | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 | Read Completion Boundary (RCB) | RO | 0b | Read Completion Boundary is 64byte. |
| 4 | Link Disable | RO | 0b | This bit disables the Link by directing the LTSSM to the Disable state when Set. This bit is reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. |
| 5 | Retrain Link | RO | 0b | This bit is not applicable and is reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read. |
| 6 | Common Clock Configuration | RW | 0b | When Set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. |
| 7 | Extended Sync | RW | 0b | When Set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state and when in the Recovery state. |
| 8 | Enable Clock Power Management | RW | 1b | 0b: Clock power management is disabled and μPD720201/μPD720202 hold CLKREQ# signal low.<br>1b: When this bit is Set, μPD720201/μPD720202 are permitted to use CLKREQ# signal to power manage Link clock according to protocol defined in appropriate form factor specification.<br>If the CLKREQFORCE bit in HCConfiguration register is '1', CLKREQ# signal always is held low although Enable Clock Power Management bit is '1'. |
| 9 | Hardware Autonomous Width Disable | RO | 0b | Disables hardware from changing the Link width. |
| 15 : 10 | Rsvd | - | - | Reserved. |

#### 3.2.5.8 Link Status Register

**Table 3-45. Link Status Register (Offset Address: B2h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Current Link Speed | RO | 1b | This field indicates the negotiated Link speed of the given PCI Express Link.<br>0001b : 2.5GT/s PCI Express Link<br>0010b : 5.0GT/s PCI Express Link |
| 9 : 4 | Negotiated Link Width | RO | 1b | This field indicates the negotiated width of the given PCI Express Link. |
| 11 : 10 | Rsvd | - | - | Reserved. |
| 12 | Slot Clock Configuration | RO | 1b | This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. |
| 13 | Data Link Layer Link Active | RO | 0b | This bit indicates the status of the Data Link Control and Management State Machine. It returns a ‘1’b to indicate the DL_Active state, ‘0’b otherwise. |
| 15 : 14 | Rsvd | - | - | Reserved. |

#### 3.2.5.9 Device Capabilities 2 Register

**Table 3-46. Device Capabilities 2 Register (Offset Address: C4h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Completion Timeout Ranges Supported | RO | 0b | Completion Timeout programming not supported. |
| 4 | Completion Timeout Disable Supported | RO | 1b | Indicates support for the Completion Timeout Disable mechanism. |
| 10 : 5 | Rsvd | - | - | Reserved. |
| 11 | LTR Mechanism Supported | RO | 1b | Indicates support for the Latency Tolerance Reporting (LTR) mechanism capability. |
| 31 : 12 | Rsvd | - | - | Reserved. |

#### 3.2.5.10 Device Control 2 Register

**Table 3-47. Device Control 2 Register (Offset Address: C8h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Completion Timeout Value | RW | 0b | Default range : 50us to 50ms. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 4 | Completion Timeout Disable | RW | 0b | When Set, this bit disables the Completion Timeout mechanism. |
| 9 : 5 | Rsvd | - | - | Reserved. |
| 10 | LTR Mechanism Enable | RW | 0b | When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. |
| 15 : 11 | Rsvd | - | - | Reserved. |

#### 3.2.5.11 Device Status 2 Register

**Table 3-48. Device Status 2 Register (Offset Address: CAh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Rsvd | - | - | Reserved. |

#### 3.2.5.12 Link Capabilities 2 Register

**Table 3-49. Link Capabilities 2 Register (Offset Address: CCh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Rsvd | - | - | Reserved. |

#### 3.2.5.13 Link Control 2 Register

**Table 3-50. Link Control 2 Register (Offset Address: D0h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Target Link Speed | RWS | 10b | This field is used to set the target compliance mode speed when software is using the Enter Compliance bit to force a Link into compliance mode.<br>0010b : 5.0GT/s Target Link Speed |
| 4 | Enter Compliance | RWS | 0b | Software is permitted to force a Link to enter Compliance mode at the Target Link Speed by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 5 | Hardware Autonomous Speed Disable | RWS | 0b | When Set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. |
| 6 | Rsvd | - | - | Reserved. |
| 9 : 7 | Transmit Margin | RWS | 0b | This field controls the value of the non-deemphasized voltage level at the Transmitter pins. This register is intended for debug, compliance testing purposes only. |
| 10 | Enter Modified Compliance | RWS | 0b | When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. |
| 11 | Compliance SOS | RWS | 0b | When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns,. |
| 12 | Compliance De-emphasis | RWS | 0b | This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. |

### 3.2.5.14 Link Status 2 Register

**Table 3-51. Link Status 2 Register (Offset Address: D2h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Current De-emphasis Level | RO | 1b | When the Link is operating at 5GT/s speed, this bit reflects the level of de-emphasis.<br>1b : -3.5dB<br>0b : -6dB |
| 15 : 1 | Rsvd | - | - | Reserved. |

### 3.2.6 RENESAS Specific Registers

#### 3.2.6.1 FW Version Register

**Table 3-52. FW Register (Offset Address: 6Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Rsvd. | RO | HwInit | Reserved |
| 15 : 8 | FW Version Low | RO | HwInit | FW Version Low. |
| 23 : 16 | FW Version High | RO | HwInit | FW Version High. |
| 31 : 24 | Rsvd | RO | HwInit | Reserved |

#### 3.2.6.2 PHY Control 0 Register

**Table 3-53. PHY Control 0 Register (Offset Address: DCh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Rsvd. | RW | HwInit | Reserved |

#### 3.2.6.3 PHY Control 1 Register

**Table 3-54. PHY Control 1 Register (Offset Address: E0h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Rsvd | RW (μPD720201)<br>Rsvd (μPD720202) | HwInit | Reserved |

#### 3.2.6.4 PHY Control 2 Register

**Table 3-55. PHY Control 2 Register (Offset Address: E4h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| μPD720201 | | | | |
| 3 : 0 | BC_MODE_P1 | RW | 0000b | Battery charging port type for PORT1. Can be set to one of the following:.<br>0000b : SDP only<br>0001b : CDP only<br>0010b : SDP – DCP<br>0011b : CDP – DCP<br>0100b : SDP – FVO1<br>0101b : CDP – FVO1<br>0110b : SDP – FVO2<br>0111b : SDP – FVO2<br>1111b – 1000b : Reserved |
| 7 : 4 | BC_MODE_P2 | RW | 0000b | Battery charging port type for PORT2. Can be set to one of the values listed for bits 3:0 above. |
| 11 : 8 | BC_MODE_P3 | RW | 0000b | Battery charging port type for PORT3. Can be set to one of the values listed for bits 3:0 above. |
| 15 : 12 | BC_MODE_P4 | RW | 0000b | Battery charging port type for PORT4. Can be set to one of the values listed for bits 3:0 above. |
| 17 : 16 | TRTFCTL_P1 | RW | 01b | Hi-Speed Eye Tr/Tf fine control for PORT1.<br>00b : -1 (make low pitch)<br>01b : 0 (default)<br>10b : +1<br>11b : +2 (make steep pitch) |
| 19 : 18 | TRTFCTL_P2 | RW | 01b | Hi-Speed Eye Tr/Tf fine control for PORT2.<br>00b : -1 (make low pitch)<br>01b : 0 (default)<br>10b : +1<br>11b : +2 (make steep pitch) |
| 21 : 20 | TRTFCTL_P3 | RW | 01b | Hi-Speed Eye Tr/Tf fine control for PORT3.<br>00b : -1 (make low pitch)<br>01b : 0 (default)<br>10b : +1<br>11b : +2 (make steep pitch) |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 23 : 22 | TRTFCTL_P4 | RW | 01b | Hi-Speed Eye Tr/Tf fine control for PORT4.<br>00b : -1 (make low pitch)<br>01b : 0 (default)<br>10b : +1<br>11b : +2 (make steep pitch) |
| 31 : 24 | Rsvd | Rsvd | HwInit | Reserved |
| μPD720202 | | | | |
| 3 : 0 | BC_MODE_P1 | RW | 0000b | Battery charging port type for PORT1. Can be set to one of the following:<br>0000b : SDP only<br>0001b : CDP only<br>0010b : SDP – DCP<br>0011b : CDP – DCP<br>0100b : SDP – FVO1<br>0101b : CDP – FVO1<br>0110b : SDP – FVO2<br>0111b : SDP – FVO2<br>1111b – 1000b : Reserved |
| 7 : 4 | BC_MODE_P2 | RW | 0000b | Battery charging port type for PORT2. Can be set to one of the values listed for bits 3:0 above. |
| 15 : 8 | Rsvd | Rsvd | 0b | Reserved |
| 19 : 16 | TRTFCTL_P1P2 | RW | 0011b | Hi-Speed Eye Tr/Tf fine control for PORT1.<br>X0X0b : -1 (make low pitch)<br>X0X1b : 0 (default)<br>X1X0b : +1<br>X1X1b : +2 (make steep pitch)<br>Hi-Speed Eye Tr/Tf fine control for PORT2.<br>0X0Xb : -1 (make low pitch)<br>0X1Xb : 0 (default)<br>1X0Xb : +1<br>1X1Xb : +2 (make steep pitch)<br>Note.“X” means “don’t care” |
| 31 : 20 | Rsvd | Rsvd | 0b | Reserved |

### 3.2.6.5 Host Controller Configuration (HCConfiguration) Register

**Table 3-56. HCConfiguration Register (Offset Address: E8h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Rsvd | RW | 0b | Reserved. |
| 8 | DeviceNonRemoval1 Enable | RW | 0b | When set to'1b', the μPD720201 forces the Device Removal(DR) bit to '1b' in both the PORT1 PORTSC and PORT5 PORTSC. The μPD720202 forces the DR bit to '1b' in both the PORT1 PORTSC and PORT3 PORTSC. |
| 9 | DeviceNonRemoval2 Enable | RW | 0b | When set to'1b', the μPD720201 forces the Device Removal(DR) bit to '1b' in both the PORT2 PORTSC and PORT6 PORTSC. The μPD720202 forces the DR bit to '1b' in both the PORT2 PORTSC and PORT4 PORTSC. |
| 10 | DeviceNonRemoval3 Enable | RW | 0b | When set to'1b', the μPD720201 forces the Device Removal(DR) bit to '1b' in both the PORT3 PORTSC and PORT7 PORTSC. |
| 11 | DeviceNonRemoval4 Enable | RW | 0b | When set to'1b', the μPD720201 forces the Device Removal(DR) bit to '1b' in both the PORT4 PORTSC and PORT8 PORTSC. |
| 15 : 12 | Reserved | RW | 0000b | Reserved. |
| 16 | UsePPON | RW | 1b | When set to '0b', the μPD720201 and μPD720202 force the Port Power Control (PPC) bit to '0b' in the HCCPARAMS register. When VBUS is not controlled by the PPON pin, this bit should be set to '0b'. |
| 18 : 17 | DisablePortCount | RW | 00b | μPD720201<br>00b :All ports are enabled.<br>01b : Port 4 and Port 8 are disabled.<br>10b : Port 3,4,7 and 8 are disabled.<br>11b : Port 2,3,4,6,7 and 8 are disabled.<br><br>μPD720202<br>00b : All ports are enabled.<br>01b : Port 2 and 4 are disabled. |
| 23 : 19 | Reserved | RW | 00000b | Reserved. |
| 24 | PSEL | RW | 1b | When set to '1b', the default value of the Active State Power Management Control fields in the PCI Express Link Control Register is 00b. When this bit is '0b', the default value is 11b. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 25 | Reserved | RW | 0b | Reserved. |
| 26 | AUXDET | RW | 1b | Auxiliary Power Detect. When the system supports remote wakeup from D3cold, this bit should be set to '1b'. |
| 27 | CLKREQ Force Disable | RW | 0b | When set to '1b', μPD720201 and μPD720202 force the CLKREQ# disabled. |
| 28 | SerialNumber Capability Enable | RW | 0b | When set to '1b', Serial Number Capability area is enabled. |
| 31 : 29 | Reserved | RW | 0b | Reserved. |

### 3.2.6.6 External ROM Information Register

**Table 3-57. External ROM Information Register (Offset Address: ECh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | ROM Information | RO | 0000h | When system has mounted the External ROM, HW will set the External ROM ID. |

### 3.2.6.7 External ROM Configuration Register

**Table 3-58. External ROM Configuration Register (Offset Address: F0h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | ROM Parameter | RW | 0000h | To access the External ROM, the software must set the ROM Parameter.<br>Refer to section 6.2. |

### 3.2.6.8 FW Download Control and Status Register

**Table 3-59. FW Download Control and Status Register (Offset Address: F4h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | FW Download Enable | RW | 0b | When set to ‘1b’, DATA0 and DATA1 register are enabled for FW download by BIOS. When FW download is completed, this bit must be set to ‘0b’. After setting ‘0b’, Result Code field is updated. |
| 1 | FW Download Lock | RW1S | 0b | When set to ‘1b’, FW Download process never operates even if FW Download Enable is ‘1b’. Once set, this bit remains ‘1b’ until PONRSTB is asserted. |
| 3 : 2 | Reserved | RO | 00b | Reserved |
| 6 : 4 | Result Code | RO | 0b | This field shows the result of FW Download.<br>000b : Invalid (no result yet)<br>001b : Success<br>010b : Error<br>111b ~ 011b : Reserved. |
| 7 | Reserved | RO | 0b | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 8 | Set DATA0 | RW1S | 0b | When set to '1b', a download request is initiated to the μPD720201/μPD720202. Before set to '1b', FW data shall be written in the Data0 Register. When Data0 download is completed, this bit is automatically cleared to '0b'. |
| 9 | Set DATA1 | RW1S | 0b | When set to '1b', a download request is initiated to the μPD720201/μPD720202. Before set to '1b', FW data shall be written in the Data1 Register. When Data1 download is completed, this bit is automatically cleared to '0b'. |
| 15 : 10 | Reserved | RO | 000000b | Reserved. |

### 3.2.6.9 External ROM Access Control and Status Register

**Table 3-60. FW Control and Status Register (Offset Address: F6h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | External ROM Access Enable | RW | 0b | When set to '1b', accessing an external ROM is enabled. It is prohibited to set both this bit and FW Download Enable to '1b' at the same time. Before writing '1b' to this bit, the DATA0 register must be set to 53524F4Dh to enable FW writing. |
| 1 | External ROM Erase | RW | 0b | When this bit is set to '1b', External ROM Data is erased. When this operation is complete, this bit is cleared to '0b' automatically. Before writing '1b' to this bit, the DATA0 register must be set to 5A65726Fh. |
| 2 | Reload | RW | 0b | When this bit is set to '1b', External ROM Data is reloaded. This function is used when immediate reload is required after External ROM is updated. At the completion of reload process, this bit is cleared to '0b' automatically. |
| 3 | Reserved | RO | 0b | Reserved |
| 6 : 4 | Result Code | RO | 000b | This field shows the result of External ROM update process.<br>000b : Invalid (no result yet)<br>001b : Success<br>010b : Error<br>111b~011b : Reserved. |
| 7 | Reserved | RO | 0b | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 8 | Set DATA0 | RW1S | 0b | When set to'1b', External ROM Write Request is initiated. Before setting to '1b', FW data shall be written in the DATA0 register. When the data0 download is completed, this bit is automatically cleared to '0b'. Setting Get Data0 or Get DATA1 while Set DATA0 is '1b' results in undefined behavior. |
| 9 | Set DATA1 | RW1S | 0b | When set to'1b', External ROM Write Request is initiated. Before setting to '1b', FW data shall be written in the DATA1 register. When the data1 download is completed, this bit is automatically cleared to '0b'. Setting Get Data0 or Get DATA1 while Set DATA1 is '1b' results in undefined behavior. |
| 10 | Get DATA0 | RW1S | 0b | When set to'1b', External ROM Read Request is initiated. This bit is automatically cleared to '0b' when valid data is available in the Data0 register. Setting Set Data0 or Set DATA1 while Get DATA0 is '1b' results in undefined behavior. |
| 11 | Get DATA1 | RW1S | 0b | When set to'1b', External ROM Read Request is initiated. This bit is automatically cleared to '0b' when valid data is available in the Data1 register. Setting Set Data0 or Set DATA1 while Get DATA1 is '1b' results in undefined behavior. |
| 14 : 12 | Reserved | RO | 000b | Reserved |
| 15 | External ROM Exists | RO | HwInit | Indicates that the External ROM is connected. Even if the external ROM exists, FW can be downloaded from External ROM . In this case, FW in the xHC is overwritten by FW download data.<br>1 : External ROM Exists<br>0 : No External ROM Exists |

### 3.2.6.10 DATA0 Register

**Table 3-61. DATA0 Register (Offset Address: F8h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | DATA0 | RW | 0000h | This register is a window to write and read FW data. |

#### 3.2.6.11 DATA1 Register

**Table 3-62. DATA1 Register (Offset Address: FCh)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | DATA1 | RW | 0000h | This register is a window to write and read FW data. |

### 3.2.7 Advanced Error Reporting Capabilities

#### 3.2.7.1 Advanced Error Reporting Enhanced Capability Header Register

**Table 3-63. Advanced Error Reporting Enhanced Capability Header Register (Offset Address: 100h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | PCI Express Extended Capability ID | RO | 1h | ID for the Advanced Error Reporting Capability is 0001h. |
| 19 : 16 | Capability Version | RO | 1h | Indicates the version of the Capability structure present. |
| 31 : 20 | Next Capability Offset | RO | HwInit | This field contains the offset to the next PCI Express Capability structure.<br>When SerialNumber Capability Enable bit is set to '1b', this field is 140h. When SerialNumber Capability Enable bit is set to '0b', this field is 150h. |

#### 3.2.7.2 Uncorrectable Error Status Register

**Table 3-64. Uncorrectable Error Status Register (Offset Address: 104h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Rsvd | - | - | Reserved |
| 4 | Data Link Protocol Error Status | RW1CS | 0b | Data Link Protocol Error Status. |
| 5 | Surprise Down Error Status | RO | 0b | μPD720201/μPD720202 does not support this status. |
| 11 : 6 | Rsvd | - | - | Reserved. |
| 12 | Poisoned TLP Status | RW1CS | 0b | Poisoned TLP Status. |
| 13 | Flow Control Protocol Error Status | RO | 0b | μPD720201/μPD720202 does not support this status. |
| 14 | Completion Timeout Status | RW1CS | 0b | Completion Timeout Status. |
| 15 | Completer Abort Status | RW1CS | 0b | Completer Abort Status. |
| 16 | Unexpected Completion Status | RW1CS | 0b | Unexpected Completion Status. |
| 17 | Receiver Overflow Status | RW1CS | 0b | Receiver Overflow Status. |
| 18 | Malformed TLP Status | RW1CS | 0b | Malformed TLP Status. |
| 19 | ECRC Error Status | RO | 0b | μPD720201/μPD720202 does not support this status. |
| 20 | Unsupported Request Error Status | RW1CS | 0b | Unsupported Request Error Status. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 21 | Rsvd | - | - | Reserved. |

### 3.2.7.3 Uncorrectable Error Mask Register

**Table 3-65. Uncorrectable Error Status Register (Offset Address: 108h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Rsvd | - | - | Reserved. |
| 4 | Data Link Protocol Error Mask | RWS | 0b | Data Link Protocol Error Mask. |
| 5 | Surprise Down Error Mask | RO | 0b | μPD720201/μPD720202 does not support this status. |
| 11 : 6 | Rsvd | - | - | Reserved. |
| 12 | Poisoned TLP Mask | RWS | 0b | Poisoned TLP Mask. |
| 13 | Flow Control Protocol Error Mask | RO | 0b | μPD720201/μPD720202 does not support this status. |
| 14 | Completion Timeout Mask | RWS | 0b | Completion Timeout Mask. |
| 15 | Completer Abort Mask | RWS | 0b | Completer Abort Mask. |
| 16 | Unexpected Completion Mask | RWS | 0b | Unexpected Completion Mask. |
| 17 | Receiver Overflow Mask | RWS | 0b | Receiver Overflow Mask. |
| 18 | Malformed TLP Mask | RWS | 0b | Malformed TLP Mask. |
| 19 | ECRC Error Mask | RO | 0b | μPD720201/μPD720202 does not support this status. |
| 20 | Unsupported Request Error Mask | RWS | 0b | Unsupported Request Error Mask. |
| 31 : 21 | Rsvd | - | - | Reserved. |

### 3.2.7.4 Uncorrectable Error Severity Register

**Table 3-66. Uncorrectable Error Severity Register (Offset Address: 10Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Rsvd | - | - | Reserved. |
| 4 | Data Link Protocol Error Severity | RWS | 1b | Data Link Protocol Error Severity. |
| 5 | Surprise Down Error Severity | RO | 1b | μPD720201/μPD720202 does not support this status. |
| 11 : 6 | Rsvd | - | - | Reserved. |
| 12 | Poisoned TLP Severity | RWS | 0b | Poisoned TLP Severity. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 13 | Flow Control Protocol Error Severity | RO | 1b | μPD720201/μPD720202 does not support this status. |
| 14 | Completion Timeout Severity | RWS | 0b | Completion Timeout Severity. |
| 15 | Completer Abort Severity | RWS | 0b | Completer Abort Severity. |
| 16 | Unexpected Completion Severity | RWS | 0b | Unexpected Completion Severity. |
| 17 | Receiver Overflow Severity | RWS | 1b | Receiver Overflow Severity. |
| 18 | Malformed TLP Severity | RWS | 1b | Malformed TLP Severity. |
| 19 | ECRC Error Severity | RO | 0b | μPD720201/μPD720202 does not support this status. |
| 20 | Unsupported Request Error Severity | RWS | 0b | Unsupported Request Error Severity. |
| 31 : 21 | Rsvd | - | - | Reserved. |

### 3.2.7.5 Correctable Error Status Register

**Table 3-67. Correctable Error Status Register (Offset Address: 110h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Receiver Error Status | RO | 0b | Receiver Error Status. |
| 5 : 1 | Rsvd | - | - | Reserved. |
| 6 | Bad TLP Status | RW1CS | 0b | Bad TLP Status. |
| 7 | Bad DLLP Status | RW1CS | 0b | Bad DLLP Status. |
| 8 | REPLAY_NUM Rollover Status | RW1CS | 0b | REPLAY_NUM Rollover Status. |
| 11 : 9 | Rsvd | - | - | Reserved. |
| 12 | Replay Timer Timeout Status | RW1CS | 0b | Replay Timer Timeout Status. |
| 13 | Advisory Non-Fatal Error Status | RW1CS | 0b | Advisory Non-Fatal Error Status. |
| 31 : 14 | Rsvd | - | - | Reserved. |

### 3.2.7.6 Correctable Error Mask Register

**Table 3-68. Correctable Error Mask Register (Offset Address: 114h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Receiver Error Mask | RO | 0b | Receiver Error Mask. |
| 5 : 1 | Rsvd | - | - | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 6 | Bad TLP Mask | RWS | 0b | Bad TLP Mask. |
| 7 | Bad DLLP Mask | RWS | 0b | Bad DLLP Mask. |
| 8 | REPLAY_NUM Rollover Mask | RWS | 0b | REPLAY_NUM Rollover Mask. |
| 11 : 9 | Rsvd | - | - | Reserved. |
| 12 | Replay Timer Timeout Mask | RWS | 0b | Replay Timer Timeout Mask. |
| 13 | Advisory Non-Fatal Error Mask | RWS | 1b | Advisory Non-Fatal Error Mask. |
| 15 : 14 | Rsvd | - | - | Reserved. |

### 3.2.7.7 Advanced Error Capabilities and Control Register

**Table 3-69. Advanced Error Capabilities and Control Register (Offset Address: 118h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 4 : 0 | First Error Pointer | RO | 0b | The first Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. |
| 5 | ECRC Generation Capable | RO | 0b | No support. |
| 6 | ECRC Generation Enable | RO | 0b | No support. |
| 7 | ECRC Check Capable | RO | 0b | No support. |
| 8 | ECRC Check Enable | RO | 0b | No support. |
| 31 : 9 | Rsvd | - | - | Reserved. |

### 3.2.7.8 Header Log Register

**Table 3-70. Header Log Register (Offset Address: 11Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 127 : 0 | Header of TLP associated with error | RO | 0h | The Header Log register captures the header for the TLP corresponding to a detected error. |

### 3.2.8 Device Serial Number Enhanced Capability

#### 3.2.8.1 Device Serial Number Enhanced Capability Header Register

**Table 3-71. Device Serial Number Enhanced Capability Header Register (Offset Address: 140h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | PCI Express Extended Capability ID | RO | 3h | ID for the Device Serial Number Capability is 0003h. |
| 19 : 16 | Capability Version | RO | 1h | Indicates the version of the Capability structure present. |
| 31 : 20 | Next Capability Offset | RO | 150h | This field contains the offset to the next PCI Express Capability structure. |

#### 3.2.8.2 Serial Number Register

**Table 3-72. Serial Number Register (Offset Address: 144h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 63 : 0 | PCI Express Device Serial Number | RWO | HwInit | This field contains the IEEE defined 64-bit extended unique identifier (EUI-64 TM) loaded from External Serial ROM. This identifier includes a 24-bit company id value assigned by IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. |

### 3.2.9 Latency Tolerance Reporting (LTR) Capability

#### 3.2.9.1 LTR Extended Capability Header Register

**Table 3-73. LTR Extended Capability Header Register (Offset Address: 150h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | PCI Express Extended Capability ID | RO | 18h | ID for the LTR Extended Capability is 0018h. |
| 19 : 16 | Capability Version | RO | 1h | Indicates the version of the Capability structure present. |
| 31 : 20 | Next Capability Offset | RO | 0h | This field contains the offset to the next PCI Express Capability structure. |

#### 3.2.9.2 Max Snoop Latency Register

**Table 3-74. Max Snoop Latency Register (Offset Address: 154h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 9 : 0 | Max Snoop LatencyValue | RW | 0h | Along with the Max Snoop Latency Scale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. |
| 12 : 10 | Max Snoop latencyScale | RW | 0h | This register provides a scale for the value contained within the Maximum Snoop Latency Value field. |
| 15 : 13 | Rsvd | - | - | Reserved. |

#### 3.2.9.3 Max No-Snoop Latency Register

**Table 3-75. Max No-Snoop Latency Register (Offset Address: 156h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 9 : 0 | Max No-Snoop LatencyValue | RW | 0h | Along with the Max-No-Snoop Latency Scale field, this register specifies the maximum no-snoop latency that a device is permitted to request. |
| 12 : 10 | Max No-Snoop Latency Scale | RW | 0h | This register provides a scale for the value contained within the max No-Snoop LatencyValue field. |
| 15 : 13 | Rsvd | - | - | Reserved. |

## 3.3 Host Controller Capability Register

These registers specify the limits and capabilities of the host controller implementation.

All Capability Registers are Read-Only (RO) or hardware Initialized (HwInit attribute). The offsets for these registers are all relative to the beginning of the host controller's MMIO address space. The beginning of the host controller's MMIO address space is referred to as "Base" throughout this document.

**Table 3-76. eXtensible Host Controller Capability**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| HCIVERSION (Interface Version Number) | | Reserved | CAPLENGTH | 00h |
| HCSPARAMS1 (Structural Parameters 1) | | | | 04h |
| HCSPARAMS2 (Structural Parameters 2) | | | | 08h |
| HCSPARAMS3 (Structural Parameters 3) | | | | 0Ch |
| HCCPARAMS (Capability Parameters) | | | | 10h |
| DBOFF (Doorbell Offset) | | | | 14h |
| RTSOFF (Runtime Register Space Offset ) | | | | 18h |
| Reserved | | | | 1Ch |

### 3.3.1 Capability Registers Length (CAPLENGTH)

**Table 3-77. CAPLENGTH (Offset Address: Base + 00h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | CAPLENGTH | RO | 20h | This register is used as an offset to add to register base to find the beginning of the Operational Register Space. This value is referred to as "Operational Base" throughout this document. |

### 3.3.2 Host Controller Interface Version Number (HCIVERSION)

**Table 3-78. HCIVERSION (Offset Address: Base + 02h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | HCIVERSION | RO | 0100h | This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0 |

### 3.3.3 Structural Parameters 1 (HCSPARAMS1)

**Table 3-79. HCSPARAMS1 (Offset Address: Base + 04h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Number of Device Slots (MaxSlots) | RO | 20h | This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. |
| 18 : 8 | Number of Interrupters (MaxIntrs) | RO | 008h | This field specifies the number of Interrupters implemented on this host controller. Each Interrupter is allocated to a vector of MSI-X and controls its generation and moderation.<br>The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space. |
| 23 : 19 | Rsvd | - | - | Reserved. |
| 31 : 24 | Number of Ports (MaxPorts) | RO | 08h (μPD720201)<br>04h (μPD720202) | This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Refer to section 3.4.8 and 5.2 for more information. |

### 3.3.4 Structural Parameters 2 (HCSPARAMS2)

**Table 3-80. HCSPARAMS2 (Offset Address: Base + 08h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Isochronous Scheduling Threshold | RO | 1h | The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of microframes. |
| 7 : 4 | Event Ring Segment Table Max (ERST Max) | RO | 1h | This field determines the maximum value supported the Event Ring Segment Table entries.<br>The maximum number of Event Ring Segment Table entries<br>$= 2^{\text{ERST Max}}$ |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 25 : 8 | Rsvd | - | - | Reserved. |
| 26 | Scratchpad Restore | RO | 1b | A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events. |
| 31 : 27 | Max Scratchpad Buffers | RO | 00100b | This field indicates the number of Scratchpad Buffers system software shall reserve for the xHC. |

### 3.3.5 Structural Parameters 3 (HCSPARAMS3)

**Table 3-81. HCSPARAMS3 (Offset Address: Base + 0Ch)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | U1 Device Exit Latency | RO | 0h | Worst case latency to transition a root hub Port Link State from U1 to U0. Applies to all root hub ports. A value of '0' indicates 0 us. |
| 15 : 8 | Rsvd | - | - | Reserved. |
| 31 : 16 | U2 Device Exit Latency | RO | 0h | Worst case latency to transition a root hub Port Link State from U2 to U0. Applies to all root hub ports. A value of '0' indicates 0us. |

### 3.3.6 Capability Parameters (HCCPARAMS)

**Table 3-82. HCCPARAMS (Offset Address: Base + 10h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | 64-bit Addressing Capability | RO | 1b | This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64bits register and data structure pointer fields. A value of '1' indicates 64-bit address memory pointers implemented. |
| 1 | BW Negotiation Capability | RO | 1b | This flag identifies whether the xHC has implemented the Bandwidth Negotiation. A value of '1' indicates BW Negotiation implemented. |
| 2 | Context Size | RO | 1b | A value of '0' indicates the xHC uses 32-byte Context data structures, and '1' indicates 64-byte Context data structures. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 | Port Power Control | RO | HwInit | This flag indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register.<br>This bit is initialized by the UsePPON bit in the PCI Configuratin Space HCConfiguration Register. Refer to Section 3.2.6.5 for more information on the use of this flag. |
| 4 | Port Indicators | RO | 0b | This bit indicates whether the xHC root hub ports support port indicator control. A value of '0' indicates that the port status and control registers does not include a read/writeable field for controlling the state of the port indicator. |
| 5 | Light HC Reset Capability | RO | 0b | This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A '0' in this bit indicates that Light Host Controller Reset is not supported. |
| 6 | Latency Tolerance Messaging Capability | RO | 1b | This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A '1' in this bit indicates that LTM is supported. |
| 7 | No Secondary SID Support | RO | 1b | This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1' in this bit indicates that Secondary Stream ID decoding is not supported. |
| 8 | Parse All Event Data (PAE) | RO | 1b | This flag indicates whether the host controller implementation Parses all Event Data TRBs while advancing to the next TD after a short packet, or it skips all but the first Event Data TRB. A '0' in this bit indicates that only the first Event Data TRB is parsed. |
| 11 : 9 | Rsvd | - | - | Reserved. |
| 15 : 12 | Maximum Primary Stream Array Size (MaxPSASize) | RO | 5h | This field identifies the maximum size Primary Stream Array that that the xHC supports. The Primary Stream Array size = $2^{MaxPSASize+1}$ |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 16 | xHCI Extended Capabilities Pointer | RO | 140h | This field indicates the existence of a capabilities list. The value of this field indicates a relative offset , in 32-bit words, from Base to the beginning of the first extended capability.<br>First extended capability : Base + ( 0140h << 2 ) = Base + 500h |

### 3.3.7 Doorbell Offset (DBOFF)

**Table 3-83. DBOFF (Offset Address: Base + 14h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Doorbell Array Offset | RO | 800h | This field defines the DWORD offset of the Doorbell Array base address from the Base. |

### 3.3.8 Runtime Register Space Offset (RTSOFF)

**Table 3-84. RTSOFF Offset (Offset Address: Base + 18h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Runtime Register Space Offset | RO | 600h | This field defines the 32-byte offset of the xHC Runtime Registers from Base. |

## 3.4 Host Controller Operational Registers

This section defines the xHCI Operational Registers.

The base address of this register space is referred to as Operational Base (Refer to section 3.3.1). The Operational Base shall be DWORD aligned and is calculated by adding the value of the Capability Registers Length (CAPLENGTH) register to the Capability Base address. All registers are multiples of 32 bits in length.

Unless otherwise stated, all registers should be accessed as a 32-bit width on reads with an appropriate software mask, if needed. A software read/modify/write mechanism should be invoked for partial writes.

These registers are located at a positive offset from the Capabilities Registers.

**Table 3-85. Host Controller Operational Registers**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| USBCMD (USB Command) | | | | 20h |
| USBSTS (USB Status) | | | | 24h |
| PAGESIZE (Page Size) | | | | 28h |
| Reserved | | | | 2C~33h |
| DNCTRL (Device Notification Control) | | | | 34h |
| CRCR (Command Ring Control) | | | | 38h |
| Reserved | | | | 40~4Fh |
| DCBAAP (Device Context Base Address Array Pointer) | | | | 50h |
| CONFIG (Configure) | | | | 58h |
| Reserved | | | | 5C~3FFh |
| Host Controller Port Register Set 1 – 4 | | | | 420~49Fh |

### 3.4.1 USB Command Register (USBCMD)

The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

**Table 3-86. USBCMD Register (Offset Address: Operational Base (20h) + 00h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Run/Stop | RW | 0b | '1' = Run, '0' = Stop. When set to '1', the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes the current and any actively pipelined transactions on the USB and then halts. |
| 1 | Host Controller Reset (HCRST) | RW | 0b | This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset.<br>When software writes a '1' to this bit, Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.<br>PCI Configuration registers are not affected by this reset.<br>This bit is cleared to '0' by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a '0' to this bit and shall not write any xHC Operational or Runtime registers until while HCRST is '1'.<br>Software shall not set this bit to '1' when the HCHalted bit in the USBSTS register is a '0'. |
| 2 | Interrupter Enable | RW | 0b | This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a '1', then Interrupter host system interrupt generation is allowed. |
| 3 | Host System Error Enable | RW | 0b | When this bit is a '1', and the HSE bit in the USBSTS register is a '1', the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit. |
| 6 : 4 | Rsvd | - | - | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 | Light Host Controller Reset | RO | 0b | Not implemented. |
| 8 | Controller Save State | RW | 0b | When written by software with '1' and HCHalted = '1', then the xHC shall save any internal state that will be restored by a subsequent Restore State operation. When written by software with '1' and HCHalted = '0', or written with '0', no Save State operation shall be performed. This flag always returns '0' when read. Note that undefined behavior may occur if a Save State operation is initiated while Restore State Status (RSS) = '1' |
| 9 | Controller Restore State | RW | 0b | When set to '1', and HCHalted = '1', then the xHC shall perform a Restore State operation and restore its internal state. When set to '1' and Run/Stop = '1' or HCHalted(HCH) = '0', or when cleared to '0', no Restore State operation shall be performed. This flag always returns '0' when read. Note that undefined behavior may occur if a Restore State operation is initiated while Save State Status (SSS) = '1' |
| 10 | Enable Wrap Event | RW | 0b | When set to '1', the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to '0' no MFINDEX Wrap Events are generated. |
| 11 | Enable U3 MFINDEX Stop | RW | 0b | When set to '1', the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to '0', the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state. |
| 31 : 12 | Rsvd | - | - | Reserved. |

### 3.4.2 USB Status Register (USBSTS)

This register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to '0' in this register by writing a '1' to it (RW1C).

**Table 3-87. USBSTS Register (Offset Address: Operational Base (20h) + 04h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | HCHalted | RO | 1b | This bit is a '0' whenever the Run/Stop bit is a '1'. The xHC sets this bit to '1' after it has stopped executing as a result of the Run/Stop bit being cleared to '0', either by software or by the xHC hardware(e.g. internal error).<br>If this bit is '1', then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC. |
| 1 | Rsvd | - | - | Reserved. |
| 2 | Host System Error (HSE) | RW1C | 0b | The xHC sets this bit to '1' when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. When this error occurs, the xHC clears the Run/Stop bit in the USBCMD register. If the HSEE bit in the USBCMD register is a '1', the xHC shall also assert out-of-band error signaling to the host. |
| 3 | Event Interrupt (EINT) | RW1C | 0b | The xHC sets this bit to '1' when the Interrupt Pending (IP) bit of any Interrupter transitions from '0' to '1'.<br>The EINT flag does not generate an interrupt, it is simply a logical OR of the IMAN register IP flag '0' to '1' transitions. As such, it does not need to be cleared to clear an xHC interrupt. |
| 4 | Port Change Detect | RW1C | 0b | The xHC sets this bit to a '1' when any port has a change bit transition from a '0' to a '1'. This bit is loaded with the OR of all PORTSC change bits. |
| 7 : 5 | Rsvd | - | - | Reserved. |
| 8 | Save State Status | RO | 0b | When the Controller Save State flag in the USBCMD register is written with '1' , this bit shall be set to '1' and remain '1' while the xHC saves its internal state. When the Save State operation is complete, this bit shall be cleared to '0'. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 9 | Restore State Status | RO | 0b | When the Controller Restore State flag in the USBCMD register is written with '1', this bit shall be set to '1' and remain '1' while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be cleared to '0'. |
| 10 | Save/Restore Error | RW1C | 0b | If an error occurs during a Save or Restore operation, this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. |
| 11 | Controller Not Ready (CNR) | RO | 1b | '0' = Ready and '1' = Not Ready. Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip hardware Reset and cleared when the xHC is ready to begin accepting register writes. |
| 12 | Host Controller Error | RO | 0b | '0' = No internal xHC error conditions exist and '1' = Internal xHC error condition. If both μPD720201 and μPD720202 detect no correct firmware in Serial ROM, this flag is set. |
| 31 : 13 | Rsvd | - | - | Reserved. |

### 3.4.3 Page Size Register (PAGESIZE)

**Table 3-88. PAGESIZE Register (Offset Address: Operational Base (20h) + 08h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Page Size | RO | 0001h | This field defines the page size supported by the xHC. This xHC supports 4k byte page size .<br>Page size = $2^{(\text{Page Size} + 12)}$ |
| 31 : 16 | Rsvd | - | - | Reserved. |

### 3.4.4 Device Notification Control Register (DNCTRL)

This register is used by software to enable or disable the reporting of the reception of specific USB Device Notification Transaction Packets. A Notification Enable (Nx, where x = 0 to 15) flag is defined for each of the 16 possible device notification types. If a flag is set for a specific notification type, a Device Notification Event will be generated when the respective notification packet is received. After reset all notifications are disabled.

**Table 3-89. DNCTRL Register (Offset Address: Operational Base (20h) + 14h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Notification Enable (N0 –N15) | RW | 0h | When a Notification Enable bit is set, a Device Notification Event will be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1(bit1) to '1' enables Device Notification Event generation if a Device Notification Transaction Packet is received with its Notification Type field set to '1' (FUNCTION_WAKE). |
| 31 : 16 | Rsvd | - | - | Reserved. |

### 3.4.5 Command Ring Control Register (CRCR)

The Command Ring Control Register provides Command Ring control and status capabilities, and identifies the address and Cycle bit state of the Command Ring Dequeue Pointer. The Command Ring is 64 byte aligned, so the low order 6bits of the Command Ring Pointer shall always be '0'.

**Table 3-90. CRCR Register (Offset Address: Operational Base (20h) + 18h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Ring Cycle State (RCS) | RW | 0b | This bit identifies the value of the xHC Consumer Cycle State flag for the TRB referenced by the Command Ring Pointer.<br>Writes to this flag are ignored if Command Ring Running is '1'.<br>If the CRCR is written while the Command Ring is stopped (CRR = '0' ), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command.<br>If the CRCR is not written while the Command Ring is stopped (CRR = '0'), then the Command Ring will begin fetching Command TRBs using the current value of the internal Command Ring CCS flag.<br>Reading this flag always returns '0'. |
| 1 | Command Stop | RW | 0b | Writing a '1' to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer.<br>Next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation.<br>Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit shall always return '0'. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 2 | Command Abort | RW | 0b | Writing a '1' to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped.<br>The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation.<br>Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit always returns '0'. |
| 3 | Command Ring Running (CRR) | RO | 0b | This flag is set to '1' if the Run/Stop bit is '1' and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to '0' when the Command Ring is "stopped" after writing a '1' to the Command Stop (CS) or Command Abort(CA) flags, or if the Run/Stop bit is cleared to '0'. |
| 5 : 4 | Rsvd | - | - | Reserved. |
| 64 : 6 | Command Ring Pointer | RW | 0h | This field defined high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer.<br>Writes to this field are ignored when Command Ring Running (CRR) ='1'.<br>If the CRCR is written while the Command Ring is stopped (CRR ='0'), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command.<br>If the CRCR is not written while the Command Ring is stopped (CRR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'. |

### 3.4.6 Device Context Base Address Array Pointer Register (DCBAAP)

The Device Context Base Address Array Pointer Register identifies the base address of the Device Context Base Address Array. The memory structure referenced by this physical memory pointer is assumed to be physically contiguous and 64-byte aligned.

**Table 3-91. DCBAAP Register (Offset Address: Operational Base (20h) + 30h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 5 : 0 | Rsvd | - | - | Reserved. |
| 63 : 6 | Device Context Base Address Array Pointer | RW | 0h | This field defines high order bits of the 64-bit base address of the Device Context Pointer Array table. A table of address pointers that reference Device Context structures for the devices attached to the host. |

### 3.4.7 Configure Register (CONFIG)

This register defines runtime xHC configuration parameters.

**Table 3-92. CONFIG Register (Offset Address: Operational Base (20h) + 38h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Max Device Slots Enabled (MaxSlotsEn) | RW | 0h | This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. e.g. A value of 16 specifies that Device Slots 1 to 16 are active. A value of '0' disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references.<br>This field shall not be modified if the xHC is running. |
| 31 : 8 | Rsvd | - | - | Reserved. |

### 3.4.8 Host Controller Port Register Set

μPD720201 implements 8 root hub ports: 4 SuperSpeed ports and 4 Hi-Speed ports. A root Hub port that supports the USB3 protocol is comprised of a PORTSC, a USB3 PORTPMSC and PORTLI register. A root Hub port that supports the USB2 protocol is comprised of a PORTSC and PORTPMSC register. Ports are numbered from 1 to MaxPorts. MaxPorts is defined in the HCSPARAMS1 register. On the μPD720201, Port1 (P1), Port2 (P2), Port3 (P3) and Port4 (P4) are SuperSpeed ports, while Port5 (P5), Port6 (P6), Port7 (P7) and Port8 (P8) are Hi-Speed ports. These assignments are defined in the xHCI Supported Protocol Extended Capability (defined in section 3.7.2). The mapping of Root Hub Ports to the physical USB3 compatible connectors (C1, C2, C3 and C4) of a system are shown below. Refer to section 5.2 for more information. Note that the Port Power Pin, PPONx(x:1 to 4) of μPD720201, is ORed with both Port Power flag of the PORTSC of Porty(y:1 to 4) and that of Portz(z:5 to 8).

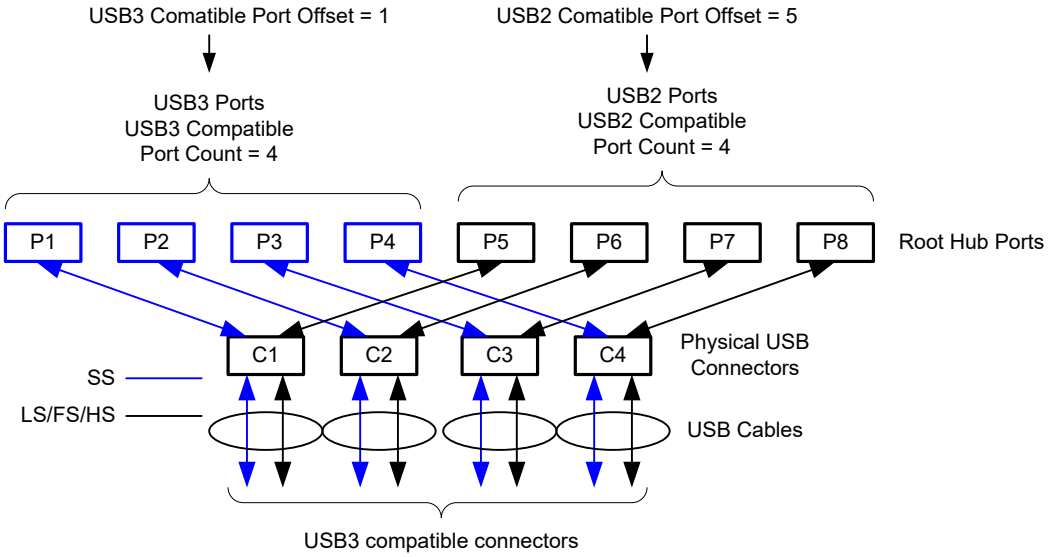



**Table 3-93. Host Controller Port Register Set (Offset shows from Base)**

| 31 24 | 23 16 | 15 8 | 7 0 | 720201 Offset | 720202 Offset |
|---|---|---|---|---|---|
| Port1(SS) PORTSC (Port Status and Control) | | | | 420h | 420h |
| Port1(SS) PORTPMSC (Port Power Management Status and Control) | | | | 424h | 424h |
| Port1 PORTLI (Port Link Info) | | | | 428h | 428h |
| Reserved | | | | 42Ch | 42Ch |
| Port2(SS) PORTSC (Port Status and Control) | | | | 430h | 430h |
| Port2(SS) PORTPMSC (Port Power Management Status and Control) | | | | 434h | 434h |
| Port2 PORTLI (Port Link Info) | | | | 438h | 438h |
| Reserved | | | | 43Ch | 43Ch |
| Port3(SS) PORTSC (Port Status and Control) | | | | 440h | - |
| Port3(SS) PORTPMSC (Port Power Management Status and Control) | | | | 444h | - |
| Port3 PORTLI (Port Link Info) | | | | 448h | - |
| Reserved | | | | 44Ch | - |
| Port4(SS) PORTSC (Port Status and Control) | | | | 450h | - |
| Port4(SS) PORTPMSC (Port Power Management Status and Control) | | | | 454h | - |
| Port3 PORTLI (Port Link Info) | | | | 458h | - |

| | | |
|---|---|---|
| Reserved | 45Ch | - |
| Port5(LS/FS/HS) PORTSC (Port Status and Control) | 460h | 440h |
| Port5(LS/FS/HS) PORTPMSC (Port Power Management Status and Control) | 464h | 444h |
| Reserved | 468h | 448h |
| Reserved | 46Ch | 44Ch |
| Port6(LS/FS/HS) PORTSC (Port Status and Control) | 470h | 450h |
| Port6(LS/FS/HS) PORTPMSC (Port Power Management Status and Control) | 474h | 454h |
| Reserved | 478h | 458h |
| Reserved | 47Ch | 45Ch |
| Port7(LS/FS/HS) PORTSC (Port Status and Control) | 480h | - |
| Port7(LS/FS/HS) PORTPMSC (Port Power Management Status and Control) | 484h | - |
| Reserved | 488h | - |
| Reserved | 48Ch | - |
| Port8(LS/FS/HS) PORTSC (Port Status and Control) | 490h | - |
| Port8(LS/FS/HS) PORTPMSC (Port Power Management Status and Control) | 494h | - |
| Reserved | 498h | - |
| Reserved | 49Ch | - |

#### 3.4.8.1 Port Status and Control Register (PORTSC)

This register is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST).

Software cannot change the state of the port unless Port Power (PP) is asserted (‘1’), regardless of the Port Power Control (PPC) capability. The host is required to have power stable to the port within 20 milliseconds of the ‘0’ to ‘1’ transition of PP. If PPC =’1’ software is responsible for waiting 20ms after asserting PP, before attempting to change the state of the port.

**Table 3-94. PORTSC Register (Offset Address: Operational Base (20h) + (400h + (10h *(n-1)))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Current Connect Status (CCS) | RO | 0b | ‘1’ = Device is present on port. ‘0’ = No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to ‘1’. This flag is ‘0’ if PP is ‘0’. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 1 | Port Enable/Disable (PED) | RW1CS | 0b | Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition.<br>PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. |
| 2 | Rsvd. | - | - | Reserved. |
| 3 | Over-current Active (OCA) | RO | 0b | This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a'0' when the over-current condition is removed. |
| 4 | Port Reset (PR) | RW1S | 0b | '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. This flag is '0' if PP is '0'. |
| 8 : 5 | Port Link State (PLS) | RWS | 100b | This field is used to power manage the port and reflects its current link state.<br>When the port is in the Enable state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition o the port.<br>This field is undefined if PP= '0'.<br>Write and Read value is shown in table3-91 and table 3-92.<br>Note: The Port Link State Write Strobe (LWS) shall be set tot '1' to write this field. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 9 | Port Power (PP) | RWS | 0b | This flag reflects a port's logical, power control state. When PP equals a '0', the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'.<br>0 = This port is in the Powered-off state.<br>1 = This port is not in the Powered-off state.<br>When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0'.<br>This bit is set after the software sets Max Device Slots Enable (MaxSlotsEn) field in Configure (CONFIG) register or Host Controller Reset (HCRST) flag in USBCMD register. |
| 13 : 10 | Port Speed | RO | 0b | This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1'). In all other cases this field shall indicate Undefined Speed.<br>Value Meaning<br>0 Undefined Speed<br>1 Full-Speed<br>2 Low-Speed<br>3 Hi-Speed<br>4 SuperSpeed<br>5-15 Reserved. |
| 15 : 14 | Port Indicator Control | RWS | 0b | Writing to these bits has no effect . |
| 16 | Port Link State Write Strobe (LWS) | RW | 0b | When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 17 | Connect Status Change (CSC) | RW1CS | 0b | '1' = Change in CCS. '0' = No change. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. |
| 18 | Port Enabled/Disabled Change (PEC) | RW1CS | 0b | '1' = change in PED. '0' = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. |
| 19 | Warm Port Reset Change (WRC) | RW1CS | 0b | Writing to this bit has no effect. |
| 20 | Over-current Change (OCC) | RW1CS | 0b | This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active (OCA). Software shall clear this bit by writing a '1' to it. |
| 21 | Port Reset Change (PRC) | RW1CS | 0b | '0' = No change. '1' = Reset complete. This flag is set to '1' due a '1' to '0' transition of Port Reset (PR). Software shall clear this bit by writing a '1' to it. |
| 22 | Port Link State Change (PLC) | RW1CS | 0b | '0' = No change. '1' = Link Status Changed. This flag is set to '1' due to table 3-93.<br>Note that this flag shall not be set if the PLS transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. |
| 23 | Port Config Error Change (CES) | RW1CS/ Rsvd | 0b | '0' = No change. '1' = Port Config Error detected. This flag indicates that the port failed to configure its link partner. Software shall clear this bit by writing a '1' to it.<br>Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 24 | Cold Attach Status (CAS) | RO | 0b | '1' = Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enable state. Software shall clear this bit by writing a '1' to WPR or the xHC shall clear this bit if CCS transitions to '1'. This flag is '0' if PP is '0' or for USB2 protocol ports. |
| 25 | Wake on Connect Enable (WCE) | RWS | 0b | Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events. |
| 26 | Wake on Disconnect Enable (WDE) | RWS | 0b | Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events |
| 27 | Wake on Over-current Enable (WOE) | RWS | 0b | Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events. |
| 29 : 28 | Rsvd | - | - | Reserved. |
| 30 | Device Removable (DR) | RO | 0b | This flag indicates if this port has a removable device attached. '1' = Device is non-removable. '0' = Device is removable. |
| 31 | Warm Port Reset (WPR) | RW1S /Rsvd | 0b | When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR,PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be Reserved. |

**Note :** n = Port Number 1, 2, 3, 4, 5, 6 ,7 and 8 for μPD720201, n = Port Number 1,2,3 and 4 for μPD720202.

**Table 3-95. PLS Write Value**

| Write Value | Description |
|---|---|
| 0 | The link shall transition to a U0 state from any of the U states. |
| 2 | USB2 protocol ports only. The link should transition to the U2 state. |
| 3 | The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. |
| 5 | USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP=1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. |
| 1,4,6-14 | Ignored |

| | |
|---|---|
| 15 | USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. |

**Table 3-96. PLS Read Value**

| Read Value | Description |
|---|---|
| 0 | Link is in the U0 State |
| 1 | Link is in the U1 State |
| 2 | Link is in the U2 State |
| 3 | Link is in the U3 State (Device Suspended) |
| 4 | Link is in the Disable State |
| 5 | Link is in the RxDetect State |
| 6 | Link is in the Inactive State |
| 7 | Link is in the Polling State |
| 8 | Link is in the Recovery State |
| 9 | Link is in the Hot Reset State |
| 10 | Link is in the Compliance Mode State |
| 11 | Link is in the Test Mode State |
| 14 : 12 | Reserved |
| 15 | Link is in the Resume State |

**Table 3-97. PLS transitions**

| Transition | Condition |
|---|---|
| U3 -> Resume | Wakeup signaling from a device |
| Resume -> Recovery -> U0 | Device Resume complete (USB3 protocol ports only) |
| Resume -> U0 | Device Resume complete (USB2 protocol ports only) |
| U3 -> Recovery -> U0 | Software Resume complete (USB3 protocol ports only) |
| U3 -> U0 | Software Resume complete (USB2 protocol ports only) |
| U2 -> U0 | L1 Resume complete (USB2 protocol ports only) |
| U0 -> U0 | L1 Entry Reject (USB2 protocol ports only) |
| Any state -> Inactive | Error (USB3 protocol ports only) |

#### 3.4.8.2 Port PM Status and Control Register (PORTPMSC)

The definitions of the fields in the PORTPMSC register depend on the USB protocol supported by the port.

This register is only reset by platform hardware during a cold reset or in response to a Host Controller Reset (HCRST).

#### 3.4.8.3 USB3 Protocol PORTPMSC definition

**Table 3-98. USB3 PORTPMSC Register (Offset Address: Operational Base (20h) + (404h + (10h*(n-1)))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | U1 Timeout | RWS | 0h | Timeout value for U1 inactivity timer. If equal to FFh, the port is disabled from initiating U1 entry. This field shall be set to '0' by the assertion of PR to '1'. |
| 15 : 8 | U2 Timeout | RWS | 0h | Timeout value for U2 inactivity timer. If equal to FFh, the port is disabled from initiating U2 entry. This field shall be set to '0' by the assertion of PR to '1'. |
| 16 | Force Link PM Accept (FLA) | RW | 0b | When this bit is set to '1', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted. This flag shall be set to '0' by the assertion of PR to '1' or when CCS = transitions from '0' to '1'. Writes to this flag have no affect if PP ='0'. This flag is '0' if PP is '0'. |
| 31 : 17 | Rsvd | - | - | Reserved. |

**Note:** In the equation for Offset Address, n = Port Number 1,2,3 or 4 for μPD720201. n = 1,2 for μPD720202.

#### 3.4.8.4 USB2 Protocol PORTPMSC definition

**Table 3-99. USB2 PORTPMSC Register (Offset Address: Operational Base (20h) +(404h + (10h*(n-1)))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 2 : 0 | L1 Status (L1S) | RO | 000b | This field is used by software to determine whether an L1-based suspend request (LMP transaction) was successful, specifically:<br>Value – Meaning<br>0 – Invalid – This field shall be ignored by software.<br>1 – Success – Port successfully transitioned to L1 (ACK)<br>2 – Not Yet – Device is unable to enter L1 at this time (NYET)<br>3 – Not Supported – Device does not support L1 transitions (STALL)<br>4 – Timeout/Error – Device failed to respond to the LPM Transaction or an error occurred.<br>5-7 – Reserved |
| 3 | Remote Wake Enable (RWE) | RW | 0b | The host system sets this flag to enable or disable the device for remote wake from L1. |
| 7 : 4 | Host Initiated Resume Duration (HIRD) | RW | 0h | System software sets this field to indicate to the recipient device how long the xHC will drive resume if it initiates an exit from L1. The value of 0000b is interpreted as 50us. Each incrementing value up adds 75us to the previous value. |
| 15 : 8 | L1 Device Slot | RW | 0h | System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of '0' indicates no device is present. The xHC uses this field to lookup information necessary to generate the LMP Token packet. |
| 16 | Hardware LPM Enable (HLE) | RW | 0b | If this bit is set to '1', then hardware controlled LPM shall be enabled for this port.. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 27 : 15 | Rsvd | - | - | Reserved |
| 31 : 28 | Port Test Control | RW | 0h | When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value.<br>A non-zero Port Test Control value is only valid to a port that is in the Powered-off state (PLS = Disable). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error.<br>The encoding of the Test Mode bits for a USB2 protocol port are:<br>Value — Test Mode<br>0 — Test mode not enabled<br>1 — Test J_STATE<br>2 — Test K_STATE<br>3 — Test SE0_NAK<br>4 — Test Packet<br>5 — Test FORCE_ENABLE<br>6-14 — Reserved<br>15 — Port Test Control Error |

**Note:** In the equation for Offset Address, n = Port Number 5,6,7 or 8 for μPD720201. n = 3 or 4 for μPD720202.

#### 3.4.8.5 Port Link Info Register (PORTLI)

The definitions of the fields in the PORTLI register depend on the USB protocol supported by the port. The USB3 Port Link Info register reports the Link Error Count, while the USB2 Port Link Info register is reserved and shall be treated as Reserved by software.

**Table 3-100. USB3 PORTLI Register (Offset Address: Operational Base (20h) + (408h + (10h * (n-1)))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Link Error Count | RO | 0h | This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip hardware Reset, HCRST, when PR transitions from '1' to '0', or when CCS = transitions from '0' to '1'. |
| 31 : 16 | Rsvd | - | - | Reserved. |

**Note:** n = Port Number 1,2,3 or 4 for μPD720201. n = 1 or 2 for μPD720202.

## 3.5 Host Controller Runtime Registers

This section defines the xHCI Runtime Register space. The base address of this register space is referred to as Runtime Base (Refer to section 3.3.8 ). The Runtime Base shall be 32-byte aligned and is calculated by adding the value Runtime Register Space Offset register to the Capability Base address. All Runtime registers are multiples of 32 bits in length.

Unless otherwise stated, all registers should be accessed with Dword references on reads, with an appropriate software mask if needed. A software read/modify/write mechanism should be invoked for partial writes.

Software should write registers containing a Qword address field using only Qword references. If a system is incapable of issuing Qword references, then writes to the Qword address fields shall be performed using 2 Dword references; low Dword-first, high-Dword second.

**Table 3-101. Host Controller Runtime Registers**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| MFINDEX (Microframe Index) | | | | 600h |
| Reserved | | | | 604~61Fh |
| IR0 (Interrupter Register Set 0) | | | | 620~63Fh |
| IR1 (Interrupter Register Set 1) | | | | 640~65Fh |
| IR2 (Interrupter Register Set 2) | | | | 660~67Fh |
| IR3 (Interrupter Register Set 3) | | | | 680~69Fh |
| IR4 (Interrupter Register Set 4) | | | | 6A0~6BFh |
| IR5 (Interrupter Register Set 5) | | | | 6C0~6DFh |
| IR6 (Interrupter Register Set 6) | | | | 6E0~6FFh |
| IR7 (Interrupter Register Set 7) | | | | 700~71Fh |

### 3.5.1 Microframe Index Register (MFINDEX)

This register is used by the system software to determine the current periodic frame. The register value is incremented every 125 microseconds (once each microframe).

This register is only incremented while Run/Stop (R/S) = '1'.

The value of this register affects the SOF value generated by USB2 Bus Instances.

**Table 3-102. MFINDEX Register (Offset Address: Runtime Base (600h) + 00h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 13 : 0 | Microframe Index | RO | 0h | The value in this register increment at the end of each microframe. Bit [13:3] may be used to determine the current 1ms Frame Index. |
| 31 14 | Rsvd | - | - | Reserved. |

### 3.5.2 Interrupter Register Set

The Interrupter logic consists of an Interrupter Management Register, an Interrupter Moderation Register, and the Event Ring Registers. A one to one mapping is defined for Interrupter to MSI-X vector.

**Table 3-103. Interrupter Register Set**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| Interrupter Management | | | | 00h |
| Interrupter Moderation Counter | | Interrupter Moderation Interval | | 04h |
| Reserved | | Event Ring Segment Table Size | | 08h |
| Reserved | | | | 0Ch |
| Event Ring Segment Table Base Address Lo | | | Reserved | 10h |
| Event Ring Segment Table Base Address Hi | | | | 14h |
| Event Ring Dequeue Pointer Lo | | | Reserved | 18h |
| Event Ring Dequeue Pointer Hi | | | | 1Ch |

#### 3.5.2.1 Interrupter Management Register (IMAN)

The Interrupter Management register allows system software to enable, disable, detect, and force xHC interrupts.

**Table 3-104. IMAN Register (Offset Address: Runtime Base (600h) + 020h + (20h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Interrupter Pending (IP) | RW1C | 0b | This flag represents the current state of the Interrupter. If IP='1', an interrupt is pending for this Interrupter. This flag is set to '1' when IE = '1', the IMODC Interrupt Moderation Counter field = '0' the Event Ring associated with the Interrupter I not empty, and EHB = '0'. A '0' value indicates that no interrupt is pending for the Interrupter. If MSI interrupts are enabled, this flag shall be cleared automatically when the PCI Dword write generated by the Interrupt assertion is complete. If PCI Pin Interrupts are enabled, this flag shall be cleared by software. |
| 1 | Interrupt Enable (IE) | RW | 0b | This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set '1', the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches '0'. If this bit is '0', then the Interrupter is prohibited from generating interrupts. |
| 31 : 2 | Rsvd | - | - | Reserved. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

### 3.5.2.2 Interrupter Moderation Register (IMOD)

The Interrupter Moderation Register controls the “interrupt moderation” feature of an interrupter, allowing system software to throttle the interrupt rate generated by the xHC.

**Table 3-105. IMOD Register (Offset Address: Runtime Base (600h) + 024h + (20h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Interrupt Moderation Interval (IMODI) | RW | FA0h (~1ms) | Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of ‘0’ disables interrupt throttling logic and interrupts shall be generated immediately if IP = ‘0’, EHB = ‘0’, and the Event Ring is not empty. |
| 31 : 16 | Interrupt Moderation Counter (IMODC) | RW | 0h | Down counter. Loaded with Interval value whenever IP is cleared to ‘0’, counts down to ‘0’, and stops. The associated interrupt shall be signaled whenever this counter is ‘0’, the Event Ring is not empty, the IE and IP flags = ‘1’, and EHB = ‘0’.<br>This counter may be directly written by software at any time to alter the interrupt rate. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

### 3.5.2.3 Event Ring Segment Table Size Register (ERSTSZ)

The Event Ring Segment Table Size Register defines the number of segments supported by the Event Ring Segment table.

**Table 3-106. ERSTSZ Register (Offset Address: Runtime Base (600h) + 028h + (20h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Event Ring Segment Table Size | RW | 0h | This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HSCPARAMS2 register.<br>For Secondary Interrupters: Writing a value of '0' to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring.<br>For the Primary Interrupter: Writing a value of '0' to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled. |
| 31 : 16 | Rsvd | - | - | Reserved. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

### 3.5.2.4 Event Ring Segment Table Base Address Register (ERSTBA)

The Event Ring Segment Table Base Address Register identifies the start address of the Evnet Ring Segment Table.

**Table 3-107. ERSTBA Register (Offset Address: Runtime Base (600h) + 30h + (20h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Rsvd | - | - | Reserved. |
| 63 : 4 | Event Ring Segment Table Base Address Register | RW | 0h | This field defines the high order bits of the start address of the Event Ring Segment Table.<br>Writing this register sets the Event Ring State Machine : EREP advancement to the Start state. This field shall not be modified if HCHalted (HCH) = '0'. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

#### 3.5.2.5 Event Ring Dequeue Pointer Register (ERDP)

The Event Ring Dequeue Pointer Register is written by software to define the Event Ring Dequeue Pointer location to the xHC. Software updates this pointer when it is finished the evaluation of an Event(s) on the Event Ring.

**Table 3-108. ERDP Register (Offset Address: Runtime Base (600h) + 038h + (20h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 2 : 0 | Dequeue ERST Segment Index (DESI) | RW | 000b | This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in. |
| 3 | Event Hander Busy (EHB) | RW1C | 0b | This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written. |
| 63 : 4 | Event Ring Dequeue Pointer | RW | 0h | This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer. |

## 3.6 Doorbell Registers

The Doorbell Array is organized as an array of up to 32 Doorbell Registers. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software utilizes the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

These registers are pointed to by the Doorbell Offset Register (DBOFF) in the xHC Capability register space. The Doorbell Array base address shall be Dword aligned and is calculated by adding the value in the DBOFF register (section 0) to “Base”. All registers are 32 bits in length. Software should read and write these registers using only Dword accesses.

**Table 3-109. Doorbell Registers**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| DB Stream ID | | Reserved | DB Target | 800h ~ 88Fh |

**Table 3-110. Doorbell Register**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | DB Target | RW | 0h | This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers.<br>Device Context Doorbells (1 – 255) |
| 15 : 8 | Rsvd | - | - | Reserved |
| 31 : 16 | DB Stream ID | RW | 0h | Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid.<br>If the endpoint does not define Streams (MaxPStreams = 0) and a non-‘0’ value is written to this field, the doorbell reference shall be ignored.<br>This field only applies to Device Context Doorbells and shall be cleared to ‘0’ for Host Controller Commands.<br>This field returns ‘0’ when read. |

## 3.7 xHCI Extended Capabilities

The μPD720201 and μPD720202 exports xHCI-specific extended capabilities utilizing a method similar to the PCI extended capabilities. It specifies a non-zero value in xHCI Extended Capabilities Pointer field of the HCPARAMS register. This value is an offset into xHC MMIO space from the Base, where the Base is beginning of the host controller's MMIO address space.

### 3.7.1 USB Legacy Support Capability

The USB Legacy Support provided by the xHC is optional normative functionality that is applicable to pre-OS software (BIOS) and the operating system for the coordination of ownership of the xHC.
This capability is chained through the xHCI Extended Capabilities Pointer (xECP) field and resides in MMIO space.

**Table 3-111. HC Extended Capability Registers**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| USB Legacy Support Capability Register (USBLEGSUP) | | | | 500h |
| USB Legacy Support Control and Status Register (USBLEGCTLSTS) | | | | 504h |

#### 3.7.1.1 USB Legacy Support Capability (USBLEGSUP)

This register is an xHC extended capability register. It includes a specific function section and a pointer to the next xHCI Extended Capability. This register is used by pre-OS software (BIOS) and the operating system to coordinate ownership of the xHC. This register is in the Auxiliary Power well.

**Table 3-112. USBLEGSUP (Offset Address: xECP (500h) + 00h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Capability ID | RO | 1h | This field identifies the xHCI Extended capability. The xHCI Extended capability ID for the USB Legacy Support is 01h. |
| 15 : 8 | Next Capability Pointer | RO | 4h | This field points to the xHC MMIO space offset of the next xHCI extended capability pointer. |
| 16 | HC BIOS Owned Semaphore | RW | 0h | The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software. |
| 23 : 17 | Rsvd | - | - | Reserved. |
| 24 | HC OS Owned Semaphore | RW | 0h | System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit reads as '0'. |
| 31 : 25 | Rsvd | - | - | Reserved. |

### 3.7.1.2 USB Legacy Support Control / Status (USBLEGCTLSTS)

Pre-OS (BIOS) software uses this register to enable System Management Interrupts (SMIs) for every xHCI/USB event it needs to track. Bits [21:16] of this register are simply shadow bit of USBSTS register [5:0]. This register is in the Auxiliary Power well.

**Table 3-113. USBLEGCTLSTS (Offset Address: xECP (500h) + 04h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | USB SMI Enable | RW | 0b | When this bit is a '1', and the SMI on SMI on Event Interrupt bit in this register is a '1', the host controller will issue an SMI immediately. |
| 3 : 1 | Rsvd | - | - | Reserved. |
| 4 | SMI on Host System Error Enable | RW | 0b | When this bit is a '1', and the SMI on Host System Error bit in this register is a '1', the host controller will issue an SMI immediately. |
| 12 : 5 | Rsvd | - | - | Reserved. |
| 13 | SMI on OS Ownership Enable | RW | 0b | When this bit is a '1' and the OS Ownership Change bit is '1', then the host controller will issue an SMI. |
| 14 | SMI on PCI Command Enable | RW | 0b | When this bit is '1' and SMI on PCI Command is '1', then the host controller will issue an SMI. |
| 15 | SMI on BAR Enable | RW | 0b | When this bit is '1' and SMI on BAR is '1', then the host controller will issue an SMI. |
| 16 | SMI on Event Interrupt | RO | 0b | Shadow bit of Event Interrupt (EINT) bit in the USBSTS register.<br>This bit follows the state the Event Interrupt (EINT) bit in the USBSTS register, e.g. it automatically clears when EINT clears or set when EINT is set. |
| 19 : 17 | Rsvd | - | - | Reserved. |
| 20 | SMI on Host System Error | RO | 0b | Shadow bit of Host System Error (HSE) bit in the USBSTS register.<br>To clear this bit to '0', system software shall write a '1' to the Host System Error (HSE) bit in the USBSTS register. |
| 28 : 21 | Rsvd | - | - | Reserved. |
| 29 | SMI on OS Ownership Change | RW1C | 0b | This bit is set to '1' whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from '1' to a '0' or '0' to a '1'. |
| 30 | SMI on PCI Command | RW1C | 0b | This bit is set to '1' whenever the PCI Command Register is written. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 | SMI on BAR | RW1C | 0b | This bit is set to '1' whenever the Base Address Register (BAR) is written. |

**Note:** SMI – System Management Interrupt.
BAR – Base Address Register.

### 3.7.2 xHCI Supported Protocol Capability

**Table 3-114. xHCI Supported Protocol Capability Register**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| Revision Major | Revision Minor | Next Capability Pointer | Capability ID | 00h |
| Name String | | | | 04h |
| PSIC | Protocol Defined | Compatible Port Count | Compatible Port Offset | 08h |
| Reserved | | | Protocol Slot Type | 0Ch |

#### 3.7.2.1 USB 3.0 Supported Protocol Capability

**Table 3-115. Offset 00h - xHCI Supported Protocol Capability Field (Offset Address: xECP + 10h (510h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Capability ID | RO | 02h | This field identifies the xHCI Extended capability. The xHCI Extended capability ID for the USB Supported Protocol is 02h. |
| 15 : 8 | Next Capability Pointer | RO | 05h | This field points to the xHC MMIO space offset of the next xHCI extended capability pointer. |
| 23 : 16 | Minor Revision | RO | 00h | Minor Specification Release Number in Binary –Coded Decimal. |
| 31 : 24 | Major Revision | RO | 03h | Major Specification Release Number in Binary –Coded Decimal. |

**Table 3-116. Offset 04h - xHCI Supported Protocol Capability Field (Offset Address: xECP + 14h (514h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Name String | RO | 20425355h | This field is a mnemonic name string that references the specification with which the xHC is compliant. |

**Table 3-117. Offset 08h - xHCI Supported Protocol Capability Field (Offset Address: xECP + 18h (518h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | USB3 Compatible Port Offset | RO | 01h | This field specifies the starting Port Number of Root Hub Port that supports this protocol. |
| 15 : 8 | USB3 Compatible Port Count | RO | 04h (μPD720201) 02h (μPD720202) | This field identifies the number of consecutive Root Hub Ports that support this protocol. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 27 : 16 | Protocol Defined | RO | 0h | This field is reserved. |
| 31 : 28 | PSIC | RO | 0h | Protocol Speed ID Count. This field indicates the number of Protocol Speed ID Dwords that the xHCI Supported Protocol Capability data structure contains. |

**Table 3-118. Offset 0Ch - xHCI Supported Protocol Capability Field (Offset Address: xECP + 1Ch (51Ch))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 4 : 0 | Protocol Slot Type | RO | 0h | This field is reserved. |
| 31 : 5 | Rsvd | - | - | Reserved. |

### 3.7.2.2 USB 2.0 Supported Protocol Capability

**Table 3-119. Offset 00h - xHCI Supported Protocol Capability Field (Offset Address: xECP + 24h (524h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Capability ID | RO | 02h | This field identifies the xHCI Extended capability. The xHCI Extended capability ID for the USB Supported Protocol is 02h. |
| 15 : 8 | Next Capability Pointer | RO | 07h | This field points to the xHC MMIO space offset of the next xHCI extended capability pointer. |
| 23 : 16 | Minor Revision | RO | 00h | Minor Specification Release Number in Binary –Coded Decimal. |
| 31 : 24 | Major Revision | RO | 02h | Major Specification Release Number in Binary –Coded Decimal. |

**Table 3-120. Offset 04h - xHCI Supported Protocol Capability Field (Offset Address: xECP + 28h (528h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Name String | RO | 20425355h | This field is a mnemonic name string that references the specification with which the xHC is compliant. |

**Table 3-121. Offset 08h - xHCI Supported Protocol Capability Field (Offset Address: xECP + 2Ch (52Ch))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | USB2 Compatible Port Offset | RO | 05h (μPD720201) 03h (μPD720202) | This field specifies the starting Port Number of Root Hub Port that supports this protocol. |
| 15 : 8 | USB2 Compatible Port Count | RO | 04h (μPD720201) 02h (μPD720202) | This field identifies the number of consecutive Root Hub Ports that support this protocol. |
| 16 | Rsvd | - | - | Reserved |
| 17 | HSO | RO | 0b | Hi-Speed Only. 0b indicates this USB2 ports are Low, Full, and Hi-Speed capable. |
| 18 | IHI | RO | 0b | Integrated Hub Implemented. 0b indicates this host does not implement integrated hub. |
| 19 | HLC | RO | 0b | Hardware LMP Capability. If this bit is set to '1', the ports described by this capability support hardware controlled USB2 Link Power Management. |
| 27 : 20 | Rsvd | - | - | Reserved |
| 31 : 28 | PSIC | RO | 0h | Protocol Speed ID Count. This field indicates the number of Protocol Speed ID Dwords that the xHCI Supported Protocol Capability data structure contains. |

**Table 3-122. Offset 0Ch - xHCI Supported Protocol Capability Field (Offset Address: xECP + 30h (530h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 4 : 0 | Protocol Slot Type | RO | 0h | This field is reserved. |
| 31 : 5 | Rsvd | - | - | Reserved. |

### 3.7.3 Debug Capability

**Table 3-123. Debug Capability Register Layout**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| Reserved | DCERST Max | Next Capability Pointer | Capability ID | 00h |
| Reserved | | DB Target | Reserved | 04h |
| Reserved | | Event Ring Segment Table Size | | 08h |
| Reserved | | | | 0Ch |
| Event Ring Segment Table Base Address Lo | | | Reserved | 10h |
| Event Ring Segment Table Base Address Hi | | | | 14h |
| Event Ring Dequeue Pointer Lo | | | Reserved | 18h |
| Event Ring Dequeue Pointer Hi | | | | 1Ch |
| Debug Capability Control Register | | | | 20h |
| Debug Capability Status Register | | | | 24h |
| Debug Capability Port Status and Control Register | | | | 28h |
| Reserved | | | | 2Ch |
| Debug Capability Context Pointer Lo | | | Reserved | 30h |
| Debug Capability Context Pointer Hi | | | | 34h |
| Vendor ID | | Reserved | DbC Protocol | 38h |
| Device Revision | | Product ID | | 3Ch |

#### 3.7.3.1 Debug Capability ID Register

**Table 3-124. Offset 00h – Debug Capability Field (Offset Address: xECP + 50h (550h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Capability ID | RO | 02h | This field identifies the xHCI Extended capability. The xHCI Extended capability ID for the USB Supported Protocol is 02h. |
| 15 : 8 | Next Capability Pointer | RO | 00h | This field points to the xHC MMIO space offset of the next xHCI extended capability pointer. |
| 20 : 16 | DCERST Max | RO | 00h | This field determines the maximum value supported the Debug Capability Event Ring Segment Table Base Size registers. 0h indicates that the maximum number of Event Ring Segment Table entries is 1. |
| 31 : 21 | Rsvd. | - | - | Reserved. |

### 3.7.3.2 Debug Capability Doorbell Register

**Table 3-125. Offset 04h – Debug Capability Field (Offset Address: xECP + 54h (554h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | Rsvd | - | - | Reserved. |
| 15 : 8 | DB Target | WO | 00h | Doorbell Target. This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell.<br>Value – Definition<br>0 – Data EP 1 OUT Enqueue Pointer Update<br>1 – Data EP 1 IN Enqueue Pointer Update<br>2 : 255 – Reserved. |
| 31 : 16 | Rsvd | - | - | Reserved. |

### 3.7.3.3 Debug Capability Event Ring Segment Table Size Register

**Table 3-126. Offset 08h – Debug Capability Field (Offset Address: xECP + 58h (558h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Event Ring Segment Table Size | RW | 0000h | This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Debug Capability Event Ring Segment Table Base Address Register. Software shall initialize this register before setting the Debug Capability Enable field in the Debug Capability Control Register. |
| 31 : 16 | Rsvd. | - | - | Reserved. |

### 3.7.3.4 Debug Capability Event Ring Segment Table Base Address Register

**Table 3-127. Offset 0Ch – Debug Capability Field (Offset Address: xECP + 60h (560h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Rsvd. | - | - | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 63 : 4 | Event Ring Segment Table Base Address Register | RW | 0h | This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the Debug Capability Enable field. |

### 3.7.3.5 Debug Capability Event Ring Dequeue Pointer Register

**Table 3-128. Offset 18h – Debug Capability Field (Offset Address: xECP + 68h (568h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 2 : 0 | DESI | RW | 000b | This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. |
| 3 | Rsvd | - | - | Reserved. |
| 63 : 4 | Dequeue Pointer | RW | 0h | This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the Debug Capability Enable field. |

### 3.7.3.6 Debug Capability Event Ring Dequeue Pointer Register

**Table 3-129. Offset 20h – Debug Capability Field (Offset Address: xECP + 70h (570h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | DCR | RO | 0b | DbC Run. When ‘0’, Debug Device is not in the Configured state. When ‘1’, Debug Device is in the Configured state and bulk Data pipe transactions are accepted by Debug Capability and routed to the IN and OUT Transfer Rings. A ‘0’ to ‘1’ transition of the Port Reset bit will clear this bit to ‘0’. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 1 | LSE | RW | 0b | Link Status Event Enable. Setting this bit to a '1' enables the Debug Capability to generate Port Status Change Events due the Port Link Status Change bit transitioning from a '0' to a '1'. |
| 2 | HOT | RW1S | 0b | Halt OUT TR. While this bit is '1', the Debug Capability shall generate STALL TPs for all IN TPs received for the OUT TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT)request is received for the endpoint. This field is valid only when the Debug Capability is in Run Mode (DCR = '1'). When not in Run Mode, this field shall return '0' when read, and writes will have no effect. |
| 3 | HIT | RW1S | 0b | Halt IN TR. While this bit is '1', the Debug Capability shall generate STALL TPs for all OUT DPs received for the IN TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT) request is received for the endpoint. This field is valid only when the Debug Capability is in Run Mode |
| 4 | DRC | RW1C | 0b | This bit shall be set to '1' when DCR bit is cleared to '0', i.e. by any DbC Port State transition that exits the DbC-Configured state. While this bit is '1' the Debug Capability Doorbell Register (DCDB) is disabled. Software shall clear this bit to re-enable the DCDB. |
| 15 : 5 | Rsvd. | - | - | Reserved. |
| 23 : 16 | Debug Max Burst Size | RO | 0h | This field identifies the maximum burst size supported by the bulk endpoints of this DbC implementation. |
| 30 : 24 | Device Address | RO | 0h | This field reports he USB device address assigned to the Debug Device during the enumeration process. This field is valid when the DbC Run bit is '1'. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 | DCE | RW | 0h | Debug Capability Enable. Setting this bit to a '1' enables xHC USB Debug Capability operation. This bit is a '0' if the USB Debug Capability is disabled. Clearing this bit releases the Root Hub port assigned to the Debug Capability, and terminates any Debug Capability Transfer or Event Ring activity., |

#### 3.7.3.7 Debug Capability Status Register

**Table 3-130. Offset 24h – Debug Capability Field (Offset Address: xECP + 74h (574h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Event Ring Not Empty | RO | 0b | When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the Debug Capability Event Ring Dequeue Pointer register. |
| 23 : 1 | Rsvd | - | - | Reserved. |
| 31 : 24 | Debug Port Number | RO | 0h | This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port. |

### 3.7.3.8 Debug Capability Port Status and Control Register

**Table 3-131. Offset 28h – Debug Capability Field (Offset Address: xECP + 78h (578h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | CCS | RO | 0b | Current Connect Status. ‘1’ = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. ‘0’ = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a ‘0’ to ‘1’ transition of this bit. This flag is ‘0’ if DCE is ‘0’. |
| 1 | PED | RW | 0b | Port Enabled/Disabled. This flag shall be set to ‘1’ by a ‘0’ to ‘1’ transition of CCS or a ‘1’ to ‘0’ transition of the PR. This field is ‘0’ if DCE or CCS are ‘0’. |
| 3 : 2 | Rsvd | - | - | Reserved. |
| 4 | PR | RO | 0b | ‘1’ = Port is in Reset. ‘0’ = Port is not in Reset. This bit is set to ‘1’ when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug Capability. This field is ‘0’ if DCE or CCS are ‘0’. |
| 8 : 5 | PLS | RO | 000b | This field reflects its current link state. This field is only relevant when a Debug Host is attached.<br>Value — Meaning<br>0 — U0 State<br>1 — U1 State<br>2 — U2 State<br>3 — U3 State<br>4 — Disabled State<br>5 — RxDetect State<br>6 — Inactive State<br>7 — Polling State<br>8 — Recovery State<br>9 — Hot Reset State<br>15: 10 — Reserved |
| 9 | Rsvd | - | - | Reserved. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 13 : 10 | Port Speed | RO | 0h | This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed.<br>Value — Meaning<br>0 — Undefined Speed<br>1 – 15 — Protocol Speed ID |
| 16 : 14 | Rsvd | - | - | Reserved. |
| 17 | CSC | RW1S | 0b | Connect Status Change. '1' = Change in Current Connect Status. '0' = No change. Indicates a change has occurred in the port's Current Connect Status. The xHC sets this bit to '1' for all changes to the Debug Device connect status, even if system software has not cleared an existing DbC Connect Status Change. This field is '0' if DCE is '0'. |
| 20 : 18 | Rsvd | - | - | Reserved. |
| 21 | PRC | RW1C | 0b | Port Reset Change. This bit is set when reset processing on this port is complete. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to ito. This field is '0' if DCE is '0'. |
| 22 | PLC | RW1C | 0b | Port Link Status Change. This flag is set to '1' due to the following PLS transitions:<br>Transition — Condition<br>U0 -> U3 — Suspend signaling detected from Debug Host.<br>U3 -> U0 — Resume complete<br>Polling -> Disabled — Training Error<br>Ux or Recovery -> Incactive — Error |
| 23 | CEC | RW1C | 0b | Port Config Error Change. This flag indicates that the port failed to configure its link partner.' 0' = Nochange. '1' = Port Config Error detected. Software shall clear this bit by writing a '1' to it. |
| 31 : 24 | Rsvd | - | - | Reserved. |

### 3.7.3.9 Debug Capability Context Pointer Register

**Table 3-132. Offset 30h – Debug Capability Field (Offset Address: xECP + 80h (580h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 3 : 0 | Rsvd | - | - | Reserved. |
| 63 : 4 | Debug Capability Context Pointer Register | RW | 0h | This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'. |

### 3.7.3.10 Debug Capability Device Descriptor Info Register 1

**Table 3-133. Offset 38h – Debug Capability Field (Offset Address: xECP + 88h (588h))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 7 : 0 | DbC Protocol | RW | 00h | This field presented by the Debug Device in the USB Interface Descriptor bInterfaceProtocol field.<br>Value — Function<br>0 — Debug Target vendor defined.<br>1 — GNU Remote Debug Command Set supported.<br>2 - 255 — Reserved. |
| 15 : 8 | Rsvd | - | - | Reserved. |
| 31 : 16 | Vendor ID | RW | 00h | This field is presented by the Debug Device in the USB Device Descriptor idVendor field. |

### 3.7.3.11 Debug Capability Device Descriptor Info Register 2

**Table 3-134. Offset 3Ch – Debug Capability Field (Offset Address: xECP + 8Ch (58Ch))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 15 : 0 | Product ID | RW | 0000h | This field is presented by the Debug Device in the USB Device Descriptor idProduct field. |

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 16 | Device Revision | RW | 0000h | This field is presented by the Debug Device in the USB Device Descriptor bcdDeviced field. |

## 3.8 MSI-X / PBA Table

**Table 3-135. MSI-X Table Registers**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| Message Address | | | | 00h |
| Message Upper Address | | | | 04h |
| Message Data | | | | 08h |
| Reserved | | | MB | 0Ch |

**Table 3-136. PBA Table Registers**

| 31 24 | 23 16 | 15 8 | 7 0 | Offset |
|---|---|---|---|---|
| PBA Table | | | | 00h |

### 3.8.1 Message Address for MSI-X Table

**Table 3-137. Message Address (Offset Address: Base + 1000h + (10h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Message Address | RW | 0h | System-specified message lower address. For MSI-X messages, the contents of this field from an MSI-X Table entry specify the lower portion of the DWORD-aligned address. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

### 3.8.2 Message Upper Address for MSI-X Table

**Table 3-138. Message Upper Address (Offset Address: Base + 1004h + (10h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Message Upper Address | RW | 0h | System-specified message Upper address. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

### 3.8.3 Message Data for MSI-X

**Table 3-139. Message Data (Offset Address: Base + 1008h + (10h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Message Data | RW | 0h | System-specified message Data. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

### 3.8.4 Vector Control for MSI-X

**Table 3-140. Message Data (Offset Address: Base + 100Ch + (10h*Interrupter))**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 0 | Mask Bit | RW | 0b | When this bit is set, the function is prohibited from sending a message using this MSI-X Table. |
| 31 : 1 | Rsvd | - | - | Reserved. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

### 3.8.5 Pending Bits for MSI-X PBA Entries

**Table 3-141. Message Data (Offset Address: Base + 1080h)**

| Bits | Field | Read/ Write | Value (Default) | Comment |
|---|---|---|---|---|
| 31 : 0 | Pending Bits | RO | 0h | For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. |

**Note:** Interrupter is 0, 1, 2, 3, 4, 5, 6 or 7.

# 4. Power Management

## 4.1 Power Management States

This section defines the PCI Express Power Management states.

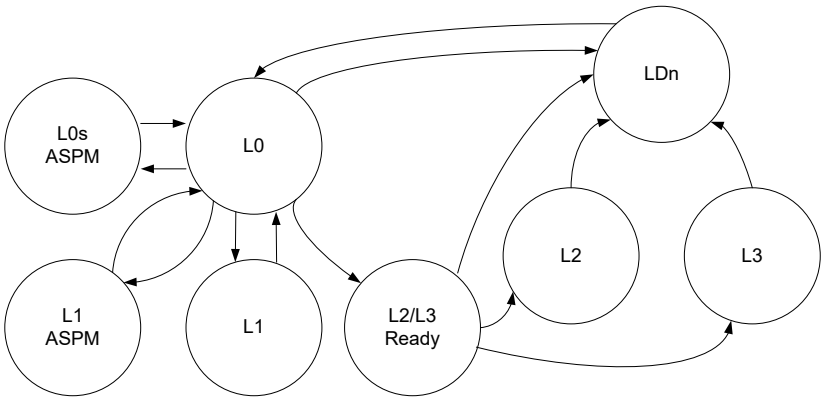
### 4.1.1 PCI Express Link State Power Management (L-States)

PCI Express defines Link power management states, replacing the bus power management states that were defined by the PCI Bus Power Management Interface Specification. Link states are not visible to PCI Power Management legacy compatible software, and are either derived from the power management D-states of the corresponding components connected to that Link or by Active State Power Management (ASPM) protocols. PCI Express Power Management defines L0, L0s, L1, L2/L3 Ready, L2, L3 and LDn. Refer to PCI Express Base Specification Rev.2.0 for more detail on PCI Express Link State Power Management.

**Table 4-1. PCI Express Link States**

| L-States | Description |
|---|---|
| L0 | Active state. All PCI Express transactions and other operations are enabled. |
| L0s | A low resume latency, energy saving “standby” ASPM state. Entry into the L0s state is managed separately for each direction of the Link. It is the responsibility of each device at either end of the Link to initiate an entry into the L0s state on its transmitting Lanes. Power management software (BIOS or OS) enables or disables this function by programming the ASPM control field in the Link Control Register. Renesas Electronics does not recommend using L0s function because transfer throughput decreases. |
| L1 (ASPM) | Higher latency, lower power “standby” ASPM state. The μPD720201 and μPD720202 can initiate entry into the L1 ASPM state in the D0 state when they detect idle time on the PCIe bus and both components on a Link enable the L1 Entry enable bit of ASPM control field in the Link Control Register. Power management software (BIOS or OS) enables or disables this function by programming the ASPM control field in the Link Control Register (3.2.5.7). |
| L1 | Higher latency, lower power “standby” state. The μPD720201 and μPD720202 initiates entry into the L1 state in the D3hot state. |
| L2/L3 Ready | Staging point for L2 or L3. The μPD720201 and μPD720202 enters the L2/L3 Ready state after receiving the PME_Turn_Off Message from the Root Complex and responding with the PME_TO_Ack. |
| L2 | Auxiliary –powered Link, deep-energy-saving state. |
| L3 | Link Off state. When no power is present, the component is in the L3 state. |
| LDn | A transitional Link Down pseudo-state prior to L0. |

**Figure 4-1. Link Power Management State Flow Diagram**



### 4.1.2 PCI Express Device Power Management States (D-States)

PCI Express supports all PCI Device power management states. The μPD720201 and μPD720202 supports D0 and D3 (D3hot and D3cold) states.

**Table 4-2. PCI Express Device Power Management States**

| D-States | Description |
|---|---|
| D0 | Normal operation state. |
| D3hot | When the Power State field in the Power Management Status / Control Register (Refer to 3.2.2.3) is set to 11b and PERST# is high, μPD720201 and μPD720202 is D3hot state. In this state, configuration and message requests are accepted. |
| D3cold | When the Power State field in the Power Management Status / Control Register (Refer to 3.2.2.3) is set to 11b and PERST# is low, μPD720201 and μPD720202 is D3cold state. |

### 4.1.3 CLKREQ# Signal

The μPD720201 and μPD720202 supports the CLKREQ# signal and assigns it to the PECREQB pin. Since the CLKREQ# signal is an open drain and active low signal an external pull-up resistor is required. Operation of the CLKREQ# signal is determined by the state of the enable clock management bit in the Link Control Register (Refer to 3.2.5.7). When the enable clock management bit is disabled, the CLKREQ# signal is asserted at all times. When the enable clock management bit is enabled, the CLKREQ# signal may be de-asserted during an L1 Link state.

**Table 4-3. Operation of CLKREQ# Signal**

| D-States | Description |
|---|---|
| D0, D3hot | The conditions that CLKREQ# is de-asserted are:<br>Enable clock management bit in the Link Control Register is 1b and<br>Link state is L1. |

### 4.1.4 Summary of PCI Express Power Management States

Table summarizes the relationship between D-state and L-State.

**Table 4-4. Summary of PCI Express Power Management States**

| D-States | L-States | Reference Clock | Conditions |
|---|---|---|---|
| D0 | L0 | ON | Active state. |
| | L0s | ON | - The L0s Entry Enable bit (3.2.5.7) in the ASPM Control field of the μPD720201 and μPD720202 is enabled. |
| | L1 ASPM | ON | - The L1 Entry Enable bit in the ASPM Control field of both the μPD720201/202 and the Root Complex are enabled.<br>- μPD720201/202 detects idle time on the PCIe bus. |
| | | OFF | - L1 Entry Enable bit of both the μPD720201/μPD720202 and the Root Complex are enabled.<br>- μPD720201/202 detects idle time on the PCIe bus.<br>- The PECREQB pin is connected to the CLKREQ# of the system.<br>- The Enable clock management bit (3.2.5.7) is set to 1b. |
| D3hot | L1 | ON | - The Power State field is set to 11b and PERST# is high. Main power sources remains during this state. |
| | | OFF | - The Power State field is set to 11b and PERST# is high. Main power sources remains during this state.<br>- The PECREQB pin is connected to the CLKREQ# of the system.<br>- The Enable clock management bit (3.2.5.7) is set to 1b. |
| D3cold | L2 | OFF | - Power State field set to 11b.<br>- Execution of the PME_Turn_Off/PME_TO_Ack handshake sequences.<br>- PERST# is low. Main power remains during this state. |

## 4.2 Power Management Event (PME) Mechanism

Power Management Event (PME) is typically utilized to revive the system. The PME mechanism is software compatible with the PME mechanism defined by the PCI Bus Power Management Interface Specification. Power Management Events are generated by the μPD720201 and μPD720202 as a means of requesting a Power Management state change. When the Link state is L1 and D-state is D3hot, the μPD720201 and μPD720202 asserts the WAKEB signal and sends PME Message to the root complex to wake up the system. On the other hand, when the Link state is L2 (D-state is D3cold), μPD720201 and μPD720202 assert the WAKEB signal to re-establish reference clock before sending PME Message to the root complex.

### 4.2.1 PME support

If the power state of host controller should be changed from D0 or D3 to the other, PME event will occur as shown in the PME_support bits in PMC (Power Management Capabilities) register. The 5-bit field in the PME_support indicates the power states in which μPD720201 and μPD720202 may send PME Message. A value of 0b for any bit indicates that it is not capable of sending PME Message while in that power state. Note that the default value of the Bit15 of the PME_support for D3cold is “HwInit” and depends on the AUXDET bit in the Host Controller Configuration Register.

### 4.2.2 Pin configuration for supporting PME generation from D3cold

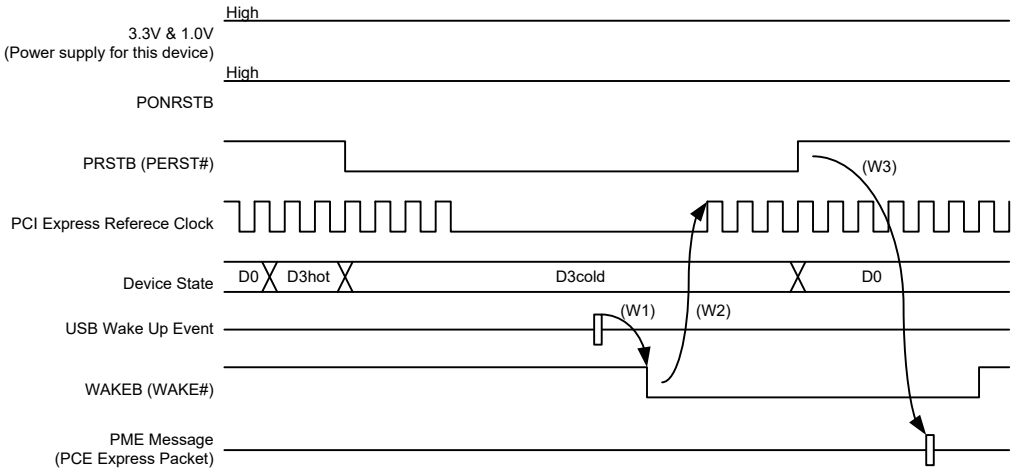
In case where the PME generation from D3cold is required, system board implementation shall be taken into consideration.

| Pin name | Wake Up support from D3cold and D3hot | Wake Up support only from D3hot |
|---|---|---|
| 3.3 V and 1.05 V | Both 3.3 V and 1.05 V power must be maintained to the μPD720201/202 during D3cold and D3hot states | Both 3.3 V and 1.05 V power must be maintained to the μPD720201/202 during D3hot states. |
| PONRSTB | “High” during D3cold and D3hot states. | “High” during D3hot states. |
| PEWAKEB | Connect to WAKE# of the system chipset and is pulled “high” with 3.3 V maintained during D3cold and D3hot states. | Connect to WAKE# of the system chipset and is pulled “high” with 3.3 V maintained during D3hot state. |
| PECREQB | Connect to CLKREQ# of the system chipset and is pulled “high” with 3.3 V maintained during D3hot states. (PECREQB is not used during D3cold.) | Connect to CLKREQ# of the system chipset and is pulled “high” with 3.3 V maintained during D3hot states. (PECREQB is not used during D3cold.) |
| OCI (2:1)B | Pulled “high” with 3.3 V maintained during D3cold and D3hot. | Pulled “high” with 3.3 V maintained during D3hot. |
| SPISO | Pulled “high” with 3.3 V maintained during D3cold and D3hot. Note that the power of the Serial ROM must be maintained during D3cold and D3hot states. | Pulled “high” with 3.3 V maintained during D3hot. Note that the power of the Serial ROM must be maintained during D3hot states. |

### 4.2.3 Timing Diagram for PME

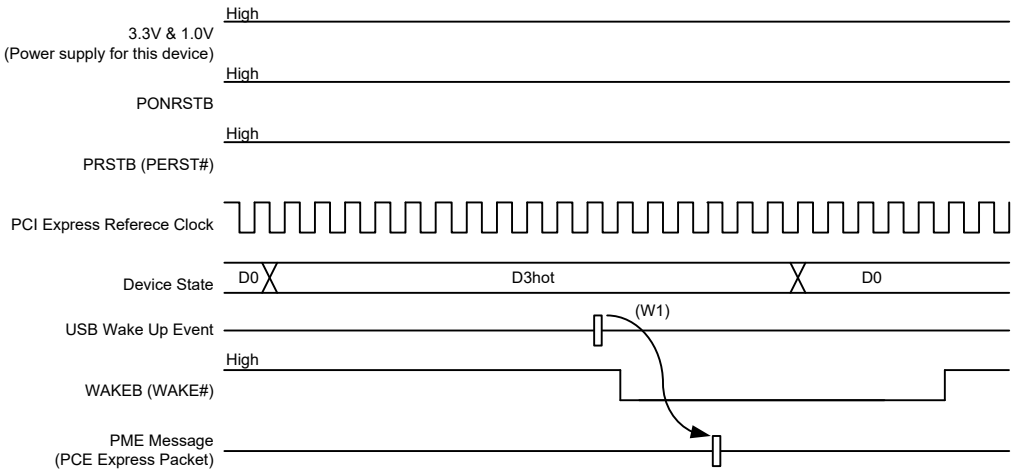
When Power State bits in PMCSR register indicate D3 and PONRST# is clamped high, the μPD720201 and μPD720202 maintain Power Management Context (PMCSR register and PORTSC register), even if the PERST# goes low and reference clock is removed. Note that the voltage level of the PERST# depends on the system during a sleeping state.

**Figure 4-2. Wake Up State Transition from D3cold (AUXDET bit = '1')**




1) PERSTB should be "high" during normal PCI operation.
2) System SW sets PME_En bit in the PMCSR register.
3) System SW sets D3 in Power State bits in the PMCSR register.
4) System goes into sleeping states and PERSTB goes low. μPD720201/202 is D3cold state.
5) When USB wake-up event occurs, WAKEB is asserted (W1).
6) Reference clock is re-established and PERSTB goes high (W2)
7) μPD720201/202 sends PME Message to the root complex (W3).

**Figure 4-3. Wake Up State Transition only from D3hot**




1) PERSTB should be “high” during normal PCI operation.
2) System SW sets PME_En bit in the PMCSR register.
3) System SW sets D3 in Power State bits in the PMCSR register.
4) System goes into sleeping states and PERSTB maintain “high”. μPD720201/202 is D3hot state.
5) When USB wake-up event occurs, μPD720201/202 sends PME Message to the root complex (W1) and asserts the WAKEB.

### 4.2.4 Wakeup Events

An external USB event may initiate a system level resume. When resume signaling is detected by a suspend USB port, the PME Event occurs if enabled (i.e. PMCSR PME_En bit = '1').

The following table summarizes the system wake-up events, defining the state of the Port Link State (PLS), Current Connect Status (CCS), Port Enabled/Disabled (PED), Over-Current Active (OCA) fields in the PORTSC register and the Port Change Detect (PCD) bit in the USBSTS register as function of the respective Wake Enable flag (WDE, WCE, WOE). The table values indicate the state of the fields after the respective event.

**Table 4-5. Wakeup Events**

| Port Status and Signaling Device State Type | Port State After Event | | | | |
|---|---|---|---|---|---|
| | PLS | CCS | PED | OCA | PCD |
| Port is in the U3. Resume signaling received. | Resume | 1 | 1 | 0 | 1 |
| A port is in a state that may detect a disconnect, and the port's WDE bit is '1'. A disconnect is detected. | RxDetect | 0 | 0 | 0 | 1 |
| Port is in the Disconnected state and the port's WCE bit is '1'. A connect is detected. | U0 (SS)<br>Polling (USB2) | 1 | 1 (SS)<br>0 (USB2) | 0 | 1 |
| If a port is in a state that may detect an over-current condition and the port's WOE bit is '1'. An over-current condition occurs. | Disabled | 0 | 0 | 1 | 1 |

**Note:** A USB2 port may detect a disconnect when the port is in the Disabled, Enabled, or Reset state. A USB3 Port may detect a disconnect when the port is in the Loopback, Compliance, Error, Polling, Enabled, or Reset States.

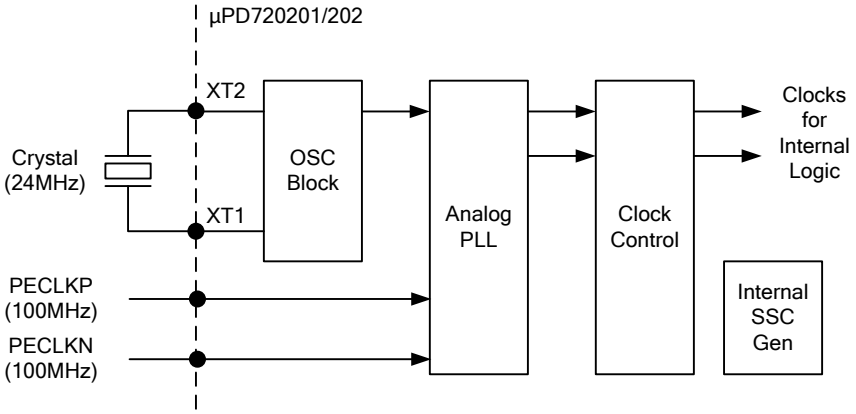
## 4.3 Control for System Clock Operation

When μPD720201 and μPD720202 are put into power down state as D3hot and D3cold, its internal clock system is controlled to reduce power consumption. This section describes the clock system and power management for the clock path.

### 4.3.1 Clock system

The μPD720201 and μPD720202 use 24 MHz crystal for system clock signal. The μPD720201 and μPD720202 also use 100MHz PCI Express reference clock for system clock. Internal analog PLL generates the system clock signals for internal logic circuit. Internal system clock signals can be controlled to stop and run by the μPD720201/202 itself. Spread Spectrum Clock (SSC) for the SuperSpeed signal is generated internally.

**Figure 4-4. μPD720201/202's Clock System**



## 4.4 Latency Tolerance Reporting (LTR) mechanism

μPD720201 and μPD720202 supports Latency Tolerance Reporting (LTR). Regarding LTR mechanism, refer to Latency Tolerance Reporting ECN of PCI Express Specification.

When the LTR Mechanism Enable bit of Device Control Register is set to 1b, μPD720201 and μPD720202 enable the Latency Tolerance Reporting (LTR) mechanism.

### 4.4.1 Timing of sending LTR message

μPD720201 and μPD720202 send the LTR Message on PCI Express bus after the following events.

a) When μPD720201 and μPD720202 receive the LTM Device Notification from USB 3.0 devices
b) When μPD720201 and μPD720202 receive the SET_LTV Command from the xHCI driver (Refer to 4.16.14 in eXtensible Host Controller Interface (xHCI) Specification Revision 1.0)
c) When the LTR Mechanism Enable in Device Control 2 Register is cleared from 1b to 0b.
d) When the HCHalted bit in USBSTS register is set to 1b
e) When the internal BELT value is updated. (For example, when the device is disconnected and current BELT value is for the disconnected device)

# 5. How to Connect to External Elements

## 5.1 Handling Unused Pins

**Table 5-1. Unused Pin Connection**

| Pin | Direction | Connection Method |
|---|---|---|
| U2DPx | I/O | Connect to GND, directly or through a resistor |
| U2DMx | I/O | Connect to GND, directly or through a resistor |
| U3TXDPx | O | Open |
| U3TXDNx | O | Open |
| U3RXDPx | I | Connect to GND, directly or through a resistor |
| U3RXDNx | I | Connect to GND, directly or through a resistor |
| OCIx | I | Pull-up by 3.3V (VDD33) |
| PPONx | O | Open |
| SMIB | O | Open |
| SPISCK | O | Pull-down with 10k ohm resistor |
| SPICSB | O | Pull-down with 10k ohm resistor |
| SPISI | O | Pull-down with 10k ohm resistor |
| SPISO | I | Pull-up with 10k ohm resistor |

**Note:** When a system has fewer than 4 downstream ports (μPD720201) or fewer than 2 downstream ports (μPD720202), the implemented ports must be assigned as shown in Tables 5-2 and 5-3 below. In addition, the DisablePortCount field in the HCConfiguration register must be set accordingly.

**Table 5-2. Port configuration for μPD720201**

| DisablePortCount register | Port1 | Port2 | Port3 | Port4 |
|---|---|---|---|---|
| 00b | | | | |
| 01b | | | | X |
| 10b | | | X | X |
| 11b | | X | X | X |

X : Unused port.

**Table 5-3. Port configuration for μPD720202**

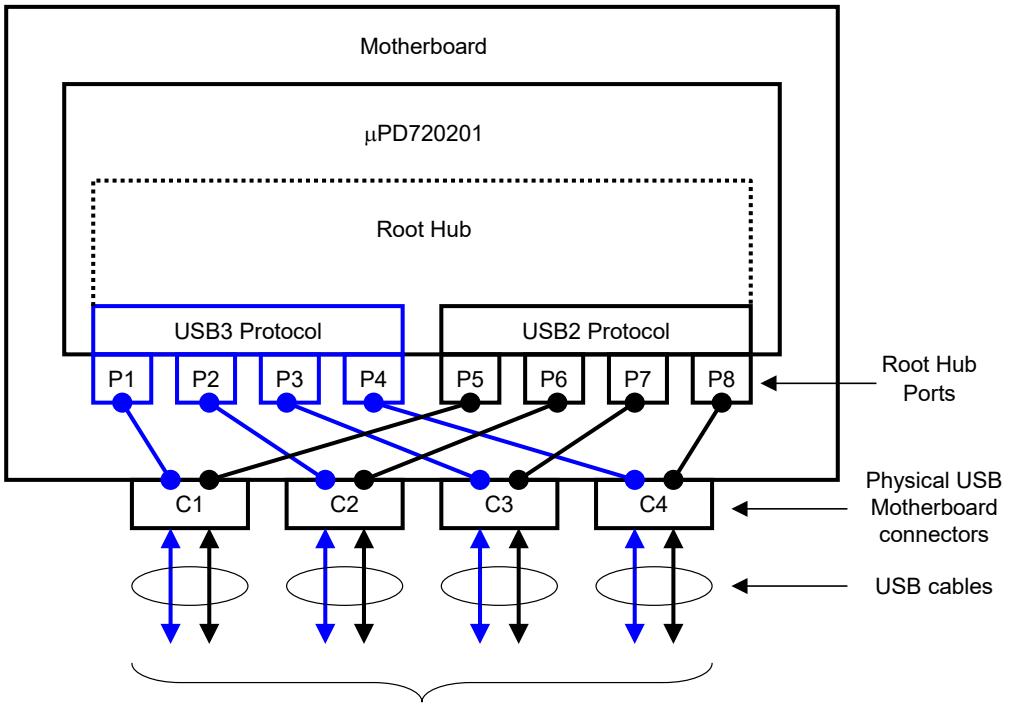
| DisablePortCount register | Port1 | Port2 |
|---|---|---|
| 00b | | |
| 01b | | X |

X : Unused port.

## 5.2 USB Port Connection

The μPD720201 implements 8 Root Hub ports (P1 – P8): 4 SuperSpeed and 4 Hi-Speed. The ports P1 to P4 provide a SuperSpeed data bus (i.e. U3RXDPx/U3RXDNx and U3TXDPx/U3TXDNx signal pairs), while P5 to P8 provide a USB2 data bus (i.e. U2DPx/U2DMx signal pair). The USB3 protocol P1 to P4 attach to the Physical USB3 compatible connector C1 to C4 respectively, while the USB2 protocol P5 and P8 attach to the Physical USB3 compatible connector C1 to C4 respectively.

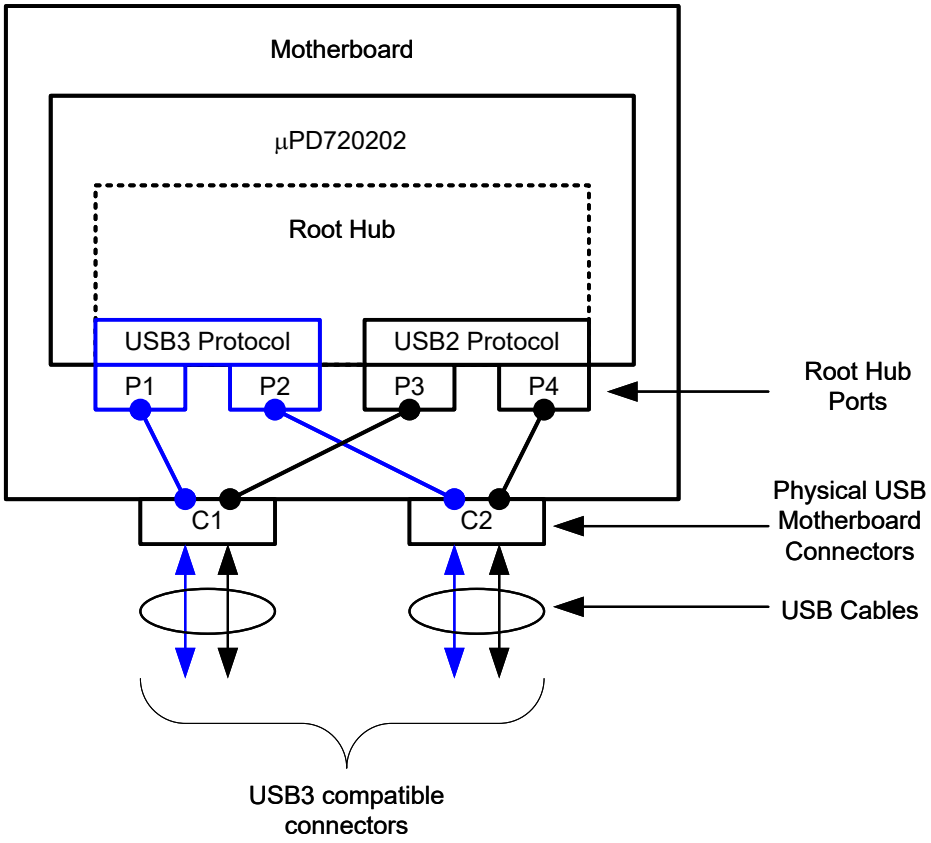
**Figure 5-1. Root Hub Port to USB Connector Mapping of μPD720201**




| USB3 Compatible Connectors | Root Hub Ports | Associated with USB Interface of μPD720201 | |
|---|---|---|---|
| C1 | P1 | U3TXDP1, U3TXDN1, U3RXDP1, U3RXDN1 | OCI1B, PPON1 |
| | P5 | U2DP1, U2DM1 | |
| C2 | P2 | U3TXDP2, U3TXDN2, U3RXDP2, U3RXDN2 | OCI2B, PPON2 |
| | P6 | U2DP2, U2DM2 | |
| C3 | P3 | U3TXDP3, U3TXDN3, U3RXDP3, U3RXDN3 | OCI3B, PPON3 |
| | P7 | U2DP3, U2DM3 | |
| C4 | P4 | U3TXDP4, U3TXDN4, U3RXDP4, U3RXDN4 | OCI4B, PPON4 |
| | P8 | U2DP4, U2DM4 | |

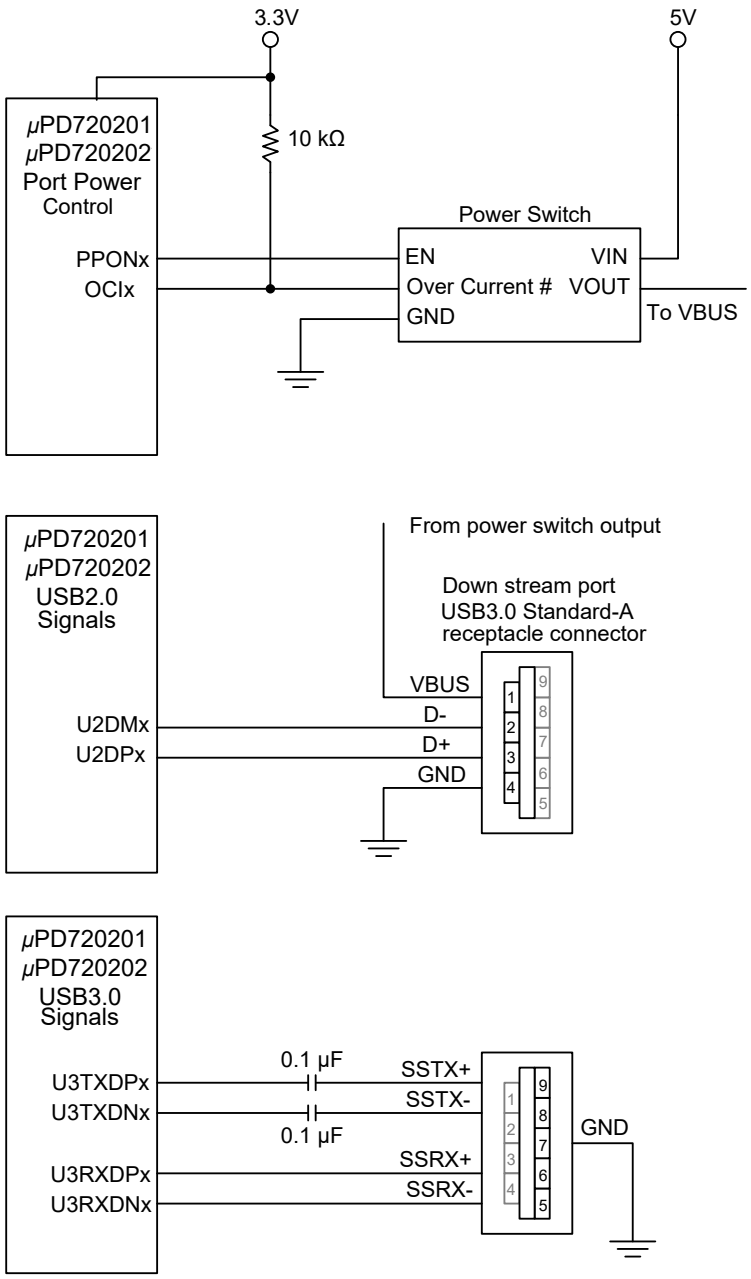
The μPD720202 implements 4 Root Hub ports (P1 – P4): 2 SuperSpeed and 2 Hi-Speed. The ports P1 and P2 provide a SuperSpeed data bus (i.e. U3RXDPx/U3RXDNx and U3TXDPx/U3TXDNx signal pairs), while P3 and P4 provide a USB2 data bus (i.e. U2DPx/U2DMx signal pair). The USB3 protocol P1 and P2 attach to Physical USB3 compatible connectors C1 and C2 respectively, while the USB2 protocol P3 and P4 attach to the Physical USB3 compatible connectors C1 and C2 respectively.

**Figure 5-2. Root Hub Port to USB Connector Mapping of μPD720202**



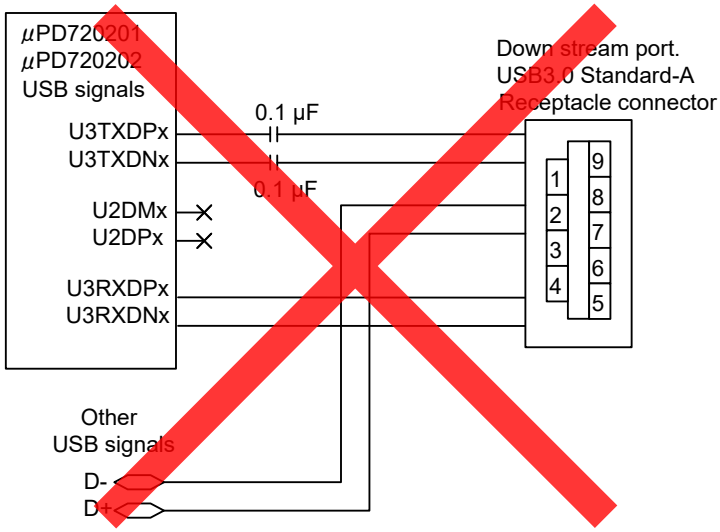

| USB3 Compatible Connectors | Root Hub Ports | Associated with USB Interface of μPD720202 | |
|---|---|---|---|
| C1 | P1 | U3TXDP1, U3TXDN1, U3RXDP1, U3RXDN1 | OCI1B, PPON1 |
| | P3 | U2DP1, U2DM1 | |
| C2 | P2 | U3TXDP2, U3TXDN2, U3RXDP2, U3RXDN2 | OCI2B, PPON2 |
| | P4 | U2DP2, U2DM2 | |

**Figure 5-3. USB Downstream Port Connection**




**Note:** The 3.3 V that pulls up OCIx must be the same 3.3 V supplied to the μPD720201 and μPD720202.

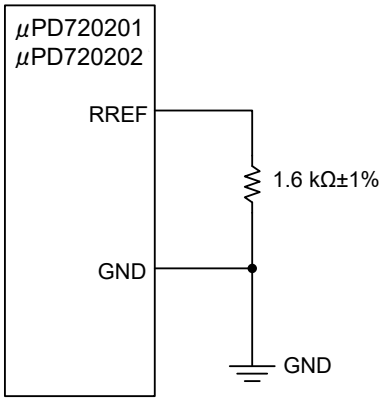
**Figure 5-4. Prohibited USB Downstream Port Connection**




**Important:** For USB 3.0 Specification compliance, the composition that only SuperSpeed signals are connected is strictly prohibited. Also, to avoid potentially severe conflicts between USB drivers, it is essential for the USB 3.0 driver to control the USB 2.0 signals as well as the USB 3.0 signals. This means the USB 2.0 signals in the USB 3.0 connector must come from the same controller (μPD720201/μPD720202) as the USB 3.0 signals.

## 5.3 Analog Circuit Connection

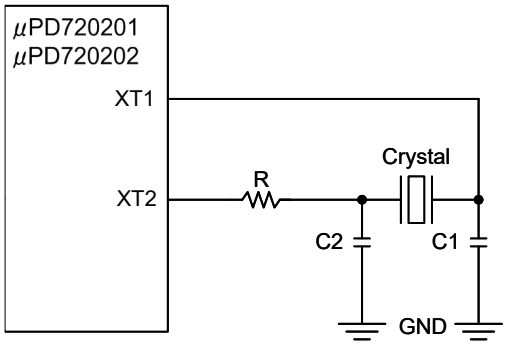
**Figure 5-5. RREF Connection**




**Note:** The board layout should minimize the total path length from RREF through the resistor to GND and path length to GND. GND must be stable.
Due to analog sensitivity, 1.62K should not be used instead of 1.60K, and two or more resistors in series or parallel should not be used in place of a single 1.60K resistor.
Although 1.6K is usually a standard 5% value, 1.60K is also commonly available in 1% tolerance.

## 5.4 Crystal Connection

**Figure 5-6. Crystal Connection**



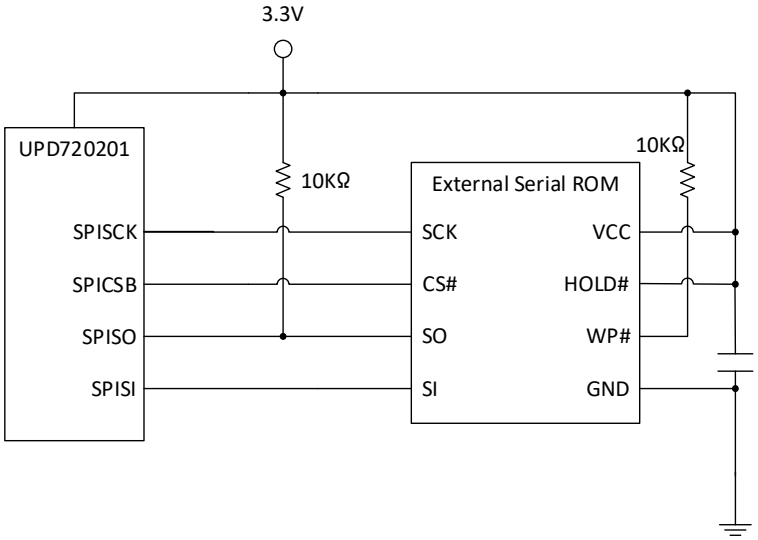

**Note:** Clock shall be 24 MHz within 100ppm. Moreover optimal crystal parameters and RC component values may be affected by the PCB layout..

## 5.5 External Serial ROM Connection

Figure 5-7 and Figure 5-8 shows the HW configuration for an external serial ROM. Refer to TN-USB-A0004A/E (μPD720202K8-701-BAA-A External Serial ROM Connection circuit update) for more detail. Refer to the application note (Document# R19AN0262EJ) regarding the supported external serial ROM list.

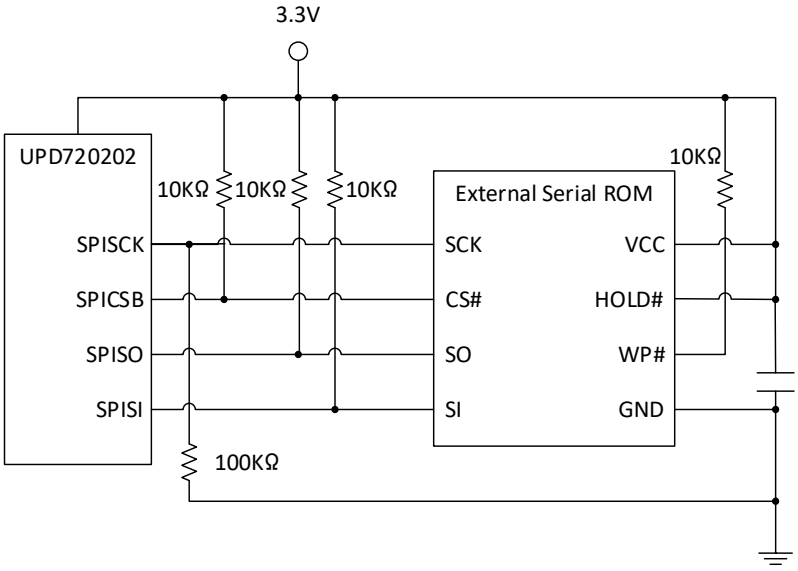
When the external serial ROM is not installed, Refer to Figure 5-9.

**Figure 5-7. External Serial ROM Connection for μPD720201**



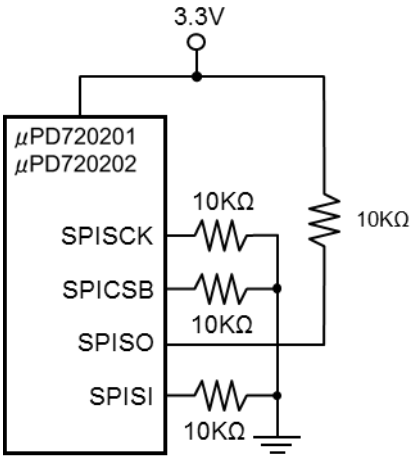

**Note:** The 3.3 V that pulls SO must be the same as the 3.3 V supplied to the μPD720201

**Figure 5-8. External Serial ROM Connection for μPD720202**




**Note:** The 3.3 V that pulls SO must be the same as the 3.3 V supplied to the μPD720202

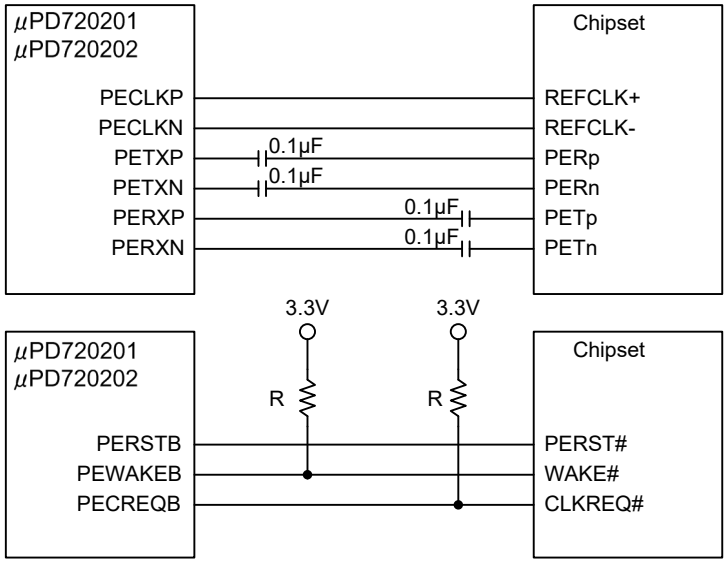
**Figure 5-9. Unused Pins Connection When the External Serial ROM Is Not Mounted**




**Note:** SPISO pin must be pulled up by VDD33 (3.3V) through a pull-up resistor in all cases.

## 5.6 PCI Express Interface Connection

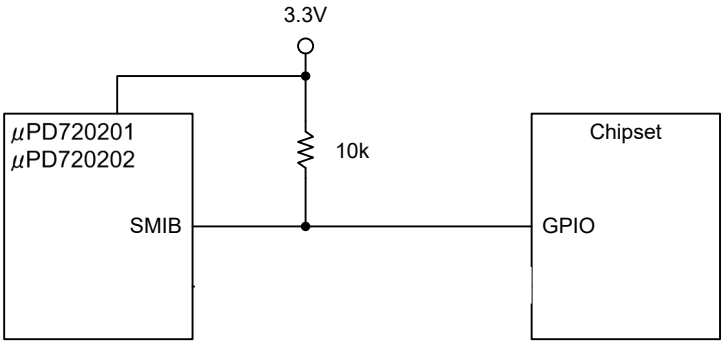
**Figure 5-10. PCI Express Interface Connection**




**Note:** PEWAKEB and PECREQB pin use an open drain buffer and should be pulled high.

## 5.7 SMIB/SMI Interface Connection

**Figure 5-11. SMIB Interface Connection**




**Note:** The 3.3 V that pulls up SMIB must be the same as the 3.3 V supplied to the μPD720201 and μPD720202.

# 6. How to Access External ROM

μPD720201 and μPD720202 (-701 versions) support the External ROM (Serial Peripheral Interface (SPI) type ROM) for firmware (FW). To access the External ROM, μPD720201 and μPD720202 support the External ROM Access Control and Status Register (ERACSR) in PCI Configuration registers. This section describes how to access the External ROM. μPD720201K8-711-BAC-A & μPD720201K8-711-BAC-M1-A & μPD720202K8-711-BAA-A & μPD720202K8-711-BAA-M1-A do not support the External ROM (Serial Peripheral Interface (SPI) type ROM). μPD720201K8-711-BAC-A & μPD720201K8-711-BAC-M1-A & μPD720202K8-711-BAA-A & μPD720202K8-711-BAA-M1-A should use the FW Download function.

## 6.1 Access External ROM Registers

Accessing the External ROM related registers uses a total of five registers in the PCI Configuration registers of μPD720201 and μPD720202.

1. External ROM Information Register (Refer to Table 3-57)
   - When the External ROM is mounted for μPD720201 or μPD720202, μPD720201 or μPD720202 sets the ROM Information.
2. External ROM Configuration Register (Refer to Table 3-58)
   - To access the External ROM, the software shall set the ROM Parameter.
3. External ROM Access Control and Status Register (ERACSR)(Refer to Table 3-60)
   - This register contains bits to access the External ROM and to check the status for the result.
4. Data0 Register (Refer to Table 3-61)
5. Data1 Register (Refer to Table 3-62)
   - Data0/1 registers are window registers for reading the External ROM data & writing FW.

Refer to the application note (Document# R19AN0262EJ) regarding the External ROM Information & Parameter which μPD720201/720202 supports. To access the External ROM, the software must set the ROM parameter before accessing the External ROM.

## 6.2 Access External ROM

This section describes the outline of accessing the External ROM sequence. μPD720201 and μPD720202 support the following functions.

1. Writing FW to the External ROM.
2. Reading ROM Data from the External ROM
3. Erasing the External ROM data of the whole chip to be “1b”. (Refer to section6.3.2.3 about the External ROM data)

### 6.2.1 How to write FW to External ROM

#### 6.2.1.1 Outline

When the System Software starts to write the FW to the External ROM, at first the System Software needs to check “External ROM Exists”. If “External ROM Exists” is ‘1b’, it indicates the External ROM is connected. After that, the System Software needs to write ‘‘53524F4Dh’ to “DATA0” and set “External ROM Access Enable” to ‘1b’. The System Software writes the first External ROM data to “DATA0”, and writes the second External ROM data to “DATA1”, then sets “Set DATA0” and “Set DATA1” to ‘1b’. After that, the System Software confirms whether “Set DATA0” is ‘0b’. If it is ‘0b’, the System Software writes the third data to “DATA0” and sets “Set DATA0”. Then the System Software confirms “Set DATA1” is ‘0b’ to write next data to “DATA1”. The System Software continues this sequence until the last data is written to “DATA0” or “DATA1”. After all data is written, the System Software must set “External ROM Access Enable” to ‘0b’.

When “External ROM Access Enable” is ‘0b’, the System Software needs to verify that “Result Code” is changed to a value other than ‘000b’. If “Result Code” is ‘001b’, FW writing is successful. If “Result Code” is ‘010b’, FW writing failed.

#### 6.2.1.2 Sequence to write the FW (External ROM data) of μPD720201 and μPD720202

1. Read “External ROM Exists” and confirm it is ‘1b’.
2. Write ‘53524F4Dh’ to “DATA0”.
3. Set “External ROM Access Enable” to ‘1b’
4. Read “Result Code” and confirm it is ‘000b’.
5. Read “Set DATA0” and confirm it is ‘0b’.
6. Write FW data to”DATA0”.
7. Read “Set DATA1” and confirm it is ‘0b’.
8. Write FW data to”DATA1”.
9. Set “Set DATA0” and “Set DATA1” to ‘1b’.
10. Read “Set DATA0” and confirm it is ‘0b’.
11. Write FW data to”DATA0”.
12. Set “Set DATA0” to ’1b’.
13. Read “Set DATA1” and confirm it is ‘0b’.
14. Write FW data to”DATA1”.
15. Set “Set DATA1” to ‘1b’.
16. Return to step 10 and repeat steps 10 to 15.
17. After writing the last data of FW, the System Software must set “External ROM Access Enable” to ‘0b’.
18. Read “Result Code” and confirm it is ‘001b’.

**Note1:** The FW of μPD720201 and μPD720202 includes the CRC16 code. The μPD720201 and μPD720202 return “Result Code” after finishing the CRC check.

**Note2:** If an immediate reload is required after the updating External ROM (sequence 18), the System Software sets “Reload” to ‘1b’. **The System Software must not set “Reload” to ‘1b’ when “Run/Stop” of USBCMD Register is ‘1b’**. At the completion of reload process, that bit cleared to ‘0b’ automatically.

### 6.2.2 How to read ROM Data from External ROM

#### 6.2.2.1 Outline

When the System Software starts to read the External ROM data from the External ROM, first the System Software needs to check “External ROM Exists”. If “External ROM Exists” is ‘1b’, it indicates the External ROM is connected. After that, the System Software needs to write ‘‘53524F4Dh’ to “DATA0” and set “External ROM Access Enable” to ‘1b’. The System Software sets “Get DATA0” and “Get DATA1” to ‘1b’ to read the External ROM data from the External ROM. After that, the System Software confirms whether “Get DATA0” is ‘0b’. If it is ‘0b’, the System Software gets the first External ROM data from “DATA0”. Then the System Software sets “Get DATA0” to ‘1b’ and confirms whether “Get DATA1” is ‘0b’. If “Get DATA1” is ‘0b’, the System Software gets the second External ROM data from “DATA1”. After that, the System Software sets “Get DATA1” to ‘1b’ and confirms whether “Get DATA0” is ‘0b’ for the getting next External ROM data.

The System Software continues this sequence until the last data is read from “DATA0” or “DATA1”. After all data is read, the System Software must set “External ROM Access Enable” to ‘0b’.

#### 6.2.2.2 Sequence to read External ROM data from External ROM

1. Read “External ROM Exists” and confirm it is ‘1b’.
2. Write ‘53524F4Dh’ to “DATA0”.
3. Set “1b” to “External ROM Access Enable”
4. Read “Result Code” and confirm it is ‘000b’.
5. Set “Get DATA0” and “Get DATA1” to ‘1b’.
6. Read “Get DATA0” and confirm it is ‘0b’.
7. Get External ROM data from “DATA0”.
8. Set “Get DATA0” to ‘1b’.
9. Read “Get DATA1” and confirm it is ‘0b’.
10. Get External ROM data from “DATA1”.
11. Set “Get DATA1” to ‘1b’.
12. Return to sequence 6 and repeat sequence 6 to sequence 11.
13. After reading the last data of External ROM data, the System Software must set “External ROM Access Enable” to ‘0b’.

### 6.2.3 How to erase the data of the whole chip to be “1b” (Chip Erase)

#### 6.2.3.1 Outline

When Chip Erase is required, first the System Software needs to check “External ROM Exists”. If “External ROM Exists” is ‘1b’, it indicates External ROM is connected. After that, the System Software needs to write ‘‘‘5A65726Fh’ to “DATA0” and set “External ROM Erase” to ‘1b’. When this operation is complete, the “External ROM Erase” is cleared to ‘0b’ automatically.

When the System Software updates the FW in the field, the System Software shall not do Chip Erase. (Refer to section 6.3.4)

#### 6.2.3.2 Sequence for Chip Erase

1. Read “External ROM Exists” and confirm it is ‘1b’.
2. Write ‘5A65726Fh’ to “DATA0”.
3. Set “1b” to “External ROM Erase”
4. Read “External ROM Erase” and confirm it is ‘000b’.

## 6.3 Data Format

This section describes the data formats for μPD720201/ μPD720202.

### 6.3.1 Firmware

The format of FW released by Renesas Electronics is shown in Figure 6-1. Each row is 8 bytes, LSB on the left. The First 2 Bytes are the header code. This value is a fixed value (55AAh). The value at offset 0004h is the FW Ver Pointer. The FW Ver Pointer indicates the address of the FW version. The other parts are undisclosed.

**Figure 6-1. Firmware**

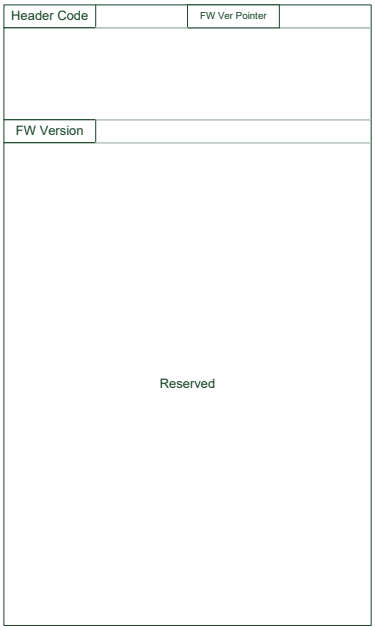



**Table 6-1. Firmware Block Description**

| Offset(Byte) | Size (Byte) | Field Name | Description |
|---|---|---|---|
| 0000h | 2 | Header Code | Header Code is 55AAh. |
| 0002h | 2 | Reserved | Reserved |
| 0004h | 2 | FW Ver Pointer | FW Version Address |
| (FW Ver Pointer)h | 2 | FW Version | FW Version. |

### 6.3.2 Vendor Specific Configuration Data Block

The System Software can write the Vendor Specific Configuration Data Block to the External ROM. The Vendor Specific Configuration Data Block configures the RENESAS Specific register when μPD720201/ μPD720202 downloads the FW from External ROM.

#### 6.3.2.1 Data Format

**Figure 6-2. Vendor Specific Configuration Data Block**

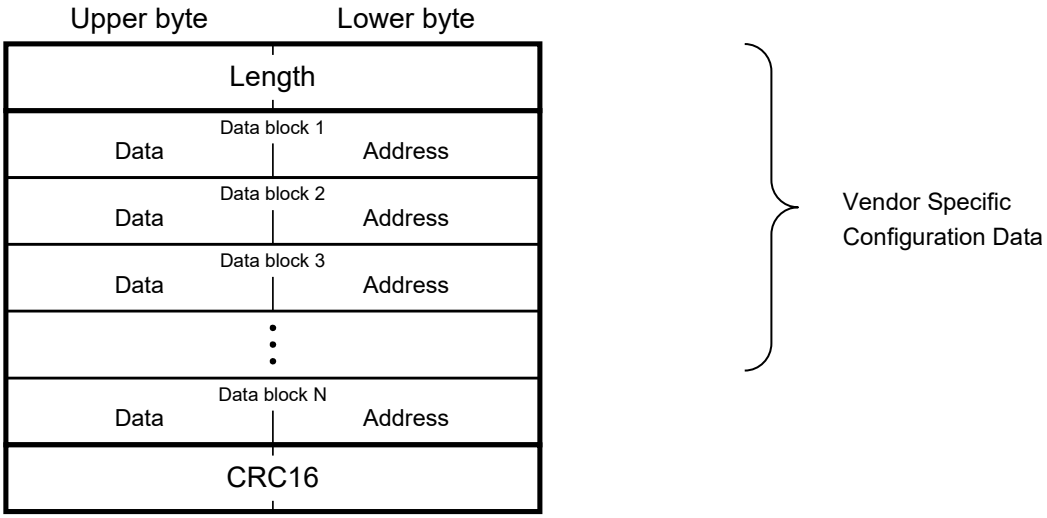



**Table 6-2. Vendor Specific Configuration Data Block Description**

| Offset(Byte) | Size (Byte) | Field Name | Description |
|---|---|---|---|
| 0000h | 2 | Length | Indicate the length of Vendor Specific Configuration Block. |
| 0002h | 2*N | Vendor Specific Configuration Data N | Indicate the Vendor Specific Configuration Data (N > 0). |
| (0002+2*N)h | 2 | CRC16 | CRC16 of Length field and Vendor Specific Configuration Data N field |

The Vendor Specific Configuration field consists of one Data block or more. Data block N consists of 2 Byte, and the first 1 Byte is Address of section 6.3.2.2, Second Byte is the value to write to the Address.

#### 6.3.2.2 Address map for Vendor Specific Configuration Block

The Vendor Specific Configuration Block has an individual address map. When μPD720201/ μPD720202 downloads the ROM data from the External ROM, μPD720201/ μPD720202 configures the RENESAS Specific register by the Vendor Specific Configuration Data Block. The address map is below.

**Table 6-3. Address Map for Vendor Specific Configuration Block**

| Address (Byte) | Register | PCI Configuration register Offset Address (Byte) |
|---|---|---|
| 03h - 00h | Subsystem Vendor ID, Subsystem ID (Refer to section 3.2.1.13 & section 3.2.1.14) | 02Fh - 02Ch |
| 0Bh - 04h | Serial Number (Refer to section 3.2.8.2) | 14Bh – 144h |

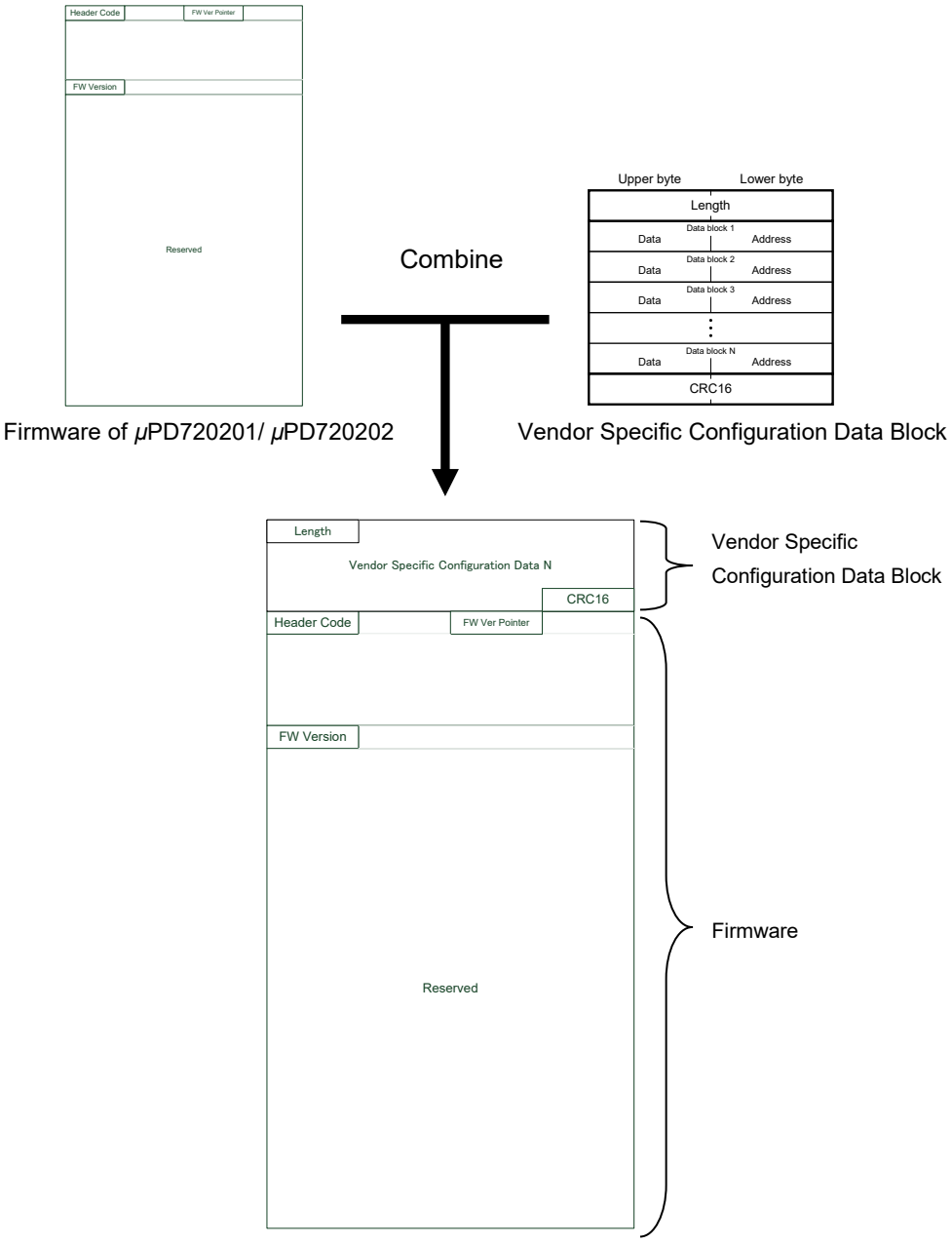
| Address (Byte) | Register | PCI Configuration register Offset Address (Byte) |
|---|---|---|
| 0Fh – 0Ch | PHY Control 0 (Refer to section 3.2.6.2) | 0DFh – 0DCh |
| 13h – 10h | PHY Control 1 (Refer to section 3.2.6.3) | 0E3h – 0E0h |
| 17h – 14h | PHY Control 2 (Refer to section 3.2.6.4) (**Note**) | 0E7h – 0E4h |
| 1Bh - 18h | Host Controller Configuration (Refer to section 3.2.6.5) | 0EBh – 0E8h |

**Note:** Even if BC_MODE_Px is set to a user defined value by the external ROM configuration, the System Software like BIOS can change the BC_MODE_Px to a user defined value. Please see the section 8.3 for the reflecting timing.

### 6.3.2.3 External ROM Data

The External ROM Data is a data for writing Firmware with Vendor Specific Configuration Data to the External ROM. This data image is the following.

**Figure 6-3. External ROM Data**



### 6.3.3 CRC16 calculation

CRC16 is generated by the following polynomial which is defined by ITU-T V.41.

$$x^{16} + x^{12} + x^5 + 1$$

The following function is an example of CRC16 calculation.

```
const UWORD16 crc_table[16] = {
        0x0000,  0x1081,  0x2102,  0x3183,  0x4204,  0x5285,  0x6306,  0x7387,   //  0 -  7
        0x8408,  0x9489,  0xA50A,  0xB58B,  0xC60C,  0xD68D,  0xE70E,  0xF78F,   //  8 - 15
};
```

```
UWORD16 update_crc16(UWORD16 crc, const BYTE *t, int len){
        int n;
        UWORD16 c = crc ^ 0xffffU;
        BYTE m;

        for(n = 0; n < len; n++) {
                m = t[n];
                c = crc_table[(c ^ m) & 0xf] ^ (c >> 4);
                c = crc_table[(c ^ (m >> 4)) & 0xf] ^ (c >> 4);
        }

        return c ^ 0xffffU;
}
```

**Note:** const UWORD16 crc_table[16] calculates the following routine.

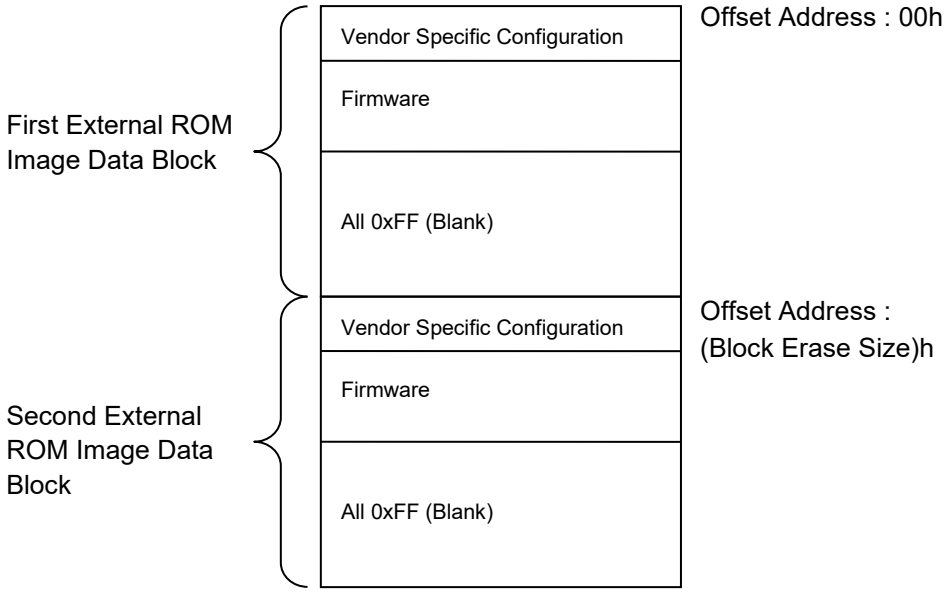
```
void make_crc_table(UWORD16 crc_table[]){
        int n,k;

        for(n = 0; n < 16; n++) {
                UWORD16 c = (UWORD16)n;
                for(k = 0; k < 4; k++) {
                        if(c & 1) c = 0x8408U ^ (c >> 1);
                        else      c >>= 1;
                }
        crc_table[n] = c;
        }
}
```

### 6.3.4 External ROM Data format

This section describes the External ROM data format of the External ROM. The External ROM Data consists of two blocks as Figure 6-4. This means that μPD720201 and μPD720202 can have two kinds of a different FW. The first is located at offset address 00h. The second is located at the offset address equal to the Block Erase Size (Refer to the application note (Document# R19AN0262EJ)).

This purpose is to prevent the ROM from being in blank status in the field. When the System Software updates the FW in the field, the System Software shall not do Chip Erase.

**Figure 6-4. External ROM Data Format**




#### 6.3.4.1 First External ROM Image Data Block of Figure 6-4

The System Software can write the External ROM Data Image to the First External ROM Image Data Block when the External ROM is in blank status. After Chip Erase, the System Software can also write the External ROM Data Image to the First External ROM Image Data Block.

This External ROM Data Block can only be erased by using Chip Erase.

#### 6.3.4.2 Second External ROM Image Data Block of Figure 6-4

The System Software can write the External ROM Data Image to the Second External ROM Image Data Block when the System Software has already written the External ROM Data Image to the First External ROM Image Data Block.

This External ROM Data Block always is erased when the System Software first sets “Set DATA0” to ‘1b’ for writing the FW.

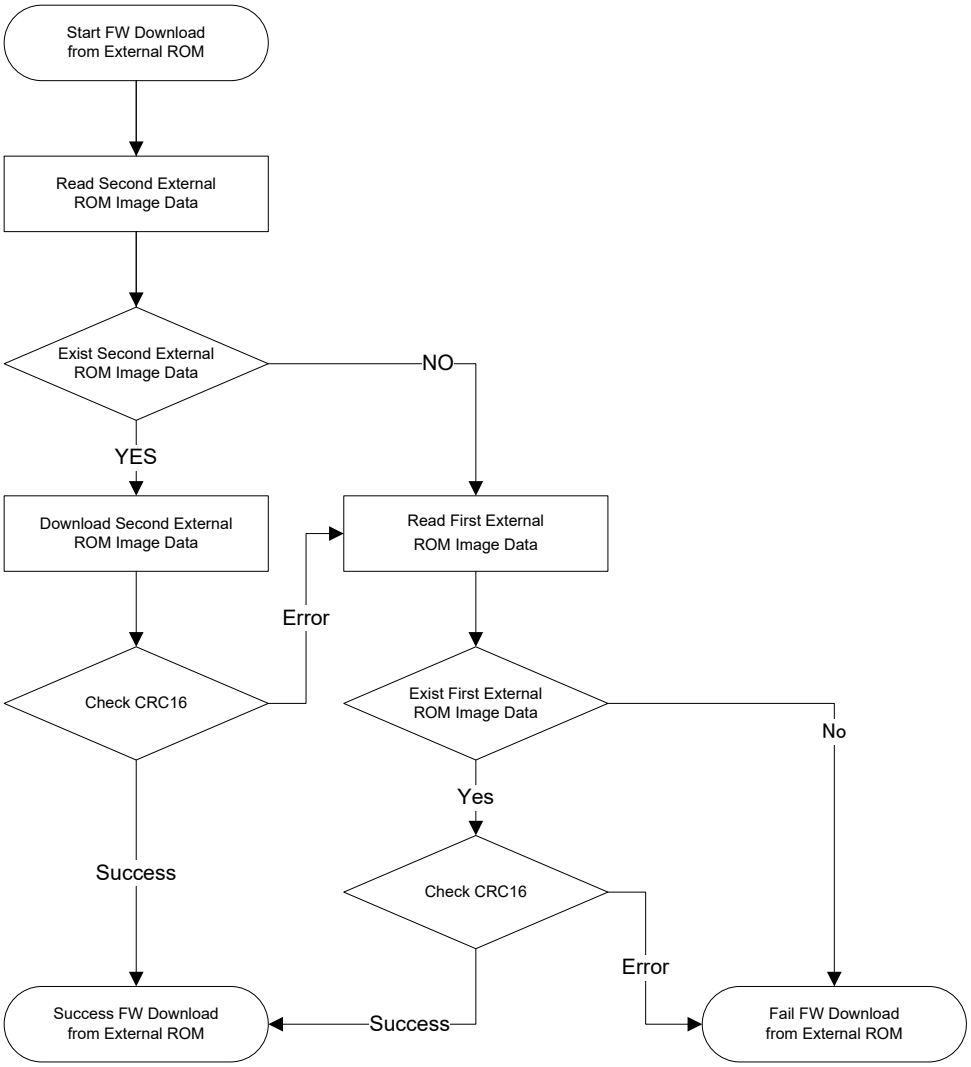
#### 6.3.4.3 Loading the FW from the External ROM

At first, when μPD720201/μPD720202 downloads the External ROM data from the External ROM, μPD720201 / μPD720202 reads data from the Second External ROM Image Data Block. If the Second External ROM Image Data is in blank status or is broken (an illegal data), μPD720201/μPD720202 reads data from the First External ROM Image Data Block and downloads the First External ROM Image Data.

If the Second External ROM Image Data Block has valid FW (External ROM data), μPD720201/μPD720202 downloads this data from the External ROM data.

**Note:** μPD720201/μPD720202 starts to download firmware from the External ROM after de-asserting PONRSTB and PERSTB.

**Figure 6-5. Loading FW from External ROM**



# 7. FW Download Interface

μPD720201 and μPD720202 supports Firmware Download Interface from the System Software (BIOS or Device Driver) for firmware. This section describes these functions.
μPD720201K8-711-BAC-A & μPD720201K8-711-BAC-M1-A & μPD720202K8-711-BAA-A & μPD720202K8-711-BAA-M1-A should use the FW Download function.
μPD720201K8-711-BAC-A & μPD720201K8-711-BAC-M1-A & μPD720202K8-711-BAA-A & μPD720202K8-711-BAA-M1-A do not support the External ROM (Serial Peripheral Interface (SPI) type ROM).

## 7.1 How to Download a Firmware into μPD720201/μPD720202

The FW Download mechanism assumes that the FW released by Renesas Electronics is located in the BIOS or other storage in advance. And BIOS or Driver reads it by DWORDS and writes it into μPD720201 and μPD720202 with the FW Download related registers (DWORD size) in the PCI Configuration Registers.

### 7.1.1 FW download registers

FW Download related registers consist of a total of three registers in PCI Configuration registers.

1. FW Download Control & Status Register (refer to Table 3-59)
   This register contains bits which control FW Download function, and status for the result.
2. DATA0 Register (refer to Table 3-61)
3. DATA1 Register (refer to Table 3-62)
   DATA0 and DATA1 are window registers for loading FW.

### 7.1.2 Outline of FW download sequences

When the System Software starts FW Download, the System Software sets “FW Download Enable” to ‘1b’. Then the System Software writes the first data to “DATA0”, and writes the second data to “DATA1”, then sets “Set DATA0” and “Set DATA1” to ‘1b’. After that, the System Software confirms whether “Set DATA0” is ‘0b’. If it is ‘0b’, the System Software writes the third data to “DATA0” and sets “Set DATA0”. Then the System Software confirms “Set DATA1” is ‘0b’ before writing the next data to “DATA1”. The System Software continues this sequence until the last data is written to “DATA0” or “DATA1”. After all data is written, the System Software must set “FW Download Enable” to ‘0b’.

When “FW Download Enable” is ‘0b’, the System Software needs to poll “Result Code” for change (other than ‘000b’). If “Result Code” is ‘001b’, FW download is a success.

### 7.1.3 FW download sequences

1. Set “FW Download Enable” to ‘1b’.
2. Read “Set DATA0” and confirm it is ‘0b’.
3. Write FW data to”DATA0”.
4. Read “Set DATA1” and confirm it is ‘0b’.
5. Write FW data to”DATA1”.
6. Set “Set DATA0” & “Set DATA1” to ‘1b’.
7. Read “Set DATA0” and confirm it is ‘0b’.
8. Write FW data to”DATA0”. Set “Set DATA0” to ‘1b’.
9. Read “Set DATA1” and confirm it is ‘0b’.
10. Write FW data to”DATA1”. Set “Set DATA1” to ‘1b’.
11. Return to step 7 and repeat the sequence from step 7 to step 10.
12. After writing the last data of FW, the System Software must set “FW Download Enable” to ‘0b’.
13. Read “Result Code” and confirm it is ‘001b’.

**Note 1**: If the Lock FW download function is needed, the System Software can lock FW download by setting “FW Download Lock” after the step 13 in the above sequence. (Refer to Table 3-59)

**Note 2**: System Software must configure RENESAS Specific registers if the Vendor specific configuration is needed. (Refer to section 3.2.6)

**Note 3**: The System Software must not set “FW Download Enable” to ‘1b’ when “Run/Stop” of USBCMD Register is ‘1b’.

**Note 4**: The “Result Code” for the External ROM Access Control and Status Register is “don’t care” during FW Download.

**Note 5**: If the External ROM is installed and the FW Download function is used, μPD720201 and μPD720202 behaves according to the FW from the FW Download function.

**Note 6**: μPD720201/μPD720202 starts to download firmware after de-asserting PONRSTB and PERSTB.

# 8. Battery Charging Function

μPD720201 and μPD720202 support the USB Battery Charging Function. It is possible to permit devices to draw VBUS current in excess of the USB2.0 specification for charging on the downstream port of μPD720201 and μPD720202. This function complies with Battery Charging Specification Rev1.2.

## 8.1 Features

- All of μPD720201 and μPD720202 downstream ports support SDP, CDP, DCP, FVO.
- It is possible to select one Battery charging mode from 8 types.
- It is possible to set the Battery charging mode on each port individually.
- VBUS shall be controlled by PPONx in each port respectively.

SDP: Standard Downsteam Port (no Battery Charging support)
CDP: Charging Downstream Port (as defined in BC1.2)
DCP: Dedicated Charging Port (as defined in BC1.2)
FVO: Fixed Voltage Output (D+ and D- are pulled up at the pre-defined voltage)

## 8.2 Battery Charging Mode

μPD720201 and μPD720202 support the Battery charging modes shown in Table 8-1.

**Table 8-1. Battery Charging Mode**

| Battery charging mode number | Battery charging port type | |
|---|---|---|
| | Under D0/D3-hot state | Under D3-cold state |
| 0 | SDP | |
| 1 | CDP | |
| 2 | SDP | DCP |
| 3 | CDP | DCP |
| 4 | SDP | FVO1 |
| 5 | CDP | FVO1 |
| 6 | SDP | FVO2 |
| 7 | CDP | FVO2 |

**Note 1:** To enable Battery charging function under S3/S4/S5, μPD720201 and μPD720202 must remain powered under S3/S4/S5. When the power is supplied only in S0 and S3, the charging function is only available in those power states.

**Note 2:** When “wake on connect function” and “wake on disconnect function” are enabled, modes 2 to 7 are not available, because these functions need to detect device attach or detach.

**Note 3:** The pre-defined voltage for D+ and D- differs between FVO1 and FVO2 to support the difference devices .

## 8.3 How to Set Up

The battery charging mode of μPD720201 or μPD720202 is set by PHY control 2 register in PCI configuration space. (Refer to section 3.2.6.4.) The PHY Control 2 register can be accessed simply and directly like any other PCI configuration register.

Setting a value in this register reflects to the downstream port after any of the following events:

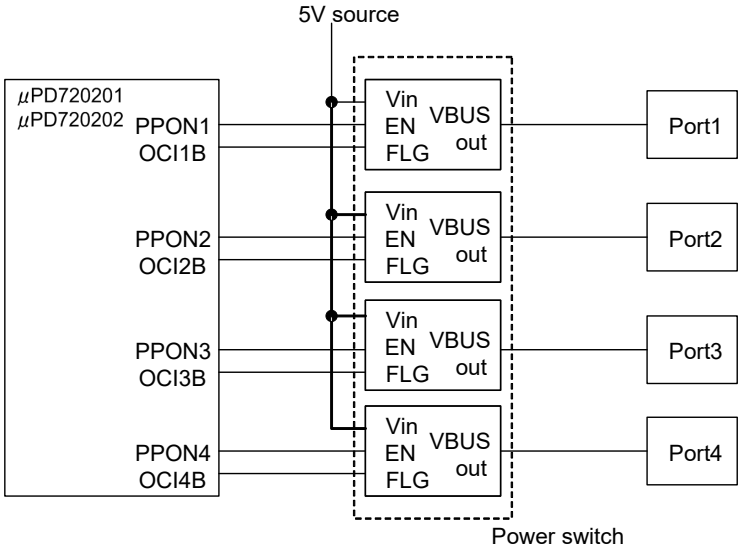
1. Resetting the host controller by using HCRST.
2. Device state transits to D3-cold.
3. Device state changes from D3-cold to D0.
4. Overcurrent is detected.

Furthermore, when External ROM for the firmware is selected in the HW configuration, it is possible to set the battery charging function by using the Vendor Specific Configuration Data Block of External ROM. Refer to chapter 6.

### 8.3.1 HW configuration requirement

Some Battery charging functions change the port type in each device state. VBUS shall be cut off temporarily when the charging port is changed, as required by the Battery Charging Specification. Thus, VBUS shall be controlled by a power switch controlled by PPONx for each port. And it is recommended to use power switches having the VBUS discharge function.

**Figure 8-1. VBUS Control Configuration with Battery Charging Function**



| REVISION HISTORY | μPD720201/μPD720202 User's Manual: Hardware |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.01 | March.31, 2011 | - | First Edition issued |
| 0.02 | May 17, 2011 | - | ● 1.3 Ordering Information<br>➢ Updated ordering information. |
| 0.03 | June 29, 2011 | - | ● Chapter1<br>➢ Changed the revision of USB Battery Charging Specification<br>● Chapter2<br>➢ Added the note to 2.3 system clock<br>● Chapter3<br>➢ Modified the description Table 5-2.<br>● Chapter5<br>➢ Added the Chapter 5 |
| 0.04 | Sep. 15, 2011 | - | ● Chapter3<br>➢ Updated Table 5-3. PCI Type 0 Configuration Space Header<br>➢ Changed the value (Default) of Max_Read_Request_Size of Table 3-41. Device Control Register (Offset Address: A8h)<br>➢ Changed the section 3.2.6.8 FW Download Control and Status Register<br>➢ Updated the section 3.3 Host Controller Capability Register<br>➢ Updated the section 3.4 Host Controller Operational Registers<br>➢ Updated the section 3.5 Host Controller Runtime Registers<br>➢ Updated the section 3.6 Doorbell Registers<br>➢ Updated the section 3.7 xHCI Extended Capabilities<br>➢ Updated the section 3.8 MSI-X / PBA Table<br>● Chapter4<br>➢ Updated Chapter 4 Power Management<br>● Chapter5<br>➢ Updated Table 5-4. Supported External Serial ROM List. |
| 1.00 | Sep. 26, 2011 | - | ● Document promoted from Preliminary to v1.00.<br>(Document No. R19UH0078E)<br>● Chapter 1<br>➢ Updated the section 1.2 Applications |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Feb. 22, 2012 | - | ● Chapter2<br>➢ Changed Table 2-7.SPI Interface (SPISO).<br>● Chapter3<br>➢ Modified the typo of Table 3-2 PCI Type 0 Configuration Space Header (Offset E4h – DCh).<br>➢ Updated Table 3-7 Revision ID Register (μPD720201).<br>➢ Updated Table 3 25 PMC Register (Offset Address: 52h)<br>➢ Updated Table 3-53 PHY Control 0 register.<br>➢ Updated Table 3-54 PHY Control 1 register.<br>➢ Updated Table 3-55 PHY Control 2 register.<br>➢ Updated Table 3-56 HCConfiguration Register.(Bit 7:0)<br>➢ Updated Table 3-57 External ROM Information Register<br>➢ Updated Table 3-58 External ROM Configuration Register.<br>➢ Changed Comment of Table 3-59 FW Download Control and Register(Bit 1, Bit 6:4).<br>➢ Modified Table 3-72 Serial Number Register (Read/Write)<br>➢ Updated Comment of Table 3-82 HCCPARAMS (Bit 3).<br>● Chapter4<br>➢ Modified 4.2 Power Management Event (PME) Mechanism<br>● Chapter5<br>➢ Changed Table 5-1 Unused Pin connection.<br>➢ Modified Figure 5-1 Root Hub Port to USB Connector Mapping of μPD720201<br>➢ Modified Figure 5-2 Root Hub Port to USB Connector Mapping of μPD720202<br>➢ Changed 5.5 External Serial ROM Connection<br>● Added Chapter 6 How to Access External ROM<br>● Added Chapter 7 Firmware Download Function<br>● Added Chapter 8 Battery Charging Function |
| 3.00 | May 25, 2012 | - | ● Chapter1<br>➢ Updated 1.3 Ordering Information<br>● Chapter3<br>➢ Modified the typo of value (Bit8:6) of Table 3-25 PMC Register. |
| 4.00 | Sep. 20, 2012 | - | ● Chapter 6<br>➢ Modified the Section 6.1 Access External ROM Registers<br>➢ Modified the Section 6.2.1.2 Sequence to write the FW (External ROM data) of μPD720201 and μPD720202<br>● Chapter 7<br>➢ Modified the Section 7.1.1 FW download registers |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 5.00 | Jan. 18, 2013 | - | ● Chapter 1<br>➢ Updated 1.1 Features<br>➢ Added “Note” to 1.3 Ordering Information<br>● Chapter 3<br>➢ Updated Table 3-55. (PHY Control 2 Register [3:0])<br>● Chapter 4<br>➢ Added the 4.4 Latency Tolerance Reporting (LTR) Mechanism<br>● Chapter 5<br>➢ Updated Figure 5-7. External Serial ROM Connection. Changed the pull-up resistor value for SPISO from 47k ohm to 10k ohm.<br>➢ Divided the supported External serial ROM list into 2 groups (Table 5-4 Supported External Serial ROM List (A) and Table 5-5 Supported External Serial ROM List (B) ) and added the comments for them.<br>● Chapter 6<br>➢ Added the description about *μ*PD720201K8-711-BAC-A & *μ*PD720202K8-711-BAA-A<br>● Chapter 7<br>➢ Added the description about *μ*PD720201K8-711-BAC-A & *μ*PD720202K8-711-BAA-A<br>● Chapter 8<br>➢ Updated section 8.1 and 8.2.<br>● All Chapters<br>➢ Modified the typo |
| 6.00 | Jan. 29, 2014 | - | ● Chapter 5<br>➢ Modified the connection method (SPISO) in Table 5-1. Changed the pull-up resistor value for SPISO from 47k ohm to 10k ohm.<br>● Chapter 6<br>➢ Added “Note” to Table 6-4 |
| 7.00 | Jun 30, 2023 | - | ● Added the new part numbers<br>● Added the figure based on TN-USB-A0004A/E (*μ*PD720202K8-701-BAA-A External Serial ROM Connection circuit update) |
| 7.10 | Sep 25, 2023 | 2 | ● Chapter 1<br>➢ Updated 1.3 Ordering Information |
| 8.00 | Mar 08, 2024 | - | ● Added the new part number<br>● Chapter 5<br>● Updated description in section 5.5<br>● Removed Table 5-4/Table 5-5 and its relevant description<br>● Chapter 6<br>● Updated description in section 6.1<br>● Removed Table 6-1 and its relevant description |
| 8.01 | Jun 03, 2024 | 2 | ● Modified 1.3 Ordering Information |

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