ADE9178

Energy Management DSP with PEN Fault Detection

FEATURES

- Metrology chip for use with any combination of the following AFE's;
  - ADE9113 (3-Channel, Isolated, Sigma-Delta ADC)
  - ADE9112 (2-Channel, Isolated, Sigma-Delta ADC)
  - ADE9103 (3-Channel, Non - Isolated, Sigma-Delta ADC)
- Can support up to 4 ADE9113/ADE9112/ADE9103 daisy chained ADCs via 4-Wire SPI
  - Supports up to a total of 12 ADC channels of data
- 4-Wire SPI interface for Host MCU communications up to 25MHz
- Total Active Energy calculation
- Class B accuracy (1%), Supports;
  - MID 2014/32/EU ANNEX V
  - EN 50470-1:2006
  - EN 50470-3:2006
  - EN 50470-3:2022
  - IEC 62052-11:2020
  - IEC 62053-21:2020
  - OIML G 22:2022
  - NIST Handbook 44:2023
- Total Apparent Energy calculation using Filtered RMS
- DC Metrology Support
- Energy Accumulation, Import and Export for reverse power/vehicle to grid (V2G) applications
- Basic Power Quality Features
  - Short duration under or over (Dip/Swell) voltage detection
  - Short duration under or over (Dip/Swell) current detection
  - Line Frequency calculation with 10mHz accuracy
  - Angles between phase voltages and currents
  - Power Factor calculation
- Configurable Phase, Gain and Offset calibration registers for all ADC channels
- 2 Configurable Calibration Frequency (CF) pulse outputs
- Configurable "No Load Detection"
- Phase Sequence Detection
- RMS on Full Cycle, RMS on Half Cycle and Filtered RMS on all ADC channels
- 45-65Hz supported frequency range
- 4 user programmable Interrupt outputs (IRQ's)
- PEN Open Fault Detection (BS 7671:2018 Amendment 1:2020)
- Waveform Streaming via UART TX pin
- Datapath multiplexing to allow any ADC data to be used for any data processing path
- Temperature range: -40°C to +105°C
- Package: 5mm x 5mm, 40-pin TQFN-EP

APPLICATIONS

- Electric Vehicle Supply Equipment
- Shunt-based polyphase meters
- Solar inverters
- Energy and Power monitoring

GENERAL DESCRIPTION

The ADE9178 is a metrology DSP for use with a combination of ADE9113/ADE9112/ADE9103 sigma delta ADC's. The ADE9178 is a high accuracy, 3-phase electrical energy measurement IC primarily for the EVSE market with SPI interface and two flexible pulse outputs. The ADE9178 can interface with up to four daisy chained ADE9113/ADE9112/ADE9103 devices via SPI protocol. The ADE9178 incorporates all the signal processing required to perform total active energy, apparent energy measurements and RMS calculations. A fixed function digital signal processor (DSP) executes this signal processing.

The ADE9178 is well suited for the EVSE market due to its broad feature set such as PEN (Protective Earth and Neutral) Open Fault Detection without the need for any additional hardware, overcurrent and overvoltage detection using RMS of half cycle/one cycle and V2X (Vehicle to Grid/Home etc.) capabilities.

The ADE9178 measures active and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires, single phase, and split phase while supporting both 50Hz and 60Hz line frequencies. The ADE9178 provides gain, offset and phase calibration features for each ADC channel. The CF1 and CF2 logic outputs provide power information that is proportional to the measured accumulated energy.

The ADE9178 can also support DC metrology with DC offset correction. The ADE9113/ADE9112/ADE9103 sigma delta ADC's provide a very low offset drift which makes this solution well suited for DC metrology.

The ADE9178 incorporates some basic power quality measurement features, such as short duration under or over voltage/current detection, line voltage period measurements, and angles between phase voltages and currents. A host MCU can be used to communicate with the ADE9178 via a 4-wire SPI interface. Waveform streaming can be accessed by the host MCU via the WAVEFORM_TX pin of the ADE9178. The ADE9178 also has 4 user-programmable interrupt pins, $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$ and $\overline{\text{IRQ3}}$, to indicate that an enabled interrupt event has occurred. The ADE9178 is available in a 40-lead, TQFN package.

Rev. A

TYPICAL APPLICATIONS CIRCUIT

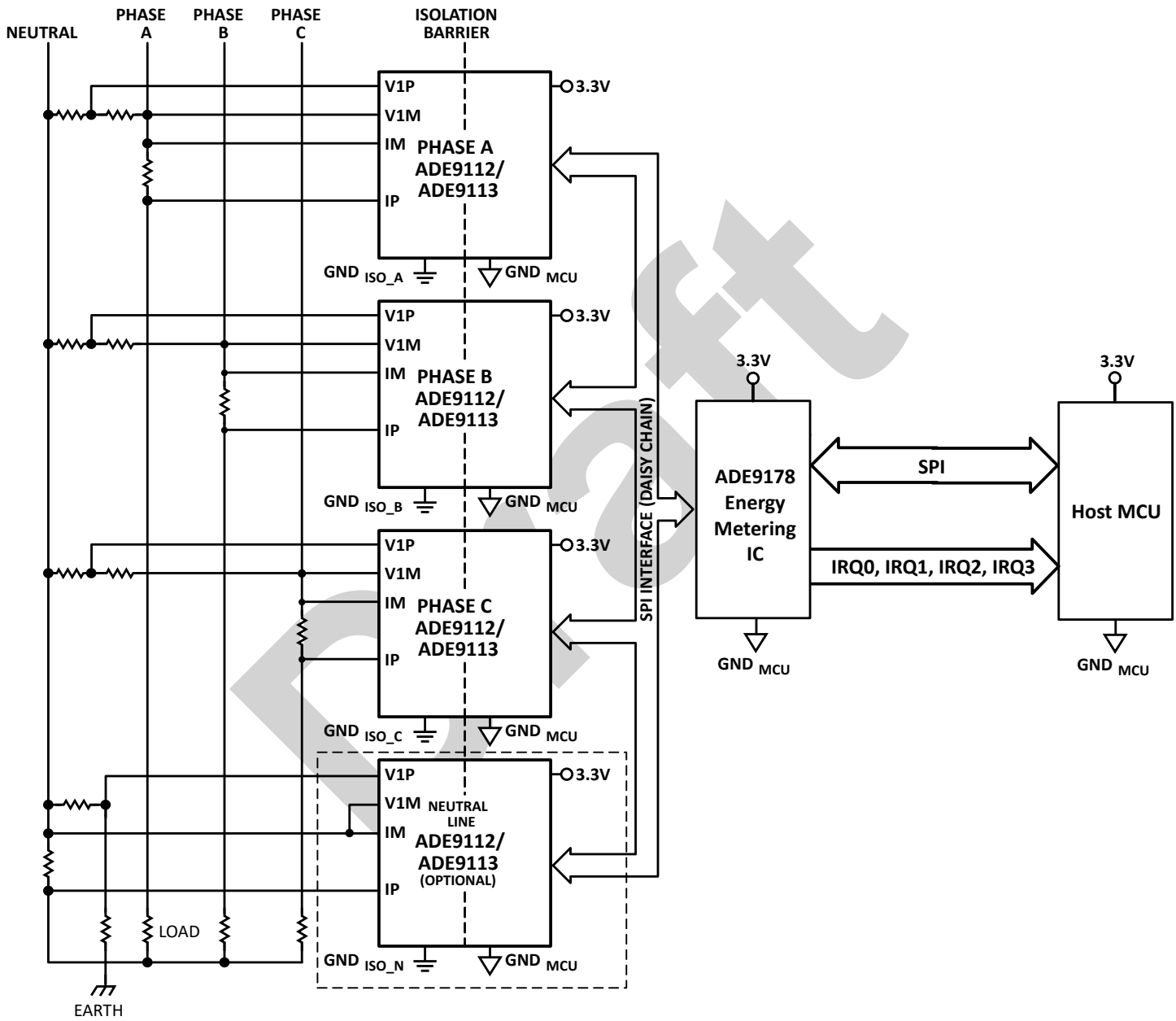


Figure 1. Typical Applications Circuit

FUNCTIONAL BLOCK DIAGRAM

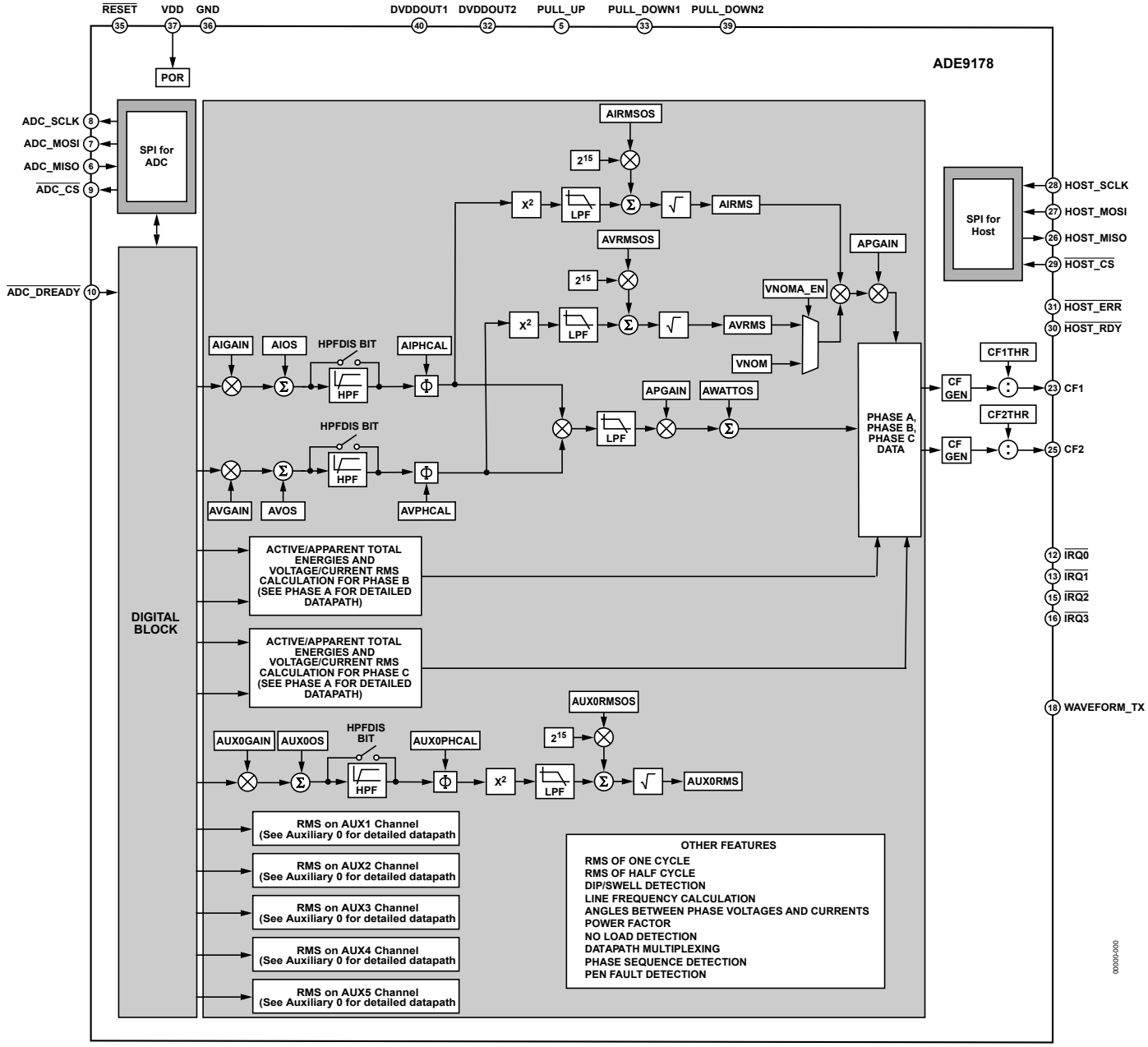


Figure 2. Functional Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

SPECIFICATIONS

SYSTEM SPECIFICATIONS, ADE9178 AND ADE9113/ADE9112/ADE9103

VDD = 3.3V ± 10%, GND = DGND = 0V, T_{MIN} to T_{MAX}=-40°C to +105°C, T_{TYP} = 25°C, HPF On

Table 1. System Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total Active Energy					
Measurement Error (Per Phase)					
Total Active Energy		TBD		%	Over a dynamic range of ___ to ___, Power Factor (PF) = ___
		TBD		%	Over a dynamic range of ___ to ___,Power Factor (PF) = ___
		TBD		%	Over a dynamic range of ___ to ___,Power Factor (PF) = ___
Total Active Energy Bandwidth		1.61		kHz	
Total Apparent Energy					
Measurement Error (Per Phase)					
Total Apparent Energy		TBD		%	Over a dynamic range of ___ to ___, Power Factor (PF) = ___
		TBD		%	Over a dynamic range of ___ to ___,Power Factor (PF) = ___
		TBD		%	Over a dynamic range of ___ to ___,Power Factor (PF) = ___
Root Mean Square (RMS) Measurements					
Filtered IRMS		TBD		%	Over a dynamic range of ___ to ___
Filtered VRMS		TBD		%	Over a dynamic range of ___ to ___
IRMS of Half Cycle		TBD		%	Over a dynamic range of ___ to ___
VRMS of Half Cycle		TBD		%	Over a dynamic range of ___ to ___
IRMS of Full Cycle		TBD		%	Over a dynamic range of ___ to ___
VRMS of Full Cycle		TBD		%	Over a dynamic range of ___ to ___
Metrology Measurements					
Phase Angle					
Measurement Error		TBD		Degrees	Line Frequency = 45Hz to 65Hz, HPF on
Power Factor					
Measurement Error		TBD			
Period					
Measurement Error		TBD		mHz	
CF1, CF2 Pulse Outputs					
Maximum Output Frequency		1		kHz	Full Scale Current and Voltage Inputs,PF = 1
Duty Cycle		TBD		%	
Active Low Pulse Width		TBD			
CF Jitter		TBD		%	
Boot Time					
System Level Boot Time[1]		TBD		ms	

[1] System Level Boot Time is the time it takes for ADE91xx and ADE9178 to power up and start processing samples.

SPECIFICATIONS

ADE9178 SPECIFICATION

Table 2. ADE9178 Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Power Supply					
VDD	2.97	3.3	3.63	V	
IDD		TBD		mA	Needs to be characterized
Boot Time					
Boot Time				ms	Needs to be characterized
Logic Inputs - ADC_MISO, HOST_MOSI, HOST_SCLK, $\overline{\text{HOST\_CS}}$, $\overline{\text{ADC\_DREADY}}$, $\overline{\text{RESET}}$					
Input High Voltage (V_{INH})	2.31			V	
Input Low Voltage (V_{INL})			0.99	V	
Internal Capacitance (C_{IN})		4		pF	
Logic Outputs - $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$, ADC_MOSI, ADC_SCLK, $\overline{\text{ADC\_CS}}$, HOST_MISO, CF1					
Output High Voltage (V_{OH})	2.9			V	
Isource		6		mA	
Output Low Voltage (V_{OL})		0.2	0.4	V	
Isink		6		mA	
Logic Outputs - CF2, $\overline{\text{HOST\_RDY}}$, $\overline{\text{HOST\_ERR}}$					
Output High Voltage (V_{OH})	2.9			V	
Isource		10		mA	
Output Low Voltage (V_{OL})		0.2	0.4	V	
Isink		10		mA	

SPI INTERFACE TIMING PARAMETERS

Table 3. SPI Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{CS}}$ to SCLK Positive Edge	t_{SS}		10		ns
SCLK Frequency	f_{SCLK}			25	MHz
SCLK Period	t_{SCLK}		$1/f_{SCLK}$		ns
SCLK Low Pulse Width	t_{SL}		$t_{SCLK}/2$		ns
SCLK High Pulse Width	t_{SH}		$t_{SCLK}/2$		ns
Data Input Setup Time Before SCLK Edge	t_{DSU}		5		ns
Data Input Hold Time After SCLK Edge	t_{DHD}		1		ns
MISO Disable After $\overline{\text{CS}}$ Rising Edge	t_{DIS}		10		ns
$\overline{\text{CS}}$ High After SCLK Edge	t_{SFS}		10		ns
$\overline{\text{CS}}$ High Pulse Width	t_{CH}		$1/f_{SCLK}$		ns

SPECIFICATIONS

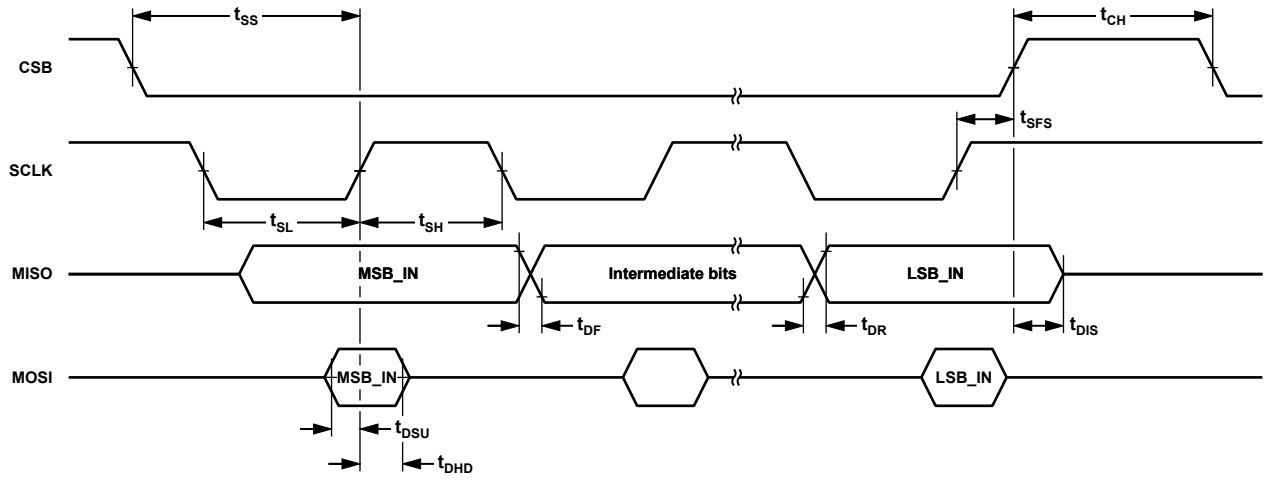


Figure 3. SPI Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
VDD to GND	-0.3V to +3.63V
$\overline{\text{RESET}}$, GPIO's to GND	-0.3V to VDD + 0.3V
Total Current into ALL GPIO Combined	100mA
GND	100mA
Output Current (sink) by Any GPIO Pin	25mA
Output Current (source) by Any GPIO Pin	-25mA
Continuous Package Power Dissipation 40 TQFN-EP (multilayer board) TA = +70°C (derate 35.7mW/°C above +70°C)	2857.10mW
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Pin TQFN-EP	45.0	2.0	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

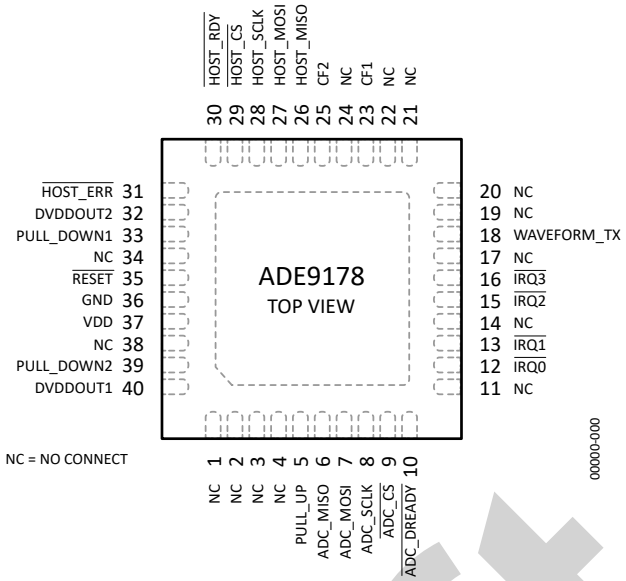


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output	Active Low/High	Description
1	NC	N/A	N/A	No Connect.
2	NC	N/A	N/A	No Connect.
3	NC	N/A	N/A	No Connect.
4	NC	N/A	N/A	No Connect.
5	PULL_UP	N/A	N/A	1kΩ Pull Up to VDD.
6	ADC_MISO	Input	Active High	Data Input for the ADC SPI Port to the supported AFE's.
7	ADC_MOSI	Output	Active High	Data Output for the ADC SPI Port from the supported AFE's.
8	ADC_SCLK	Output	Active High	Serial Clock Output for the ADC SPI Port.
9	$\overline{\text{ADC\_CS}}$	Output	Active Low	Chip Select for ADC SPI port.
10	$\overline{\text{ADC\_DREADY}}$	Input	Active Low	DREADY Input, Signal to let ADE9178 know that ADC samples are ready.
11	NC	N/A	N/A	No Connect.
12	$\overline{\text{IRQ0}}$	Output	Active Low	User Programmable Interrupt Request Output.
13	$\overline{\text{IRQ1}}$	Output	Active Low	User Programmable Interrupt Request Output.
14	NC	N/A	N/A	No Connect.
15	$\overline{\text{IRQ2}}$	Output	Active Low	User Programmable Interrupt Request Output.
16	$\overline{\text{IRQ3}}$	Output	Active Low	User Programmable Interrupt Request Output.
17	NC	N/A	N/A	No Connect.
18	WAVEFORM_TX	Output	Active High	Waveform Streaming via a UART TX pin.
19	NC	N/A	N/A	No Connect.
20	NC	N/A	N/A	No Connect.
21	NC	N/A	N/A	No Connect.
22	NC	N/A	N/A	No Connect.
23	CF1	Output	Active High	Calibration Frequency (CF) Logic Output. This output provides power information and is used for operational and calibration purposes.
24	NC	N/A	N/A	No Connect.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Input/Output	Active Low/High	Description
25	CF2	Output	Active High	Calibration Frequency (CF) Logic Output. This output provides power information and is used for operational and calibration purposes.
26	HOST_MISO	Output	Active High	Data Output for the SPI Port to the Host MCU.
27	HOST_MOSI	Input	Active High	Data Input for the SPI Port from the Host MCU.
28	HOST_SCLK	Input	Active High	Serial Clock input from the Host MCU.
29	$\overline{\text{HOST\_CS}}$	Input	Active Low	Chip Select input for Host SPI Port.
30	$\overline{\text{HOST\_RDY}}$	Output	Active Low	Flag to let the Host MCU know that response from the host command is ready.
31	$\overline{\text{HOST\_ERR}}$	Output	Active Low	Flag to let the Host MCU know there was an error during the command processing.
32	DVDDOUT2	N/A	N/A	Bypass with 4.7nF to GND.
33	PULL_DOWN1	N/A	N/A	1kΩ Pull Down to GND.
34	NC	N/A	N/A	No Connect.
35	$\overline{\text{RESET}}$	Input	Active Low	External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic) and begins execution.
36	GND	N/A	N/A	Ground Reference for the Input Circuitry.
37	VDD	Input	N/A	Supply Voltage. This pin provides the supply voltage. For specified operation, maintain the supply voltage at 3.3 V ± 10%. Bypass with 100nF to GND and 1µF with 10mΩ to 150mΩ ESR to GND.
38	NC	N/A	N/A	No Connect.
39	PULL_DOWN2	N/A	N/A	1kΩ Pull Down to GND.
40	DVDDOUT1	N/A	N/A	Bypass with 100nF to GND and 1µF with 10mΩ to 150mΩ ESR to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

TEST CIRCUIT

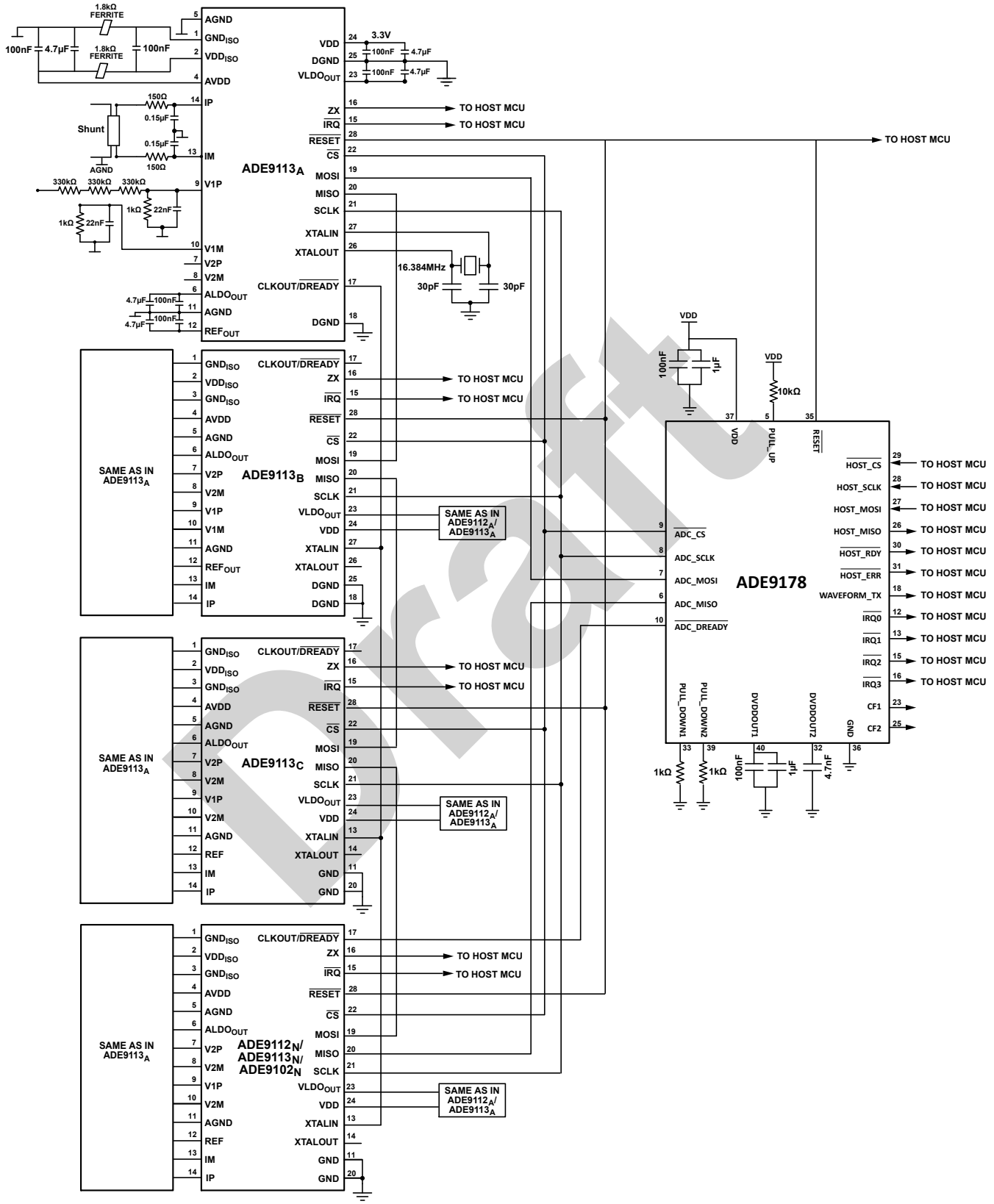


Figure 5. ADE9178 +ADE91xx Test Circuit

TERMINOLOGY

Please refer to the Analog WIKI for common terminology: https://wiki.analog.com/resources/eval/user-guides/metrology-terminology

ADC AND HOST SPI INTERFACE

ADC SPI INTERFACE

ADE9178 receives ADC samples through ADC SPI interface. The application should connect the ADC in daisy chain mode as explained in ADE9113 data sheet. The ADC clock should be provided by crystal to PHASE A ADC. Clock for PHASE B, PHASE C AND PHASE N ADC's can be connected to DREADY/CLKOUT of PHASE A as shown in figure. The DREADY of last ADC in the chain should be connected to DREADY input pin of ADE9178. Figures below show the required connections when 4 ADCs and 3 ADCs are connected to ADE9178. Single and 2 ADC configurations are also supported.

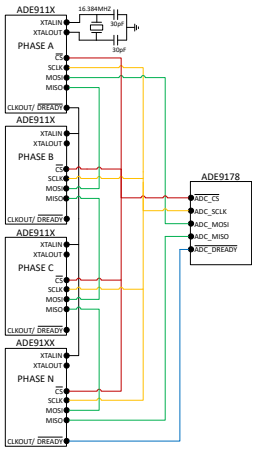


Figure 6. 4 ADC's Connection Diagram to ADE9178

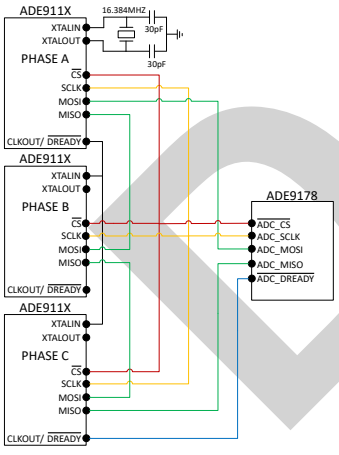


Figure 7. 3 ADC's Connection Diagram to ADE9178

ADE9178 supports three voltage (referred as AV, BV , CV) and three current channels (referred as AI, BI, CI) for metrology measurements and 6 auxiliary channels (AUX0, AUX1, …, AUX5) for other measurements. The ADE9178 provides a multiplexer option that allows any ADC output to be redirected to any processing data path by writing appropriate slot number to ADC_REDIRECT0 and ADC_REDIRECT1 register.

In above connections ADC SPI frames will contain data in following order (with last ADC data coming first). This position in SPI frames is referred as slots in this document where SLOT0 is the I channel of the ADC which has its MISO connected directly to ADE9178.

Table 7. ADC Channel to ADE9178 SLOT Mapping for 4 and 3 ADC Configurations

4 ADC's Connected (ADC_CONFIG:NUM_ADC = 0x4)			3 ADC's Connected (ADC_CONFIG:NUM_ADC = 0x3)		
Phase	ADC Channel	ADE9178 SLOT	Phase	ADC Channel	ADE9178 SLOT
Phase N	I	SLOT0	Phase C	I	SLOT0
Phase N	V1	SLOT1	Phase C	V1	SLOT1
Phase N	V2	SLOT2	Phase C	V2	SLOT2
Phase C	I	SLOT3	Phase B	I	SLOT3
Phase C	V1	SLOT4	Phase B	V1	SLOT4
Phase C	V2	SLOT5	Phase B	V2	SLOT5
Phase B	I	SLOT6	Phase A	I	SLOT6
Phase B	V1	SLOT7	Phase A	V1	SLOT7
Phase B	V2	SLOT8	Phase A	V2	SLOT8
Phase A	I	SLOT9	Ignored	n/a	SLOT9
Phase A	V1	SLOT10	Ignored	n/a	SLOT10
Phase A	V2	SLOT11	Ignored	n/a	SLOT11

Note, this means for a change in NUM_ADC value away from default (0x4) the ADC_REDIRECT0 and ADC_REDIRECT1 registers MUST be updated. For example, with a 3 ADC configuration outlined in Figure 7 above, SLOT0 will now be mapped to the current channel of phase C rather than the current channel of phase N.

The table below shows the default values to write to ADC_REDIRECT0 and ADC_REDIRECT1 for different NUM_ADC values assuming that the phase order matches the examples outlined above (ADE9178 MOSI connected to the first ADC in the chain and ADE9178 MISO connected to the last ADC in the chain).

For channels that are not present, a slot number of 0x1F should be written to corresponding bitfields of the ADC_REDIRECT0 and ADC_REDIRECT1.

Table 8. Default ADC_REDIRECTx Values

NUM_ADC Value	ADC_REDIRECT0 Value	ADC_REDIRECT1 Value
0x4	0x6431D2A	0x410150B
0x3	0x1190C7	0x3FFF88A8
0x2	0x3FF00464	0x3FFFFC45
0x1	0x3FFFFC01	0x3FFFFFE2

By default, for above connection, following mapping is done where AV1, BV1, CV1, are mapped to AV, BV, and CV AND AV2, BV2, CV2, NI, NV1, NV2 are mapped to auxiliary channels as follows.

ADC AND HOST SPI INTERFACE

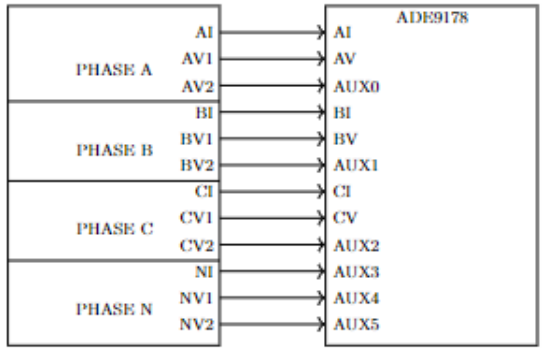


Figure 8. ADC to ADE9178 Channel Mapping

Multiple ADC Synchronization

If multiple ADCs are connected to ADE9178, the application can periodically issue synchronization of these ADCs through register ADC_CONTROL register. This ensures that all ADCs sample at the same time. The ADC_CONTROL register can be used to synchronize all ADCs periodically. To ensure correct operation it is recommended to synchronize ADCs by writing ADC_CONTROL = 0x5 (SYNC = 1 , RUN = 1) once every day. ADE9178 will perform a synchronization sequence if the ADCs are out of sync. Note that energy calculation can be disrupted for ~1ms during synchronization if it is required.

HOST SPI INTERFACE

The SPI interface of the ADE9178 always acts as the subordinate and consists of six pins. These pins are shown with prefix HOST in the diagram below. Apart from standard SPI pins, $\overline{\text{HOST\_RDY}}$ or $\overline{\text{HOST\_ERR}}$ signal is used to indicate response is ready or error has occurred.

Data shifts into the device at the MOSI logic input on the falling edge of SCLK, and the device samples the input data on the rising edge of SCLK. Data shifts out of the ADE9178 at the MISO logic output on the falling edge of SCLK and must be sampled by the main device on the rising edge of SCLK. The least significant byte of the word is shifted in and out first. The most significant bit of each byte is sent first.

The default state of MISO pin is high. The ADE9178 is compatible with the following micro controller SPI port clock polarity and phase settings:

CPOL = 1 and CPHA = 1(typically Mode 3).

The maximum serial clock frequency supported by this interface is 25MHz.

ADE9178 takes time to a process read or write command. ADE9178 raises $\overline{\text{HOST\_RDY}}$ when the command is successful. The host program should initiate the SPI read only after this IRQ is raised.

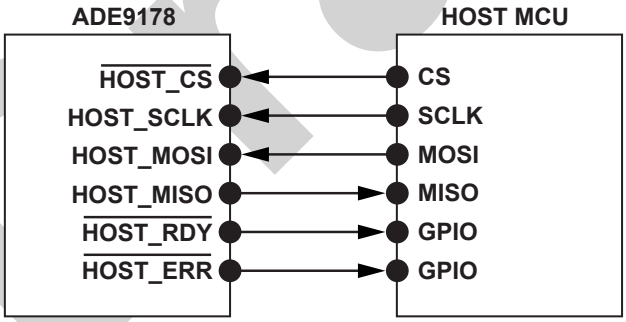


Figure 9. ADE9178 to HOST MCU SPI Connection

Table 9. HOST SPI Pin Description

Pins	Description
$\overline{\text{HOST\_CS}}$, HOST_SCLK, HOST_MOSI, HOST_MISO	Standard 4 wire SPI pins
$\overline{\text{HOST\_ERR}}$	Indicates last command has thrown error.
$\overline{\text{HOST\_RDY}}$	Indicates response for last command is ready

The $\overline{\text{HOST\_CS}}$ input must stay low for the whole SPI transaction. Bringing $\overline{\text{HOST\_CS}}$ high during a data transfer operation aborts the transfer. A new transfer can be initiated by returning the $\overline{\text{HOST\_CS}}$ logic input low. Therefore, if the application does not need to read back the register value (success case) or the status bits (error case) after a write command the application MCU can toggle $\overline{\text{HOST\_CS}}$ to ignore the returned value. Note, $\overline{\text{HOST\_CS}}$ must be low for a minimum of TBD for the command to successfully abort.

It is not recommended to tie $\overline{\text{HOST\_CS}}$ to ground because the high to low transition on $\overline{\text{HOST\_CS}}$ starts the ADE9178 SPI transaction.

ADC AND HOST SPI INTERFACE

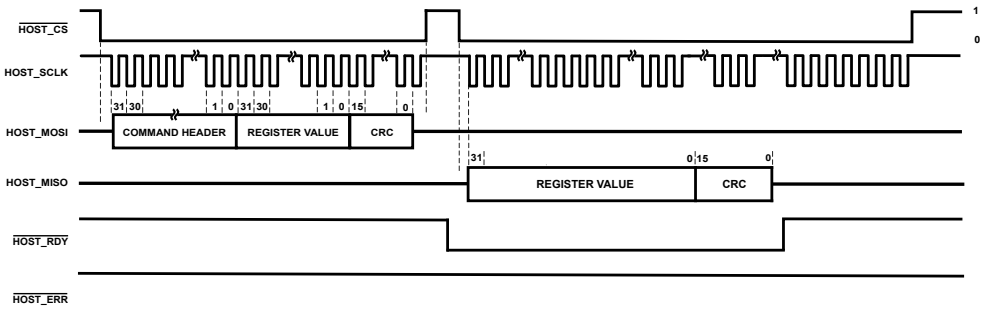


Figure 10. Register Write SPI Protocol - Success Case

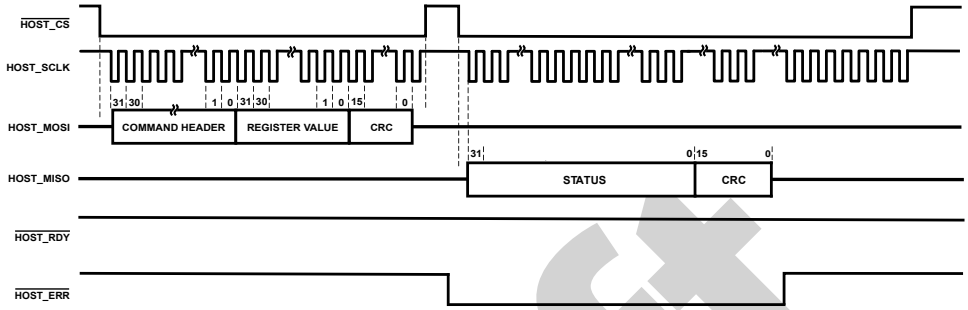


Figure 11. Register Write SPI Protocol - Error Case

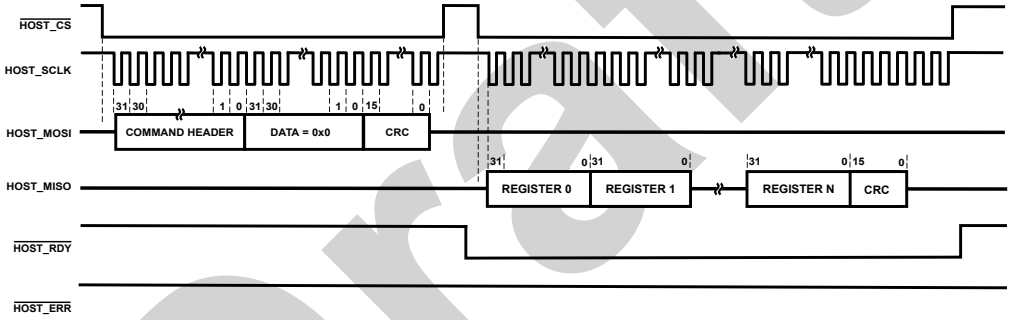


Figure 12. Register Read SPI Protocol - Success Case

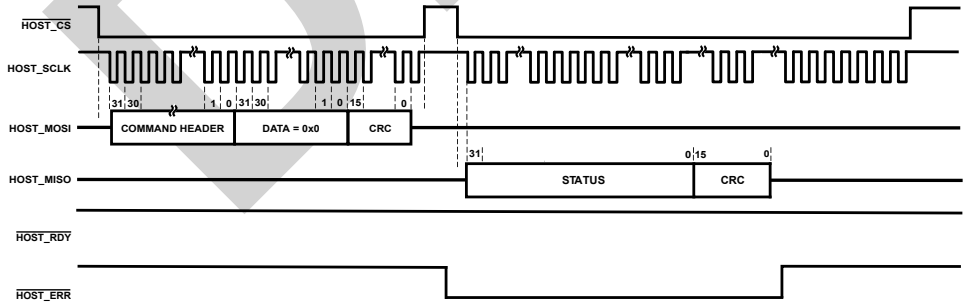


Figure 13. Register Read SPI Protocol - Error Case

Note that all data including register values for write, read response and status are 32 bit values and sent over the SPI as least significant byte first as shown in figure.

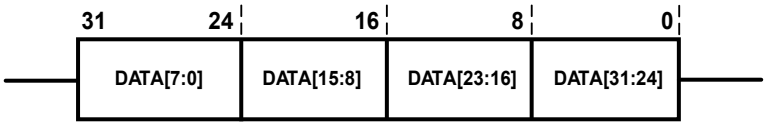


Figure 14. ADE9178 Data/Response SPI Frame Format

ADC AND HOST SPI INTERFACE

The command header is also a 32 bit field with 24th bit indicating if the command is read or write. The format for the read and write command header is shown in the figures below

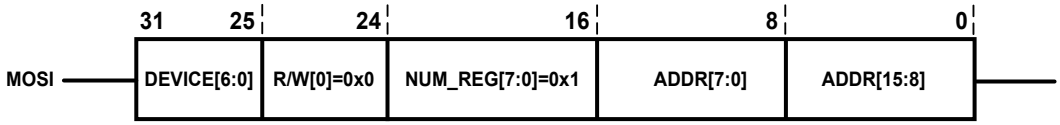


Figure 15. Write Command Header

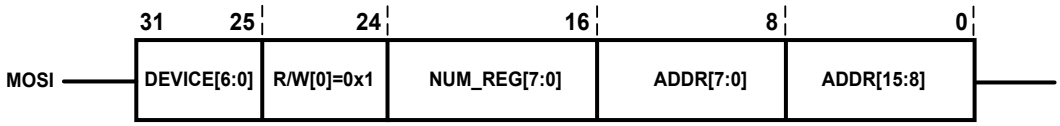


Figure 16. Read Command Header

Table 10. Command Header Details

Field	Description
ADDR	Address of registers which need to be accessed
R/W	1 - Read 0 - Write
Device	0 - ADE9178 1 - ADC1 - ADC connected to ADC_MISO pin of ADE9178 2 - ADC2 - ADC connected to ADC_MOSI pin of ADC1 3 - ADC3 - ADC connected to ADC_MOSI pin of ADC2 4 - ADC4 - ADC connected to ADC_MOSI pin of ADC3 5 - All ADCs
NUM Registers	Number of registers to be read. ADE9178 will send those many registers starting from the address in the command header. Note that this shall be 1 for write commands. If the device field of the command is not ADE9178 (0) , "NUM_REGISTER" field is ignored and always two 8 bit registers are returned as response. Refer to ADC SPI Interface for more details.

In case of error, 4 bytes status code is sent as response for read and write command.

The following table outlines the status codes that could be returned.

Table 11. Status Code Description

Code	Description	Most Common Reason for Error	Solution
0x1	Invalid address	Address present in ADDR field of command header is wrong	Use macros in ade9178.h for address
0x2	Invalid device Id	Device field is more than 5	Check device field is less than 5
0x3	Read/write to more than one register is not supported for this address	NUM_REGISTERS field > 1 for write command	Make NUM_REGISTERS = 1 for write command
0x4	Attempted write to a read only register	The address of the requested write is read only register	Check the address that if it is really the one intended to write
0x5	Insufficient baud rate for waveform streaming	Baud rate provided BAUD_RATE field of WFS_CONFIG register is not sufficient to stream all channels enabled in WFS_CONFIG register	Update WFS_CONFIG such that baud rate is large enough to stream enabled channels
0x6	Configuration registers are locked	A lock command was issues previously to lock write to all configuration registers	Unlock config registers by writing 0 to CONFIG_LOCK register
0x7	Invalid ADC_REDIRECT configuration	Incorrect values are written to ADE_REDIRECT0 or ADC_REDIRECT1 register	Verify if the redirect register values are correct or not.

ADC AND HOST SPI INTERFACE

Table 11. Status Code Description (Continued)

Code	Description	Most Common Reason for Error	Solution
0x8	Command failed to execute	Command failed but reason is not clear	Report the command sequence to support team
0x9	ADC not initialized	ADC initialization has failed and communication with ADCs is not established.	Initialize the ADCs by writing 2 to ADC_CONTROL register

Support for Reading and Writing ADC registers

ADE9178 provides support for reading and writing ADC registers by configuring the 'device' field of the command. If the device is a non-zero value less than 5, the read or write command is sent to corresponding ADC. If the 'device' field is 5, the same command is sent to **ALL** ADCs in the daisy chain. ADC reads return two 8 bit values, the value at the address in the command header and the value at the consecutive address.

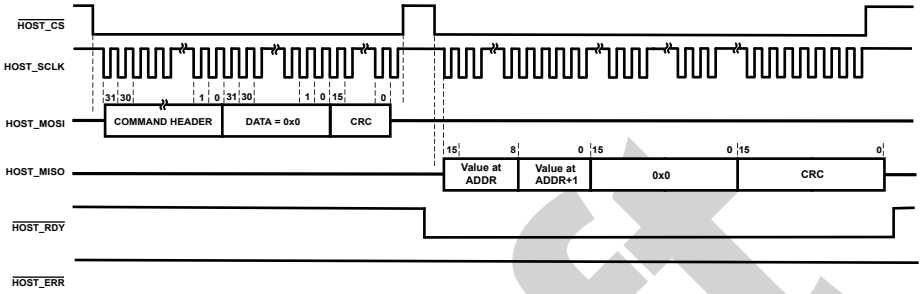


Figure 17. Protocol to Read ADC Registers Individually

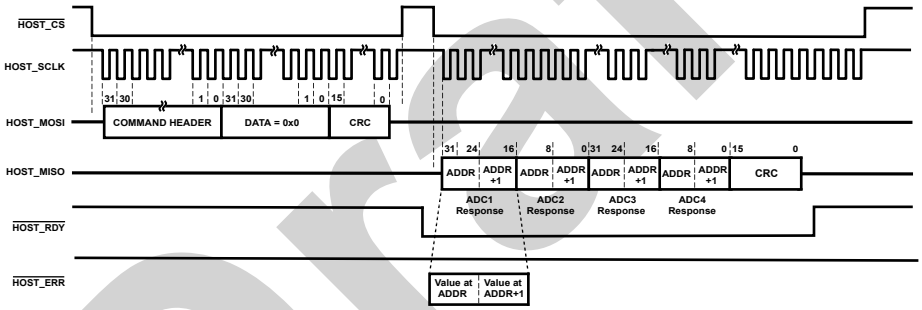


Figure 18. Protocol to Read ADC Registers Simultaneously

See Table 10 to relate ADC number to physical ADC channel e.g. ADC1 relates to the ADC that is connected to the ADC_MISO pin of the ADE9178.

For single ADC write the protocol is the same as outlined in Figure 10 except the register value in the "Command Header" and the "Register Value" is stored in the lower 8 bits of the 32 bit register (upper 24 bits are 0 padded). For multiple ADC write it is important to note that the same register value is written to **ALL** ADCs.

SPI Protocol CRC

The ADE9178 SPI port calculates a CRC of the data sent out on its MISO pin so that the integrity of the data received by the main can be checked and it is appended to the SPI read data as part of the SPI transaction. Also ADE9178 verifies the CRC of the data received on its MOSI pin, so that any bit flip during the command read/write can be detected. The CRC algorithm implemented within the ADE9178 is based on the CRC-16-CCITT algorithm with initial value 0xFFFF. The CRC will be the last data sent in the transaction (after Command header and Register value)

The CRC verification is enabled by default. User can disable the CRC by writing CRC_DIS bit of CONFIG0 to 1 (write 0x20000180 to disable CRC check but keep all other defaults the same). In case of incorrect CRC ADE9178 will not execute the command. The $\overline{\text{HOST\_ERR}}$ pin and status codes (ADI_SM_RESULT_CRC_ERROR) are used to indicate the incorrect CRC to the user.

ADC AND HOST SPI INTERFACE

CRC of Configuration Registers

The configuration register CRC feature monitors many register values. It also optionally includes 15 register sets that are individually selectable in the CRC_OPTEN register. The result is stored in the CRC_RSLT register. If any of the monitored registers change value, the CRC_RSLT changes as well, and the CRC_CHG bit in the STATUS 1 register is set; this can also be configured to generate an interrupt on $\overline{\text{IRQ1}}$. The order in which the registers are calculated is given in table below in register details section

Configuration Lock

To prevent accidental overwriting of configuration registers, a provision to lock writing of configuration registers are provided. The user can write 0x1 CONFIG_LOCK register. After this all writes to configuration registers other than CONFIG_LOCK will return error. The configuration register write can be unlocked by writing 0x0 to CONFIG_LOCK register.

FULL SCALE CODES AND CONVERSION EQUATIONS

ADE9178 calculates various parameters on the input channels and provides output as 32-bit registers in fixed point format. It can be easily converted to physical units such as Amperes, Volts, Watt etc. It is required to have knowledge of what is the input voltage and current that gives full scale ADC input and what are the output registers given by ADE9178 for such input. Signals corresponding to full scale input in physical units are referred as X_{FS} where X_{FS} can be either I_{FS},V_{FS} or AUX_{FS} based on whether channels are current, voltage or auxiliary respectively. These parameters are choices made during system design and is assumed that the application developers are already aware of it. The following table summarizes the ADE9178 register values when full scale inputs are provided at ADC inputs. These are referred as X_{FS_CODES} where X can vary based on type of the register.

Table 12. Terminology and Full Scale Codes

Notation	Description	Value	Applicable Registers
I_{FS}	Current in amperes (A) which gives full scale signal at ADC input. This is the current that gives full scale at the ADC current (IP) inputs of 31.25mV	Depends on system parameters. Refer to example system configuration. Depends on shunt resistor size	
V_{FS}	Voltage in volts (V) which gives full sale input at ADC input. This is the voltage that gives full scale at the ADC voltage (V1P) inputs of 1V	Depends on system parameters. Depends on resistor divider ratio	
AUX_{FS}	Signal value in appropriate units which gives full scale value at ADC input. The units can be either voltage or current. This is the voltage/current that gives full scale at the auxiliary ADC input (V2P) inputs of 1V	Depends on system parameters.	
RMS_{FS_CODES}	RMS output register value when full scale input is applied at the ADC input	107310840	xRMS, xRMSONE, xRMSHALF, xDIP, xSWELL, xPEAK
POW_{FS_CODES}	Power output register value when full scale voltage and current of same phase is applied at the ADC input	85829040	xWATT, xVA
PCF_{FS_CODES}	PCF output for waveform streaming	6706531	
M	Meter constant(impls/kWHr) which defines the frequency of the CF pulse output.	System Configuration. Supported between 100 and 10000	

The format for configuration registers for each feature are given along with description of appropriate features can be found in the following sections. Following equations can be used to convert output registers to physical quantities.

Table 13. Conversion Equations

Purpose	Equation		Unit	Applicable registers
RMS related output calculation	$\left(\frac{X_{FS}}{RMS_{FS\_CODES}}\right) * X$	(1)	Xrms	Where X = xRMS, xRMSONE, xRMSHALF,xDIP, , xSWELL, xPEAK
Power Calculation	$\left(\frac{I_{FS} * V_{FS}}{POW_{FS\_CODES}}\right) * X$	(2)	WATT, VA	Where X = xWATT , xVA
Energy Calculation	$\left[\frac{I_{FS} * V_{FS}}{POW_{FS\_CODES}}\right] * \left[\frac{(X_{HI} \ll 13) + X_{LO}}{4000}\right]$	(3)	WATT*Seconds	Where X_{HI}= xWATTHR_xx_HI or xVAHR_HI X_{LO} = xWATTHR_xx_LO or xVAHR_LO
Power Factor	$xPF * 2^{-27}$			APF,BPF and CPF
Period Calculation	$\frac{xPERIOD + 1}{4000 * 2^{16}}$	(4)	seconds	xPERIOD, PEN_PERIOD
Angle calculation	$2\pi\frac{ANGL\_X\_Y * 256}{xPERIOD + 1}$	(5)	radians	ANGL_X_Y where X and Y are phase voltage or currents. e.g. ANGL_AV_BV or ANGL_BI_CI

WORKED EXAMPLES

This section gives example calculations for the above conversion equations with the following system parameters:

FULL SCALE CODES AND CONVERSION EQUATIONS

System Parameters

- $V_{NOMINAL}$= 220Vrms
- $I_{NOMINAL}$ = 10Arms
- Line Frequency = 50Hz
- Shunt Resistor = 500µΩ
- Voltage Divider
  - R1 = 990kΩ
  - R2 = 1kΩ
  - Divider Ratio = 0.001

Full Scale Voltage =

$$V_{FS} = \left(\frac{V_{ADC\_FS}}{Divider\_Ratio}\right) \div \sqrt{2} \quad = \quad \left(\frac{1}{0.001}\right) \div \sqrt{2} = 707Vrms$$

Full Scale Current =

$$I_{FS} = \left(\frac{I_{ADC\_FS}}{Shunt\_Resistance}\right) \div \sqrt{2} \quad = \quad \left(\frac{0.03125}{500 \times 10^{-6}}\right) \div \sqrt{2} = 44.188Arms$$

Full Scale Auxiliary =

$$AUX_{FS} = \left(\frac{AUX_{ADC\_FS}}{Divider\_Ratio}\right) \div \sqrt{2} \quad = \quad \left(\frac{1}{0.001}\right) \div \sqrt{2} = 707Vrms$$

RMS Output Calculation

if AIRMS = 24285092 decimal then,

$$AIRMS_{CONVERTED} = \frac{I_{FS}}{RMS_{FS\_CODES}} * AIRMS \quad = \quad \frac{44.188}{107310840} * 24285092 = 10.00Arms$$

if AVRMS = 33394314 decimal then,

$$AVRMS_{CONVERTED} = \frac{V_{FS}}{RMS_{FS\_CODES}} * AVRMS \quad = \quad \frac{707}{107310840} * 33394314 = 220.013Vrms$$

Power Calculation

If AWATT = 6044931 decimal then

$$AWATT_{CONVERTED} = \frac{I_{FS} * V_{FS}}{POW_{FS\_CODES}} * AWATT \quad = \quad \frac{44.188 * 707}{85829040} * 6044931 = 2200.295 \quad Watts$$

If AVA = 6038115 decimal then

$$AVA_{CONVERTED} = \frac{I_{FS} * V_{FS}}{POW_{FS\_CODES}} * AVA \quad = \quad \frac{44.188 * 707}{85829040} * 6038115 = 2197.814 \quad VA$$

Energy Calculation

If AWATTHR_POS_HI = 2950618 decimal and AWATTHR_POS_LO = 7367 decimal then

$$Energy = \frac{I_{FS} * V_{FS}}{POW_{FS\_CODES}} * \frac{(X_{HI} \ll 13) + X_{LO}}{4000} \quad = \quad \frac{44.188 * 707}{85829040} * \frac{(2950618 \ll 13) + 7367}{4000} = 2199.54 \quad Watt \quad Seconds$$

If AVAHR_HI = 2950549 decimal and AVAHR_LO = 7354 decimal then

$$Energy = \frac{I_{FS} * V_{FS}}{POW_{FS\_CODES}} * \frac{(X_{HI} \ll 13) + X_{LO}}{4000} \quad = \quad \frac{44.188 * 707}{85829040} * \frac{(2950549 \ll 13) + 7354}{4000} = 2199.49 \quad Watt \quad Seconds$$

Power Factor Calculation

If APF = 67114928 decimal then,

$$APF_{CONVERTED} = APF * 2^{-27} = 67114928 * 2^{-27} = 0.50005$$

FULL SCALE CODES AND CONVERSION EQUATIONS

Period Calculation

If APERIOD = 5242710 decimal then,

$$APERIOD_{CONVERTED} = \frac{APERIOD + 1}{4000 * 2^{16}} = \frac{5242710 + 1}{4000 * 2^{16}} = 19.9994ms = 50.0015Hz$$

Angle Calculation

If ANGL_AV_BV = 6826 decimal then and APERIOD = 5242738 decimal then,

$$Angle = 2\pi\frac{\mathrm{ANGL_{XY}} * 256}{\mathrm{xPERIOD} + 1} = 2\pi\frac{6826 * 256}{5242738 + 1} = 2.094 \text{ radians} = 119.992 \text{ degrees}$$

See Conversion equation tab in the Calibration & Conversion excel for calculators. Can be found on the product web page.

ADE9178 DATA PROCESSING FLOW

This section explains the processing done on the ADC data received before calculating various parameters

CURRENT CHANNEL DATA PROCESSING PATH

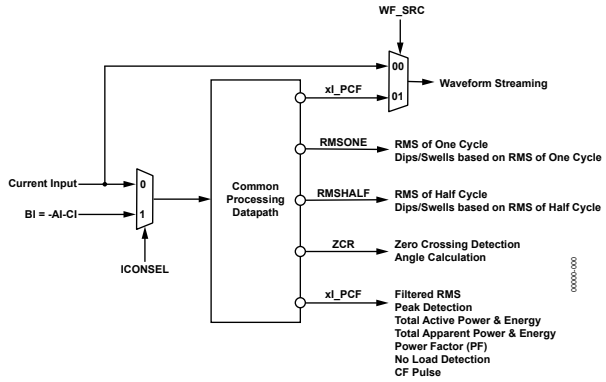


Figure 19. Current Channel Data Path

ADE9178 has three current channels. The data paths for the AI, BI, and CI Current channels is shown in Figure 19 . Write to the ICONSEL bit in the CONFIG0 register to calculate BI = −AI − CI. This setting can help save the cost of a current sensor in some 3-wire delta configurations. Waveform data can be streamed to the Host MCU directly from the ADC samples or from after the PCF (Phase Compensation Filter). WF_SRC[6:5] bits in the WFS_CONFIG register configures which data is streamed.

VOLTAGE CHANNEL DATA PROCESSING PATH

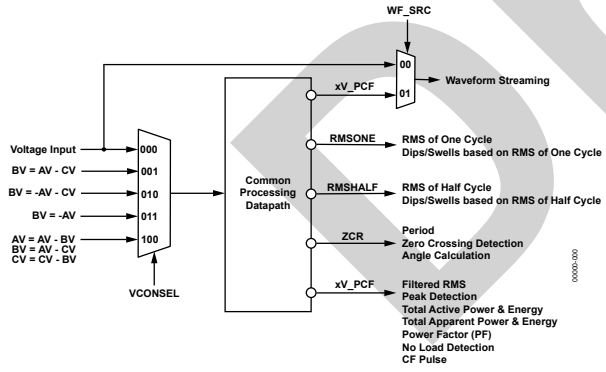


Figure 20. Voltage Channel Data Path

ADE9178 has three voltage channels. The data paths for the AV, BV, and CV voltage channels is shown in Figure 20 . VCONSEL [2:0] field of CONFIG0 register can be used to configure the channels for different meter configurations such as Wye and Delta. Same as the current channel, WF_SRC[6:5] bits in the WFS_CONFIG register can be used to configure which data is streamed to the Host MCU.

AUXILIARY CHANNEL DATA PROCESSING PATH

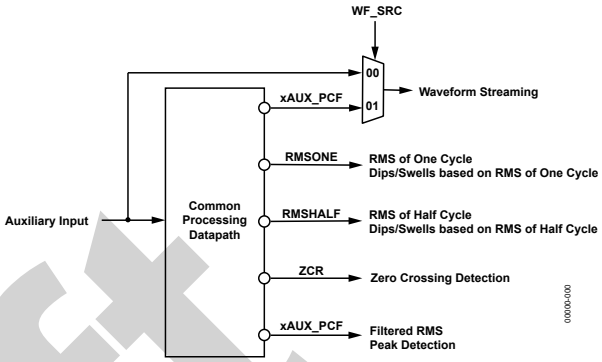


Figure 21. Auxiliary Channel Data Path

ADE9178 supports 6 auxiliary channels. This can be used for various other measurements including neutral current measurements or additional voltages. The datapath for auxiliary channels are shown in Figure 21. Same as the current and voltage channel, WF_SRC[6:5] bits in the WFS_CONFIG register can be used to configure which data is streamed to the Host MCU.

ADE9178 DATA PROCESSING FLOW

COMMON DATA PROCESSING PATH

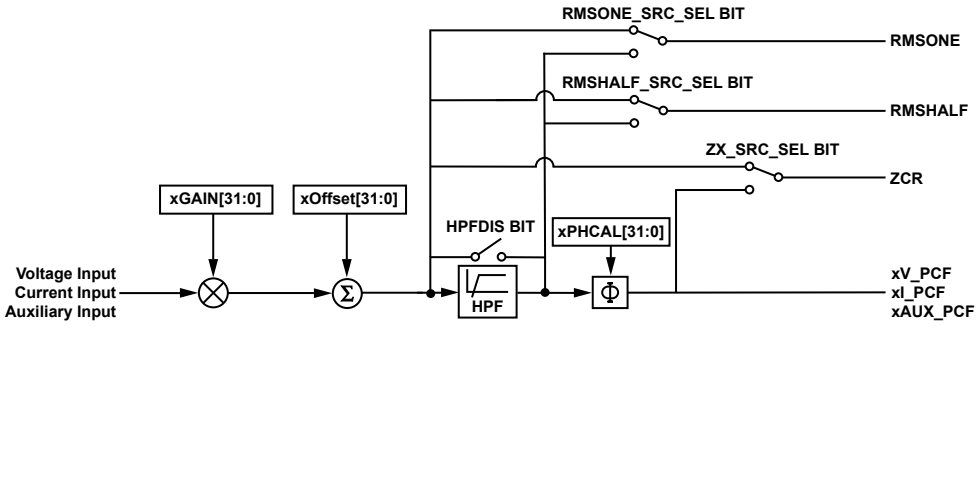


Figure 22. Common Data Path

Gain, and Offset Corrections

All channels support gain and offset compensation. Separate registers are provided for each channel

$$xINP = \left(1 + \frac{xGAIN}{2^{27}}\right) * xINP_0 + xOS$$

where, $xINP_0$ is the initial input value before applying gain and offset calibration.

Note, xOS is only used for DC metering applications.

See Calibration Method for worked examples

High Pass Filter (HPF)

A high-pass filter is provided on all the channels to remove dc offsets for accurate RMS and energy measurements. It is enabled by default with a corner frequency is 0.625 Hz. To disable the high-pass filter set the HPFDIS bit in the CONFIG0 register. The corner frequency is configured with the HPF_CRN bits in the CONFIG0 register.

Table 14. HPF Corner Gain with 50Hz Input Signal

HPF_CRN	$f_{-3\ dB}$ Hz	HPF_GAIN	Settling Time to 1% for DC Step (sec)	Settling Time to 0.1% for DC Step (Sec)
0	38.7	0.80	0.0178	0.0268
1	19.6	0.94	0.0363	0.0544
2	9.90	0.99	0.0731	0.1097
3	4.97	1.00	0.1468	0.2202
4	2.49	1.00	0.2942	0.4412
5	1.25	1.00	0.5889	0.8833
6 (default)	0.625	1.00	1.1784	1.7675
7	0.313	1.00	2.3573	3.5359

ADE9178 DATA PROCESSING FLOW

Phase Compensation

xPHCAL register is provided to compensate phase errors. By default, all channels are delayed by one sample (4.5°). It is recommended to keep the voltage channel xVPHCAL as default value (0) to keep angle between voltages of different phases same. Use the following equation to calculate the xPHCAL value for a given phase correction (ϕ)° angle for current with respect to it's voltage.

$$xPHCAL = \frac{\sin(\phi - \omega) + \sin(\omega)}{\sin(2\omega - \phi)} * 2^{27} \quad where \quad \omega \quad is \quad equal \quad to: \quad 2\pi f_{LINE} * \frac{1}{4000} \tag{6}$$

Zero Crossing and RMS Source Selection

The output of common processing block goes to feature calculations. As shown in Figure 22 , additional bits are provided to choose the sources to following inputs:

- One Cycle RMS Input – RMSONE_SRC_SEL bit of CONFIG0 register can be used to configure whether this should be before or after high pass filter.
- Half cycle RMS Input - RMSHALF_SRC_SEL bit of CONFIG0 register can be used to configure whether this should be before or after high pass filter.
- Zero crossing Input – ZX_SRC_SEL bit of CONFIG0 register selects whether data used in the zero-crossing detection comes before or after the high-pass filter and phase compensation.
- Phase Compensation Output = This goes to power and energy calculations

Note the bits RMS_ONE_SRC_SEL, RMS_HALF_SRC_SEL, ZX_SRC_SEL and HPFDIS are common for all channels.

POWER AND ENERGY MEASUREMENTS

POWER CALCULATION

Total Active Power

The ADE9178 computes total active power on up to three phases. The measurement is equal to the sum of active power of all fundamental and harmonic components of the voltages and currents.

The total active power on each phase is calculated by first multiplying the xI_PCF and xV_PCF waveforms. Then the result is low-pass filtered, unless the DISAPLPF bit in the CONFIG0 register is equal to 1. Finally, the xPGAIN is applied to perform a gain correction and the xWATTOS value is applied to correct the watt offset. The active power calculations, one for each channel (AWATT, BWATT, and CWATT), are updated every 1kHz. The complete datapath is shown in Figure 23.

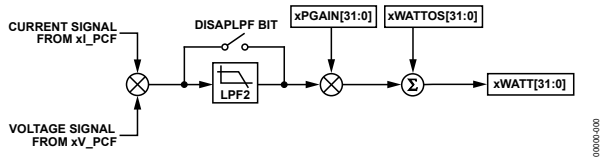


Figure 23. Total Active Power Datapath

The low-pass filter, LPF2, extracts the total active power, attenuating harmonics of a 50 Hz or 60 Hz fundamental by 64 dB so that, at full scale, the variation in the low-pass filtered active power is very small, ±0.062%.. Enable the LPF2 (DISAPLPF = 0) for normal operation. Disable LPF2 (by setting DISAPLPF to 1) in the CONFIG0 register to obtain instantaneous total active power. DISAPLPF is 0 at reset.

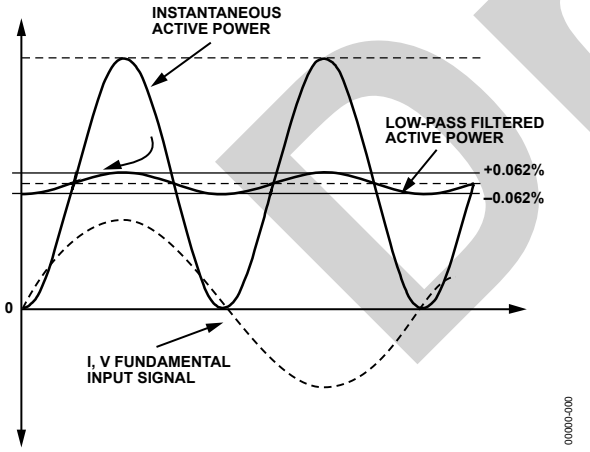


Figure 24. LPF Diagram

The total active power measurements can be calibrated by gain and offset. The following equations indicate how the gain and offset calibration registers modify the results in the corresponding power registers:

$$xWATT = \left(1 + \frac{xPGAIN}{2^{27}}\right) * xWATT_0 + xWATTOS$$

where, $xWATT_0$is thei initial xWATT register value (decimal) before gain and offset calibration. See Power Gain Calibration for worked example.

The xWSIGN bits in the PHSIGN register indicate the sign of the active power value. Bits [3:1] (REVAPC, REVAPB, and REVAPA) in the STATUS0 register are set when a sign change occurs in the active power measurement.

Total Apparent Power

The ADE9178 computes total apparent power on up to three phases. Apparent power is calculated by multiplying the current RMS measurement (xIRMS), by the corresponding voltage RMS (xVRMS), and then applying a gain correction, xPGAIN. The result is stored in the xVA register which is updated at 1kHz. Note that the offset of the total apparent power calculation is performed by calibrating the xIRMS and xVRMS measurements (using the xIRMSOS and xVRMSOS registers), and there is no specific offset compensation register for the apparent power signal processing.

ADE9178 offers a register (VNOM) that contains a desired RMS value. If the VNOMx_EN bits in the CONFIG0 register are set, VNOM RMS is multiplied with xIRMS to calculate xVA. The complete apparent power signal processing datapath is shown in Figure 25.

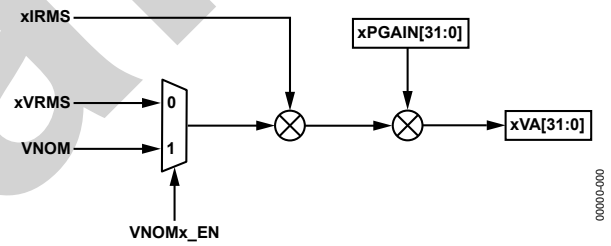


Figure 25. Total Apparent Power Path

ENERGY CALCULATION

The energy path consists of an internal accumulator to perform summation of power outputs generated at 1kHz. The accumulation is carried out for either a user defined time duration or number of half-line cycles based upon the EGY_TMR_MODE bit configured in the EP_CFG register. The time/half line cycles is set in the EGY_TIME register. Set the EGY_PWR_EN bit in EP_CFG register to enable energy accumulation.

After EGY_TIME + 1 milliseconds or EGY_TIME + 1 half line cycle (depending on EGY_TMR_MODE), the EGYRDY bit is set in the STATUS0 register, and the energy output registers are updated. The data from the internal energy accumulator is either added or latched to the output register depending on the EGY_LD_ACCUM bit setting in the EP_CFG register. The user can configure automatic resetting the energy output register after reading them using the RD_RST_EN bit in the EP_CFG register. The figure shows an overview of energy accumulation. Three separate accumulators

POWER AND ENERGY MEASUREMENTS

are provided for positive, negative, and signed accumulation. Even though the diagram shows only accumulation of AWATT, there are similar separate accumulators for other active energy channels (BWATT and CWATT) .Apparent energy channels (AVA, BVA & CVA) only have positive accumulators. Energy is not accumulated if a no load is detected.

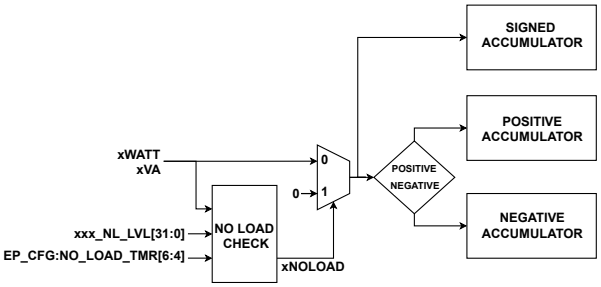


Figure 26. No Load and Sign Check

where x is the phase (A, B, or C) and xxx is either "ACT" or "APP" depending on if the energy being calculated is active or apparent.

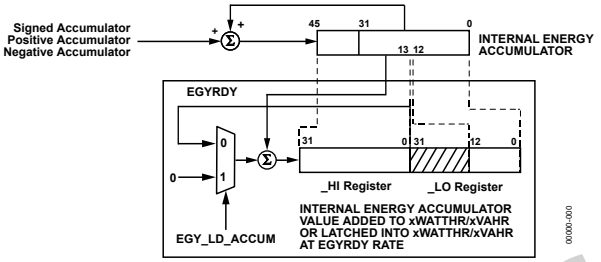


Figure 27. Energy Accumulation Flow

In half line cycle accumulation mode, the energy is accumulated over an integer number of half-line cycles and is synchronized to one of the voltage channels zero crossings decided by the ZX_SEL bits in the ZX_LP_SEL register. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation and allows the energy to be accumulated accurately over a shorter time. This mode greatly simplifies the energy calibration and significantly reduces the time required to calibrate the meter.

Note that with full-scale inputs, the internal and output energy registers overflows in 51.242 sec of samples. Hence, EGY_TIME register value must be set to value lower than 5124d for half line cycle accumulation and lower than 51241d in time accumulation mode to prevent overflowing of the output registers.

Each energy output register is 45 bits wide, split between two registers: a register containing the 32 most significant bits, xHR_xx_HI or xHR_HI , and a register containing the 13 least significant bits, xHR_xx_LO or xHR_LO (where x = xWATT or xVA and xx = SIGNED, POS or NEG, for example AWATTHR_POS_HI or AVAHR_HI). The lower 13 bits of energy output are stored in the xHR_LO register.

See Worked Examples section for how to calculate the energy register value.

In some installations, it is not required to accumulate energy at very high precision. In such cases only the xHR_xx_HI or xHR_HI register can be read and can ignore the value in xHR_xx_LO or XHR_LO register.

For example, if the accumulated energy value is 0x0456789ABCDE, then xHR_xx_HI or xHR_HI will store 0x22B3C4D5 and xHR_xx_LO or xHR_LO will contain 0x1CDE.

Total Active Energy

For each phase, there are three types of active energy outputs available: positive energy, negative energy and signed energy. The registers available for active energy are xWATTHR_SIGNED_HI and xWATTHR_SIGNED_LO, xWATTHR_POS_HI and xWATTHR_POS_LO, and xWATTHR_NEG_HI and xWATTHR_NEG_LO to store signed, positive and negative energy outputs respectively.

Total Apparent Energy

For each phase, there exists one positively accumulated apparent energy output (xVAHR_HI and xVAHR_LO).

No Load Detection

No-load detection prevents energy accumulation due to noise when the input currents are below a given meter start current. To determine if a no-load condition is present, the ADE9178 evaluates if the accumulated energy is below a user defined threshold over a user defined time period, which is done on a per phase and per energy channel basis. The NOLOAD_TMR[2:0] bits in the EP_CFG register determine whether to evaluate the no-load condition over 64 samples to 4096 samples, 64/4 ksps = 16 ms to 1024 ms, , as described in Table 15 . No-load detection is enabled by default, over the minimum time of 64/4 ksps = 16 ms. No-load detection is disabled when the NOLOAD_TMR[2:0] bits in the EP_CFG are equal to 111 (binary). No load accumulation is always done in absolute accumulation mode. See Figure 26.

Table 15. No Load Detection Table

NOLOAD_TMR	Samples to Evaluate in No Load Condition	Time That No Load Detection is Evaluated(ms)
0	64	16
1	128	32
2	256	64
3	512	128
4	1024	256
5	2048	512
6	4096	1024
7	No Load Disabled	No Load Disabled

POWER AND ENERGY MEASUREMENTS

The user defined no load thresholds can be written into the ACT_NL_LVL, and APP_NL_LVL registers to sets the no load threshold for the total active energy and total apparent energy respectively. The configured threshold is directly compared against the accumulated power to decide no load detection. For example to configure a no load threshold of 0.1% of full scale active power accumulated for 64 samples, ACT_NL_LVL should be configured to (POW_{FS_CODES}* 0.001 * 64).

No load status of active energy and apparent energy are indicated using the bits WATTNLOAD and VANLOAD of STATUS0/STATUS1 register respectively. The user can enable an interrupt to occur when the no load status changes, either going into or out of no load. The PHNOLOAD register indicates whether each phase of energy is in no load.

Figure 28 shows what happens when the xWATT, low-pass filtered active power value goes above the user configured no load threshold and then back down below it again. The same concept applies to apparent energy values as well.

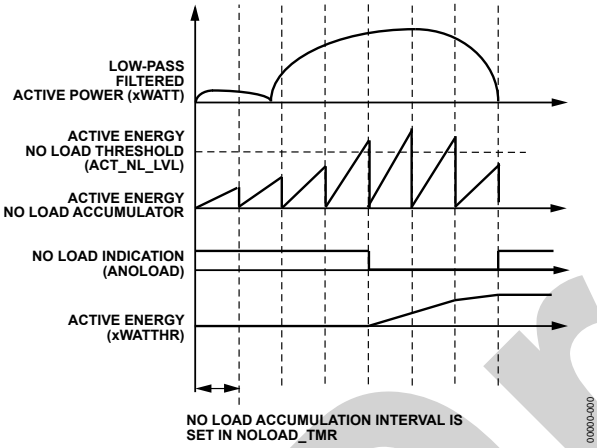


Figure 28. No Load Behavior

Power Factor Calculation

The total active power and total apparent power are accumulated over 1 sec. Then, the power factor is calculated on each phase according to this equation:

$$xPF = \frac{xWATT\ \ accumulated\ \ over\ \ 1sec}{xVA\ \ accumulated\ \ over\ \ 1sec} \quad (7)$$

The accumulation is a signed accumulation. The sign of the xPF calculation follows the sign of xWATT. The power factor results is stored in 5.27 fixed point format. The highest power factor value is 0x07FF_FFFF, which corresponds to a power factor of 1. A power factor of −1 is stored as 0xF800_0000. To determine the power factor from the xPF register value, use this equation:

$$Power\ \ Factor\ \ (PF) = xPF * 2^{-27} \quad (8)$$

CF PULSE GENERATION

Many electricity meters are required to provide a pulse output that is proportional to the energy being accumulated, with a given pulse per kWh meter constant. The ADE9178 includes two pulse outputs that are proportional to the energy accumulation.

A block diagram of the CFx pulse generation is shown below. The ACCMODE[8:7] bits in the CFx_CONFIG register decides the CF accumulation mode (Signed, Positive or Negative accumulation for active power and Positive accumulation only for apparent power). The PHASESEL[6:4] bits in the CFx_CONFIG register determines which phases to include for CF accumulation. The PWRSEL[3:1] bits in the CFx_CONFIG register decides whether active power or apparent power is used for CF accumulation. If the application wants to clear CF accumulator, it can be done using the ACC_CLEAR[10] bit in the CFx_CONFIG register. The CF pulses are generated when accumulated value from previous CF pulse exceeds CFx_THR * 2^8.

POWER AND ENERGY MEASUREMENTS

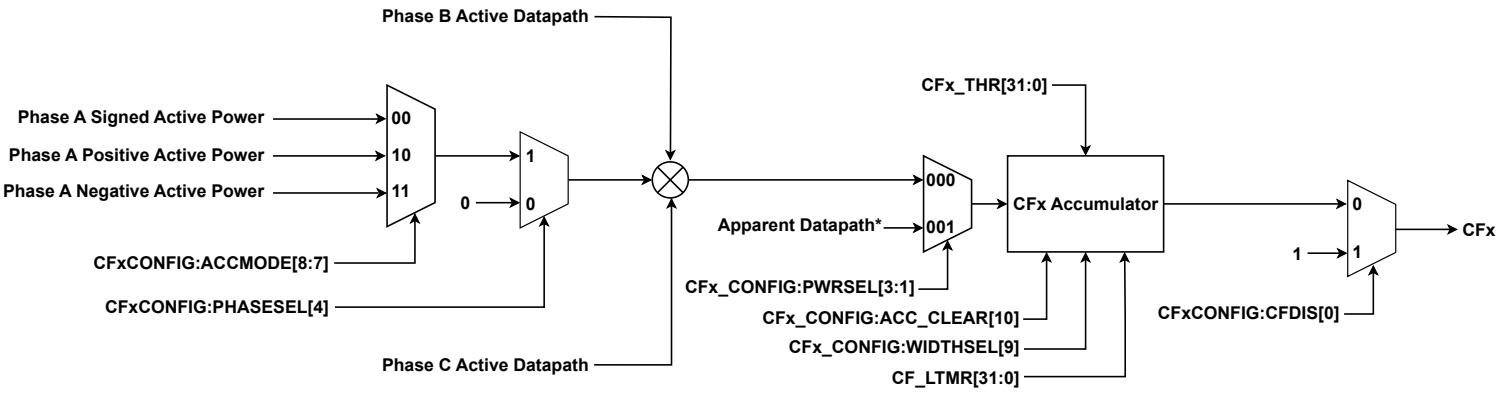


Figure 29. CF Pulse Active Data Path

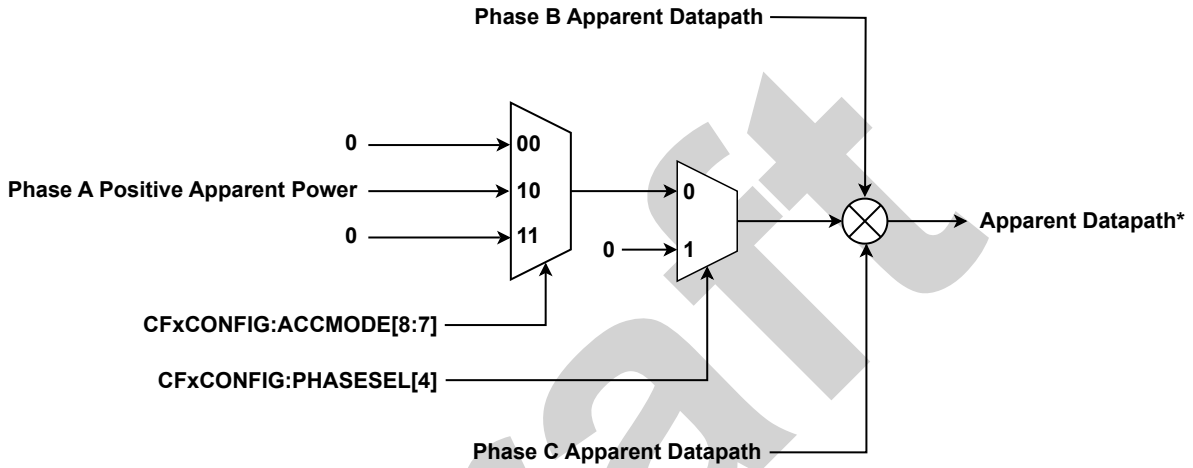


Figure 30. Apparent Data Path

The low pulse width of CF pulse can be controlled by CF_LTMR(in µs, e.g. CF_LTMR = 50000 decimal would set the low pusle width to 50ms) register as per following table. However, if the CF pulse period is less than 50% of CF_LTMR, low pulse width is set as 50% of the CF pulse period.

Note, for best CF performance, CF frequency should be read from the falling edge of the signal.

Table 16. WIDTHSEL Configuration

WIDTHSEL	Active Low Pulse Width for Low Frequencies (< 6.25Hz)	Active Low Pulse Width for High Frequencies (> 6.25Hz)	Behavior when Entering No Load
0	80 ms	50% of period	if CFx is low, finish current pulse,return high
1	CF_LTMR (in us)	50% of period	

CFx_THR register can be used to control the frequency of the pulses. ADE9178 issues a pulse whenever accumulated energy from previous CF pulse crosses (CFx_THR * 256) . To generate M impulses per kWHr , use following formula for setting the threshold.

$$CFx\_THR = \frac{1000 * 60 * 60 * POW_{FS\_CODES} * 4000}{M * I_{FS} * V_{FS} * 256} \quad (9)$$

where M is the desired impulses per kWHr at full scale inputs, I_{FS} is full scale current in amperes and V_{FS} is full scale voltage in volts. POW_{FS_CODES} is the full-scale power code and can be obtained from full scale code documentation.

The expected frequency of CF pulse at full scale input can be calculated as,

$$CF(Hz) = \frac{POW_{FS\_CODES} * 4000}{CFx\_THR * 256} \quad (10)$$

POWER AND ENERGY MEASUREMENTS

Note that the maximum CF frequency supported by ADE9178 is 1KHz. So minimum value of CF_X_THR should be more than,

$$CFx\_THR = \frac{POW_{FS\_CODES} * 4000}{1000 * 256} = \frac{85829040 * 4000}{1000 * 256} = 1341079 \quad decimal \tag{11}$$

for single phase accumulation and more than,

$$CFx\_THR = \frac{POW_{FS\_CODES} * 4000}{1000 * 256} \times 3 = \frac{85829040 * 4000}{1000 * 256} \times 3 = 4023236 \quad decimal$$

for three phase accumulation.

Example

System Parameters

- V_{FS}= 707Vrms
- I_{FS} = 44.188Arms
- M = 10000 impls/kWHr

$$CFx\_THR = \frac{1000 * 60 * 60 * 85829040 * 4000}{10000 * 44.188 * 707 * 256} = 15453719 \quad decimal$$

Therefore if $V_{NOMINAL}$ = 220Vrms and $I_{NOMINAL}$= 32Arms expected CF pulse output will be 19.5556Hz

Please refer to the CF Pulse Setup Tab in the calibration & conversion excel for a CFx_THR calculator. Can be found on the product web page.

ALL CHANNEL MEASUREMENTS

This section explains the measurements that are done for all 12 channels.

ROOT MEAN SQUARE MEASUREMENT (RMS)

ADE9178 supports three types of RMS measurements.

1. Filtered RMS
2. One cycle RMS
3. Half Cycle RMS

Each type of RMS is calculated for all the input channels and separate offset registers are provided for each of these for calibration purpose. Offsets for Filtered RMS, RMS of one cycle and RMS of half cycle can be specified in xRMSOS, xRMSONEOS and xRMSHALFOS registers respectively. Note that the offset is applied in the squared domain as shown in the figure.

$$xRMS = \sqrt{xRMS_0^2 + \left(2^{15} * xRMSOS\right)} \quad (12)$$

where $xRMS_0$is the initial xRMS value before offset calibration

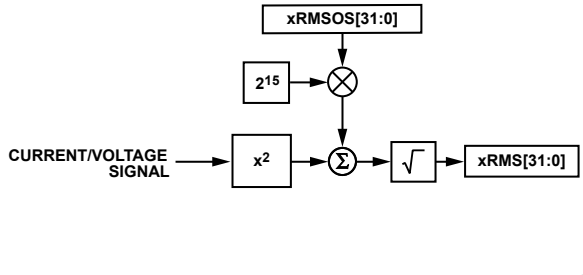


Figure 31. Common RMS Data Path

The number of samples accumulated and averaged varies with the RMS type and is explained in subsequent sections. There is no gain registers separately for RMS calibrations and the application is expected to use signal gain xxGAIN for gain adjustments.

RMS of ONE Cycle

This feature calculates RMS over every period of input signal. One-cycle RMS measurements of all channels are done over the same time interval and update at the same time as indicated by the RMSONERDY bit in the STATUS0 register. The output is stored in xRMSONE register and is updated every cycle. The LP_SEL bits in the ZX_LP_SEL register select which voltage channel line period value to be used in the one-cycle RMS measurement. Alternatively, the user can set the number of samples used in the calculation by setting the UPERIOD_SEL bit in CONFIG0, where the user configured USER_PERIOD register is used instead of the selected line period value. USER_PERIOD is specified in Q16 fixed point format as period in number of samples. For example if the application wants to set 0.21ms , USER_PERIOD shall be configured as 0.21 * 4000 * 2^{16} = 0x 348000 . The RMSONE_SRC_SEL bit in CONFIG0 register decides which waveform input samples should be used for one-cycle RMS measurement. If the bit is set to 1, it indicates the ADC samples before the high pass filter to be used. If the bit is set to 0 then samples obtained after the HPF are used for calculation. See Figure 22. Since the high pass filter has a significant settling time associated with it, it is recommended to use the data from before the high-pass filter for the fastest response time.

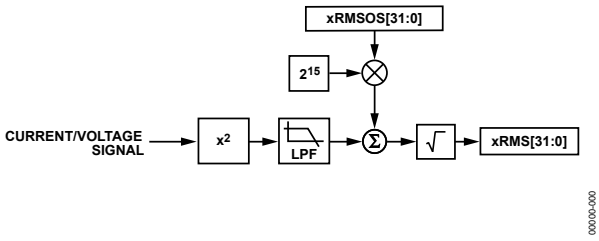
RMS of ½ Cycle

This feature calculates RMS and updates xRMSHALF registers over every half period of signal. Note that this behavior is different from ADE9000 where RMS was calculated over one cycle but updated every ½ cycle. The RMSHALF_SRC_SEL bit in CONFIG0 (See Figure 22) register decides which waveform input samples used for half-cycle RMS measurement are to be taken before or after the HPF filter. There are two modes of operation. Each channel has a separate configuration bit in RMSHALF_CONFIG register to choose between the two modes. If the bit is set to 0, then the RMS of half cycle measurement is synchronized to the zero crossing of corresponding channel. This means that the ZX bit for a particular channel in STATUS0 gets set after the xRMSHALF registers are updated. If the bit is set to 1, then the user can specify half period in USER_PERIOD_HALF register which will be used for measurement. In this case the output will not be synchronized with zero crossings. This mode can be used when measuring non-periodic signals.USER_PERIOD_HALF is specified in Q16 fixed point format as period in number of samples same as USER_PERIOD for One Cycle RMS. For example if the application wants to set 0.21ms , USER_PERIOD_HALF shall be configured as 0.21 * 4000 * 2^{16} = 0x 348000.

Filtered RMS

The ADE9178 offers filter-based RMS updated every 1KSPS. The output of filtered RMS is available in xRMS registers. The settling time for this RMS measurement is approximately 580 ms for both 50 Hz and 60 Hz input signals. Filtered RMS has a bandwidth of 1.61kHz.

Figure 32. Filtered RMS Data Path



ZERO CROSSING DETECTION

The ADE9178 offers zero-crossing detection on all ADC input signals. Each channel is associated with a ZX bit in STATUS0 and STATUS1 registers which are set when zero crossing is detected on that channel. However, ZX output from ADE9178 has very high jitter and hence is not intended for external use. User are expected to use zero crossing detection output from the ADC if high accuracy is required.

ALL CHANNEL MEASUREMENTS

The ZX_SRC_SEL in the CONFIG0 register select whether data going into the zero-crossing detection circuit comes before or after the high-pass filter and phase compensation(See Figure 22) . By default, the xPCF waveforms after the high-pass filter (HPF) are used for zero crossing detection . The zero-crossing circuit is the time base for line period, angle, RMS HALF measurements, and energy accumulation using line cycle accumulation mode.

Note that the high-pass filter has settling times given in Table 14 . Thus, for a fast response, it is recommended to set ZX_SRC_SEL to look for a zero crossing before the high-pass filter. However, if the high-pass filter is disabled with HPFDIS = 1 or if ZX_SRC_SEL = 1, note that a dc offset on the input may cause the time between negative to positive and positive to negative zero crossings and positive to negative to negative to positive zero crossings to change, indicating that the ZX detection does not have a 50% duty cycle.

The input signals are passed through a first order low pass with corner frequency of 85Hz to remove harmonics.

The low-pass filter settling time is 51 samples, 51/4 kSPS, which results in 12.75 ms. Figure 33 shows the delay between the detected zero-crossing signal and the input. Note that there is a 3.5 to 4.3 ms delay between the input signal zero crossing and the ZX zero crossing indication, with a 50 Hz input signal. Zero crossings are generated on both negative to positive and positive to negative transitions.

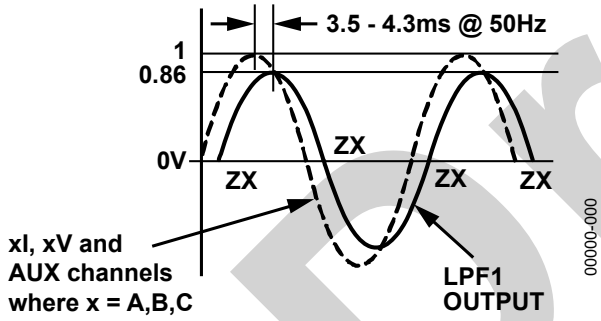


Figure 33. Zero Crossing Timing

To provide protection from noise for zero-crossing events used for period calculation, zero crossing events are not generated for voltage channels if the absolute value of the ZX LPF filter output signal is smaller than the threshold ZXTHRSH. Additionally, on all ADC channels, to prevent false zero crossings after a zero crossing is generated, 1 ms must elapse before the next zero crossing can be output. Calculate the zero-crossing threshold, ZXTHRSH, from the following equation:

$$ZXTHRSH = \frac{PCF_{FS\_CODES} * LPF_{ATTENUATION}}{x}$$

where $LPF_{ATTENUATION}$=0.86 at 50Hz and 0.81 at 60Hz. x is the fraction of full scale for which the zero crossing will be blocked.

For example, for a 50Hz input, it is required to block zero crossing detection for samples 100× lower than full scale PCF output. Then:

$$ZXTHRSH = \frac{6706531 * 0.86}{100} = 57676d$$

Zero-Crossing Timeout

The zero-crossing timeout feature alerts the user if a zero-crossing event is not generated after a user configured amount of time. This feature is available only on the voltage channels. If a zero-crossing is not detected after (ZXTOUT+1) milliseconds, the corresponding ZXTOx bit in the STATUS1 register is set. For example, if ZXTOUT is equal to 1000, and if a zero-crossing is not detected on Phase A for 1001 ms, then ZXTOAV bit is set in the STATUS1 register.

Combined Voltage Zero Crossing

Apart from zero crossing input signal, ADE9178 provides zero crossing of a combined signal from AV. BV and CV. The combined signal is formed as s (AV + BV − CV)/2 . This zero crossing, ZX_COMB, is stable even if one or more phases drops out.

Zero Crossing Use in Other Functions

The following features are dependent on zero crossing detection. The behavior of each feature when zero crossing is absent is given in the table.

Table 17. Zero Crossing Use in Other Functions

Function Using Zero Crossing	ZX Transition Used	Corresponding STATUSx register bits	Selecting Which Phase to use for Measurement	Effect if ZX Does Not Occur
ZX Indication in STATUS0 Register[1]	Negative to positive, and positive to negative	ZXAI, ZXBI, ZXCI, ZXAV, ZXBV, ZXCV, ZXAUX0, ZXAUX1, ZXAUX2, ZXAUX3, ZXAUX4, ZXAUX5 and ZXCOMB of STATUS0 and STATUS1 registers	Not applicable	ZXx bit is latched in STATUS1. If cleared, it is not set again. ZXx interrupt does not occur.

ALL CHANNEL MEASUREMENTS

Table 17. Zero Crossing Use in Other Functions (Continued)

Function Using Zero Crossing	ZX Transition Used	Corresponding STATUSx register bits	Selecting Which Phase to use for Measurement	Effect if ZX Does Not Occur
Zero Crossing Timeout	Negative to positive, and positive to negative	ZXTOAV, ZXTOBV, ZXTOCV of STATUS0 and STATUS1 registers	Not applicable	Zero-crossing timeout is indicated by the ZXTOAV, ZXTOBV or ZXTOCV bit in the STATUS0 register and an interrupt can be enabled to occur.
Phase Sequence Error Detection	Negative to positive only	SEQERR of STATUS0 and STATUS1 registers	Not applicable	If one to two ZX events are missing, SEQERR is generated. If all ZX are missing then SEQERR bit is not set
Energy Accumulation	Negative to positive, and positive to negative	Not applicable	ZX_LP_SEL:ZX_SEL[1:0] selects the zero-crossing output used for line cycle energy accumulation and ZX output pin.	Line cycle accumulation does not update.
Line Period Measurement	Negative to positive only	Not applicable	Not applicable	Coerced to default value: 0x00A0_0000 if ACCMODE.SELFREQ = 0, for a 50 Hz network; 0x0085_5554 if ACCMODE.SELFREQ = 1, for a 60 Hz network.
RMSONE, DIPONE, SWELLONE	Negative to positive only	STATUS2 register	ZX_LP_SEL:LP_SEL[3:2] selects the phase voltage line period used as the basis for these calculations.	If the selected line period is invalid because zero-crossings are not detected or the calculation results in something outside a 40 Hz to 70Hz range, the line period used for the calculation is coerced to the default line period: 0x00A0_0000 if ACCMODE:SELFREQ = 0, for a 50 Hz network; 0x0085_5554 if ACCMODE:SELFREQ = 1, for a 60 Hz network. This line period is used to calculate RMSONE and associated events.
RMSHALF, DIPHALF, SWELLHALF	Negative to positive, and positive to negative	STATUS3 register	Not applicable	If bits are set to 1 in the RMSHALF_CONFIG register then the corresponding RMSHALF register value is calculated based on the user configured half line cycle period register (USER_PERIOD_HALF) Otherwise, if zero crossing is not detected, the corresponding RMSHALF register value is not updated. DIPHALF and SWELLHALF is not detected in such cases.
Angle Measurements	Negative to positive only	Not applicable	Not applicable	Does not update; keeps last value.

[1] The ZX output from ADE9178 has very high jitter, hence it is not intended for external use

PEAK DETECTION

The ADE9178 records the peak value measured on the current, voltage and auxiliary channels, from the xPCF waveforms. The VPEAKSEL[2:0], IPEAKSEL[2:0] , AUXPEAKSEL[5:0] bits in the PEAK_CONFIG register allow the user to select which channels to monitor for peak detection.

ALL CHANNEL MEASUREMENTS

The IPEAK register stores the peak current value in IPEAKVAL[23:0] and indicates which phase(s) currents reached the value in the IPPHASE[2:0] bits. Similarly, VPEAKVAL and VPPHASE bits of VPEAK register and AUXPEAKVAL and AUXPHASE bits in AUXPEAK registers provides similar information for voltage and auxiliary channels respectively.

DIP AND SWELLS

Dip indicates if the RMS of input signal went below a specified threshold for a user configured number of cycles. Conversely, swell indicates if the RMS of input signal went above a threshold for a specified number of cycles. ADE9178 supports dip/swell detection on RMSONE and RMSHALF outputs for all ADC channels.

The corresponding xRMSHALF or xRMSONE is compared against the configured xDIPHALF_LVL or xDIPONE_LVL. If the consecutive RMS values are less than the level for configured number of xDIPHALF_CYC (register unit in half line cycles) or xDIPONE_CYC (register value units in one line cycles) , then the corresponding smallest dip RMS value is updated in xDIPONE or xDIPHALF registers (same register format as all RMS output registers). Each channel is associated with separate LVL and CYC registers. For example if the application wants to flag DIP if the AVRMSONE goes below 20% of the full scale for 5 line cycles then , AVDIPONE_LVL register should be configured as RMS_{FS_CODE} * 0.2 = 107310840 * 0.2 = 21462168 decimal and AVDIPONE_CYC should be set to 5 decimal. Note, if 0 or 1 is written to the CYC register, the dip/swell flag will be set after 1 cycle.

Similarly, for swell detection, corresponding xRMSHALF or xRMSONE is compared against the configured xSWELLHALF_LVL or xSWELLONE_LVL If the consecutive RMS values are greater than the level for configured number of xSWELLHALF_CYC or xSWELLONE_CYC , then maximum RMS values is updated in the xSWELLONE or xSWELLHALF registers. Each channel is associated with separate LVL and CYC registers.

Status of RMSONE dips/swells is provided in STATUS2 register and status of RMSHALF dips/swells is provided in STATUS3 register. If DIP_SWELL_x_IRQ_MODE bit in CONFIG0 register is set, then bit in STATUS registers is set only when entering or exiting the dip or swell condition. Otherwise by default, the bit is set continuously after every xDIPx_CYC or xSWELLX_CYC cycles. $\overline{IRQ2}$/$\overline{IRQ3}$ outputs can be enabled by setting the appropriate bit in the MASK2/MASK3 registers to generate interrupts for these flags.

The diagrams below show the expected behavior for both "continuous" and "Enter and Exit" IRQ modes. In both examples the CYC register has been set to 0x2.

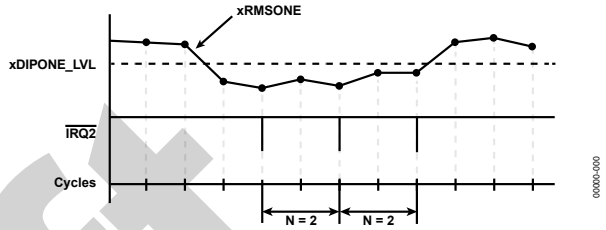


Figure 34. Continuous IRQ mode

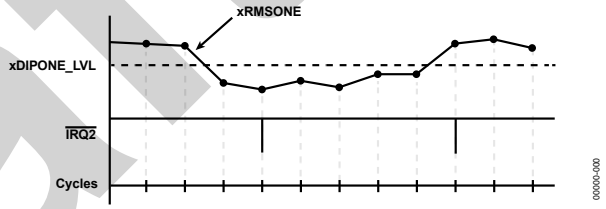


Figure 35. Enter and Exit IRQ mode

ANGLE MEASUREMENT

ADE9178 measures angles between voltage signals, current signals and angle between voltage and current signals. Note that angle measurement is not available for auxiliary channels. It is measured as the time between negative to positive zero crossings of corresponding signals, as shown in figure below

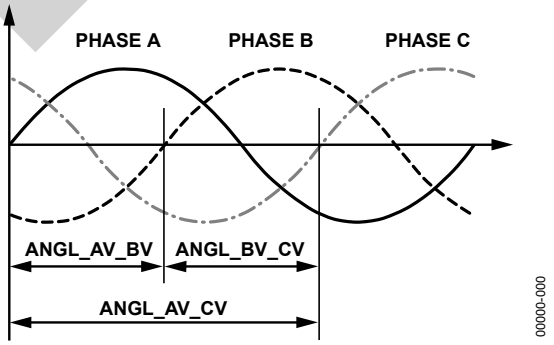


Figure 36. Angle between Voltages

ALL CHANNEL MEASUREMENTS

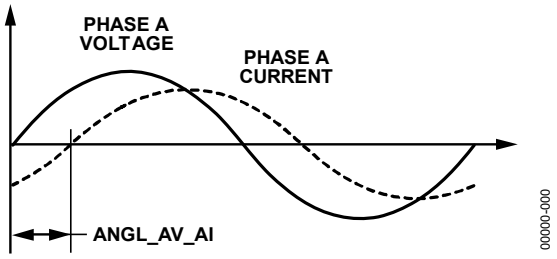


Figure 37. Angle between Voltage and Current

The output is given as 3 registers ANGL_AV_BV , ANGL_AV_CV, ANGL_BV_CV for voltage , 3 registers ANGL_AI_BI , ANGL_AI_CI, ANGL_BI_CI for current and another three registers ANGL_AV_AI , ANGL_BV_BI, ANGL_CV_CI angle between voltage and current of corresponding phases. Use following equation to convert the register to angle in radians

$$Angle\left(rad\right) = 2\pi\frac{\mathrm{ANGL_{XY}} * 256}{\mathrm{xPERIOD} + 1} \quad (13)$$

In above equation xPERIOD corresponds to the PERIOD of selected channels. There is no period register available for current output and corresponding voltage period values can be used for angle calculation. If the frequency of the signal is known, following formula can also be used to convert angle registers to radians.

$$Angle\left(rad\right) = 2\pi\frac{\mathrm{ANGL_{XY}} * f_{LINE}}{4000 * 2^{8}}$$

See Worked Examples section and Calibration & Conversion excel for calculator

MEASUREMENTS ONLY FOR VOLTAGE CHANNELS

LINE PERIOD CALCULATION

ADE9178 calculates period using zero crossings on voltage channels and combined voltage channels described in the Zero Crossing Detection section . The line period, t_L can be calculated from the xPERIOD register according to the following equation:

$$t_L = \frac{xPERIOD + 1}{4000 * 2^{16}} \quad (14)$$

If the calculated period value is outside the range of 40 Hz to 70 Hz, or if the negative to positive zero crossings for that phase are not detected, the xPERIOD register is coerced to correspond to 50 Hz or 60 Hz, according to the setting of the SELFREQ bit in the CONFIG0 register. With SELFREQ = 0 for a 50 Hz network, xPERIOD register is coerced to 0x0050 0000. If SELFREQ = 1, indicating a 60 Hz network, the xPERIOD register is coerced to 0x0042 AAAA.

PHASE SEQUENCE ERROR DETECTION

ADE9178 monitors the zero crossings of the voltage signals and raises sequence error if they are not in expected order. If SEQ_CYC is not set to 1, ADE9178 flags sequence error only after getting SEQ_CYC consecutive zero crossing errors.

After applying VCONSEL, the expected sequence of voltage signals for a 3-phase system is as follows.

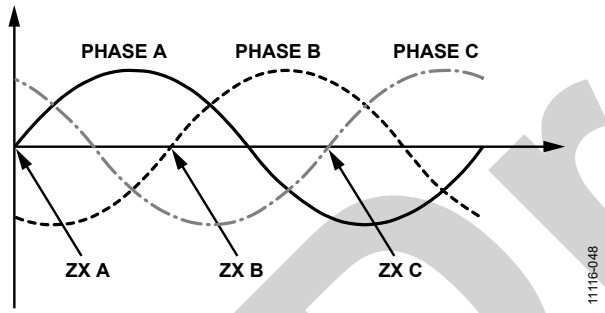


Figure 38. Regular Succession of Zero-Crossing Events: Phase A, Phase B, and Phase C

Following diagram shows a sequence with phase sequence error

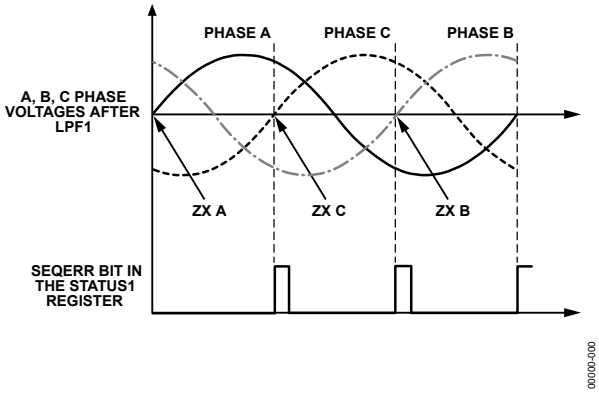


Figure 39. SEQERR Bit Set to 1 When Phase A Voltage is Followed by Phase C Voltage

Note that phase sequence error also happens if one of the voltage channels are missing as shown in below

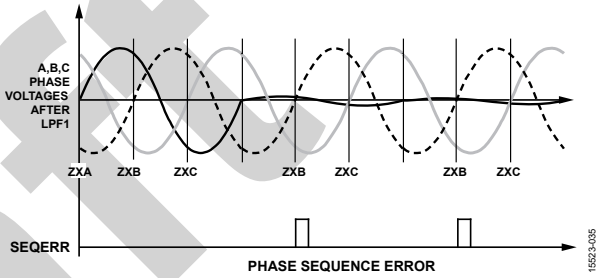


Figure 40. 4-Wire WYE, 4-Wire Delta Phase Sequence Error from a Phase Voltage Dropping below ZXTHRSH with SEQ_CYC = 1

MEASUREMENTS ONLY FOR CURRENT CHANNELS

NEUTRAL CURRENT MISMATCH

The ADE9178 calculates the RMS of the sum of AI + BI + CI and stores the result in the ISUMRMS register. The ISUMRMSOS register allows offset calibration of this measurement. The scaling is the same as for the other xIRMS and xIRMSOS registers. Additionally, any one of the six auxiliary ADC path can be selected by configuring the ISUM_AUXSEL bits in CONFIG0 register to be used for neutral current sensing. This channel can be either added or subtracted from the sum of phase channels by configuring ISUM_CFG bits in CONFIG0 register.

In some cases, the application may want to get an interrupt if the RMS of the sum of current channels exceeds a threshold. This threshold value can be set in the ISUMLVL register. IMISMATCH bit of STATUS0 is set when ISUMRMS exceeds ISUMLVL.

PEN FAULT DETECTION

This feature is designed to detect PEN faults according to the BS7671:2018 Amendment 1:2020 standard.

ADE9178 provides additional RMSONE calculation and dip/swell detection on certain channels to enable easy PEN Fault detection. Three channels are used for PEN Fault Detection, PEN_CHANA, PEN_CHANB and PEN_CHANC. The PEN channels can be configured using the PEN_CHANSELA, PEN_CHANSELB and PEN_CHANSELC bits in the PEN_CONFIG register. The PEN channels can be any of the 12 ADC channels AV, BV, CV, AI, BI, CI, AUX0, AUX1, AUX2, AUX3, AUX4 and AUX5.

RMS OF PEN FAULT CHANNELS

Four additional one cycle RMS values (same as RMS of ONE Cycle section) are calculated on the following signals.

1. VSUMRMSONE = (PEN_CHANA + PEN_CHANB + PEN_CHANC)/3
2. VABRMSONE = PEN_CHANA – PEN_CHANB
3. VACRMSONE = PEN_CHANA - PEN_CHANC
4. VBCRMSONE = PEN_CHANB - PEN_CHANC

RMSONE_SRC_SEL bit in the CONFIG0 register decides whether input is before or after high pass filter (HPF). Period is calculated for any one of the selected PEN channels based on PEN_LP_SEL bits in the PEN_CONFIG and is stored in the PEN_PERIOD register (see Table 13 section for formula to convert to seconds). This period value is used for the PEN channel RMS measurements. Separate RMS offset calibration registers are also provided for each of PEN channel (VSUMRMSONEOS, VABRMSONEOS, VACRMSONEOS, VBCRMSONEOS). The PEN channel RMS offset register format is the same as the other RMS offset registers (xxRMSOS)

Example

If PEN_CONFIG is set up in the following configuration:

PEN_CHANSELA = 0000 = AV Data Processing Path

PEN_CHANSELB = 0010 = BV Data Processing Path

PEN_CHANSELC = 0100 = CV Data Processing Path

PEN_LP_SEL = 11 = Combined PEN Channels (AV + BV - CV)/2

Then the PEN Fault output registers will be calculated as follows:

VSUMRMSONE = (AV + BV + CV)/3

VABRMSONE = AV - BV

VACRMSONE = AV - CV

VBCRMSONE = BV - CV

PEN_PERIOD = Period of combined PEN Channels

DIPS AND SWELLS ON PEN FAULT CHANNELS

Swells can be detected based on VSUMRMSONE value while both dips and swells and can be detected on the three phase to phase voltage RMS values (VABRMSONE, VACRMSONE and VBCRMSONE). Separate dip/swell levels and cycle configuration registers (VxRMSONE_LVL & VxRMSONE_CYC, see section Dip and Swells for more details) are provided for each of the four PEN fault channels. Four status bits (VSUMSWELLONE, VABSWELLONE, VACSWELLONE & VBCSWELLONE) are provided for swells and three status bits (VABDIPONE, VACDIPONE & VBCDIPONE) are provided for dips in the STATUS2 register which if required can be configured to generate interrupts on $\overline{\text{IRQ2}}$ (See Dip and Swells section for more details)

WAVEFORM STREAMING

ADE9178 streams the waveform samples through UART interface. The baud rate can be configured using the BAUD_RATE[4:1] bits in the WFS_CONFIG register. ADE9178 supports waveform streaming of either raw ADC samples or samples after phase compensation filter using the WF_SRC[6:5] bits in the WFS_CONFIG register (setting to 00 will stream raw ADC values and 01 will stream the samples after the phase compensation filter). The sampling rate of the samples streamed is 4kHz.

Samples of different channels are transmitted in interleaved format as follows

Table 18. Transmission Format

AV	AI	BV	BI	CV	CI	AUX0	AUX1	AUX2	AUX3	AUX4	AUX5

The individual channels can be enabled or disabled by setting the corresponding x_WFS_EN bits in the WFS_CONFIG register. For example to stream AV and AI data only, set the AV_WFS_EN[7] and AI_WFS_EN[8] bits to 1 in the WFS_CONFIG register. If a channel is disabled, the samples corresponding to that channel are not transmitted and is occupied by subsequent channel. For example if only AV, BV and CV are enabled , samples would streamed as follows:

Table 19. Transmission Format with only AV,BV and CV are Enabled

AV	BV	CV	AV	BV	CV

The baud rate required for transmission varies with number of channels enabled. It is recommended to use the 3072kbps - the highest baud rate supported for waveform streaming. A baud rate of at least 3072000 is required to stream all channels together. Samples will be dropped if the baud rate is below that. If the baud rate is less than required baud rate when writing WFS_CONFIG register, error pin is asserted.

Each sample is sent as a 32-bit integer with upper 24 bits indicating the sample value and lower 8 bits indicating the corresponding channel. This channel id can be used to synchronize various channels . For example, if the number of enabled channels is 12 , to synchronize the starting of the capture to 0th channel , the following steps should be followed:

1. Skip the bytes from UART till 0x0 is encountered.
2. Once 0x0 is received at the Nth byte, check if N+4th byte is 0x1 , N + 8th byte is 0x2 and N+12th byte is 0x3. If not go back to step 1

The lowest byte of each 32-bit word is sent first through UART.

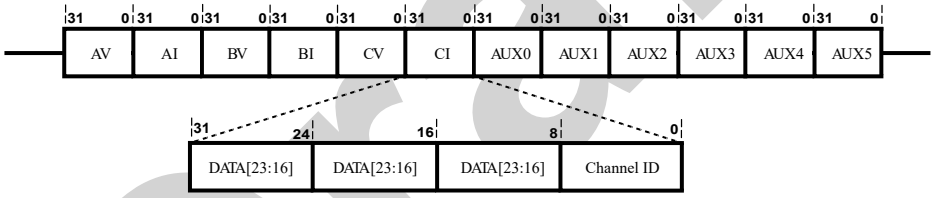


Figure 41. Waveform Streaming UART Transmission Format

The following table summarizes the minimum baud-rate requirement to stream the waveform samples.

Table 20. Minimum Baud-rate Requirements

Channels Enabled	Minimum Baud rate
12	3072000
11	2048000
10	2048000
9	2048000
8	1536000
7	1536000
6	1024000
5	1024000
4	1024000
3	512000
2	512000
1	256000

OUTPUT REGISTER UPDATE RATES

Most of the ADE9178 output registers are updated every 1ms interval (1KHz rate). The following table summarizes the list of registers that are **not** updated at the 1kHz rate.

Table 21. Update Rates

Register Name	Description	Update Rate	Status Bits
xxRMSONE	One cycle RMS registers	Line period	RMSONERDY (STATUS0/1)
xxRMSHALF	Half cycle RMS registers	2 * Line Period	ZXxx(STATUS0/1)
xWATTHR_POS_LO/HI, xWATTHR_NEG_LO/HI, xWATTHR_SIGNED_LO/HI xVAHR_LO/HI	Active /apparent energy registers	Depends on EGY_TMR_MODE bit of EP_CFG	EGYRDY (STATUS0/1)
xPF	Power Factor	1Hz	PF_RDY (STATUS0/1)
xxDIPHALF	Minimum RMSHALF during a half cycle dip event	2 * Line Period but updated only when DIPHALF is detected	xxDIPHALF (STATUS3)
xxDIPONE	Minimum RMSONE during a one cycle dip event	Line Period but updated only when DIPONE is detected	xxDIPONE (STATUS2)
xxSWELLHALF	Maximum RMSHALF during a half cycle swell event	2 * Line Period but updated only when SWELLHALF is detected	xxSWELLHALF (STATUS3)
xxSWELLONE	Maximum RMSONE during a one cycle swell event	Line Period but updated only when SWELLONE is detected	xxSWELLONE (STATUS2)

INTERRUPTS AND STATUS OUTPUTS

ADE9178 provides five 32 bit registers STATUS0, STATUS1, STATUS2 , STATUS3 and ERROR_STATUS to indicate various events/errors in the system. There are corresponding MASK0 , MASK1 , MASK2, MASK3 and ERROR_MASK registers which can be used to map a particular event to one of the interrupt pins IRQ0, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$ or $\overline{\text{IRQ3}}$. These pins go low when an enabled interrupt occurs and stays low until the event is acknowledged by writing '1' to the corresponding bit in the STATUS register.

Note that STATUS0 and STATUS1 contains exactly same events except the 14th bit. STATUS0 14th bit is for RSTDONE (non-maskable) and STATUS1 14th bit is for ERROR(bit enabled by default in the MASK1 register) . Two registers are provided to allow mapping to $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ for these events.

As there is no dedicated IRQ pin associated with the ERROR_STATUS register, bit 14 of the STATUS1 register (ERROR) is used to map any error bits in the ERROR_STATUS register to the $\overline{\text{IRQ1}}$ pin. If an error occurs the STATUS1 ERROR bit is asserted only if the corresponding bit is set in the ERROR_MASK register. STATUS1 bit 14 (ERROR) is masked to $\overline{\text{IRQ1}}$ by default. Read the ERROR_STATUS register to determine the cause of the interrupt.

Example

If user wants to generate an interrupt on $\overline{\text{IRQ1}}$ whenever ADC_RUNTIME_ERROR is detected from ERROR_STATUS, then the user needs to set bit 3 in the ERROR_MASK register. Bit 14 of STATUS1 is logical OR of the ERROR_STATUS bits set in ERROR_MASK.

IRQ Re-occurrence behavior

Most bits of STATUS0 and STATUS1 (like CFx, RMSONERDY, PF_RDY, ZXx) are associated with an event and these bits are set whenever the corresponding events occur. For certain other bits, the rate at which the bits are set are dependent upon a user configurable value as can be seen in the table below:

Table 22. Re-occurrence Behavior

STATUS0 Bits	Re-occurrence Behavior
EGY_RDY	After every EGY_TIME+1 milliseconds or EGY_TIME+1 half line cycles
SEQERR	After every SEQ_CYC number of consecutive phase sequence errors
ZXTOAV, ZXTOBV, ZXTOCV	After every ZXTOUT+1 milliseconds

The IRQ re-occurrence behavior for dips/swells bits in STATUS2/STATUS3 registers depends upon the DIP_SWELL_x_IRQ_MODE configuration bit in CONFIG0 register. When this configuration bit is 0 ,then the STATUS register bit is set only when entering or exiting the dip/swell condition. However, if the configuration bit is set to 1 then the STATUS bits are set periodically after every DIP_CYC/SWELL_CYC cycles for as long as the channel is in dips/swells condition.

POWER MANAGEMENT

INITIALISING THE CHIPSET

ADE9178 checks its integrity during boot time. If the check fails pins $\overline{\text{HOST\_RDY}}$ and $\overline{\text{HOST\_ERR}}$ go low together and ADE9178 enters into a standby mode. A hardware reset is required to take ADE9178 out of this state. Please see Hardware Reset Section on how to perform a hardware reset.

HARDWARE RESET

The ADE9178 has a dedicated reset pin. Hardware reset occurs when the $\overline{\text{RESET}}$ pin is brought low (default state is weak pullup) for at least 1.5us. During a hardware reset, all the registers are set to their default values. ADE9178 reset pin and ADE91xx reset pins should be tied together as shown in theTest Circuit.

APPLICATIONS INFORMATION

CALIBRATION METHOD

The system is calibrated at nominal operating voltage and current using an accurate source. The worked-out example is shown only for phase A. The calculation remains same for other channels also well. All calibration steps involve providing a known signal to the relevant ADC channels and compare one of the output registers to the expected value of the register.

System Parameters

- VNOMINAL = 220 Vrms
- INOMINAL = 10 Arms
- Line frequency = 50 Hz
- Shunt Resistor = 500µΩ
- Voltage Divider
  - R1 = 990kΩ
  - R2 = 1kΩ
  - Divider Ratio = 0.001

Full Scale Voltage:

$$V_{FS} = \left(\frac{V_{ADC\_FS}}{Divider\_Ratio}\right) \div \sqrt{2} = \left(\frac{1}{0.001}\right) \div \sqrt{2} = 707Vrms$$

Full Scale Current:

$$I_{FS} = \left(\frac{I_{ADC\_FS}}{Shunt\_Resistance}\right) \div \sqrt{2} = \left(\frac{0.03125}{500 \times 10^{-6}}\right) \div \sqrt{2} = 44.188Arms$$

Full Scale Auxiliary:

$$AUX_{FS} = \left(\frac{AUX_{ADC\_FS}}{Divider\_Ratio}\right) \div \sqrt{2} = \left(\frac{1}{0.001}\right) \div \sqrt{2} = 707Vrms$$

RMS Gain Calibration

This section explains how to calculate the xxGAIN register which affects all output parameters of ADE9178. RMS values are used to calibrate the gain.

With the nominal voltage and current inputs, read the appropriate RMS register (e.g. AIRMS, AVRMS or AUXRMS). It is recommended to read the RMS values once per zero-crossings for 1 sec and average them for better accuracy.

The expected RMS register value for given voltage and current can be calculated as follows:

$$xRMS_{EXPECTED} = \frac{RMS_{FS\_CODES} * X_{NOMINAL}}{X_{FS}}$$

where $X_{NOMINAL}$ is the nominal signal applied at the ADC input and $X_{FS}$is either V_{FS},I_{FS}or AUX_{FS}.

The xxGAIN register can be calculated from expected and observed RMS register as follows:

$$xxGAIN = \left(\frac{xRMS_{EXPECTED}}{xRMS_{MEASURED}} - 1\right) * 2^{27}$$

Example

With the given example system parameters, the following shows the calculations for AV channel gain.

$$AVRMS_{EXPECTED} = \frac{107310840 * 220}{707} = 33392341 \quad decimal$$

If $AVRMS_{MEASURED}$ is 33512088 decimal then,

$$AVGAIN = \left(\frac{33392341}{33512088} - 1\right) * 2^{27} = -479595 \quad decimal = 0xFFFFF8AE96$$

APPLICATIONS INFORMATION

DC Offset Calibration

All xOS registers shall be 0 for AC metrology applications

RMS Offset Calibration

To calibrate RMS offset register, apply a small signal typically at 5000:1 or less dynamic range to the channel you are trying to calibrate. It is recommended to keep the other channel as nominal. In this example the calibrate the current offset, the calibration current is set to 20 mA and the voltage is kept at nominal.

The expected RMS register value for given input can be calculated as follows:

$$xRMS_{EXPECTED} = \frac{RMS_{FS\_CODES} * X_{REDUCED}}{X_{FS}}$$

where $X_{REDUCED}$ is the reduced calibration signal applied at the ADC input and $X_{FS}$is either V_{FS},I_{FS}or AUX_{FS}.

The xxRMSOS register can be calculated from expected and observed RMS register as follows:

$$xxRMSOS = \left(\frac{xRMS^2_{EXPECTED} - xRMS^2_{MEASURED}}{2^{15}}\right)$$

Example

With the reduced input current to 20mV, the following shows the calculations for AI channel offset.

$$AIRMS_{EXPECTED} = \frac{107310840 * 0.02}{44.188} = 48570 \quad decimal$$

If $AIRMS_{MEASURED}$ is 48733 decimal then,

$$AIRMSOS = \left(\frac{48570^2 - 48733^2}{2^{15}}\right) = -484 \quad decimal \quad = \quad 0xFFFFFFE1D$$

Power Gain Calibration

xPGAIN is the gain calibration register for Phase x. The active and apparent powers in each phase have a common gain register.

Configure ADE9178 as follows:

1. Apply nominal voltage and current at power factor = 1
2. set EP_CFG = 0x17 and EGY_TIME = 99 (1 sec accumulation)
3. Read the xWATTHR_SIGNED_HI register after at least 2 second

The expected xWATTHR_SIGNED_HI register value for nominal inputs can be calculated as follows:

$$xWATTHR\_SIGNED\_HI_{EXPECTED} = I_{FSP} * V_{FSP} * POW_{FS\_CODES} * Accumulation\_Time * 4000 * 2^{-13}$$

where $I_{FSP}$is the nominal current as a fraction of full scale and V_{FSP} is the nominal voltage as a fraction of full scale.

The xPGAIN register value can be obtained as follows:

$$xPGAIN = \left(\frac{xWATTHR\_SIGNED\_HI_{EXPECTED}}{xWATTHR\_SIGNED\_HI_{MEASURED}} - 1\right) * 2^{27}$$

Example

With the given example system parameters, the following shows the calculations for APGAIN.

$$I_{FSP} = \frac{10}{44.188} = 0.22631$$

APPLICATIONS INFORMATION

$$V_{FSP} = \frac{220}{707} = 0.31117$$

$$AWATTHR\_SIGNED\_HI_{EXPECTED} = 0.22631 * 0.31117 * 85829040 * 1 * 4000 * 2^{-13} = 2951248 \quad decimal$$

If AWATTHR_SIGNED_HI$_{MEASURED}$=2846714 decimal then,

$$APGAIN = \left(\frac{2951248}{2846714} - 1\right) * 2^{27} = 4928600 \quad decimal \quad = \quad 0x4B313D$$

Power Offset Calibration

Like the RMS offset calibration, the power offset calibration is performed with a small current at 5000:1 or less dynamic range. In this example, the offset calibration current is 20 mA and the voltage is 220 V.

Configure ADE9178 as follows:

1. Apply nominal voltage and offset calibration current at power factor = 1
2. set EP_CFG = 0x17 and EGY_TIME = 999d (10 sec accumulation)
3. Read the xWATTHR_SIGNED_HI register after at least 20 seconds

The expected xWATTHR_SIGNED_HI register value for nominal inputs can be calculated as follows:

$$xWATTHR\_SIGNED\_HI_{EXPECTED} = I_{FSP} * V_{FSP} * POW_{FS\_CODES} * Accumulation\_Time * 4000 * 2^{-13}$$

where $I_{FSP}$is the nominal current as a fraction of full scale and V_{FSP} is the nominal voltage as a fraction of full scale.

The xPGAIN register value can be obtained as follows:

$$xWATTOS = \frac{xWATTHR\_SIGNED\_HI_{EXPECTED} - xWATTHR\_SIGNED\_HI_{MEASURED}}{Accumulation\_Time * 4000 * 2^{-13}}$$

Example

With the given example system parameters, the following shows the calculations for APGAIN.

$$I_{FSP} = \frac{0.02}{44.188} = 0.00045$$

$$V_{FSP} = \frac{220}{707} = 0.31117$$

$$AWATTHR\_SIGNED\_HI_{EXPECTED} = 0.00045 * 0.31117 * 85829040 * 10 * 4000 * 2^{-13} = 59025 \quad decimal$$

If AWATTHR_SIGNED_HI$_{MEASURED}$=58134 decimal then,

$$AWATTOS = \frac{59025 - 58134}{10 * 4000 * 2^{-13}} = 182 \quad decimal = 0xB6$$

Phase Calibration

It is recommended to keep the voltage channel xVPHCAL as default value (0). To calculate xIPHCAL, apply a nominal current and voltage at lagging power factor of 0.5, calculate phase error from power factor xPF measured as follows.

$$\phi = \frac{\pi}{3} - \cos^{-1}\left(\frac{xPF_{MEASURED}}{2^{27}}\right)$$

The xIPHCAL register can be calculated as follows:

$$xIPHCAL = \frac{\sin(\phi - \omega) + \sin(\omega)}{\sin(2\omega - \phi)} * 2^{27}$$

where ω is equal to

APPLICATIONS INFORMATION

$2\pi * f_{LINE} * \frac{1}{4000}$

Example

If $APF_{MEASURED}$= 67144872 decimal then

$$\phi = \frac{\pi}{3} - \cos^{-1}\left(\frac{67144872}{2^{27}}\right) = 0.00031$$

For 50Hz signal:

$$\omega = 2\pi * 50 * \frac{1}{4000} = 0.07854$$

$$AIPHCAL = \frac{\sin(0.00031 - 0.07854) + \sin(0.07854)}{\sin(2 * 0.07854 - 0.00031)} * 2^{27} = 265515 \quad decimal \quad = \quad 0x40D2B$$

QUICK START

This section describes how to set up the ADE9178 and ADE91xx Chipset for a 3-phase, 4-wire measurement.

1. Configure the HOST MCU to monitor to $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{HOST_RDY}$and $\overline{HOST\_ERR}$ pins of ADE9178.
2. Issue a hardware reset to ADE9178 and ADCs by toggling corresponding reset pins.
   a. SeeHardware Reset section
3. ADE9178 checks the integrity during boot time and both $\overline{HOST\_RDY}$ and $\overline{HOST\_ERR}$ pins go low if the integrity error is detected. If this happens toggle the hardware reset pin of ADE9178. If the error persists , contact support team.
4. Wait for $\overline{IRQ0}$ interrupt from ADE9178.
   a. Read the STATUS0 register and check that the RSTDONE bit is set. Note: RSTDONE bit is expected to be set for first $\overline{IRQ0}$. Otherwise there is an internal error and it is recommended to reset ADE9178.
   b. Clear RSTDONE interrupt by writing 1 to the RSTDONE bit in the STATUS0 register
5. By default all error interrupts in the ERROR_STATUS register are enabled and $\overline{IRQ1}$ will be triggered if there is an error.
   a. The details of the error can be obtained by reading ERROR_STATUS register.
      1. See Interrupts and Status Outputs section for more details.
6. If energy is monitored using the CF outputs, configure the following registers. Skip this section if the CF outputs are not used.
   a. Configure the PWRSEL bits in the CFx_CONFIG register to select the energy type to monitor.
   b. Configure the PHASESEL bits in the CFx_CONFIG register to select the phases to include in the CF calculation.
   c. Configure the ACCMODE bits in the CFx_CONFIG register to select the accumulation mode.
   d. Set the CFx_THR register based on the desired impulse per kilowatt-hour.
      ▶ See CF Pulse Generation section for CFx_THR formula.
   e. Configure the WIDTHSEL bit in the CFx_CONFIG register to set the low pulse width.
      ▶ See Table 16 in "CF Pulse Generation" section for more details.
   f. Enable the CF by clearing the CFDIS bit in the CFx_CONFIG register to 0.
7. If energy is monitored using energy registers, configure the following registers:
   a. Configure the EGY_TMR_MODE bit in the EP_CFG register to select sample (EGY_TMR_MODE = 0) or line cycle (EGY_TMR_MODE = 1) accumulation. Set the desired samples or half line cycles in the EGY_TIME register (N - 1ms for sample accumulation and N - 1 half line cycles for line cycle accumulation).
   b. Configure the EGY_LD_ACCUM bit in the EP_CFG register to add the internal energy register to user energy register on EGYRDY (EGY_LD_ACCUM = 0), or to overwrite the user energy register with the internal energy register value (EGY_LD_ACCUM = 1).
   c. Configure the RD_RST_EN bit in the EP_CFG register to enable reset of user energy registers on read (RD_RST_EN = 1), or to disable reset of user energy registers on read (RD_RST_EN = 0).
   d. Configure the NOLOAD_TMR bits in the EP_CFG register and set the ACT_NL_LVL and APP_NL_LVL level registers to detect no load and prevent energy accumulation of noise. See "No Load Detection" section for more details

APPLICATIONS INFORMATION

8. The ADE9178 can provide interrupts for a variety of events on the $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$ and $\overline{IRQ3}$ pins. The MASK0, MASK1, MASK2, MASK3 or ERROR_MASK and STATUS0, STATUS1, STATUS2, STATUS3 or ERROR_STATUS registers manage the respective interrupt pins.
    a. See "Interrupts and Status Outputs" section for more details.
9. Write calibration coefficient registers to ADE9178.
    a. See Calibration Method section
10. Configure ADC related parameters and start the data processing.
    a. Configure number of ADCs connected by writing to the NUM_ADC bits in the ADC_CONFIG register.
    b. Review ADC_REDIRECT1 and ADC_REDIRECT2 default values and update if the channel mapping required is different to default.
        1. Note, ADC_REDIRECT1 and ADC_REDIRECT2 must be updated if the number of ADCs present is different than the default 4.
        2. See Table 8
    c. Initialize the ADCs by setting ADC_INIT bit in the ADC_CONTROL register to 1 (Auto Clears).
    d. Separately, enable data capture and processing by setting the ADC_RUN bit in the ADC_CONTROL register to 1.
11. See the following sections to set up other metrology features:
    a. Total Active Power
    b. Total Apparent Power
    c. RMS of ONE Cycle
    d. RMS of ½ Cycle
    e. Peak Detection
    f. Dip and Swells
    g. Phase Sequence Error Detection
    h. Zero-Crossing Timeout
    i. Neutral Current Mismatch
    j. PEN Fault Detection
    k. Waveform Streaming
12. Enable energy accumulation by setting the EGY_PWR_EN bit in the EP_CFG register to 1.
13. To prevent any changes to the ADE9178 configuration, enable write protection by writing 1 to the CONFIG_LOCK register.
    a. See Configuration Lock section for more details
14. After the RUN bit of ADC_CONTROL is set , the output registers will be updated at a frequency shown in Table 21.
    a. See Output Register Update Rates section

ORDERING GUIDE

Table 25. Ordering Guide

Model	Temperature Range	Package Description	Landing Pattern
TBD	-40°C to 105°C	5mm x 5mm, 40-pin TQFN-EP	90-0016