***Question 1***

***PT1***

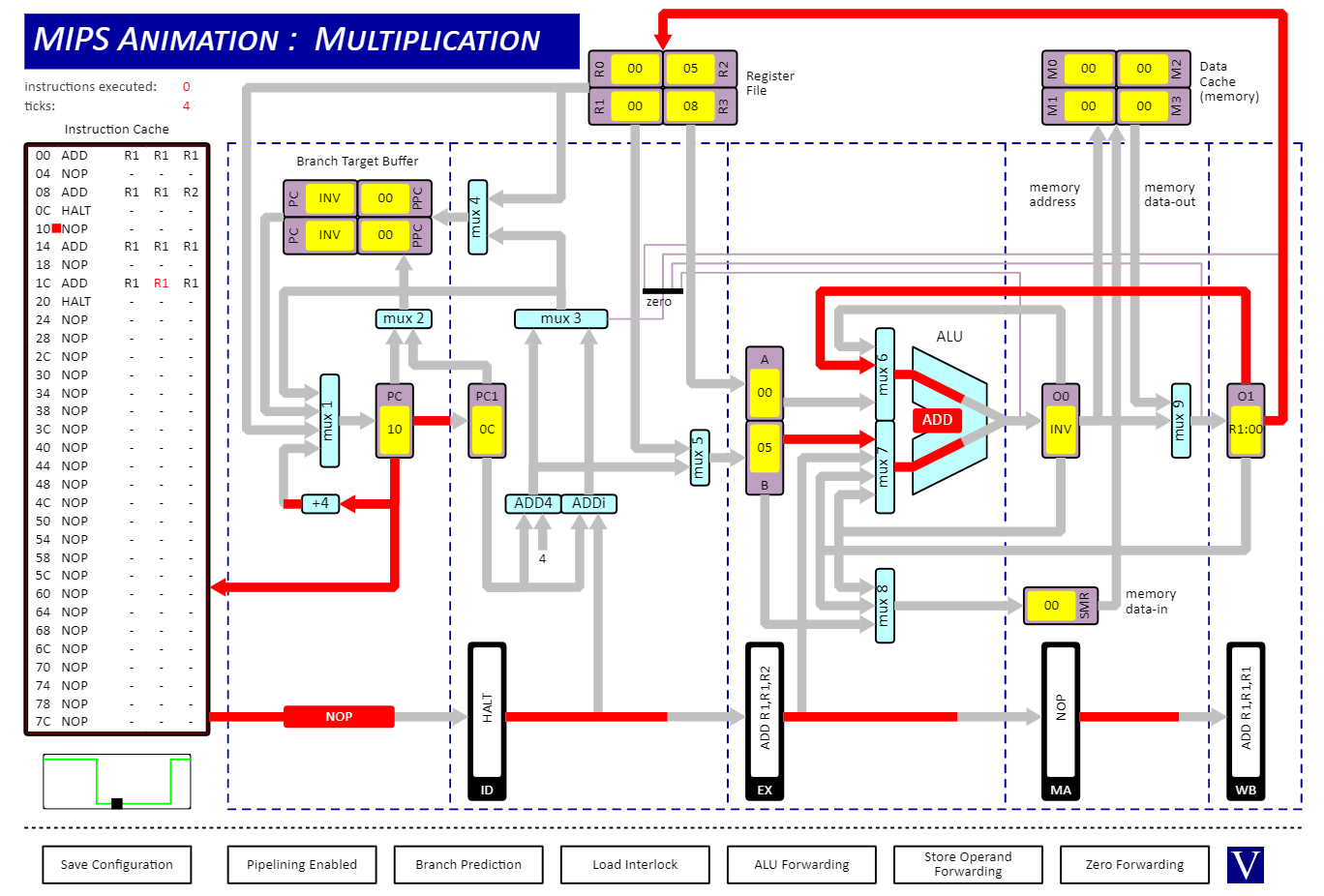
**Instructions**

ADD R1, R1, R1

NOP -, -, -

ADD R1, R1, R2

**Screenshot**



***PT2***

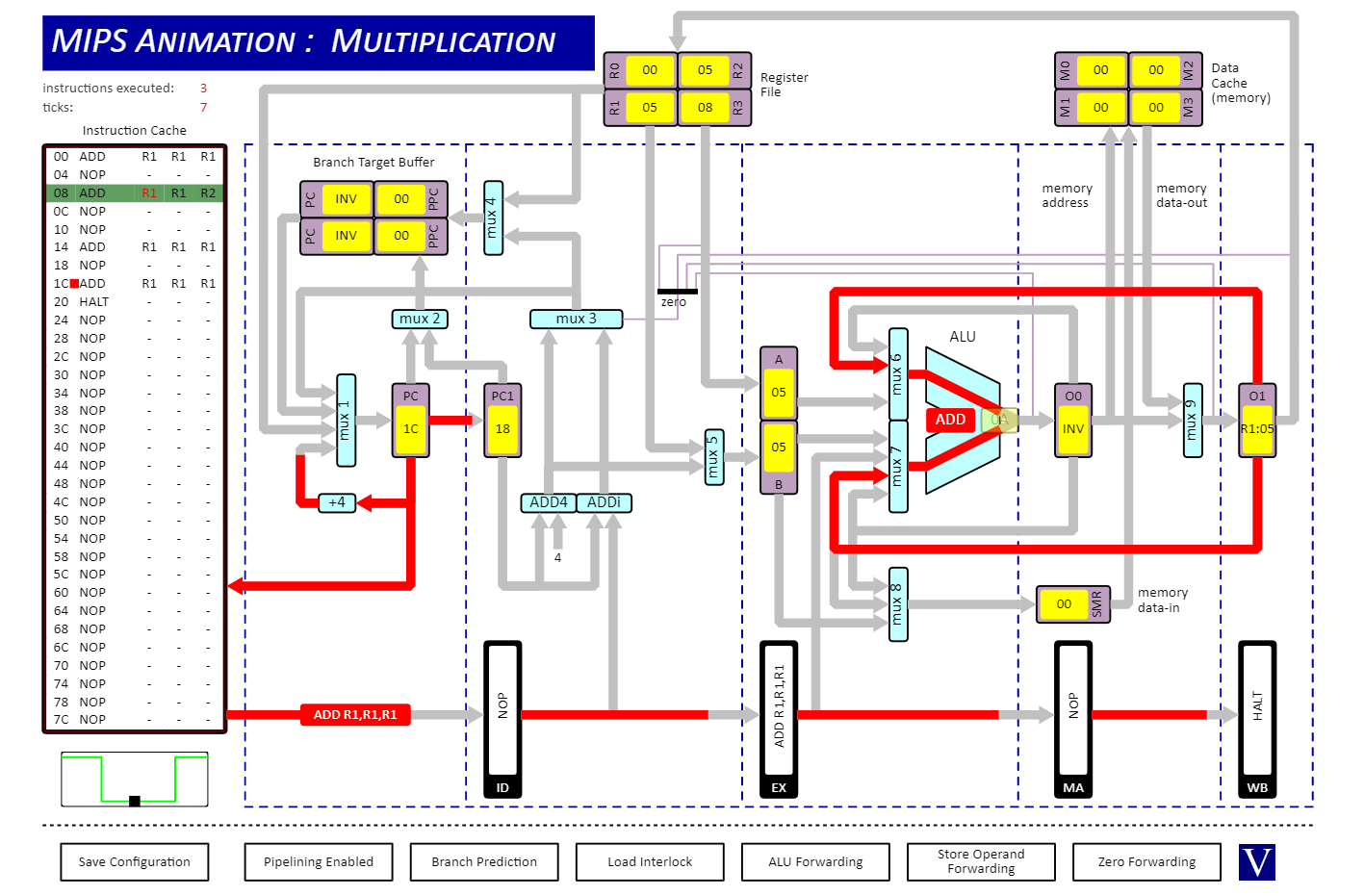
**Instructions**

ADD R1, R1, R1

NOP -, -, -

ADD R1, R1, R1

**Screenshot**

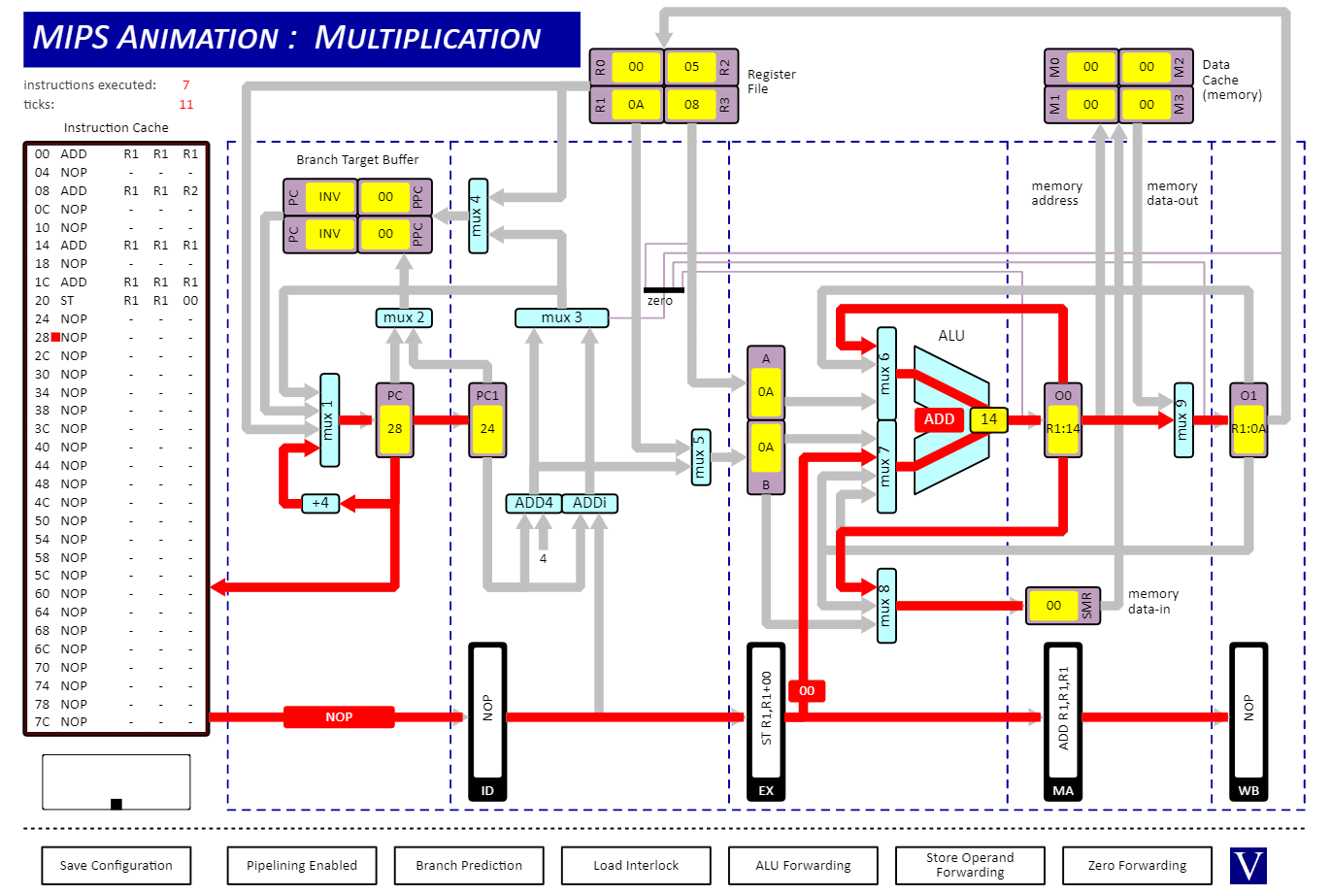


***PT3***

**Instruction**

ST R1, R1, 00

**Screenshot**

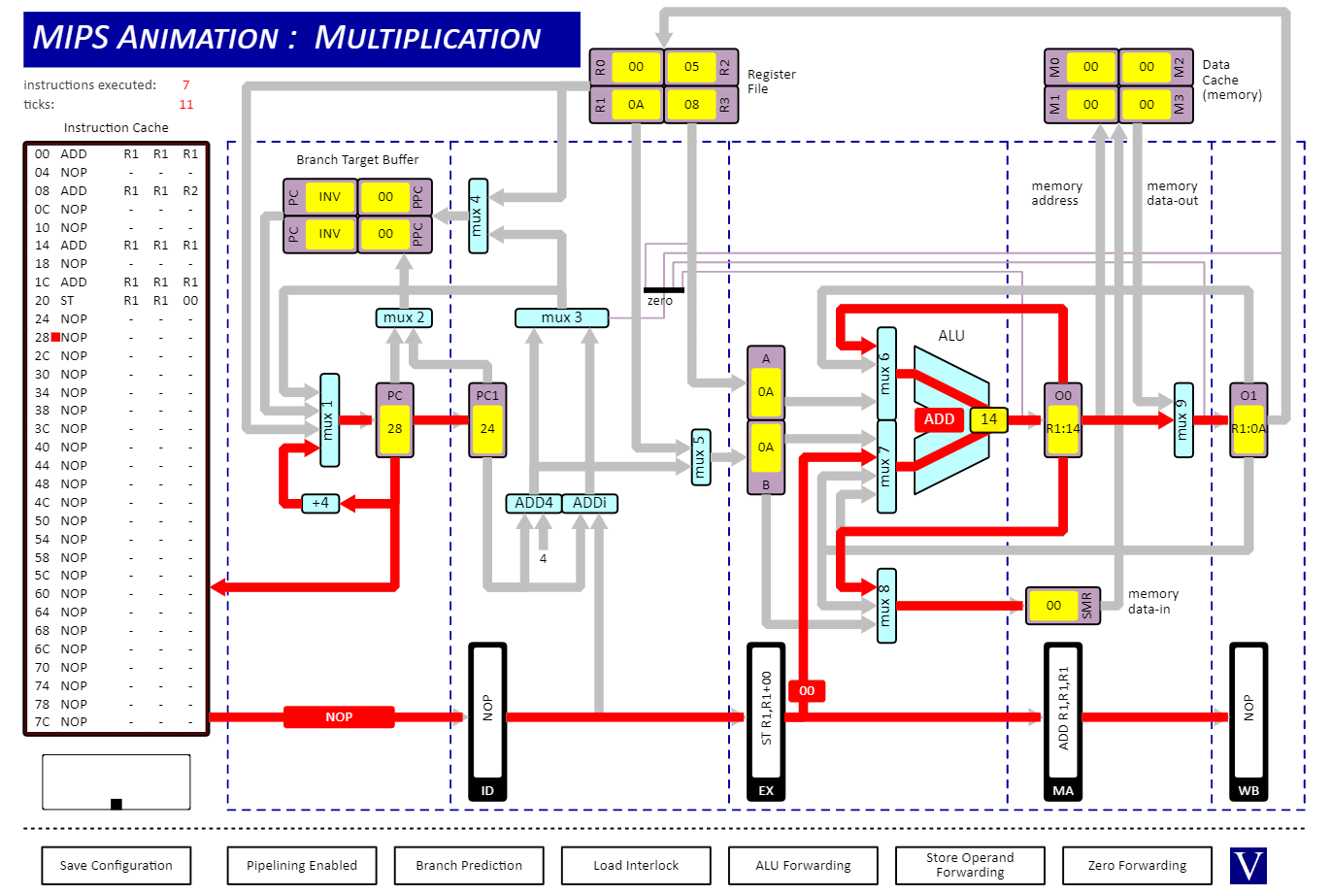


***PT4***

**Instruction**

ST R1, R1, 00

**Screenshot**

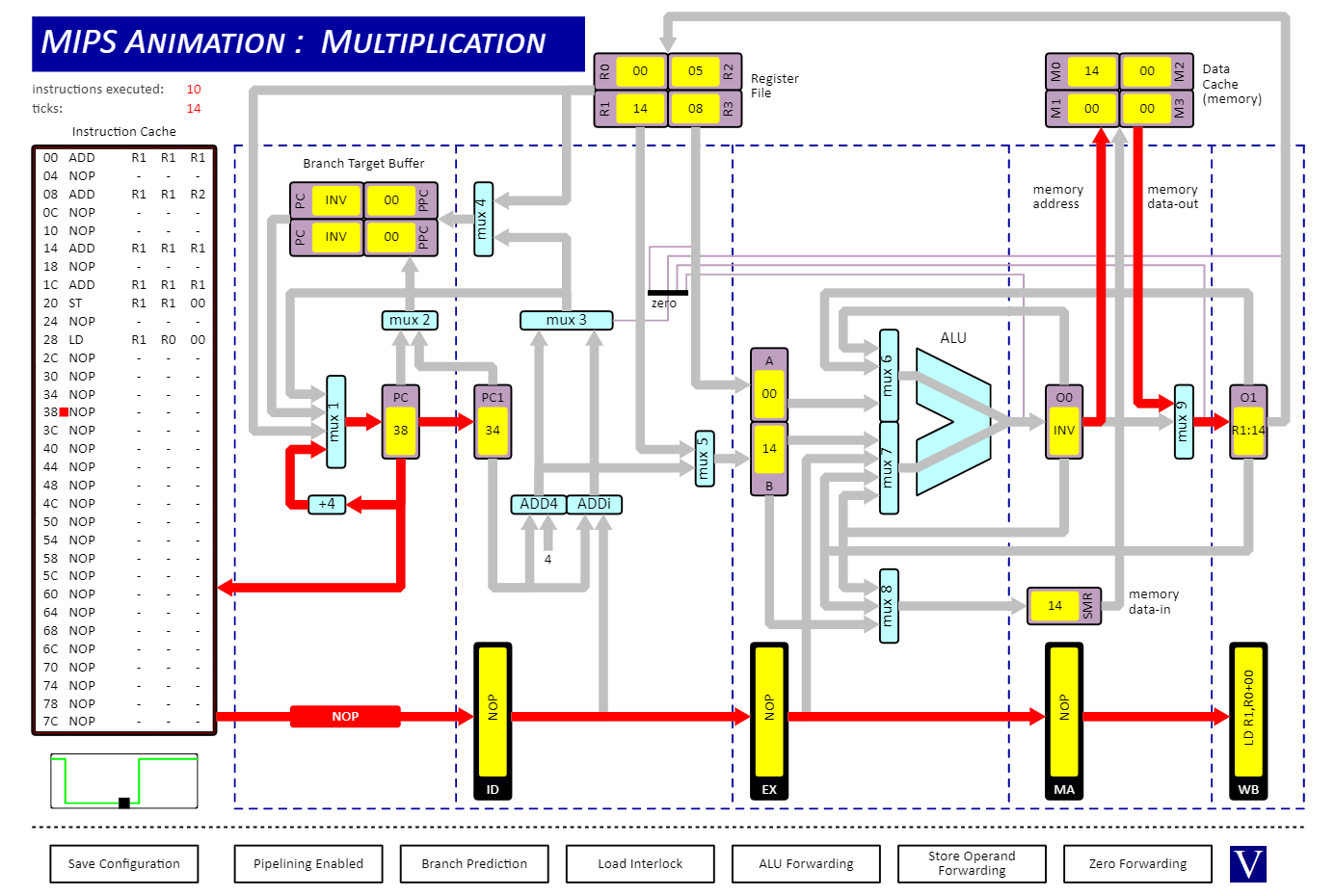


***PT5***

**Instruction**

LD R1, R0, 00

**Screenshot**



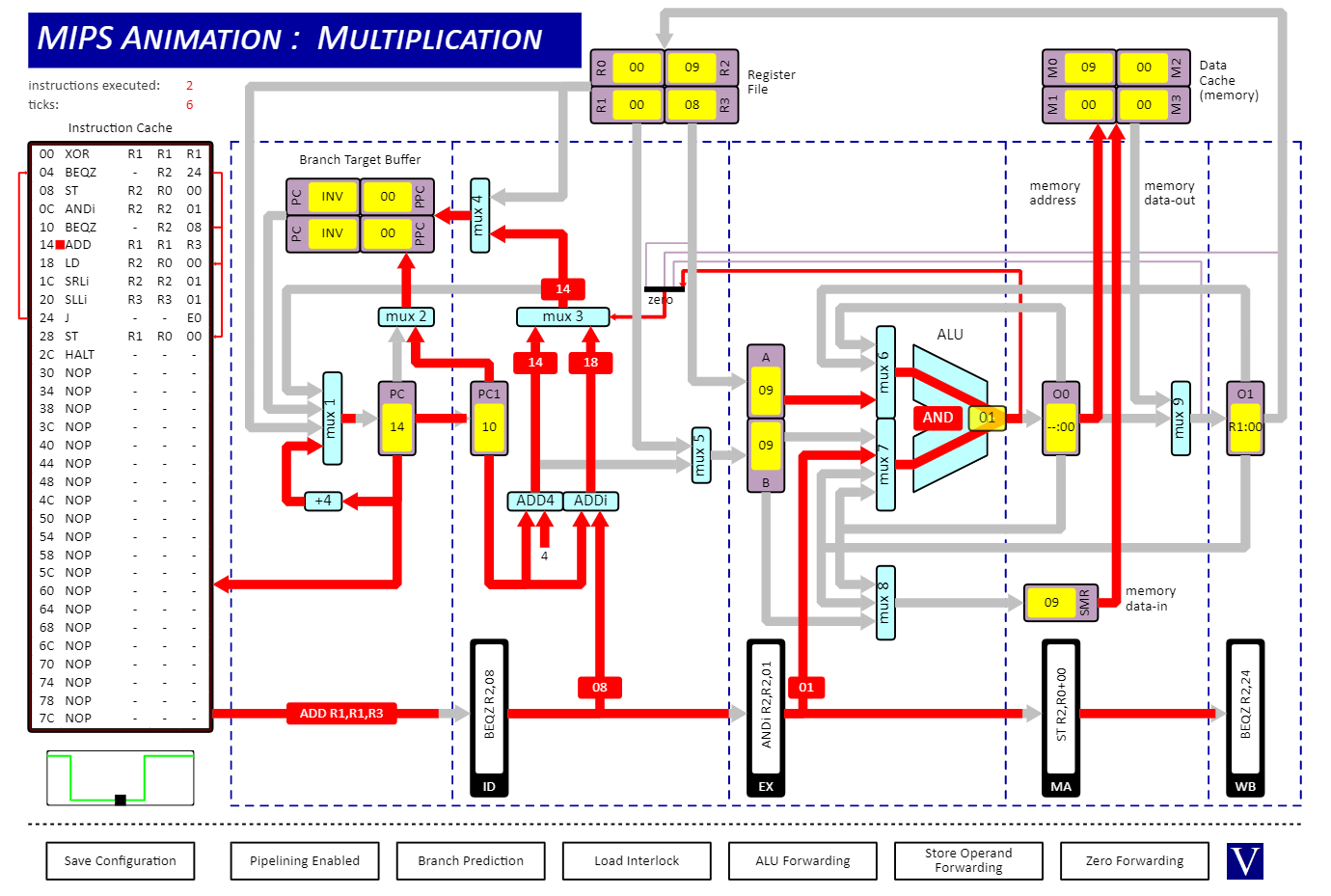
***PT6***

**Instructions**

ANDi R2, R2, 01

BEQZ -, R2, 08

**Screenshot**

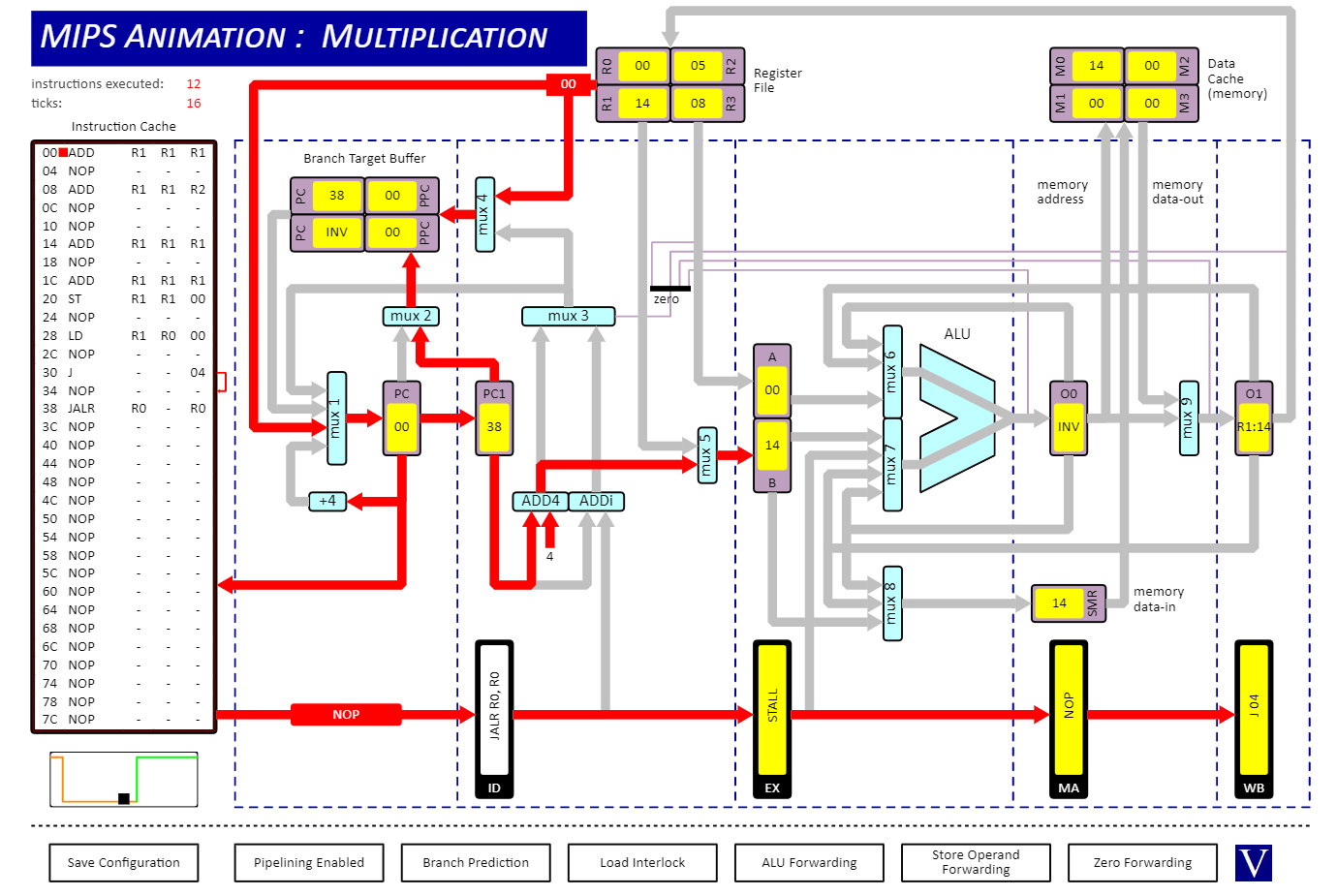


***PT7***

**Instruction**

JALR RO, -, R0

**Screenshot**

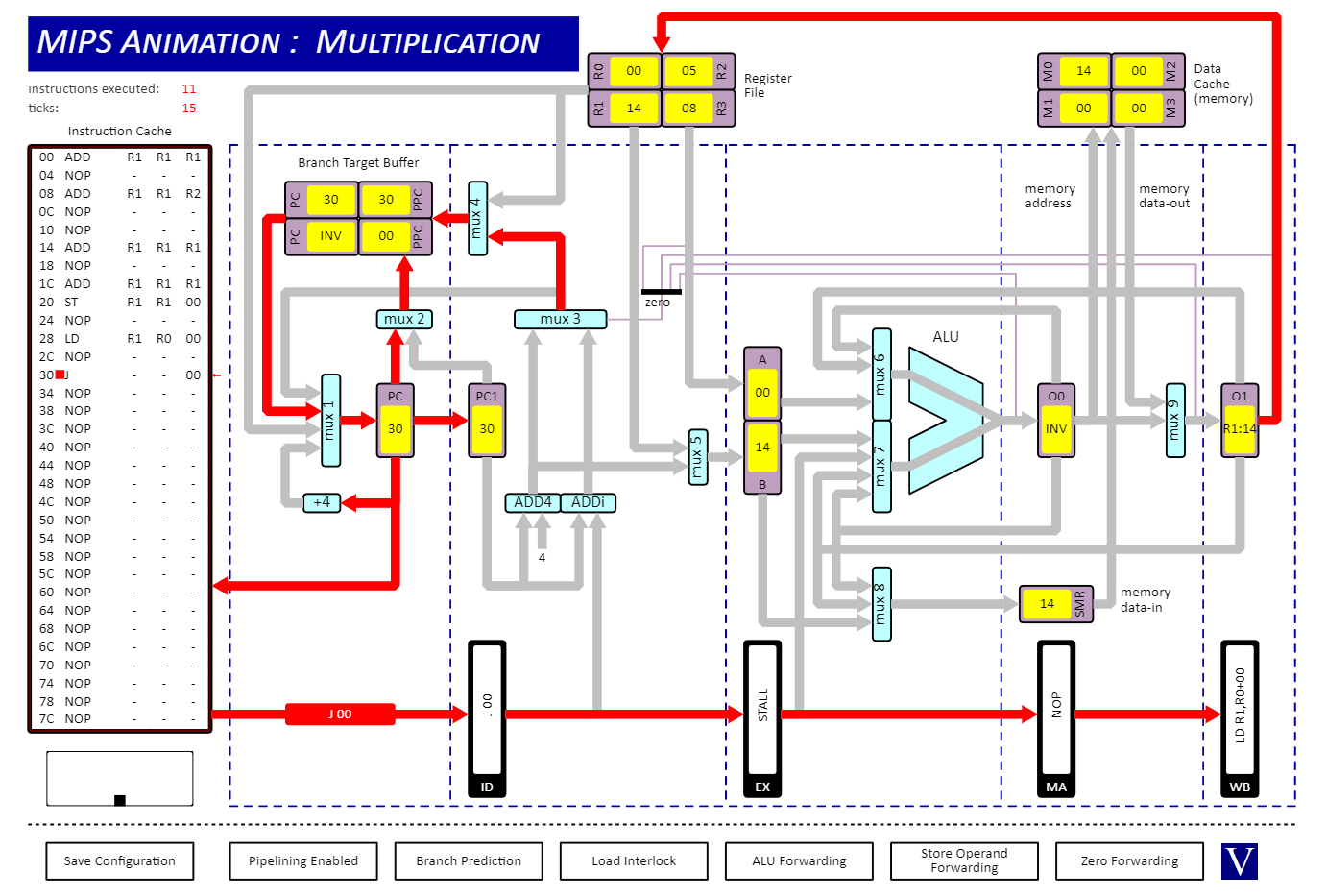


***PT8***

**Instruction**

J -, -, 00

**Screenshot**

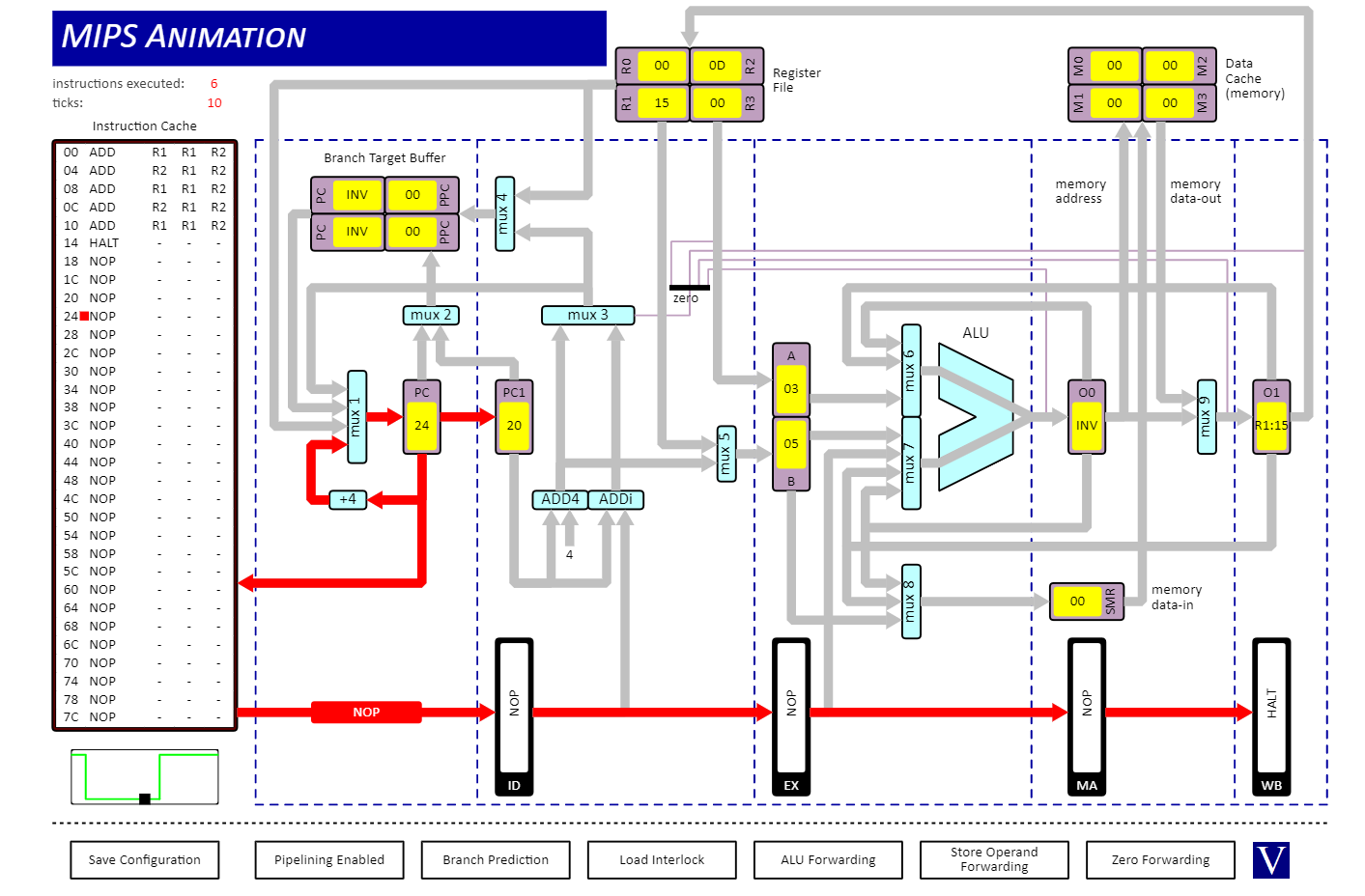


***Question 2***

**Part I**

Number of clock cycles needed to execute : 10

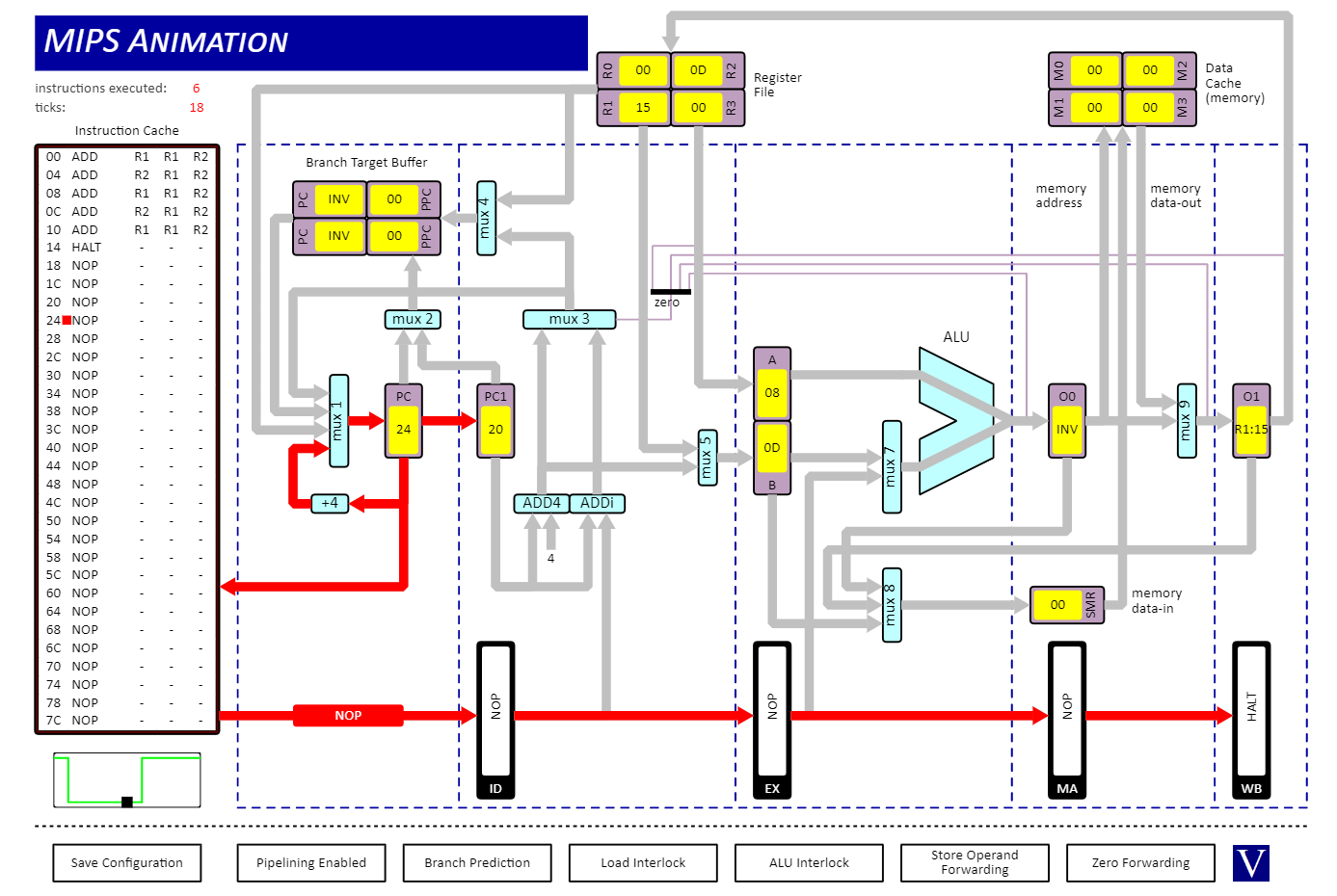
**Screenshot**



**Part II**

Number of clock cycles needed to execute : 18

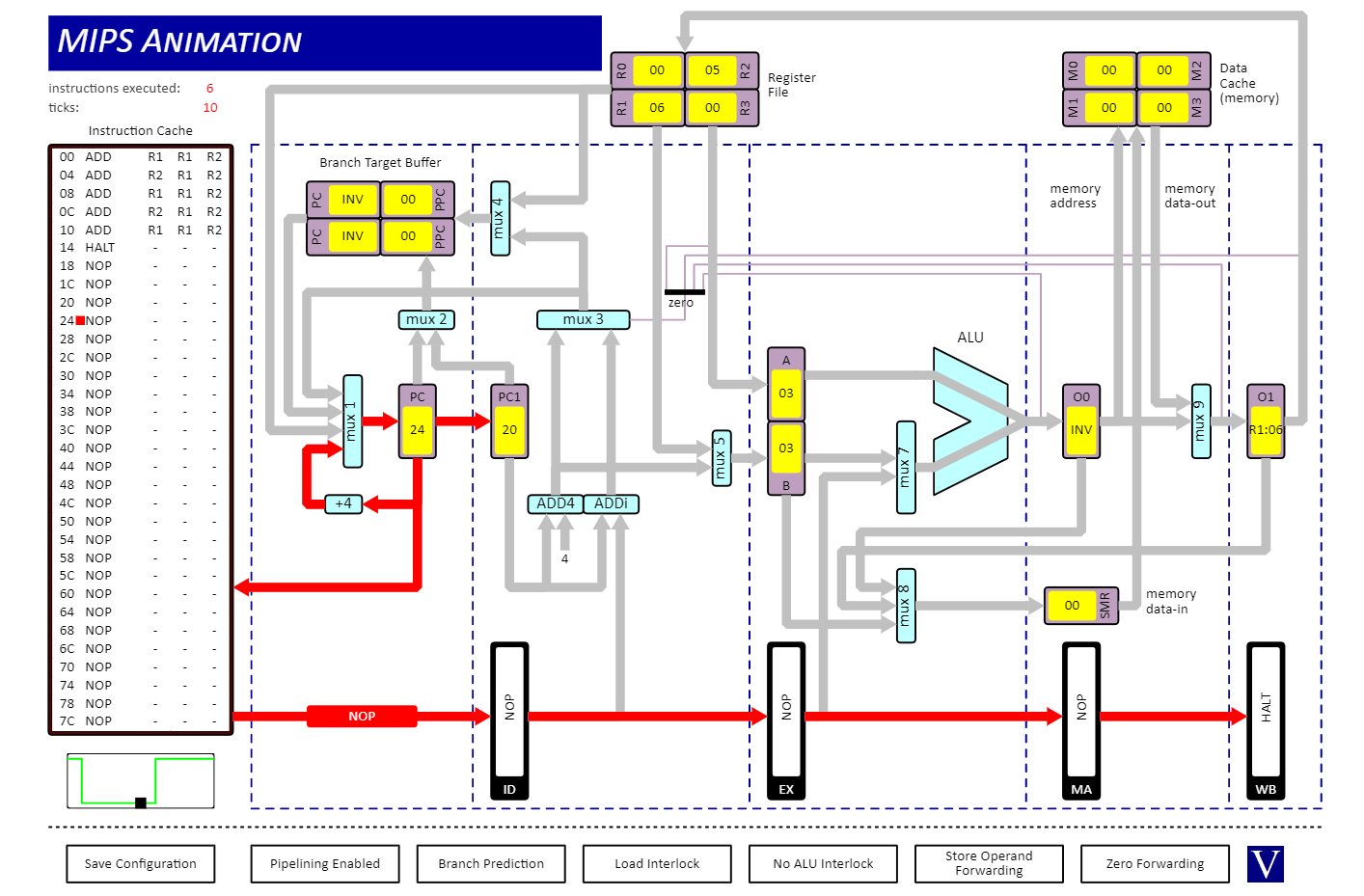
**Screenshot**



**Part III**

Number of clock cycles needed to execute : 10

**Screenshot**



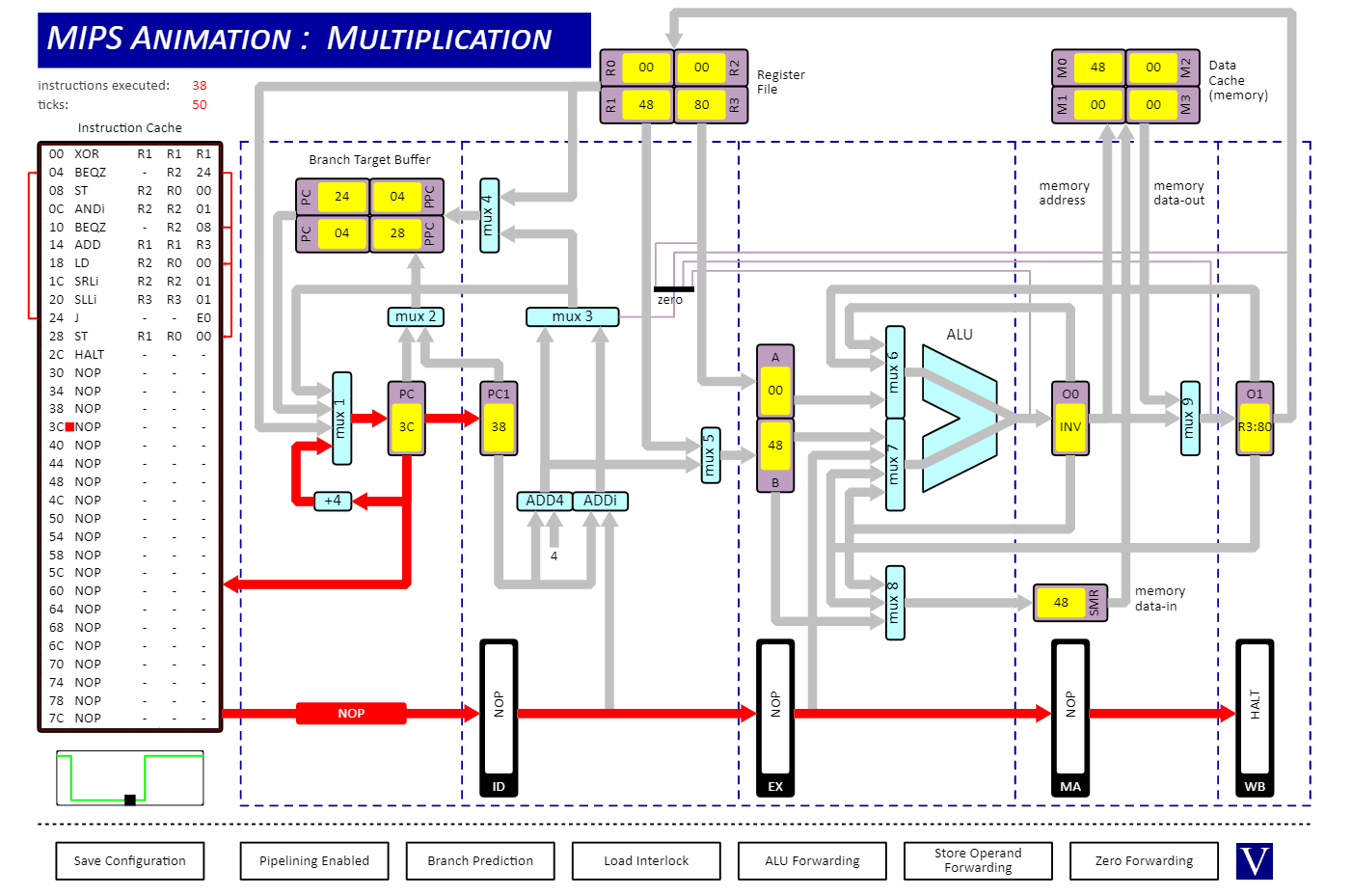
***Question 3***

**Part I**

Number of instructions : 38

Number of clock cycles : 50

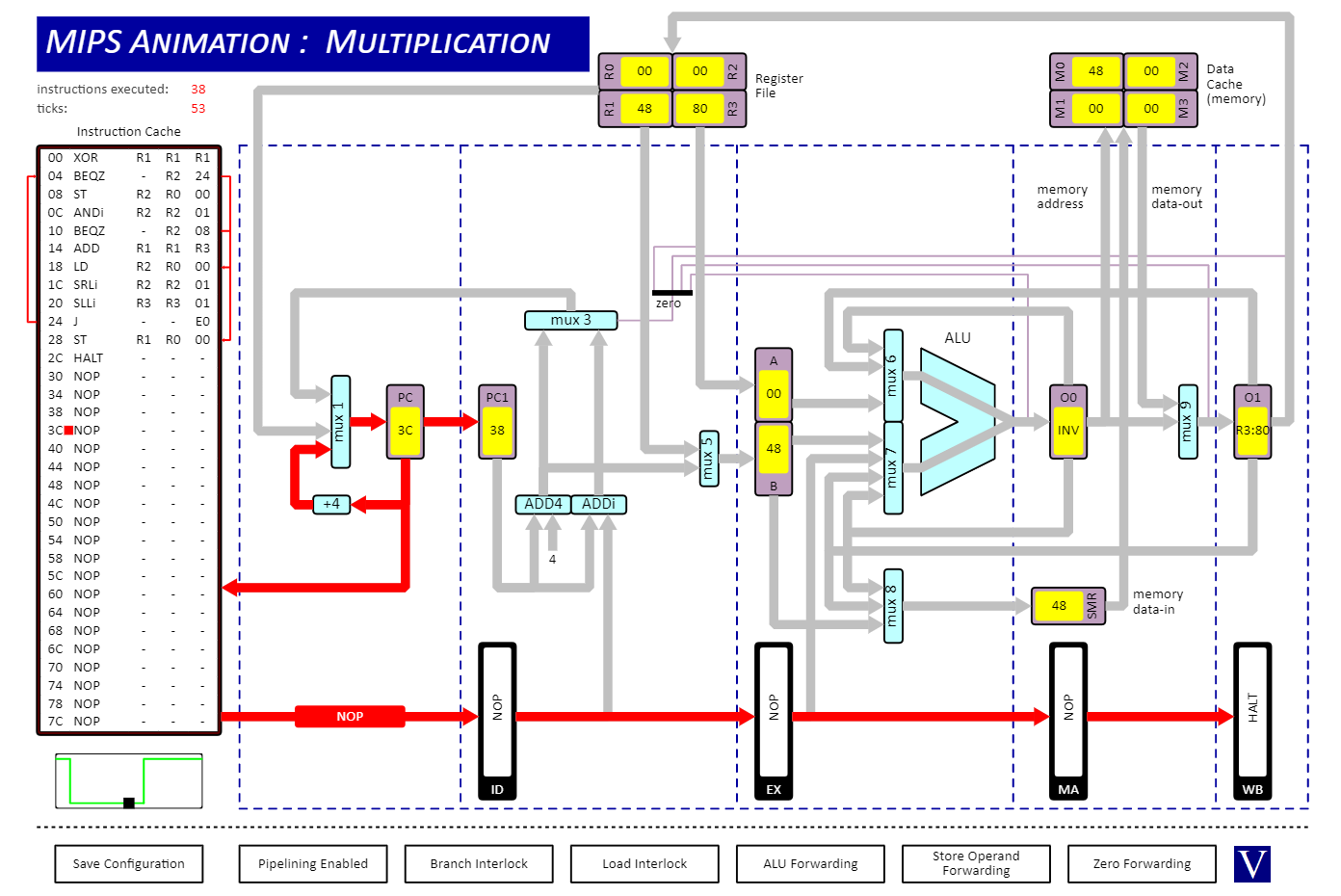
Why are these numbers not equal? Pipeline stalls



**Part II**

Number of instructions : 38

Number of clock cycles : 53



**Part III**

