ECE302 Computer Organization and Architecture L T P C 3 0 0 3

Version No.: 1.20

Prerequisite: ECE103 Digital Logic Design

Objectives:

• To demonstrate the application of discrete mathematics, Boolean algebra, and simple digital design to the field of computers and computer architecture.

- To describe the functioning of the control unit and look at the different implementations of the control unit (hardwired and microprogrammed)
- Recognize and analyze the basics of hierarchical memory and virtual memory.
- To describe I/O system and its interconnection with CPU and memory.
- To expose the learners the different architectural and organizational design issues that can affect the performance of a computer such as Instruction Sets design, Pipelining, RISC architecture, and Superscalar architecture.
- Recognize and illustrate parallel architectures and interconnection networks

Expected Outcome:

- The knowledge of how previous engineering science curricula have been applied in the field of computers and computer architecture.
- The ability to perform basic computer system component designs, defines an instruction set architecture and assembly language for the computer system, analyze the performance of the computer and identify a range of performance enhancements.
- An ability to engage in lifelong learning of the computing system performance and architecture evolution.
- A knowledge of contemporary issues related to the architecture, design, implementation and use of Computers.

Unit I Computing Systems- An Introduction

Definitions - Organization and Architecture, Structure and Functional blocks, Bus interconnection, designing for Performance, Structure of IAS computer.

Unit II Central Processing Unit

Register organization, Arithmetic and Logic Unit- numbering systems, Integer Representation, Integer Arithmetic – Addition, 2's Complement subtraction, Multiplication and division, Floating point Representation and Arithmetic Instruction set, Addressing modes, Data path implementation, Register Transfer Notation (RTN), Abstract RTN, and Concrete RTN, Control Unit - Hardwired control unit and Micro instruction, sequencing and execution.

Unit III Memory System & I/O Organization

Semiconductor RAM memories-Internal organization of Memory Chips, SRAM, DRAM, Read-Only memories-ROM, PROM, EPROM, EEPROM, Secondary storage- magnetic disk, optical memory.

Cache Memories-Mapping Function-Direct, Set Associative, (Replacement algorithms), Performance consideration-Interleaving, Hit Rate and Miss Penalty.

Virtual memory - Address translation, Paging and segmentation.

Unit IV I/O Organization

Interfacing I/O Devices with CPU- Programmed I/O, Interrupt driven I/O, DMA controlled I/O

OPERATING SYSTEM SUPPORT

Overview, Scheduling-FCFS, SJF, Priority, Mutual exclusion, Memory management.

Unit V Computing System Performance and Architecture Evolution

Von-Neumann vs. Harvard architectures, Instruction Cycle- Fetch, Decode, Execute Decode, Moore's law, RISC -Instruction execution Characteristics, use of a large register file, compiler-based registers optimization, pipelining and Pipeline hazards, No. of Pipeline stage, Performance consideration .Instruction level parallelism-overview, Design issues, Super Scalar Processors, VLIW.

Unit VI Multiprocessors

Processor level parallelism-Dependency, Flynn taxonomy, Memory organization for Multiprocessors system, Symmetric Multiprocessor, Cache Coherence and The MESI Protocol.

Textbooks:

- 1. Computer Organization and Architecture William Stallings Sixth Edition, Pearson/PHI 2003.
- 2. Computer Systems Architecture M.Moris Mano, IIIrd Edition, Pearson/PHI 2003.

Reference Book:

1. Computer Organization and Design-the hardware/software interface -David A. Patterson, John L. Hennessy, Third edition, Morgan Kaufmann Publishers, 2009.

Mode of Evaluation CAT- I & II, Quiz, Assignments, Term End Examination.

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