

2023 Digital IC Design Homework 1

NAME	伍志忠						
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Functional Simulation Result							
Stage 1	Pass	Stage 2	Pass	Stage 3	Pass	Stage 4	Pass
Stage 1							
Stage 2							
Stage 3							
Stage 4							
Description of your design							
<p>寫了一個 multi_cmp 在 MMS_4num.v</p> <p>利用 generate 以遞迴的方式自動不停的拆 2 辦</p> <p>用 $sel \wedge (a > b)$ 來決定要輸出那一邊</p>							