2023 Digital IC Design

Homework 1: Max-Min Selector

1. Introduction:

The Max-Min selector (MMS) is a combinational circuit that can output the maximum or minimum value of a set of numbers. In this homework, you are required to design a 4-input MMS circuit, which determines the maximum or minimum value among four input numbers. The 4-input MMS circuit is then used to constitute an 8-input MMS circuit. The specifications and function of the 4-input MMS and the 8-input MMS are detailed in the following sections.

1.1. The 4-input MMS

The logic diagram of the 4-input MMS for this homework is shown in Fig. 1, and its specifications of I/O interface is listed in Table I. Two-staged comparison and selection operation is adopted to select the maximum or minimum value among 4 numbers. The selection of the multiplexers is based on the comparison result and the *select* signal. The comparison and selection operation is shown in Fig. 2, and Table II lists all the selection cases of the multiplexers.

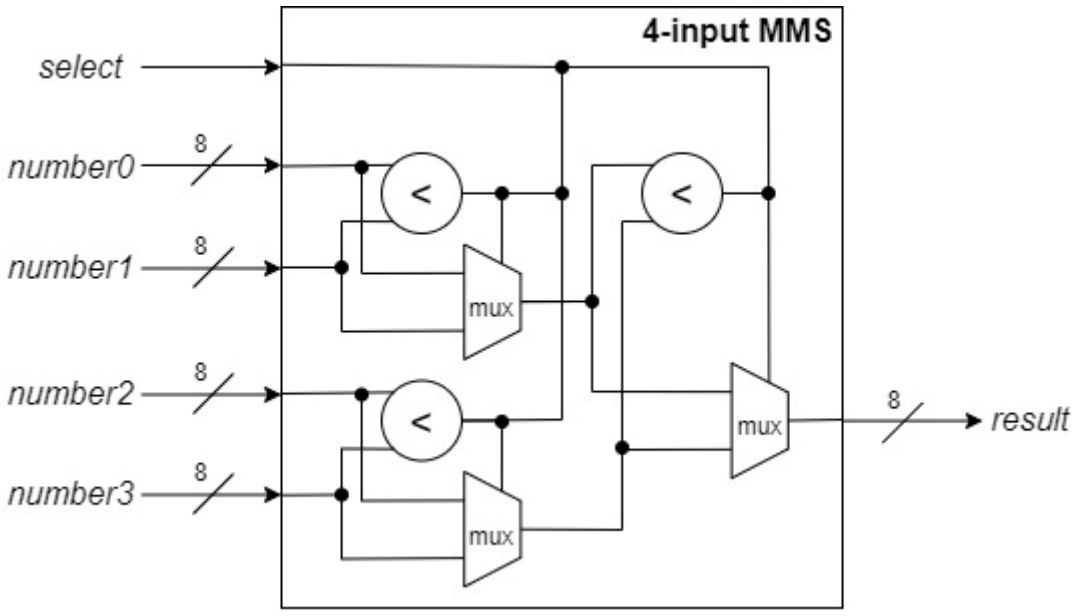

Fig. 1. The logic diagram of the 4-input MMS.

Table I. I/O interface of the 4-input MMS.

Signal Name	I/O	width	Description
number0 ~ 3	I	8	Input number 0 ~ 3
select	I	1	When the *select* signal is 0, *result* should be the maximum value. If the *select* signal is 1, *result* should be the minimum value
result	O	1	Selection result

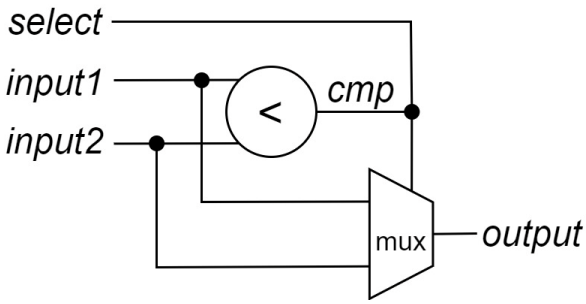

Fig. 2. The comparison and selection operation.

Table II. The selection case of the multiplexer.

{*select*, *cmp*}	*output*
00	*input1*
01	*input2*
10	*input2*
11	*Input1*

1.2. The 8-input MMS

The logic diagram of the 8-input MMS for this homework is shown in Fig. 3, and its specifications of I/O interface is listed in Table III. In this homework, you must construct the 8-input MMS circuit with your 4-input MMS modules. Two 4-input MMS modules are used to select the maximum/minimum value among numbers 0~3 and numbers 4~7, respectively. A comparison and selection operation is adopted to determine the final result of the 8-input MMS.

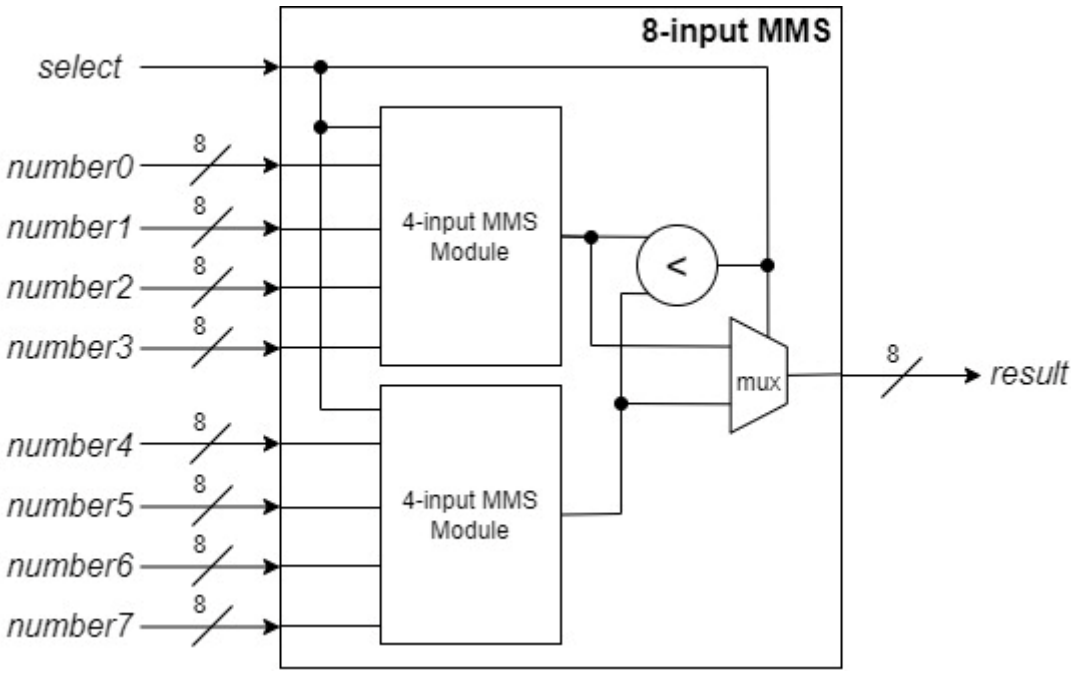

Fig. 3. The logic diagram of the 8-input MMS.

Table III. I/O interface of the 8-input MMS.

Signal Name	I/O	width	Description
number0 ~ 7	I	8	Input number 0 ~ 7.
select	I	1	When the *select* signal is 0, *result* should be the maximum value. If the *select* signal is 1, *result* should be the minimum value
result	O	1	Selection result

1.3 File Description

File Name	Description
MMS_4num.v	The module of 4-input MMS.
MMS_8num.v	The module of 8-input MMS.
MMS_tb.v	The testbench file. The content in this file is **not allowed** to be modified.
test_data_4num.dat	Test data for 4-input MMS verification.
test_data_8num.dat	Test data for 8-input MMS verification.
golden_data_4num.dat	Golden data for 4-input MMS verification.
golden_data_8num.dat	Golden data for 8-input MMS verification.

2. Scoring:

2.1. Maximum selection with 4-input MMS [30%]

The result should be generated correctly, and you will get the following message in ModelSim simulation.

```
# -------------Stage 1 : Maximum selection with 4-input MMS-------------
#
# -------------Stage 1 :              Pass!                -------------
```

Fig. 4. Simulation result for maximum selection with 4-input MMS.

2.2. Minimum selection with 4-input MMS [30%]

The result should be generated correctly, and you will get the following message in ModelSim simulation.

```
# -------------Stage 2 : Minimum selection with 4-input MMS-------------
#
# -------------Stage 2 :              Pass!                -------------
```

Fig. 5. Simulation result for minimum selection 4-input MMS.

2.3. Maximum selection with 8-input MMS [20%]

The result should be generated correctly, and you will get the following message in ModelSim simulation. Please construct the 8-input MMS circuit with your 4-input MMS modules. Otherwise, you can just get half of the points.

```
# -------------Stage 3 : Maximum selection with 8-input MMS-------------
#
# -------------Stage 3 :              Pass!                -------------
```

Fig. 6. Simulation result for maximum selection with 8-input MMS.

2.4. Minimum selection with 8-input MMS [20%]

The result should be generated correctly, and you will get the following message in ModelSim simulation. Please construct the 8-input MMS circuit with your 4-input MMS modules. Otherwise, you can just get half of the points.

```
# -------------Stage 4 : Minimum selection with 8-input MMS-------------
#
# -------------Stage 4 :              Pass!                -------------
```

Fig. 7. Simulation result for minimum selection with 8-input MMS.

3. Submission:

3.1. Submitted files

You should classify your files into two directories and compress them to .zip format. The naming rule is HW1_studentID_name.zip. If your file is not named according to the naming rule, you will lose five points.

	RTL category
*.v	All of your Verilog RTL code
	Documentary category
*.pdf	The report file of your design (in pdf).

3.2. Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible.

3.3. Note

Please submit your .zip file to folder HW1 in moodle.

Deadline: 2023/3/20 23:55

If you have any problem, please contact TA by email

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