2023 Digital IC Design Homework 3

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| NAME | 伍志忠 | | | | |
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| **Simulation Result** | | | | | |
| Functional simulation | | Score:100 | | Gate-level simulation | Score:100 |
| (your functional sim result) | | | |  | |
| **Synthesis Result** | | | | | |
| Total logic elements | | | 124 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 1 | | |
| Total cycle used | | | 938 | | |
| Clock width | | | 5 | | |
|  | | | | | |
| **Description of your design** | | | | | |
| 1.先用一個reg把東西接起來  2.把8bit ascii碼轉成自己的編碼  3.存進一個queue，方便之後暫停 3.prefix轉postfix，分別存進num和跟op(+-\*等等)的stack  4.當處理時遇到需要輸出，就開始做運算邊把東西pop出來 5.最後剩2個以下數字並且運算符號是等於時，輸出 | | | | | |

*Scoring = Area cost \* Timing cost*

*Area cost = Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used \* Clock width*

**\* Total logic elements must not exceed 1500.**