2023 Digital IC Design Homework 4

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| NAME | 伍志忠 | | | | |
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| **Simulation Result** | | | | | |
| Functional simulation | | 100 | | Gate-level simulation | 100 |
| (your functional sim result) | | | | (your gate-level sim result) | |
| **Synthesis Result** | | | | | |
| Total logic elements | | | 348 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 3 | | |
| Total cycle used | | | 12327 | | |
|  | | | | | |
| **Description of your design** | | | | | |
| 以x,y的奇偶分成四個group，左上角要資料要9個點，以S形跑過每個點，其他點可以重複利用前一次要的6個資料，因此其他點只要要3次資料。  要完資料後，乘法，加總，輸出到mem  其中L1是L0每次輸出前先要資料，然後跟conv round up後的資料比較大小後輸出。 還有加上一些眉眉角角偷面積的地方，像是Embedded multiplier 9-bit elements不知道為什麽只算9的面積，因此加上(\* multstyle = "dsp" \*)強制使用dsp block等等，不然位移應該是比較好的作法。 | | | | | |

*Scoring = (Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements) X Total cycle used*

**\* Total logic elements must not exceed 1000.**