2023 Digital IC Design Homework 4

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| --- | --- | --- | --- | --- | --- |
| NAME |  | | | | |
| Student ID |  | | | | |
| **Simulation Result** | | | | | |
| Functional simulation | | Score | | Gate-level simulation | Score |
| (your functional sim result) | | | | (your gate-level sim result) | |
| **Synthesis Result** | | | | | |
| Total logic elements | | |  | | |
| Total memory bits | | |  | | |
| Embedded multiplier 9-bit elements | | |  | | |
| Total cycle used | | |  | | |
| (your flow summary) | | | | | |
| **Description of your design** | | | | | |
|  | | | | | |

*Scoring = (Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements) X Total cycle used*

**\* Total logic elements must not exceed 1000.**