2023 Digital IC Design Homework 5

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| **Simulation Result** | | | | |
| Functional simulation | | Completed | Gate-level simulation | Completed |
| (your functional sim result) | | | (your gate-level sim result) | |
| **Evaluation Results** | | | | |
| test1.png | | 32.03 | test2.png | 33.72 |
| test3.png | | 35.9 | test4.png | 28.37 |
| test5.png | | 29.7 | test6.png | 34.03 |
| **Description of your design** | | | | |
| 先用某個進階板的bilinear（<https://casual-effects.com/research/McGuire2009Bayer/bayer-jgt09.pdf>），再用修改過的EECI，藉由限制a+1=2^n，因此weight必定是2^N，方便乘法的計算，而weight加總除法的部份由於排列下來只有439種，因此寫了另一個c產生LUT將除法變成乘法計算。  該硬體由於會跑一次進階板的bilinear跟兩次EECI，需要跑15882100 NS | | | | |

*Scoring = average PSNR of the six test images*

**\* PSNR of all interpolation results should meet at least the baseline.**