Computational Storage: Where Are We Today?

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ABSTRACT

Computational Storage Devices (CSDs), which are storage devices including general-purpose, special-purpose, and/or reconfigurable processing units, are now becoming commercially available from different vendors. CSDs are capable of running software that usually run on the host CPU – but on the storage device, where the data reside. Thus, a server with one or more CSD may improve the overall performance and energy consumption of software dealing with a large amount of data.

With the aim of fostering CSD's research and adoption, this position paper argues that commercially available CSDs are still missing a wealth of functionalities that should be carefully considered for their widespread deployment in production data centers. De facto, existing CSDs ignore (heterogeneous) resource management issues, do not fully consider security nor multi-user, nor data consistency, nor usability. Herein, we discuss some of the open research questions, and to what degree several well-known programming models may help solving them – considering also the design of the hardware and software interfaces.

1 Introduction

Computational Storage (CS) is a type of near data processing [16] architecture that enables data to be processed within the storage device in lieu of being transported to the host central processing unit (CPU) [12]. Figure 1 generalizes several CS architectures investigated by SNIA [11].

CS architectures introduce numerous advantages: a) unload the host CPU(s) – thus, a cheaper CPU can be installed, or the CPU can run other tasks; b) decrease data transfers, increase performance – only essential data need to be transferred from the storage to the CPU, general- or special-purpose processing elements or reconfigurable units on the CS device(s) may process data instead of the CPU, even in parallel; c) reduce energy consumption – a storage device on PCIe cannot consume more than 25W in total [41], thus processing units on computational storage devices (CSDs) consume just a fraction of it, versus server-grade host CPU power consumption that floats around 100W; d) preserve data-center infrastructure expenditure – scales data-center performance without requiring investments in faster networks.

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While research on in-storage processing on HDDs [12, 34] and SSDs [37, 31, 29, 42] has been carried on since the 1990's and 2010's, respectively, only recently CS platforms becomes commercially viable with a few companies already selling SSDs with CS capabilities – e.g., Samsung [9], NGD [6], and ScaleFlux [10]. Despite CSDs' market appearance, these devices are cumbersome to program and reason with, which may hinder their wide adoption. In fact, there is no software nor hardware support for processing units resource management in CSD, nor security, consistency and general usability consideration.

Based on the authors experience working on several academic and industry CS prototypes in the latest years, this paper is an attempt at reviewing the state-of-the-art, listing the most pressing open research questions with CSD, and analyzing the suitability of different programming models in answering such questions – without forgetting about the hardware/software interface that is still not CSD ready. This work focuses on single direct-attached CSD, with storage and compute units resident on the same device. However, we believe the same findings apply widely, such as to smart disk array controllers. Additionally, the work generically looks at CSD with general-purpose CPUs, special-purpose CPUs, as well as CSD with re-configurable hardware (FPGA). Hence, we will refer to all of those as "processing units".

Briefly, our conclusion is that hardware and software for CSD is not ready yet, and more have to be done at the hardware and software level to fully leverage the technology at scale.

2 Background and Motivation

Computational storage *reduces the input and output transaction interconnect load* through mitigating the volume of data that must be transferred between the storage and compute planes. As a result, it stands to better serve modern workloads such as high-volume big data analytics and AI tasks with faster performance [27], to improve data center infrastructure utilization [29], together with many other benefits. We discuss several below.

A primary benefit of computational storage is *faster and more energy-efficient data processing.* Computational storage architectures offload work usually processed by host compute elements – CPU and eventual accelerators, to storage devices. Without CS, for example in the data analytics context, a request made by the host compute elements requires that all data from a storage device be transferred to it. The host compute elements must then thin down the data prior to performing their designated task. In a CS approach, the storage device takes the initial step of qualifying data based on its relevance following an host request – before moving the data to the main compute tier to be processed. Thus, possibly reducing the amount of data to be moved and processed by the host. The reduced host compute instructions per work-

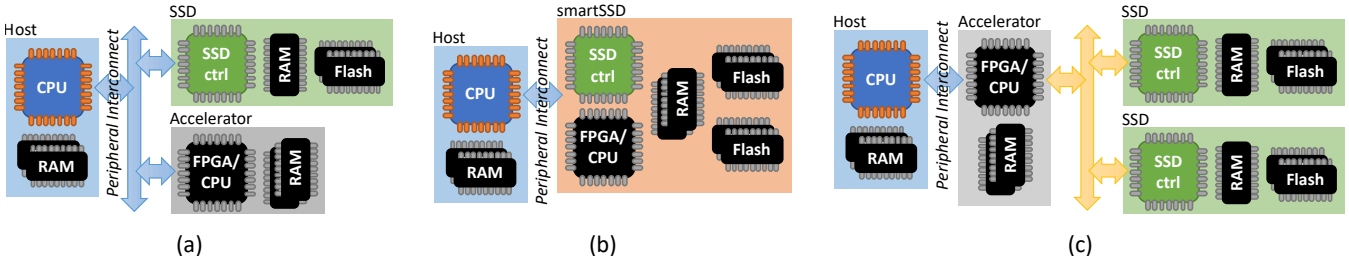

Figure 1: A few architectures of computational storage devices considered in the SNIA CS SIG [43]. (a) An FPGA and/or a CPU (with DRAM, but without storage media) sits along with an SSD on a peripheral interconnect; (b) An FPGA and/or a CPU is bundled together within an SSD (including SSD controller, RAM and storage media); (c) An FPGA and/or a CPU (with DRAM, but without storage media) on a peripheral interconnect connect to one or more SSD via another interconnect.

load means that the host CPUs, and eventual accelerators, have more processing power available to support other workloads.

Another benefit of computational storage is that it *makes a shared storage environment more beneficial to the most performance-hungry workloads*. Typically, a direct-attached storage approach is used to serve these workloads to avoid storage network latency, but also to increase throughput by spreading the data across many devices. However, this often results in resource underutilization, and also introduces further delay by needing to search multiple devices for the relevant data. In contrast, CS allows applications to be executed into each storage device, at the same time. This provides a level of parallel processing to enable a microservices-like approach to running those applications across all the individual devices. Such ability to process the data simultaneously greatly reduces the time to locate the data and provide the host the results needed.

Computational storage can also help *leveraging the existing network infrastructure for much longer*, as well as to truly scale next-generation networks. Because computational capabilities enable the storage to work on a larger data set first, it leverages higher I/O capabilities of modern SSDs and avoids performance being restricted by a network. As a result, the network interconnect is less critical with computational storage. Thus, computational storage stands to add value by enabling multiple applications' performance to be accelerated on the same infrastructure, while at the same time optimizing utilization of infrastructure resources across the stack.

2.1 State of Hardware and Software

Most SSDs have dedicated processing and memory elements – i.e., embedded multicore CPU or FPGA, and DRAM, other than flash memory. Those are used to execute read, write, and erase commands on user data, as well as flash management functions.

With available computing resources on SSDs, several projects [31, 42, 29, 12, 38, 25, 35, 14, 28, 46, 36, 39, 45, 44, 24, 35, 13, 23] explored opportunities to run user-defined data-intensive compute tasks, such as database operations, in the SSD device itself. While performance improvements and energy savings were observed, several challenges prevented the broad usage and adoption of computational SSDs. First, the processing capabilities available were limited by design: low-performance embedded processors, or resource constrained FPGAs, and the high-latency to the in-storage DRAM require extra careful programming to run user-defined code to avoid performance limitations. Second, a flexible and generic interface and programming model to easily execute on an SSD user-defined code written in a high-level programming language (such as C/C++) were never defined. Additionally, the programming model also needs to support the concurrent execution of various in-storage applications with multiple threads to make it an efficient platform for complex user applications. Nevertheless, interfaces at different layers of the hardware and software have to be defined on the host and CSD to make a platform actually usable. Third, none considered how to handle multiple users.

Such works have been carried on a multitude of different hardware and software. To the best of our knowledge, as of today there are just two CSD development boards openly available: the OpenSSD [1] from Hanyang University (implementing the architecture in Figure 1.b), and the DFC [26] developed by a collaboration of DellEMC and NXP (implementing the architecture in Figure 1.c). Both feature a multicore ARM general purpose-processor, accelerators, and re-configurable hardware, other than a sort of Flash memory and DRAM. Despite open-source, they are based on old standards and are not supported anymore. On the other hand, storage vendors have their own non-openly available prototypes [31, 38, 15], and FPGA boards have been used for research [42, 46] – which are not easily accessible to non FPGA-experts. Simulation environments from the academic community exist as well [30, 8, 15], but lack support.

Very recently, CSDs become available on the market, including NGD in-situ processing SSD [6] that features multiple 64bit ARM cores, ScaleFlux CSD [10] and Samsung SmartSSD [9] based on FPGA (implementing the architecture in Figure 1.b). Other products, such as Eideticom NoLoad Computation Storage Processor [5], implement storage and compute on different PCIe boards, as depicted in Figure 1.c, enabled by p2p DMA and NVMe's CMB [21]. These products triggered SNIA to working on a proposal to extend the NVMe protocol for CSD [11] – which at the moment is work in progress. Hence, we believe that something should be done soon in order to make computational storage devices more compelling to the masses. Notably, mainly due to companies IP matters, current CSD products provide very limited customizability, and cannot be easily used for research purposes, such as interface or programming model exploration.

3 Open Research Questions

We believe that showing improved performance and energy reductions is not enough to persuade the widespread adoption of CSD. Hence, herein we present a variety of open research questions identified within existing CS technologies, involving a) resource management, b) security, c) data consistency, and d) usability.

3.1 Resource Management

A server with one or more CSDs is per-se a single system. But from the software point of view, since each (group of identical)

processing units, on the motherboard or on any CSD, runs its own software stack, such server looks like a distributed system. Resource management in single systems as well as in distributed systems is fundamental to provide efficient and fair usage of hardware resources, including processing units, memory, and storage. For example, this implies that at any given time no single resource is overloaded nor applications are starving for resources. Similarly, a single user shouldn't monopolize the usage of all resources. Resource management policies may be needed to balance the workload among compute resources in order to meet performance and power goals. However, this is lacking in emerging CS architectures and in related works.

Questions. a) Where to take resource management decision? On the host CPU or on each CSD, or on both? b) When there is replication among CSDs, on which replica to map a certain computation? c) How to maintain workload and energy consumption information across available processing units on the host and the CSDs?– especially, with the aim of taking resource management decisions? d) What to do when CSDs are overloaded? Should the overloaded CSD notify the host or other CSDs, and then what? e) How to provide fairness of resources (such as CPU cycles, FPGA real-estate, memory/flash space, and flash-channel traffics) among different users? f) How to map data to multiple CSDs, and/or to different flash channels inside a CSD? g) For applications that do use a single CSD, what is the break-even point between running on the host CPU and on the CSD? (Is this workload dependent?)

3.2 Security

When a single SSD stores data from different users it is fundamental to do not allow users to access each other's data. With today's SSDs, there are two different approaches for controlling data access. The first is to use a file system – each file has an owner, etc. The second is to use either hardware virtualization (SRIOV) or NVMe namespaces [7], in order to assign different part of the storage to different owners. Despite the existence of protection mechanisms, the code running on the CSD's processing unit (CPU, accelerator, FPGA) has potentially access to all data stored on the flash chips. When using a file system for access control, it is fundamental to define secure mechanisms and techniques to maintain the same concept of users internally and externally. This is due to the semantic gap between the storage device and software running on the host CPU – the host CPU knows about the file system, and users, but that is not always true for the storage device. It is worth noting that users' knowledge can be asymmetric, in the sense that a CSD doesn't need to know all users' details as the host CPUs in most of the cases. The code running on the CSD should access only what it is allowed to access.

Another problem is trusting the identity and integrity of the reconfigurable hardware, software, and firmware on the CSD itself. Assuming a method to only install proper firmware and systems software exists, it is fundamental that only and exclusively user-submitted code runs on the CSD other than that. Moreover, user-submitted code should not alter the integrity of the firmware and systems software on the CSD.

Questions. a) How to isolate multiple applications among each other on the CSD? b) How to make them safe from about denial of service? c) Diverse programming models require different isolation techniques. For example, hardware virtualization can be used to isolate different software stacks. d) How much software isolation does cost? Will this cost overshadow the benefits? e) How to make sure the code running on the CSD is legit? Not just at boot, but also during runtime?

3.3 Data Consistency

When data is read and written by multiple parties, consistency problems may arise. For example, the same block of data can be concurrently read by the host CPU and the CSD's CPU, imagine the software running on one of these two modifies the block's content. After such modification, which is unilateral, each CPU will operate on different data – while assuming the data is the same. In fact, immediately after a CPU modifies the data, it should inform the other. The same issue applies not just to file content but also to file system meta-content. For example, the software running on the host CPU or on CSD's CPU creates a new file – the creation must be notified to the other CPU, but the same extends to almost all file system operations. Obviously, classic file systems for personal computer do not address such issues. Furthermore, common disk interfaces (e.g., SATA, SAS, NVMe) are not prepared to manage such situations as well — interfaces were built assuming disks controller strictly executes commands from the host CPU. Similarly, data maybe replicated or sharded among several disks. For consistency, modification on replicated or sharded data should happen in parallel – the same applies to erasure-code or parity blocks [13].

Finally, a single CSD, may fail during any operation, including obviously, in-storage data processing. Replication, sharding, and parity/erasure coding, may definitely be used to tolerate failures other than improve performance. Such techniques will likely be implemented atop CSDs. To support that CSD may implement additional features for example to communicate failures.

Questions. a) How to show the same file system to the host and CSD software? b) What about file system updates? How to update the software on the host about file modifications on the CSD? c) Is a new file system needed? Can classic file systems be extended to support that? Do distributed file systems solve this problem already? If yes, what about performance? d) How to extend current storage interfaces to provide notifications for data changed into the CSD? Are notifications needed at all? e) What about explicit transaction management? f) What about hardware and software failures? g) What if there is replication and a new file is added, how to deal with that? h) How CSDs communicate between each other for replication or any other operation that requires coordinated operations on multiple drives? i) Does communication need to go via the host CPU or should it go directly (e.g., via the P2P DMA/RDMA) – what is faster?

3.4 Usability

To widen adoption, usability is certainly of fundamental importance. CSDs should be easy and quick to program, deploy, and debug at any level of software (user-level or kernel-level).

Debugging applications running among a host CPU and a CSD's CPU shouldn't be a nightmare. For example, one of the most complicated steps after the development of a distributed software is the debugging – this is exactly because in those environments the programmer ends up having multiple debuggers, or log traces coming from different systems, that have to be synchronized to be useful and identify the source of the problem. Debugging in distributed systems may provide some hints.

A major matter is if a CSD should be considered as a totally independent computer node, or as a part of a computer node? We believe that it strongly depends on the available hardware resources – if the computational and memory resources are au pair to the one available to the host resources, users may be able to run the same workloads atop host and CSDs. However,

if the resources are not the same, CSDs should be considered as storage-side accelerators – thus, shouldn't run a full-fledged workload that should executed on the host CPU instead. Based on that, decision on what workload(s) to run on CSD may be taken by the software running on the host CPU or by a datacenter scheduler. However, in the latter case, a CSD should be reachable via network, which requires the CSD to be built with a network interface hardware, at an additional cost.

Questions. a) Other than programmability, how to easily deploy applications on CSDs? b) Can applications be mapped to storage devices transparently? (Without the application, nor the developer, requiring to know on what storage device to be run.) c) Basically, a resource manager is needed, but what information such resource manager needs from the application to make best placement decisions? d) How to design an API that minimizes application modifications and it is easy to use? A simple and POSIX-like API is enough for adoption?

4 Programming Model

Clearly, the programming models available to the programmer that wants to run his/her application among host and CSD processing units largely affect the way the questions in Section 3 will be answered. We believe that there is no "one-size-fit-all" programming model that work for all kinds of applications, and therefore a quantitative and qualitative evaluation of each model is sought. In this section, we discuss a few programming models, and describe for each how we envision the questions would be answered, which is summarized in Table 1.

4.1 Dataflow

Within the dataflow model (e.g., [31, 32]), a sequence of transformation operations is defined for each chunk of data in transit. A transformation operation receives a chunk of data in input, and outputs the transformed chunk of data. Where "data in transit" generically identifies blocks of data travelling between different hardware and software layers, including not only blocks of data transferred from flash chips to the CSD/host CPUs, but also blocks of data flowing through the different kernel's and applications' software layers.

When used with CSD. Mapping the dataflow programming model into a CSD environment is straightforward: for each storage command (i.e., disk block read or write), one or a set of transformation operations are associated, similarly to [19, 13, 40]. The communication between the host and the CSD's processing units could be handled by extending standard interfaces (e.g., SATA, NVMe). Extensions include new commands to download transformation operations, or modifications to the existent commands to exchange per-session or global data between host and CSD's CPUs.

The dataflow model handles well most of the four concerns listed in Section 3. The beauty of this programming model is that operations can be defined at a fine granularity and executed anywhere, simplifying resource management. Operations maybe moved back to host for load balancing or can be replicated if data is replicated, transparently. In addition, multiple operations can be merged, split, as well as parallelized. When parallelized, access to per-session or global data must be protected for consistency. For security, a method to associate data with users must be introduced. Finally, dataflow programs can be defined in any language, although a language that provides some sort of formal properties, such as termination and memory safety, is preferred.

Unfortunately, only a bunch of applications are implemented within this programming model, which requires program rewriting when an application was written within the message-passing or shared memory model. Therefore, research on compiler tools that automatically convert applications into dataflow is sought.

4.2 Client-Server

This includes applications developed and deployed within distributed systems, such as Message Passing Interface (MPI), Remote Procedure Call (RPC), MapReduce, etc. The only requirement for these applications is a network connection between multiple compute nodes – TCP/IP, UDP, or RDMA are the most common. Such applications are strictly partitioned in multiple programs, each of which runs on a different processing node.

When used with CSD. Applications developed with this programming model can be directly mapped into a CSD setup without any modification – assuming the application can run in the software environment provided by the CSD. This is achieved by establish a network channel between host and CSD CPUs, and/or amongst CSD CPUs [6]. However, native compiled applications may need to be recompiled to the instruction set architecture (ISA) of the CSD's CPU (such as ARM). Although not impossible, it may require an entire toolchain, and the recompilation of all libraries required by the program. Furthermore, as many of such distributed applications are based on a very large software base, involving many different libraries, which consumes a lot of memory as well as storage. Hence, running such applications on weak CPUs – the ones we expect to be available on CSDs, can hinder performance.

Moreover, with this model, the resource management granularity is at the program level – this is because only programs can be moved between CPUs (assuming the same program is available for all CPU ISAs present in the system). Algorithms are embedded in the different programs building the application; thus, the resource manager cannot act at more fine grain for optimizations.

Security is provided at the application level, which can be eventually embedded in a container (OS-level virtualization). Standard OS techniques can be used to enable CSD's application to only access data belonging to a specific user.

4.3 Shared Memory

The shared memory programming model is widely adopted on multicore processors. It requires a form of (consistent) shared memory between processing units. When hardware shared memory is not available, software shared memory, or distributed (virtual) shared memory (DSM), may be used [20, 33] . Another assumption of the shared memory programming model is that all CPUs are identical, or at least implement the same ISA.

When used with CSD. CSD's CPU and host CPU may not have the same ISA. In fact, many of the existent deployments are characterized by x86 CPUs on the host and ARM CPUs on the CSD. Academic projects, such as Popcorn Linux [22, 18] and H-Container [17], enable applications developed for shared memory multicore to run on heterogeneous ISA cores, transparently – without any application modification. This includes starting an application on the host CPU and then migrating all its threads to a CSD, and the contrary.

In this model, resource management can be potentially done at the finest grain of an assembly instruction. In that way, the computation can swing between host CPU and CSD's CPU at any time, based for example on the compute-intensiveness and where the data is.

The issue with this programming model is that when hardware shared memory is not available, it should be provided by software, which may be expensive. However, future PCIe advancements may offer consistent shared memory among a

	Resource Management	Security	Consistency	Usability
Dataflow	Automatic, very efficient	Very good, with low overhead	Controlled by resource manager	Application dependent
Message-passing	Quite inefficient	Program-level	Must be handled by the programmer	Very good (just reuse apps, or at most recompile)
Shared memory	Automatic, very efficient	Thread/program-level (but also basic block)	Transparent Software consistency, maybe expensive	Very good (just reuse apps) but needs special system software

Table 1: A qualitative summary and comparison of programming models vs. research questions described in Section 3.

device's CPU on PCIe and the host CPU [2, 3, 4]. In addition, the shared memory programming model also needs to take care about the consistency problem, and computation cannot be parallelized or optimized from the external resource manager. Finally, security can be achieved via the mechanisms available in classic operating systems, but further research needs to be done.

5 Storage Interface

The most widely adopted storage interfaces are block-based, file-based, and object-based. We purposely tried to refer to none of those along the paper when possible. This is because we believe our findings applies to any of them. Herein, we review the hardware and software implications of each programming model. We believe an hardware- or software-only approach is not sufficient.

5.1 Hardware Interface

The dataflow programming model requires limited storage interface modifications. As discussed in Section 4.1, a transformation operation should just be assigned to a dataflow, and for each data block of the dataflow the operation will be called. Therefore, the minimal requirement to today's storage interfaces, such as NVMe, is to provide additional commands to: 1) download a program; 2) attach/detach a program to a dataflow; 3) define a dataflow; 4) debugging/logging. All such commands can simply extend the existent NVMe protocol/interface, will supporting legacy software. Note that with this interface, developers don't care about what software is running on the CSD's CPU(s), e.g., it can be Linux, or it can be a firmware.

Server-client programming models may also require limited storage interface modifications. As described in Section 4.2, only a message-passing channel to emulate network communication is necessary – which can be implemented with sending and receiving queues (similarly to RDMA, NVMe, etc). Such extension may extend the NVMe protocol/interface by adding a new command set to it, which includes commands for communication but also to download code to the CSD (Linux), and boot, log, debug the software.

The shared memory programming model (Section 4.3) is perse the one that demands more changes to the current storage interfaces when a performant implementation is needed, i.e., no software DSM overheads. If that is not needed, the same interface modifications required by the client-server programming model are demanded. Such modifications are enough to implement software DSM. Instead, when a performant implementation is needed, a sort of hardware shared memory should be available among the host CPU(s) and the CSD's CPU(s), for example provided by new coherent peripheral bus interconnects [2, 3, 4]. Hardware shared memory does not have to be consistent – the consistency can be provided via software.

5.2 Software Interface

An application written within the dataflow programming model doesn't require any specific software interface – in fact, programs declare the input source as well as the output source that maybe streams of data from or to storage media. The application developer is not directly exposed to any CSD-specific hardware interface, a runtime system shields the programmer from these technicalities.

When an application is written instead within the server-client or shared memory programming model, it is expected to directly interface with the flash array when executing on a CSD. Note that this necessary for performance. Hence, a software interface to access the flash array should be defined. A naïve solution is to abstract each different flash array's channel with a UNIX device. Thus, each user may be assigned with a different channel. Despite a practical solution, because it maps quite well with the underlying hardware, and can be used for protection/isolation, it is highly unlikely that different users are assigned with different NAND channels for performance reasons – this is because writing and reading several channels in parallel gives high performance.

Moreover, (if we don't consider KV-SSD technologies) an user accesses data on storage via files. Files are a file system abstraction, usually provided by the host operating system, which is not necessary known on the SSD. Therefore, a more fine-grain solution is needed for protecting/isolating the data of different users, that requires another abstraction for the programmer. The concept of stream, such as a list of (non-sequential) flash blocks could be a solution, but existent hardware doesn't provide any related mechanism.

On the host side, the same CS hardware interface should be usable by software at the user- and kernel-level. This is to support traditional file system in kernel-space as well as modern storage software in user-space (e.g., SPDK). A "symmetric" kernel/user interface is needed.

Finally, in order to support situations when the code cannot be moved to the CSD, and therefore it should run on the host operating system, a symmetric software interface should be implementable on the host machine and on the CSD.

6 Concluding Remarks

In this paper, we briefly survey the state of the art of computational storage and we raised several open challenges that might need to be considered to facilitate the adoption of the computational storage technology in both research and industry communities – existent computational storage hardware and software are not ready to be used in production at scale. We then discussed how the most widely-used programming models with hardware/software interfaces can help solving such challenges. We believe that our discussions and lessons presented in this paper can provide a higher degree of clarity about what's likely to be needed

for the mass adoption of the computational storage technology.

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