PES University, Bengaluru

(Established under Karnataka Act 16 of 2013)

END SEMESTER ASSESSMENT (ESA) - May 2023

UE19EC302 - Digital VLSI Design

Total Marks : 100.0

1.a. Draw the following
i) VLSI design flow in three domains (Y-chart representation) and also the simplified VLSI Design Flow.
ii) Circuit diagram of the BiCMOS NOR2 gate and BiCMOS NAND2 gate. (10.0 Marks)

1.b. Draw the CMOS inverter circuit diagram with voltage transfer characteristics curve and mention the operating conditions for the load and the driver in all five regions. (10.0 Marks)

2.a. Briefly explain the various steps involved in n-well CMOS fabrication process with the help of cross- sectional schematic. (10.0 Marks)

2.b. i)Distinguish Buried and Butting contact cuts in nMOS circuits with suitable diagrams.
ii)Draw the circuit diagram, monochrome stick diagram and mask layout for the two input CMOS NAND gate. (10.0 Marks)

3.a. i)Define Scaling of MOS Circuits and mention the different scaling models.

ii)An interconnect line runs over an insulating oxide layer that is 1000 Å thick. The line has a width of 0.5μm and is 40μm long. The sheet resistance is known to be 25Ω
a) Find the line resistance R_{line}
b) Find the line capacitance C_{line}. Use Ɛox = 3.453 x 10^{-13} F/cm and express the answer in femtofarads (fF) where 1 fF = 10^{-15} F.
c) Find the time constant t for the line in units of picoseconds (ps) where 1 ps= 10^{-12} sec. (10.0 Marks)

3.b. Calculate the inverter pair delay for the following with a relevant circuit diagram.
i) NMOS
ii) CMOS (10.0 Marks)

4.a. Implement the following function using CMOS Transmission gate?
i) XOR gate
ii) 4:1 MUX (10.0 Marks)

4.b. i)Dynamic CMOS logic circuits cannot be cascaded . Justify the statement
ii)With the help of a neat diagram, explain in brief an 8-bit carry -select adder.
(10.0 Marks)

5.a. Explain in detail time borrowing in latch based sequencing systems.
(10.0 Marks)

5.b. With a neat diagram, explain
i) Resistive load SRAM
ii) 1T DRAM Cell. (10.0 Marks)