PES University, Bengaluru

(Established under Karnataka Act 16 of 2013)

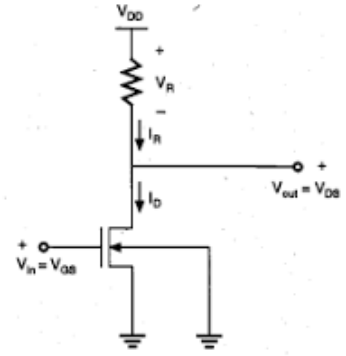
END SEMESTER ASSESSMENT (ESA) - May 2023

UE21EC251B - Digital VLSI Design

Total Marks : 100.0

1.a. With the help of voltage transfer characteristics indicating different regions of operation explain CMOS inverter and derive the equation for V_{TH} inverter threshold voltage of the same (8.0 Marks)

1.b. Consider the resistive load inverter with the following specifications



Resistive-load inverter circuit.

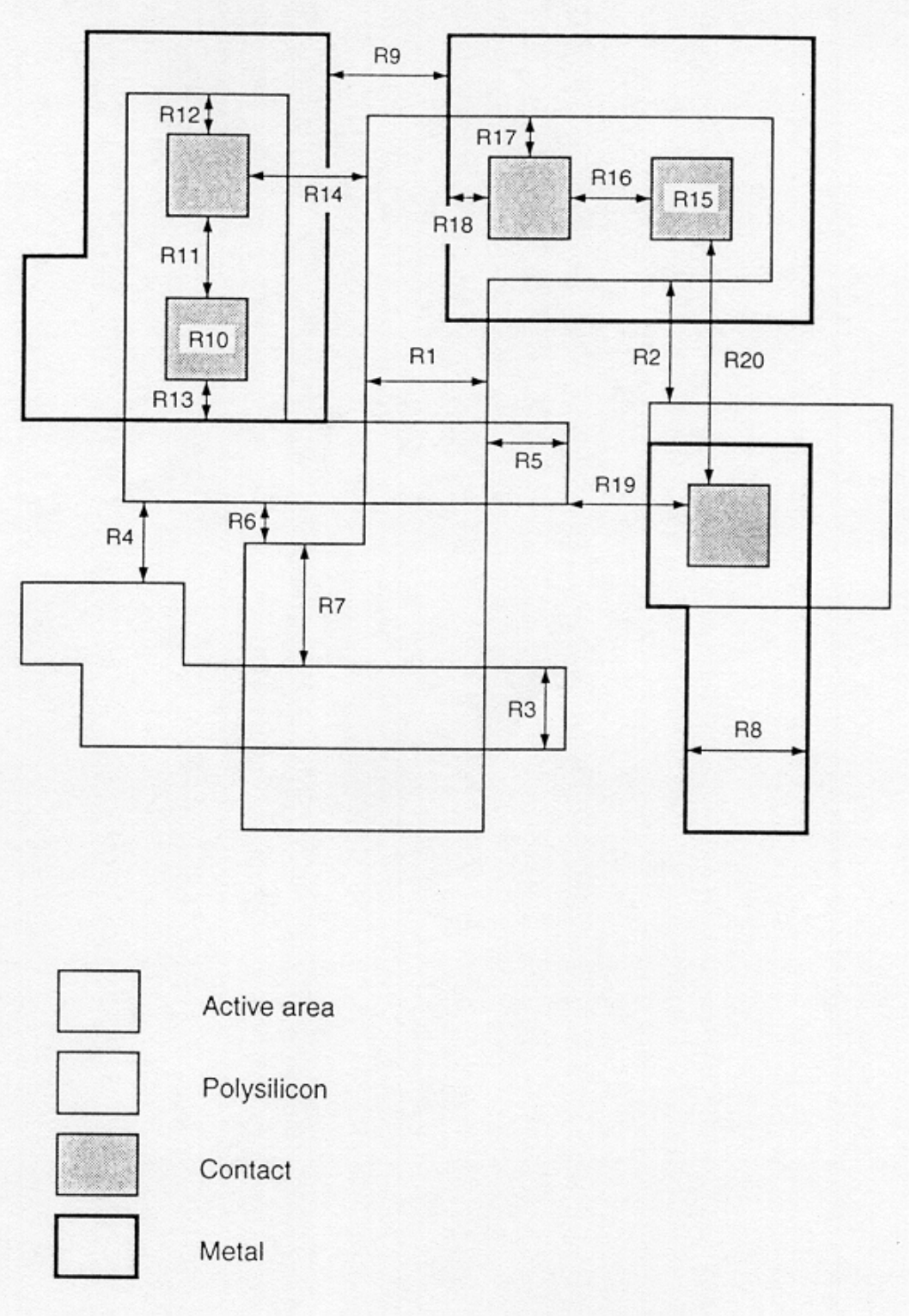
VDD=5V
Kn'=30uA/V2
VT0=1V
RL=200Kohm
Calculate the aspect ratio of driver MOSFET if PDC(average) =60uW
also calcualte NML and NMH of the circuit (8.0 Marks)

1.c. in a depletion load NMOS inverter what is the operating region of driver and load MOSFET in the following case of inverter operation
i. When Vin=VOH and Vout= VOL
ii. When Vin=VOL and Vout=VOH (4.0 Marks)

2.a. In the following figure write the description and its corresponding lambda rule values for following rules

R4
R10
R14
R20

(4.0 Marks)



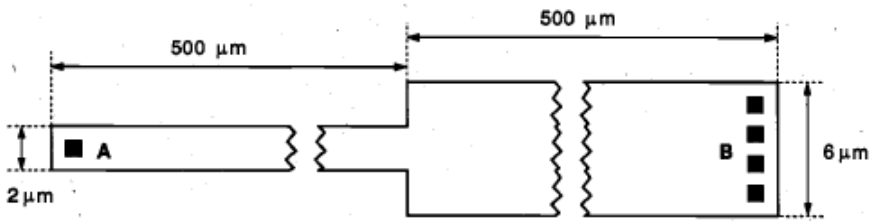
2.b. With the help of relavent diagrams explain the process flow of NMOS fabrication process (8.0 Marks)

2.c. Write the schematic diagram of the following boolean equation
$Y = ((A + B)(C + D)E)'$
Write the layout of the same by justifying its Eulers path (8.0 Marks)

3.a. Derive the equation of ς_{PHL} High to Low delay of CMOS inverter using differential equation method (8.0 Marks)

3.b. Derive the expression for switching power dissipation of CMOS inverter (6.0 Marks)

3.c.



Poly over field oxide	C_{pf}	Area	0.066	fF / µm^2
		Perimeter	0.046	fF / µm
Metal - 1 over field oxide	C_{m1f}	Area	0.030	fF / µm^2
		Perimeter	0.044	fF / µm
Metal - 2 over field oxide	C_{m2f}	Area	0.016	fF / µm^2
		Perimeter	0.042	fF / µm
Metal - 1 over Poly	C_{m1p}	Area	0.053	fF / µm^2
		Perimeter	0.051	fF / µm
Metal - 2 over Poly	C_{m2p}	Area	0.021	fF / µm^2
		Perimeter	0.045	fF / µm
Metal - 2 over Metal - 1	C_{m2m1}	Area	0.035	fF / µm^2
		Perimeter	0.051	fF / µm

calculate Lumped delay of ploysilicon interconnect line from A to B if sheet resistance is 30Ω/square (6.0 Marks)

4.a. With the help of gate level and schematic diagram explain CMOS AOI based JK latch also write its truth table and timing diagram (6.0 Marks)

4.b. Derive the expression for transit time constant for CMOS bistable element (8.0 Marks)

4.c. use the following parameters in the table

	Setup time	Clk-Q delay	D to Q delay	Contamination delay	Hold time
Flipflop	65ps	50ps	na	35ps	30ps
Latches	25ps	50ps	40ps	35ps	30ps

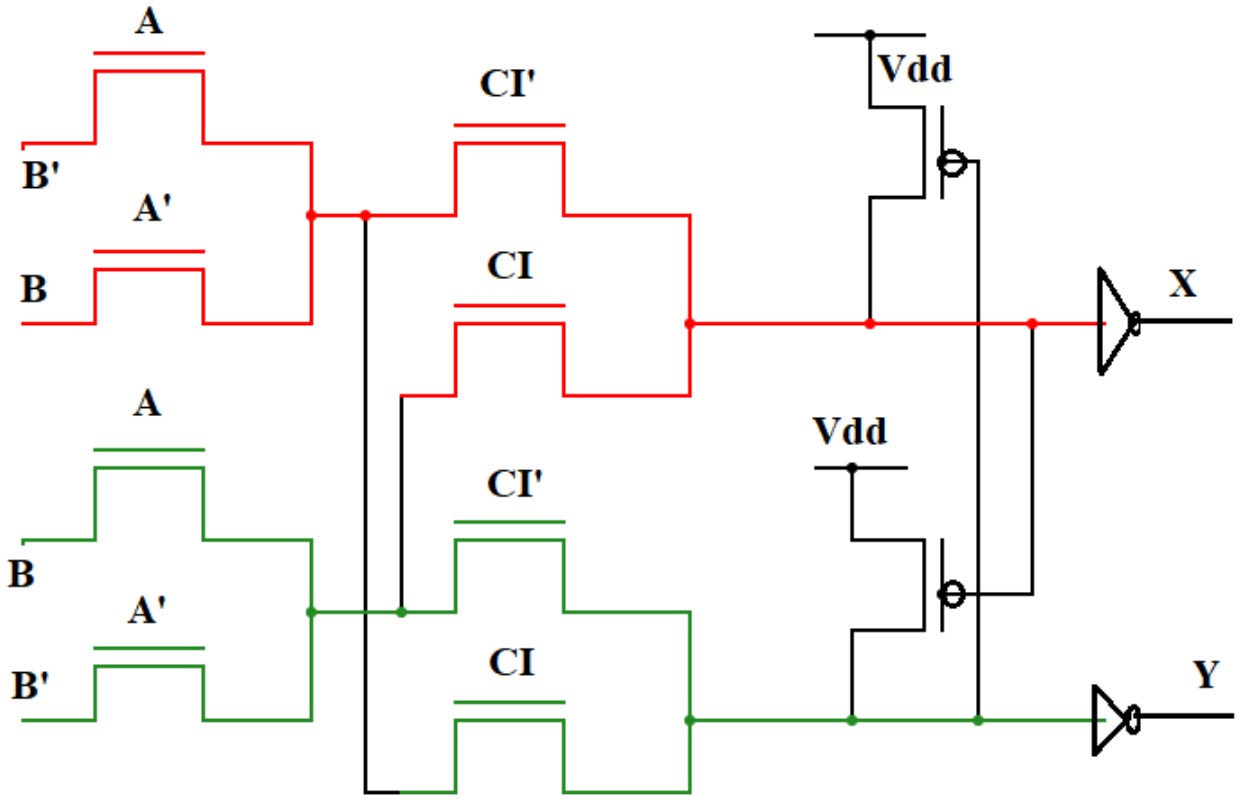
For each of the following sequencing styles maximum logic propagation delay available with in 500ps clock cycle assume clock skew and time borrowing is=0

a) Flipflops
b) Two phase transperant latches
c) pulsed latches with 80ps pulse width (6.0 Marks)

5.a. WIth the help of schematic expalin domino logic describe the drawback of the same and show that how a weak pull up helps to overcome the same (8.0 Marks)

5.b. Describe the operation of write logic 0 in 6T SRAM with design equation (8.0 Marks)

5.c. Give the logical expression for output variable X and Y where A B and CI are inputs to the system



(4.0 Marks)