PES University, Bengaluru

(Established under Karnataka Act 16 of 2013)

END SEMESTER ASSESSMENT (ESA) - JULY - 2023

UE21EC251B - Digital VLSI Design

Total Marks : 100.0

1.a. With the help of CMOS inverter VTC indicationg regions of operation and derive the expression of VIL, VIH, VOH and VOL (10.0 Marks)

1.b. For two input NAND write the schematic using BICMOS logic structure (6.0 Marks)

1.c. Consider a resistive load inverter circuit with VDD=5V Kn'=20uA/V2 Vto=0.8V RL=200Kohm W/L=2 calculate the critical voltages VoL VoH (4.0 Marks)

2.a. Write the processing steps for fabricating n-type MOS transistor (10.0 Marks)

2.b. Write the schematic and layout diagram two input NOR gate (10.0 Marks)

3.a. (10.0 Marks)

A company in Urbana, IL called Prairie Technology has access to a CMOS fabrication process with the device parameters listed below.

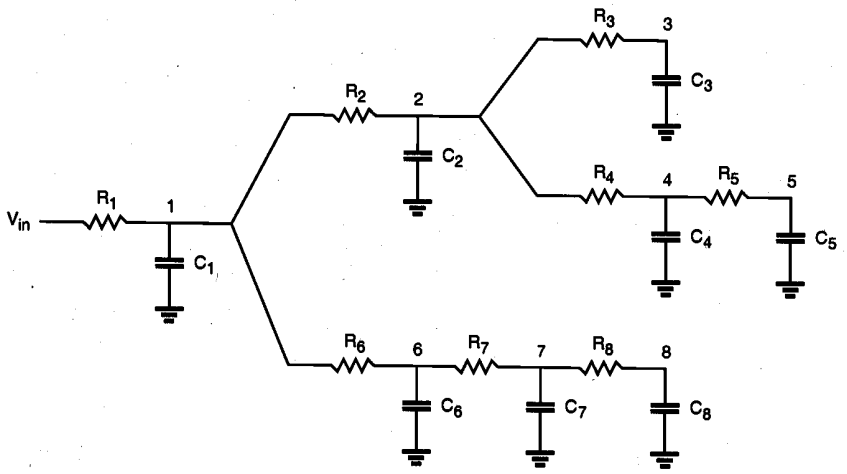
$\mu_n C_{ox} = 120\ \mu A/V^2$
$\mu_p C_{ox} = 60\ \mu A/V^2$
$L = 0.6\ \mu m$ for both nMOS and pMOS devices
$V_{T0,n} = 0.8\ V$
$V_{T0,p} = -1.0\ V$
$W_{min} = 1.2\ \mu m$

Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the following performance specifications.

- $V_{th} = 1.5$ V for $V_{DD} = 3$ V,
- Propagation delay times $\tau^*_{PHL} \leq 0.2$ ns and $\tau^*_{PLH} \leq 0.15$ ns,
- A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V, assuming a combined output load capacitance of 300fF and ideal step input.

3.b. With the help of schematic, waveforms and design equation explain CMOS ring oscillator (6.0 Marks)

3.c.



Calculate Elmore delay at node 7 (4.0 Marks)

4.a. With the help of schematic diagram explain CMOS implementation of D-latch (7.0 Marks)

4.b. Write the transistor schematic of AOI-based implementation of the clocked NOR-based SR latch circuit. (5.0 Marks)

4.c. with the help of block and timing diagrams explain the following sequencing methods for MAX delay constraints
i. FF
ii Two phase latches
iii Pulsed latches (8.0 Marks)

5.a. Use transmission gate and write the schematic of the following expression
i 2:1 mux
ii 6T implementation of 2 input XOR gate
iii. F=AB+A'C'+AB'C (10.0 Marks)

5.b. Explain the working of FULL CMOS 6T SRAM and explain the read0 operation and its design stratagy (10.0 Marks)