PES University, Bengaluru

(Established under Karnataka Act 16 of 2013)

END SEMESTER ASSESSMENT (ESA) - DEC 2023

UE19EC302 - Digital VLSI Design

Total Marks : 100.0

1.a. Draw the VLSI design flow in three domains (Y-chart representation) and also the simplified VLSI Design Flow. (10.0 Marks)

1.b. Draw the CMOS inverter circuit diagram with voltage transfer characteristics curve and mention the operating conditions for the load and the driver in all five regions. (10.0 Marks)

2.a. Briefly explain the various steps involved in n-well CMOS fabrication process with the help of cross- sectional schematic. (10.0 Marks)

2.b. Draw the circuit diagram, monochrome stick diagram and mask layout for the two input CMOS NAND gate. (10.0 Marks)

3.a. Calculate the inverter pair delay for the following with a relevant circuit diagram.
i) NMOS
ii) CMOS (10.0 Marks)

3.b. Define Scaling of MOS Circuits and mention the different scaling models. Obtain the scaling
factors (for all the models) for the following device parameters
i) Saturation current, Idss
ii) Current Density, J (10.0 Marks)

4.a. Dynamic CMOS logic circuits cannot be cascaded . Justify the statement (10.0 Marks)

4.b. Implement the following function using CMOS Transmission gate?
i) XOR gate
ii) 4:1 MUX (10.0 Marks)

5.a. With a neat diagram, explain Resistive load SRAM Cell. (10.0 Marks)

5.b. Explain in detail time borrowing in latch based sequencing systems.
(10.0 Marks)