PES University, Bengaluru

(Established under Karnataka Act 16 of 2013)

END SEMESTER ASSESSMENT (ESA) - Jan - May 2024

UE22EC251B - Digital VLSI Design

Total Marks : 100.0

1.a. Derive the expression for critical voltages V_{IH} and V_{IL} of CMOS inverter.

(8.0 Marks)

1.b. Design a resistive load inverter with R_L = 1K ohm, such that V_{OL} = 0.6V. The enhancement-type nMOS driver transistor has the following parameters

$V_{DD} = 5.0\ V$
$V_{T0} = 1.0\ V$
$\gamma = 0.2\ V^{1/2}$
$\lambda = 0$
$\mu_n C_{ox} = 22.0\ \mu A/V^2$

1. Determine the required aspect ratio, W/L
2. Determine V_{IL} and V_{IH}.
3. Determine noise margins NML and NMH

(7.0 Marks)

1.c. Draw the circuit diagram of the given expression using nMOS and BiCMOS design.

$Y = \overline{(A + D)(B + C)}$

(4.0 Marks)

1.d. Draw the circuit diagram of the depletion load nMOS inverter. Also mention the region of operation of the load and driver transistor of the depletion load nMOS inverter when input is 0, V_{IL}, V_{TH}, and V_{DD} (6.0 Marks)

2.a. With a relevant diagram, explain the steps involved in the nMOS fabrication process (9.0 Marks)

2.b. Draw a circuit diagram and Layout using the Euler path method for the given expression (Use CMOS design).

(6.0 Marks)

$$Z = \overline{A(D+E)+BC}$$

2.c. NMOS transistor is fabricated using 1µm technology with the following device parameters. W = 2L, V_{DD} = 5V, I_{Dsat} = 4mA, V_{th} = 0.4V, and $N_A = 10^{17}$cm-3. What will be the scaling factor if the same transistor is scaled down to 0.5µm technology? Find the scaled values of the following device parameters for both full scaling and constant voltage scaling models

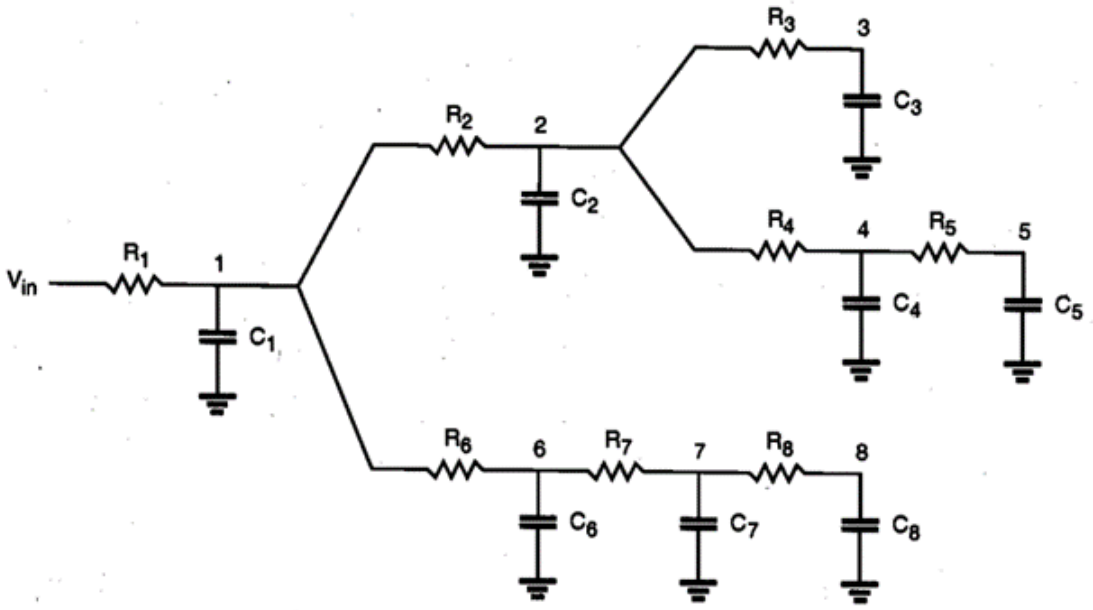
1. Channel Width
2. Channel Length
3. Threshold voltage
4. Doping density (N_A)

(5.0 Marks)

2.d. Draw the circuit diagram 1-bit full adder using a mirror CMOS circuit. Write the sum and carry out the expression for the same. (5.0 Marks)

3.a. Write the Elmore delay expression at node 4 and node 6 for the given RC tree

(4.0 Marks)



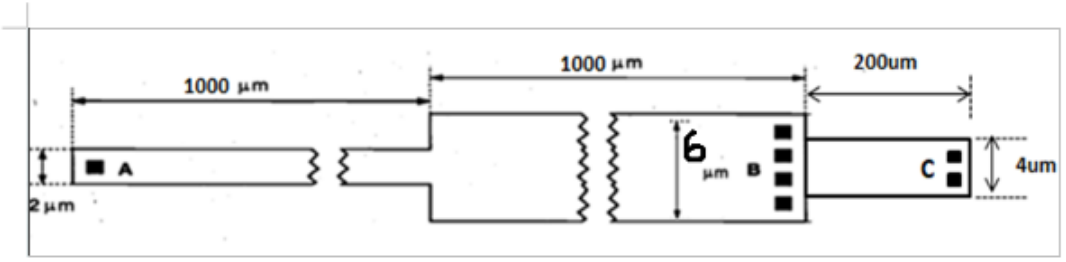
3.b. Derive the τ_{PHL} delay time of the CMOS inverter with an ideal step input pulse as an input voltage. (8.0 Marks)

3.c. An Interconnect path of Metal2 over Metal1 using 0.8um technology is shown below. The sheet resistance of Metal2 is 15 ohm / sq, assuming a step input pulse, calculate the value of R_{lumped}, parallel plate capacitance, fringing capacitance, and t_{PHL} of the interconnect line for the following model.

1. Lumped RC network
2. Distributed RC ladder network, consisting of 10 identical segments

Refer to the given table for Parasitic capacitance values

Poly over field oxide	C_{pf}	Area	0.066	fF / µm^2
		Perimeter	0.046	fF / µm
Metal - 1 over field oxide	C_{m1f}	Area	0.030	fF / µm^2
		Perimeter	0.044	fF / µm
Metal - 2 over field oxide	C_{m2f}	Area	0.016	fF / µm^2
		Perimeter	0.042	fF / µm
Metal - 1 over Poly	C_{m1p}	Area	0.053	fF / µm^2
		Perimeter	0.051	fF / µm
Metal - 2 over Poly	C_{m2p}	Area	0.021	fF / µm^2
		Perimeter	0.045	fF / µm
Metal - 2 over Metal - 1	C_{m2m1}	Area	0.035	fF / µm^2
		Perimeter	0.051	fF / µm



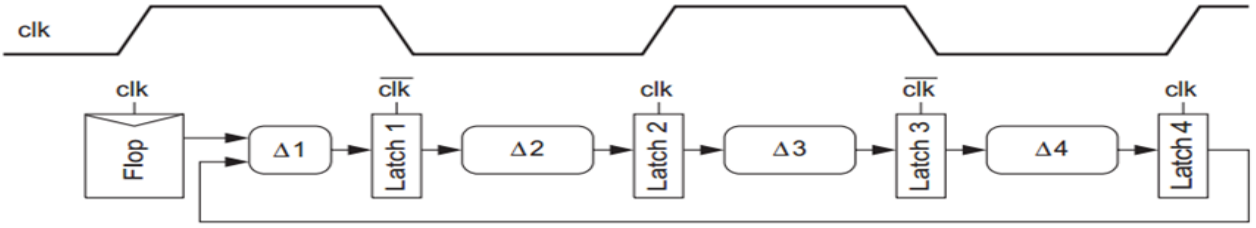
(6.0 Marks)

3.d. Explain the working of the NOR version clocked SR latch with the help of a circuit diagram (using MOSFET) and timing waveforms (7.0 Marks)

4.a. What is max-delay failure? With the relevant block diagram, equations, and timing diagram, explain how flip-flop-based sequencing methods can avoid setup time failure. (7.0 Marks)

4.b. Determine the amount of time borrowed by each latch for the path shown in the figure below, and whether any latches violate the setup time for a cycle time of 1000ps. Assume there is no clock skew and the propagation delay includes latch delays.

$\Delta 1 = 550$ ps; $\Delta 2 = 580$ ps; $\Delta 3 = 450$ ps; $\Delta 4 = 200$ ps



(5.0 Marks)

4.c. Explain the Read '0' operation and obtain the design strategy in 6T SRAM cell (7.0 Marks)

4.d. Explain the working principle of CMOS dynamic logic. (6.0 Marks)