PES University, Bengaluru

(Established under Karnataka Act 16 of 2013)

END SEMESTER ASSESSMENT (ESA) - DEC 2023

UE21EC251B - Digital VLSI Design

Total Marks : 100.0

1.a. Derive the expression for critical voltages in CMOS inverter along with Voltage transfer charactaristics (10.0 Marks)

1.b. Write the transistor level schmatic for the expression Y=A(B+C) (10.0 Marks)

2.a. With the neat labelled diagram explain the nMOS fabrication process (10.0 Marks)

2.b. Draw the schematic and layout of 3 input AND gate (10.0 Marks)

(10.0 Marks)

3.a.

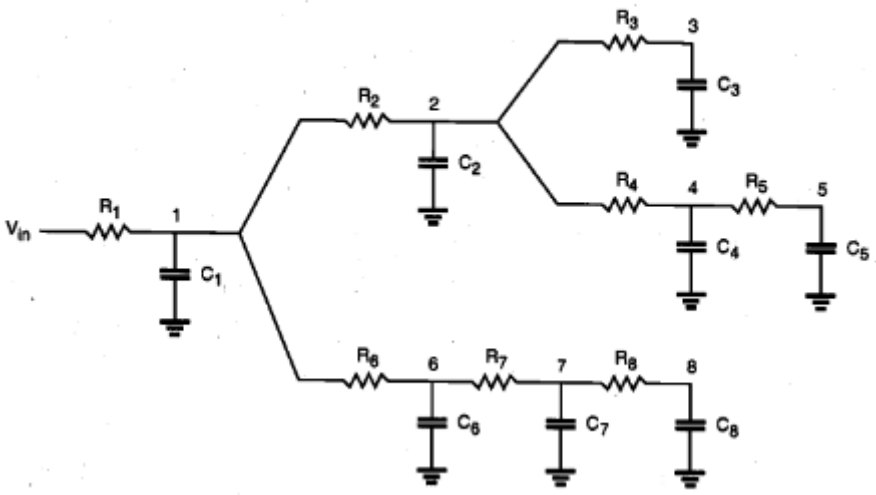
A company in Urbana, IL called Prairie Technology has access to a CMOS fabrication process with the device parameters listed below.

$\mu_n C_{ox} = 120\ \mu A/V^2$
$\mu_p C_{ox} = 60\ \mu A/V^2$
$L = 0.6\ \mu m$ for both nMOS and pMOS devices
$V_{T0,n} = 0.8\ V$
$V_{T0,p} = -1.0\ V$
$W_{min} = 1.2\ \mu m$

Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the following performance specifications.

- $V_{th} = 1.5$ V for $V_{DD} = 3$ V,
- Propagation delay times $\tau^*_{PHL} \leq 0.2$ ns and $\tau^*_{PLH} \leq 0.15$ ns,
- A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V, assuming a combined output load capacitance of 300fF and ideal step input.

3.b.



Calculate Elmore delay at node 5 (6.0 Marks)

3.c. Draw the circuit and explain ring oscillator (4.0 Marks)

4.a. With the help of block and timing diagram explain the following sequencing methods
FF
Two phase latch
pulsed latches (10.0 Marks)

4.b. Write the transistor level schematic of the following sequential circuit (10.0 Marks)

5.a.

5.a. Use transmission gate and write the schematic of the following expression
i 2:1 mux
ii 6T implementation of 2 input XOR gate
iii. F=AB+A'C'+AB'C

(10.0 Marks)

5.b. Explain the working of 6TSRAM (10.0 Marks)