

Prachi Deodatta Gore

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TECHNICAL SKILLS

Languages: SystemVerilog, HTML, CSS, Python, C

Developer Tools: Cadence Virtuoso, Vivado, Matlab, VS Code, Git

ACHIEVEMENTS

PIL The Hunt '24 - Won 6th place out of 250+ students (CTF competition)

Infeynite 2024 - honorable mention

PIL The Hunt '25 - Won 9th place out of 270+ students

PROJECTS

Functional Verification of PicoRV32 RISC-V Core | *SystemVerilog, Functional Coverage*

January 2026

- * Developed layered functional verification environment for PicoRV32 RV32I processor in SystemVerilog
- * Achieved 93.3% RV32I instruction coverage using automated functional and code coverage analysis
- * Implemented constrained-random stimulus, monitors, scoreboard, and coverage-driven verification flow
- * Validated arithmetic, logical, control-flow, and memory instructions against ISA specification

ChipOS | *C, RISC-V Assembly, QEMU*

March 2025

- * Built bare-metal RISC-V operating system with custom bootloader, interrupts, and microkernel design
- * Implemented interactive shell, dual text editors (VIM-style), and custom filesystem
- * Designed memory management and process abstractions enabling full OS functionality

RV32IM Processor Core | *SystemVerilog, Vivado, Artix-7*

October 2025

- * Designed single-cycle RISC-V RV32IM processor core from scratch in SystemVerilog
- * Implemented full M-extension including MUL/DIV variants
- * Verified functionality using directed testbench covering RV32I and M instructions

Ampiear – Digital Hearing Aid | *Python, DSP*

December 2025

- * Designed 7-stage DSP pipeline with STFT-based filter bank and Wiener noise reduction
- * Implemented WDRc compression and NAL-NL2 gain prescription for hearing loss compensations

COURSEWORK

2nd year: Computer Aided Digital Design, Analog Circuit Design, Network Analysis and Synthesis, Digital Signal Processing, Digital VLSI Design, Control Systems, Linear Algebra and Applications

5th Sem: Embedded Systems, Functional and Formal Verification of Digital Designs, Computer Communication Networks, Computer Organization and Design, Digital Communication

Currently enrolled (6th Sem): High Performance Computing, Cryptography, VLSI Circuit Testing and Testability, Transmission Lines, Waveguides and Antennas, Machine Learning and Applications

Attended Standard Cell Workshop: Synthesized a half adder using customized standard cells in 180nm technology

Attended SoC Design Workshop: gained knowledge about various SoC components, peripheral interfaces, and memory organization

EDUCATION

PES University

Bangalore, India

Bachelor of Technology in Electronics and Communication, CGPA - 7.61/10.00

2023 – 2027

Primus Public School

Bangalore, India

Higher Secondary School Certificate - 89%

2020 – 2023

The Amaatra Academy

Bangalore, India

Secondary School Certificate - 94%

2020