

模拟与数字电路

Analog and Digital Circuits



课程主页 扫一扫

实验课: vivado 安装与组合逻辑电路实验

Experiment Course: Install Vivado and Combinational Logic Circuit Experiment

主讲: 焦博

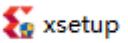
Instructor: Bo Jiao

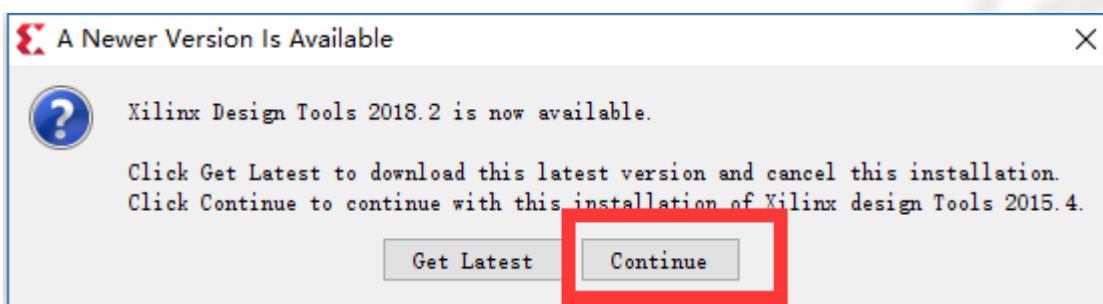
提纲

- vivado安装
- Verilog HDL 简单回顾
- 实验简单说明
- 新建工程
- 仿真并查看结果

Vivado 安装

首先打开文件：Xilinx_Vivado_SDK_xxx

点击  xsetup





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Select Edition to Install

Select an edition to continue installation. You will be able to customize the content in the next page.

Vivado HL WebPACK

Vivado HL WebPACK is the no cost, device limited version of Vivado HL Design Edition.

Vivado HL Design Edition

Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

Vivado HL System Edition

Vivado HL System Edition is a superset of Vivado HL Design Edition with the addition of System Generator for DSP. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

Documentation Navigator (Standalone)

Xilinx Documentation Navigator (DocNav) provides access to Xilinx technical documentation both on the Web and on the Desktop. This is a standalone installation without Vivado Design Suite.

Vivado 2015.4 Installer - Vivado HL Design Edition



Vivado HL Design Edition

Customize your installation by (de)selecting items in the tree below. Moving cursor over selections below provide additional information.

Vivado HL Design Edition includes the full complement of Vivado Design Suite tools for design, including C-based design with Vivado High-Level Synthesis, implementation, verification and device programming. Complete device support, cable drivers and Documentation Navigator are included. Users can optionally add the Software Development Kit to this installation.

- Design Tools
 - Vivado Design Suite
 - Software Development Kit
 - Documentation
- Devices
 - SoCs
 - Zynq-7000
 - Zynq UltraScale+ MPSoC
 - 7 Series
 - UltraScale
 - UltraScale+
- Installation Options
 - Install Cable Drivers
 - Acquire or Manage a License Key
 - Enable WebTalk for Vivado to send usage statistics to Xilinx (Always enabled for WebPACK license)
 - Install WinPcap for Ethernet Hardware Co-simulation
 - Launch configuration manager to associate System Generator for DSP with MATLAB
 - Enable WebTalk for SDK to send usage statistics to Xilinx

Device 型号决定安装包大小，建议按需安装

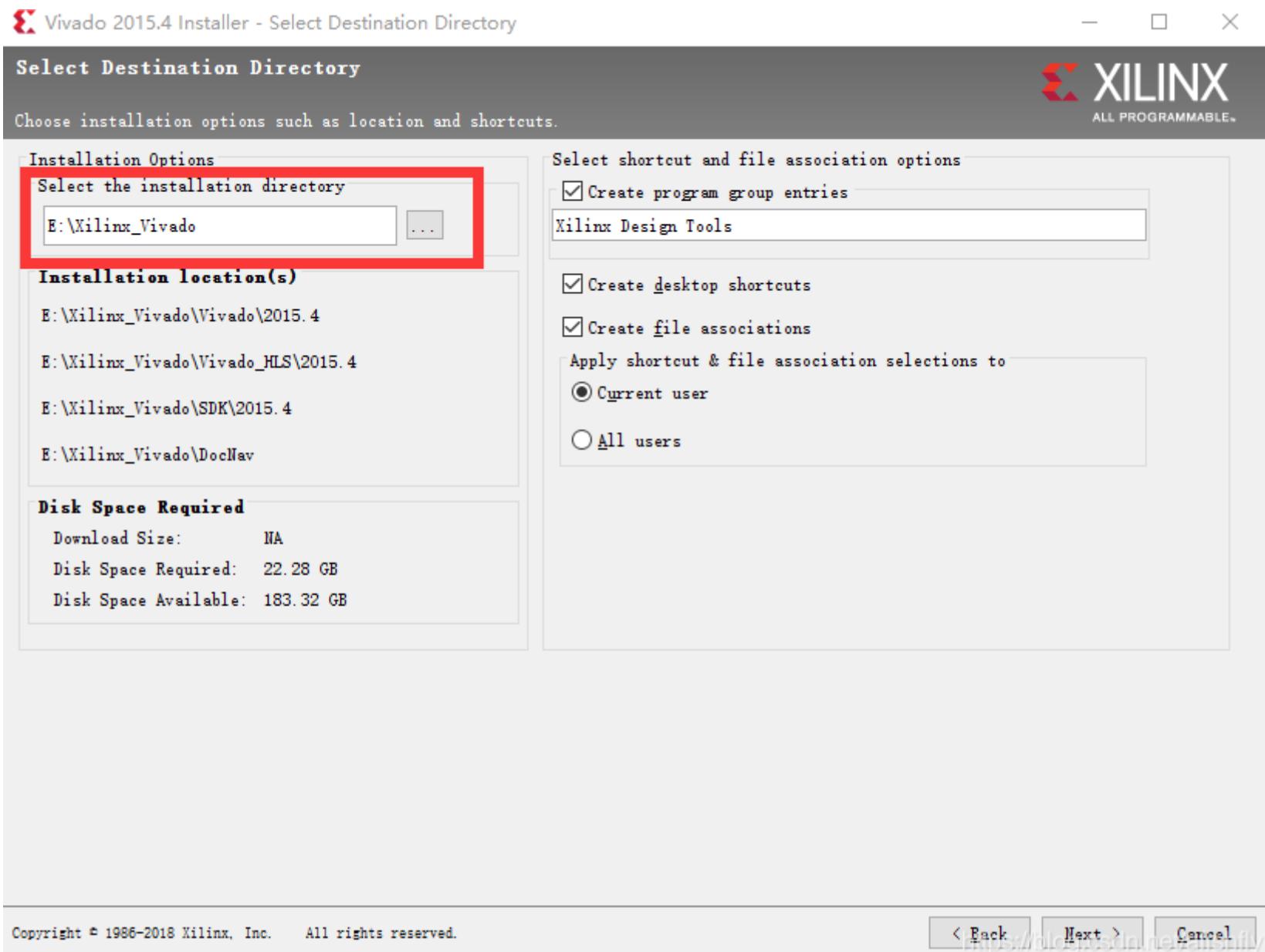
Download Size: NA
Disk Space Required: 22.28 GB

[Reset to Defaults](#)

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[< Back](#) [Next >](#) [Cancel](#)

可更改安装路径

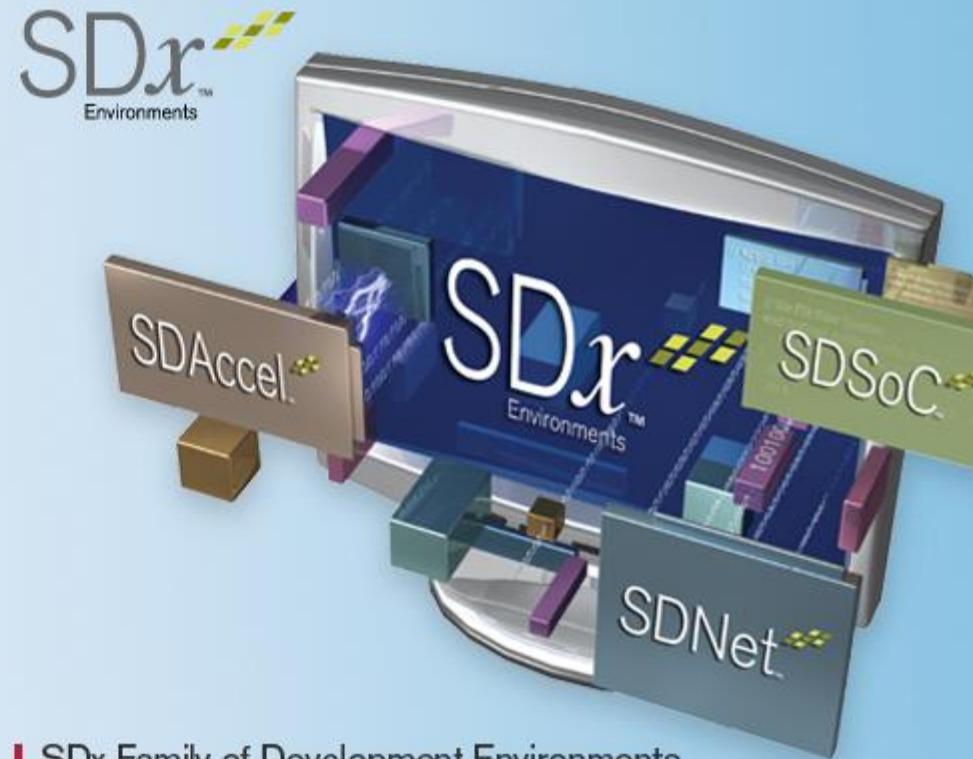


Installation Progress

Installing files, 0% completed.

Final Processing...

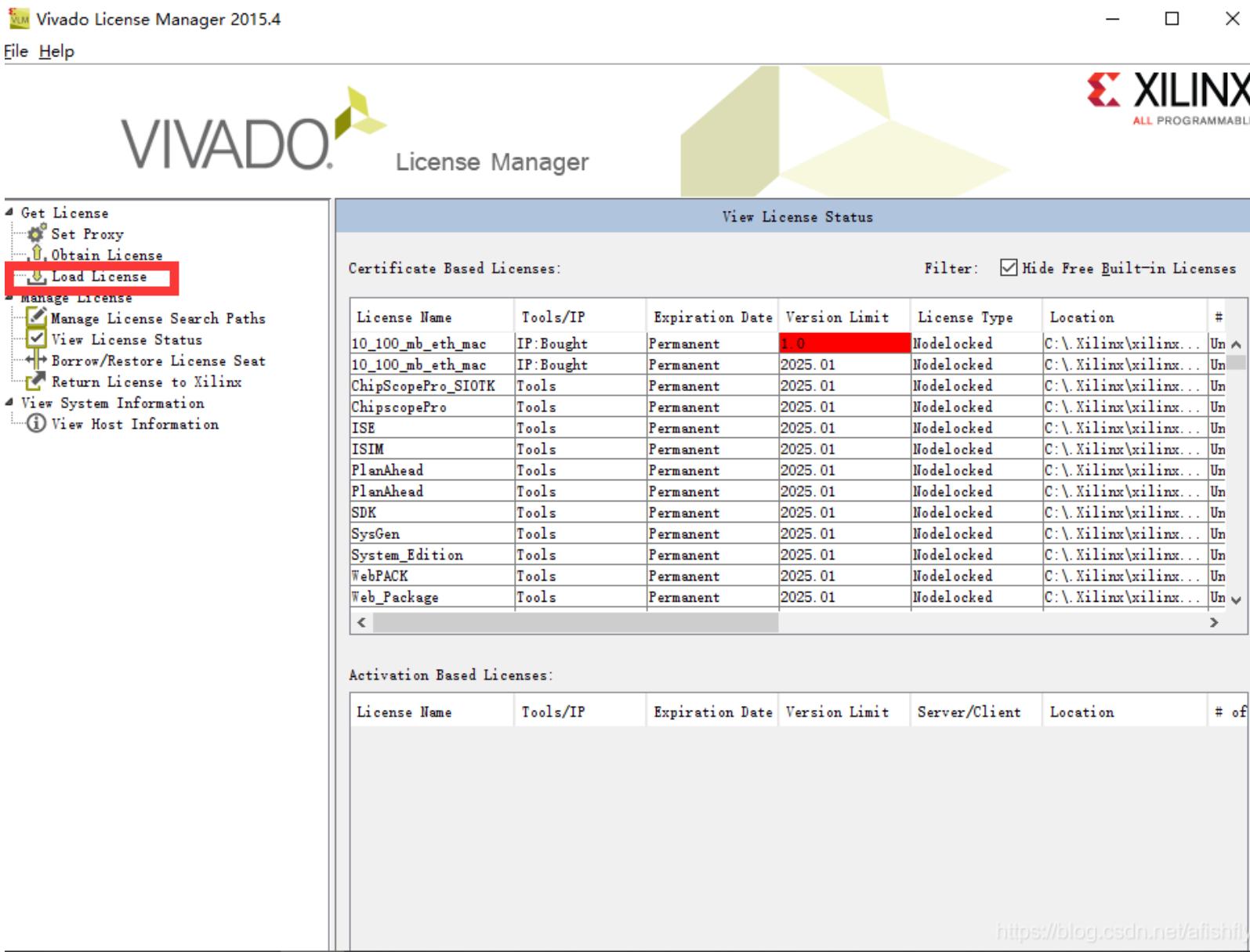
 XILINX
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SDx Family of Development Environments
for Systems and Software Engineers

www.xilinx.com/sdx

Load License





License Manager



Load License

Certificate Based Licenses

Click the 'Copy License' button to copy a certificate-based license (.lic file) into the local .Xilinx directory. Xilinx applications automatically detect valid, node-locked licenses (*.lic) residing in the local .Xilinx directory.

2 使用准备好的license

Activation Based Licenses

Click the 'Activate License' button to load a response XML file into VLM to activate your machine for Xilinx tools and IP.

Activate License...

<https://blog.csdn.net/afishily>

Verilog 简单回顾

Verilog HDL行为描述语言作为一种结构化和过程性的语言，其语法结构非常适合于算法级和RTL级的模型设计。这种行为描述语言具有以下功能：

- 可描述顺序执行或并行执行的程序结构。
- 用延迟表达式或事件表达式来明确地控制过程的启动时间。
- 通过命名的事件来触发其它过程里的激活行为或停止行为。
- 提供了条件、if-else、case、循环程序结构。
- 提供了可带参数且非零延续时间的任务(task)程序结构。
- 提供了可定义新的操作符的函数结构(function)。
- 提供了用于建立表达式的算术运算符、逻辑运算符、位运算符。

Arithmetic and Logistic Expression

- Logical operation vs. Bit-wise operation : $a \&\& b \mid\mid !c$ $a \& b \mid \sim c$
- Logical shift vs. arithmetic shift : $a >> 1$ $a >>> 1$
- Concatenation operation: $\{a[2:0], b[4:3]\}, \{\{3\}a\}, b$
- Logistic operation: $\&a$ b $|c$
- Ternary conditional operation: $is_zero ? 0 : A$
- Conversion between signed and unsigned: $\$signed(a), \$unsigned(b)$
- Vector slicing: $a[3:0], b[7-:4], b[4+:4]$
- Use Assignment to perform combinational logic:
 - `assign {a[2], a[0]} = 2'b10;`
 - `begin a = b; c = a; end`

More Expression

- If-else

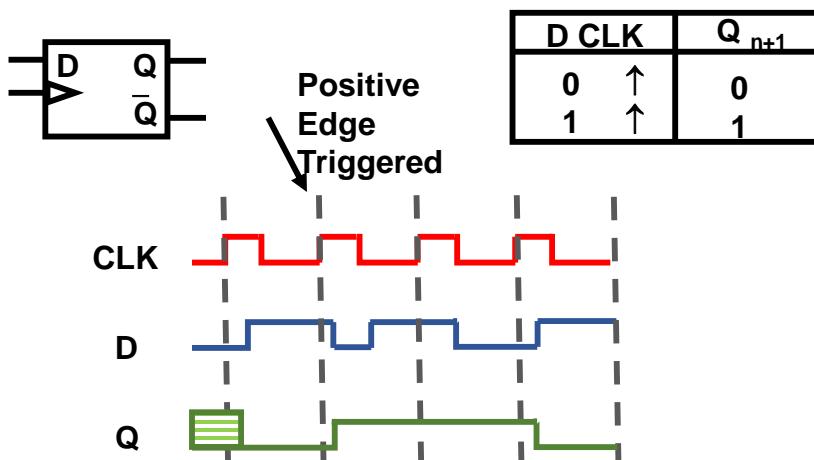
```
if (mode == 2'b01) begin
    y = a + b;
    z = a - b;
end
else if (mode == 2'b10) begin
    y = a * b;
    z = a >> b;
end
```

- Loop Generation Block

```
genvar i;
generate
    for (i = 0; i < 16; i = i + 1)
        begin: gen_add
            myadder a0(a[i], b[i],c[i]);
        end
    endgenerate
```

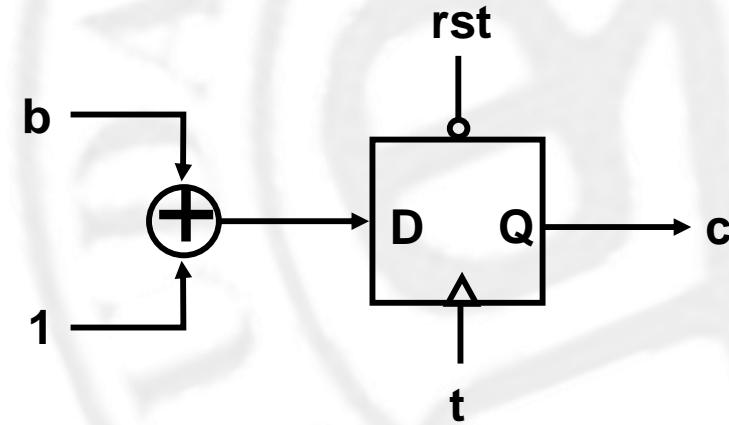
Sequential Always Block

- D Flip-Flop



- Use sequential always blocks
- Blocking and Non block Assignment

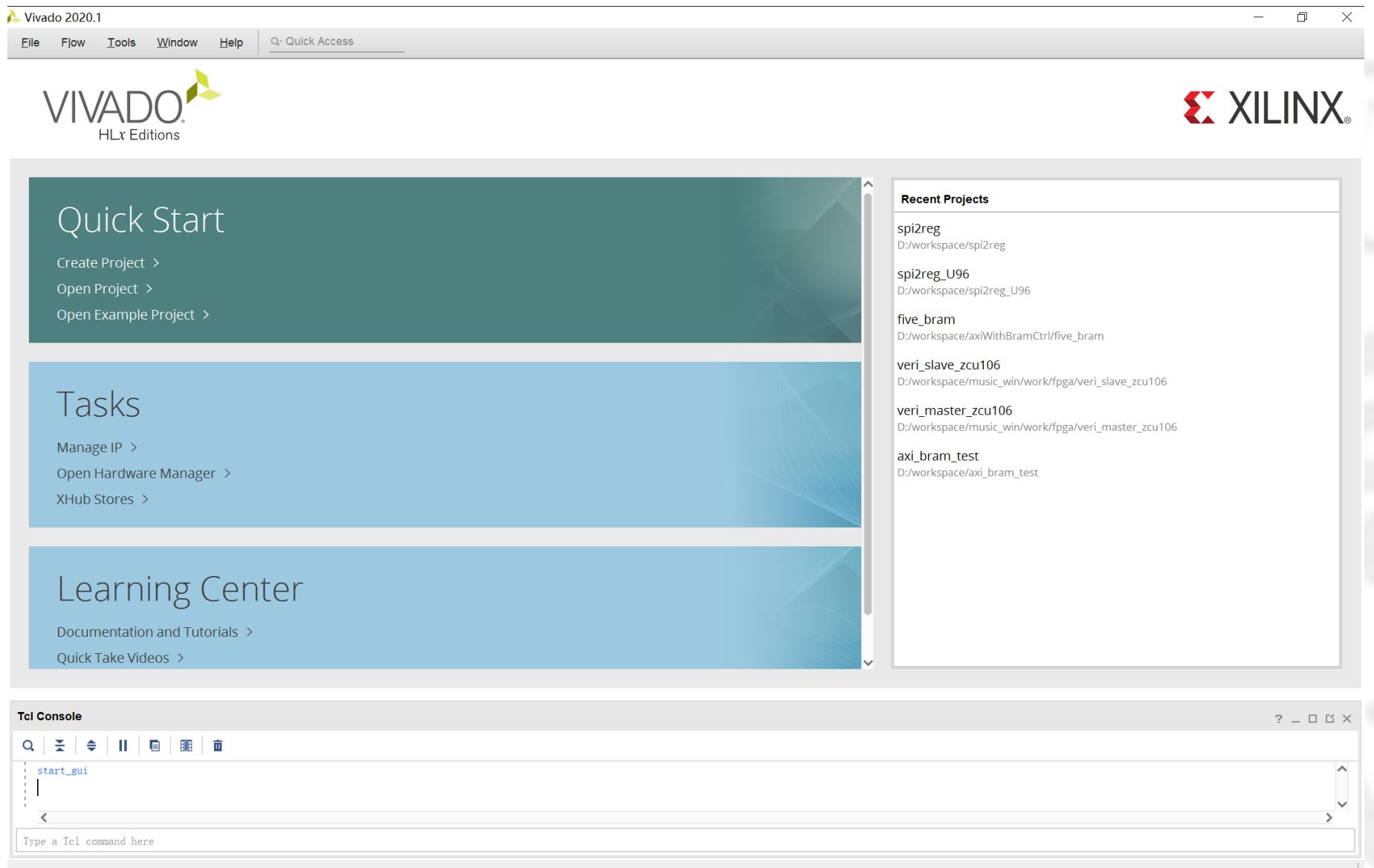
```
reg [2:0] c;
always @ (posedge t and negedge rst)
begin
  if (!rst) begin
    c <= 3'd0;
  end
  else begin
    c <= b + 3'd1;
  end
end
```



实验说明

a、b、c、d、e五人在进行一局Moba游戏，由于前期大规模落后对面，几乎失去赢得游戏的希望，现有一次投降重新进行对局的机会，五人中至少三人投降则可完成投降，五人均不能弃权。以result表示投降结果， $result = 1$ 表示投降成功。试写出result的表达式并用Verilog实现该电路逻辑，并建立testbench完成功能验证。

新建工程





XILINX®

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager
- XHub Stores >

Learning C

- Documentation and Tutorials
- Quick Take Videos >

Tcl Console

```
start_gui
```

Type a Tcl command here

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: fiveVote

Project location: D:/workspace/circuitExperiment

Create project subdirectory

Project will be created at: D:/workspace/circuitExperiment/fiveVote

< Back Next > Finish Cancel

工程名和路径



Quick Start

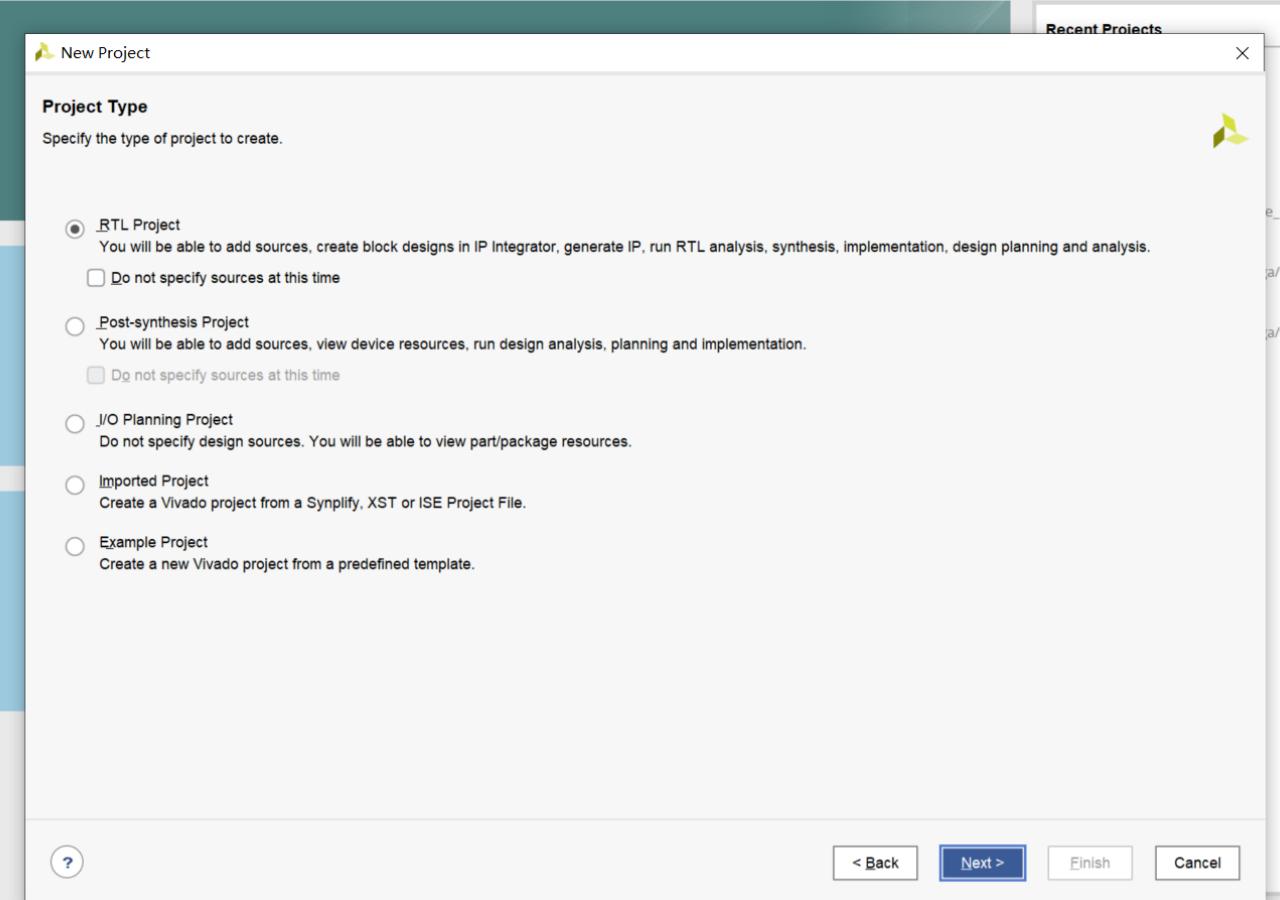
Create Project >
Open Project >
Open Example Project >

Tasks

Manage IP >
Open Hardware Manager >
XHub Stores >

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Documentation and Tutorials >
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Tcl Console



```
start_gui
```

创建一个新的项目



Quick Start

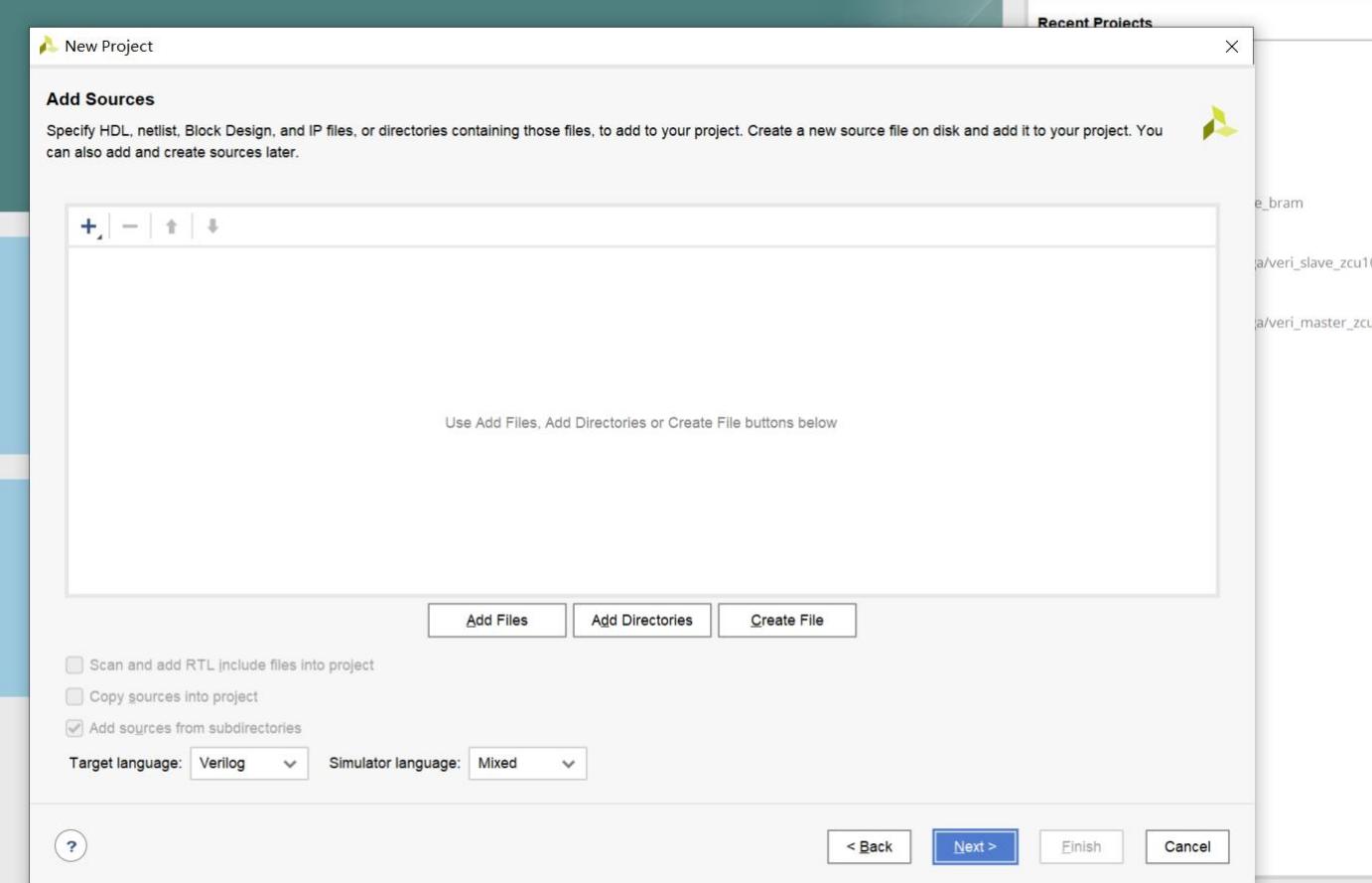
- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- XHub Stores >

Learning Center

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- Quick Take Videos >
- Release Notes Guide >



Tcl Console

Q | X | E | I | D | M | T | B
start_gui

Type a Tcl command here

创建一个新的项目



Quick Start

Create Project >

Open Project >

Open Example Project >

Tasks

Manage IP >

Open Hardware Manager >

XHub Stores >

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Documentation and Tutorials >

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Release Notes Guide >

New Project

Recent Projects

Default Part

Choose a default Xilinx part or board for your project.

根据条件选择硬件型号

Parts | Boards

Reset All Filters

Install/Update Boards

Vendor: All Name: All Board Rev: Latest

Search: Q

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev
Ultra96v1 Evaluation Platform		em.avnet.com	1.2	xczu3eg-sbva484-1-e	484	Rev 1
Ultra96v2 Evaluation Platform		em.avnet.com	1.0	xczu3eg-sbva484-1-e	484	Rev 1
ZedBoard Zynq Evaluation and Development Kit		em.avnet.com	1.4	xc7z020clg484-1	484	d
ZYNQ-7 ZC702 Evaluation Board		xilinx.com	1.4	xc7z020clg484-1	484	1.0
ZYNQ-7 ZC706 Evaluation Board		xilinx.com	1.4	xc7z045ffg900-2	900	1.1
Zynq UltraScale+ ZCU102 Evaluation Board		xilinx.com	2.0	xcvu280-fvh1156-2-i	1156	1.1

< Back Next > Finish Cancel

Tcl Console

start_gui

Type a Tcl command here

创建一个新的项目



Quick Start

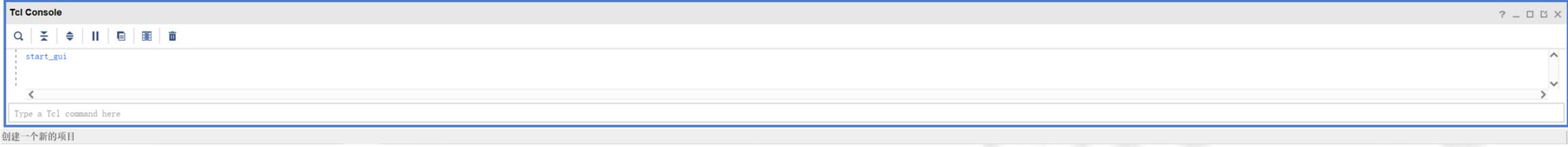
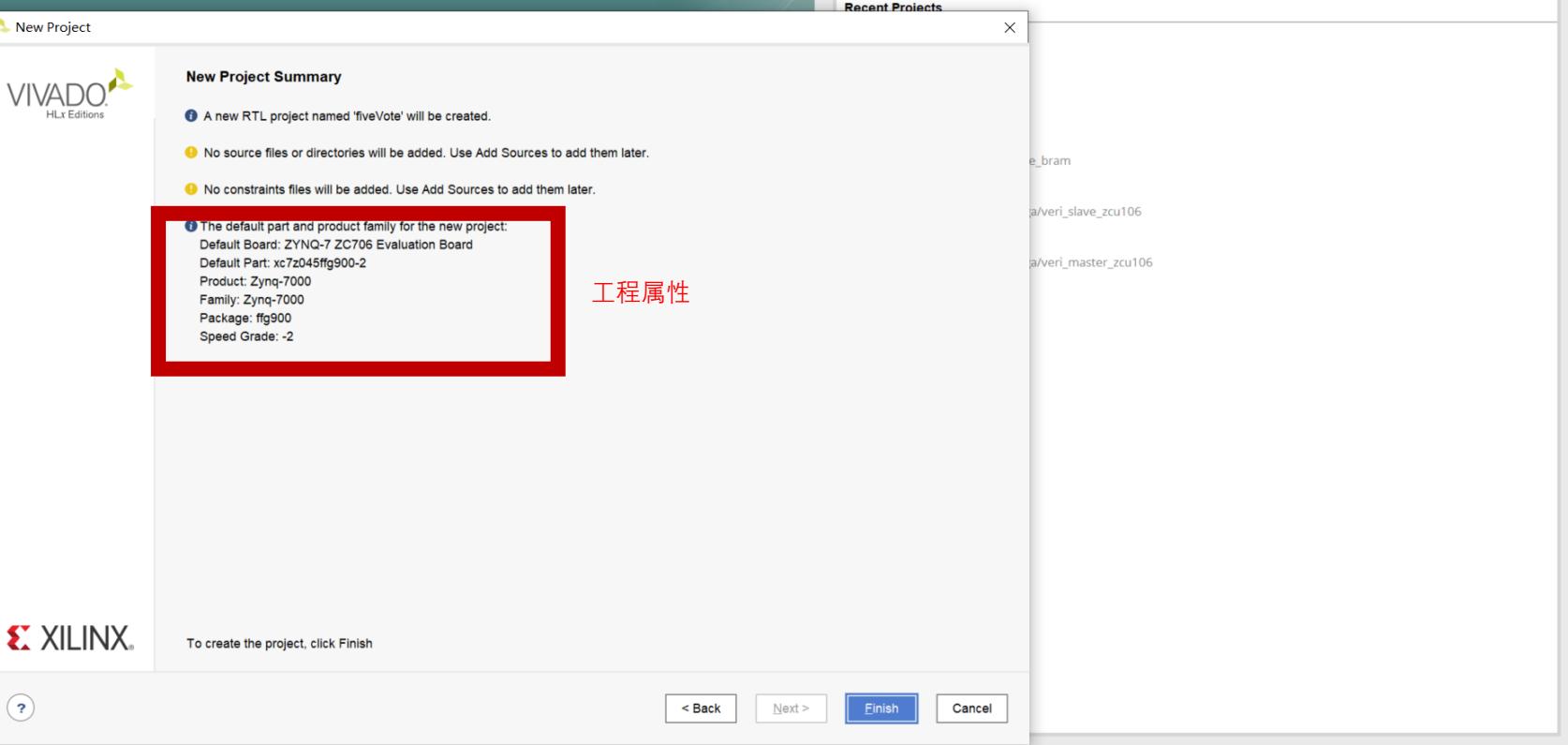
Create Project >
Open Project >
Open Example Project >

Tasks

Manage IP >
Open Hardware Manager >
XHub Stores >

Learning Center

Documentation and Tutorials >
Quick Take Videos >
Release Notes Guide >





Quick Start

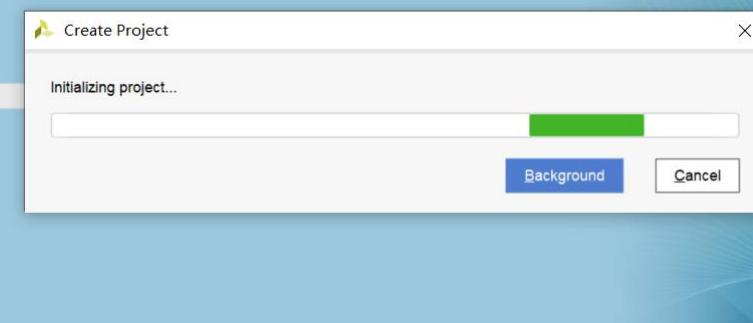
- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- XHub Stores >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >



Recent Projects

spi2reg	D:/workspace/spi2reg
spi2reg_U96	D:/workspace/spi2reg_U96
five_bram	D:/workspace/axiWithBramCtrl/five_bram
veri_slave_zcu106	D:/workspace/music_win/work/fpga/veri_slave_zcu106
veri_master_zcu106	D:/workspace/music_win/work/fpga/veri_master_zcu106
axi_bram_test	D:/workspace/axi_bram_test

Tcl Console

```
INFO: [IP_Flow 19-1704] No user IP repositories specified
<
Type a Tcl command here
Initializing project...
```

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access Ready Default Layout

Flow Navigator PROJECT MANAGER - fiveVote

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

Design Source Add Sources (Alt+A)

在工程内添加Verilog文件

Project Summary

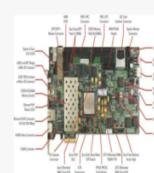
Overview Dashboard

Settings Edit

Project name: fiveVote
 Project location: D:/workspace/circuitExperiment/fiveVote
 Product family: Zynq-7000
 Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045fg900-2)
 Top module name: Not defined
 Target language: Verilog
 Simulator language: Mixed

Board Part

Display name: ZYNQ-7 ZC706 Evaluation Board
 Board part name: xilinx.com:z706:part0:1.4
 Board revision: 1.1
 Connectors: No connections
 Repository path: D:/Xilinx/Vivado/2020.1/data/boards/board_files
 URL: www.xilinx.com/zc706
 Board overview: ZYNQ-7 ZC706 Evaluation Board



Synthesis

Status: Not started
 Messages: No errors or warnings
 Part: xc7z045fg900-2
 Strategy: Vivado Synthesis Defaults
 Report Strategy: Vivado Synthesis Default Reports

Implementation

Status: Not started
 Messages: No errors or warnings
 Part: xc7z045fg900-2
 Strategy: Vivado Implementation Defaults
 Report Strategy: Vivado Implementation Default Reports

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Part
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)	xc7z045fg900-2
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)	xc7z045fg900-2

指定和/或创建源文件添加到工程

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access Ready Default Layout ? x

Flow Navigator

PROJECT MANAGER - fiveVote

Sources 0

- Design Sources
- Constraints
- Simulation Sources
 - sim_1
- Utility Sources

Project Summary

Overview | Dashboard

Settings Edit

Project name: fiveVote

Add Sources

This guides you through the process of adding and creating sources for your project

Add or create constraints

Add or create design sources

Add or create simulation sources

VIVADO
HDX Editions

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

XILINX

Not started
No errors or warnings
xc7z045fg900-2
Vivado Implementation Defaults
Vivado Implementation Default Reports

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Part
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)	xc7z045fg900-2
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)	xc7z045fg900-2

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q Quick Access Ready Default Layout ?

Flow Navigator □ ? -

PROJECT MANAGER - fiveVote

Sources ? - □ ×

Design Sources
Constraints
Simulation Sources
sim_1
Utility Sources

Project Summary Overview | Dashboard

Settings Edit

Project name: fiveVote

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

Add Files Add Directories Create File

Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories

< Back Next > Finish Cancel

Create Verilog 文件, 如果已经有Verilog文件, 可以直接 add

Tcl Console Messages Log Reports Design Runs

Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strategy Part

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Part
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)	xc7z045ffg900-2
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)	xc7z045ffg900-2

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Ready

Default Layout

PROJECT MANAGER - fiveVote

Flow Navigator

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

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PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1
- Utility Sources

Project Summary

Overview | Dashboard

Settings Edit

Project name: fiveVote

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

Create Source File

Create a new source file and add it to your project.

File type: Verilog

File name: fiveVote.v

File location: <Local to Project>

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

OK Cancel

新建 fiveVote.v

Tcl Console Messages Log Reports Design Runs

Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strategy Part

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Part
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)	xc7z045fg900-2
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)	xc7z045fg900-2

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access Ready Default Layout

PROJECT MANAGER - fiveVote

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1
- Utility Sources

Updating Q: Settings

Project Summary

Overview | Dashboard

Settings Edit

Project name: fiveVote
 Project location: D:/workspace/circuitExperiment/fiveVote
 Product family: Zynq-7000
 Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045ffg900-2)

Define Module

Define a module and specify I/O Ports to add to your source file.
 For each port specified:
 MSB and LSB values will be ignored unless its Bus column is checked.
 Ports with blank names will not be written.

Module Definition

Module name: fiveVote

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
input	v		0	0

OK Cancel

Implementation

Status: Not started
 Messages: No errors or warnings
 Part: xc7z045ffg900-2
 Strategy: Vivado Implementation Defaults
 Report Strategy: Vivado Implementation Default Reports

Tcl Console | Messages | Log | Reports | Design Runs

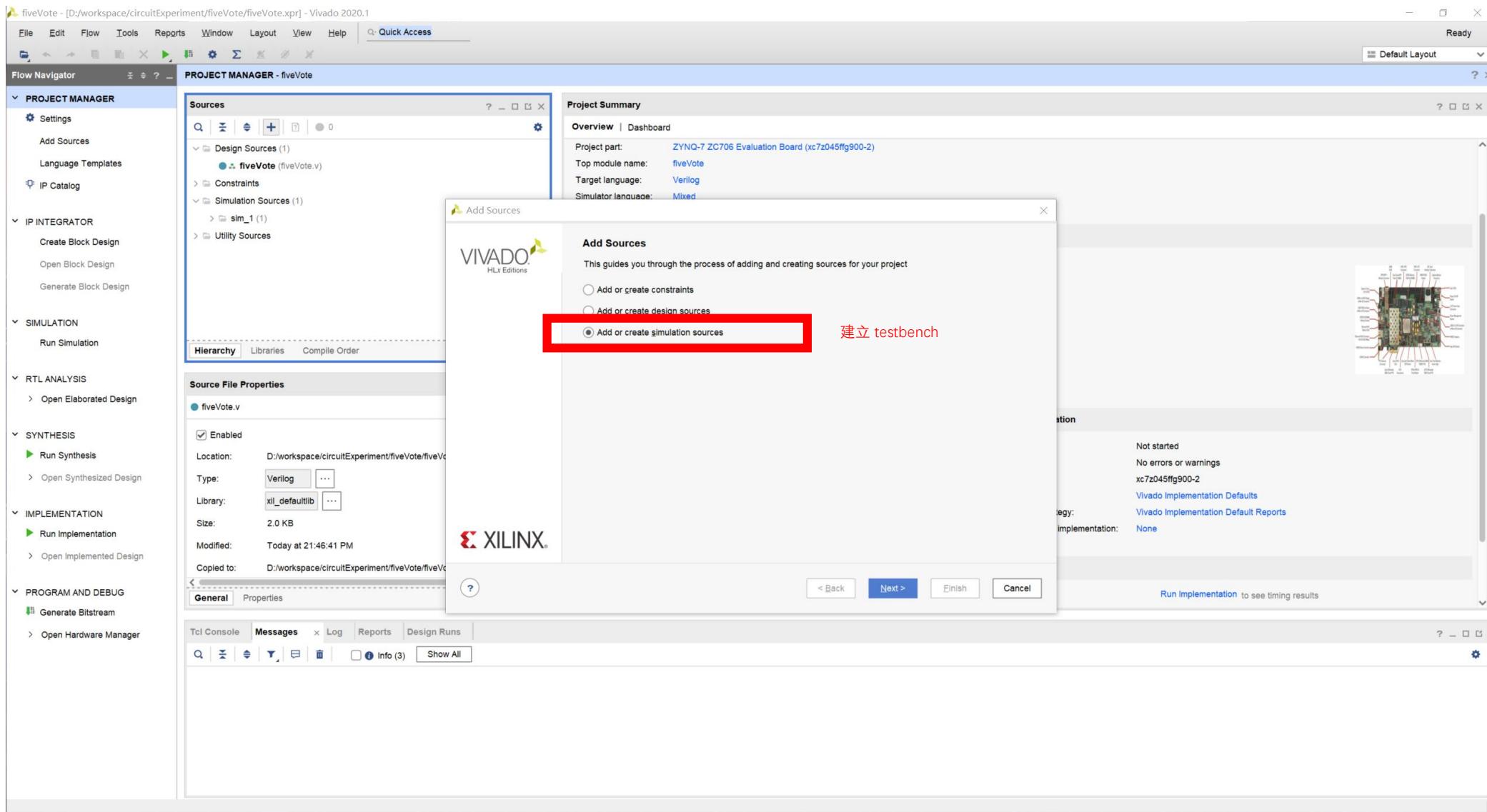
Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Part
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)	xc7z045ffg900-2
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)	xc7z045ffg900-2

Method one

```
module fiveVote(  
  
    input  a,  
    input  b,  
    input  c,  
    input  d,  
    input  e,  
    output result  
  
);  
  
assign result = (a && b && c && d && e) || (a && b && c && d && ~e)  
|| (a && b && c && ~d && e) || (a && b && c && ~d && ~e)  
|| (a && b && ~c && d && e) || (a && b && ~c && d && ~e)  
|| (a && b && ~c && ~d && e) || (a && ~b && c && d && e)  
|| (a && ~b && ~c && d && e) || (a && ~b && c && ~d && e )  
|| (a && ~b && c && d && ~e) || (~a && b && c && d && e)  
|| (~a && ~b && c && d && e) || (~a && b && ~c && d && e)  
|| (~a && b && c && ~d && e) || (~a && b && c && d && ~e);  
endmodule
```

仿真并完成验证



fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready Default Layout

Flow Navigator PROJECT MANAGER - fiveVote

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

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PROGRAM AND DEBUG

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Sources

- Design Sources (1)
 - fiveVote (fiveVote.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

fiveVote.v

- Enabled
- Location: D:/workspace/circuitExperiment/fiveVote/fiveV
- Type: Verilog
- Library: xil_defaultlib
- Size: 2.0 KB
- Modified: Today at 21:46:41 PM
- Copied to: D:/workspace/circuitExperiment/fiveVote/fiveV

General Properties

Tcl Console Messages Log Reports Design Runs

Messages

Info (3) Show All

Project Summary

Overview | Dashboard

Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045fg900-2)

Top module name: fiveVote

Target language: Verilog

Simulator language: Mixed

Add Sources

Add or Create Simulation Sources

Specify simulation set: sim_1

Add Files Add Directories Create File

Use Add Files, Add Directories or Create File buttons below

Scan and add RTL include files

Copy sources into project

Add sources from subdirectories

Include all design sources for simulation

Addition

Create testbench文件, 如果已经有Verilog文件, 可以直接add

Not started

No errors or warnings

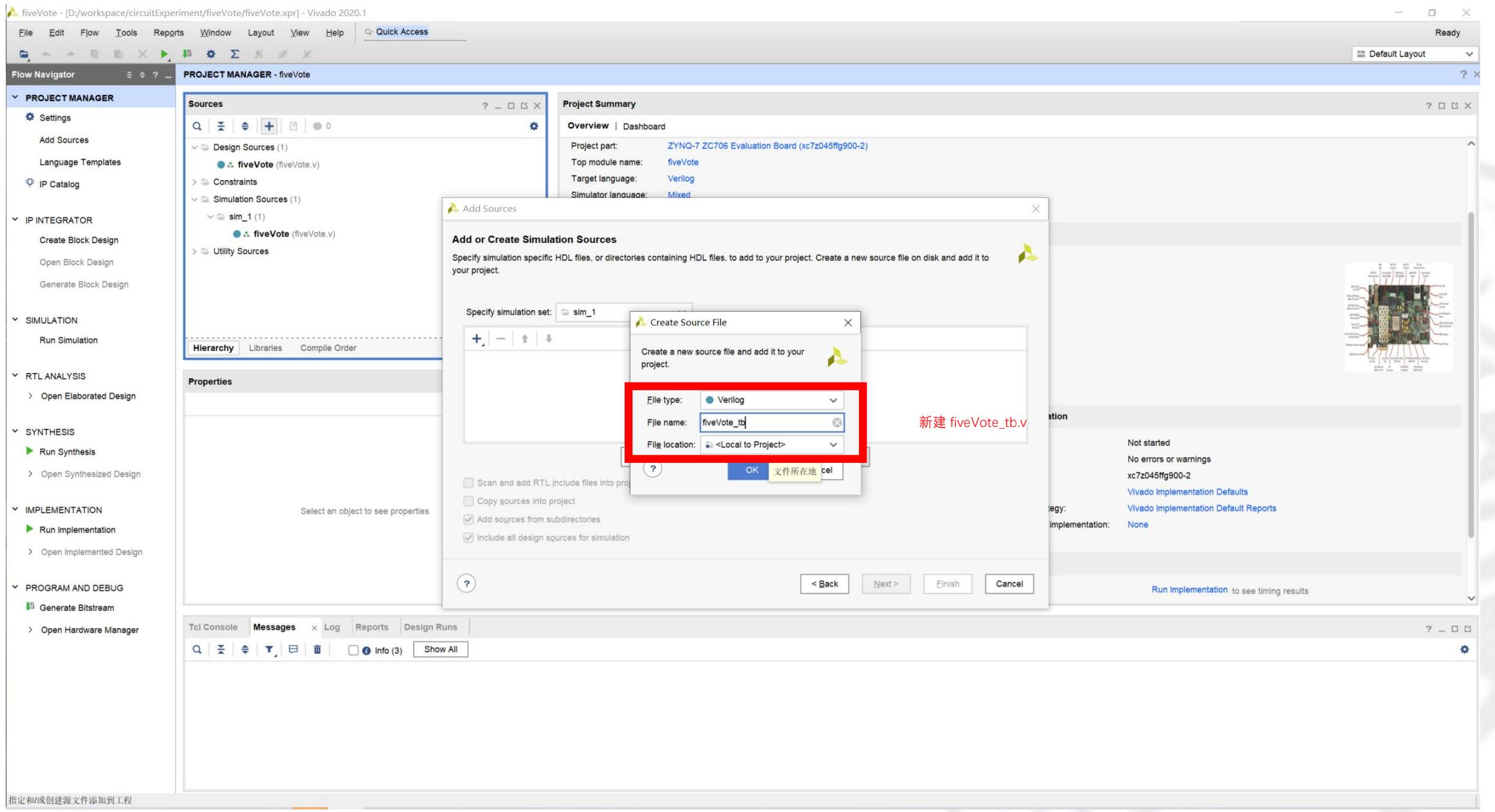
xc7z045fg900-2

Vivado Implementation Defaults

Vivado Implementation Default Reports

Implementation: None

Run Implementation to see timing results



fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready Default Layout

Flow Navigator PROJECT MANAGER

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

PROJECT MANAGER - fiveVote

Sources

- Design Sources (1)
 - fiveVote (fiveVote.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - fiveVote (fiveVote.v)
- Utility Sources

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

Project Summary

Overview | Dashboard

Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045ffg900-2)

Top module name: fiveVote

Target language: Verilog

Simulator language: Mixed

Add Sources

Add or Create Simulation Sources

Specify simulation set: sim_1

Index	Name	Library	Location
1	fiveVote_tb.v	xil_defaultlib	<Local to Project>

Add Files Add Directories Create File

Scan and add RTL Include files into project

Copy sources into project

Add sources from subdirectories

Include all design sources for simulation

?

< Back Next > Finish Cancel

Not started
No errors or warnings
xc7z045ffg900-2
Vivado Implementation Defaults
Vivado Implementation Default Reports
Implementation: None

Run Implementation to see timing results

Tcl Console Messages Log Reports Design Runs

Show All

指定和/或创建源文件添加到工程

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready Default Layout ? x

Flow Navigator **PROJECT MANAGER - fiveVote**

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

PROJECT MANAGER - fiveVote

Sources ? - Updating

- Design Sources (1)
 - fiveVote (fiveVote.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - fiveVote (fiveVote.v)
- Utility Sources

Hierarchy Libraries Compile Order

Properties ? - Select an object to see properties

Project Summary

Overview | Dashboard

Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045ffg900-2)

Top module name: fiveVote

Target language: Verilog

Simulator language: Mixed

Board Part

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: fiveVote_tb

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
input	input		0	0

DRC Violations

Run implementation to see DRC results

Implementation

- Status: Not started
- Messages: No errors or warnings
- Part: xc7z045ffg900-2
- Strategy: Vivado Implementation Defaults
- Report Strategy: Vivado Implementation Default Reports
- Incremental implementation: None

Timing

Run implementation to see timing results

Tcl Console Messages Log Reports Design Runs

Info (3) Show All

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready Default Layout ?

Flow Navigator ▾ PROJECT MANAGER - fiveVote

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - fiveVote (fiveVote.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - fiveVote (fiveVote.v)
- Utility Sources

Hierarchy Libraries Compile Order

Properties

Select an object to see properties

Project Summary

Overview | Dashboard

Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045fg900-2)

Top module name: fiveVote

Target language: Verilog

Simulator language: Mixed

Board Part

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: fiveVote

The module definition has not been changed.
Are you sure you want to use these values?

I/O Port Definition

Port Name	Direction	Bus	MSB	LSB
input	input		0	0

OK Cancel

DRC Violations

Run Implementation to see DRC results

Implementation

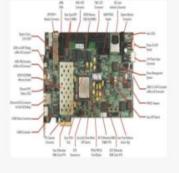
- Status: Not started
- Messages: No errors or warnings
- Part: xc7z045fg900-2
- Strategy: Vivado Implementation Defaults
- Report Strategy: Vivado Implementation Default Reports
- Incremental implementation: None

Timing

Run Implementation to see timing results

Tcl Console Messages Log Reports Design Runs

Info (3) Show All



fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready Default Layout

Flow Navigator PROJECT MANAGER

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

PROJECT MANAGER - fiveVote

Sources

- Design Sources (1)
 - fiveVote (fiveVote.v)
- Constraints
- Simulation Sources (2)
 - fiveVote (fiveVote_tb.v)
 - Utility Sources

Hierarchy Libraries Compile Order

fiveVote.v and fiveVote_tb.v

Project Summary

Overview | Dashboard

Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045fg900-2)

Top module name: fiveVote

Target language: Verilog

Simulator language: Mixed

Board Part

Display name: ZYNQ-7 ZC706 Evaluation Board

Board part name: xilinx.com:zc706:part0:1.4

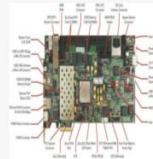
Board revision: 1.1

Connectors: No connections

Repository path: D:/Xilinx/Vivado/2020.1/data/boards/board_files

URL: www.xilinx.com/zc706

Board overview: ZYNQ-7 ZC706 Evaluation Board



Source File Properties

fiveVote.v

Enabled

Location: D:/workspace/circuitExperiment/fiveVote/fiveVote.srcc/sources_1/new

Type: Verilog

Library: xil_defaultlib

Size: 2.0 KB

Modified: Today at 21:46:41 PM

Copied to: D:/workspace/circuitExperiment/fiveVote/fiveVote.srcc/sources_1/new

General Properties

Synthesis

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z045fg900-2
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	None

Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z045fg900-2
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Run Implementation to see DRC results

Timing

Run Implementation to see timing results

Tcl Console Messages Log Reports Design Runs

Info (3) Show All

```
module fiveVote_tb(
);
reg a,b,c,d,e;
wire result;
fiveVote fiveVote(
    .a(a),
    .b(b),
    .c(c),
    .d(d),
    .e(e),
    .result(result)
);
initial begin
begin
    a = 1'b0;
    b = 1'b0;
    c = 1'b0;
    d = 1'b0;
    e = 1'b0;
end
```

```
#100
begin
    a = 1'b1;
    b = 1'b0;
    c = 1'b0;
    d = 1'b0;
    e = 1'b0;
end
#100
begin
    a = 1'b1;
    b = 1'b0;
    c = 1'b1;
    d = 1'b0;
    e = 1'b1;
end
#100
begin
    a = 1'b1;
    b = 1'b0;
    c = 1'b1;
    d = 1'b1;
    e = 1'b0;
end
#100
begin
    a = 1'b1;
    b = 1'b1;
    c = 1'b1;
    d = 1'b1;
    e = 1'b0;
end
#100
begin
    a = 1'b1;
    b = 1'b1;
    c = 1'b0;
    d = 1'b1;
    e = 1'b0;
end
```

```
#100
begin
    a = 1'b1;
    b = 1'b0;
    c = 1'b1;
    d = 1'b0;
    e = 1'b1;
end
#100
begin
    a = 1'b0;
    b = 1'b0;
    c = 1'b0;
    d = 1'b1;
    e = 1'b1;
end
#100
begin
    a = 1'b0;
    b = 1'b0;
    c = 1'b0;
    d = 1'b1;
    e = 1'b1;
end
#100
begin
    a = 1'b1;
    b = 1'b1;
    c = 1'b0;
    d = 1'b1;
    e = 1'b0;
end
#100
begin
    a = 1'b1;
    b = 1'b1;
    c = 1'b0;
    d = 1'b1;
    e = 1'b0;
end
end
endmodule
```

Vivado Simulator

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready Default Layout ? x

Flow Navigator PROJECT MANAGER - fiveVote

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation
- Run Behavioral Simulation (highlighted with a red box)

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - fiveVote (fiveVote.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - fiveVote_tb (fiveVote_tb.v) (1)
 - Utility Sources

Project Summary

Overview | Dashboard

Settings Edit

Project name: fiveVote
Project location: D:/workspace/circuitExperiment/fiveVote
Product family: Zynq-7000
Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045ffg900-2)
Top module name: fiveVote
Target language: Verilog
Simulator language: Mixed

Board Part

Display name: ZYNQ-7 ZC706 Evaluation Board
Board part name: xilinx.com:zc706:part0:1.4
Board revision: 1.1
Connectors: No connections
Repository path: D:/Xilinx/Vivado/2020.1/data/boards/board_files
URL: www.xilinx.com/zc706
Board overview: ZYNQ-7 ZC706 Evaluation Board
Changes

Tcl Console Messages Log Reports Design Runs

General Properties

Synthesis Implementation

Status: Not started Status: Not started
Messages: No errors or warnings Messages: No errors or warnings
Part: xc7z045ffg900-2 Part: xc7z045ffg900-2
Strategy: Vivado Synthesis Defaults Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Synthesis Default Reports Report Strategy: Vivado Implementation Default Reports

Vivado Commands (7 status messages)

- General Messages (7 status messages)
 - Command: launch_simulation (6 more like this)
- Simulation (14 status messages)
 - sim_1 (14 status messages)
 - Vivado Simulator 2020.1 (13 more like this)

Info (18) Status (21) Show All

?

Default Layout

?

x

fiveVote - [D:/workspace/circuitExperiment/fiveVote/fiveVote.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready Default Layout ? x

Flow Navigator PROJECT MANAGER - fiveVote

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - fiveVote (fiveVote.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - fiveVote_tb (fiveVote_tb.v) (1)
- Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

fiveVote_tb.v

Enabled

Location: D:/workspace/circuitExperiment/fiveVote/fiveVote.srscs/sim_1/new

Type: Verilog

Library: xil_defaultlib

Size: 1.7 KB

Modified: Today at 22:00:51 PM

Copied to: D:/workspace/circuitExperiment/fiveVote/fiveVote.srscs/sim_1/new

General Properties

Tcl Console Messages Log Reports Design Runs

Info (10) Status (1) Show All

Vivado Commands (1 status message)

- General Messages (1 status message)
 - Command: launch_simulation

Project Summary

Overview | Dashboard

Project part: ZYNQ-7 ZC706 Evaluation Board (xc7z045ffg900-2)

Top module name: fiveVote

Target language: Verilog

Simulator language: Mixed

Board Part

Display name: ZYNQ-7 ZC706 Evaluation Board

Board part name: xilinx.com:zc706:part0:1.4

Board revision: 1.1

Connectors: No connections

Repository path: D:/Xilinx/Vivado/2020.1/data/boards/board_files

URL: www.xilinx.com/zc706

Run Simulation

Executing elaborate step...

Background Cancel

Part: xc7z045ffg900-2

Strategy: Vivado Synthesis Defaults

Report Strategy: Vivado Synthesis Default Reports

Incremental synthesis: None

Implementation

Status: Not started

Messages: No errors or warnings

Part: xc7z045ffg900-2

Strategy: Vivado Implementation Defaults

Report Strategy: Vivado Implementation Default Reports

Incremental implementation: None

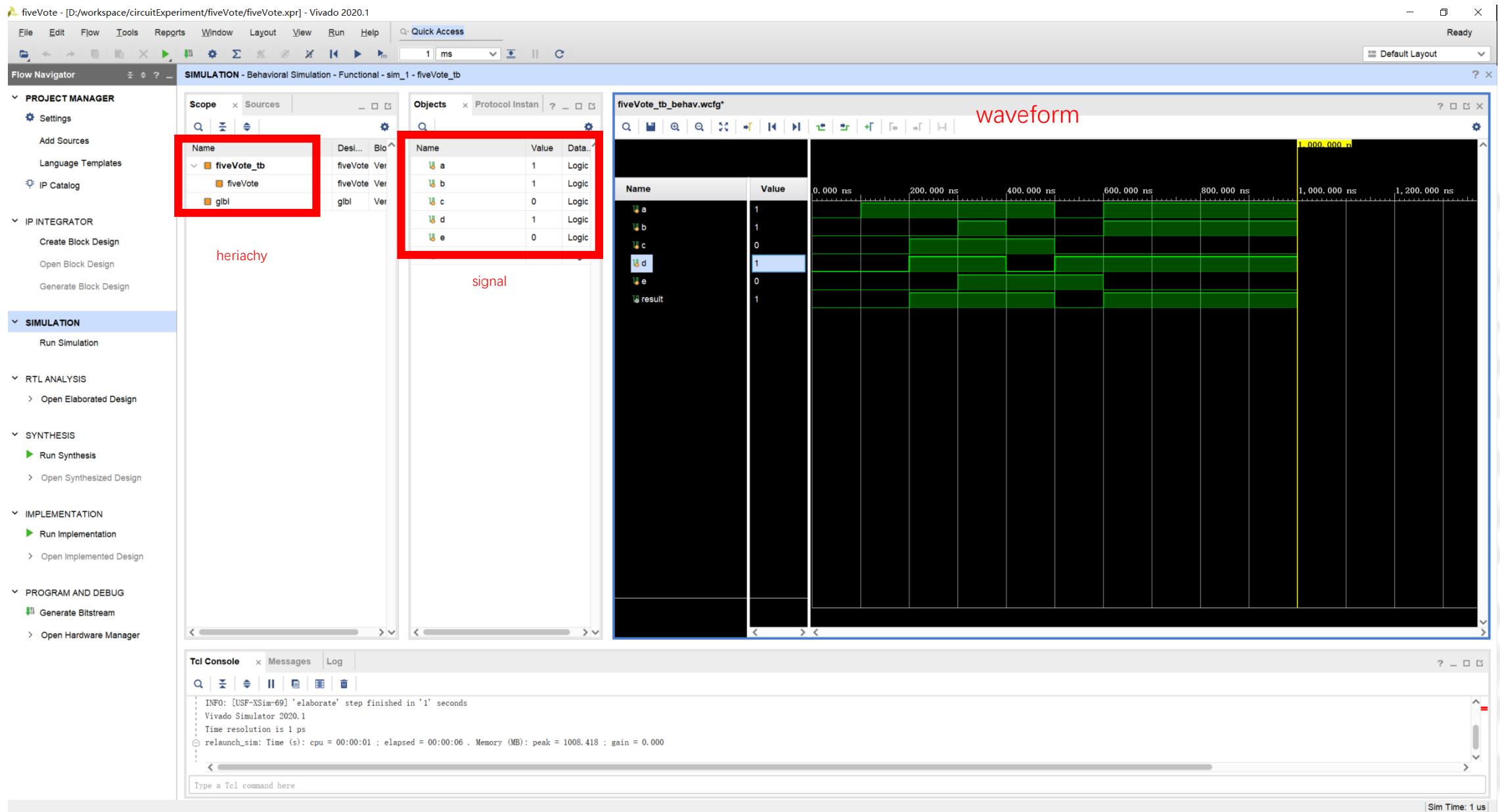
DRC Violations

Run Implementation to see DRC results

Timing

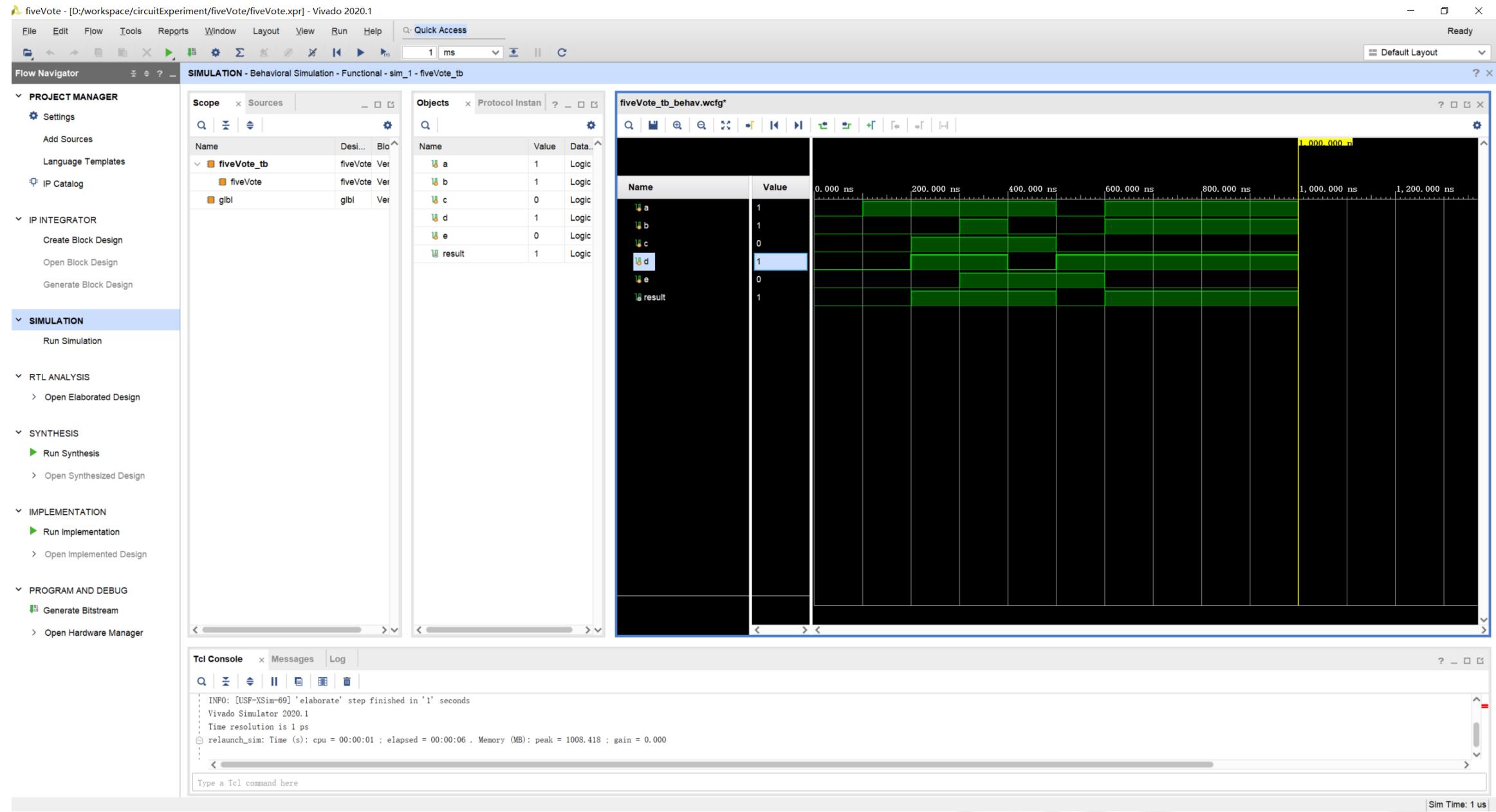
Run Implementation to see timing results

Executing elaborate step...



Another method

```
module fiveVote(  
  
    input  a,  
    input  b,  
    input  c,  
    input  d,  
    input  e,  
    output result  
  
);  
  
assign result = (a && b && c) || (a && b && d) ||  
                (a && b && e) || (a && c && d) ||  
                (a && c && e) || (a && d && e) ||  
                (b && c && d) || (b && c && e) ||  
                (c && d && e);  
endmodule
```



```
module fiveVote(
```

```
    input  a,  
    input  b,  
    input  c,  
    input  d,  
    input  e,  
    output result
```

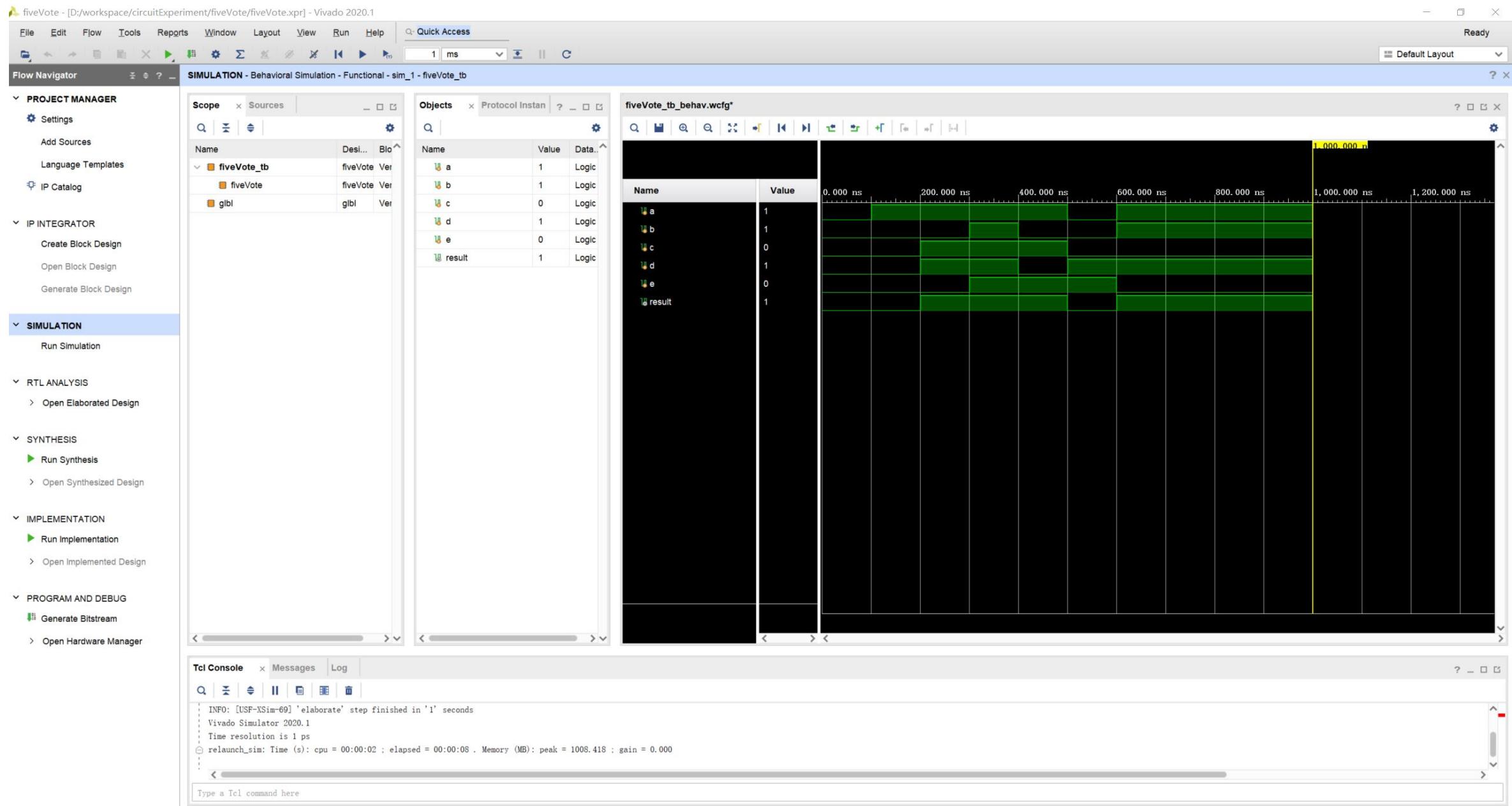
```
);
```

```
assign result = (a && b && c) || (a && b && d) ||  
                (a && b && e) || (a && c && d) ||  
                (a && c && e) || (a && d && e) ||  
                (b && c && d) || (b && c && e) ||  
                (c && d && e);
```

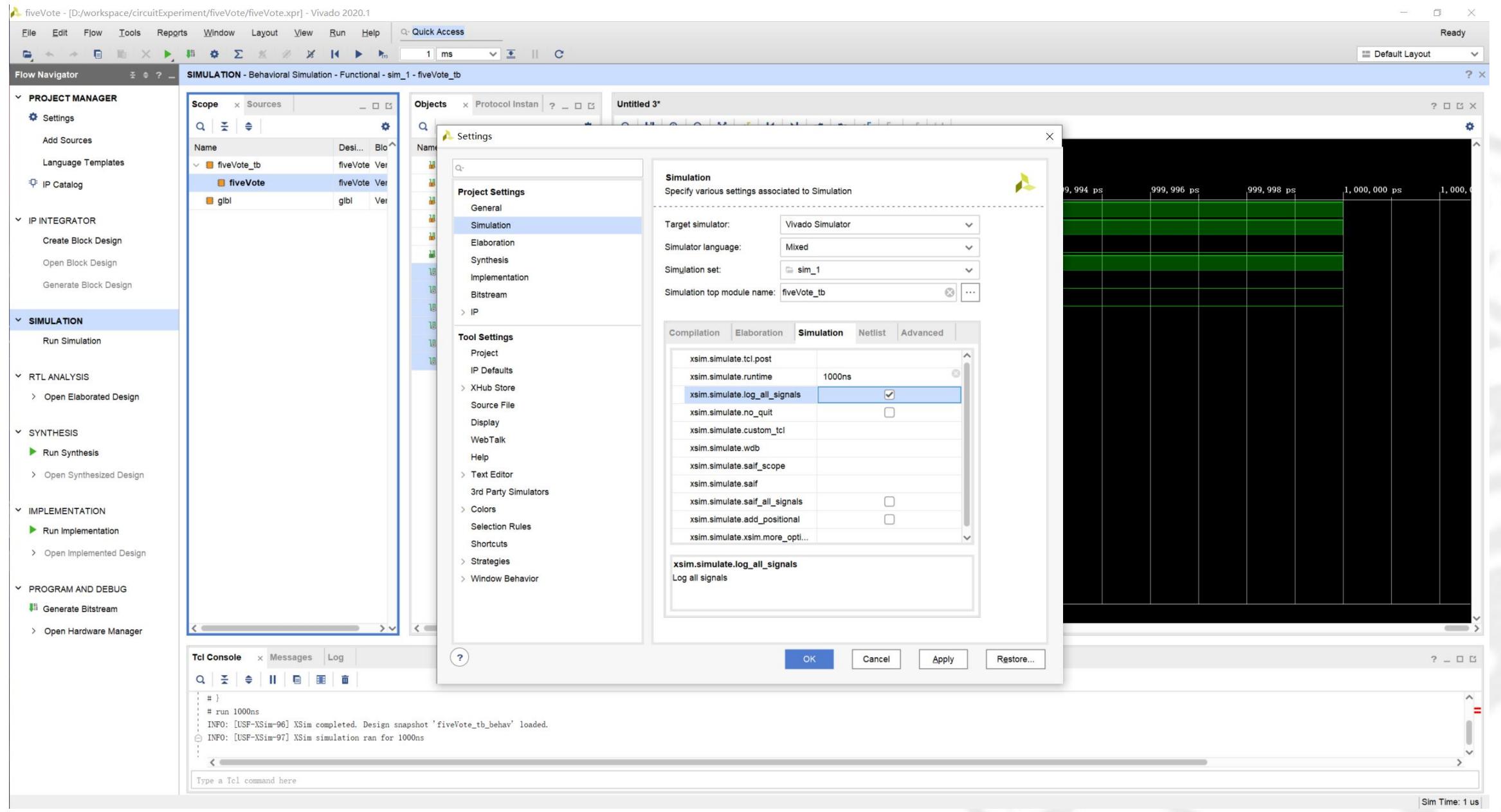
```
endmodule
```

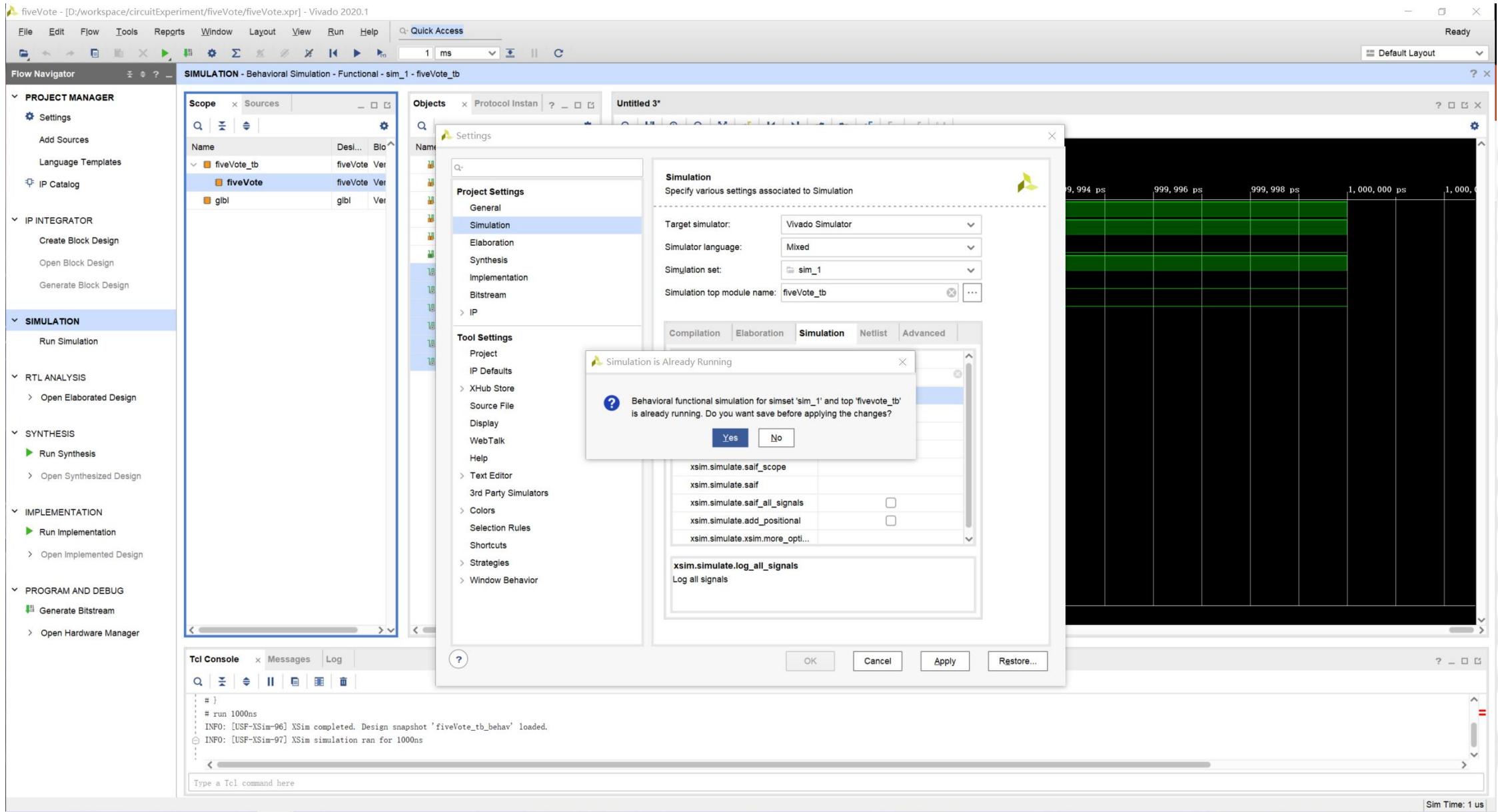
```
wire abc,abd,abe,acd,ace,ade,bcd,  
      bce,cde;
```

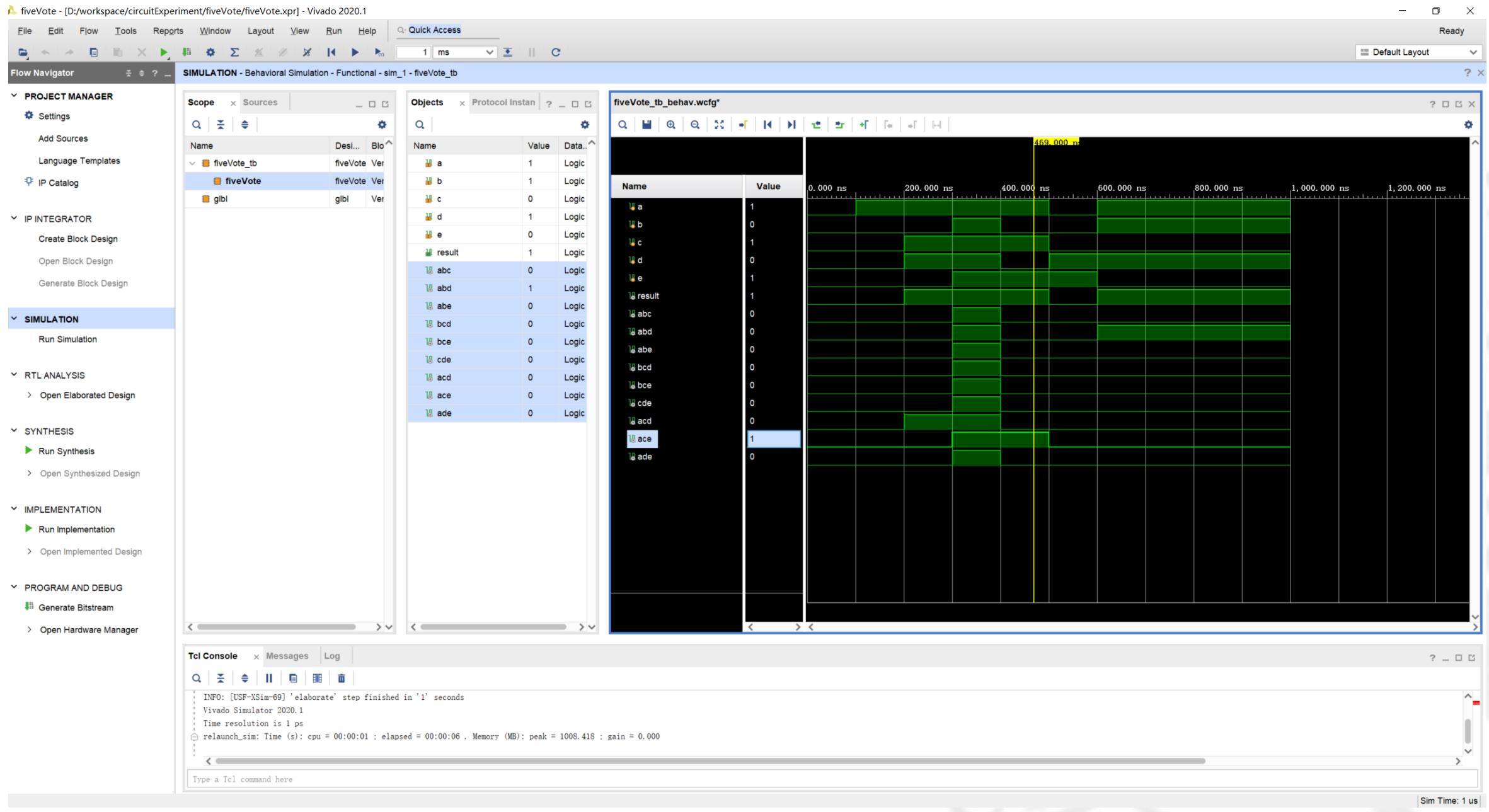
```
assign abc = a && b && c;  
assign abd = a && b && d;  
assign abe = a && b && e;  
assign acd = a && c && d;  
assign ace = a && c && e;  
assign ade = a && d && e;  
assign bcd = b && c && d;  
assign bce = b && c && e;  
assign cde = c && d && e;  
assign result = abc || abd ||  
              abe || acd ||  
              ace || ade ||  
              bcd || bce ||  
              cde;
```



Add all signals







Another Method

```
module fiveVote(  
    input  a,  
    input  b,  
    input  c,  
    input  d,  
    input  e,  
    output result  
);  
  
    assign result = (a + b + c + d + e > 2);  
  
endmodule
```

