FAET630004: Computer & AI Architecture **(Due: 03/23/19)**

Homework Assignment #1

Instructor: Chixiao Chen *Name:* , *FudanID:*

- This HW counts 15% of your final score, please treat it carefully.
- Please submit the electronic copy via mail: cxchen@fudan.edu.cn before 03/23/2019 11:59pm.
- It is encouraged to use LaTeX to edit it, the source code of the assignment is available via: https://www.overleaf.com/read/fgtznxwhfrss
- You can also open it by Office Word, and save it as a .doc file for easy editing. Also, you can print it out, complete it and scan it by your cellphone.
- Problem 2 needs verilog/SV simulation. If you do not have a local verilog simulator, please use an online tool: https://www.edaplayground.com/, you need register for save.
- You can answer the assignment either in Chinese or English

Problem 1: Translation from C code to Assembly Code (20+20=40 points)

(a) Please translate the following C code into assembly language, using the RV32I instruction set shown in Appendix I.
(b) When using the compressed version in Appendix II, how many bytes will be saved ?

```
int b;    // b is a global variable

void multiplier (int a){
   int i, result;
   for (i = 0; i<b; i++){
      result=result+a;
   }
}
```

Solution:

Problem 2: Verilog/System Verilog for a Register File

(20+20+20=60 points)

As the R-type, I-type, and S-type indicate, the RISC-V has a uniform register file (RF) design. If you are the verilog engineer who is asked to design a VERY **SIMPLE** version of the RV32I RF, please complete the problems below.

(a) How many ports should the RF have? What about their direction (input/output/inout)? Please use a table to illutrate it.
(b) Write a verilog/SV RTL for the RF. (hint: 32 32-bit integer registers and zero register is always zero.)
(c) Write a testbench for the RF in verilog/SV to perform the following assembly code. Please also include the simulated waveform in your solution.

```
addi x11, x0, 31
addi x12, x0, -60
add  x15, x11, x12
```

Solution:

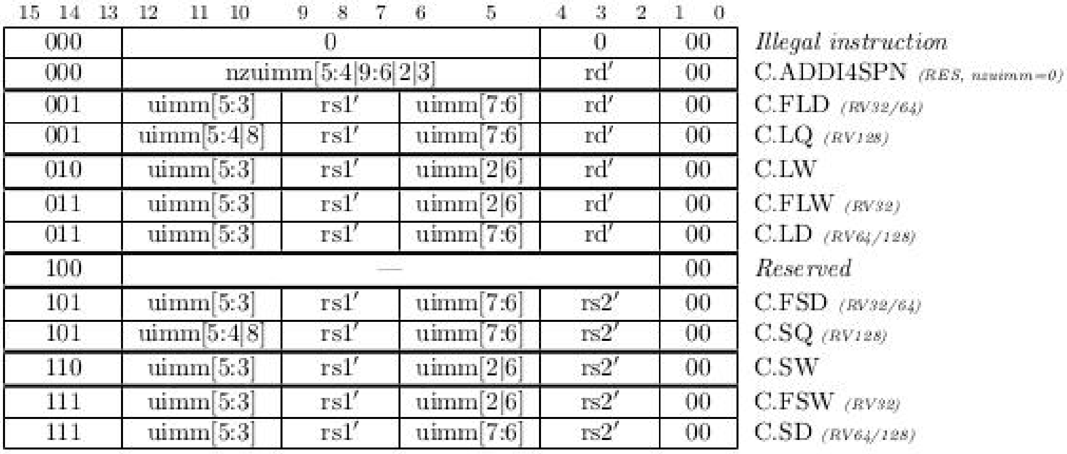
Appendix I:

RV32I Base Instruction Set

<table>
<tr><td colspan="6">imm[31:12]</td><td>rd</td><td>0110111</td><td>LUI</td></tr>
<tr><td colspan="6">imm[31:12]</td><td>rd</td><td>0010111</td><td>AUIPC</td></tr>
<tr><td colspan="6">imm[20|10:1|11|19:12]</td><td>rd</td><td>1101111</td><td>JAL</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>000</td><td>rd</td><td>1100111</td><td>JALR</td></tr>
<tr><td colspan="2">imm[12|10:5]</td><td colspan="2">rs2</td><td>rs1</td><td>000</td><td>imm[4:1|11]</td><td>1100011</td><td>BEQ</td></tr>
<tr><td colspan="2">imm[12|10:5]</td><td colspan="2">rs2</td><td>rs1</td><td>001</td><td>imm[4:1|11]</td><td>1100011</td><td>BNE</td></tr>
<tr><td colspan="2">imm[12|10:5]</td><td colspan="2">rs2</td><td>rs1</td><td>100</td><td>imm[4:1|11]</td><td>1100011</td><td>BLT</td></tr>
<tr><td colspan="2">imm[12|10:5]</td><td colspan="2">rs2</td><td>rs1</td><td>101</td><td>imm[4:1|11]</td><td>1100011</td><td>BGE</td></tr>
<tr><td colspan="2">imm[12|10:5]</td><td colspan="2">rs2</td><td>rs1</td><td>110</td><td>imm[4:1|11]</td><td>1100011</td><td>BLTU</td></tr>
<tr><td colspan="2">imm[12|10:5]</td><td colspan="2">rs2</td><td>rs1</td><td>111</td><td>imm[4:1|11]</td><td>1100011</td><td>BGEU</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>000</td><td>rd</td><td>0000011</td><td>LB</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>001</td><td>rd</td><td>0000011</td><td>LH</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>010</td><td>rd</td><td>0000011</td><td>LW</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>100</td><td>rd</td><td>0000011</td><td>LBU</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>101</td><td>rd</td><td>0000011</td><td>LHU</td></tr>
<tr><td colspan="2">imm[11:5]</td><td colspan="2">rs2</td><td>rs1</td><td>000</td><td>imm[4:0]</td><td>0100011</td><td>SB</td></tr>
<tr><td colspan="2">imm[11:5]</td><td colspan="2">rs2</td><td>rs1</td><td>001</td><td>imm[4:0]</td><td>0100011</td><td>SH</td></tr>
<tr><td colspan="2">imm[11:5]</td><td colspan="2">rs2</td><td>rs1</td><td>010</td><td>imm[4:0]</td><td>0100011</td><td>SW</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>000</td><td>rd</td><td>0010011</td><td>ADDI</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>010</td><td>rd</td><td>0010011</td><td>SLTI</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>011</td><td>rd</td><td>0010011</td><td>SLTIU</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>100</td><td>rd</td><td>0010011</td><td>XORI</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>110</td><td>rd</td><td>0010011</td><td>ORI</td></tr>
<tr><td colspan="4">imm[11:0]</td><td>rs1</td><td>111</td><td>rd</td><td>0010011</td><td>ANDI</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">shamt</td><td>rs1</td><td>001</td><td>rd</td><td>0010011</td><td>SLLI</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">shamt</td><td>rs1</td><td>101</td><td>rd</td><td>0010011</td><td>SRLI</td></tr>
<tr><td colspan="2">0100000</td><td colspan="2">shamt</td><td>rs1</td><td>101</td><td>rd</td><td>0010011</td><td>SRAI</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>000</td><td>rd</td><td>0110011</td><td>ADD</td></tr>
<tr><td colspan="2">0100000</td><td colspan="2">rs2</td><td>rs1</td><td>000</td><td>rd</td><td>0110011</td><td>SUB</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>001</td><td>rd</td><td>0110011</td><td>SLL</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>010</td><td>rd</td><td>0110011</td><td>SLT</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>011</td><td>rd</td><td>0110011</td><td>SLTU</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>100</td><td>rd</td><td>0110011</td><td>XOR</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>101</td><td>rd</td><td>0110011</td><td>SRL</td></tr>
<tr><td colspan="2">0100000</td><td colspan="2">rs2</td><td>rs1</td><td>101</td><td>rd</td><td>0110011</td><td>SRA</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>110</td><td>rd</td><td>0110011</td><td>OR</td></tr>
<tr><td colspan="2">0000000</td><td colspan="2">rs2</td><td>rs1</td><td>111</td><td>rd</td><td>0110011</td><td>AND</td></tr>
<tr><td>0000</td><td colspan="2">pred</td><td>succ</td><td>00000</td><td>000</td><td>00000</td><td>0001111</td><td>FENCE</td></tr>
<tr><td>0000</td><td colspan="2">0000</td><td>0000</td><td>00000</td><td>001</td><td>00000</td><td>0001111</td><td>FENCE.I</td></tr>
<tr><td colspan="4">000000000000</td><td>00000</td><td>000</td><td>00000</td><td>1110011</td><td>ECALL</td></tr>
<tr><td colspan="4">000000000001</td><td>00000</td><td>000</td><td>00000</td><td>1110011</td><td>EBREAK</td></tr>
<tr><td colspan="4">csr</td><td>rs1</td><td>001</td><td>rd</td><td>1110011</td><td>CSRRW</td></tr>
<tr><td colspan="4">csr</td><td>rs1</td><td>010</td><td>rd</td><td>1110011</td><td>CSRRS</td></tr>
<tr><td colspan="4">csr</td><td>rs1</td><td>011</td><td>rd</td><td>1110011</td><td>CSRRC</td></tr>
<tr><td colspan="4">csr</td><td>zimm</td><td>101</td><td>rd</td><td>1110011</td><td>CSRRWI</td></tr>
<tr><td colspan="4">csr</td><td>zimm</td><td>110</td><td>rd</td><td>1110011</td><td>CSRRSI</td></tr>
<tr><td colspan="4">csr</td><td>zimm</td><td>111</td><td>rd</td><td>1110011</td><td>CSRRCI</td></tr>
</table>

Figure 1: RV32I RISC-V Instruction Set

Appendix II:



15 14 13	12 11 10	9 8 7	6 5	4 3 2	1 0	
000	0			0	00	*Illegal instruction*
000	nzuimm[5:4|9:6|2|3]			rd′	00	C.ADDI4SPN *(RES, nzuimm=0)*
001	uimm[5:3]	rs1′	uimm[7:6]	rd′	00	C.FLD *(RV32/64)*
001	uimm[5:4|8]	rs1′	uimm[7:6]	rd′	00	C.LQ *(RV128)*
010	uimm[5:3]	rs1′	uimm[2|6]	rd′	00	C.LW
011	uimm[5:3]	rs1′	uimm[2|6]	rd′	00	C.FLW *(RV32)*
011	uimm[5:3]	rs1′	uimm[7:6]	rd′	00	C.LD *(RV64/128)*
100	—				00	*Reserved*
101	uimm[5:3]	rs1′	uimm[7:6]	rs2′	00	C.FSD *(RV32/64)*
101	uimm[5:4|8]	rs1′	uimm[7:6]	rs2′	00	C.SQ *(RV128)*
110	uimm[5:3]	rs1′	uimm[2|6]	rs2′	00	C.SW
111	uimm[5:3]	rs1′	uimm[2|6]	rs2′	00	C.FSW *(RV32)*
111	uimm[5:3]	rs1′	uimm[7:6]	rs2′	00	C.SD *(RV64/128)*

Figure 2: Compressed RISC-V Instruction Set