M74ALS138P

6249827 MITSUBISHI (DGTL LOGIC)

91D 12395 D

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

T-66-21-55

DESCRIPTION

The M74ALS138P is a semiconductor integrated circuit of a 3-line-to-8-line decoder/demultiplexer with enable inputs.

FEATURES

- Three types of enable inputs
- 4 to 16 decoder/demultiplexer capability without adding external components
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

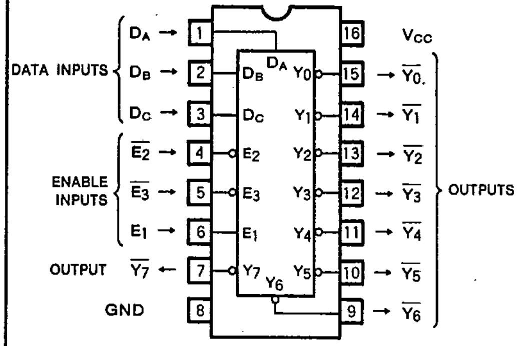
FUNCTIONAL DESCRIPTION

Using as a decoder, give the address in 3-bit binary code on inputs $D_A \sim D_C$, and one output among outputs $\overline{Y_0} \sim \overline{Y_7}$ corresponding to the address is low and the other seven outputs are all high. In this case, enable input E_1 is set high and enable inputs $\overline{E_2}$ and $\overline{E_3}$ are set low. When E_1, $\overline{E_2}$ and $\overline{E_3}$ are in any other condition, the outputs are high irrespective of the status of $D_A \sim D_C$.

When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making E_1, $\overline{E_2}$ and $\overline{E_3}$ the data inputs and $D_A \sim D_C$ the selection inputs.

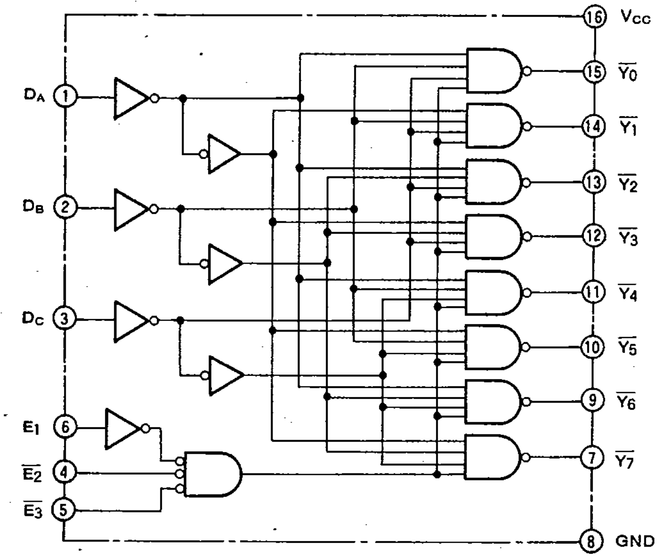
In addition to the features of this device the M74ALS137P and M74ALS131P offer an address latch function and an address register function respectively.

PIN CONFIGURATION (TOP VIEW)


DATA INPUTS
D_A → 1
D_B → 2
D_C → 3
ENABLE INPUTS
E2 → 4
E3 → 5
E1 → 6
OUTPUT Y7 ← 7
GND 8
16 Vcc
15 → Y0
14 → Y1
13 → Y2
12 → Y3
11 → Y4
10 → Y5
9 → Y6
OUTPUTS
D_A D_B D_C E2 E3 E1 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0

Outline 16P4

LOGIC DIAGRAM


16 Vcc
D_A 1
D_B 2
D_C 3
E1 6
E2 4
E3 5
15 Y0
14 Y1
13 Y2
12 Y3
11 Y4
10 Y5
9 Y6
7 Y7
8 GND

M74ALS138P

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

Inputs					Outputs							
E_1	$\overline{E_X}$	D_C	D_B	D_A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1: $\overline{E_X}=\overline{E_2}+\overline{E_3}$

X : irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5～+7	V
V_I	Input voltage		−0.5～+7	V
V_O	Output voltage	High-level state	−0.5～V_{CC}	V
Topr	Operating free-air ambient temperature range		−20～+75	℃
Tstg	Storage temperature range		−65～+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−0.4	mA
I_{OL}	Low-level output current	0		8	mA
Topr	Operating free-air ambient temperature range	−20		+75	℃

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IC}	Input clamp voltage	V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC}=4.5～5.5V, I_{OH}=−0.4mA		V_{CC}−2			V
V_{OL}	Low-level output voltage	V_{CC}=4.5V	I_{OL}=4mA		0.25	0.4	V
			I_{OL}=8mA		0.35	0.5	
I_I	Input current at maximum voltage	V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=5.5V, V_I=0.4V				−0.1	mA
I_O	Output current	V_{CC}=5.5V, V_O=2.25V		−30		−112	mA
I_{CC}	Supply current	V_{CC}=5.5V			5	10	mA

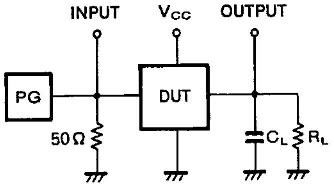
* : All typical values are at V_{CC}=5V, Ta=25°C.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits (Note 2)							Unit
				$V_{CC}=5V$ $C_L=15pF$ $R_L=500\Omega$	$V_{CC}=4.5\sim5.5V$ $C_L=50pF$ $R_L=500\Omega$						
				$T_a=25℃$	$T_a=0\sim70℃$			$T_a=-20\sim+75℃$			
		Inputs	Output	Typ	Min	Typ *	Max	Min	Typ *	Max	
t_{PLH}	Propagation time	D_A, D_B D_C	$\overline{Y}$	12	6	13	22	6	13	23	ns
t_{PHL}				9	6	11	18	6	11	19	
t_{PLH}		E_1, $\overline{E_2}$ $\overline{E_3}$	$\overline{Y}$	10	4	11	17	4	11	18	ns
t_{PHL}				10	5	12	17	5	12	18	

*: All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 2: Measurement circuit


INPUT
V_{CC}
OUTPUT
PG
DUT
50Ω
C_L
R_L

(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

$t_r=2ns$, $t_f=2ns$

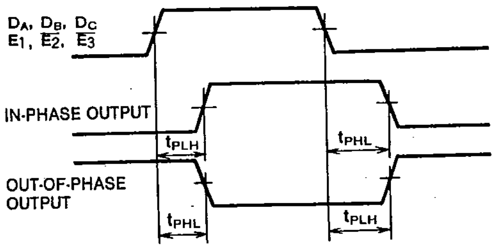
$V_{IH}=3.5V$, $V_{IL}=0.3V$

duty cycle=50%

$Z_O=50\Omega$

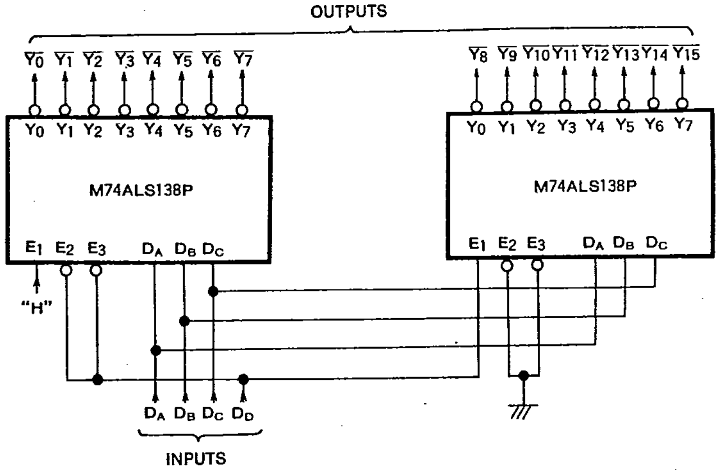
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)


DA, DB, DC
E1, E2, E3
IN-PHASE OUTPUT
tPLH
tPHL
OUT-OF-PHASE OUTPUT
tPHL
tPLH

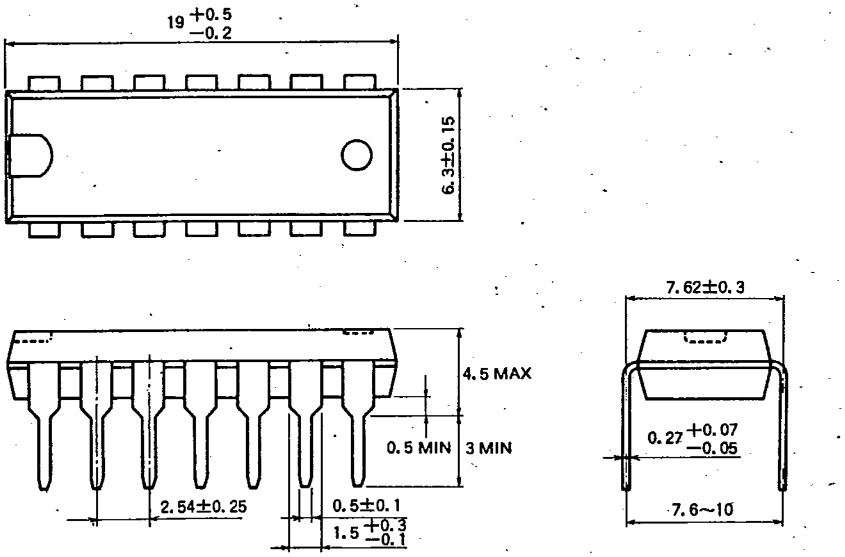
APPLICATION EXAMPLES

4-line to 16-line decoder/demultiplexer


OUTPUTS
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
Y8 Y9 Y10 Y11 Y12 Y13 Y14 Y15
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
M74ALS138P
E1 E2 E3 DA DB DC
"H"
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
M74ALS138P
E1 E2 E3 DA DB DC
DA DB DC DD
INPUTS

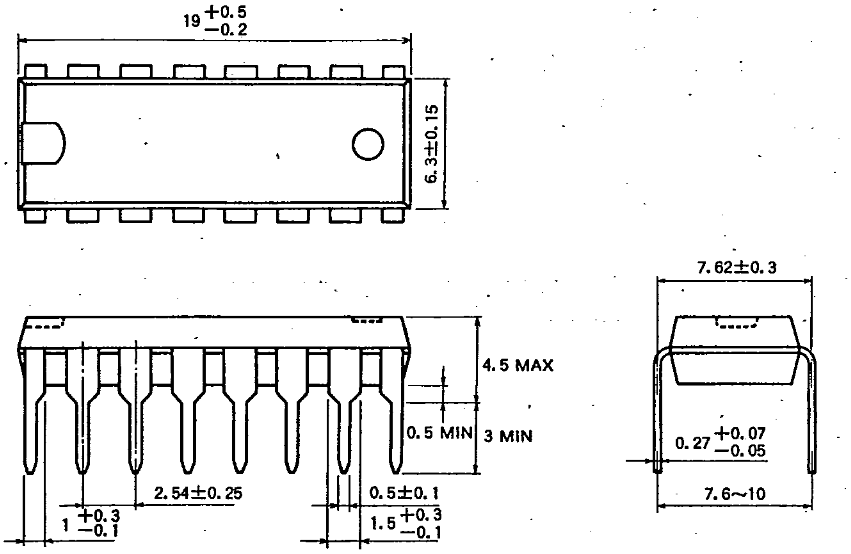
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm


19 +0.5 −0.2
6.3±0.15
7.62±0.3
4.5 MAX
0.5 MIN
3 MIN
0.27 +0.07 −0.05
2.54±0.25
0.5±0.1
1.5 +0.3 −0.1
7.6~10

TYPE 16P4 16-PIN MOLDED PLASTIC DIP

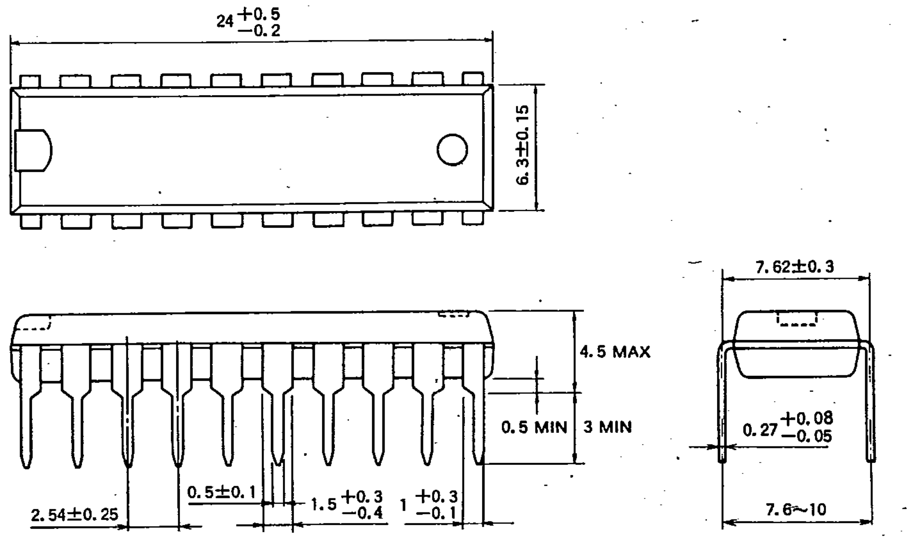
Dimension in mm


19 +0.5 −0.2
6.3±0.15
7.62±0.3
4.5 MAX
0.5 MIN
3 MIN
0.27 +0.07 −0.05
2.54±0.25
0.5±0.1
1 +0.3 −0.1
1.5 +0.3 −0.1
7.6~10

PACKAGE OUTLINES

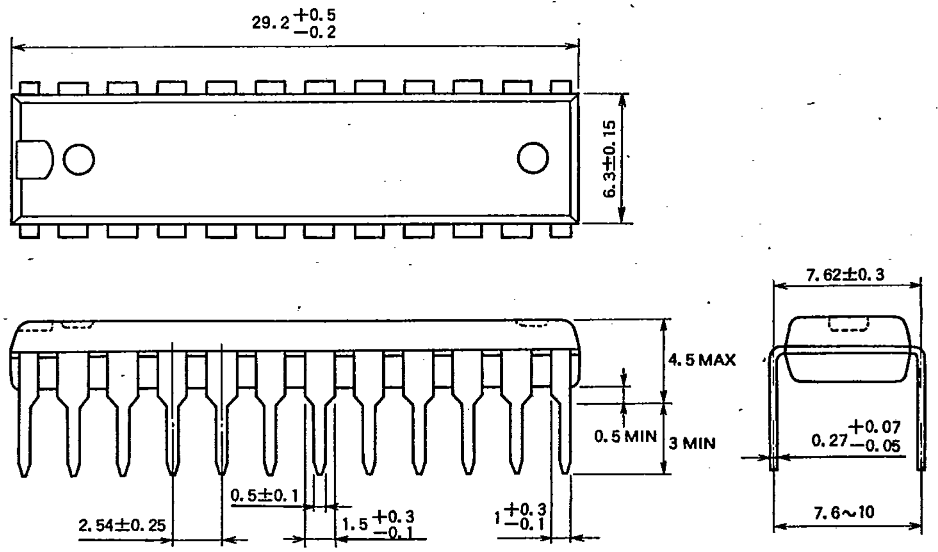
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm


24 +0.5 −0.2
6.3±0.15
7.62±0.3
4.5 MAX
0.5 MIN
3 MIN
0.27 +0.08 −0.05
2.54±0.25
0.5±0.1
1.5 +0.3 −0.4
1 +0.3 −0.1
7.6~10

TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm


29.2 +0.5 −0.2
6.3±0.15
7.62±0.3
4.5 MAX
0.5 MIN
3 MIN
0.27 +0.07 −0.05
0.5±0.1
2.54±0.25
1.5 +0.3 −0.1
1 +0.3 −0.1
7.6~10

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	★	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	★	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	★	Hex Inverter	14P2P
M74ALS05ADP	★★	Hex Inverter with Open Collector Output	14P2P
M74ALS08DP	★	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	★★	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	★	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	★	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	★★	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	★★	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	★★	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	★	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	★★	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	★★	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	★	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	★★	Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	★	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	★★	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	★	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	★★	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	★	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	★★	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	★★	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	★★	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	★	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	★★	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	★★	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	★	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	★	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	★	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	★★	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	★★	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	★★	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	★★	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	★★	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	★★	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	★★	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	★★	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	★★	Hex Noninverting Buffer	14P2P

★: New product ★★: Under development

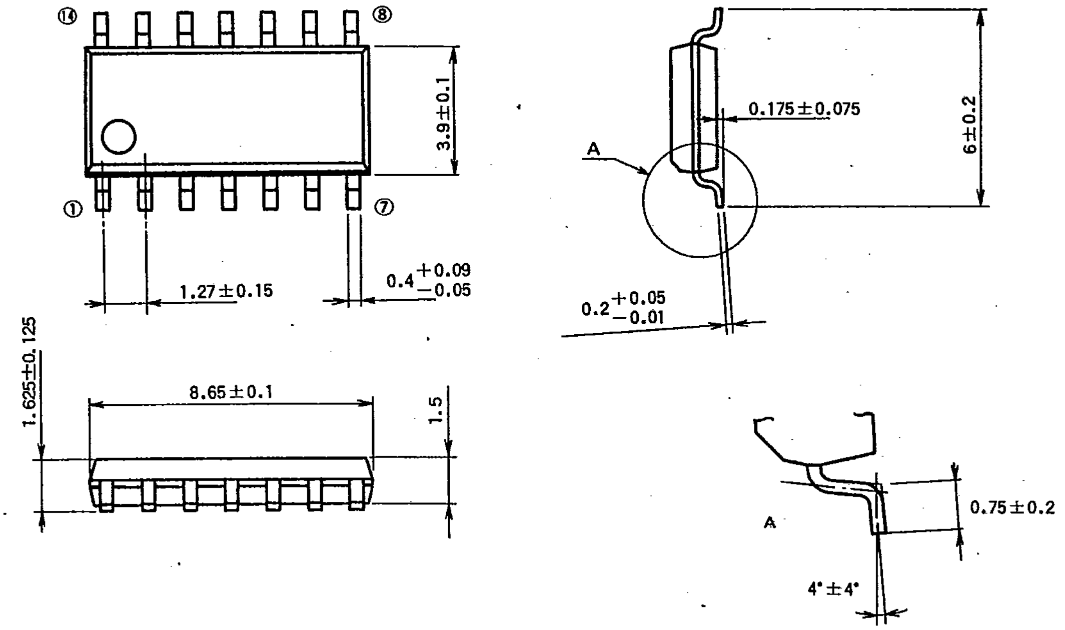
DESCRIPTION

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

T-90-20

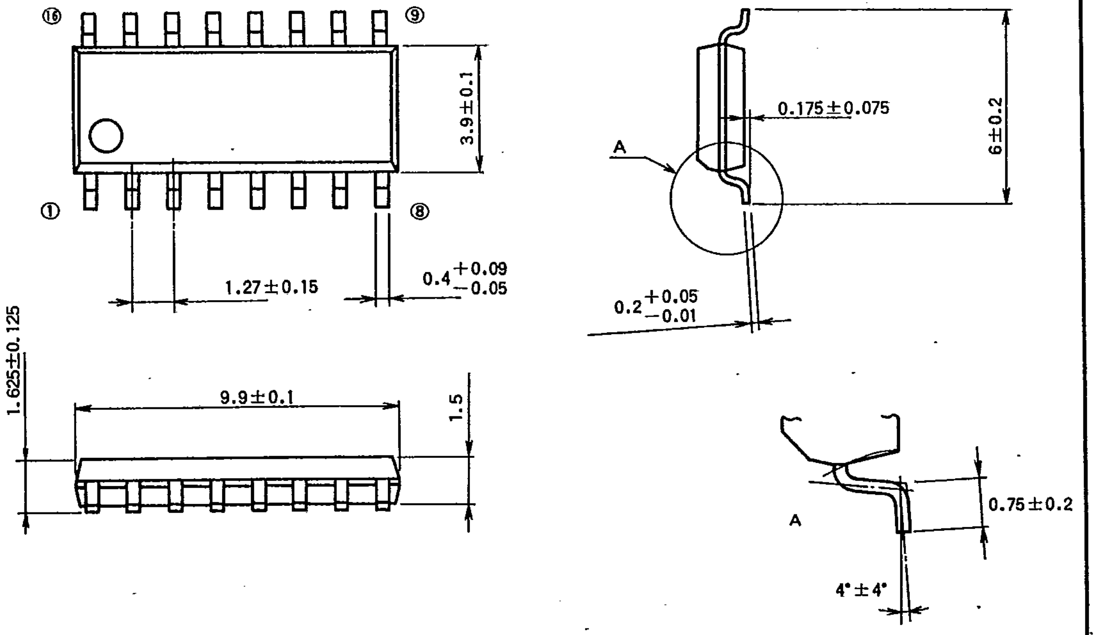
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm


⑭
⑧
①
⑦
3.9±0.1
1.27±0.15
0.4+0.09 −0.05
0.175±0.075
A
6±0.2
0.2+0.05 −0.01
1.625±0.125
8.65±0.1
1.5
0.75±0.2
A
4°±4°

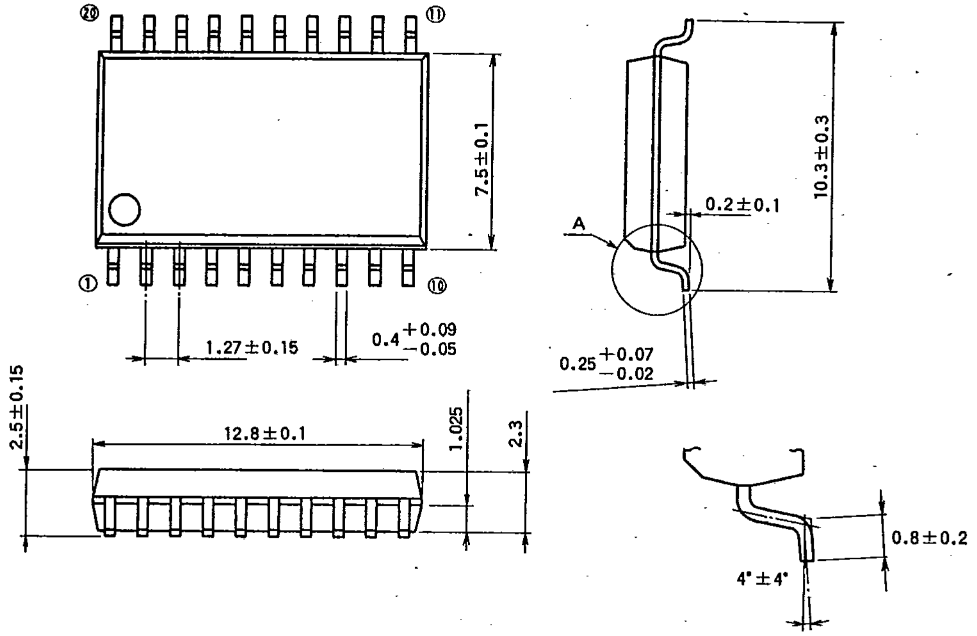
TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm


⑯
⑨
①
⑧
3.9±0.1
1.27±0.15
0.4+0.09 −0.05
0.175±0.075
A
6±0.2
0.2+0.05 −0.01
1.625±0.125
9.9±0.1
1.5
0.75±0.2
A
4°±4°

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP (JEDEC 300mil body)

Dimension in mm


⑳
⑪
①
⑩
7.5±0.1
1.27±0.15
0.4 +0.09 −0.05
2.5±0.15
12.8±0.1
1.025
2.3
10.3±0.3
0.2±0.1
A
0.25 +0.07 −0.02
0.8±0.2
4°±4°