DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS74AP is a semiconductor intergrated circuit containing 2 D-type positive edge-triggered flip-flop circuits with discrete terminals for clock input T, data input D and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Each flip-flop can be used independently.
- Direct set and reset inputs
- Positive edge-triggering
- Q and Q outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change emerges in outputs Q and \overline{Q} in accordance with the function table. By using \overline{S}_D and \overline{R}_D , this IC can be made into a direct R-S flip-flop. When both S_D and R_D are low, $Q = \overline{Q} = \text{high}$. However, when both of them change to high at the same time, the status of Q and \overline{Q} cannot be anticipated. For use as a D-type filip-flop, \overline{S}_D and \overline{R}_D must be kept in high.

FUNCTION TABLE

SD	ĀD	Т	Ð	Q	Q.
L	Н	X	×	н	٦
Н	L	×	×	L	Н
L	L	х	Х	н*	н*
н	н	L	х	Q ⁰	Δ̄o
н	., н	t	н	Н	L
н	н	t	L	L	Н

Note 1: † : Transition from low to high-level

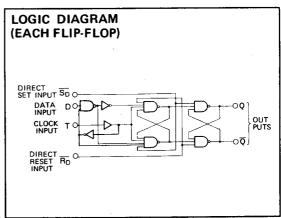
Q⁰: level of Q before the indicated steady-state input conditions were established.

 $\overline{Q^0}$: level of \overline{Q} before the indicated steady-state input conditions were established.

X : Irrelevant

 Nonstable, it will not persist when R_D, S_D inputs return to their inactive (high) level.

PIN CONFIGURATION (TOP VIEW) DIRECT RESET INPUT 1RD -Voc DIRECT RESET INPUT - 2RD DATA INPUT DATA INPUT CLOCK INPUT DIRECT 1 SD 11 CLOCK INPUT DIRECT SET INPUT OUTPUTS OUTPUTS GND Outline 14P4



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75 \, \text{°C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
Vcc	Supply voltage		-0.5~+7	V
VI	Input voltage		-0.5~+5.5	V
Vo	Output voltage	High-level state	-0.5~ V _{CC}	V
Topr	Operating free-air ambient temperature range		-20 - +75	rc
Tstg	Storage temperature range		-65~+150	°C

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RECOMMENDED OPERATING CONDITIONS ($T_a = -20 - +75 \, ^{\circ}C$, unless otherwise noted)

_				Limits			
Symbol	Parameter :			Тур	Max	Unit	
Vcc	Supply voltage			5	5.25	٧	
Юн	High-level output current	V _{OH} ≥ 2.7∨	0		-400	μA	
		V _{OL} ≤0.4∨	0		4	mΑ	
10L	Low-level output current V _{OL} ≤0.5V		0		8	mΑ	

ELECTRICAL CHARACTERISTICS ($T_a = -20 - +75 \,^{\circ}\!\!\!$ C, unless otherwise noted)

			T		Limits			Unit
Symbol	Parameter	ter Test conditions		Min	Тур*	Max	Onit	
VIH	High-level input voltage				2	1		V
VIL	Low-level input voltage						0.8	V
V _{IC}	Input clamp voltage		V _{CC} = 4.75V, I _{IC} = -	V _{CC} = 4.75V, I _{IC} = -18mA		ļ	1.5	V
VoH	High-level output voltage		$V_{\rm CC}$ = 4.75V, V _i =0.8V, V _i =2V $I_{\rm OH}$ = -400 μ A		2.7	3.4		٧
VOL	Low-level output voltage		V _{CC} = 4.75V	I _{OL} = 4mA		0.25	0.4	V
			V _I · 0.8V, V _I =2V	I _{OL} = 8mA		0.35	0.5	V
		D, T					20	
	High-level input current	SD, RD	V _{CC} = 5.25V, V _I = 2.7V			40	μA	
l _{iH}		D, T	5 0511111			0.1		
	Sp. Ro		V _{CC} = 5.25V, V _I =10V				0.2	mΑ
	D, T		051/11/10/11/1			0.4		
· IIE	Low-level input current \$\overline{S}_D, \overline{R}_D\$		V _{CC} = 5.25V. V _I 0.4V			- 0.8	mΑ	
los	Short-circuit output current (Note 2)	V _{CC} 5.25V, V _O = 0V		- 20		100	mΑ
log	Supply current		V _{CC} = 5.25V, (Note 3)			4	8	mΑ

^{* :} All typical values are at V_{CC} = 5V, Ta = 25°C.

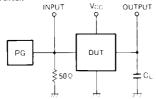
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: Measurement circuit

SWITCHING CHARACTERISTICS (V_{CC} = 5V. T_a = 25 °C. unless otherwise noted)

	0	T disi	Limits			Unit
Symbol	Parameter	Test conditions	Min	Тур	Max	Cint
fmax	Maximum clock frequency		25	50		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation			11	25	ns
tenL	time, from T to Q, Q	C∟≕15pF		11	40	ns
tpLH	Low-to-high-level, high-to-low-level output propagation	(Note 4)		8	25	ns
tehL	time, from S _D , R _D to Q, Q			11	40	ns

Note 4: Measurement circuit



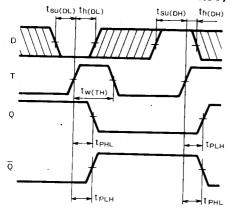
- (1) The pulse generator (PG) has the following characteristics PRR = 1MHz, t_f = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P,P}$, Z_O = 50Ω
- (2) C_L includes probe and jig capacitance.

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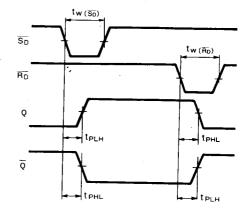
TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25\,$ °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		
			Min	Тур	Max	Unit
t _{w(TH)}	Clock input T high pulse width		25	4		ns
tw(SD, RD)	Direct set and reset inputs SD, RD pulse width		25	4		
t _{su(DH)}	Setup time high D to T					ns
tsu(bL)	Setup time low D to T	- ,	20	10		ns
th(DH)	Hold time high D to T	-	20	8		ns
th(DL)	Hold time low D to T		5	- 5	1 -	ns
(DE)			5	- 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

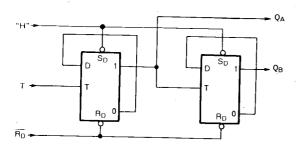


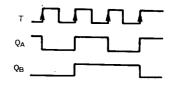
Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.



APPLICATION EXAMPLE

%divider





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