

Lecture 5: **CMOS Transistor Theory**

Assignment for 9/12

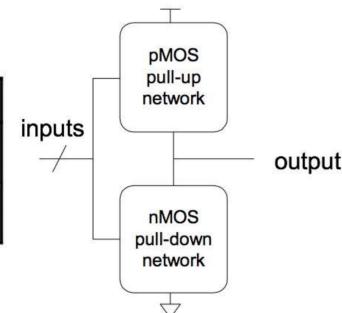
- Complete Lab2
- Text book reading sections 2.1T 2.3 (30 pages)

Quiz 2 Sept. 10, 2019 CPEG460/660

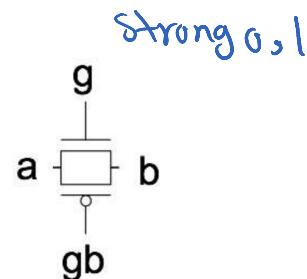
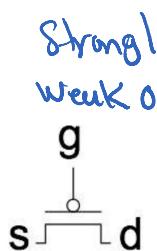
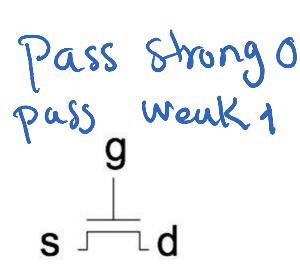
Name: _____

1. Complete the table below. Possible states are ON, OFF, Float and Crowbar.

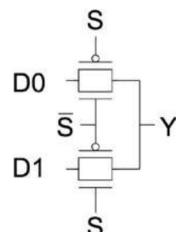
	Pull-up OFF	Pull-up ON
Pull-down OFF	float	on
Pull-down ON	off	x



2. Label the following gates as "passes weak 1", "passes weak 0", "passes strong 1", "passes strong 0". Each circuit gets two labels.

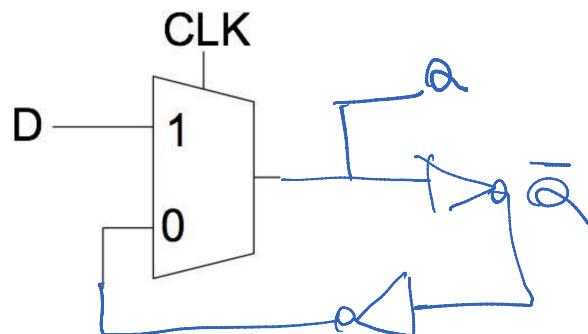


3. Complete the truth table for a 2:1 multiplexer below.



S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

4. Complete schematic for D Latch circuit using only inverters. Label output ports Q and QBar.



Outline

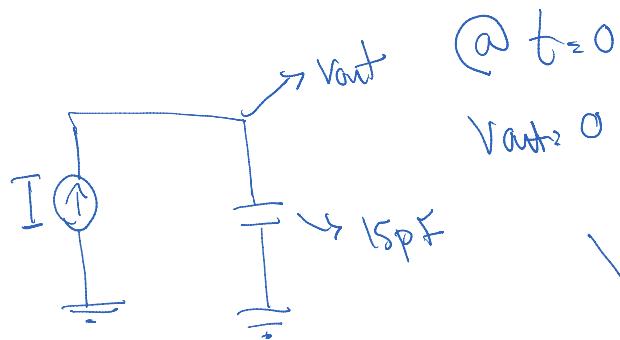
- ❑ Introduction
- ❑ MOS Capacitor
- ❑ nMOS I-V Characteristics
- ❑ pMOS I-V Characteristics
- ❑ Gate and Diffusion Capacitance

Introduction

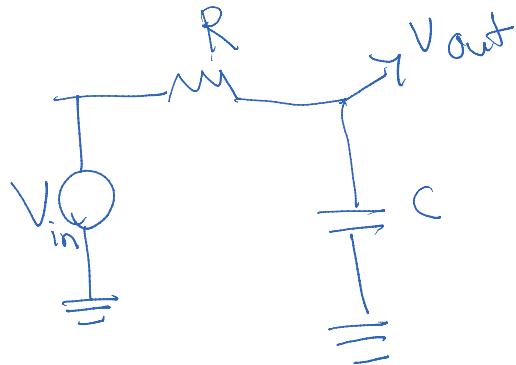
- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
 - Depends on terminal voltages
 - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
 - $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C/I) \Delta V$
 - Capacitance and current determine speed



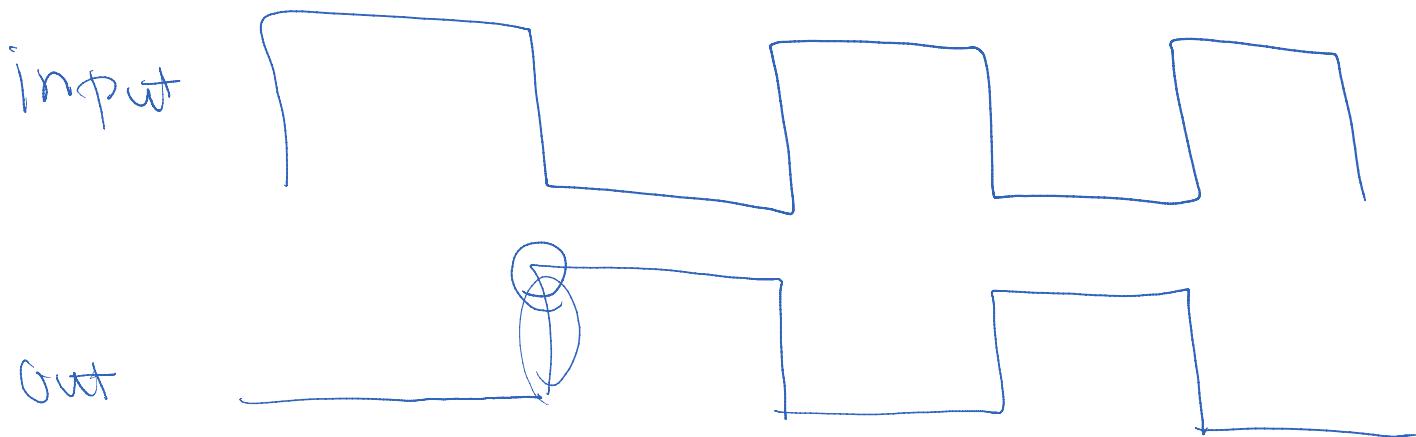
$$I = C \frac{\Delta V}{\Delta t} \Rightarrow \Delta V = \frac{\Delta t \cdot I}{C}$$



$$V = \frac{t \cdot I}{C}$$



$$V_{out} = V_{in} \cdot R \cdot C$$



MOS Capacitor

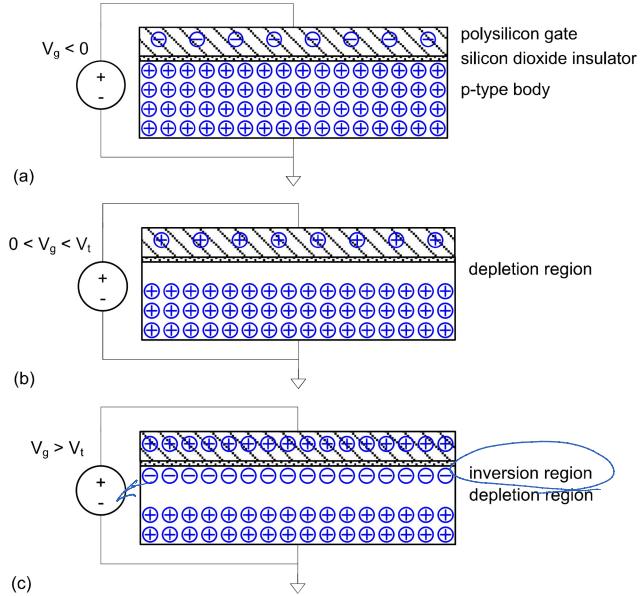
- Gate and body form MOS capacitor

- Operating modes

- Accumulation
- Depletion
- Inversion

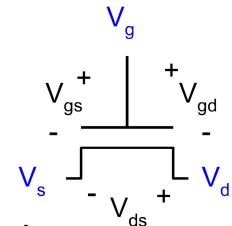
(cut off)

long sat



Terminal Voltages

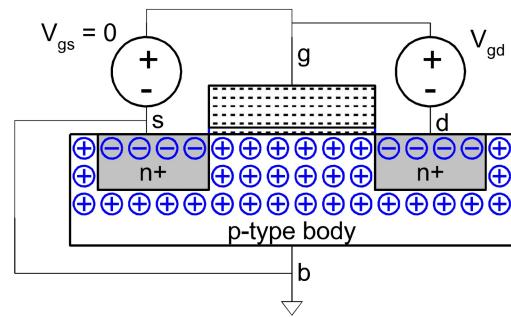
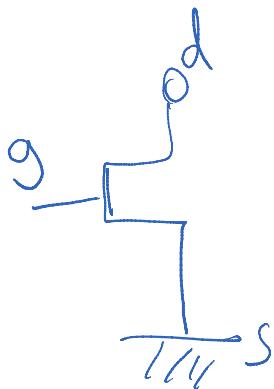
- ❑ Mode of operation depends on V_g , V_d , V_s
 - $V_{gs} = V_g - V_s$
 - $V_{gd} = V_g - V_d$
 - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$



- ❑ Source and drain are symmetric diffusion terminals
 - By convention, source is terminal at lower voltage
 - Hence $V_{ds} \geq 0$
- ❑ nMOS body is grounded. First assume source is 0 too.
- ❑ Three regions of operation
 - *Cutoff*
 - *Linear*
 - *Saturation*

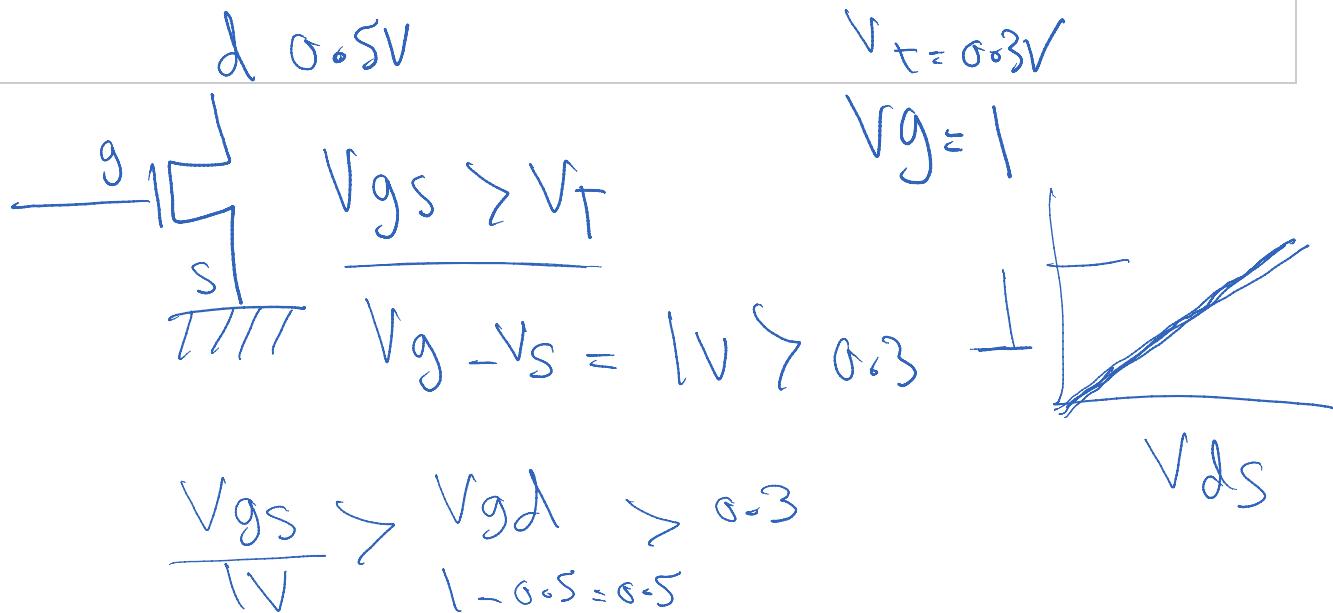
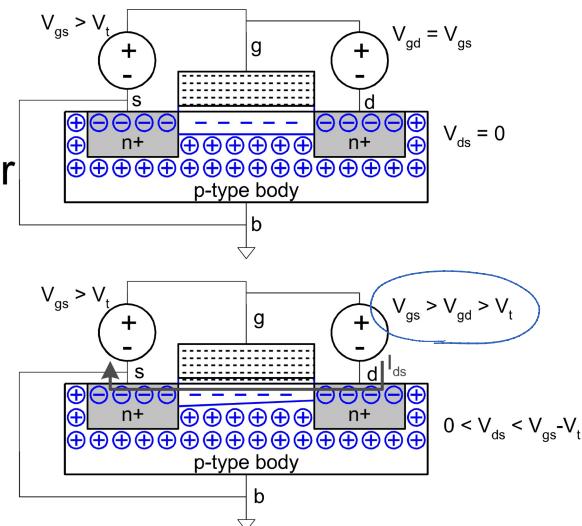
nMOS Cutoff

- ❑ No channel
- ❑ $I_{ds} \approx 0$



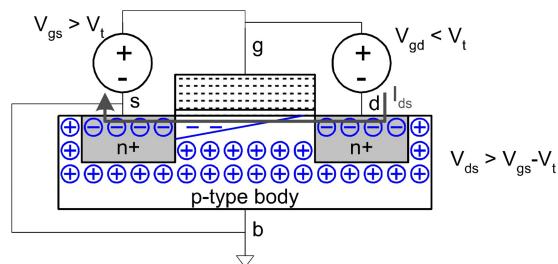
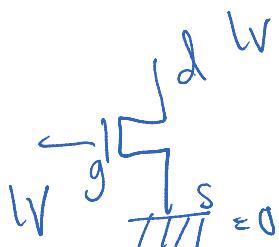
nMOS Linear

- Channel forms
- Current flows from d to s
 - e⁻ from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current *saturates*
- Similar to current source



$$V_{ds} = V - 0 = V$$

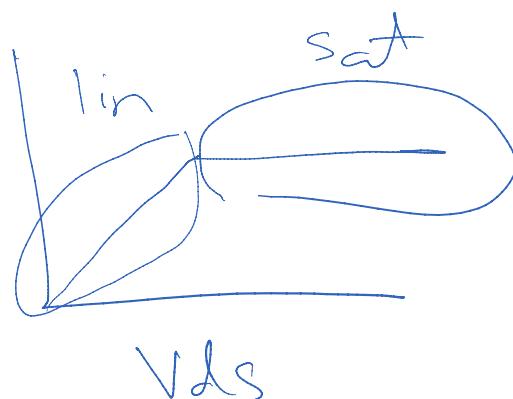
$$V_t \approx 0.3V$$

$$V_{gs} \approx V - V_t \approx V$$

$$V_{gs} - V_t = 0.7V$$

$$V_{ds} > V_{gs} - V_t$$

I



I-V Characteristics

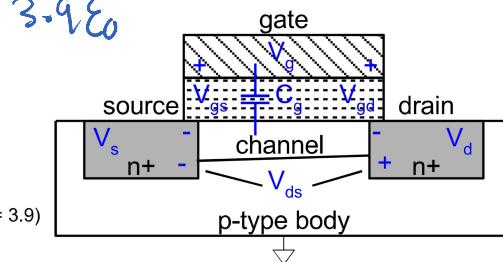
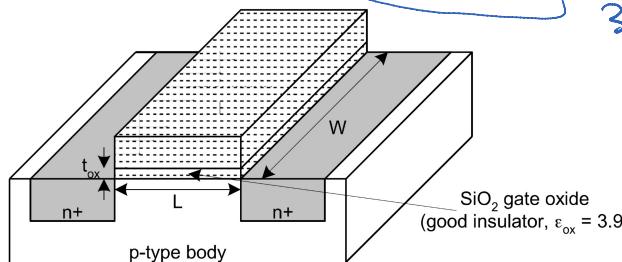
- In Linear region, I_{ds} depends on
 - How much charge is in the channel?
 - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversions
 - Gate - oxide - channel

$$\square Q_{\text{channel}} = C_g \cdot (V_{gc} - V_T)$$

$$\square C_g = K_{ox} \epsilon_0 \frac{WL}{t_{ox}} = \epsilon_{ox} \frac{WL}{t_{ox}} = C_{ox} W \cdot L$$



$$V_{gc} = V_g - V_C$$

$$= V_{gs} - \frac{V_{ds}}{2}$$

$$V_C = \frac{(V_S + V_D)}{2} = V_S + \frac{V_{ds}}{2}$$

Permittivity of free space

$$\epsilon_0 = 8.85 \times 10^{-14} \frac{\text{F}}{\text{cm}}$$

Permittivity of SiO_2

$$K_{ox} = 3.9$$

$$\epsilon_{ox} = K_{ox} \epsilon_0 = 3.9 \epsilon_0$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

fixed based on tech

Carrier velocity

- Charge is carried by e-
 - Electrons are propelled by the lateral electric field between source and drain
 - $E = \frac{V_{ds}}{L}$
 - Carrier velocity v proportional to lateral E-field
 - $v = \mu \cdot E = \mu \cdot \frac{V_{ds}}{L}$
 - Time for carrier to cross channel:
 - $t = \frac{L}{v} \Rightarrow \frac{L}{\mu \cdot \frac{V_{ds}}{L}}$
- μ = mobility

nMOS Linear I-V

□ Now we know

- How much charge Q_{channel} is in the channel
- How much time t each carrier takes to cross

$$\begin{aligned}
 I_{ds} &= \frac{Q_{\text{channel}}}{t} = \frac{Q_{\text{channel}}}{L \cdot V} \\
 &= \left(M \cdot C_{\text{ox}} \cdot \frac{W}{L} \right) \left(V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds} \\
 &= \beta \left(V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds}
 \end{aligned}$$

$$\beta = M \cdot C_{\text{ox}} \cdot \frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
 - When $V_{ds} > V_{dsat} = \textcircled{V_{GT}}$
- Now drain voltage no longer increases current

$$\begin{aligned}I_{ds} &= \frac{\beta}{2} (V_{gs} - V_t)^2 \\&= \underbrace{M \cdot C_{ox} \cdot \frac{W}{L}}_{\beta} \textcircled{V_{GT}^2}\end{aligned}$$

nMOS I-V Summary

- Shockley 1st order transistor models

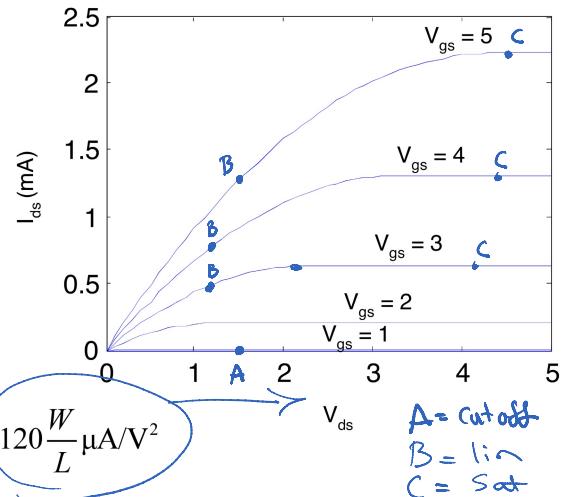
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \end{cases}$$

cutoff
linear
saturation

Example

- We will be using a $0.6 \mu\text{m}$ process for your project
 - From AMI Semiconductor
 - $t_{\text{ox}} = 100 \text{ \AA}$
 - $\mu = 350 \text{ cm}^2/\text{V}\cdot\text{s}$
 - $V_t = 0.7 \text{ V}$
- Plot I_{ds} vs. V_{ds}
 - $V_{\text{gs}} = 0, 1, 2, 3, 4, 5$
 - Use $W/L = 4/2 \lambda$

$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left(\frac{3.9 \times 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left(\frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

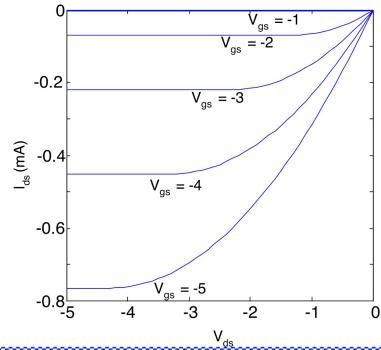


$$C_{\text{ox}} = K_{\text{ox}} \frac{\epsilon_0}{t_{\text{ox}}}$$

pMOS I-V

- All dopings and voltages are inverted for pMOS
 - Source is the more positive terminal
- Mobility μ_p is determined by holes
 - Typically 2-3x lower than that of electrons μ_n
 - $120 \text{ cm}^2/\text{V}\cdot\text{s}$ in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
 - In this class, assume

$$\mu_n / \mu_p = 3$$

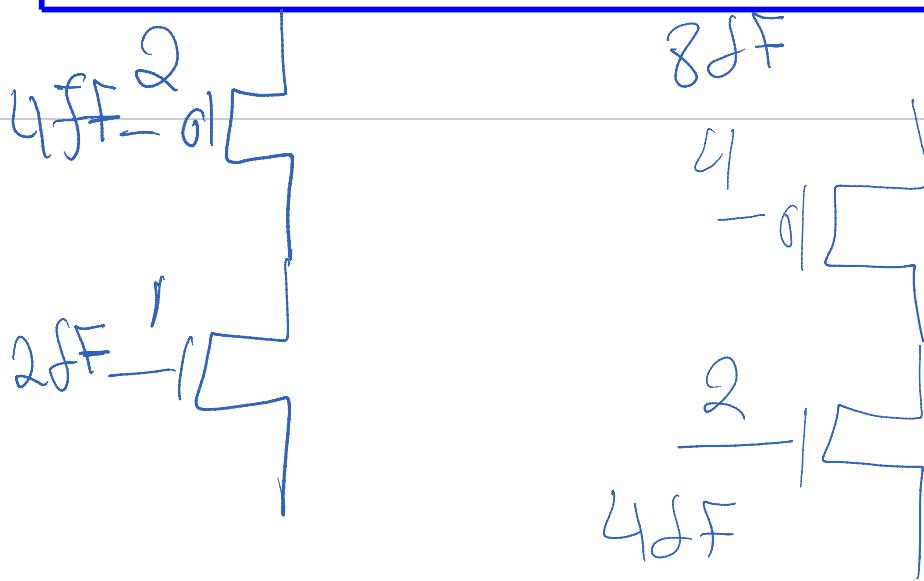
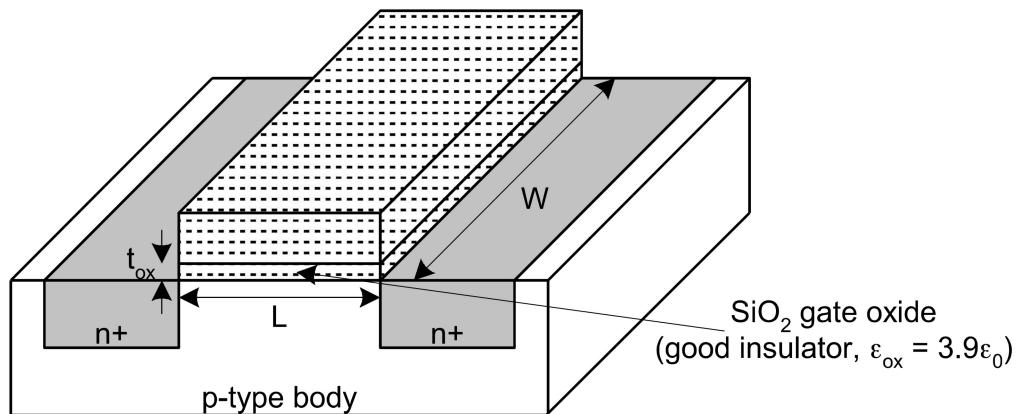


Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
 - Creates channel charge necessary for operation
- Source and drain have capacitance to body
 - Across reverse-biased diodes
 - Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance

- Approximate channel as connected to source
- $C_{gs} = \epsilon_{ox} WL/t_{ox} = C_{ox}WL = C_{\text{permicron}}W$
- $C_{\text{permicron}}$ is typically about $2 \text{ fF}/\mu\text{m}$



Diffusion Capacitance

- ❑ C_{sb}, C_{db}
- ❑ Undesirable, called parasitic capacitance
- ❑ Capacitance depends on area and perimeter
 - Use small diffusion nodes
 - Comparable to C_g for contacted diff
 - $\frac{1}{2} C_g$ for uncontacted
 - Varies with process

