LAB2 – Inverter Tutorial: Test Bench Creation and Transient Simulation

Objectives:
- learn to create a test bench for testing schematics (steps 1-2)
- learn to perform a transient simulation using the SpectreS simulator (steps 3-7)
- learn to verify operation of schematic (steps 3-7)
- learn to save and recall simulator states (step 8)

Assumptions:
- Working Cadence VM and VMWARE software (Lab 1)
- Schematic for inverter has been completed (Lab 1)

*1.* ***Start cadence virtual machine, after connecting to the VPN***

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virtuoso &
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2. ***Creating the TestFixture (testbench)***

- In the Library Manager, click on your "**lab1**" Library.
- From the Library Manager Menu choose: **File→ New → Cellview...**
- Fill it as shown below, to create a new cell called: **inv_tb**
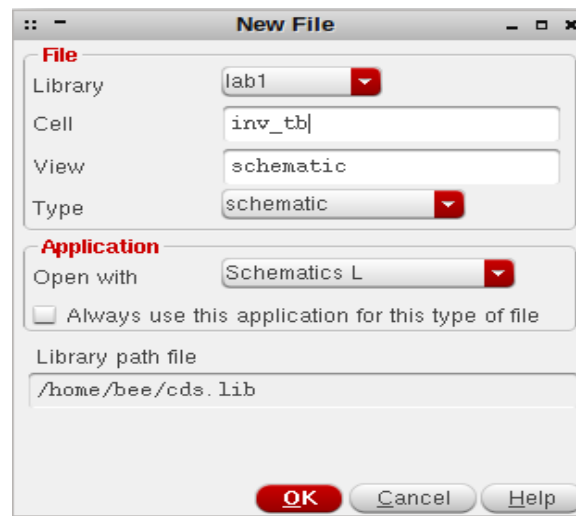
- Click **OK**. A new Composer-Schematic window appears.
- Add the components below by using the same technique you used when creating the inverter schematic in the previous lab.
- From the menu choose: **ADD->Instance**   (or simply press **i**)
- Using the **component browser**, "instance" the following parts onto your schematic, from the following libiraries:

    - vdd (**Library**: analogLib, **vdd**)
    - gnd (**Library**: analogLib, **gnd**)
    - DC Source (**Library**: analogLib, **vdc**)
    - pulsed voltage source (**Library**: analogLib, **vpulse**)
    - capacitor (**Library**: analogLib, **cap**)
- Place them on your schematic in the arrangement shown in the figure below:
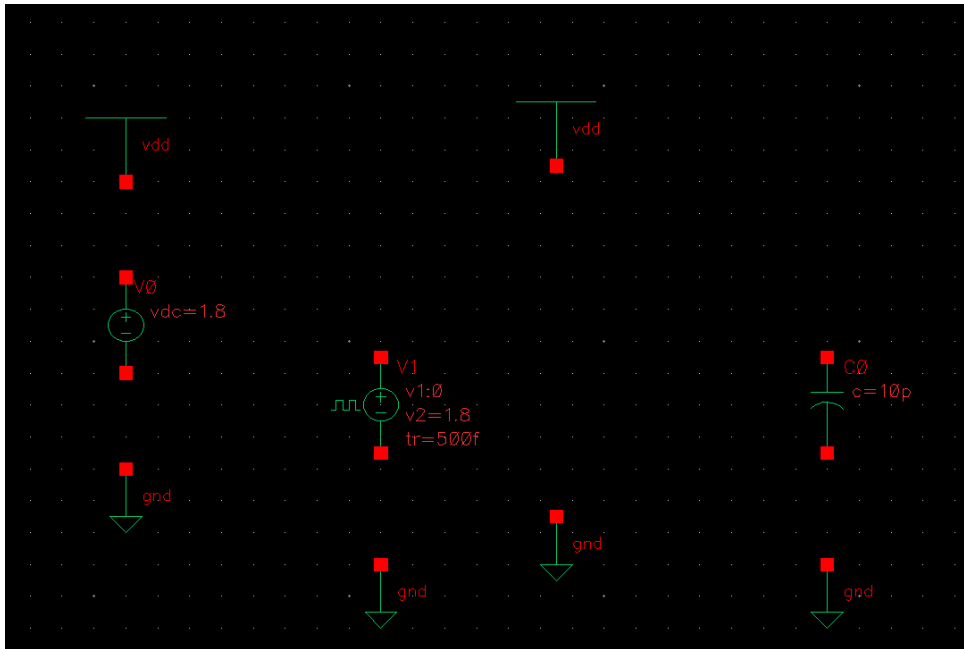
The final component to instance is the **inverter** symbol you created in the last lab.
- From the menu choose: **Create->Instance**   (or simply press **i**)
- In the component browser, choose the library: **Lab1**
- Select the "inv" part to instance, and you will be able to add your inverter's symbol to the schematic
- Press <esc> after placing the inverter on your schematic.
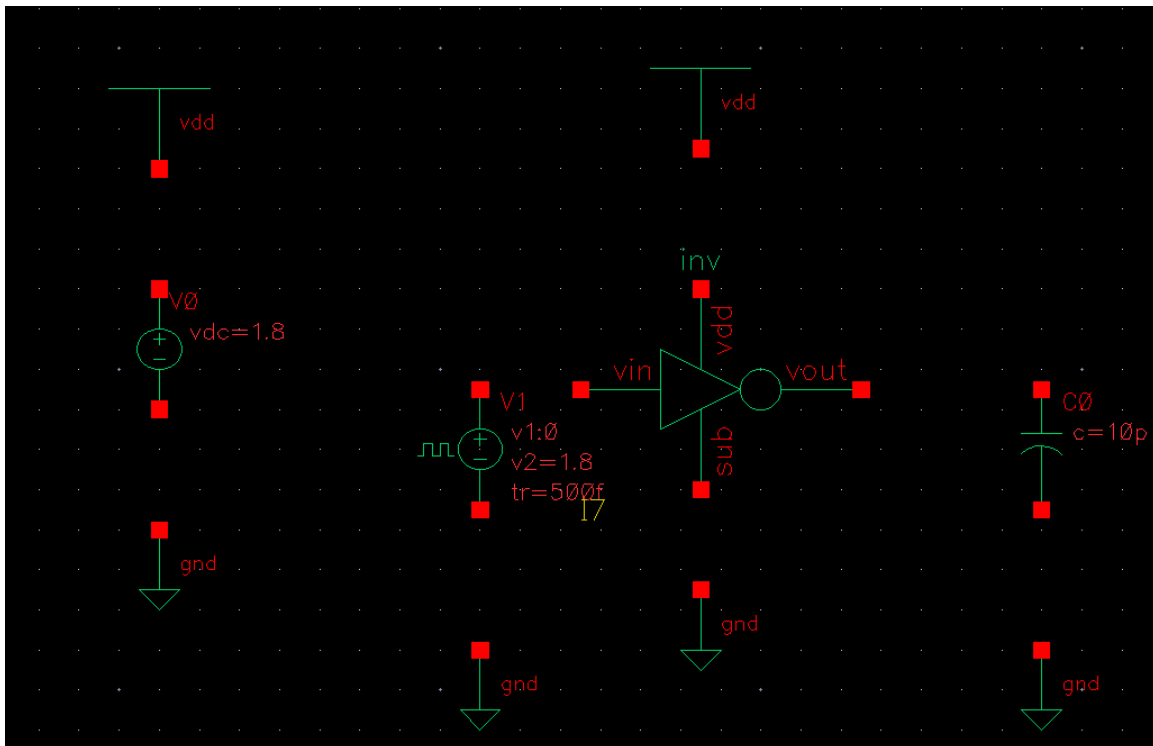
- Connect wires to the part terminals as follows:
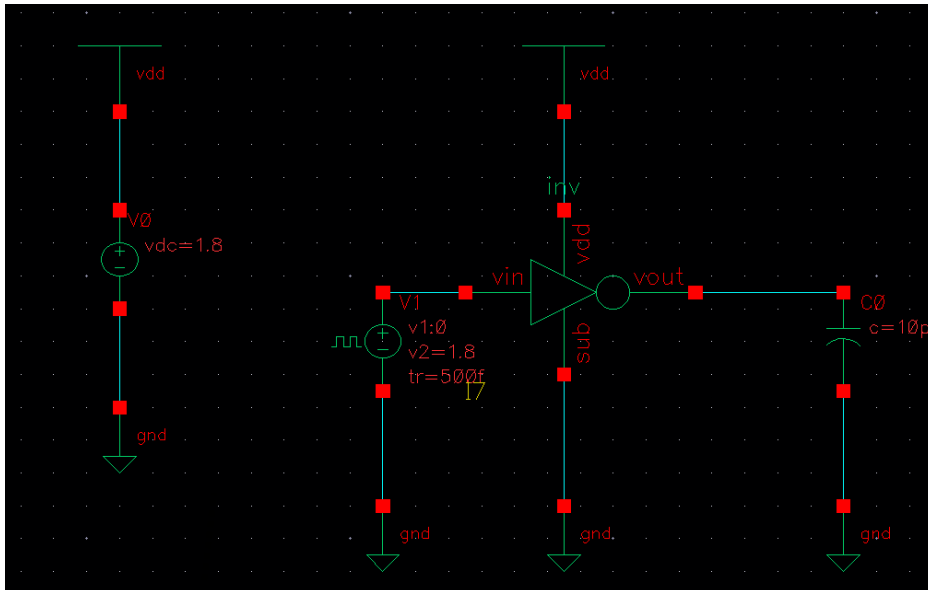
- Click on the **DC Voltage source**, and press the letter "**q**" on your keyboard. This will bring up the object's properties.
- In the property list, set the "**DC Voltage**" property to "**1.8**", and then press OK.

Repeat the above procedure to adjust the properties of the parts below.
-Pulsed Voltage Source:

       Voltage 1 = 0,
       Voltage 2 = 1.8,
       Delay time = 0,
       Rise time = 500f,
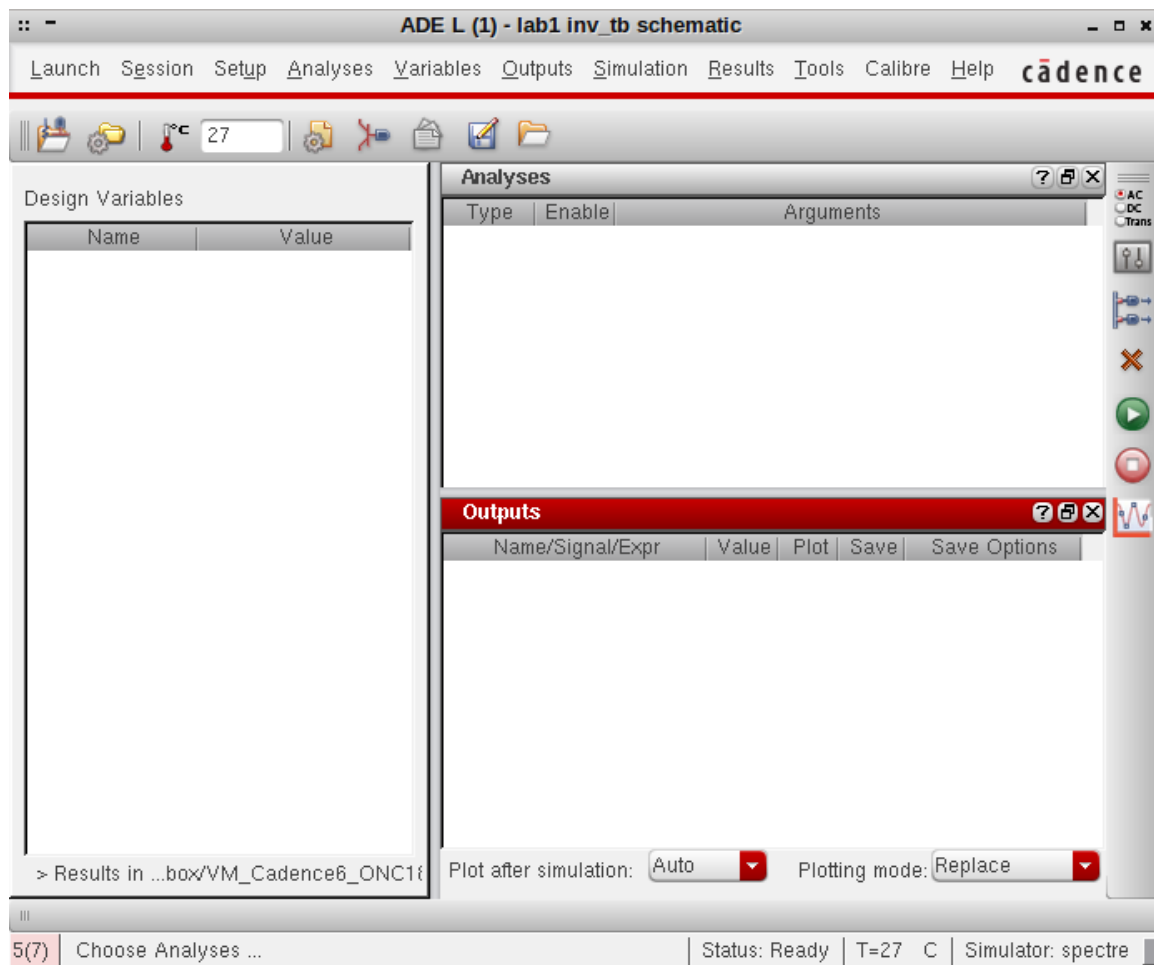   Fall time = 500f,
       Pulse width = 25u,
       Period = 50u.

-capacitor:

       Capacitance=10p

- Upon completion, press the "check and save" icon from the toolbar. Or use the menu to click Design->Check_and_Save

3. Initializing the Simulation Environment

- In the schematic window, from the menu select Launch->ADE L. In a few seconds, the Analog Artist Simulation window appears, as shown here.


4. Performing a Transient Analysis
- From the menu choose Analysis →Choose...
- The form appears.
- Select the "**tran150u**" analysis
- *Note: trans analysis: This provides the transient output response of the circuit with respect to time. The user specifies the time period and the time variant input wave-form while the simulator calculates the output response.*
- Set stop time = 150u as shown in the figure *(this will allow 3 pulses from our pulsed source).*
- **Make sure Enabled is checked**
- Press OK
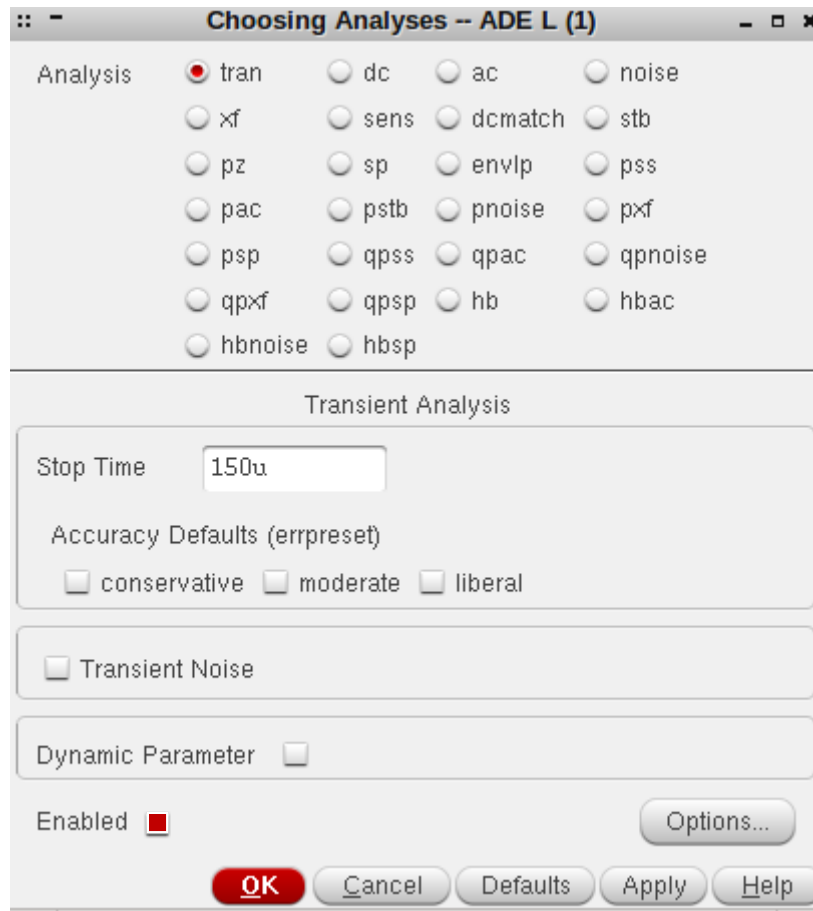
Saving and Plotting Simulation Data

- We wish to select the output **WIRE** whose voltage we wish the simulator to record vs. time.
- This is done from the simulator's menu by choosing:
- **Outputs → To be Plotted → Select on Schematic**.
- The schematic window is moved into the forefront. Now, "click" on the **NET** (aka wire) you wish to have plotted.
- Click on the wire (aka NET), to the left of the inverter (the **input** net)
- Then click on the wire to the right of the inverter (the **output** net)
- Press <**esc**> to end "net selection" mode

- Move your schematic window so that you can see the "simulation" window from before. You will notice in the "**Outputs**" region, the two NET's you selected will be listed (as in the figure below)
- *NOTE: your net name's may be different then the ones in this document.*
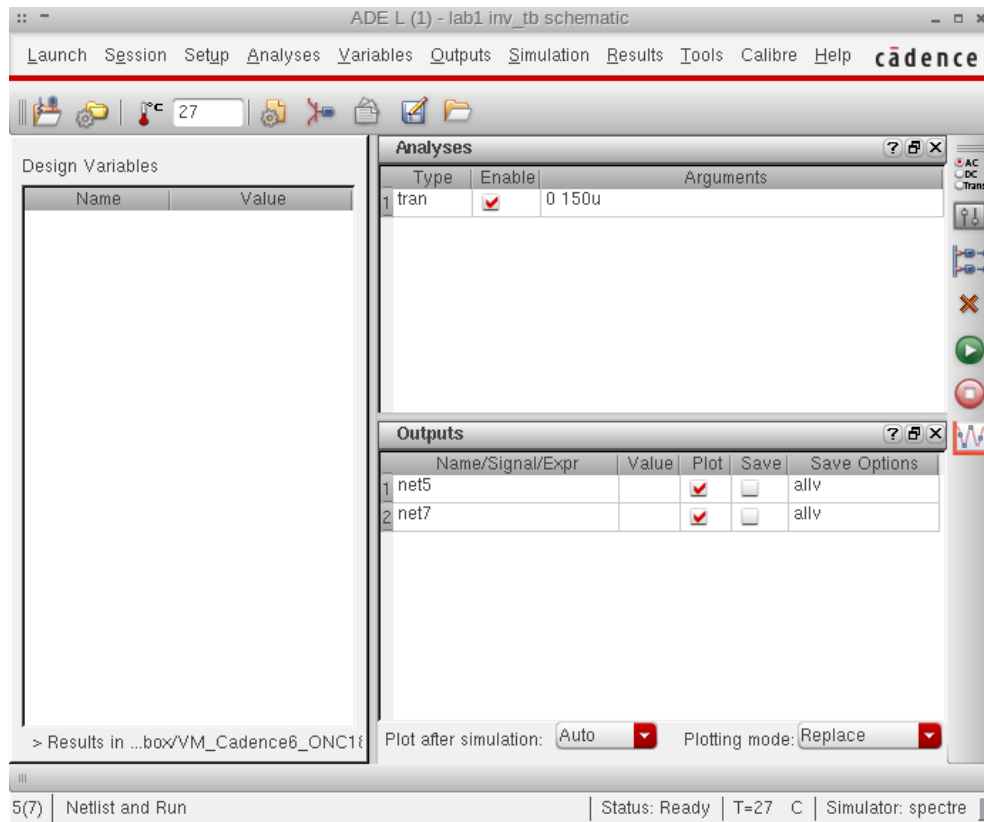
Running the Simulation – The Waveform Window

- Click on the **Simulation**->**Netlist and Run** icon (little green play button icon in the simulator control window).
- When it is complete, the plots are shown automatically.

The two plots will be overlapped on top of one another. You must separate them by choosing from the plot menu: **Graph->Split All Strips**
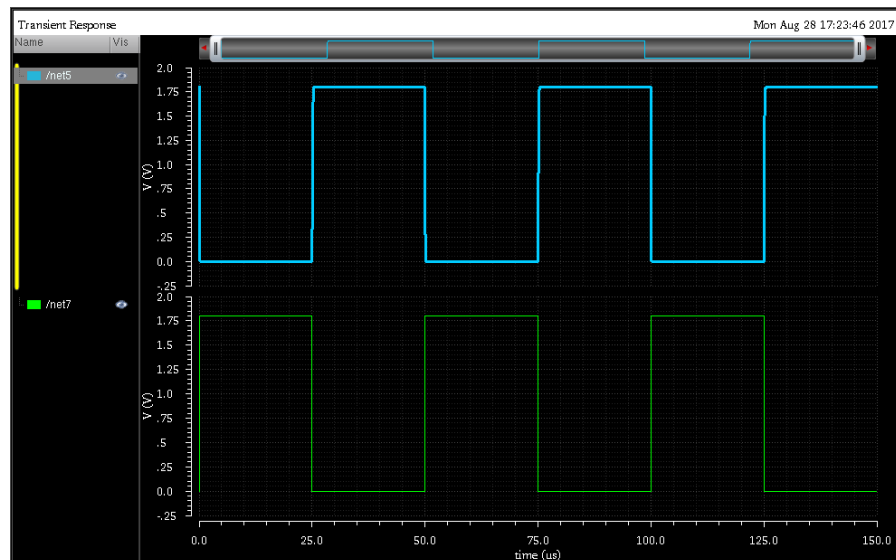
- You may zoom in, using "z" key and drawing a box around the area of the graph you wish to zoom into. By zooming, you can see the charge/discharge of the capacitor in the output net.

Saving Simulation State

- Once you have completed a complicated simulation, you may wish to "save" all of your simulation settings. From the simulator menu, choose**: Session->Save State…**

- Give the "state" of the simulator a name that is meaningful like: **inv_transient_simulation** as in the graphic below:
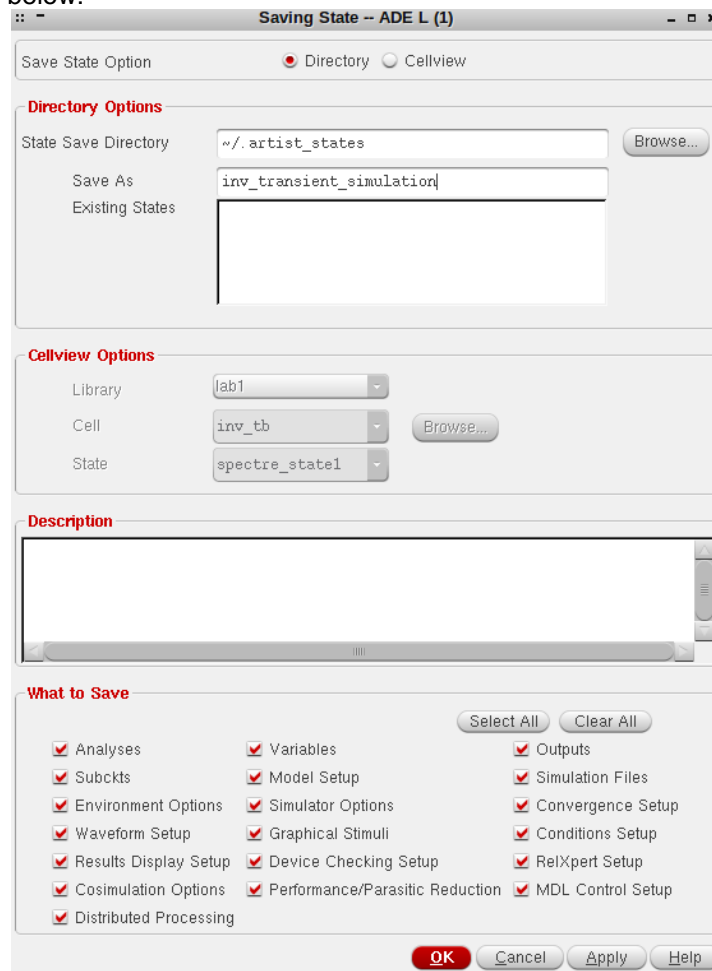
- Later, if you wish to recall the saved state, choose: Session->Load State… and you will be show all of the simulation states for this cell (inv_tb).