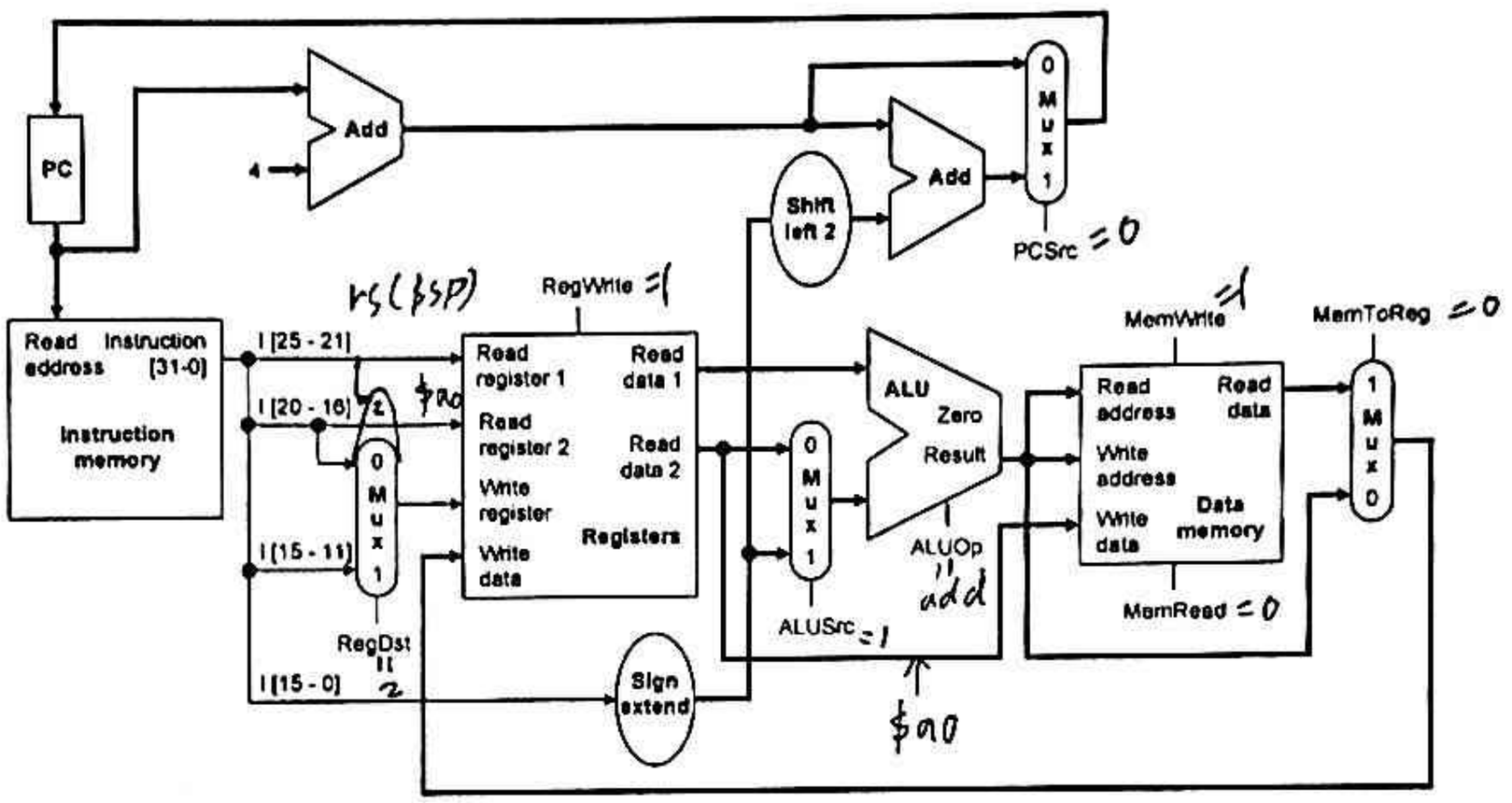
CPEG 323 Practice Final Exam

Question 1: Single-cycle Datapath and Performance



Part 1)

Consider the above single-cycle datapath. We want to implement a new I-type MIPS instruction ***push $rt*** which grows the stack by 4 bytes and stores $rt onto the stack.

Example: The instruction `push $a0` is equivalent to the MIPS instruction sequence: `addi $sp, $sp, -4; sw $a0, 0($sp)`

Question: Make the fewest possible changes to the given datapath to implement the push instruction. Be sure to indicate the value of all control signals, including any new control signals.

Part (2)

The latencies of the component of the single-cycle datapath from Problem 1 are as follows: Memory read/write: 200ps, Register read: 150 ps, Register write: 100ps, ALU: 250ps (all other components have negligible latency, 1 ps = 10^{-12} seconds).

(a) If the clock-cycle time is made as small as possible, what is the clock frequency?

clock-cycle time = latency of the slowest instruction (lw here)

$lw = MR + RR + ALU + MR + RW = 200 + 150 + 250 + 200 + 100 = 900\ ps$

$$\text{frequency} = \frac{1}{\text{clock-cycle time}} = \frac{1}{900 \times 10^{-12}} = \frac{10}{9}\ GHz$$

(b) We have to choose between two performance optimizations: either a new ALU (latency 200 ps) or a new memory (latency 100 ps). Which would be a better choice? Justify your answer.

new ALU: used one time: 250-200 = 50 ps speed up

new memory: used two times (2 MR): 2×(200-100) = 200 ps speed up

new memory is better!