

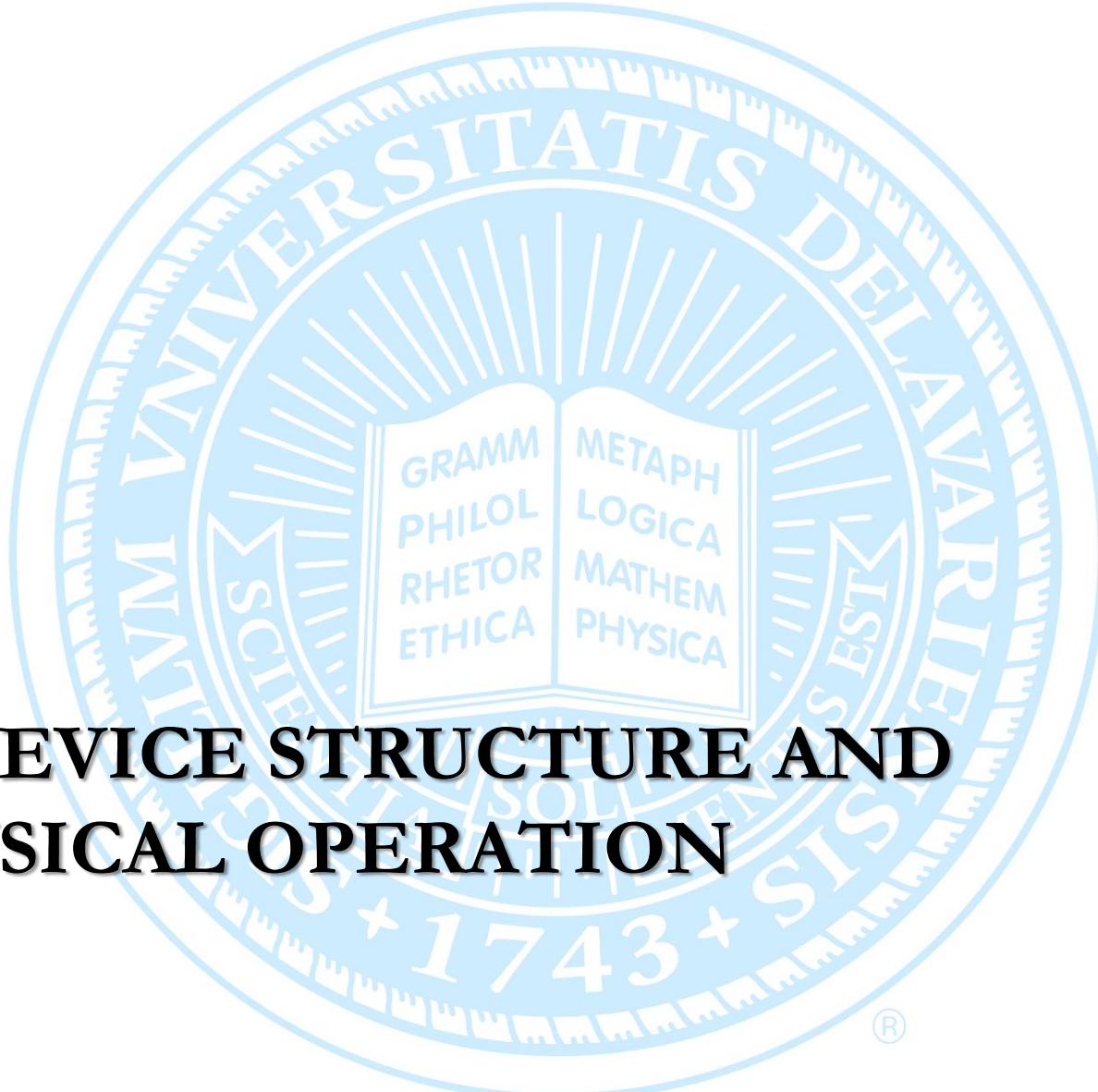
UNIVERSITY *of* DELAWARE
Chapter 5
MOS Field Effect Transistors
(MOSFETs)





IN THIS CHAPTER YOU WILL LEARN

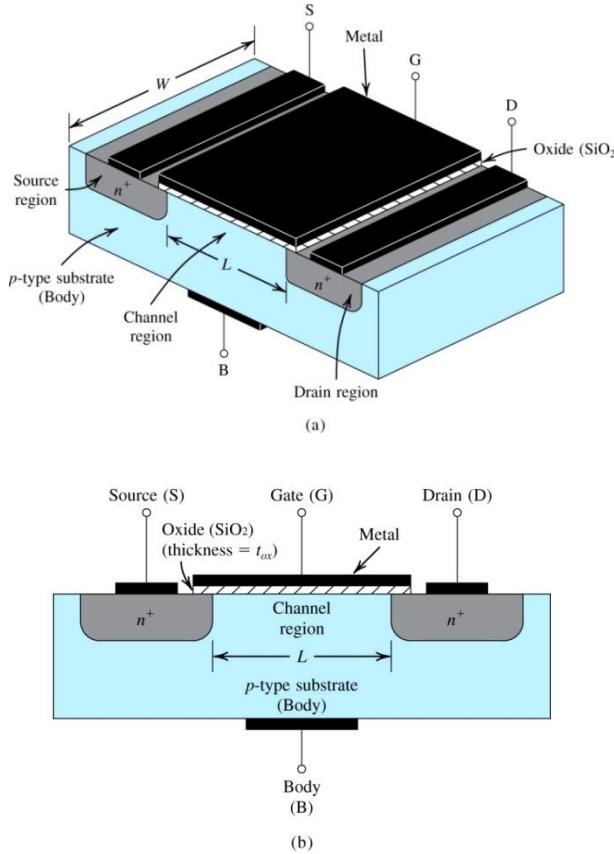
1. The physical structure of the MOS transistor and how it works.
2. How the voltage between two terminals of the transistor controls the current that flows through the third terminal, and the equations that describe these current-voltage characteristics.
3. How to analyze and design circuits that contain MOS transistors, resistors, and dc sources.



5.1 DEVICE STRUCTURE AND PHYSICAL OPERATION



n-channel enhancement-type MOSFET.

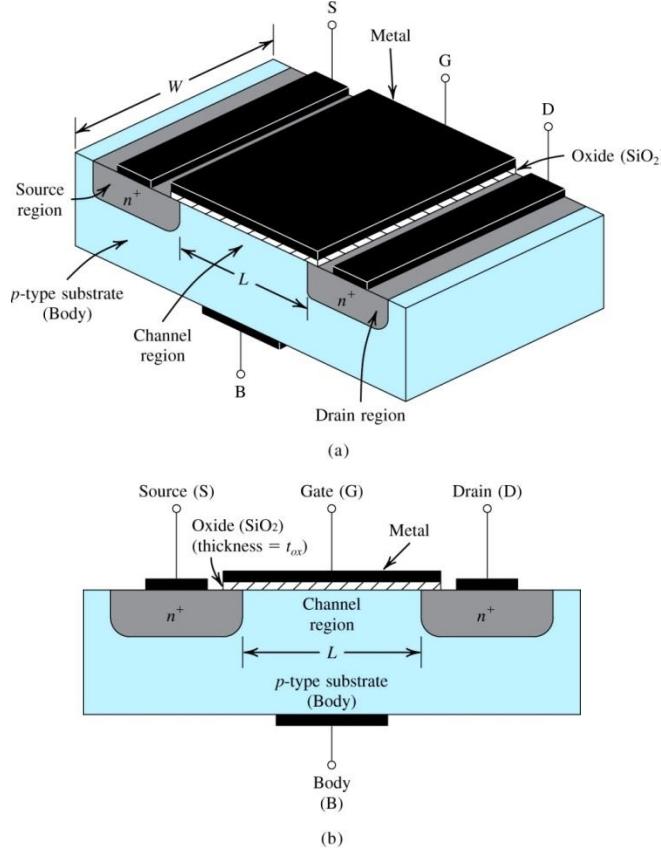


The transistor is fabricated on a *p*-type substrate, which is a single-crystal silicon wafer that provides physical support for the device. Two heavily doped *n*-type regions, indicated in the figure as the *n*⁺ **source** and the *n*⁺ **drain** regions, are created in the substrate. A thin layer of silicon dioxide (SiO_2), which is an excellent electrical insulator is grown on the surface of the substrate, covering the area the source and drain regions. Metal is deposited on top of the oxide to form the **gate** electrode of the device. Metal contacts are also made to the source, the drain, and the substrate, also known as the **body**.

Figure 5.1 Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross section. Typically $L = 0.03 \text{ } \mu\text{m}$ to $1 \text{ } \mu\text{m}$, $W = 0.1 \text{ } \mu\text{m}$ to $100 \text{ } \mu\text{m}$, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm



n-channel enhancement-type MOSFET.



The transistor has a width, W , of $0.1 \mu\text{m}$ to $100 \mu\text{m}$ and a length, L , of $0.03 \mu\text{m}$ to $1 \mu\text{m}$ typically.

The typical thickness of the silicon dioxide (SiO_2) layer, t_{ox} , is 1 nm to 10 nm .

Figure 5.1 Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross section. Typically $L = 0.03 \mu\text{m}$ to $1 \mu\text{m}$, $W = 0.1 \mu\text{m}$ to $100 \mu\text{m}$, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm



Operation under Zero Bias

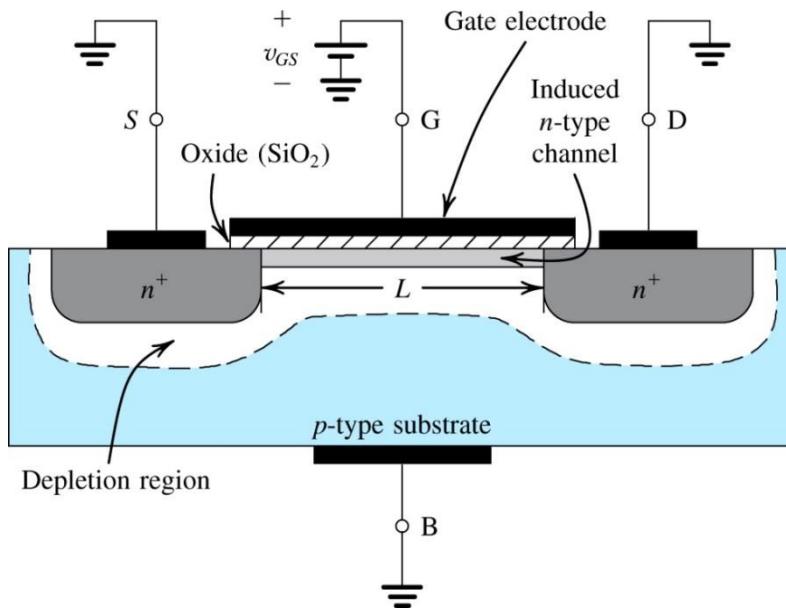


Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the *pn* junction between the n⁺ drain region and the p-type substrate, and the other diode is formed by the *pn* junction between the p-type substrate and the n⁺ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of $10^{12} \Omega$).



Creating a channel for current flow

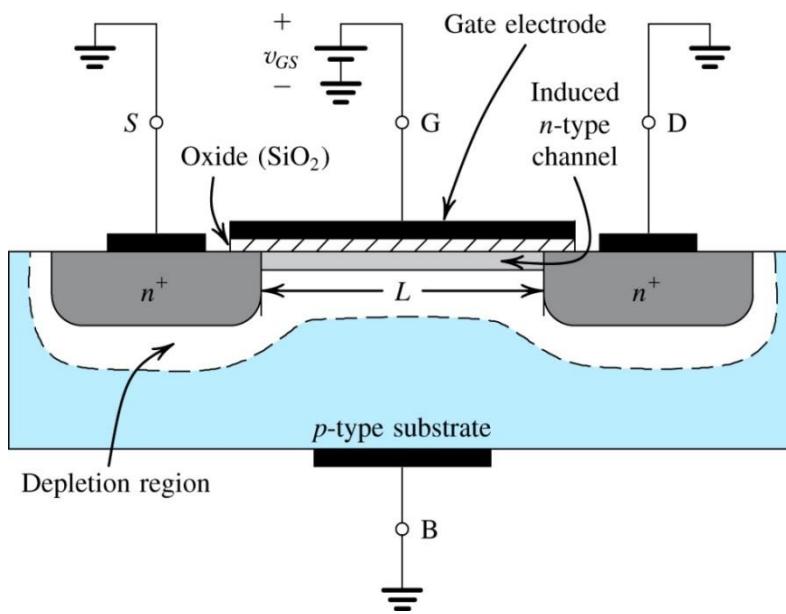


Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

Consider the case where we have grounded the source and the drain and applied a positive voltage to the gate (v_{GS}).

The positive voltage on the gate:

- 1) Repels holes leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "uncovered" because the neutralizing holes have been pushed downward into the substrate.
- 2) Attracts electrons from the source and drain regions thereby inducing an n -type channel under the gate from the source to the drain.

We call this an n -channel MOSFET, or an NMOS transistor



MOSFETs

Note that an *n*-channel MOSFET is formed in a *p*-type substrate: The channel is created by *inverting* the substrate surface from *p*-type to *n*-type. Hence the induced channel is also called an **inversion layer**.

The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted V_t . Obviously, V_t for an *n*-channel FET is positive. The value of V_t is controlled during device fabrication and typically lies in the range of 0.3 V to 1.0 V.

The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{GS} is applied. This is the origin of the name "field-effect transistor" (FET).



Oxide Capacitance

The excess of v_{GS} over V_t is termed the **effective voltage** or the **overdrive voltage** (v_{OV}) and is the quantity that determines the charge in the channel.

$$v_{OV} \equiv v_{GS} - V_t$$

We can express the magnitude of the electron charge in the channel by

$$|Q| = c_{ox}(WL)v_{OV}$$

Where c_{ox} is the **oxide capacitance** - the capacitance of the parallel-plate capacitor per unit gate area (in F/m²), W is the width of the channel, and L is the length of the channel.

$$c_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Where ϵ_{ox} is the permittivity of the silicon dioxide

$$\epsilon_{ox} = 3.9\epsilon_0 = 3.45 \times 10^{-11} \text{ F/m}$$



Oxide Capacitance cont.

The oxide thickness t_{ox} is determined by the process technology used to fabricate the MOSFET. As an example, for a process with $t_{ox} = 4 \text{ nm}$.

$$c_{ox} = \frac{3.45 \times 10^{-11} \text{ F/m}}{4.0 \times 10^{-9} \text{ m}} = 8.6 \times 10^{-3} \text{ F/m}^2$$

It is much more convenient to express c_{ox} per micron squared . For our example, this yields:

$$c_{ox} = 8.6 \text{ fF}/\mu\text{m}^2$$

For a MOSFET fabricated in this technology with a channel length $L = 0.18 \mu\text{m}$ and a channel width $W = 0.72 \mu\text{m}$, the total capacitance between gate and channel is:

$$C = c_{ox}WL = 8.6 \times 0.18 \times 0.72 = 1.1 \text{ fF}$$



Applying a Small v_{DS}

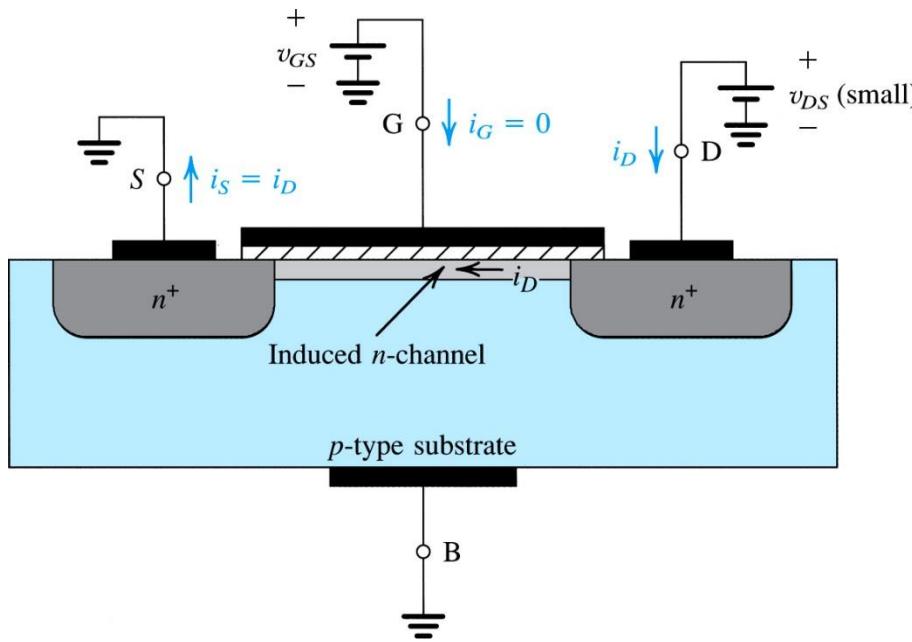


Figure 5.3 An NMOS transistor with $v_{GS} > V_T$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS} . Specifically, the channel conductance is proportional to $v_{GS} - V_T$, and thus i_D is proportional to $(v_{GS} - V_T)$ v_{DS} . Note that the depletion region is not shown (for simplicity).

Having induced a channel, we now apply a positive voltage v_{DS} between drain and source. We first consider the case where v_{DS} is small (i.e., 50 mV or so). The voltage v_{DS} causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain. By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, i_D , will be from drain to source.



Applying a Small v_{DS}

We now wish to calculate the value of i_D . Of particular interest in calculating the current i_D is the charge per unit channel length, which can be found from:

$$|Q| = c_{ox}(WL)v_{ov} \quad \frac{|Q|}{\text{unit channel length}} = c_{ox}(W)v_{ov}$$

The voltage v_{DS} establishes an electric field E across the length of the channel,

$$|E| = \frac{v_{DS}}{L}$$

This electric field in turn causes the channel electrons to drift toward the drain with a velocity given by:

$$\text{electron drift velocity} = \mu_n |E| = \mu_n \frac{v_{DS}}{L}$$

This current can be found by multiplying the charge per unit length by the electron drift velocity:

$$i_D = \left[(\mu_n c_{ox}) \left(\frac{W}{L} \right) v_{ov} \right] v_{DS}$$



From Ch3: 1) Drift current

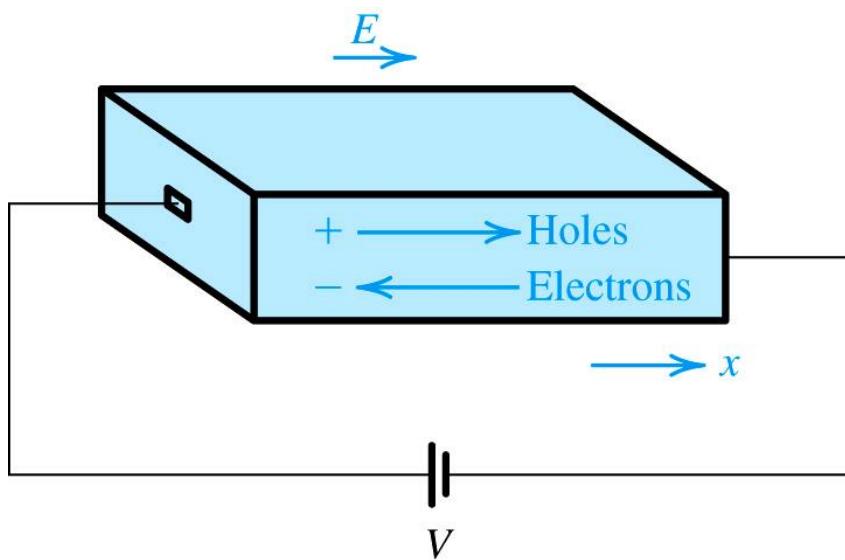


Figure 3.5 An electric field E established in a bar of silicon causes the holes to drift in the direction of E and the free electrons to drift in the opposite direction. Both the hole and electron drift currents are in the direction of E .

Drift speed/velocity for holes

$$v_{p-drift} = \mu_p E$$

Drift speed/velocity for electrons

$$v_{n-drift} = -\mu_n E$$

Where

v is the velocity in cm/s

E is the electric field (V/cm)

μ is the mobility ($\text{cm}^2/(\text{V s})$)

For intrinsic silicon

$$\mu_p = 480 \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \quad \text{hole mobility}$$

$$\mu_n = 1350 \frac{\text{cm}^2}{\text{V} \cdot \text{s}} \quad \text{electron mobility}$$



From Ch 3: Carrier Mobility vs Temperature

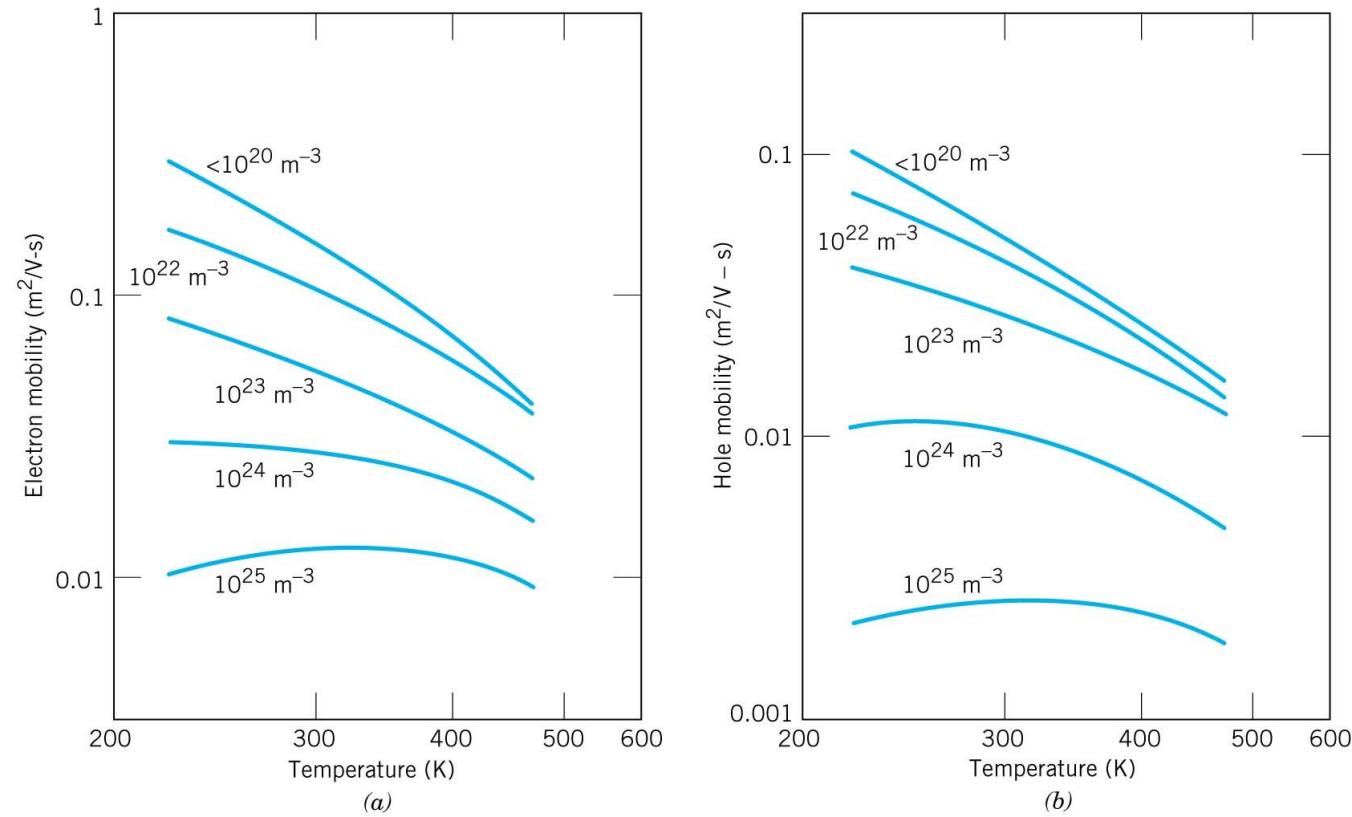


FIGURE 18.18 Temperature dependence of (a) electron and (b) hole mobilities for silicon that has been doped with various donor and acceptor concentrations. Both sets of axes are scaled logarithmically. (From W. W. Gärtnert, “Temperature Dependence of Junction Transistor Parameters,” *Proc. of the IRE*, **45**, 667, 1957. Copyright © 1957 IRE now IEEE.)



Applying a Small v_{DS}

$$i_D = \left[(\mu_n c_{ox}) \left(\frac{W}{L} \right) v_{OV} \right] v_{DS} \quad \text{Ohm's law: } I = V/R$$

Thus, for small v_{DS} , the channel behaves as a linear resistance whose value is controlled by the overdrive voltage v_{OV} , which in turn is determined by v_{GS} :

$$i_D = \left[(\mu_n c_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t) \right] v_{DS}$$

This conductance g_{DS} of the channel is:

$$g_{DS} = (\mu_n c_{ox}) \left(\frac{W}{L} \right) v_{OV} = (\mu_n c_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t)$$



Channel Conductance, g_{DS}

This conductance g_{DS} of the channel is:

$$g_{DS} = (\mu_n c_{ox}) \left(\frac{W}{L} \right) v_{OV} = (\mu_n c_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t)$$

$\mu_n c_{ox}$ is determined by the process technology used to fabricate the MOSFET.
We define this as the **process transconductance parameter**.

$$k'_n = \mu_n c_{ox} \left[\text{A/V}^2 \right]$$

W/L is the **transistor aspect ratio**.

The product of the process transconductance parameter and the transistor aspect ratio is known as the **MOSFET transconductance parameter**.

$$k_n = k'_n \left(\frac{W}{L} \right) = (\mu_n c_{ox}) \left(\frac{W}{L} \right) \left[\text{A/V}^2 \right]$$



Applying a Small v_{DS}

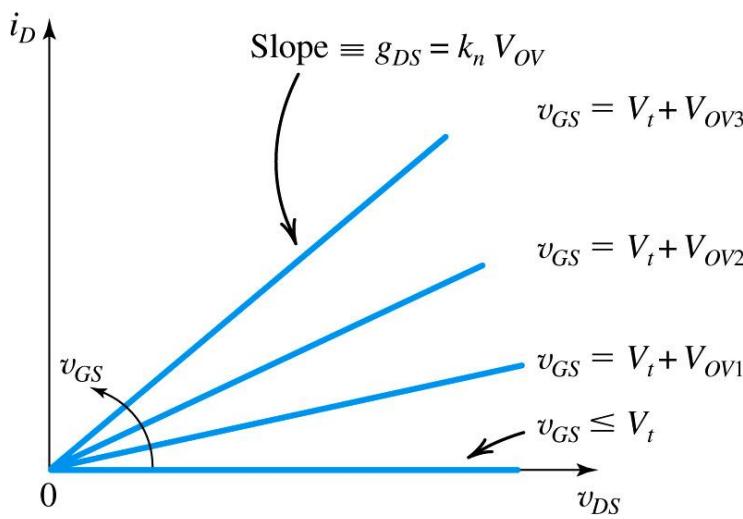


Figure 5.4 The i_D - v_{DS} characteristics of the MOSFET in Fig 5.3 when the voltage applied between drain and source, v_{DS} , is kept small. The device acts as a linear resistance whose value is controlled by v_{GS} .

when v_{DS} is kept small, the MOSFET behaves as a linear resistance r_{DS} whose value is controlled by the gate voltage v_{GS}

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{(\mu_n c_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t)}$$

First a channel has to be induced. Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**.

Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.



Operation as v_{DS} is increased

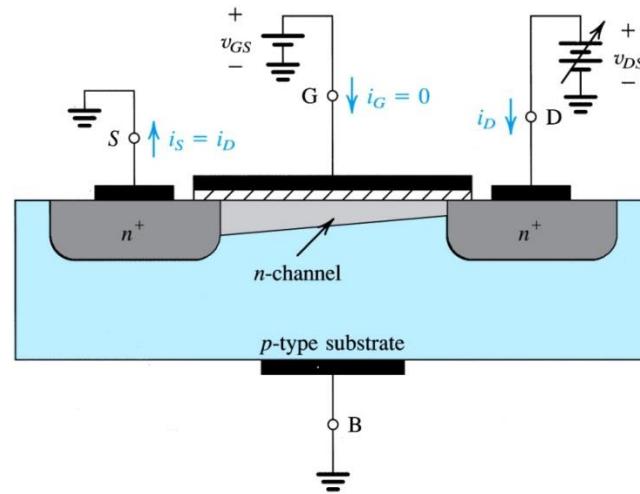


Figure 5.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value $> V_t$.

Refer to Fig. 5.5, and note that v_{DS} appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage (measured relative to the source) increases from zero to v_{DS} . Thus the voltage between the gate and points along the channel decreases from $v_{GS} = V_t + V_{OV}$ at the source end to $v_{GD} = v_{GS} - v_{DS} = V_t + V_{OV} - v_{DS}$ at the drain end.



Operation as v_{DS} is increased

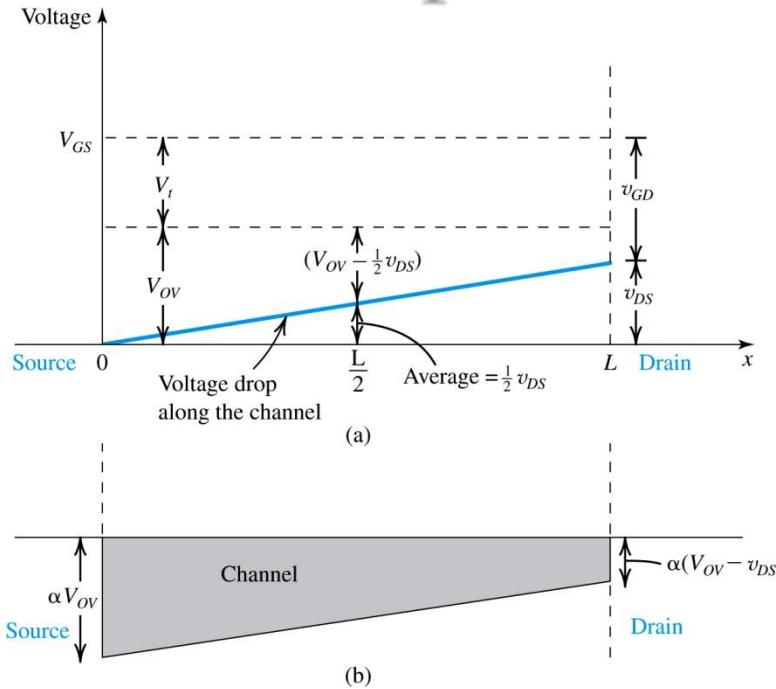


Figure 5.6 (a) For a MOSFET with $v_{GS} = V_t + V_{OV}$, application of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2} v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. (b) The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to V_{OV} , that at the drain end is proportional to $(V_{OV} - v_{DS})$.

Since the channel depth depends on this voltage, and specifically on the amount by which this voltage exceeds V_t , we find that the channel is no longer of uniform depth; rather, the channel will take the tapered shape shown in Fig. 5.5, being deepest at the source end (where the depth is proportional to V_{OV}) and shallowest at the drain end (where the depth is proportional to $V_{OV} - v_{DS}$). This point is further illustrated in Fig. 5.6.



Operation as v_{DS} is increased

The charge in the tapered channel is proportional to the channel cross-sectional area shown in Fig. 5.6(b). This area in turn can be easily seen as proportional to:

$$\frac{1}{2}[V_{OV} + (V_{OV} - v_{DS})] = V_{OV} - \frac{v_{DS}}{2}$$

We had initially found that

$$i_D = \left[k'_n \left(\frac{W}{L} \right) v_{OV} \right] v_{DS}$$

Where we replace v_{OV} with $V_{OV} - v_{DS}/2$ yielding:

$$i_D = k'_n \left(\frac{W}{L} \right) \left(V_{OV} - \frac{v_{DS}}{2} \right) v_{DS}$$

This relationship describes the semi-parabolic portion of the i_D - v_{DS} curve

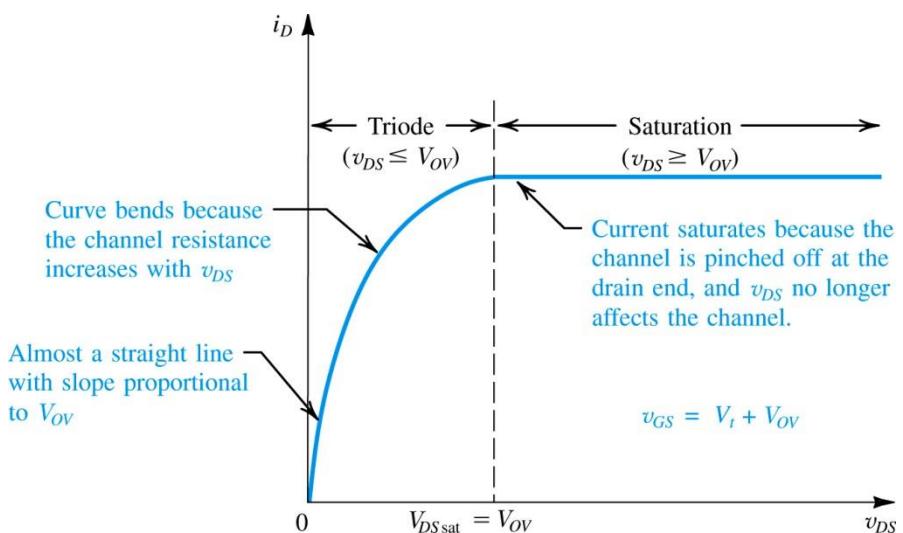


Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.



Operation as v_{DS} is increased

$$i_D = k'_n \left(\frac{W}{L} \right) \left(V_{OV} - \frac{v_{DS}}{2} \right) v_{DS}$$

Which is often written as:

$$i_D = k'_n \left(\frac{W}{L} \right) \left(V_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$

for an arbitrary value of V_{OV} , we can replace V_{OV} by $(v_{GS} - V_t)$

$$i_D = k'_n \left(\frac{W}{L} \right) \left((v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$

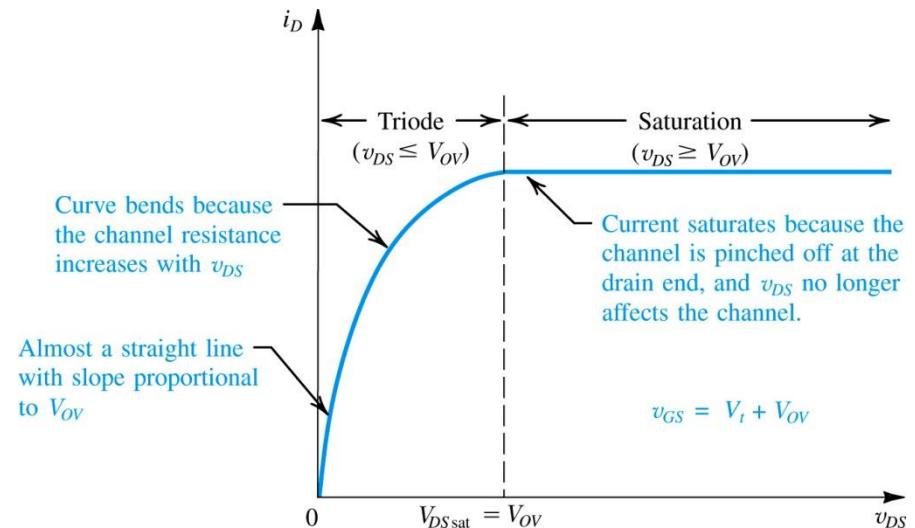


Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.



Operation for $v_{DS} \geq V_{OV}$

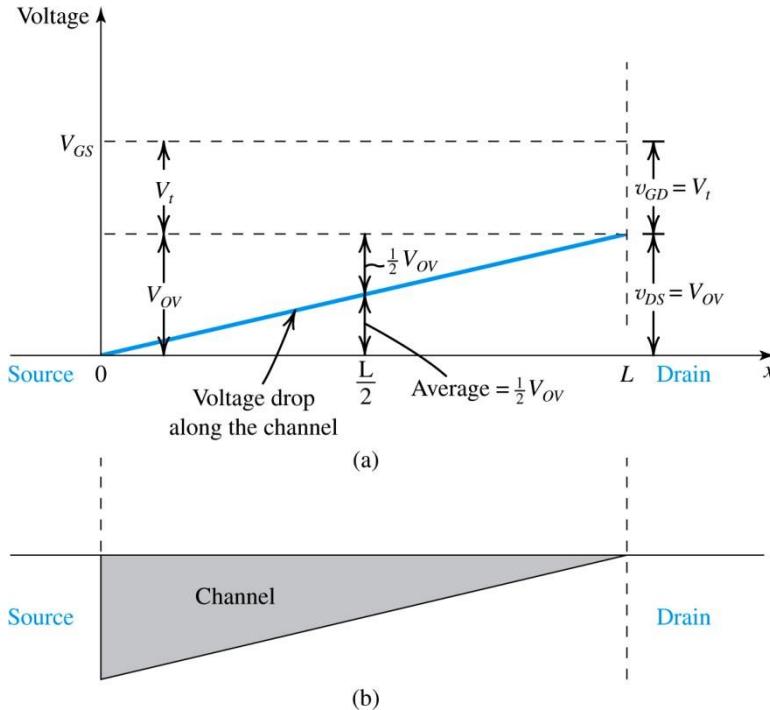


Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, as v_{DS} is increased to V_{OV} . At the drain end, v_{GD} decreases to V_t and the channel depth at the end reduces to zero (pinch off).

At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{DSat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.

In the previous analysis v_{DS} must be less than V_{OV} , for as $v_{DS} = V_{OV}$, $v_{GS} = V_t$, and the channel depth at the drain end reduces to zero. The zero depth of the channel at the drain end gives rise to the term **channel pinch-off**. Increasing v_{DS} beyond this value has no effect on the channel shape and charge, and the current through the channel remains constant at the value reached for $v_{DS} = V_{OV}$.

The drain current thus **saturates** at the value:

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) V_{OV}^2$$

The MOSFET is then said to have entered the **saturation region**

$$v_{DSsat} = V_{OV} = V_{GS} - V_t$$

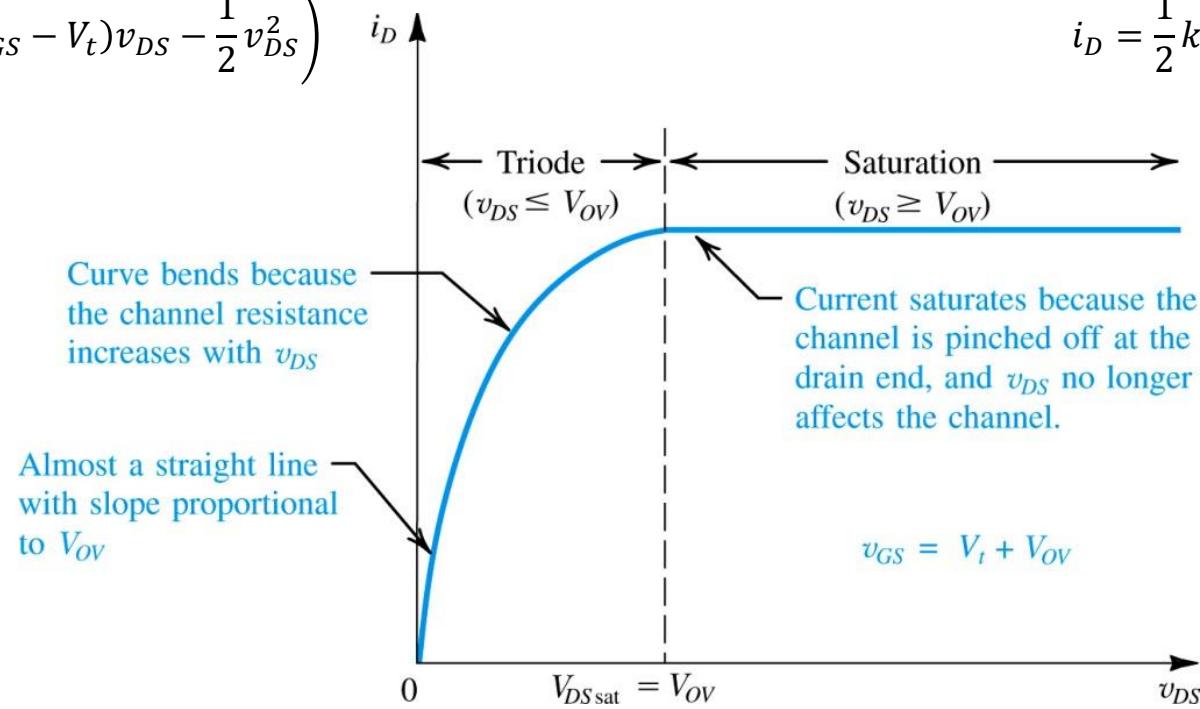


NMOS transistor curve

Triode Region

$$i_D = k'_n \left(\frac{W}{L} \right) \left(V_{OV} v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$

$$i_D = k'_n \left(\frac{W}{L} \right) \left((v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$



Saturation Region

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2$$

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2$$

Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.



The *p*-Channel MOSFET

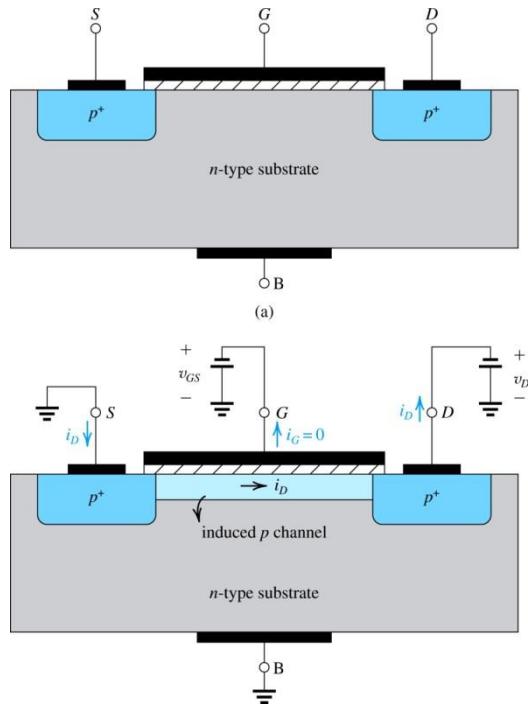


Figure 5.9 (a) Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor shown in Fig. 5.1(b) except that all semiconductor regions are reversed in polarity. (b) A negative voltage v_{GS} of magnitude greater than $|V_{tp}|$ induces a *p* channel, and a negative v_{DS} causes a current i_D to flow from source to drain.

To induce a channel for current flow between source and drain, a negative voltage is applied between the gate and the source where

$$v_{GS} \leq V_{tp} \quad \text{or} \quad |v_{GS}| \geq |V_{tp}|$$

the **process transconductance parameter** for the PMOS device is:

$$k'_p = \mu_p c_{ox} \left[\text{A/V}^2 \right]$$

the **transistor transconductance parameter** is:

$$k_p = k'_p \left(\frac{W}{L} \right) \left[\text{A/V}^2 \right]$$



Complementary MOS or CMOS

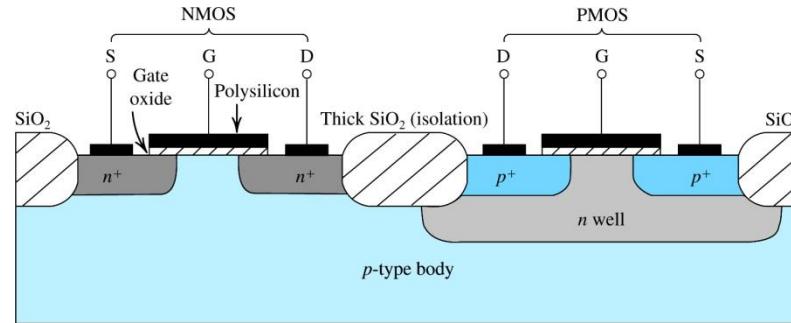
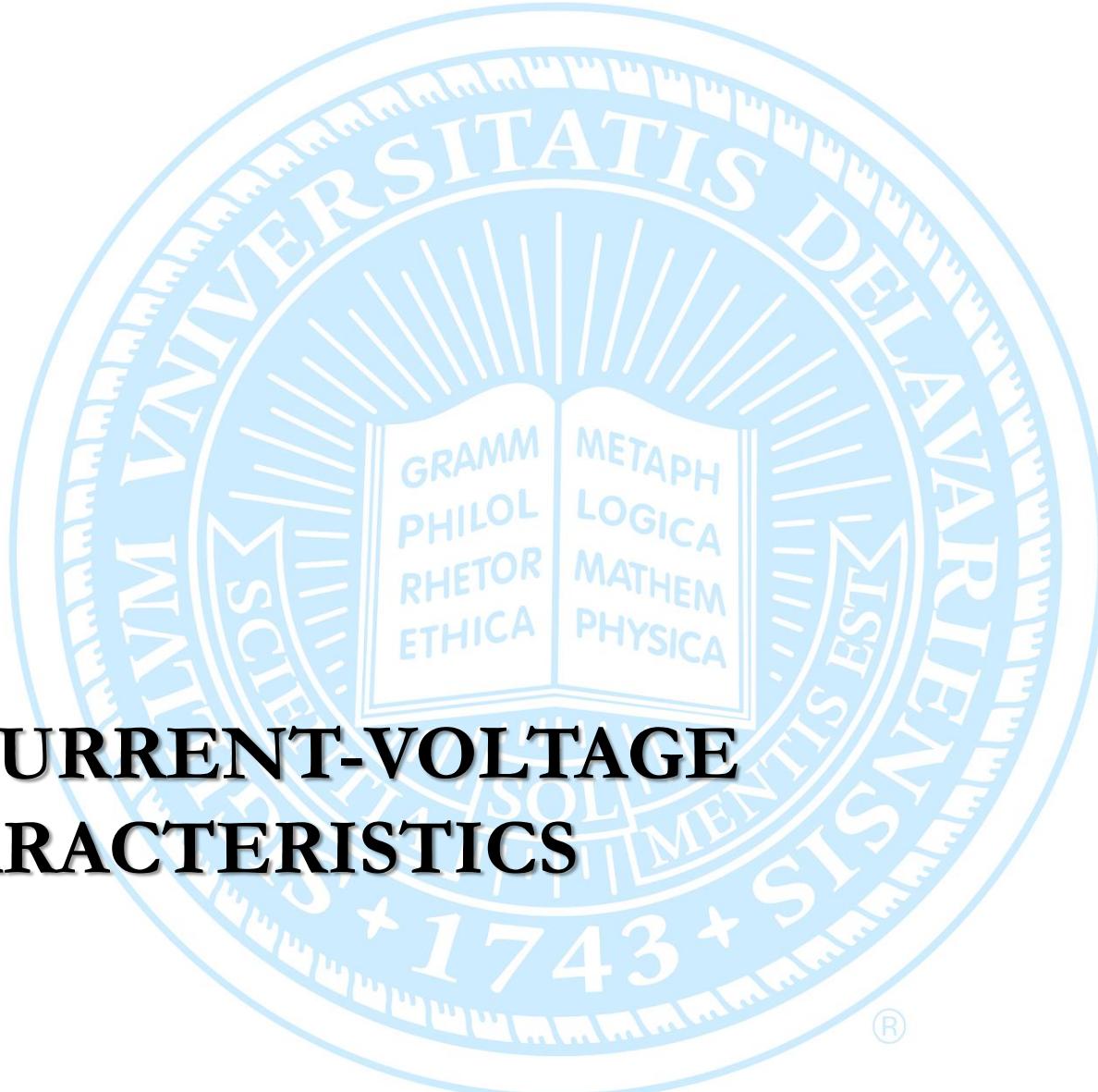


Figure 5.10 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate n -type region, known as an n well. Another arrangement is also possible in which an n -type body is used and the n device is formed in a p well. Not shown are the connections made to the p -type body and to the n well; the latter functions as the body terminal for the p -channel device.

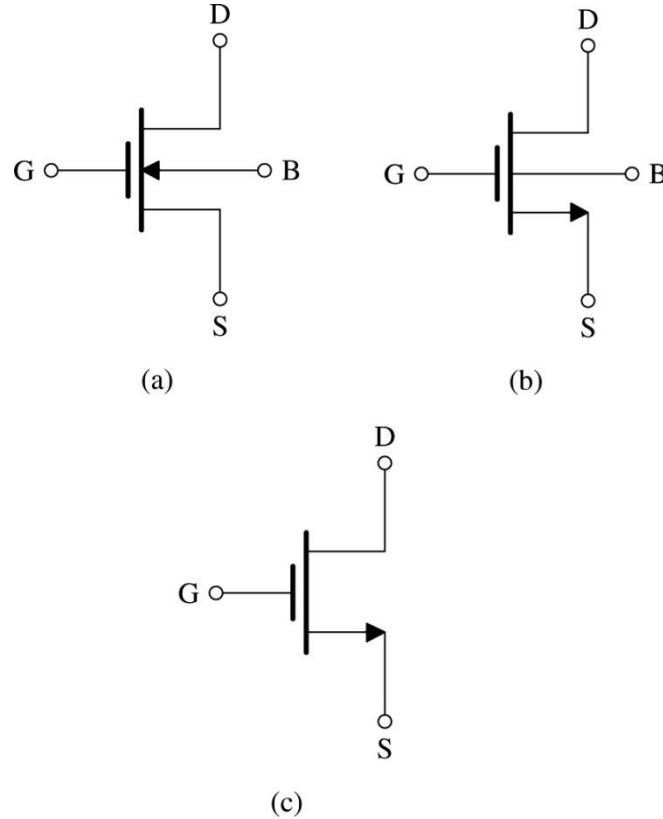
PMOS technology originally dominated MOS integrated-circuit manufacturing, and the original microprocessors utilized PMOS transistors. As the technological difficulties of fabricating NMOS transistors were solved, NMOS completely supplanted PMOS. The main reason for this change is that electron mobility μ_n is 2 to 4 times higher than the hole mobility μ_p , resulting in NMOS transistors having greater gains and speeds of operation than PMOS devices. Subsequently, a technology was developed that permits the fabrication of both NMOS and PMOS transistors on the same chip. Appropriately called **complementary MOS**, or **CMOS**, this technology is currently the dominant electronics technology.



5.2 CURRENT-VOLTAGE CHARACTERISTICS



n-Channel MOSFET Circuit Symbol

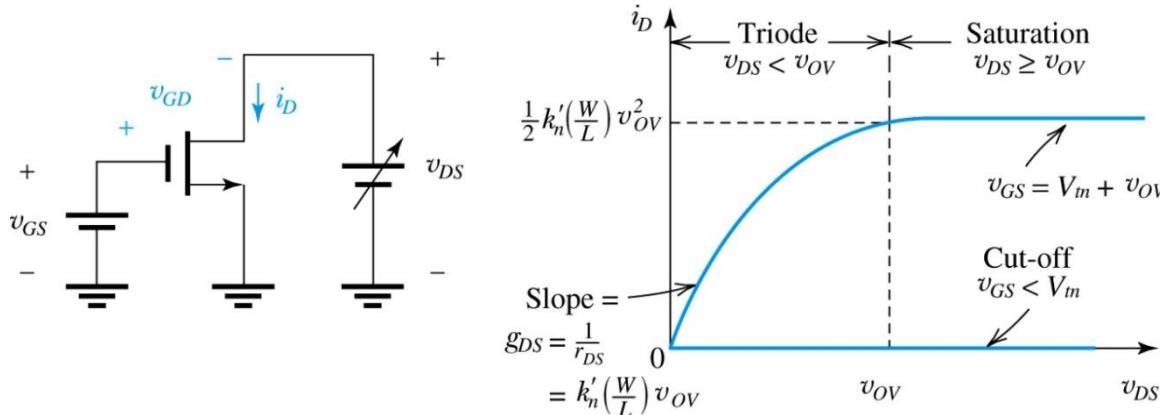


Circuit symbol for the *n*-channel enhancement-type MOSFET. Observe that the spacing between the two vertical lines that represent the gate and the channel indicates the fact that the gate electrode is insulated from the body of the device. The polarity of the *p*-type substrate (body) and the *n* channel is indicated by the arrowhead on the line representing the body.

Figure 5.11 (a) Circuit symbol for the *n*-channel enhancement-type MOSFET. (b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). (c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.



Regions of Operation of the Enhancement NMOS Transistor



$v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor

$v_{GS} = V_{tn} + v_{ov}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end.

Triode Region

$$v_{GD} > V_{tn} \quad i_D = k'_n \left(\frac{W}{L} \right) \left(v_{ov} v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$

or

$$v_{DS} < v_{ov} \quad i_D = k'_n \left(\frac{W}{L} \right) \left((v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right)$$

Saturation Region

$$v_{GD} \leq V_{tn} \quad i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{ov}^2$$

or

$$v_{DS} \geq v_{ov} \quad i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_t)^2$$



Regions of Operation of the Enhancement NMOS Transistor

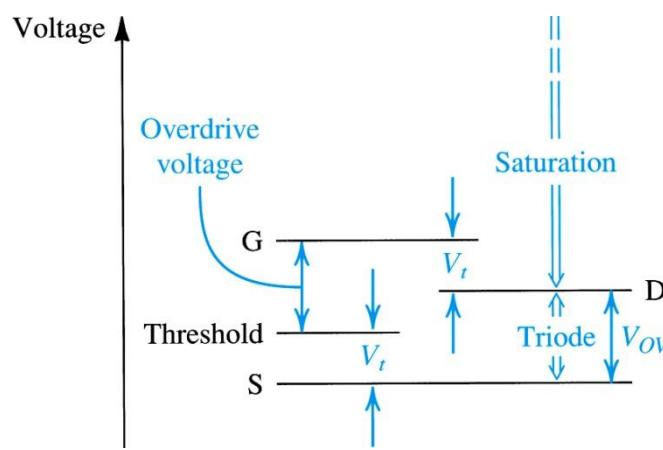


Figure 5.12 The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

The boundary between the triode region and the saturation region is determined by whether v_{DS} is less or greater than the overdrive voltage v_{OV} , at which the transistor is operating. An equivalent way to check for the region of operation is to examine the relative values of the drain and gate voltages. To operate in the triode region, the gate voltage must exceed the drain voltage by at least V_{tn} volts, which ensures that the channel remains continuous (not pinched off). On the other hand, to operate in saturation, the channel must be pinched off at the drain end; pinch-off is achieved here by keeping v_D higher than $v_G - V_{tn}$, that is, not allowing v_D to fall below v_G by more than V_{tn} volts.



The $i_D - v_{DS}$ Characteristics

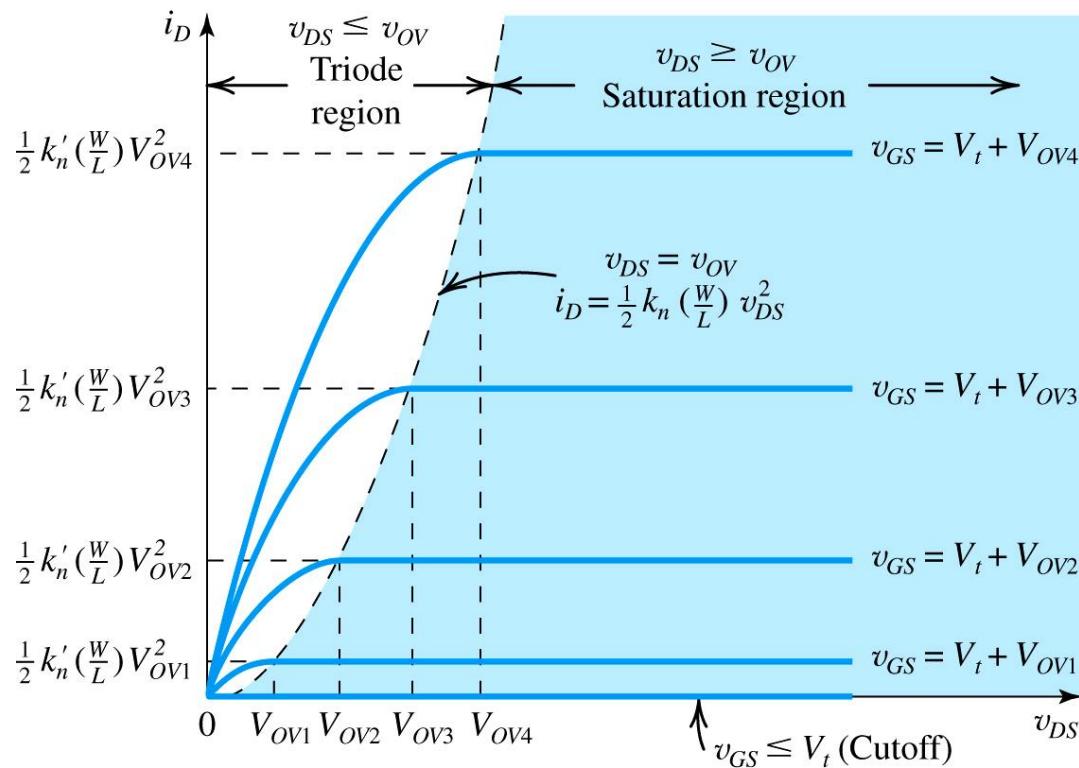
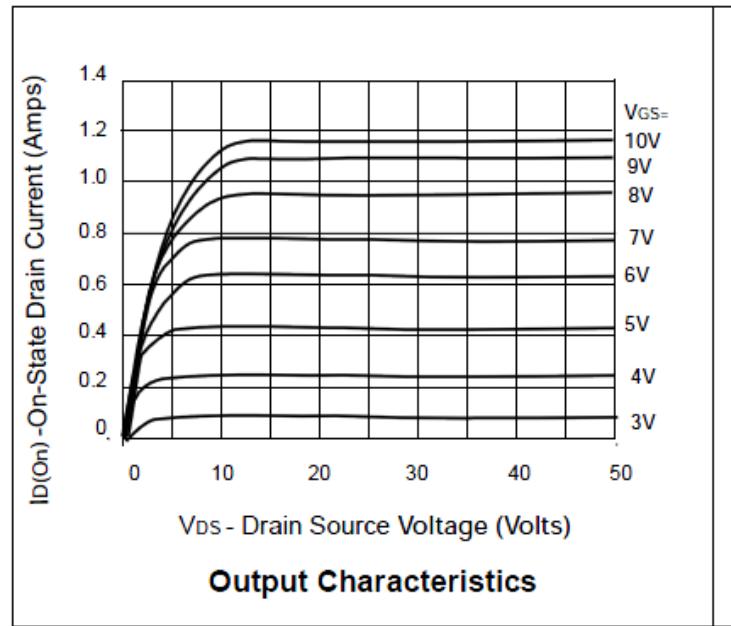


Figure 5.13 The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor.



ZVN3310A



The $i_D - v_{GS}$ Characteristics

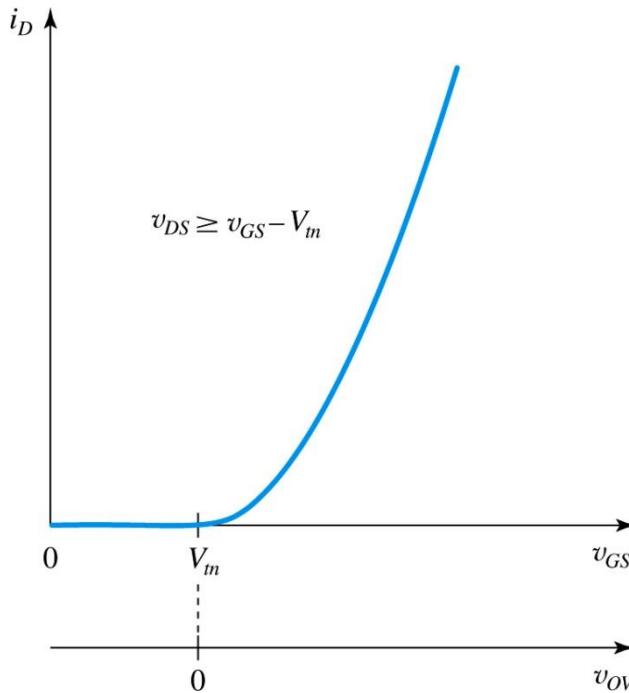


Figure 5.14 The $i_D - v_{GS}$ characteristics of an NMOS transistor operating in the saturation region. The $i_D - v_{OV}$ characteristic can be obtained by simply re-labeling the horizontal axis; that is, shifting the origin to the point $v_{GS} = V_{tn}$.

When the MOSFET is used to design an amplifier, it is operated in the saturation region. As Fig. 5.13 indicates, in saturation the drain current is constant determined by v_{GS} (or v_{OV}) and is independent of v_{DS} . That is, the MOSFET operates as a constant-current source where the value of the current is determined by v_{GS} . In effect, then, the MOSFET operates as a voltage-controlled current source with the control relationship described by:

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

or in terms of v_{OV}

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2$$

Figure 5.14 shows the $i_D - v_{GS}$ characteristics of an NMOS transistor operating in the saturation region.



Equivalent Circuit Model

the MOSFET operates as a voltage-controlled current source

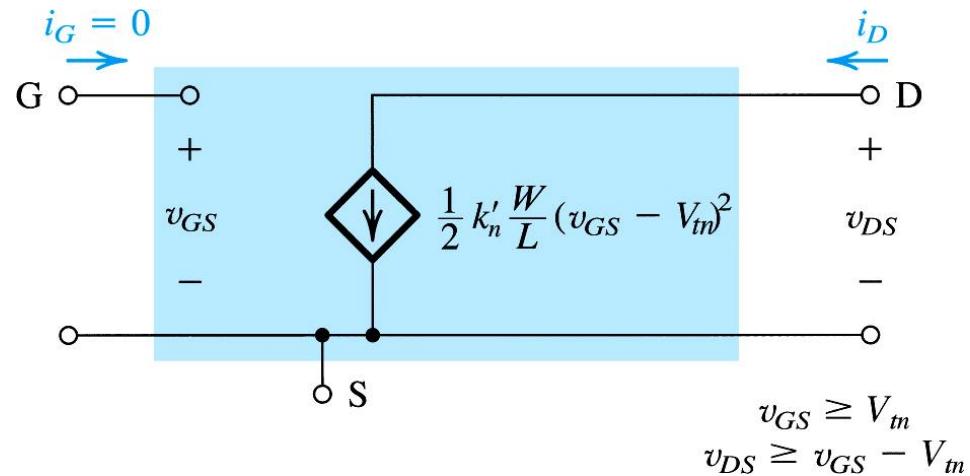


Figure 5.15 Large-signal equivalent-circuit model of an *n*-channel MOSFET operating in the saturation.

Note that the relationship is nonlinear



Finite Output Resistance in Saturation

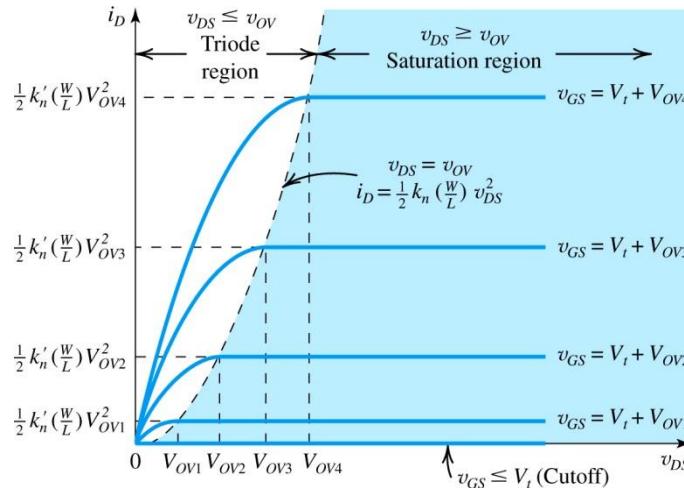


Figure 5.13 The i_D - v_{DS} characteristics for an enhancement-type NMOS transistor.

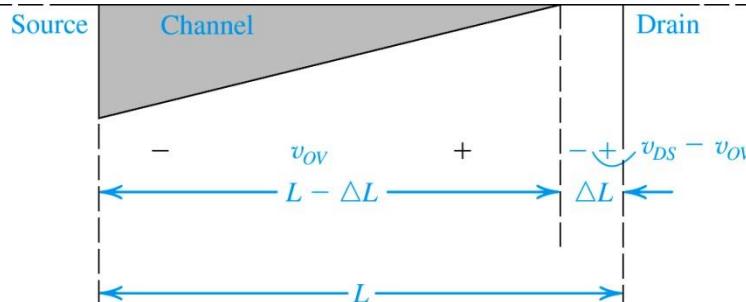


Figure 5.16 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

Indicates that in saturation, i_D is independent of v_{DS} . Thus, a change Δv_{DS} in the drain-to-source voltage causes a zero change in i_D , which implies that the incremental resistance looking into the drain of a saturated MOSFET is infinite.

In practice, increasing v_{DS} beyond v_{DSsat} moves the channel pinch-off point slightly away from the drain and towards the source. The voltage across the channel remains constant at v_{OV} and the additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region.



Finite Output Resistance in Saturation

The effective length of the channel is reduced from L to $L - \Delta L$, a phenomenon known as **channel-length modulation**. The current is inversely proportional to the channel length and therefore increases as the channel length shortens.

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

To compensate for this we add the factor $(1 + \lambda v_{DS})$

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$$

where λ is a device parameter having the units of reciprocal volts (V^{-1}). The value of λ depends both on the process technology used to fabricate the device and on the channel length L that the circuit designer selects.

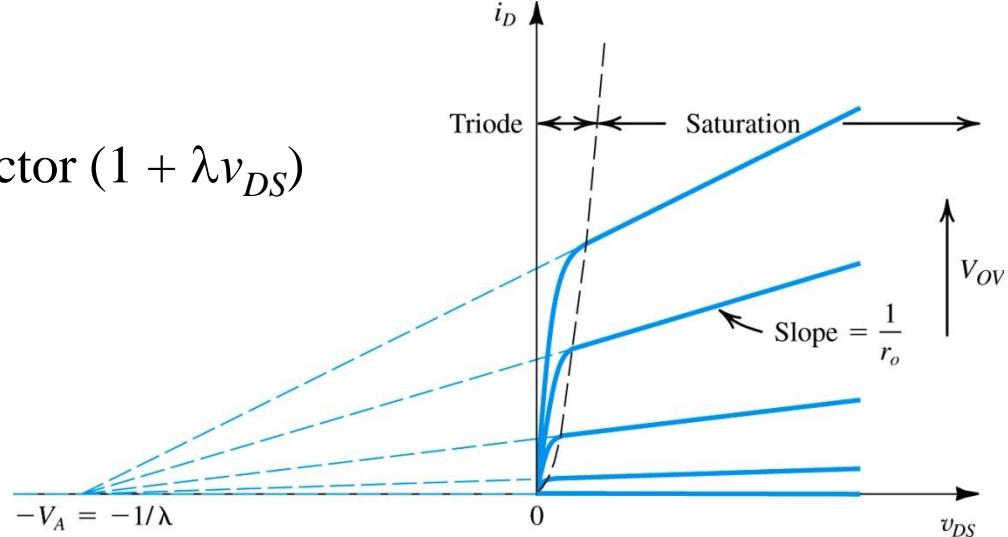


Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L .



Finite Output Resistance in Saturation

Channel-length modulation results in a linear dependence of i_D on v_{DS} in the saturation region. Inserting $v_{DS} = -1/\lambda$ in the following equation results in $i_D = 0$.

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$$

So therefore:

$$V_A = \frac{1}{\lambda} = V'_A L \text{ [V}/\mu\text{m]}$$

where V'_A is entirely process dependent.

Thus, for a given v_{GS} , a change Δv_{DS} yields a corresponding change Δi_D in the drain current. It follows that the output resistance of the current source representing i_D in saturation is no longer infinite.

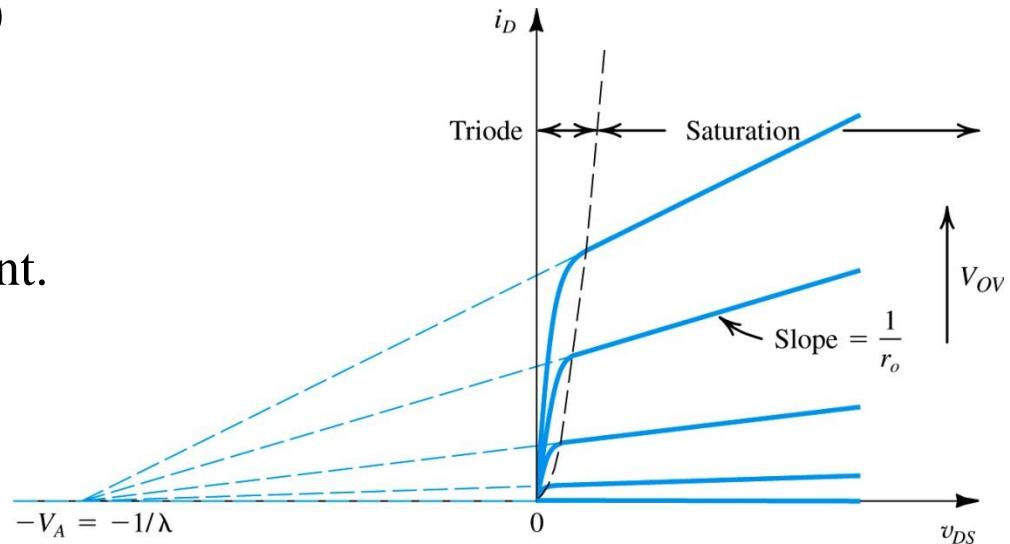


Figure 5.17 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L .



Large Signal Model on an n -channel MOSFET in Saturation

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}} \right]^{-1} \quad v_{GS} \text{ constant}$$

$$\text{Eq. (5.23)} \quad i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$$

$$r_o = \left[\lambda \frac{k'_n W}{2 L} (v_{GS} - V_{tn})^2 \right]^{-1}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

$$\text{where } I_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

I_D is the drain current *without* channel-length modulation taken into account.

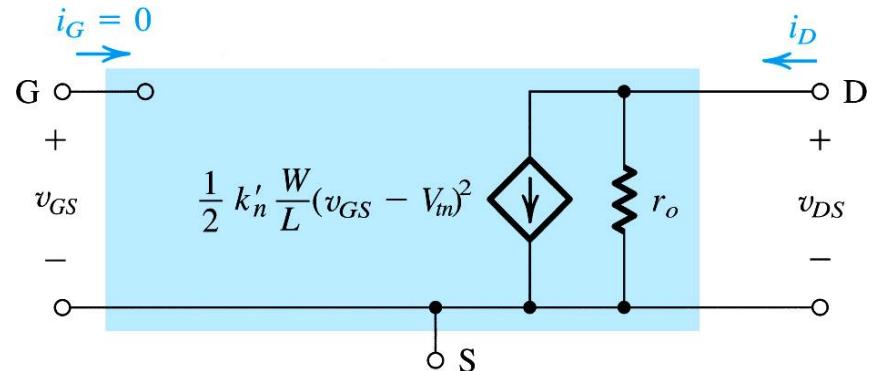
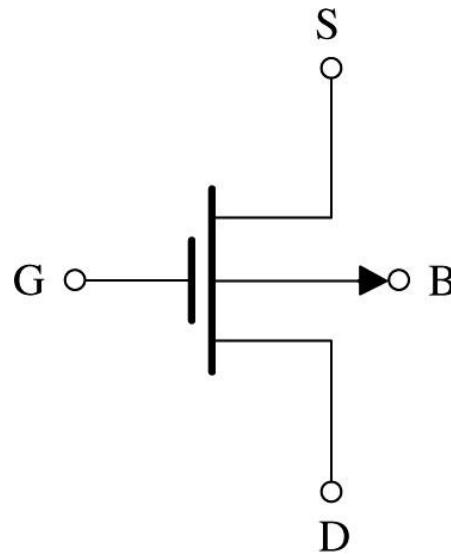


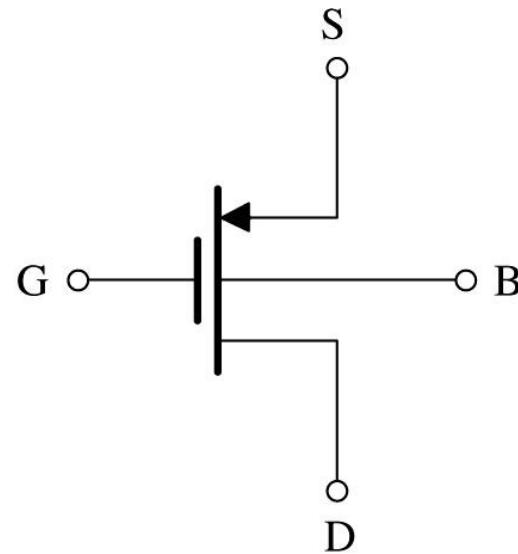
Figure 5.18 Large-signal equivalent-circuit model of an n -channel MOSFET operating in the saturation, incorporating the output resistor r_o . The output resistance models the linear dependence of i_D on v_{DS} and is given by Eq. (5.23).



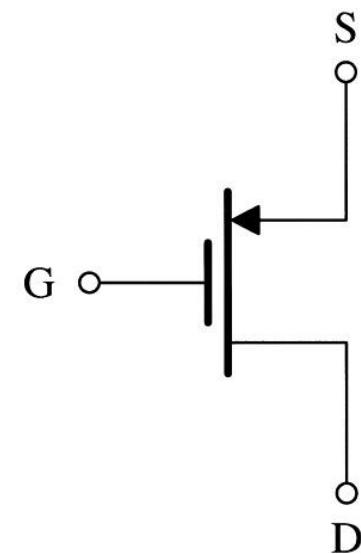
p-Channel Enhancement Mode MOSFET



(a)



(b)

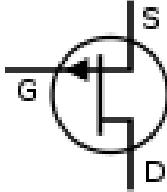
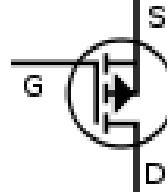
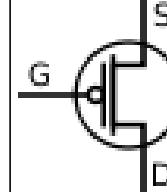
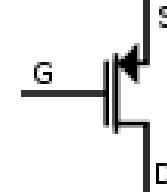
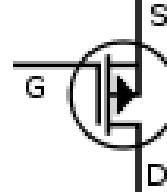
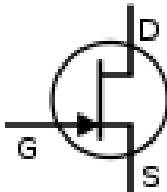
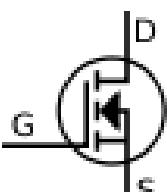
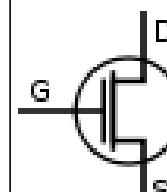
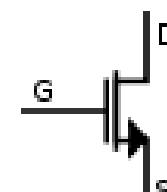
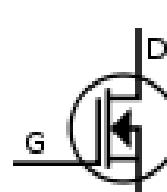


(c)

Figure 5.19 (a) Circuit symbol for the *p*-channel enhancement-type MOSFET. (b) Modified symbol with an arrowhead on the source lead. (c) Simplified circuit symbol for the case where the source is connected to the body.



FET Symbols

					P-channel
					N-channel
JFET	MOSFET enhancement	MOSFET enhancement (no bulk/body)	MOSFET depletion		

Comparison of enhancement-mode and depletion-mode MOSFET symbols, along with JFET symbols (drawn with source and drain ordered such that higher voltages appear higher on the page than lower voltages):



Regions of Operation of the Enhancement PMOS Transistor

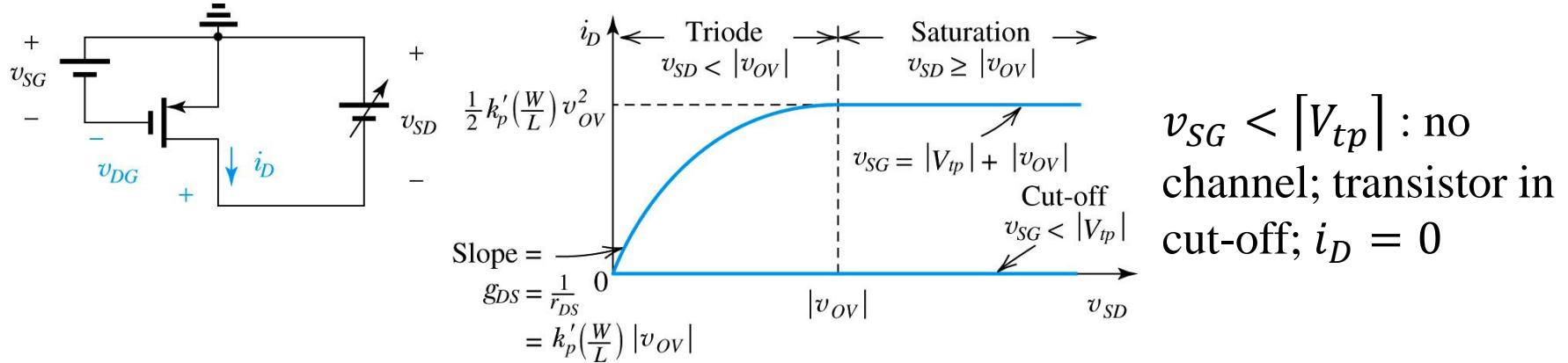


Table 5.2 Regions of Operation of the Enhancement PMOS Transistor

$v_{SG} = |V_{tp}| + |v_{ov}|$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end.

Triode Region

$$\begin{aligned} v_{DG} > |V_{tp}| \quad i_D &= k'_p \left(\frac{W}{L}\right) \left(|v_{ov}| - \frac{1}{2} v_{SD} \right) v_{SD} \\ \text{or} \quad \text{or} \end{aligned}$$

$$v_{SD} < |v_{ov}| \quad i_D = k'_p \left(\frac{W}{L}\right) \left((v_{SG} - |V_t|) v_{SD} - \frac{1}{2} v_{SD}^2 \right)$$

Saturation Region

$$\begin{aligned} v_{DG} \leq |V_{tp}| \quad i_D &= \frac{1}{2} k'_p \left(\frac{W}{L}\right) v_{ov}^2 \\ \text{or} \quad \text{or} \end{aligned}$$

$$v_{SD} \geq |v_{ov}| \quad i_D = \frac{1}{2} k'_p \left(\frac{W}{L}\right) (v_{SG} - |V_{tp}|)^2$$



Regions of Operation of the Enhancement PMOS Transistor

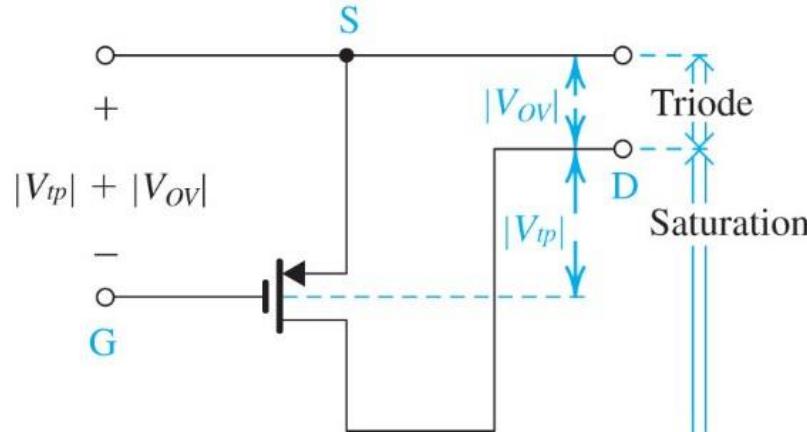
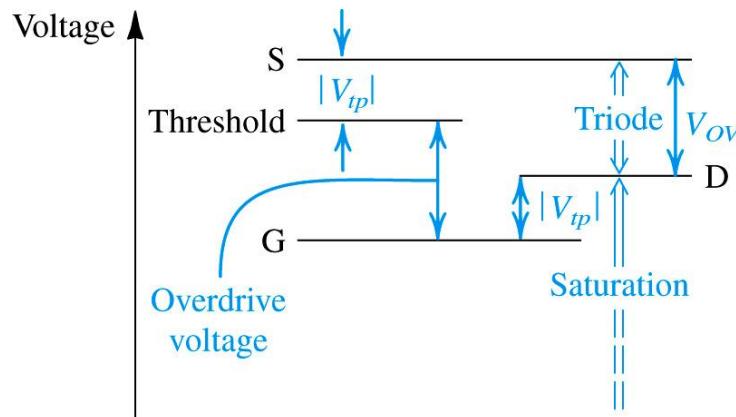


Figure 5.20 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.





Exercise 5.7 (a)

The PMOS transistor shown in Fig. E5.7 has $V_{tp} = -1$ V, $k'_p = 60 \mu\text{A}/\text{V}^2$, and $W/L = 10$.

- Find the range of V_G for which the transistor conducts.
- In terms of V_G , find the range of V_D for which the transistor operates in the triode region.
- In terms of V_G , find the range of V_D for which the transistor operates in saturation.
- Neglecting channel-length modulation (i.e., $\lambda = 0$), find the values of $|V_{OV}|$ and V_G and the corresponding range of V_D to operate the transistor in the saturation mode with $I_D = 75 \mu\text{A}$.
- If $\lambda = -0.02 \text{ V}^{-1}$, find the value of r_o corresponding to the overdrive voltage determined in (d).
- For $\lambda = -0.02 \text{ V}^{-1}$ and for the value of V_{OV} determined in (d), find I_D at $V_D = +3$ V and at $V_D = 0$ V; hence, calculate the value of the apparent output resistance in saturation. Compare to the value found in (e).

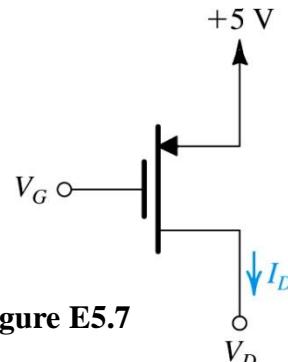


Figure E5.7

- (a) Find the range of V_G for which the transistor conducts.

$$V_{GS} \leq V_{tp} = -1\text{V}$$

$$V_G \leq V_S + V_{tp} \leq 5 - 1 \leq 4\text{V}$$



Exercise 5.7 (b,c)

The PMOS transistor shown in Fig. E5.7 has $V_{tp} = -1$ V, $k'_p = 60 \mu\text{A}/\text{V}^2$, and $W/L = 10$.

(b) In terms of V_G , find the range of V_D for which the transistor operates in the triode region.

$$V_{GD} \leq V_{tp}$$

$$V_G - V_D \leq -1\text{V}$$

$$V_D \geq V_G + 1\text{V}$$

(c) In terms of V_G , find the range of V_D for which the transistor operates in saturation.

$$V_{GD} > V_{tp}$$

$$V_G - V_D > -1\text{V}$$

$$V_D < V_G + 1\text{V}$$

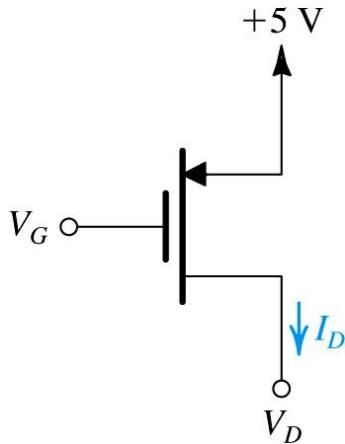


Figure E5.7



Exercise 5.7 (d)

The PMOS transistor shown in Fig. E5.7 has $V_{tp} = -1$ V, $k'_p = 60 \mu\text{A}/\text{V}^2$, and $W/L = 10$.

- (d) Neglecting channel-length modulation (i.e., $l = 0$), find the values of $|V_{OV}|$ and V_G and the corresponding range of V_D to operate the transistor in the saturation mode with $I_D = 75 \mu\text{A}$.

$$i_D = \frac{1}{2} k'_p \left(\frac{W}{L} \right) v_{OV}^2 \quad v_{OV} = \sqrt{\frac{i_D}{\frac{1}{2} k'_n \left(\frac{W}{L} \right)}} \quad v_{OV} := \sqrt{\frac{75 \mu\text{A}}{\frac{1}{2} \cdot 60 \frac{\mu\text{A}}{\text{V}^2} \cdot 10}} = 0.5 \text{ V}$$

$$|V_{ov}| = 0.5 \text{ V} = -V_{GS} + V_{tp} = V_S - V_G + V_{tp} = 4 - V_G$$

$$V_G = 4 - 0.5 = 3.5 \text{ V}$$

$$V_D < V_G + 1 \text{ V} < 4.5 \text{ V}$$

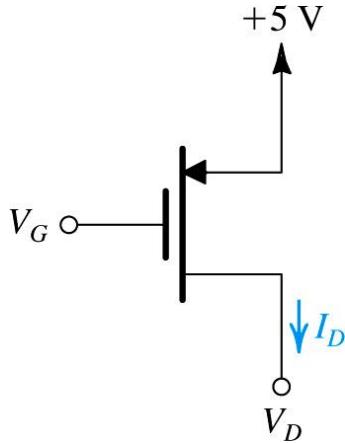


Figure E5.7



Exercise 5.7 (e,f)

The PMOS transistor shown in Fig. E5.7 has $V_{tp} = -1$ V, $k'_p = 60 \mu\text{A}/\text{V}^2$, and $W/L = 10$.

(e) If $\lambda = -0.02 \text{ V}^{-1}$, find the value of r_o corresponding to the overdrive voltage determined in

(d).

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.02 \frac{\text{V}}{75\mu\text{A}}} = 666.667 \text{k}\Omega$$

(f) For $\lambda = -0.02 \text{ V}^{-1}$ and for the value of V_{OV} determined in (d), find I_D at $V_D = +3$ V and at $V_D = 0$ V; hence, calculate the value of the apparent output resistance in saturation. Compare to the value found in (e).

$$i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) |V_{OV}|^2 (1 + |\lambda| |V_{DS}|)$$

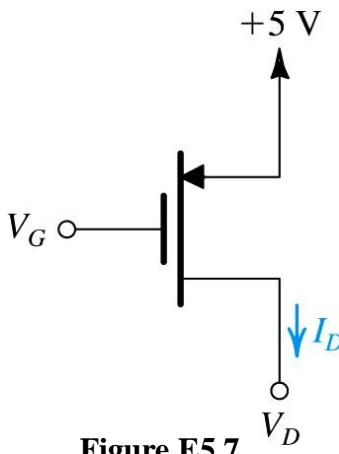


Figure E5.7

$$\text{at } V_D = +3 \text{ V}, V_{DS} = 2 \text{ V} \quad I_D := \frac{1}{2} \cdot 60 \frac{\mu\text{A}}{\text{V}^2} \cdot 10 \cdot (0.5\text{V})^2 \cdot \left(1 + \frac{0.02}{\text{V}} 2\text{V} \right) = 78 \mu\text{A}$$

$$\text{at } V_D = 0 \text{ V}, V_{DS} = 5 \text{ V} \quad I_D := \frac{1}{2} \cdot 60 \frac{\mu\text{A}}{\text{V}^2} \cdot 10 \cdot (0.5\text{V})^2 \cdot \left(1 + \frac{0.02}{\text{V}} 5\text{V} \right) = 82.5 \mu\text{A}$$

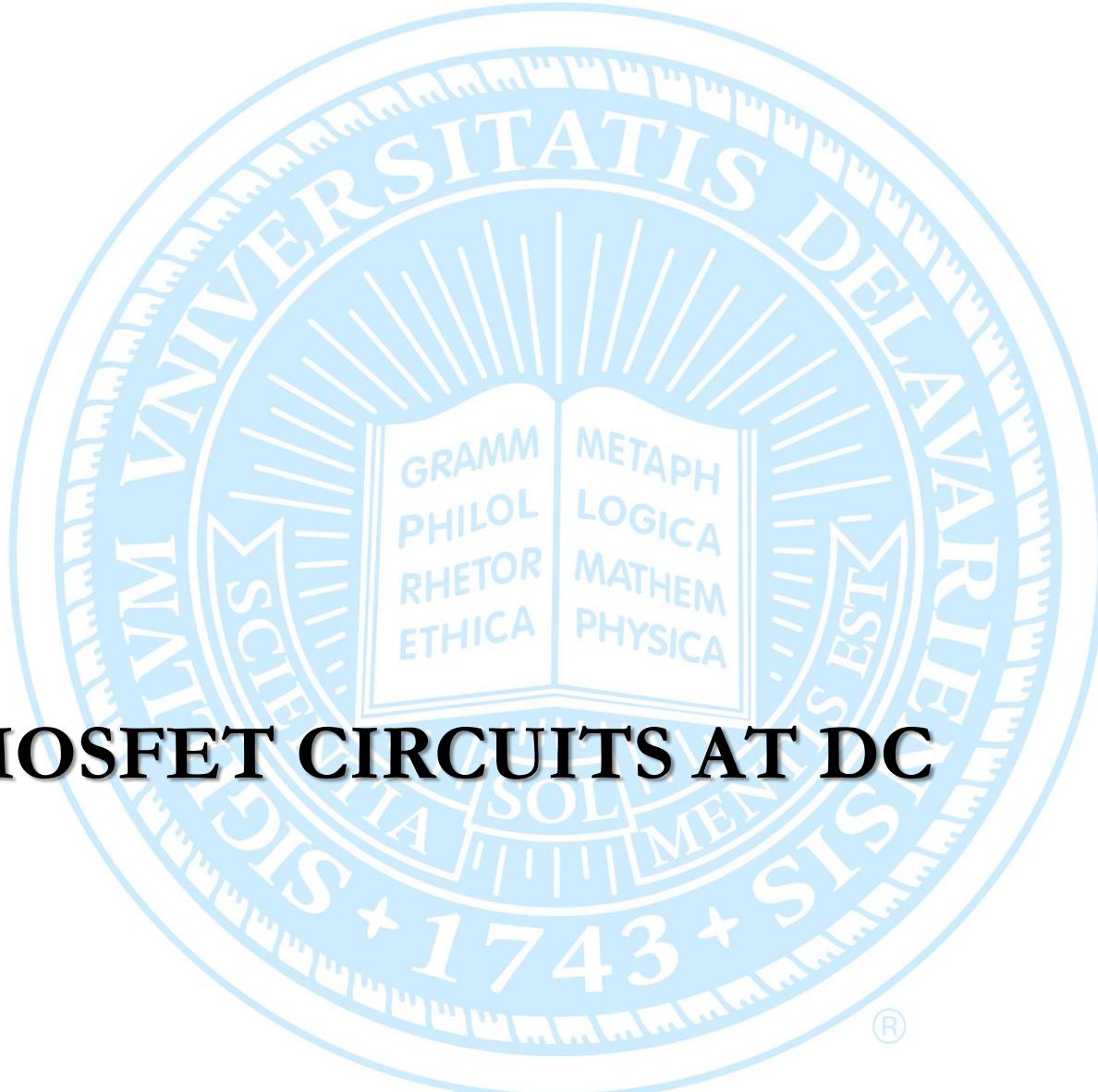
$$r_{o\text{eff}} = \frac{\Delta V_{DS}}{\Delta I_{DS}} = \frac{3\text{V}}{4.5\mu\text{A}} \quad r_{o\text{eff}} := \frac{3\text{V}}{4.5\mu\text{A}} = 666.667 \text{k}\Omega$$



Homework #9

- Read Chapter 5
- Chapter 5 Problems:
 - 5.9*
 - 5.10
 - 5.11*
 - 5.18
 - 5.19*

* Answers in Appendix L



5.3 MOSFET CIRCUITS AT DC



MOSFET Circuits at DC

Having studied the current-voltage characteristics of MOSFETs, we now consider circuits in which only dc voltages and currents are of concern. Specifically, we shall present a series of design and analysis examples of MOSFET circuits at dc. The objective is to instill in the student a familiarity with the device and the ability to perform MOSFET circuit analysis both rapidly and effectively.

To keep matters simple and thus focus attention on the essence of MOSFET circuit operation:

- 1) We will generally neglect channel-length modulation;
that is, we will assume $\lambda = 0$.
- 2) We will find it convenient to work in terms of the overdrive voltage;

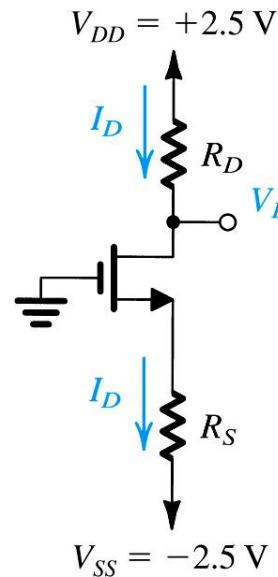
$$V_{OV} = V_{GS} - V_{tn} \text{ for NMOS and}$$

$$|V_{OV}| = V_{SG} - |V_{tp}| \text{ for PMOS.}$$



Example 5.3

Design the circuit of Fig. 5.21, that is, determine the values of R_D and R_S , so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $L = 1 \mu\text{m}$, and $W = 32 \mu\text{m}$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).



$$V_{DD} = +2.5 \text{ V}$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(2.5 - 0.5)\text{V}}{0.4\text{mA}} = 5\text{k}\Omega$$

$$I_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) v_{OV}^2$$

$$v_{OV} = \sqrt{\frac{I_D}{\frac{1}{2} k'_n \left(\frac{W}{L} \right)}}$$

$$v_{OV} := \sqrt{\frac{0.4\text{mA}}{\frac{1}{2} \cdot 100 \frac{\mu\text{A}}{\text{V}^2} \cdot \frac{32\mu\text{m}}{1\mu\text{m}}}} = 0.5 \text{ V}$$

$$V_{GS} = V_t + V_{OV} = (0.7 + 0.5)\text{V} = 1.2\text{V}$$

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{(-1.2 - -2.5)\text{V}}{0.4\text{mA}} = 3.25\text{k}\Omega$$

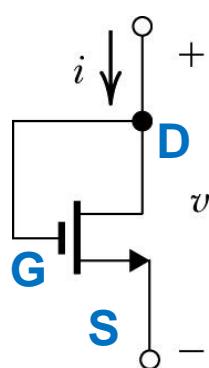
Figure 5.21 Circuit for Example 5.3.



Example 5.4

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the $i-v$ relationship of the resulting two terminal device in terms of the MOSFET parameters $k_n = k'_n(W/L)$ and V_{tn} . Neglect channel-length modulation (i.e. $\lambda = 0$). Note that this two-terminal device is known as a **diode-connected transistor**.

$$v_D = v_G \text{ so the device is operating in saturation } i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$



$$i = i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v - V_{tn})^2 = \frac{1}{2} k_n (v - V_{tn})^2$$

Figure 5.22

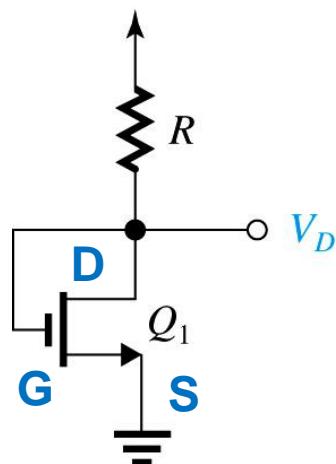


Exercise 5.9

For the circuit in Fig. E5.9, find the value of R that results in $V_D = 0.8$ V. The MOSFET has $V_{tn} = 0.5$ V, $\mu_n C_{ox} = 0.4$ mA/V², $W/L = 0.72$ $\mu\text{m}/0.18$ μm , and $\lambda = 0$.

$$v_D = v_G \text{ so the device is operating in saturation} \quad i_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (v_{GS} - V_{tn})^2$$

$$I_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (V_D - V_{tn})^2 \quad i_D := \frac{1}{2} \cdot 0.4 \frac{\text{mA}}{\text{V}^2} \cdot \frac{.72}{0.18} \cdot (0.8V - 0.5V)^2 = 72 \mu\text{A}$$



$$R = \frac{1.8V - 0.8V}{72\mu\text{A}} = \frac{1V}{72\mu\text{A}} = 13.889 \text{ k}\Omega$$

Figure E5.9



Exercise 5.10

Figure E5.10, shows a circuit obtained by augmenting the circuit of Fig E5.9 considered in Exercise 5.9 with a transistor Q_2 identical to Q_1 and a resistor R_2 . Find the value of R_2 that results in Q_2 operating at the edge of the saturation region. Use your solution to Exercise 5.9.

From Ex 5.9, the MOSFET has $V_{tn} = 0.5$ V, $\mu_n C_{ox} = 0.4 \mu\text{A}/\text{V}^2$, $W/L = 0.72 \mu\text{m}/0.18 \mu\text{m}$, and $\lambda = 0$. The triode/saturation boundary is where $V_D = V_{OV} = 0.3$ V.

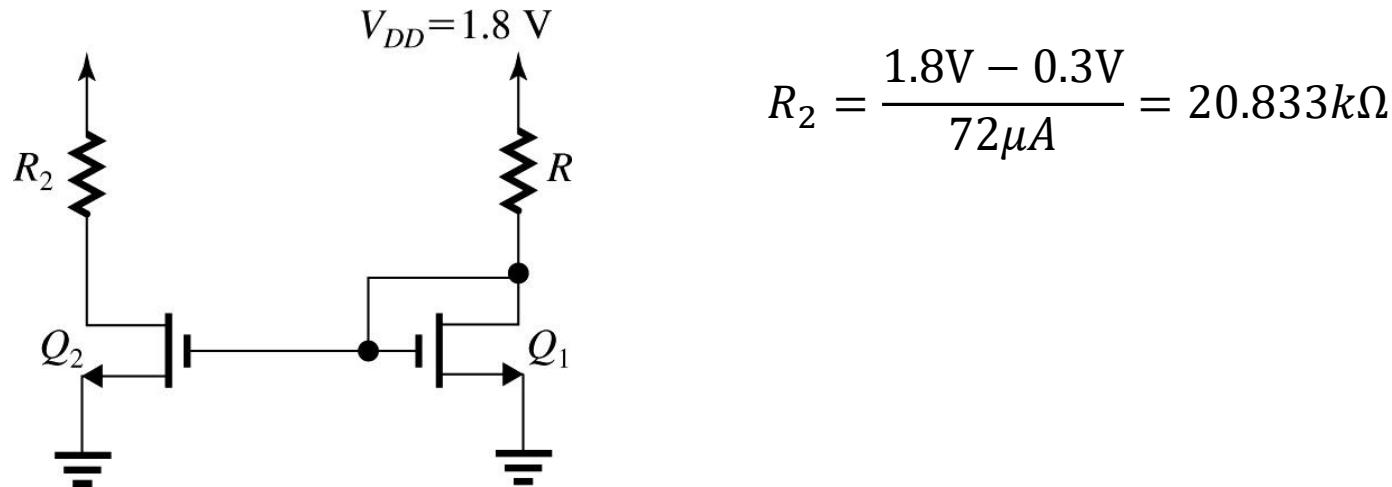


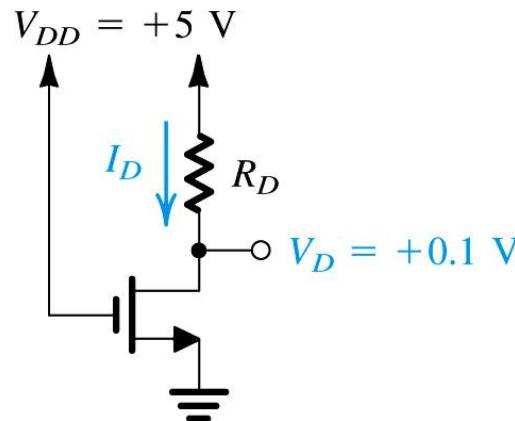
Figure E5.10



Example 5.5

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 1$ V and $k'_n(W/L) = 1$ mA/V².

Since the gate voltage is higher than the drain voltage this device is operating in the triode region so:



$$I_D = k'_n \left(\frac{W}{L} \right) \left((V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2 \right)$$
$$i_D := 1 \frac{\text{mA}}{\text{V}^2} \left[(5\text{V} - 1\text{V}) \cdot .1\text{V} - \frac{(0.1\text{V})^2}{2} \right] = 395 \mu\text{A}$$

$$R_D = \frac{5\text{V} - 0.1\text{V}}{395 \mu\text{A}} = 12.405 \text{k}\Omega$$

$$R_{DSeff} = \frac{V_{DS}}{I_D} = \frac{0.1\text{V}}{395 \mu\text{A}} = 253 \Omega$$

Figure 5.23 Circuit for Example 5.5.



Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltage at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k'_n(W/L) = 1$ mA/V². Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

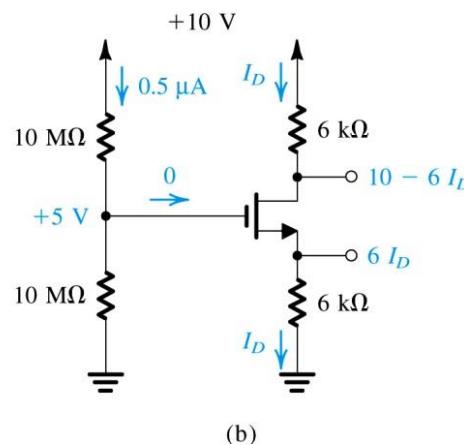
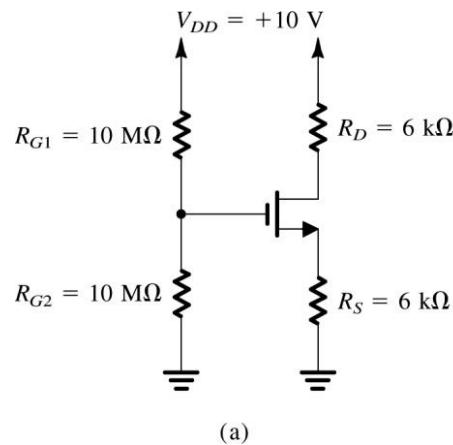


Figure 5.24 (a) Circuit for Example 5.6. (b) The circuit with some of the analysis details shown.

$$18I_D^2 - 25I_D + 8 = 0 \text{ [mA]}$$

$$I_D = 0.89 \text{ mA or } 0.5 \text{ mA}$$

$$V_S = 6I_D = 3\text{V}$$

$$V_{GS} = 5 - 6I_D = 2\text{V}$$

$$V_D = 10 - 6I_D = 7\text{V}$$

$$V_G = 5 \text{ V due to the voltage divider}$$

$$V_{GS} = 5 \text{ V} - 6I_D$$

$$I_D = \frac{1}{2}k'_n \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2$$

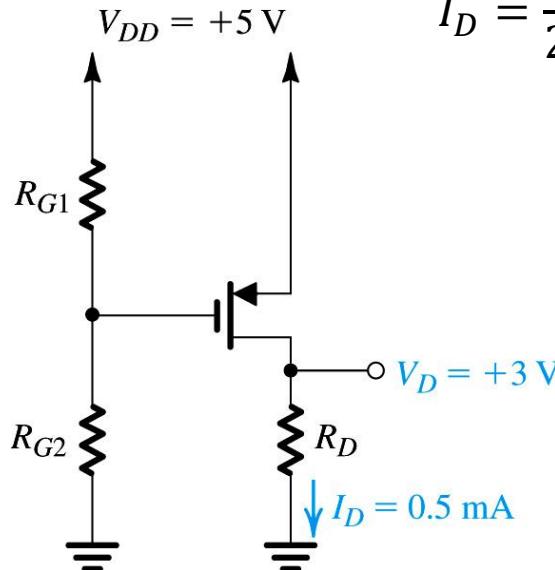
$$I_D = \frac{1}{2} \left(1 \frac{\text{mA}}{\text{V}^2} \right) ((5 - 6I_D - 1)\text{V})^2$$

$$I_D = \frac{1}{2} (4 - 6I_D)^2 [\text{mA}]$$



Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5 \text{ mA}$ and $V_D = +3 \text{ V}$. Let the enhancement-type PMOS transistor have $V_{tp} = -1 \text{ V}$ and $k'_p(W/L) = 1 \text{ mA/V}^2$. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?



$$I_D = \frac{1}{2} k'_p \left(\frac{W}{L} \right) |V_{ov}|^2 \quad V_{ov} = \sqrt{\frac{I_D}{\frac{1}{2} k'_n \left(\frac{W}{L} \right)}} \quad V_{ov} := \sqrt{\frac{0.5 \text{ mA}}{\frac{1}{2} \cdot 1 \frac{\text{mA}}{\text{V}^2}}} = 1 \text{ V}$$
$$V_{SG} = |V_{tp}| + |V_{ov}| = 1 \text{ V} + 1 \text{ V} = 2 \text{ V}$$

Therefore $V_G = 3 \text{ V}$ which can be set by the proper ratio of bias resistors and

$$R_D = \frac{3 \text{ V}}{0.5 \text{ mA}} = 6.0 \text{ k}\Omega$$

Will stay in saturation until V_D exceed V_G by $|V_{tp}|$ which would be 4 V limiting R_D to

$$R_D < \frac{4 \text{ V}}{0.5 \text{ mA}} = 8.0 \text{ k}\Omega$$

Figure 5.25 Circuit for Example 5.7.

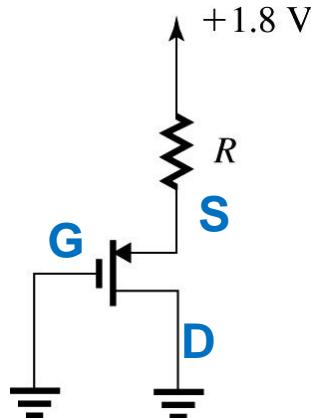


Exercise 5.14

For the circuit in Fig. E5.14, find the value of R that results in the PMOS transistor operating with an overdrive voltage $|V_{OV}| = 0.6$ V. The threshold voltage is $V_{tp} = -0.4$ V, the process transconductance parameter $k'_p = 0.1$ mA/V², and the $W/L = 10 \mu\text{m}/0.18\mu\text{m}$.

$$V_{OV} = V_{GS} - V_{tp} \quad V_{GS} = -0.6 - -0.4 = -1\text{V}$$

$$I_D = \frac{1}{2} k'_p \left(\frac{W}{L} \right) |V_{OV}|^2 \quad \frac{1}{2} \cdot 0.1 \frac{\text{mA}}{\text{V}^2} \cdot \frac{10}{0.18} (-0.6\text{V})^2 = 1\text{mA}$$



$$I_D R_D = 0.8\text{V}$$

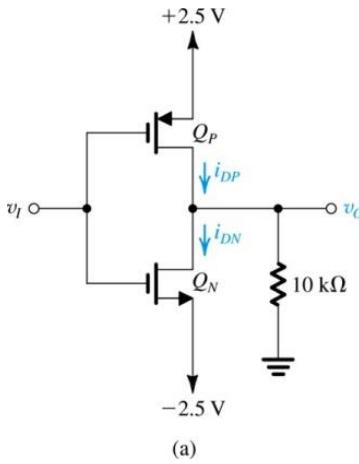
$$R_D = \frac{0.8\text{V}}{I_D} = 800\Omega$$

Figure E5.14

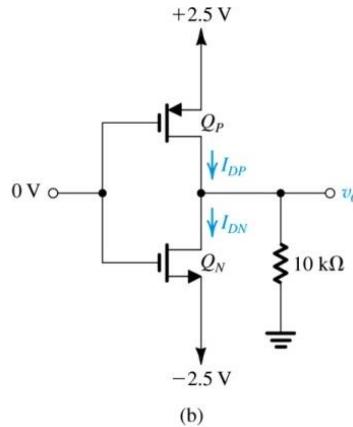


Example 5.8a

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , as well as the voltage v_O , for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .



Since Q_N and Q_P are perfectly matched and are operating at equal values of $|V_{GS}|$ (2.5 V), the circuit is symmetrical, which dictates that $v_O = 0 \text{ V}$. Thus both Q_N and Q_P are operating with $|V_{DG}| = 0 \text{ V}$ and, hence, in saturation. The drain currents can now be found from



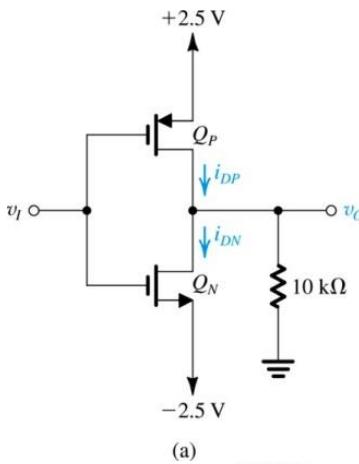
$$I_{DP} = I_{DN} = \frac{1}{2} k'_{n,p} \left(\frac{W_{n,p}}{L_{n,p}} \right) |V_{OV}|^2 = 1.125 \text{ mA}$$

Figure 5.26 Circuits for Example 5.8.



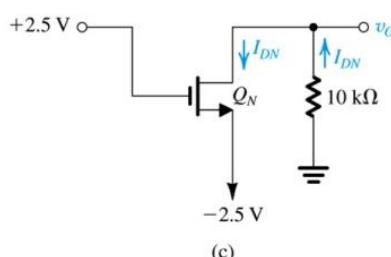
Example 5.8b

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $l = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , as well as the voltage v_O , for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .



Now, $v_I = +2.5 \text{ V}$. Transistor Q_P will have a V_{SG} of zero and thus will be cutoff, reducing the circuit to that shown in Fig. 5.26(c). We note that v_O will be negative, and thus v_{GD} will be greater than V_{tn} causing Q_N to operate in the triode region. For simplicity we shall assume that v_{DS} is small and thus use

$$I_{DN} \approx k'_n \left(\frac{W_n}{L_n} \right) (V_{GS} - V_{tn}) V_{DS} = 1 \frac{\text{mA}}{\text{V}^2} (5\text{V} - 1\text{V}) (v_O - (-2.5\text{V}))$$



$$I_{DP} = 0 \text{ mA}$$

$$I_{DN} = 0.244 \text{ mA}$$

$$I_{DN} = \frac{0 - v_O}{10 \text{ k}\Omega}$$

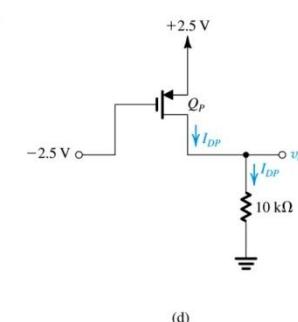
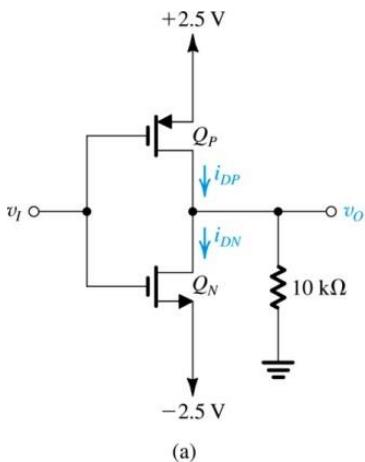
$$v_O = -2.44 \text{ V}$$

Figure 5.26 Circuits for Example 5.8.



Example 5.8c

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $l = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , as well as the voltage v_O , for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .



$$I_{DN} = 0 \text{ mA}$$

$$I_{DP} \approx k'_p \left(\frac{W_p}{L_p} \right) (V_{SG} - |V_{tp}|) V_{SD} = 1 \frac{\text{mA}}{\text{V}^2} (5\text{V} - 1\text{V}) (2.5\text{V} - v_O)$$

$$I_{DP} = \frac{v_O}{10\text{k}\Omega}$$

$$I_{DP} = 0.244 \text{ mA}$$

$$v_O = +2.44 \text{ V}$$

Finally, for $v_I = -2.5 \text{ V}$. Transistor Q_N will be cutoff, reducing the circuit to that shown in Fig. 5.26(d). We note that v_O will be positive, and thus v_{DG} will be greater than V_{tp} causing Q_P to operate in the triode region.



Exercise 5.15a

The NMOS and PMOS transistors in the circuit of Fig. E5.15 are matched, with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , as well as the voltage v_o , for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .

$v_I = 0 \text{ V}$; the circuit is matched so that the output is 0 V so VGS is 0 V and each device is turned off so $I_{DN} = I_{DP} = 0$.

$v_I = 2.5 \text{ V}$; Q_N is on so then Q_P is off so $i_{DP} = 0$.

$$I_{DN} = \frac{1}{2} k'_n \left(\frac{W}{L} \right) |V_{GS} - V_t|^2 = \frac{1}{2} \frac{1 \text{ mA}}{\text{V}^2} (V_G - V_S - V_t)^2$$

$$V_S = v_o = I_{DN} 10 \text{ k}\Omega$$

$$I_{DN} = \frac{1}{2} \frac{1 \text{ mA}}{\text{V}^2} (2.5 - I_{DN} 10 \text{ k}\Omega - 1)^2 = 0.104 \text{ mA}$$

$$v_o = I_{DN} 10 \text{ k}\Omega = 1.04 \text{ V}$$

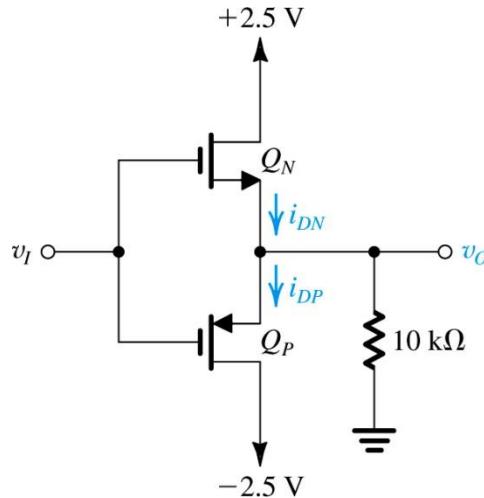


Figure E5.15



Exercise 5.15b

The NMOS and PMOS transistors in the circuit of Fig. E5.15 are matched, with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , as well as the voltage v_o , for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .

$v_I = -2.5 \text{ V}$; Q_P is on so then Q_N is off so $I_{DN} = 0$.

$$I_{DP} = \frac{1}{2} k'_p \left(\frac{W}{L} \right) (V_{SG} - V_t)^2 = \frac{1}{2} \frac{1 \text{ mA}}{\text{V}^2} (V_S - V_G - |V_t|)^2$$

$$V_S = v_o = -I_{DP} 10 \text{ k}\Omega$$

$$I_{DP} = \frac{1}{2} \frac{1 \text{ mA}}{\text{V}^2} (-I_{DP} 10 \text{ k}\Omega + 2.5 - 1)^2 = 0.104 \text{ mA}$$

$$v_o = -I_{DP} 10 \text{ k}\Omega = -1.04 \text{ V}$$

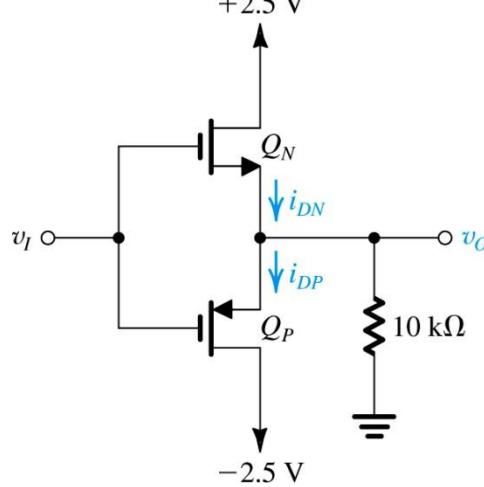
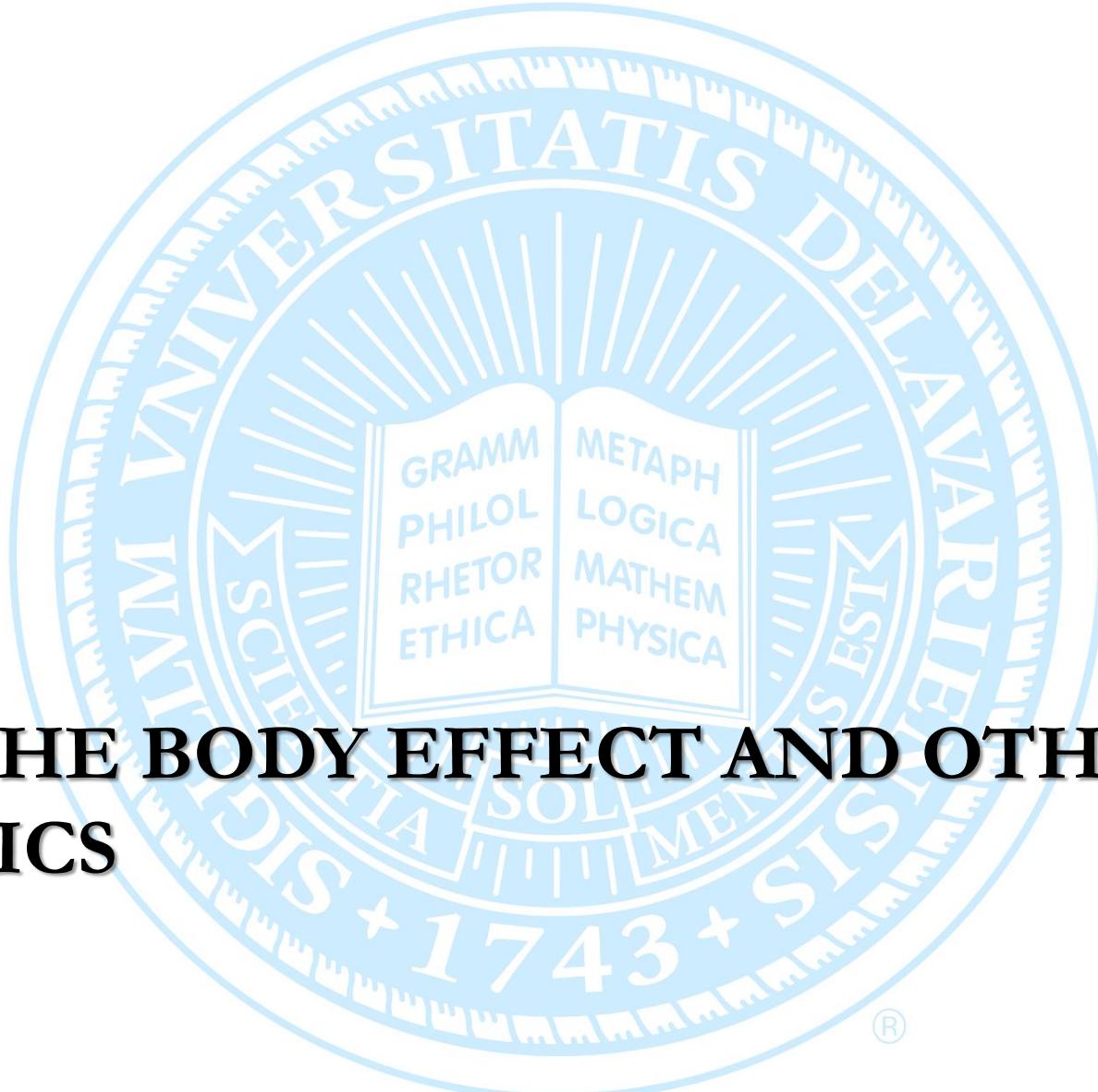


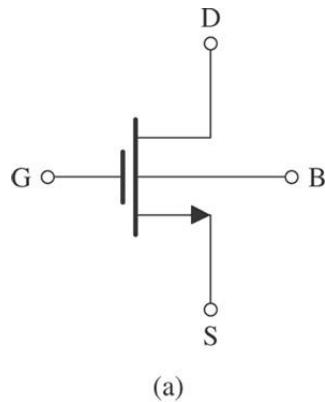
Figure E5.15



5.4 THE BODY EFFECT AND OTHER TOPICS



Modeling the Body Effect



In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the *pn* junction between the substrate and the induced channel having a constant zero (cutoff) bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether.

In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to maintain the cutoff condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit). The resulting reverse-bias voltage between source and body (V_{SB} in an *n*-channel device) will have an effect on device operation. The effect of V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage, V_t .

$$V_t = V_{t0} + \gamma \left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right]$$

Where ϕ_f is a physical parameter and $\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{c_{ox}}$



The Depletion-Type MOSFET

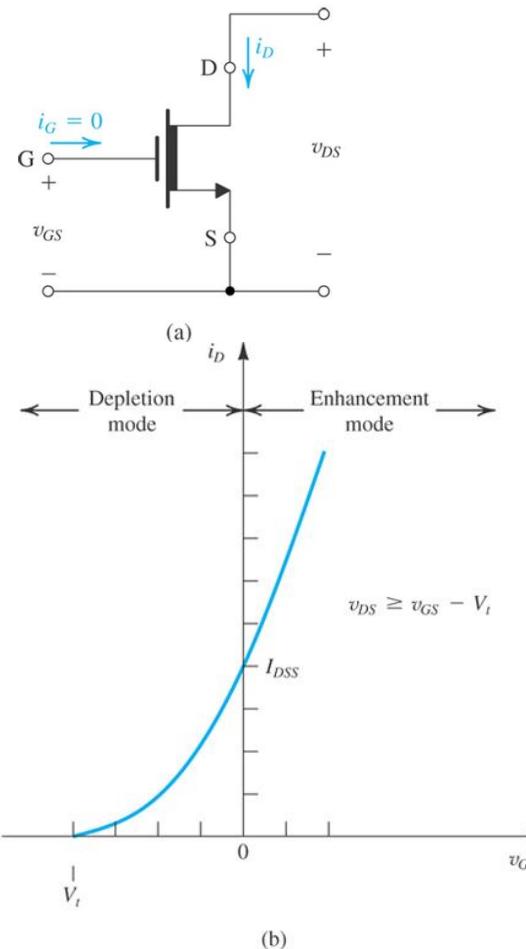


Figure 5.27 The circuit symbol (a) and the i_D - v_{GS} characteristic in saturation (b) for an *n*-channel depletion-type MOSFET.

Ch 5. MOSFETs

R. Martin



Comparison of FET Types

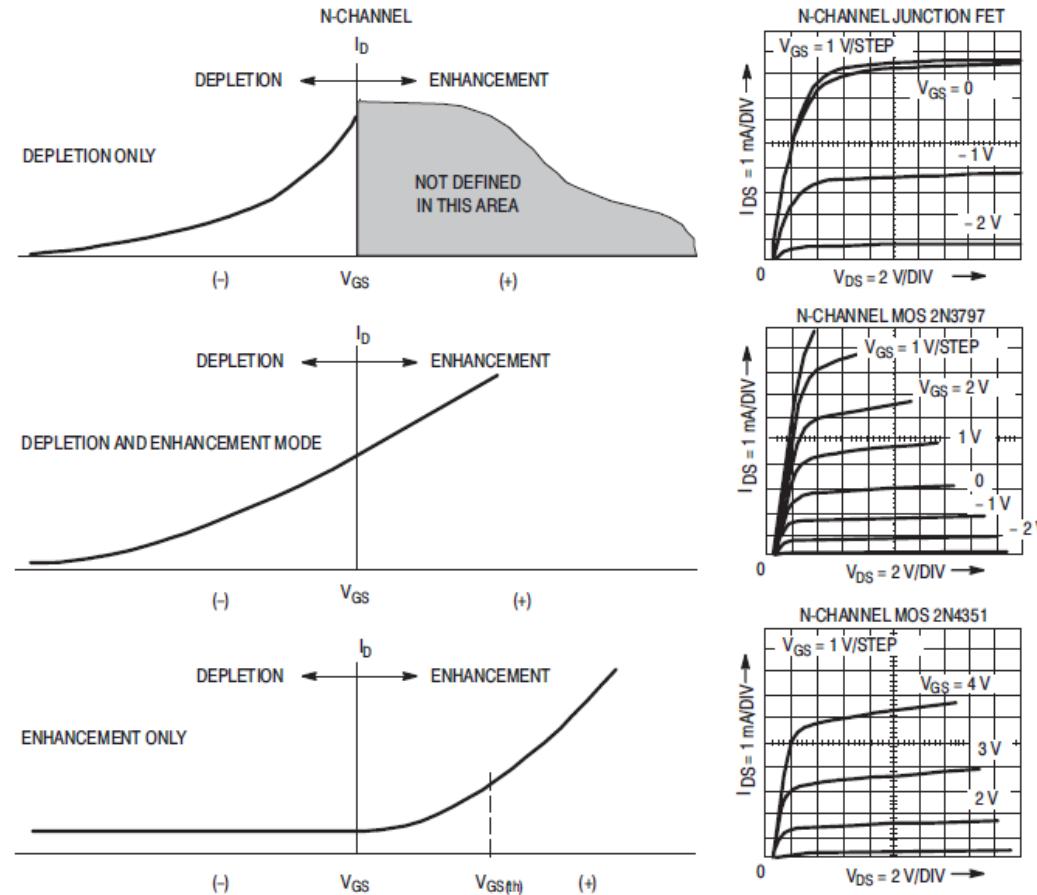


Figure 9. Transfer Characteristics and Associated Scope Traces for the Three FET Types



Homework #10

- Read Chapter 5
- Chapter 5 Problems:
 - 5.44
 - 5.48*
 - 5.55
 - 5.56*
 - 5.62
 - 5.63*

* Answers in Appendix L



Summary

- The enhancement-type MOSFET is currently the most widely used semiconductor device. It is the basis of CMOS technology, which is the most popular IC fabrication technology at this time. CMOS provides both *n*-channel (NMOS) and *p*-channel (PMOS) transistors, which increases design flexibility. The minimum MOSFET channel length achievable with a given CMOS process is used to characterize the process
- The overdrive voltage $|V_{OV}| = |V_{GS}| - |V_t|$ is the key quantity that governs the operation of the MOSFET. For amplifier applications, the MOSFET must operate in the saturation region.
- In saturation, i_D shows some linear dependence on v_{DS} as a result of the change in channel length. This channel-length modulation phenomenon becomes more pronounced as L decreases. It is modeled by ascribing an output resistance $r_o = |V_A|/I_D$ to the MOSFET model. Although the effect of r_o on the operation of discrete-circuit MOS amplifiers is small, that is not the case in IC amplifiers.



Summary

- In the analysis of dc MOSFET circuits, if a MOSFET is conducting, but its region of operation (saturation or triode) is not known, one assumes saturation-mode operation. Then, one solves the problem and checks to determine whether the assumption was justified. If not, then the transistor is operating in the triode region, and the analysis is done accordingly.
- The depletion-type MOSFET has an implanted channel and thus can be operated in either the depletion or enhancement mode. It is characterized by the same equations used for the enhancement device except for having a negative V_{tn} (positive V_{tp} for depletion PMOS transistors).