

UNIVERSITY *of* DELAWARE

# Chapter 2

## Operational Amplifiers





# IN THIS CHAPTER YOU WILL LEARN

1. The terminal characteristics of the ideal op amp.
2. How to analyze circuits containing op amps, resistors, and capacitors.
3. How to use op amps to design amplifiers having precise characteristics.
4. How to design more sophisticated op-amp circuits, including summing amplifiers, instrumentation amplifiers, integrators, and differentiators.
5. Important nonideal characteristics of op amps and how these limit the performance of basic op-amp circuits.



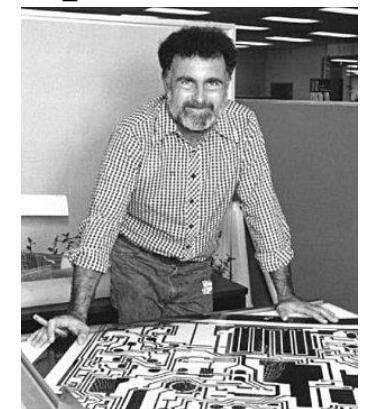
# Brief History

- 1964 – Bob Widlar designs the first op-amp: the 702.
  - Using only 9 transistors, it attains a gain of over 1000
  - Highly expensive: \$300 per op-amp
- 1965 – Bob Widlar designs the 709 op-amp which more closely resembles the current uA741
  - This op-amp achieves an open-loop gain of around 60,000.
  - The 709's largest flaw was its lack of short circuit protection.

The uA741 Operational Amplifier  
[www.calvin.edu](http://www.calvin.edu)

<http://hackaday.com/2014/04/08/heroes-of-hardware-revolution-bob-widlar/>

[https://en.wikipedia.org/wiki/Bob\\_Widlar](https://en.wikipedia.org/wiki/Bob_Widlar)



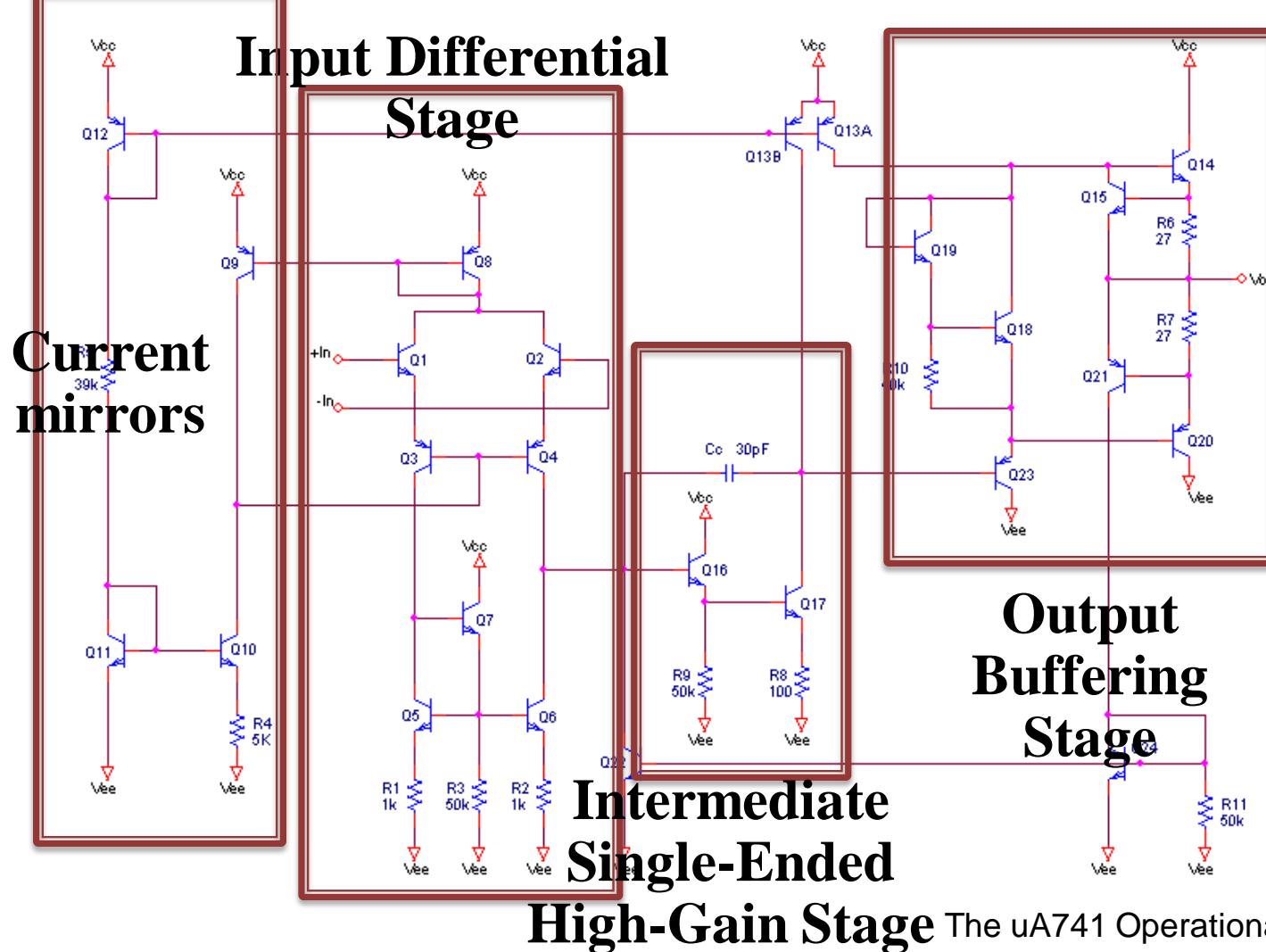


# Brief History (cont)

- After Widlar left Fairchild, Dave Fullagar continued op-amp design and came up with the uA741 which is the most popular operational amplifier of all time.
  - This design's basic architecture is almost identical to Widlar's 309 op-amp with one major difference: the inclusion of a fixed internal compensation capacitor.
    - This capacitor allows the uA741 to be used without any additional, external circuitry, unlike its predecessors.
  - The other main difference is the addition of extra transistors for short circuit protection.
  - This op-amp has a gain of around 250,000



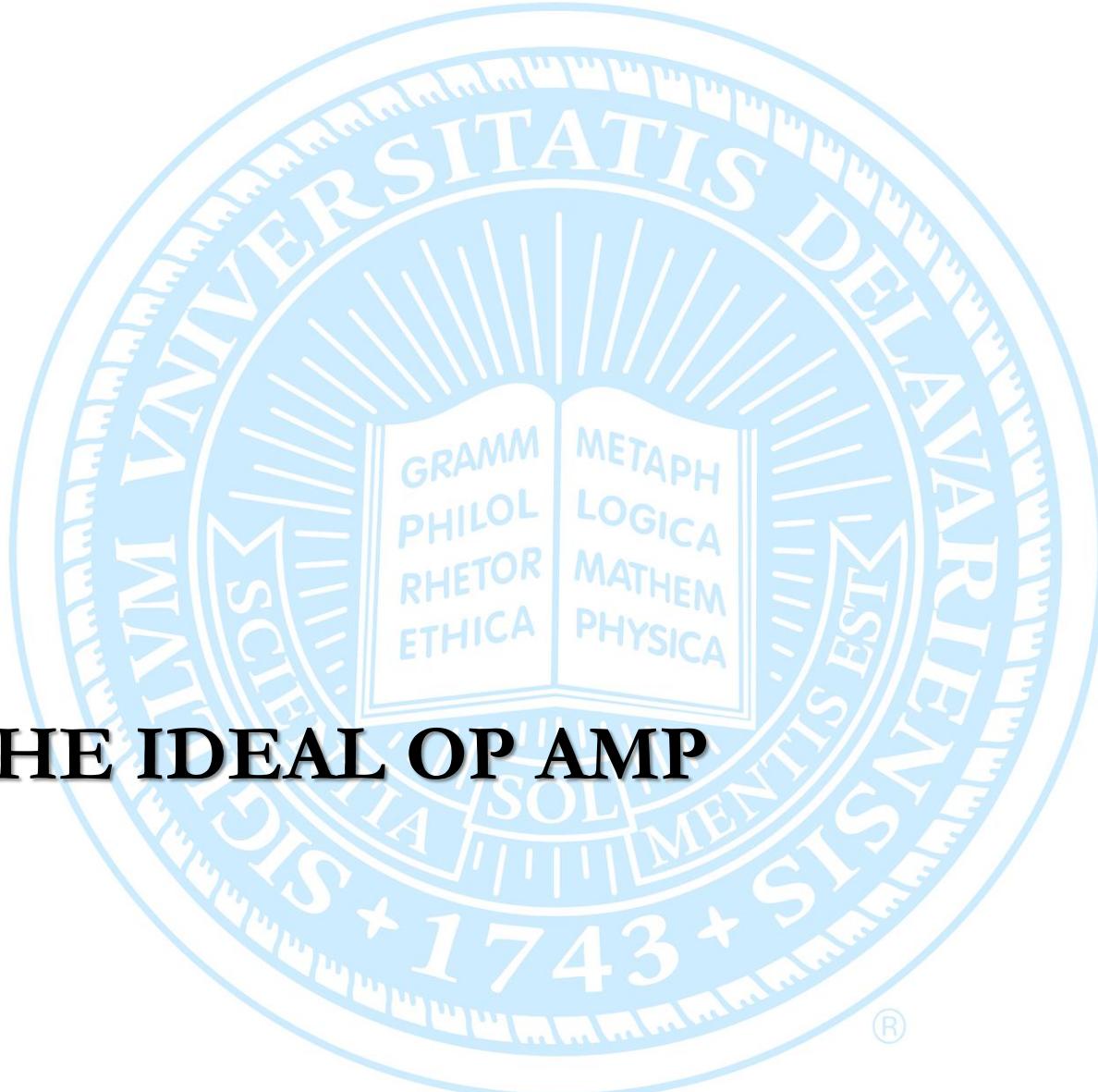
# uA741 Schematic





# Concluding Remarks

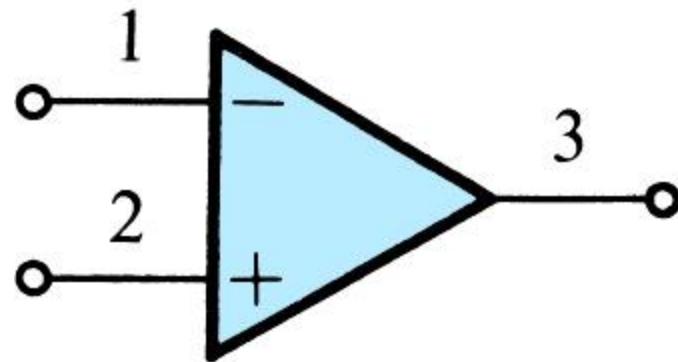
- The uA741 operational amplifier is a versatile circuit that is not adversely affected by outside interference.
  - Changes in beta, resistor values, and temperature have little effect on the op-amp.
  - This shows how well the uA741 was designed.
- However, as technology continues to improve, CMOS amplifiers are beginning to become more popular than their BJT cousins.



## 2.1 THE IDEAL OP AMP



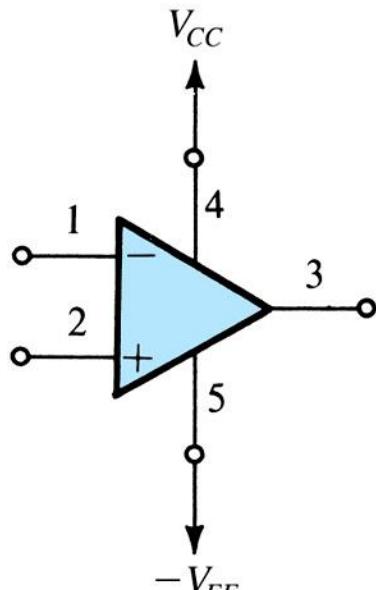
# Op-Amp Circuit Symbol



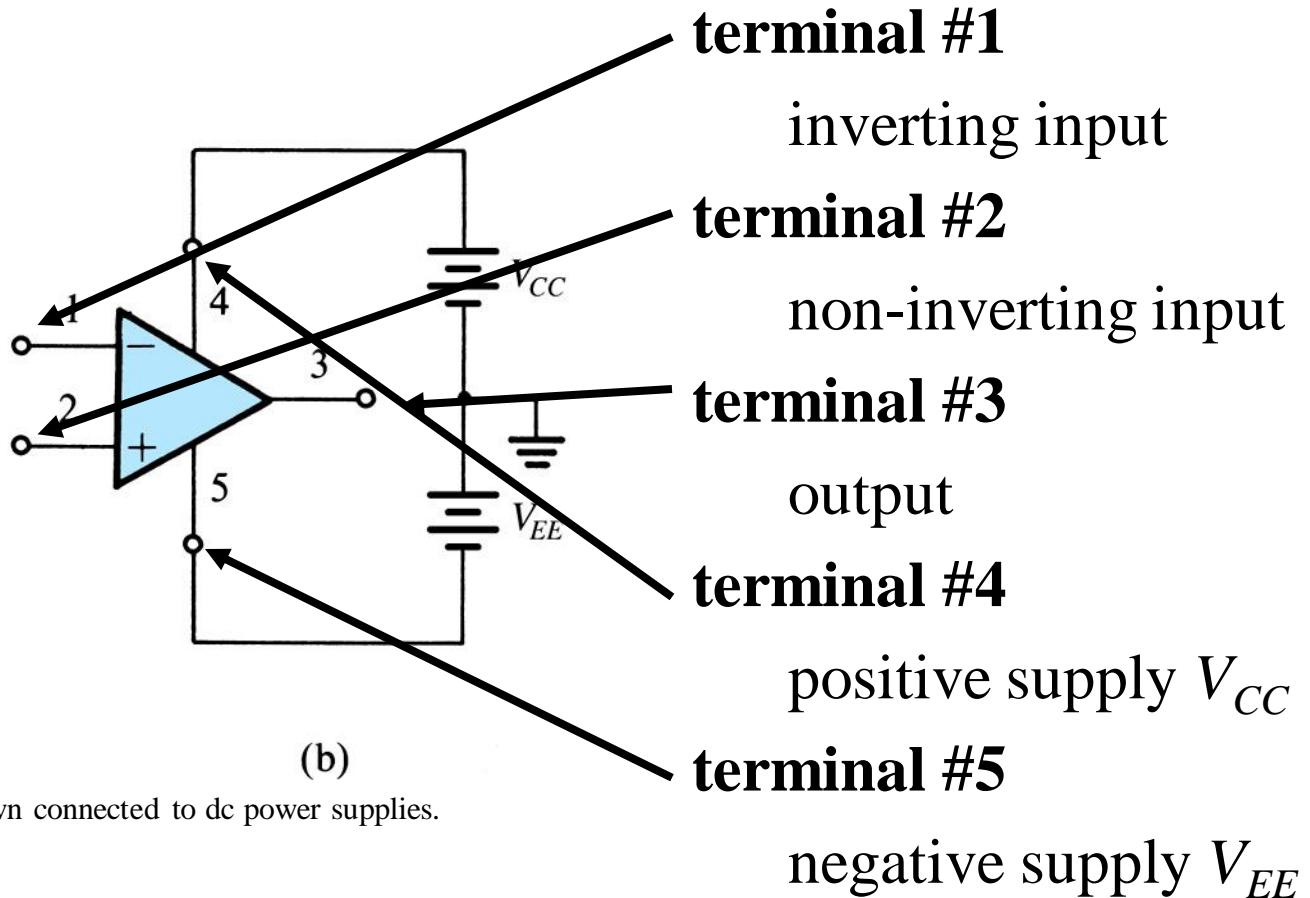
**Figure 2.1** Circuit symbol for the op amp.



# Op-Amp shown with supply terminals



(a)

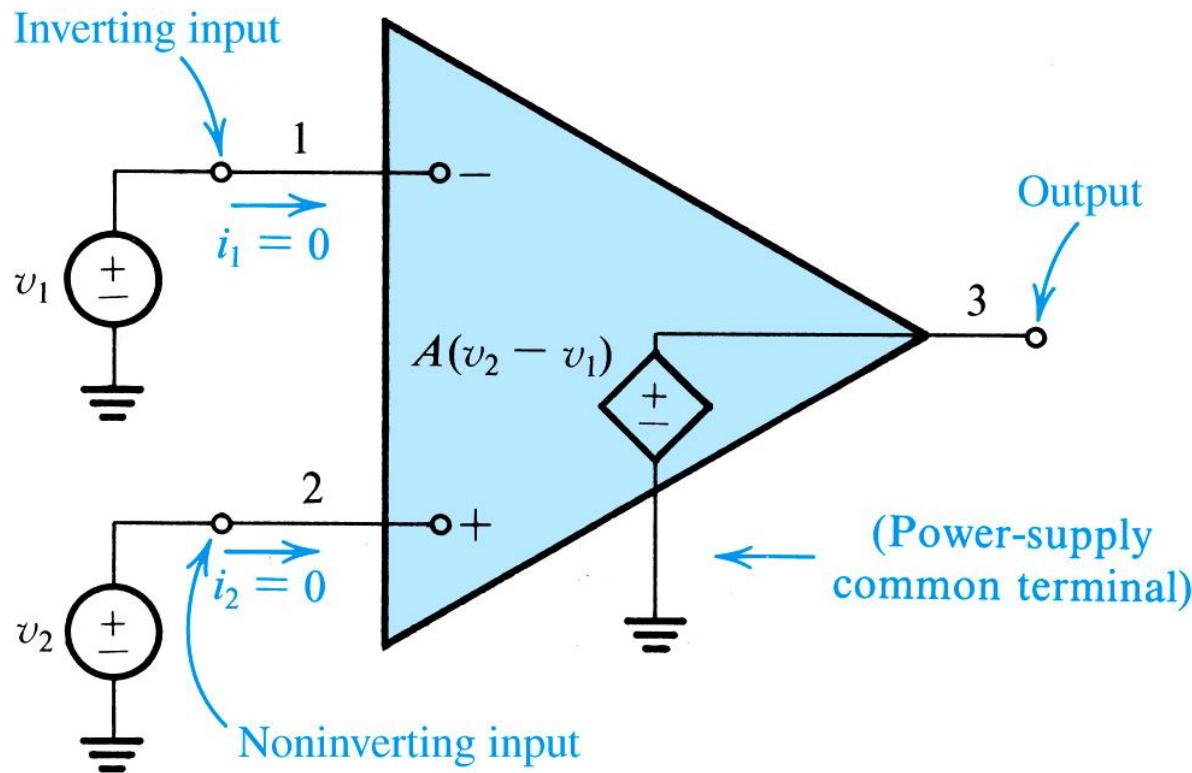


(b)

Figure 2.2 The op amp shown connected to dc power supplies.



# Equivalent Circuit

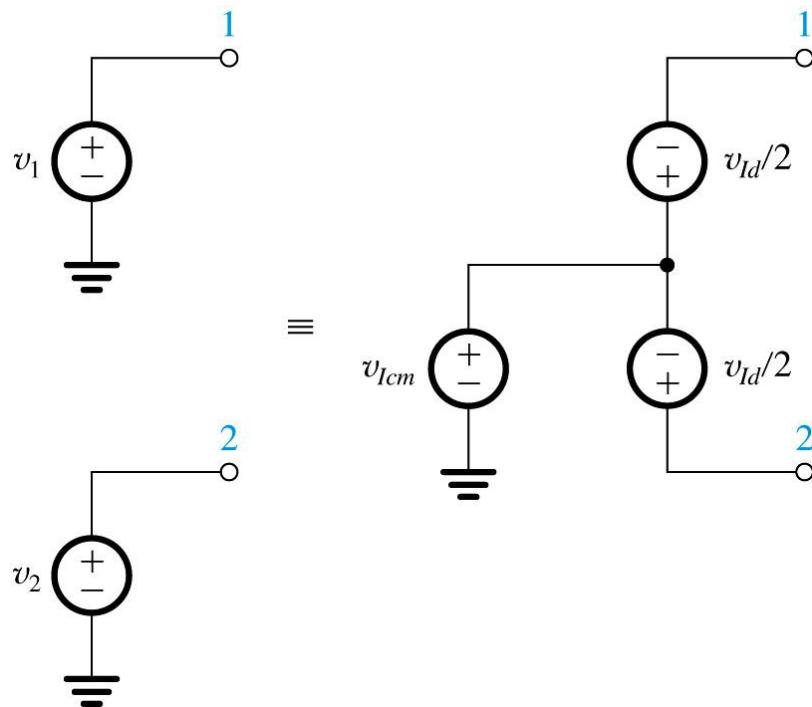


Gain,  $A$ , is called the differential gain or the open-loop gain

Figure 2.3 Equivalent circuit of the ideal op amp.



# Differential and Common-Mode Signals



**Figure 2.4** Representation of the signal sources  $v_1$  and  $v_2$  in terms of their differential and common-mode components.

The differential input signal  $v_{Id}$  is simply the difference between the two input signals  $v_1$  and  $v_2$ ; that is,

$$v_{Id} = v_2 - v_1$$

The common-mode input signal  $v_{Icm}$  is the average of the two input signals  $v_1$  and  $v_2$ ; namely

$$v_{Icm} = \frac{1}{2}(v_1 + v_2)$$

$$v_1 = v_{Icm} - \frac{v_{Id}}{2}$$

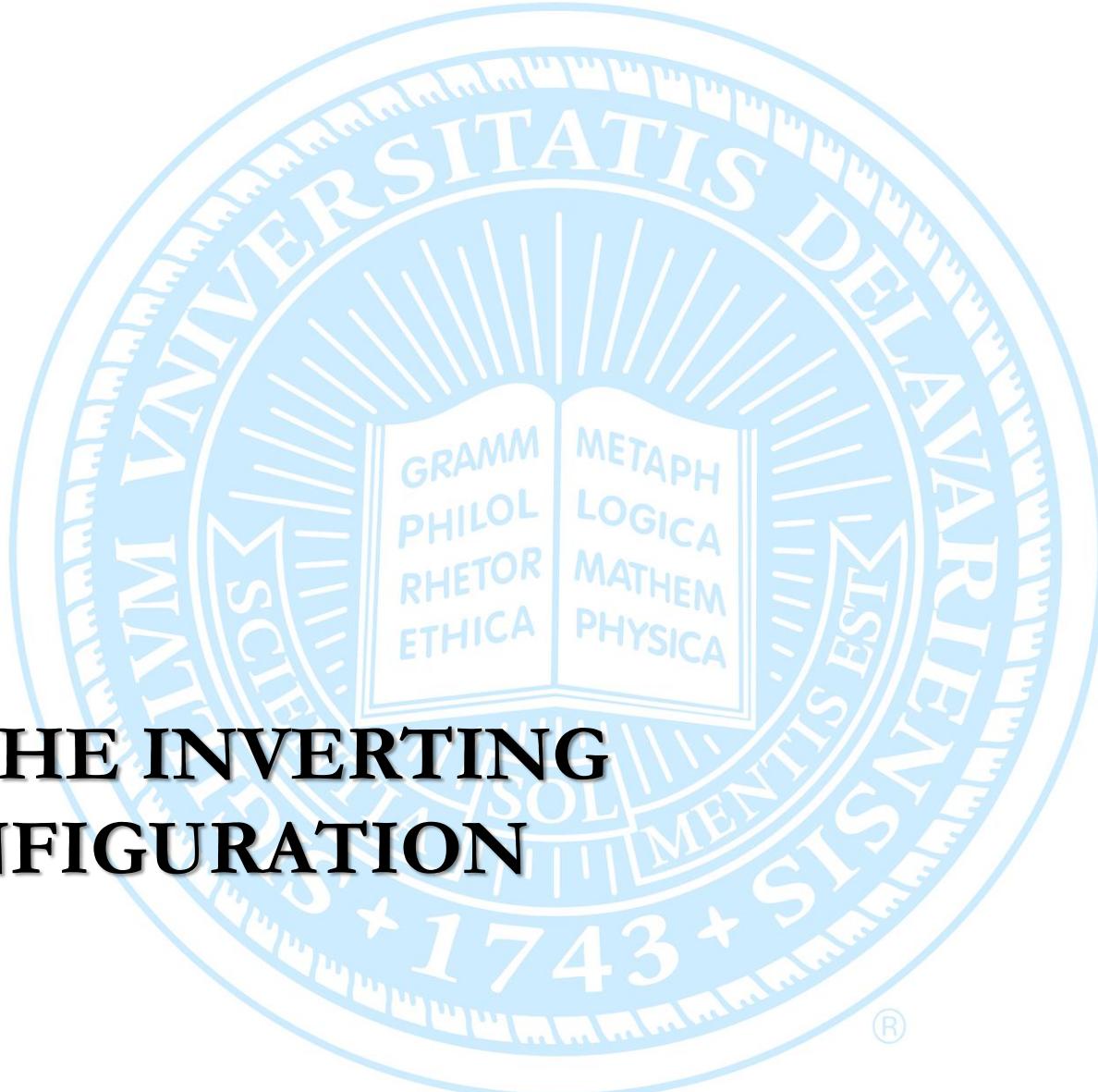
$$v_2 = v_{Icm} + \frac{v_{Id}}{2}$$



# Characteristics of the Ideal Op Amp

1)input impedance	Infinite
2)output impedance	Zero
3)common-mode gain, $A_{cm}$	Zero
common-mode rejection, CMRR	Infinite
4)open-loop gain, $A$	Infinite
5)bandwidth	Infinite

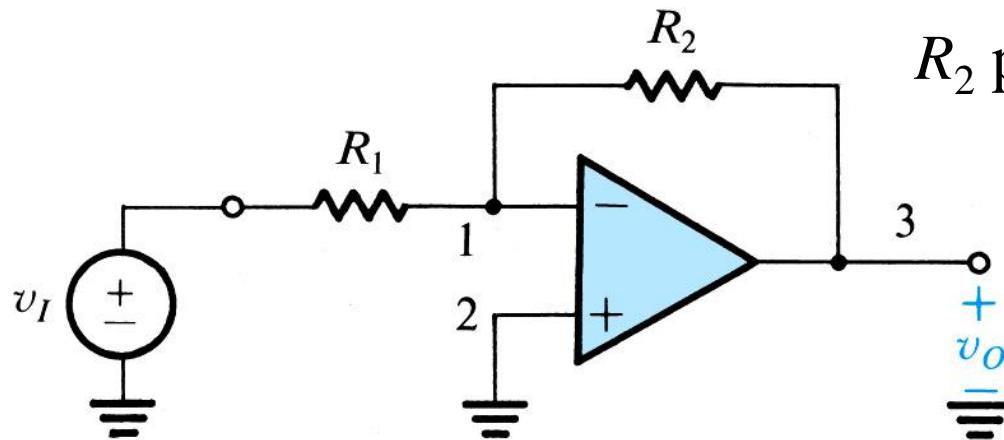
$$CMRR = 20 \log \left( \frac{A}{A_{cm}} \right)$$



## 2.2 THE INVERTING CONFIGURATION



# The Inverting Op-Amp Configuration



$R_2$  provides negative feedback

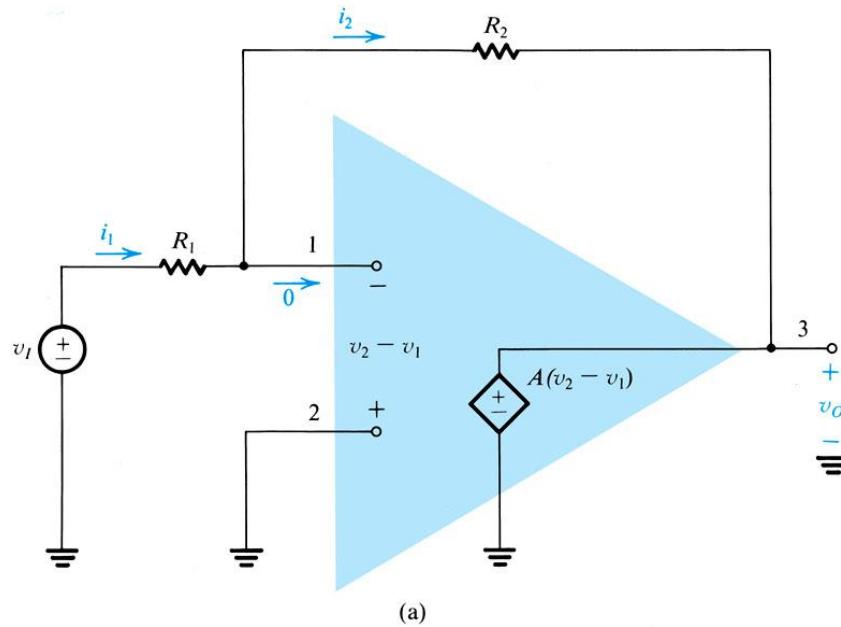
$$v_o = A(v_2 - v_1)$$

$$(v_2 - v_1) = \frac{v_o}{A}$$

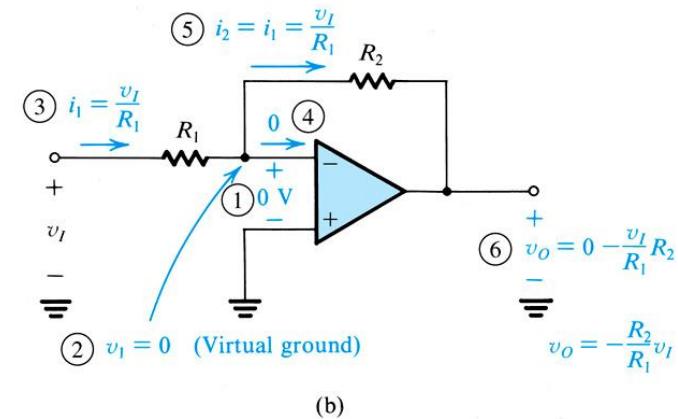
Open loop gain,  
 $A \sim \infty$

$$v_1 \approx v_2 = 0V$$

A virtual short circuit means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain  $A$ . But terminal 2 happens to be connected to ground; thus  $v_2 = 0$  and  $v_1 = 0$ . We speak of terminal 1 as being a virtual ground - that is, having zero voltage but not physically connected to ground.



(a)



(b)

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0V}{R_1} = \frac{v_I}{R_1}$$

$$v_O = v_1 - i_1 R_2 = 0V - \frac{v_I}{R_1} R_2 = -\frac{R_2}{R_1} v_I$$

The closed loop gain is independent of the open loop gain!



# Assuming Finite Open-Loop Gain

$$i_1 = \frac{v_I - \left( -\frac{v_O}{A} \right)}{R_1} = \frac{v_I + \frac{v_O}{A}}{R_1}$$

$$v_O = -\frac{v_O}{A} - i_1 R_2 = -\frac{v_O}{A} \left( \frac{v_I + \frac{v_O}{A}}{R_1} \right) R_2$$

$$G \equiv \frac{v_O}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

$A \gg 1 + \frac{R_2}{R_1}$  Minimizes the dependence of the closed loop gain,  $G$ , on the value of the open loop gain,  $A$ .

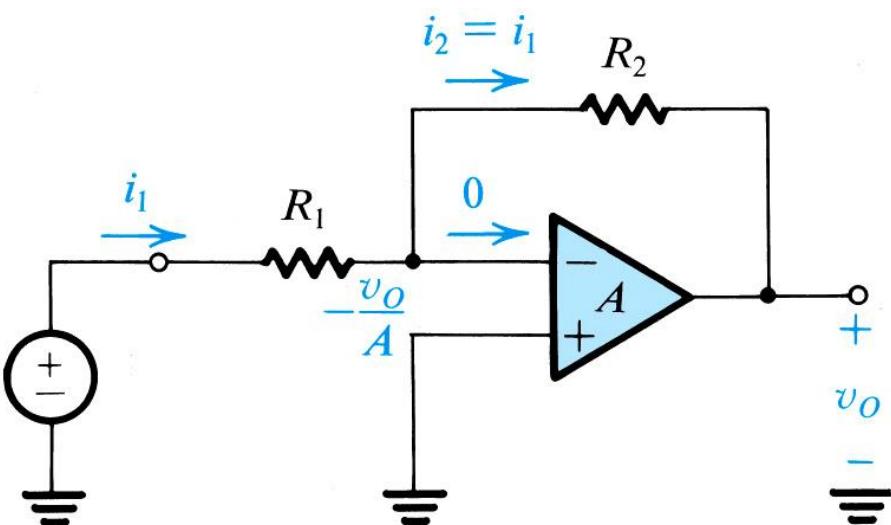
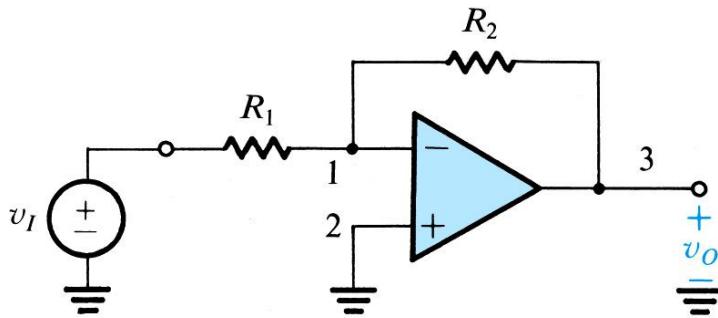


Figure 2.7 Analysis of the inverting configuration taking into account the finite open-loop gain of the op amp.



# Input and Output Resistances

What is input resistance for an inverting op-amp?



$$R_i = \frac{v_{In}}{i_{In}} = \frac{v_{In}}{(v_{In} - v_1)/R_1} = \frac{v_{In}}{v_{In}/R_1} = R_1$$

Figure 2.5 The inverting closed-loop configuration.

for the combination of ideal op-amp and external resistors, input resistance will be finite...

Since the output of the inverting configuration is taken at the terminals of the ideal voltage source  $A(v_2 - v_1)$ , it follows that the output resistance of the closed-loop amplifier is zero,  $R_o = 0 \Omega$ .



## Example 2.2

Assuming the op amp to be ideal, derive an expression for the closed-loop gain of the circuit shown in Fig. 2.8. Use this circuit to design an inverting amplifier with a gain of 100 and an input resistance of  $1 \text{ M}\Omega$ . Assume that for practical reasons it is required not to use resistors greater than  $1 \text{ M}\Omega$ .

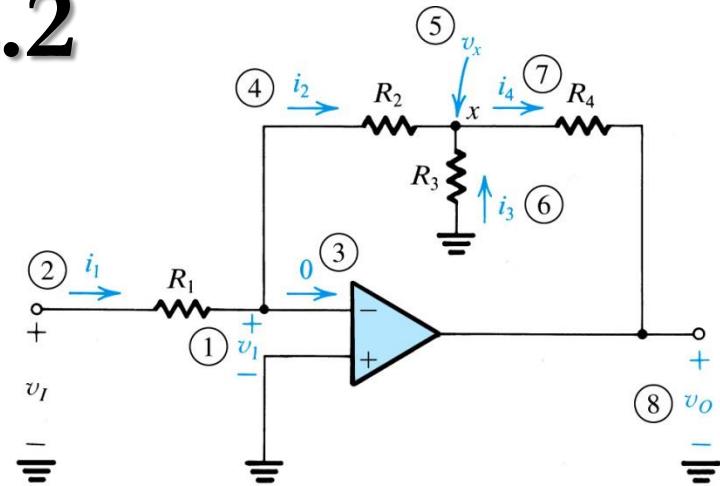


Figure 2.8: Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.

$$v_1 = \frac{-v_o}{A} \approx 0 \text{ V}$$

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I}{R_1} = i_2$$

$$v_x = v_1 - i_2 R_2 = 0 - \frac{v_I}{R_1} R_2 = -\frac{R_2}{R_1} v_I$$

$$i_3 = \frac{-v_x}{R_3} = \frac{R_2}{R_1 R_3} v_I$$

$$i_4 = i_2 + i_3 = \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I$$

$$v_O = v_x - i_4 R_4 = -\frac{R_2}{R_1} v_I - \left( \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I \right) R_4$$

$$\frac{v_O}{v_I} = - \left[ \frac{R_2}{R_1} + \frac{R_4}{R_1} \left( 1 + \frac{R_2}{R_3} \right) \right]$$

$$= -\frac{R_2}{R_1} \left( 1 + \frac{R_4}{R_2} + \frac{R_4}{R_3} \right)$$



## Example 2.2

Assuming the op amp to be ideal, derive an expression for the closed-loop gain of the circuit shown in Fig. 2.8. Use this circuit to design an inverting amplifier with a gain of 100 and an input resistance of  $1 \text{ M}\Omega$ . Assume that for practical reasons it is required not to use resistors greater than  $1 \text{ M}\Omega$ .

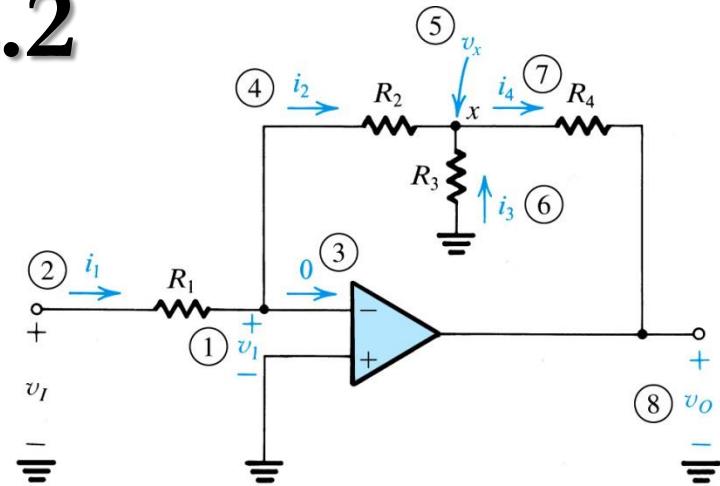


Figure 2.8: Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1} \left( 1 + \frac{R_4}{R_2} + \frac{R_4}{R_3} \right)$$

$$R_1 = 1 \text{ M}\Omega$$

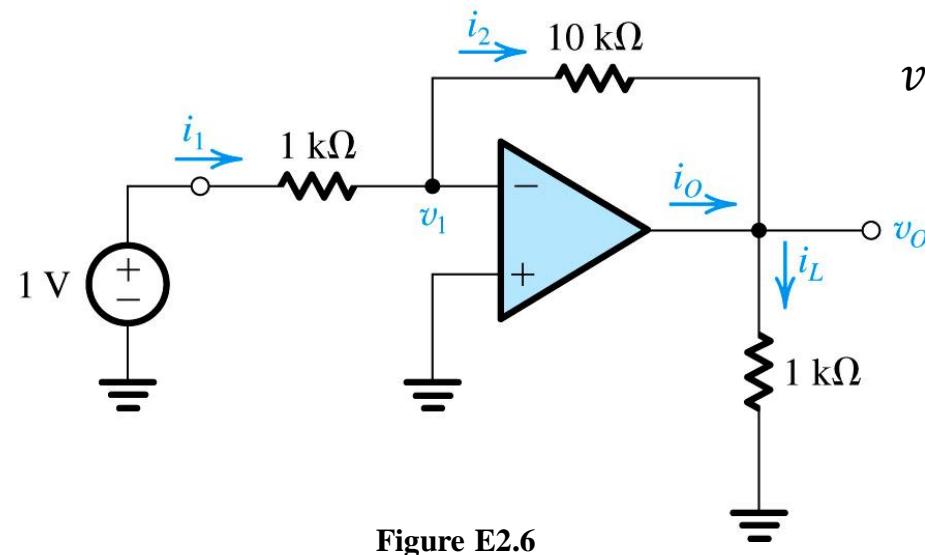
$$R_2 = 1 \text{ M}\Omega$$

$$R_4 = 1 \text{ M}\Omega$$

$$100 = 1 + \frac{R_4}{R_2} + \frac{R_4}{R_3} = 1 + 1 + \frac{1 \text{ M}\Omega}{R_3} \Rightarrow R_3 = \frac{1 \text{ M}\Omega}{98} = 10.2 \text{ k}\Omega$$



# Practice Exercise 2.6



$$v_1 = 0V$$

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I}{R_1} = \frac{1V}{1k\Omega} = 1mA$$

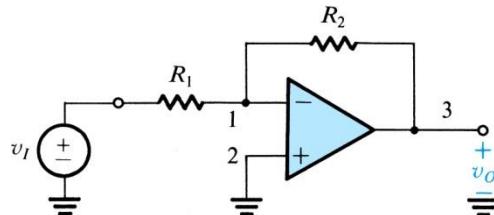
$$i_2 = i_1 = 1mA$$

$$v_O = -\frac{R_2}{R_1} = -10V$$

$$i_L = \frac{v_o}{R_L} = -10mA$$

$$i_O = i_L + i_2 = -11mA$$

Determine the values of  $v_1, i_1, i_2, v_O, i_L$ , and  $i_O$ . Also determine the voltage gain, current gain, and power gain.



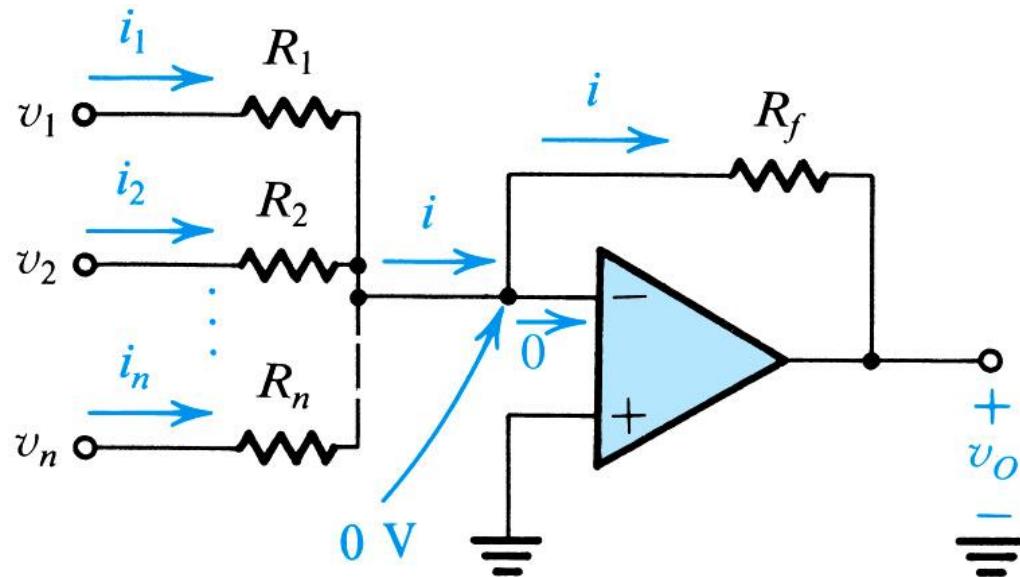
$$A_V = \frac{v_O}{v_I} = \frac{-10V}{1V} = -10V/V = 20dB$$

$$A_I = \frac{i_L}{i_I} = \frac{-10mA}{1mA} = -10A/A = 20dB$$

$$A_P = A_V A_I = 100W/W = 20dB$$



# The Weighted Summer



$$i_1 = \frac{v_1}{R_1}, i_2 = \frac{v_2}{R_2}, \dots, i_n = \frac{v_n}{R_n}$$

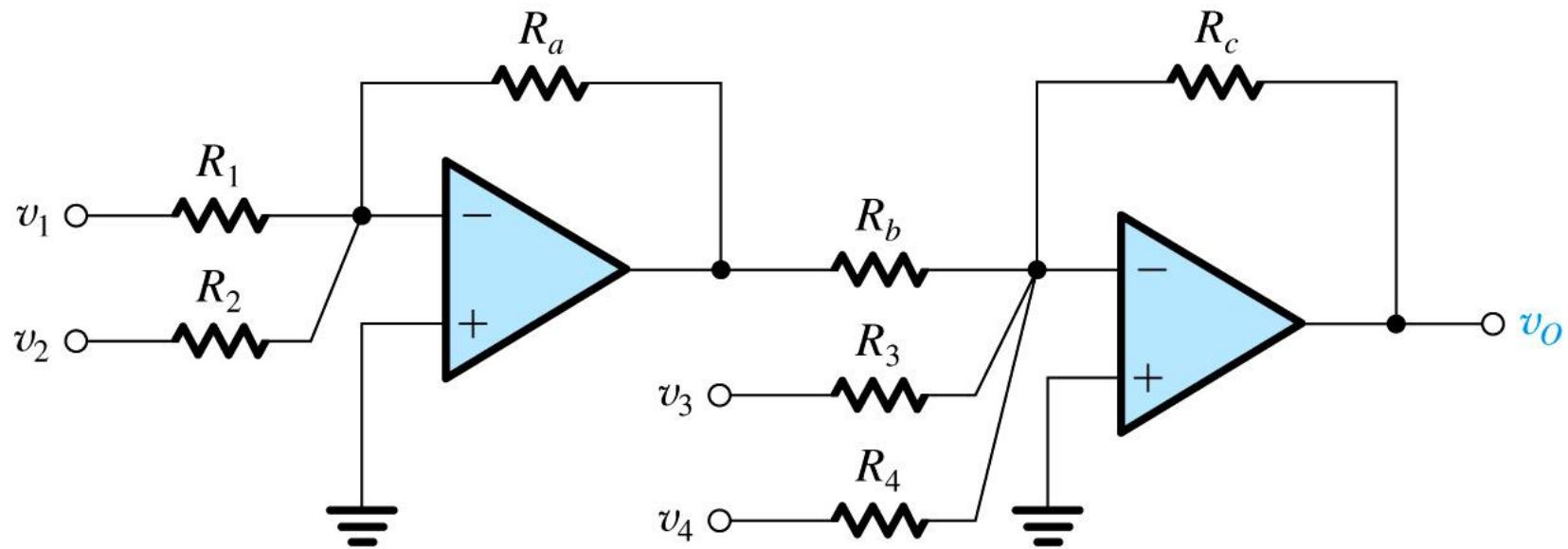
$$v_O = 0 - iR_f = -iR_f$$

$$v_O = - \left( \frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \dots + \frac{R_f}{R_n} v_n \right)$$

Figure 2.10 A weighted summer.

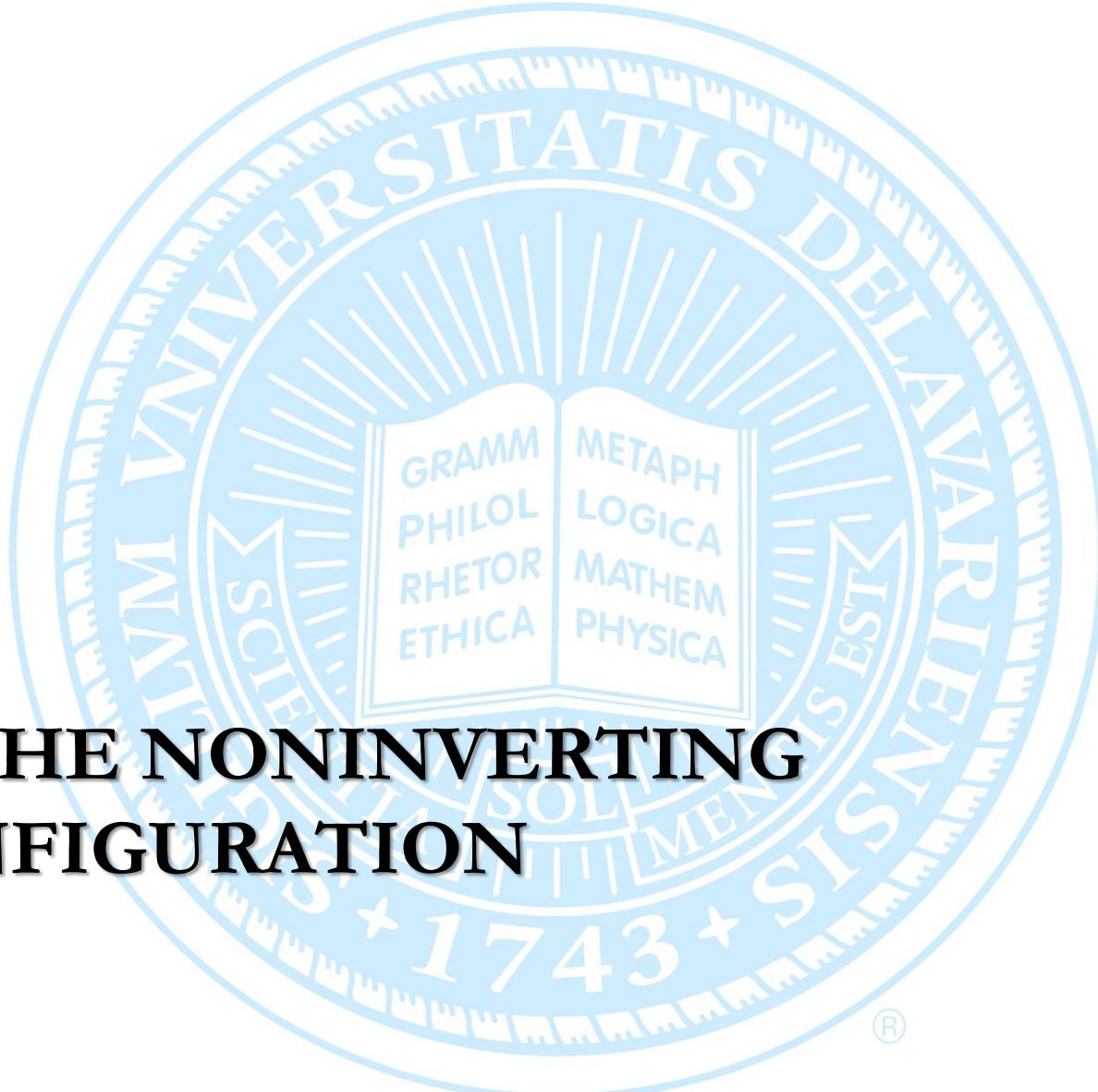


# Weighted Summer with Both Signs



**Figure 2.11** A weighted summer capable of implementing summing coefficients of both signs.

$$v_O = v_1 \left( \frac{R_a}{R_1} \right) \left( \frac{R_c}{R_d} \right) + v_2 \left( \frac{R_a}{R_b} \right) \left( \frac{R_c}{R_d} \right) - v_3 \left( \frac{R_c}{R_3} \right) - v_4 \left( \frac{R_c}{R_4} \right)$$



## 2.3 THE NONINVERTING CONFIGURATION



# Noninverting Op-Amp Configuration

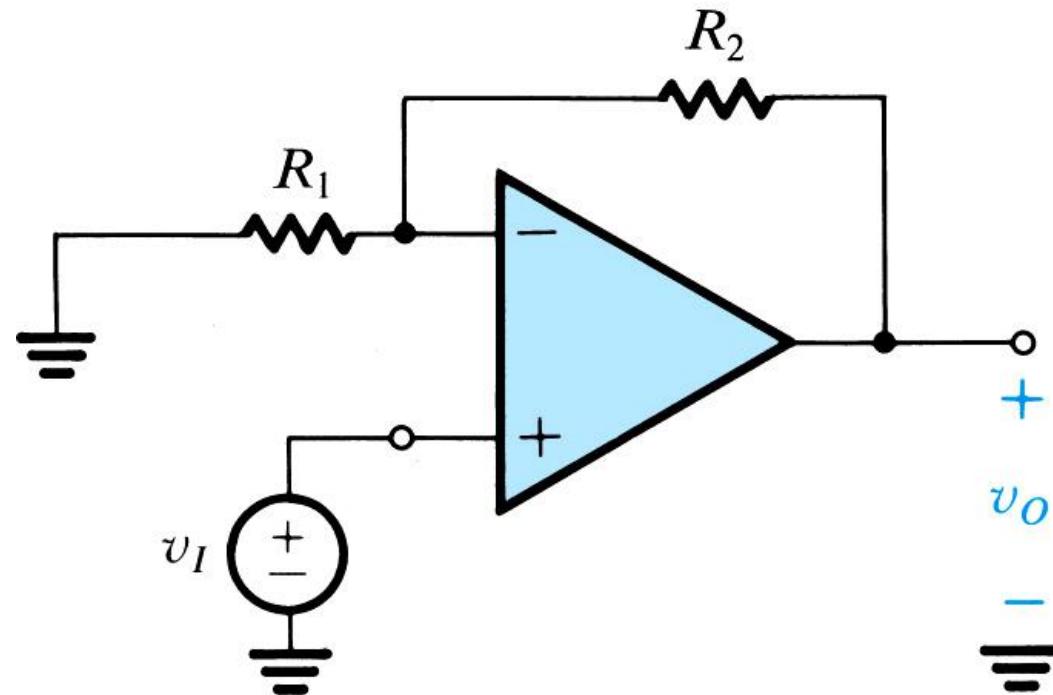
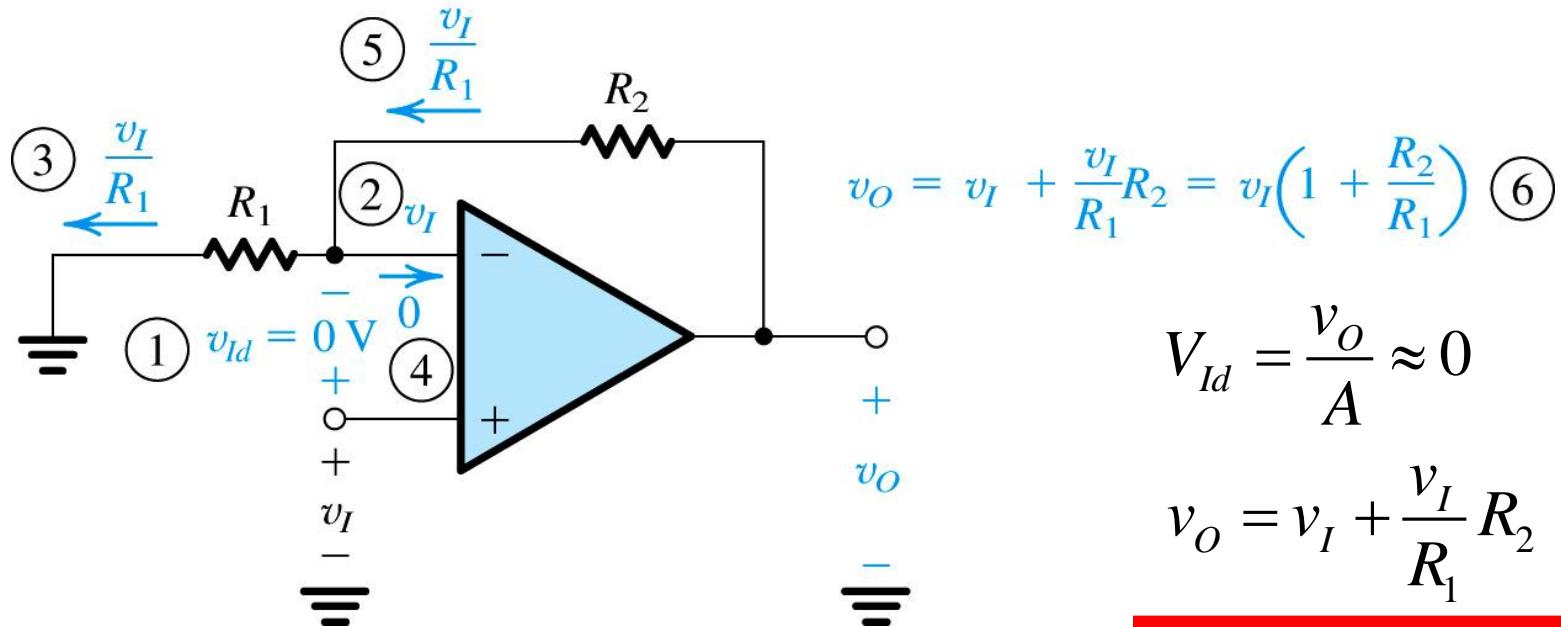


Figure 2.12 The noninverting configuration.



$$G \equiv \frac{v_O}{v_I} = 1 + \frac{R_2}{R_1}$$

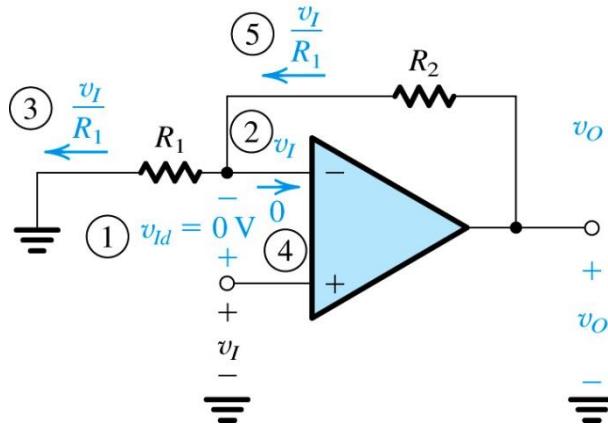
Figure 2.13 Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

## Alternate view – voltage divider

$$v_1 = v_O \left( \frac{R_1}{R_1 + R_2} \right) = v_I \quad \Rightarrow G \equiv \frac{v_O}{v_I} = \left( \frac{R_1 + R_2}{R_1} \right) = 1 + \frac{R_2}{R_1}$$



# Finite Open-Loop Gain, $A$



$$v_O = v_I + \frac{v_I}{R_1} R_2 = v_I \left(1 + \frac{R_2}{R_1}\right) \quad (6)$$

$$G \equiv \frac{v_O}{v_I} = \frac{1 + (R_2/R_1)}{1 + (1 + R_2/R_1)/A}$$

**Figure 2.13** Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

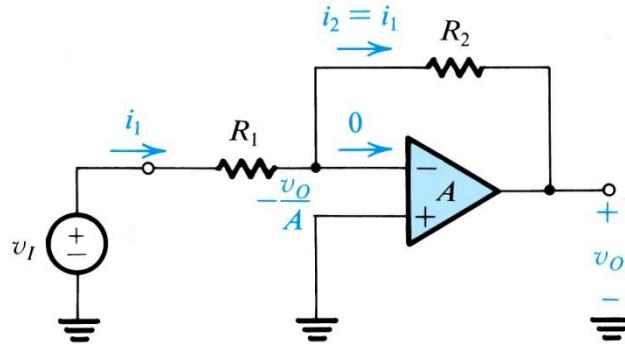
$$A \gg 1 + \frac{R_2}{R_1} \quad \text{Minimizes the dependence of the closed loop gain, } G, \text{ on the value of the open loop gain, } A.$$

$$\% \text{ gain error} = \frac{1 + (R_2/R_1)}{A + 1 + (R_2/R_1)} \times 100$$



# Finite Open-Loop Gain, $A$

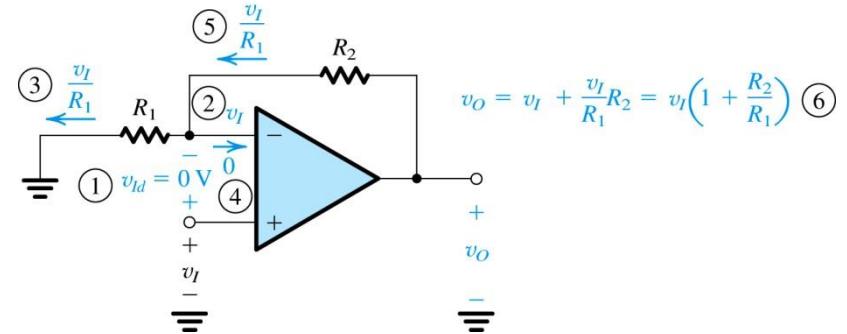
Inverting Configuration



**Figure 2.7** Analysis of the inverting configuration taking into account the finite open-loop gain of the op amp.

$$G \equiv \frac{v_O}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

Noninverting Configuration



**Figure 2.13** Analysis of the noninverting circuit. The sequence of the steps in the analysis is indicated by the circled numbers.

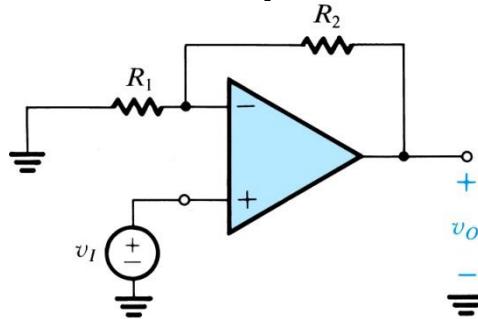
$$G \equiv \frac{v_O}{v_I} = \frac{1 + (R_2/R_1)}{1 + (1 + R_2/R_1)/A}$$

$$\% \text{ gain error} = \frac{1 + (R_2/R_1)}{A + 1 + (R_2/R_1)} \times 100$$



# Input and Output Resistances

What is input resistance for a noninverting op-amp?



$$R_i = \frac{v_{In}}{i_{In}} \approx \frac{v_{In}}{0A} = \infty \Omega$$

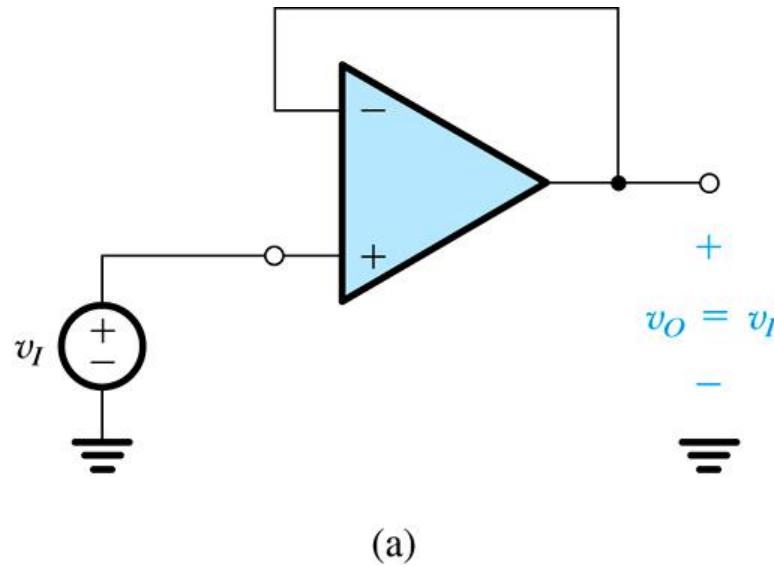
Figure 2.12 The noninverting configuration.

for the combination of ideal op-amp and external resistors, input resistance will be infinite...

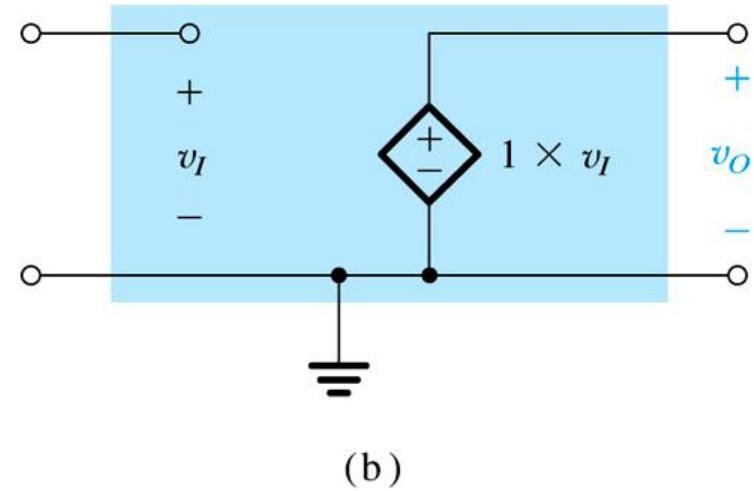
Since the output of the noninverting configuration is taken at the terminals of the ideal voltage source  $A(v_2 - v_1)$ , it follows that the output resistance of the closed-loop amplifier is zero,  $R_o = 0 \Omega$ .



# Unity Gain Buffer or Voltage Follower



(a)



(b)

Figure 2.14 (a) The unity-gain buffer or follower amplifier. (b) Its equivalent circuit model.

For the buffer amp, output voltage is equal (in both magnitude and phase) to the input source. However, any current supplied to the load is drawn from amplifier supplies ( $V_{CC}$ ,  $V_{EE}$ ) and not the input source ( $v_I$ ).



## Exercise 2.9

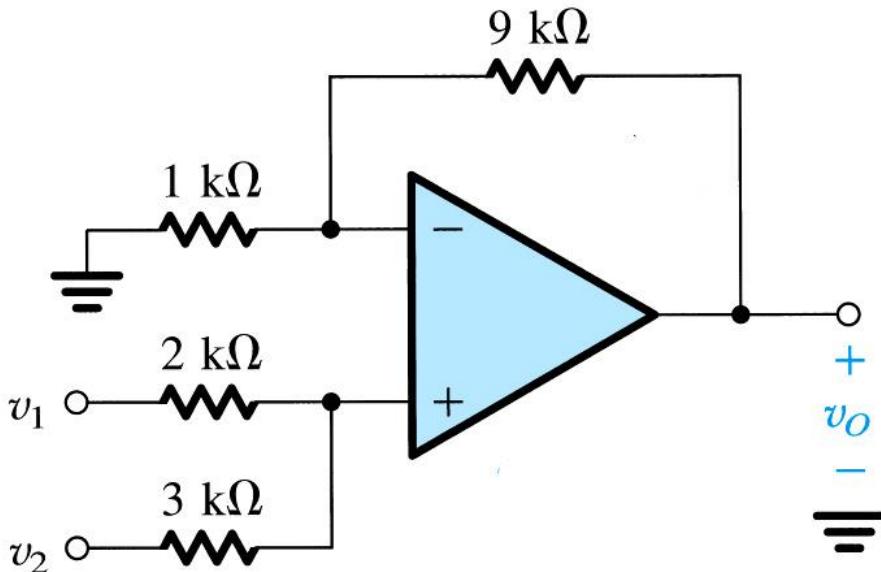


Figure E2.9

Use the superposition principle to find the output voltage of the circuit shown in Fig. E2.9.

$$G \equiv \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1} = 1 + \frac{9\text{k}\Omega}{1\text{k}\Omega} = 10$$

1) First set  $v_2$  to 0V.

$$v_{o1} = Gv_{i1} = 10 \frac{3\text{k}\Omega}{3\text{k}\Omega + 2\text{k}\Omega} v_1 = 6v_1$$

2) Then set  $v_1$  to 0V.

$$v_{o2} = Gv_{i2} = 10 \frac{2\text{k}\Omega}{3\text{k}\Omega + 2\text{k}\Omega} v_2 = 4v_2$$

3) Then sum the two outputs

$$v_o = v_{o1} + v_{o2} = 6v_1 + 4v_2$$



# Exercise 2.13

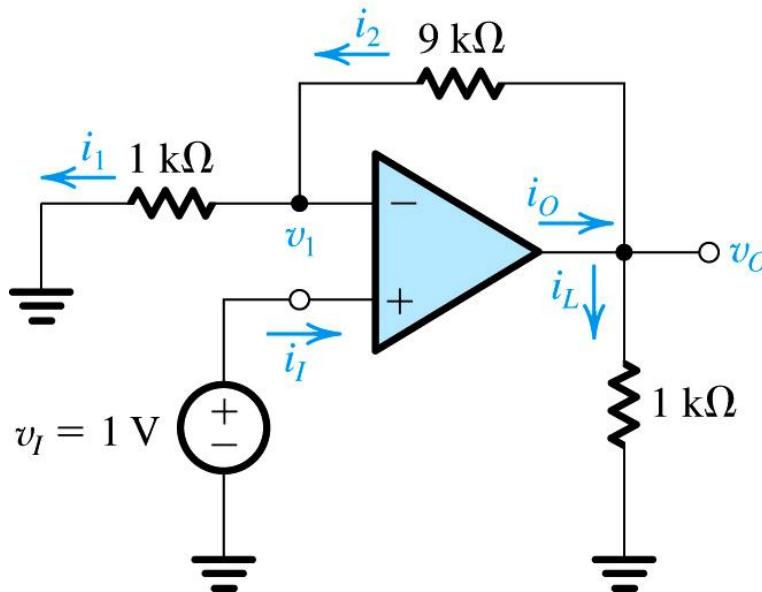


Figure E2.13

For the circuit in Fig. E2.13 find the values of  $i_I$ ,  $v_1$ ,  $i_1$ ,  $i_2$ ,  $v_O$ ,  $i_L$ , and  $i_O$ . Also find the voltage gain  $v_o/v_I$ , the current gain  $i_L/i_I$ , and the power gain  $P_L/P_I$ .

$$\begin{aligned}i_I &= 0\text{mA} & v_1 &= 1\text{V} \\i_1 &= 1\text{mA} & i_2 &= 1\text{mA} \\v_O &= 1\text{V} + (1\text{mA} \times 9\text{k}\Omega) = 10\text{V} \\i_L &= \frac{v_o}{1\text{k}\Omega} = 10\text{mA} \\i_O &= i_2 + i_L = 11\text{mA}\end{aligned}$$

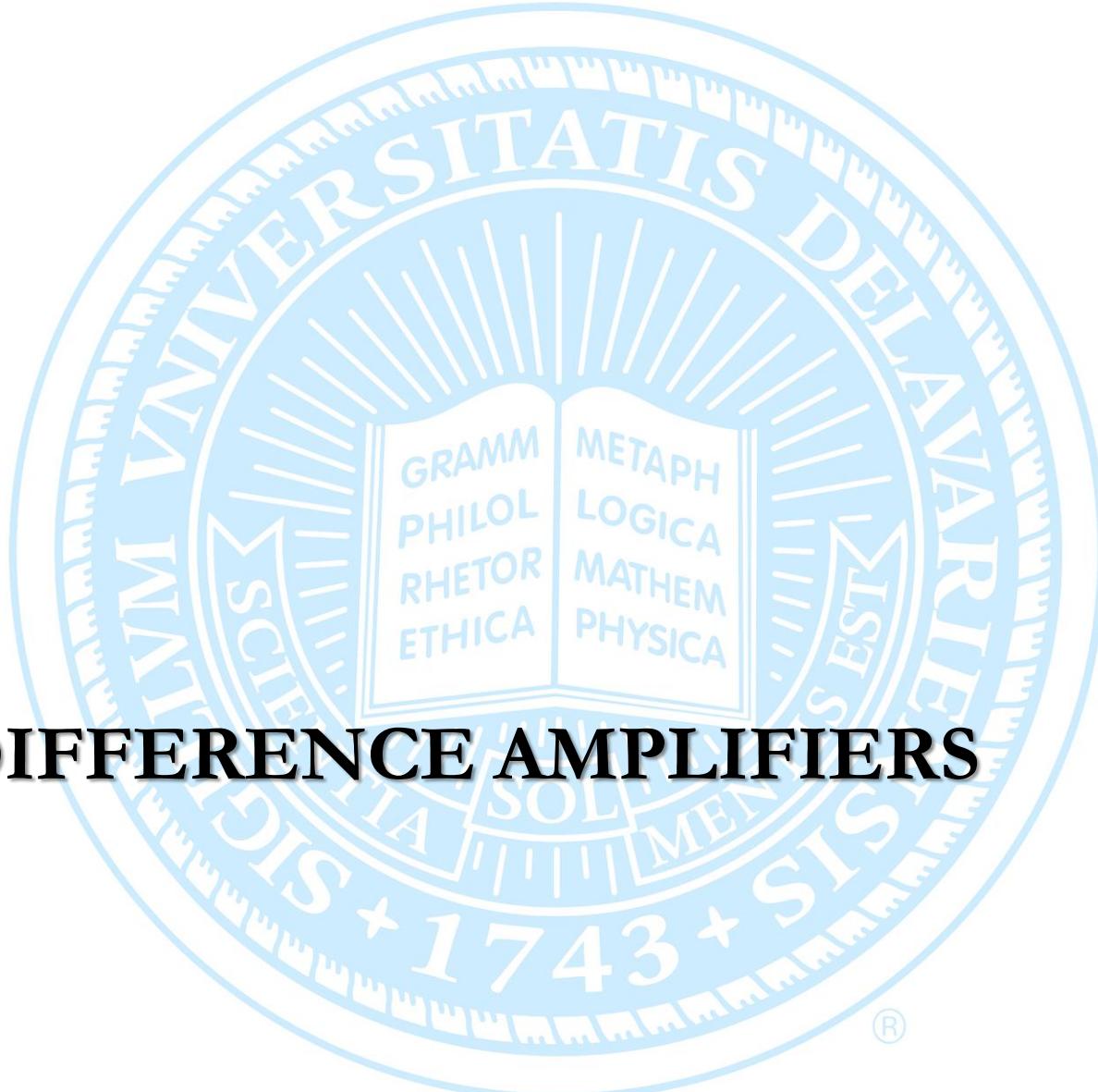
$$\begin{aligned}A_v &= \frac{v_o}{v_I} = 10\text{V/V} = 20\text{dB} \\A_i &= \frac{i_L}{i_I} = \frac{10\text{mA}}{0\text{mA}} = \infty\text{A/A} \\A_p &= \frac{i_L v_o}{i_I v_I} = \infty\text{W/W}\end{aligned}$$



# Homework #3

- Read Chapter 2
- Chapter 2 Problems:
  - 2.2\*
  - 2.8\*
  - 2.10
  - 2.44\*
  - 2.49

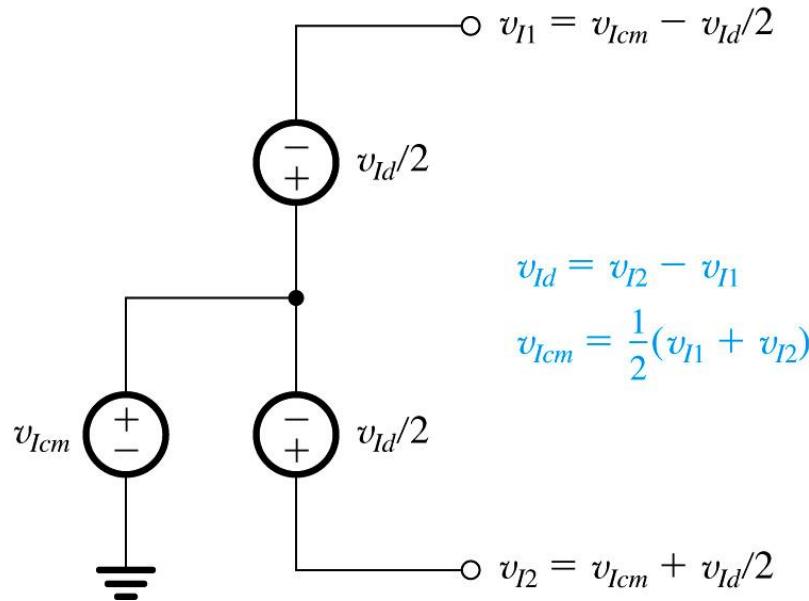
\* Answers in Appendix L



## 2.4 DIFFERENCE AMPLIFIERS



# Common Mode Rejection Ratio, CMRR



**Figure 2.15** Representing the input signals to a differential amplifier in terms of their differential and common-mode components.

$$v_O = A_d v_{id} + A_{cm} v_{icm}$$

$$v_{id} = v_{I2} - v_{I1}$$

$$v_{icm} = \frac{1}{2}(v_{I2} + v_{I1})$$

The efficacy of a differential amplifier is measured by the degree of its rejection of common-mode signals in preference to differential signals. This is usually quantified by a measure known as the common-mode rejection ratio (CMRR), defined as

$$\text{CMRR} = 20 \log \left( \frac{|A_d|}{|A_{cm}|} \right)$$



# Single Op-Amp Difference Amplifier

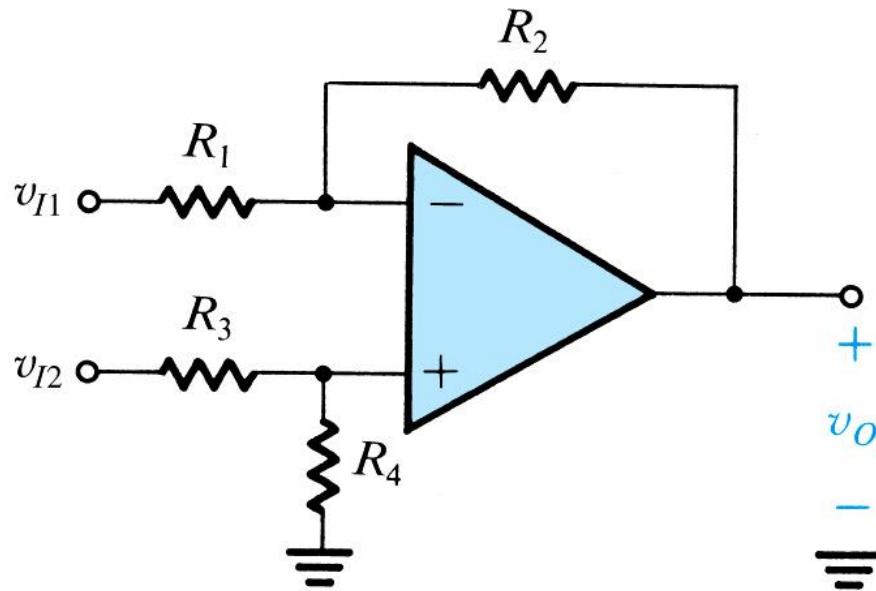


Figure 2.16 A difference amplifier.

$$\frac{R_4}{R_4 + R_3} \left( 1 + \frac{R_2}{R_1} \right) = \frac{R_2}{R_1}$$

To balance the noninverting and inverting gains we want

$$\frac{R_4}{R_4 + R_3} = \frac{R_2}{R_2 + R_1}$$

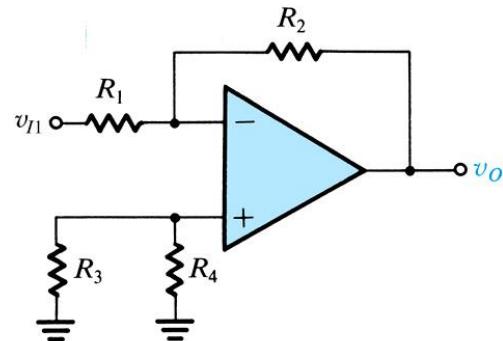
Which is true if

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$

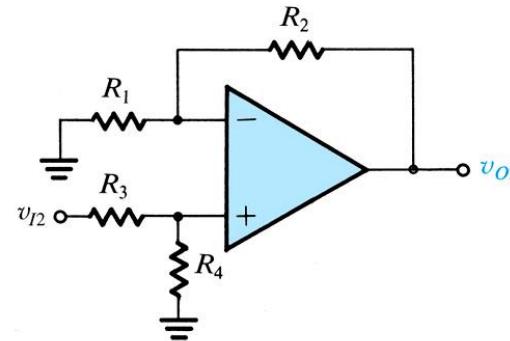


# Testing the Performance of the Circuit

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$



(a)



(b)

Figure 2.17 Application of superposition to the analysis of the circuit of Fig. 2.16.

1) First set  $v_{I2}$  to 0V.

2) Then set  $v_{I1}$  to 0V.

$$v_{O1} = -\frac{R_2}{R_1} v_{I1}$$

$$v_{O2} = \left( \frac{R_4}{R_3 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) v_{I2} = \frac{R_2}{R_1} v_{I2}$$

3) Then sum the two outputs

$$v_O = v_{O1} + v_{O2} = -\frac{R_2}{R_1} v_{I1} + \frac{R_2}{R_1} v_{I2} = \frac{R_2}{R_1} (v_{I2} - v_{I1}) = \frac{R_2}{R_1} v_{Id}$$

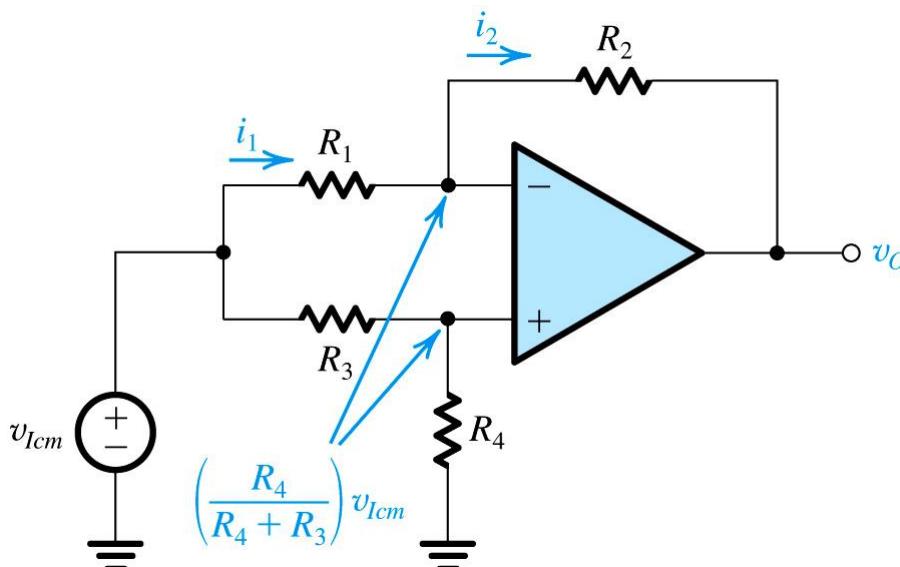
$$\Rightarrow A_d \equiv \frac{v_O}{v_{Id}} = \frac{R_2}{R_1} \text{ V/V}$$



# Common-Mode Gain, $A_{cm}$

Derived on page 80

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$



**Figure 2.18** Analysis of the difference amplifier to determine its common-mode gain  $A_{cm} \equiv v_O/v_{Icm}$ .

$$v_O = \frac{R_4}{R_4 + R_3} \left( 1 - \frac{R_2}{R_1} \frac{R_3}{R_4} \right) v_{Icm}$$

$$v_O = \frac{R_4}{R_4 + R_3} \left( 1 - \frac{R_2}{R_1} \frac{R_1}{R_2} \right) v_{Icm}$$

$$v_O = \frac{R_4}{R_4 + R_3} (1 - 1) v_{Icm} = 0$$

$$A_{cm} \equiv \frac{v_O}{v_{Icm}} = 0 \text{V/V}$$

$$\text{CMRR} = 20 \log \left( \frac{|A_d|}{0} \right) = \infty \text{dB}$$



# Determining the Input Resistance

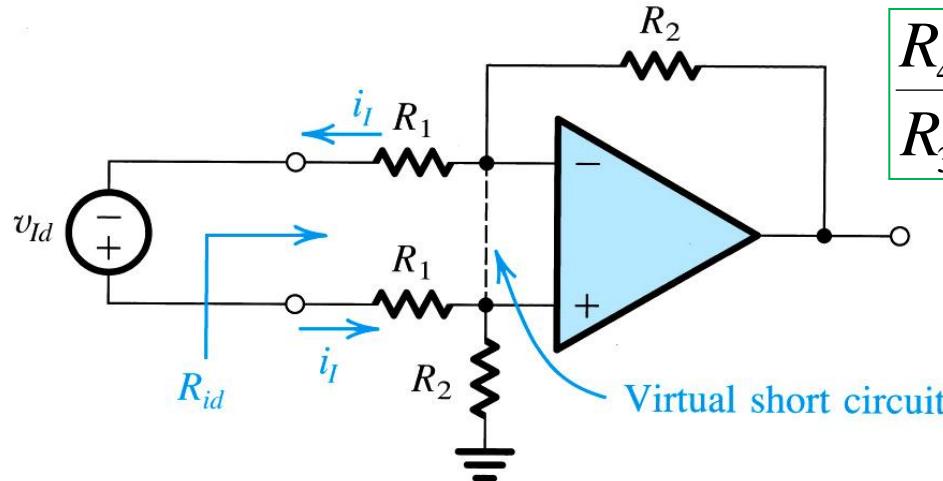


Figure 2.19 Finding the input resistance of the difference amplifier for the case  $R_3 = R_1$  and  $R_4 = R_2$ .

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \Rightarrow \text{choose } R_3 = R_1 \text{ and } R_4 = R_2$$

Since the two input terminals of the op amp track each other in potential, we may write a loop equation as:

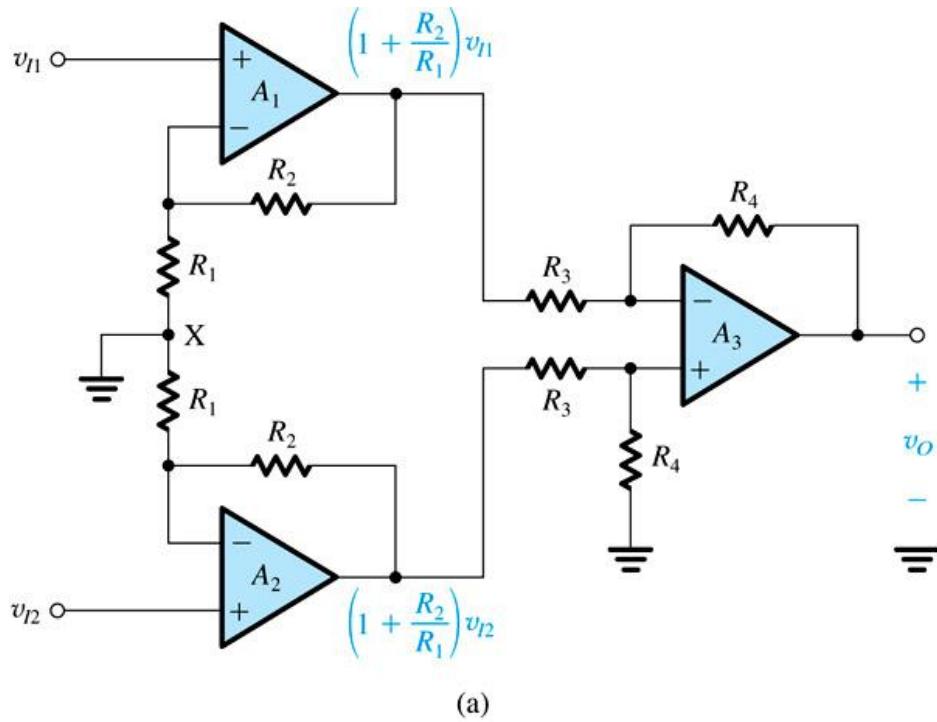
$$v_{Id} = R_1 i_I + 0 + R_1 i_I = 2R_1 i_I$$

the differential input resistance is:  $R_{id} \equiv \frac{v_{Id}}{i_I} = 2R_1$

Note that if the amplifier is required to have a large differential gain ( $R_2/R_1$ ), then  $R_1$  of necessity will be relatively small and the input resistance will be correspondingly low, a drawback of this circuit. Another drawback of the circuit is that it is not easy to vary the differential gain of the amplifier.



# The Instrumentation Amplifier



$$v_O = \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right) v_{Id}$$

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right)$$

$$A_{cm} \equiv \frac{v_O}{v_{Icm}} = 0$$

**Figure 2.20** A popular circuit for an instrumentation amplifier.

(a) Initial approach to the circuit.



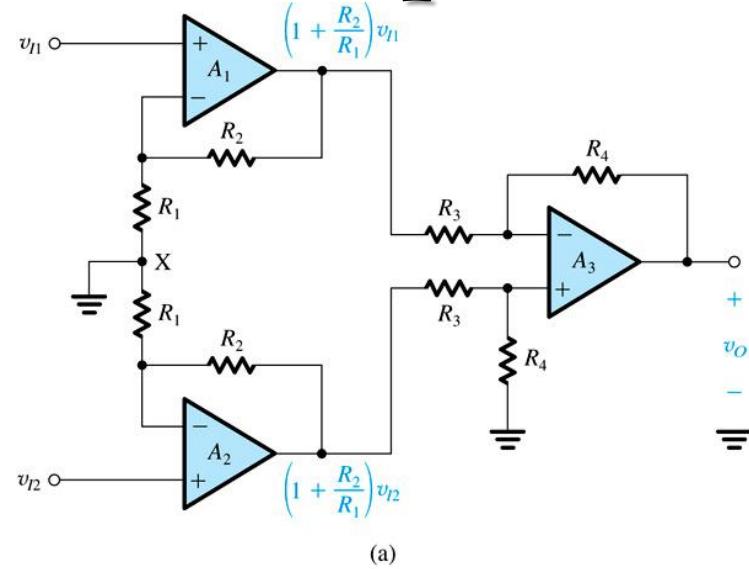
# The Instrumentation Amplifier

## Advantages

- Very high input resistance
- High differential gain
- Low common mode gain

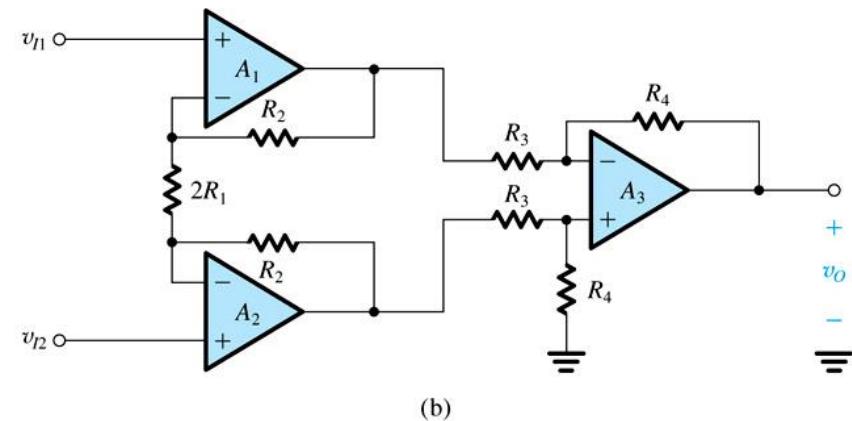
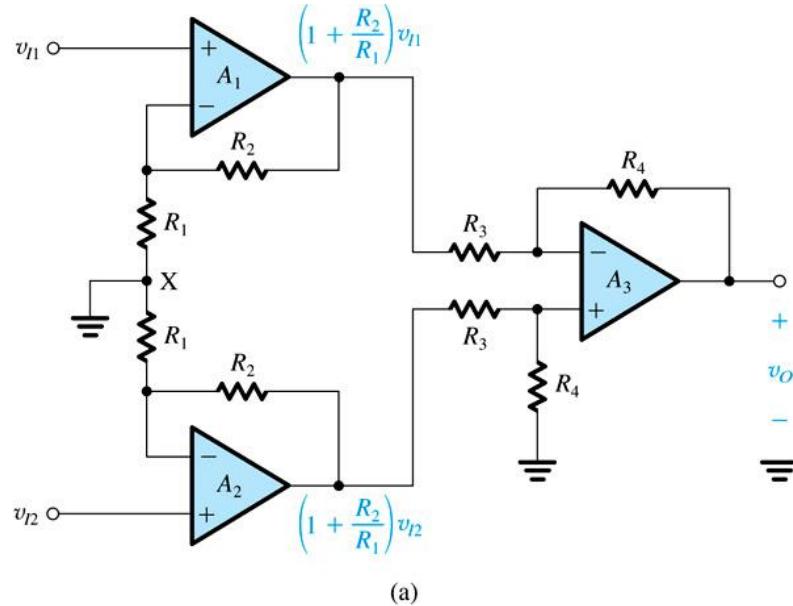
## Disadvantages

- Input common-mode signal is amplified by the first stage
- The two amplifiers in the first stage have to match perfectly
- Two resistors have to be varied simultaneously to vary the differential gain (and perfectly matched)





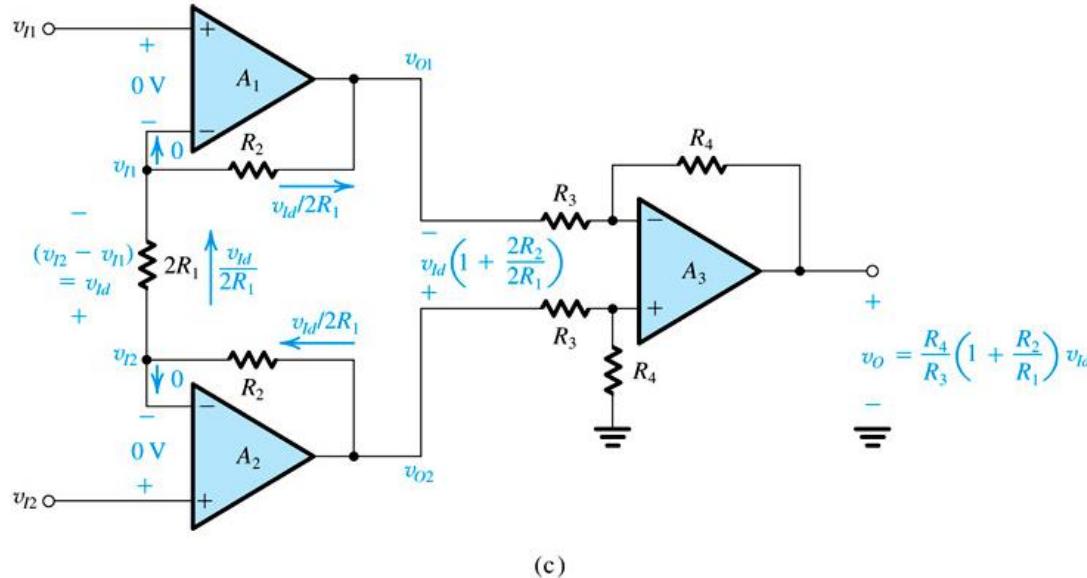
# The Instrumentation Amplifier take2



**Figure 2.20** A popular circuit for an instrumentation amplifier. **(a)** Initial approach to the circuit **(b)** The circuit in **(a)** with the connection between node X and ground removed and the two resistors R<sub>1</sub> and R<sub>2</sub> lumped together. This simple wiring change dramatically improves performance.



# The Instrumentation Amplifier



**Figure 2.20** A popular circuit for an instrumentation amplifier.

(c) Analysis of the circuit in (b) assuming ideal op amps.

Proper differential operation does not depend on matching resistors  $R_2$ . If one of the resistors is  $R_2$  and one is  $R'_2$   $A_d$  becomes:

$$v_{O2} - v_{O1} = \left(1 + \frac{2R_2}{2R_1}\right) v_{Id}$$

$$v_O = \frac{R_4}{R_3} (v_{O2} - v_{O1})$$

$$= \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right) v_{Id}$$

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right)$$

$$A_d \equiv \frac{v_O}{v_{Id}} = \frac{R_4}{R_3} \left(1 + \frac{R_2 + R'_2}{2R_1}\right)$$



## 2.5 INTEGRATORS AND DIFFERENTIATORS



# The Inverting Configuration with General Impedances

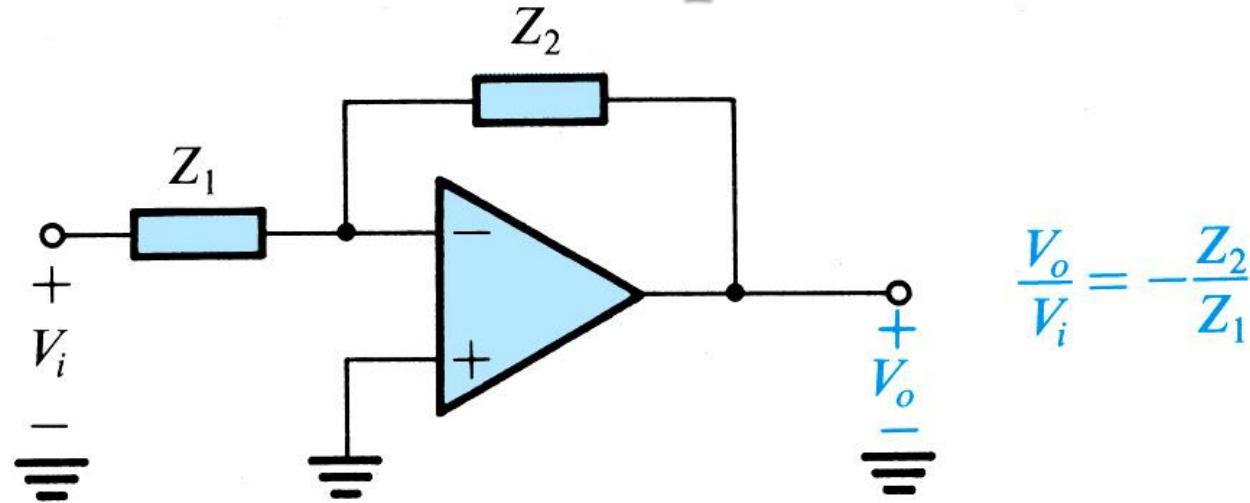


Figure 2.22 The inverting configuration with general impedances in the feedback and the feed-in paths.

Gain can vary with frequency,  $s (j\omega)$ :

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)}$$

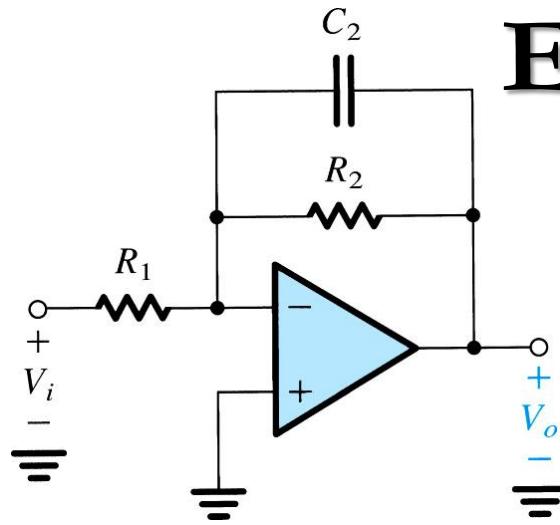


Figure 2.23 Circuit for Example 2.4.

## Example 2.4 (p. 88)

For the circuit in Fig. 2.23, derive an expression for the transfer function  $V_o(s)/V_i(s)$ . Show that the transfer function is that of a low-pass STC circuit. By expressing the transfer function in the standard form shown in Table 1.2 on page 36, find the dc gain and the 3-dB frequency. Design the circuit to obtain a dc gain of 40 dB, a 3-dB frequency of 1 kHz, and an input resistance of 1 k $\Omega$ . At what frequency does the magnitude of transmission become unity? What is the phase angle at this frequency?

$$Z_1 = R_1, Z_2 = R_2 \parallel (1/sC_2) = \frac{R_2}{1 + sC_2 R_2}$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2}{Z_1} = \frac{-R_2/R_1}{1 + sC_2 R_2}$$



# Table 1.2 Frequency Response of STC Networks

	Low-Pass (LP)	High-Pass (HP)
Transfer Function $T(s)$	$\frac{K}{1 + (s/\omega_0)}$	$\frac{Ks}{s + \omega_0}$
Transfer Function for physical frequencies $T(j\omega)$	$\frac{K}{1 + j(\omega/\omega_0)}$	$\frac{K}{1 - j(\omega_0/\omega)}$
Magnitude Response $ T(j\omega) $	$\frac{ K }{\sqrt{1 + (\omega/\omega_0)^2}}$	$\frac{ K }{\sqrt{1 + (\omega_0/\omega)^2}}$
Phase Response $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega = 0$	$K$	$0$
Transmission at $\omega = \infty$	$0$	$K$
3-dB Frequency	$\omega_0 = 1/\tau$ , $\tau$ = time constant $\tau = CR$ or $L/R$	

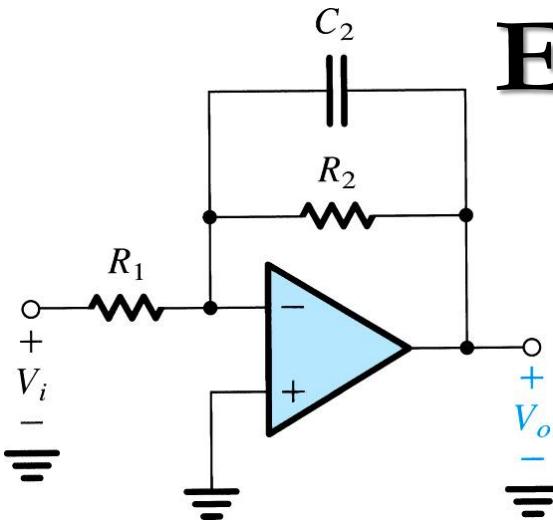


Figure 2.23 Circuit for Example 2.4.

## Example 2.4 (p. 88)

For the circuit in Fig. 2.23, derive an expression for the transfer function  $V_o(s)/V_i(s)$ . Show that the transfer function is that of a low-pass STC circuit. By expressing the transfer function in the standard form shown in Table 1.2 on page 36, find the dc gain and the 3-dB frequency. Design the circuit to obtain a dc gain of 40 dB, a 3-dB frequency of 1 kHz, and an input resistance of 1 k $\Omega$ . At what frequency does the magnitude of transmission become unity? What is the phase angle at this frequency?

$$Z_1 = R_1, Z_2 = R_2 \parallel (1/sC_2) = \frac{R_2}{1 + sC_2 R_2}$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2}{Z_1} = \frac{-R_2/R_1}{1 + sC_2 R_2}$$

STC –  
low-pass filter

$$T(j\omega) = \frac{K}{1 + j(\omega/\omega_0)}$$

$$K = -\frac{R_2}{R_1} \quad \omega_0 = \frac{1}{C_2 R_2}$$

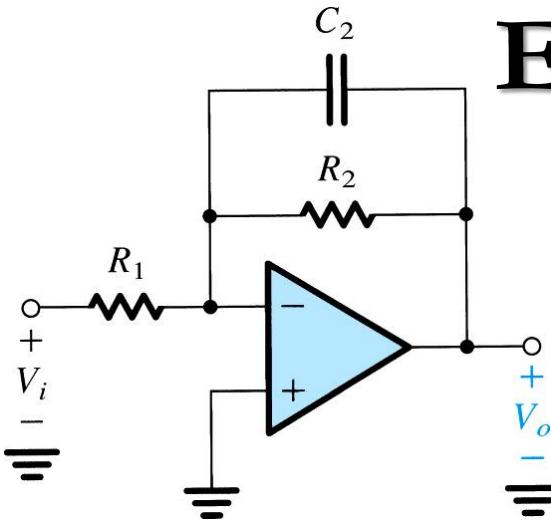


Figure 2.23 Circuit for Example 2.4.

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2}{Z_1} = \frac{-R_2/R_1}{1+sC_2R_2}$$

$$K = -\frac{R_2}{R_1} = 40 \text{dB} = 100 \text{V/V}$$

$$\Rightarrow \frac{R_2}{R_1} = 100 \quad R_1 = 1 \text{k}\Omega \quad \Rightarrow R_2 = 100 \text{k}\Omega$$

## Example 2.4 (p. 88)

For the circuit in Fig. 2.23, derive an expression for the transfer function  $V_o(s)/V_i(s)$ . Show that the transfer function is that of a low-pass STC circuit. By expressing the transfer function in the standard form shown in Table 1.2 on page 36, find the dc gain and the 3-dB frequency. Design the circuit to obtain a dc gain of 40 dB, a 3-dB frequency of 1 kHz, and an input resistance of 1 k $\Omega$ . At what frequency does the magnitude of transmission become unity? What is the phase angle at this frequency?

$$\omega_0 = \frac{1}{C_2 R_2} = 2\pi f_0 = 2\pi \times 1 \text{kHz}$$

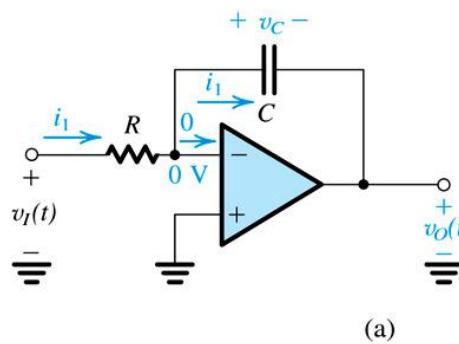
$$\Rightarrow C_2 = 1.59 \text{nF}$$

Magnitude response ( $|T(j\omega)|$ ) drops at 20 dB/decade (6 dB/octave) so the response will be unity (0 dB) at  $100f_0 = 100 \text{ kHz}$ .



# The Miller or Inverting Integrator

$$Z_1(s) = R \text{ and } Z_2(s) = 1/sC$$



$$v_o(t) = -\frac{1}{CR} \int_0^t v_i(t) dt - V_C$$

$$\frac{V_o}{V_i} = -\frac{1}{sCR}$$

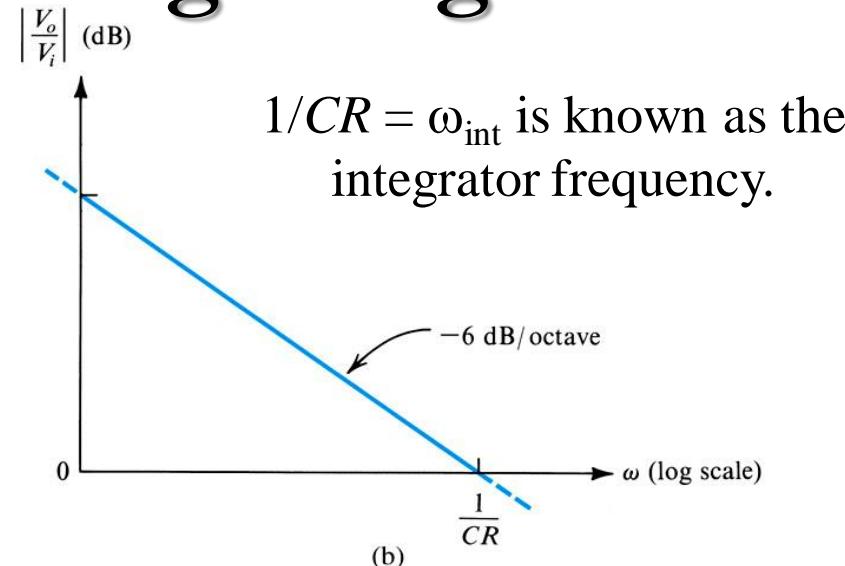


Figure 2.24 (a) The Miller or inverting integrator. (b) Frequency response of the integrator.

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{sCR}$$

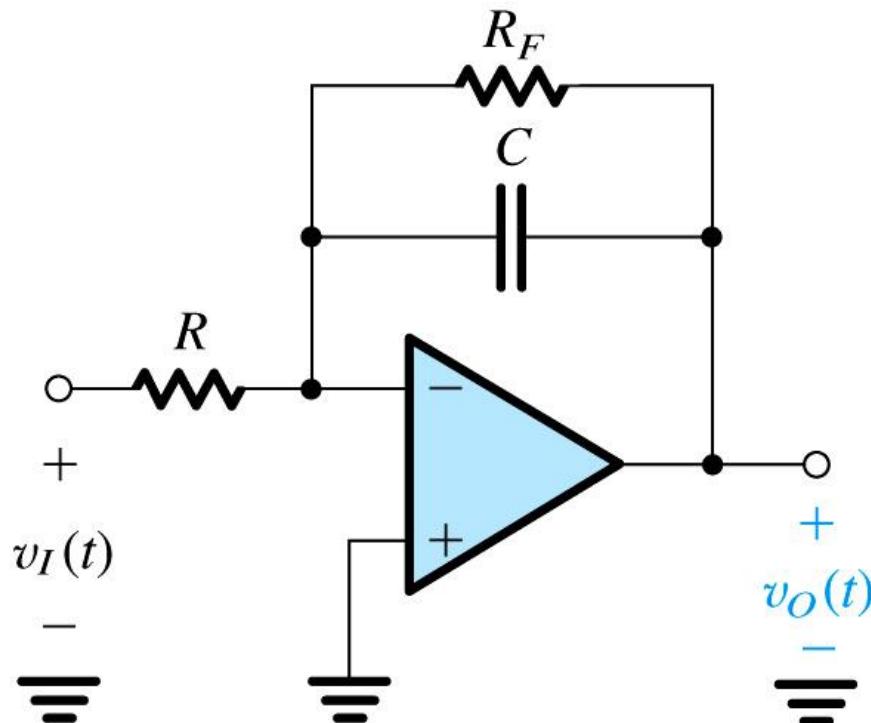
$CR$  is known as the integrator time constant.

$$T(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR}$$

$$|T(j\omega)| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{1}{\omega CR}$$



# The Miller or Inverting Integrator

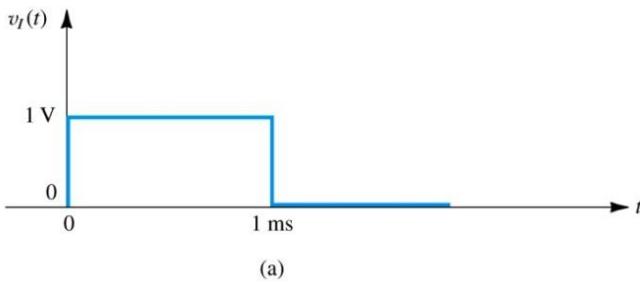


$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2}{Z_1} = -\frac{R_F/R}{1+sCR_F}$$

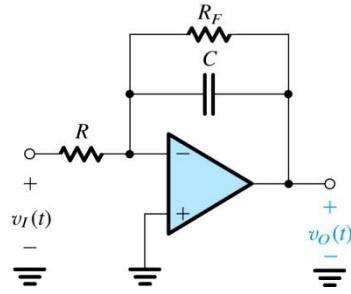
**Figure 2.25** The Miller integrator with a large resistance  $R_F$  connected in parallel with  $C$  in order to provide negative feedback and hence finite gain at dc.



## Example 2.5 (p. 92)



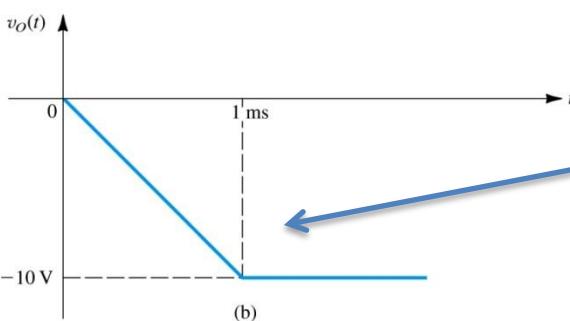
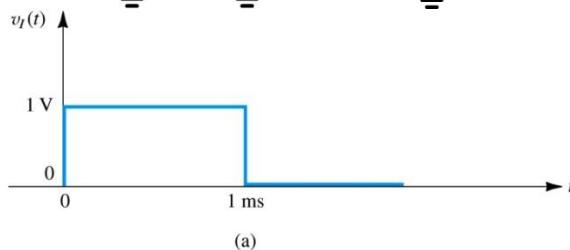
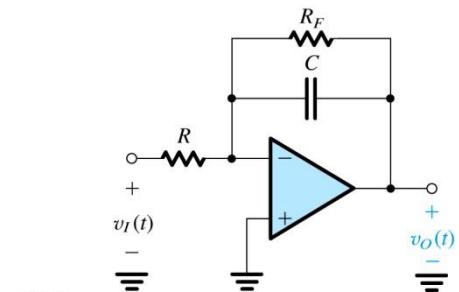
**Figure 2.26** Waveforms for Example 2.5: (a) Input pulse.



Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.26(a)]. Let  $R = 10 \text{ k}\Omega$  and  $C = 10 \text{ nF}$ . If the integrator capacitor is shunted by a  $1\text{-M}\Omega$  resistor, how will the response be modified? The op amp is specified to saturate at  $\pm 13 \text{ V}$ .

$$\begin{aligned}v_O(t) &= -\frac{1}{CR} \int_0^t v_I(t) dt - V_C \\&= -\frac{1}{CR} \int_0^t 1 dt, \quad 0 \leq t \leq 1\text{ms}\end{aligned}$$

$$v_O(t) = -10t, \quad 0 \leq t \leq 1\text{ms} \quad t \text{ is in ms}$$

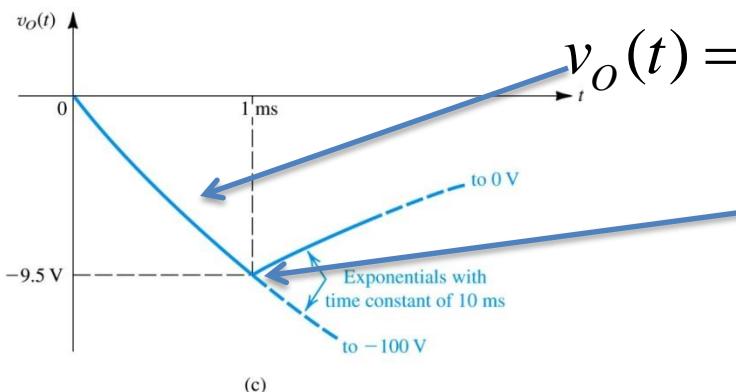
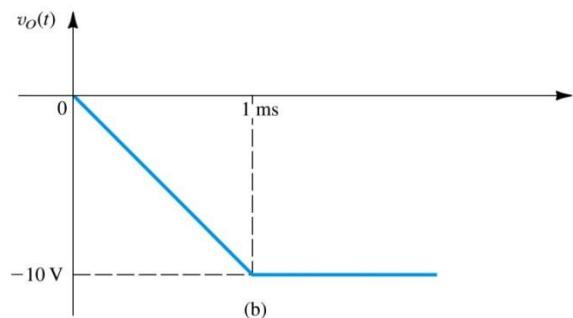
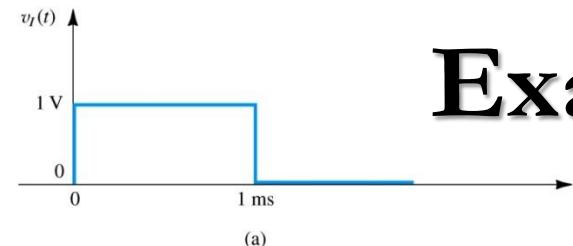


## Example 2.5 (p. 92)

Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.26(a)]. Let  $R = 10 \text{ k}\Omega$  and  $C = 10 \text{ nF}$ . If the integrator capacitor is shunted by a  $1\text{-M}\Omega$  resistor, how will the response be modified? The op amp is specified to saturate at  $\pm 13 \text{ V}$ .

$$v_O(t) = -10t, \quad 0 \leq t \leq 1\text{ms} \quad t \text{ is in ms}$$

**Figure 2.26** Waveforms for Example 2.5: (a) Input pulse. (b) Output linear ramp of ideal integrator with time constant of 0.1 ms.



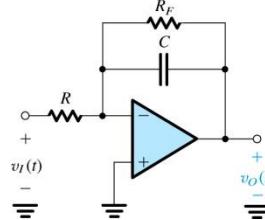
## Example 2.5 (p. 92-94)

Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.26(a)]. Let  $R = 10 \text{ k}\Omega$  and  $C = 10 \text{ nF}$ . If the integrator capacitor is shunted by a  $1\text{-M}\Omega$  resistor, how will the response be modified? The op amp is specified to saturate at  $\pm 13 \text{ V}$ .

$$10\text{nF} \times 1\text{M}\Omega = 10\text{ms}$$

$$v_O(t) = -100(1 - e^{-t/10\text{ms}})t, \quad 0 \leq t \leq 1\text{ms}$$

$$v_O(1\text{ms}) = -100(1 - e^{-1/10})t = -9.52\text{V}$$



**Figure 2.26** Waveforms for Example 2.5: (a) Input pulse. (b) Output linear ramp of ideal integrator with time constant of 0.1 ms. (c) Output exponential ramp with resistor  $R_F$  connected across integrator capacitor.



# 2/16/2012 EDN Design Ideas

## Use an integrator instead of coupling capacitors

Vladimir Rentyuk, Modul-98 Ltd, Zaporozhye, Ukraine

An ultrasonic sensor circuit requiring self-adjustment to the level of an ac-input signal also must accommodate the signal's unknown and variable dc-bias voltage. The circuit cannot use an ac coupling capacitor, and the resulting output must be level-shifted to a known dc offset. The design uses a dc-offset compensator (Figure 1).

For proper circuit operation, use a single-supply, high-input-impedance, rail-to-rail-output dual operational amplifier similar to the AD822 (Reference 1). You can adjust the reference voltage,  $V_{REF}$ , using potentiometer  $R_1$  to set the output offset level, which is equal to the reference voltage and usually half the supply voltage,  $V_{CC}$ , for full dynamic range.  $IC_{1B}$  amplifies

and inverts the high-frequency ac-input signal with a gain of  $R_4/R_3$ .

Subtracting integrator  $IC_{1A}$  provides compensation of any unsuitable offset voltage within the negative-feedback loop. The ac-signal component attenuates based on  $R_3C_1$  values, leaving only the averaged dc-offset component to hold the  $IC_{1B}$  output's average voltage equal to the reference voltage. Figure 2 shows the compensation action for a bias step of 4V, which completes in approximately 100 msec.

also works as a differentiator to step changes in the dc input with constant-output offset voltage. EDN

### REFERENCE

1 "AD822 Single-Supply, Rail-to-Rail Low Power FET-Input Op Amp," Analog Devices Inc, 2003, <http://bit.ly/yokb04>.

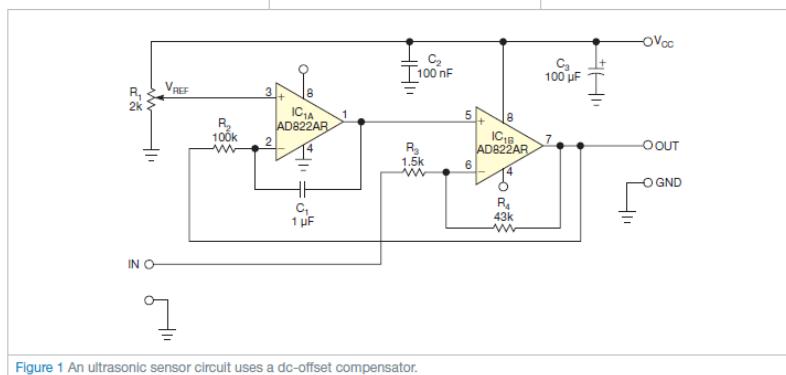
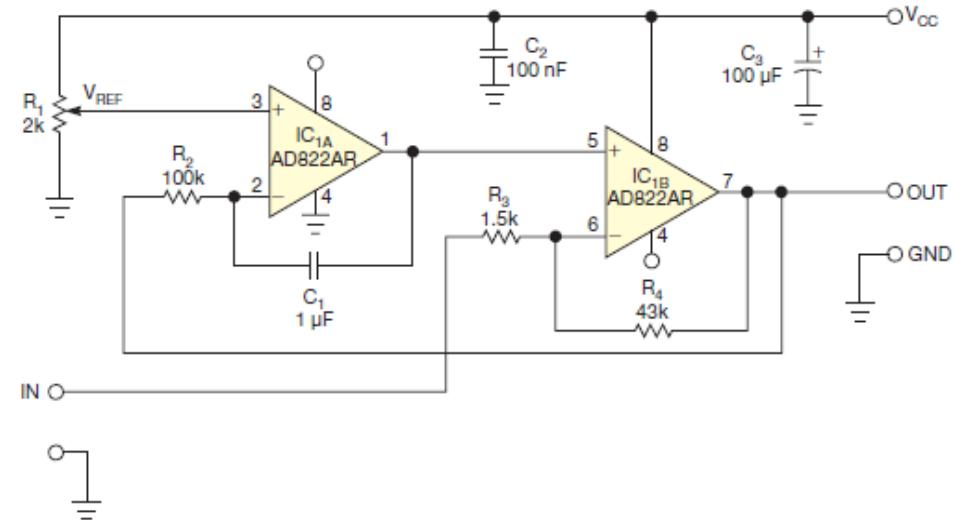


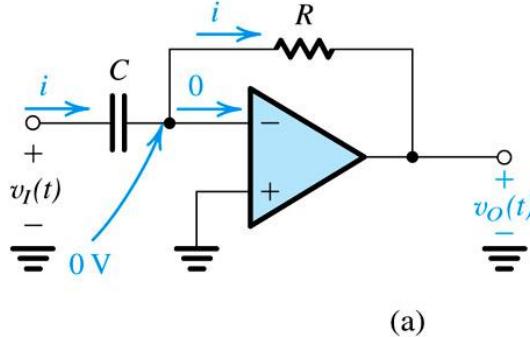
Figure 1 An ultrasonic sensor circuit uses a dc-offset compensator.





# The Op-Amp Differentiator

$$Z_1(s) = 1/sC \text{ and } Z_2(s) = R$$



$$\begin{aligned}i(t) &= C \frac{dv_I(t)}{dt} \\v_O(t) &= -CR \frac{dv_I(t)}{dt} \\ \frac{V_o}{V_i} &= -sCR\end{aligned}$$

Figure 2.27 (a) A differentiator.

$$\frac{V_o(s)}{V_i(s)} = -sCR$$

$CR$  is known as the differentiator time constant.

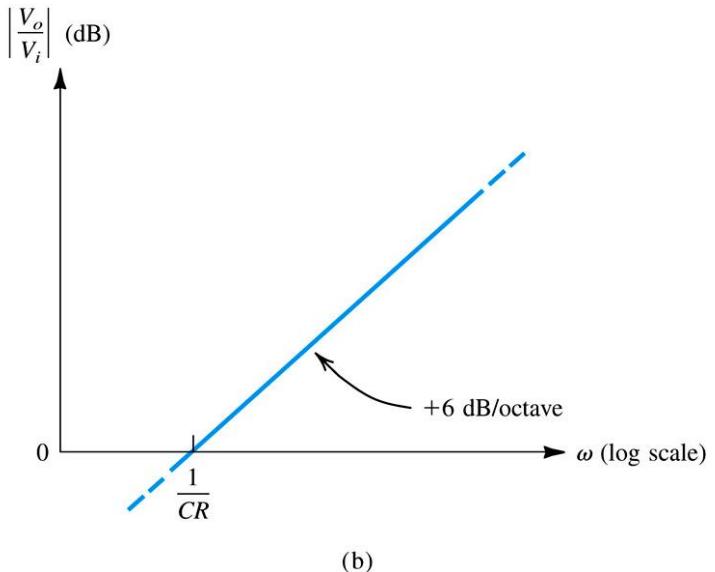


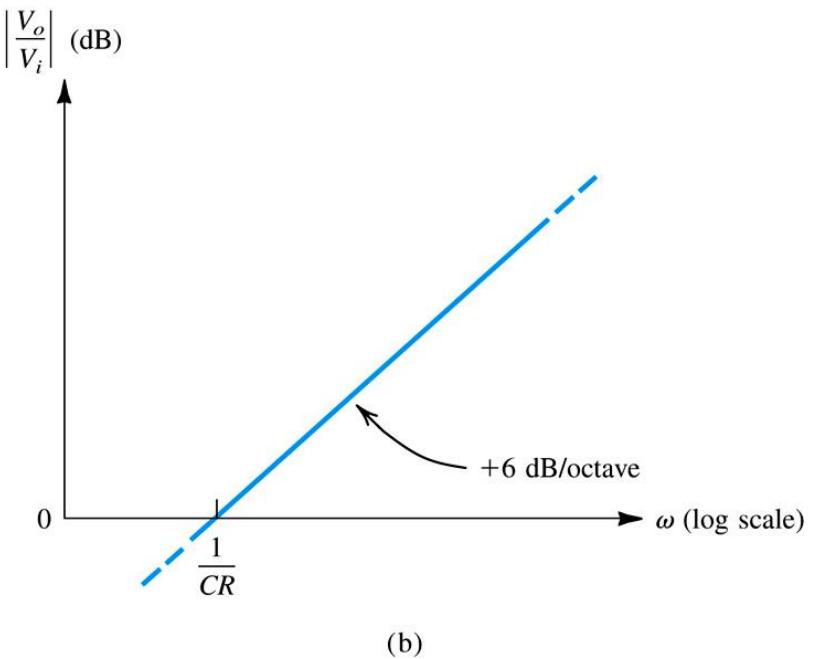
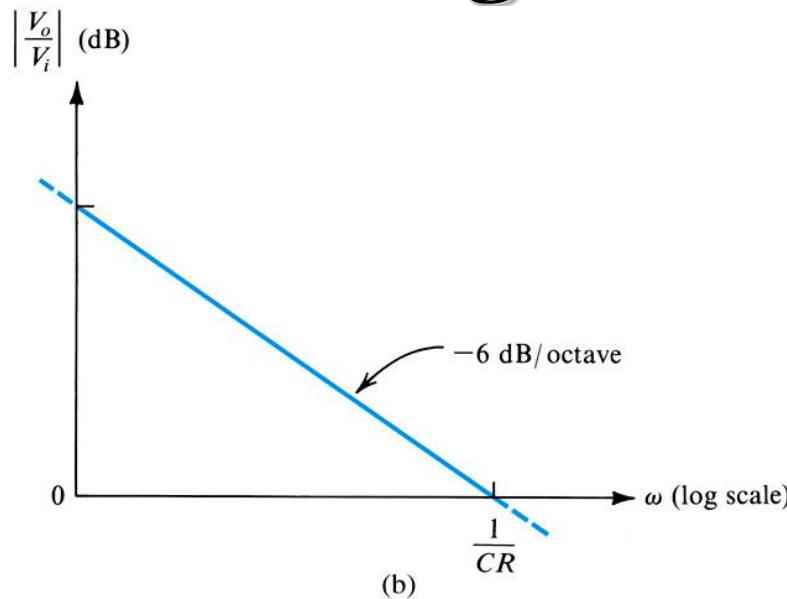
Figure 2.27 (b) Frequency response of a differentiator with a time-constant  $CR$ .

$$T(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega CR$$

$$|T(j\omega)| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \omega CR$$

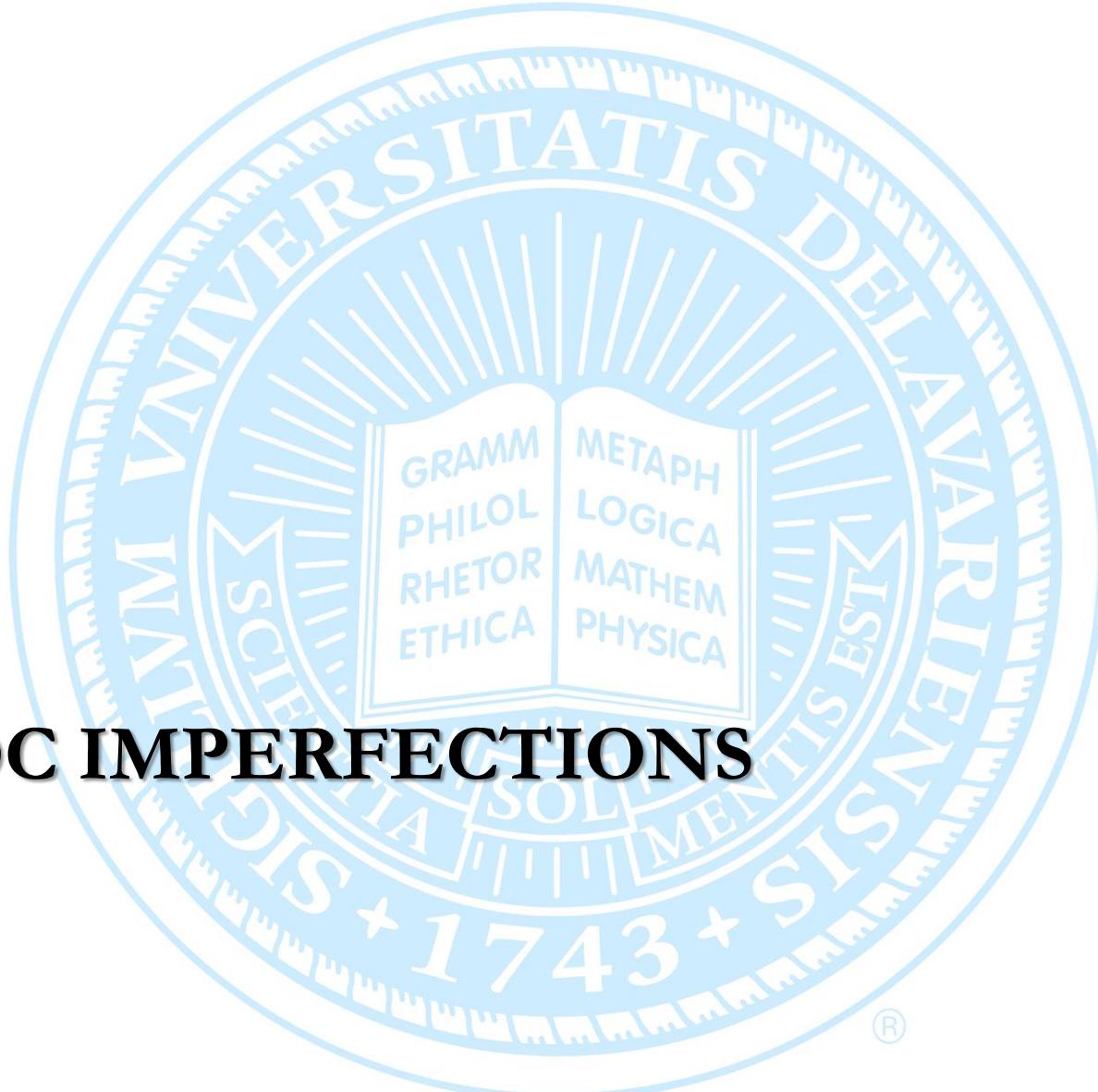


# Integrator vs Differentiator



$$|T(j\omega)| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \frac{1}{\omega CR}$$

$$|T(j\omega)| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \omega CR$$



## 2.6 DC IMPERFECTIONS



# Characteristics of the Ideal Op Amp

1)input impedance	Infinite
2)output impedance	Zero
3)common-mode gain	Zero
common-mode rejection	Infinite
4)open-loop gain, $A$	Infinite
5)bandwidth	Infinite



# Nonideal Op-Amps

- Covered in ELEG 309
  - Offset Voltage
  - Input Bias and Offset Currents
- Covered in ELEG 312
  - Finite common-mode gain (i.e. noninfinite CMRR)
  - Noninfinite input resistance
  - Nonzero output resistance



# Input Offset Voltage

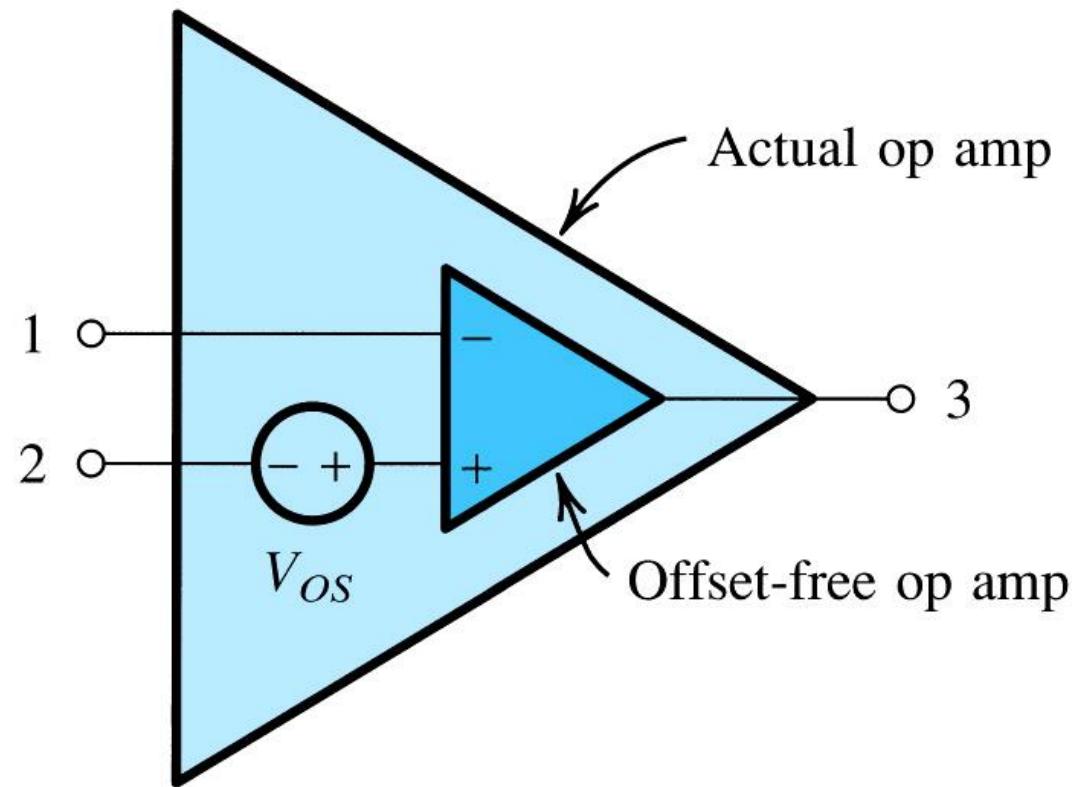
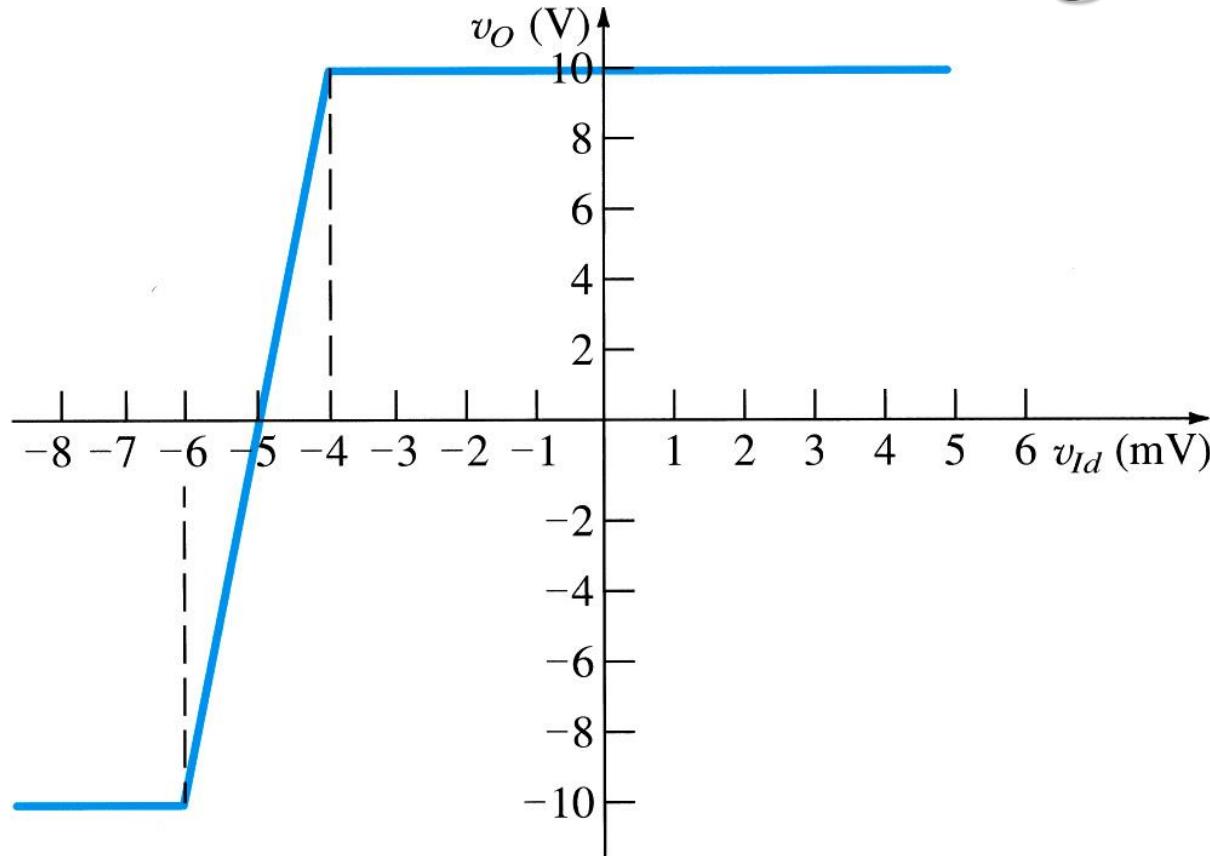


Figure 2.28 Circuit model for an op amp with input offset voltage  $V_{OS}$ .



# Transfer Characteristic of an Op Amp with 5 mV offset voltage



**Figure E2.21** Transfer characteristic of an op amp with  $V_{OS} = 5$  mV.



# LM324 Quad Op-Amp

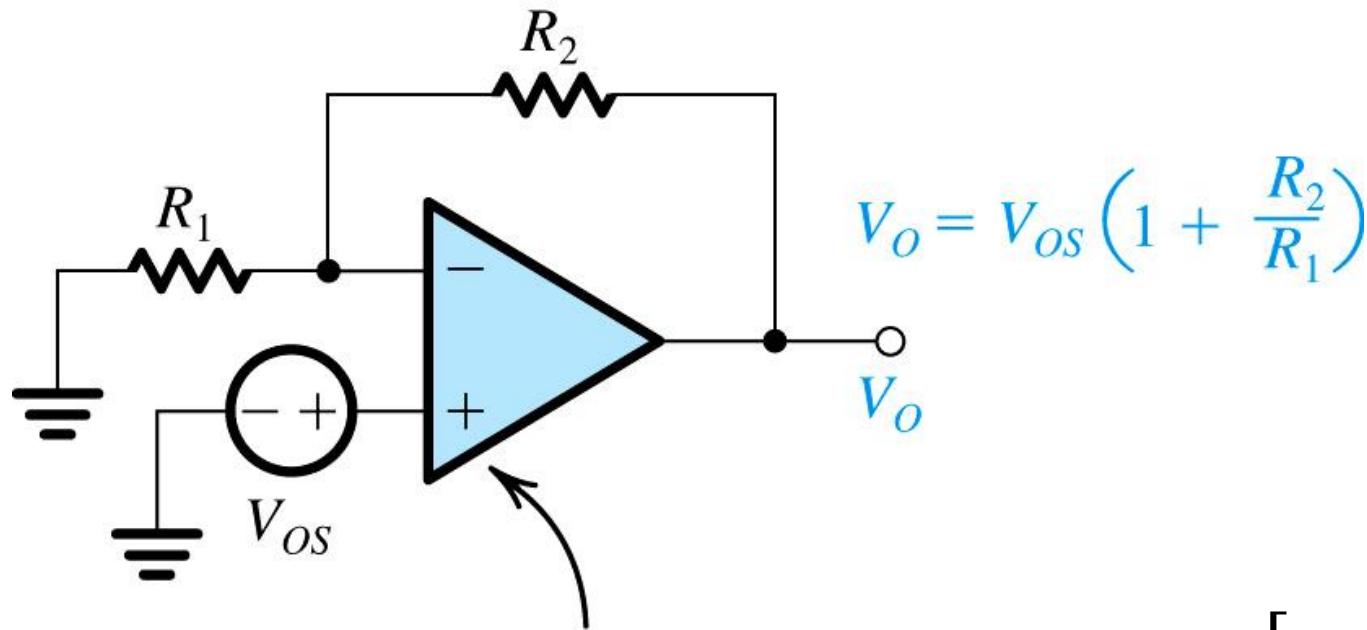
## Electrical Characteristics

$V^+ = +5.0V$ , (Note 7), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) $T_A = 25^\circ C$	1	2		1	3		2	3		mV
Input Bias Current (Note 9)	$I_{IN(+)} \text{ or } I_{IN(-)}$ , $V_{CM} = 0V$ , $T_A = 25^\circ C$	20	50		40	80		45	100		nA
Input Offset Current	$I_{IN(+)} \text{ or } I_{IN(-)}$ , $V_{CM} = 0V$ , $T_A = 25^\circ C$	2	10		2	15		5	30		nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$ , (LM2902, $V^+ = 26V$ ), $T_A = 25^\circ C$	0	$V^+ - 1.5$		0	$V^+ - 1.5$		0	$V^+ - 1.5$		V
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps $V^+ = 30V$ (LM2902 $V^+ = 26V$ ) $V^+ = 5V$	1.5	3		1.5	3		1.5	3		mA
Large Signal Voltage Gain	$V^+ = 15V$ , $R_L \geq 2k\Omega$ , ( $V_O = 1V$ to $11V$ ), $T_A = 25^\circ C$	50	100		50	100		25	100		V/mV
Common-Mode	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$ ,	70	85		70	85		65	85		dB



# Effect of Input Offset Voltage



Offset-free  
op amp

$$V_O = V_{OS} \left[ 1 + \frac{R_2}{R_1} \right]$$

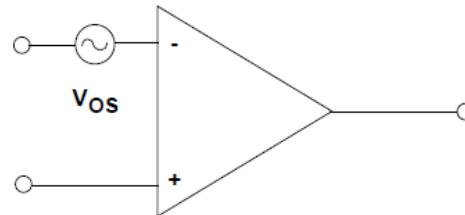
**Figure 2.29** Evaluating the output dc offset voltage due to  $V_{OS}$  in a closed-loop amplifier.



## Op Amp Input Offset Voltage

### DEFINITION OF INPUT OFFSET VOLTAGE

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the *input offset voltage*,  $V_{os}$ . Input offset voltage is modeled as a voltage source,  $V_{os}$ , in series with the inverting input terminal of the op amp as shown in Figure 1.

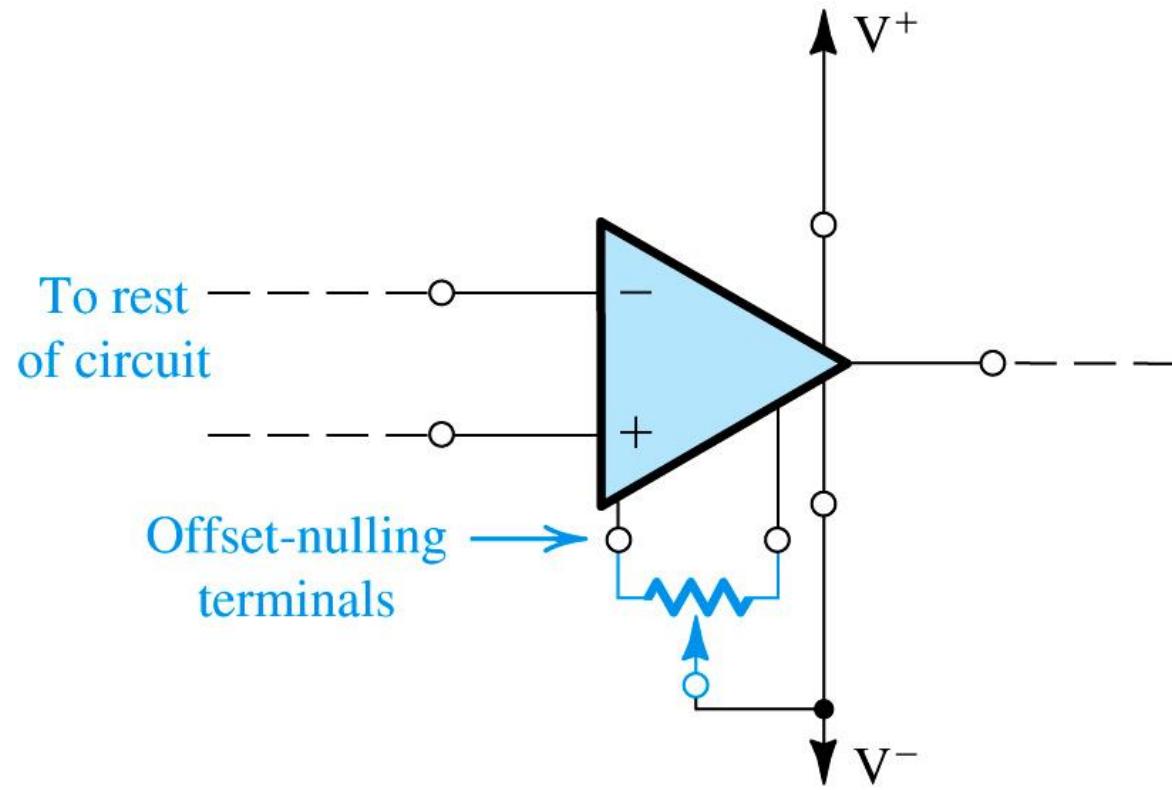


- ◆ **Offset Voltage:** The differential voltage which must be applied to the input of an op amp to produce zero output.
- ◆ **Ranges:**
  - Chopper Stabilized Op Amps: <1µV
  - General Purpose Precision Op Amps: 50-500µV
  - Best Bipolar Op Amps: 10-25µV
  - Best JFET Input Op Amps: 100-1,000µV
  - High Speed Op Amps: 100-2,000µV
  - Untrimmed CMOS Op Amps: 5,000-50,000µV
  - DigiTrim™ CMOS Op Amps: <100µV-1,000µV

Figure 1: Typical Op Amp Input Offset Voltage



# DC Offset Voltage Trim



**Figure 2.30** The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.



## µA741, µA741Y GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

SLOS094B – NOVEMBER 1970 – REVISED SEPTEMBER 2000

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Designed to Be Interchangeable With Fairchild µA741

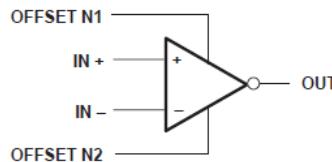
### description

The µA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

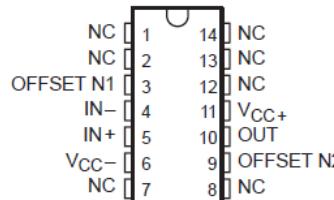
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The µA741C is characterized for operation from 0°C to 70°C. The µA741I is characterized for operation from -40°C to 85°C. The µA741M is characterized for operation over the full military temperature range of -55°C to 125°C.

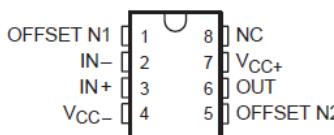
### symbol



µA741M...J PACKAGE  
(TOP VIEW)



µA741M...JG PACKAGE  
µA741C, µA741I...D, P, OR PW PACKAGE  
(TOP VIEW)



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### APPLICATION INFORMATION

Figure 2 shows a diagram for an input offset voltage null circuit.

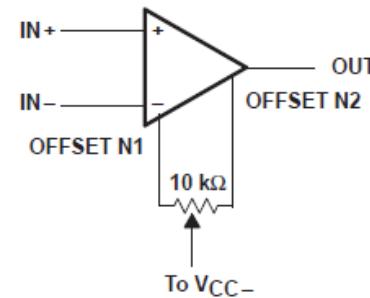
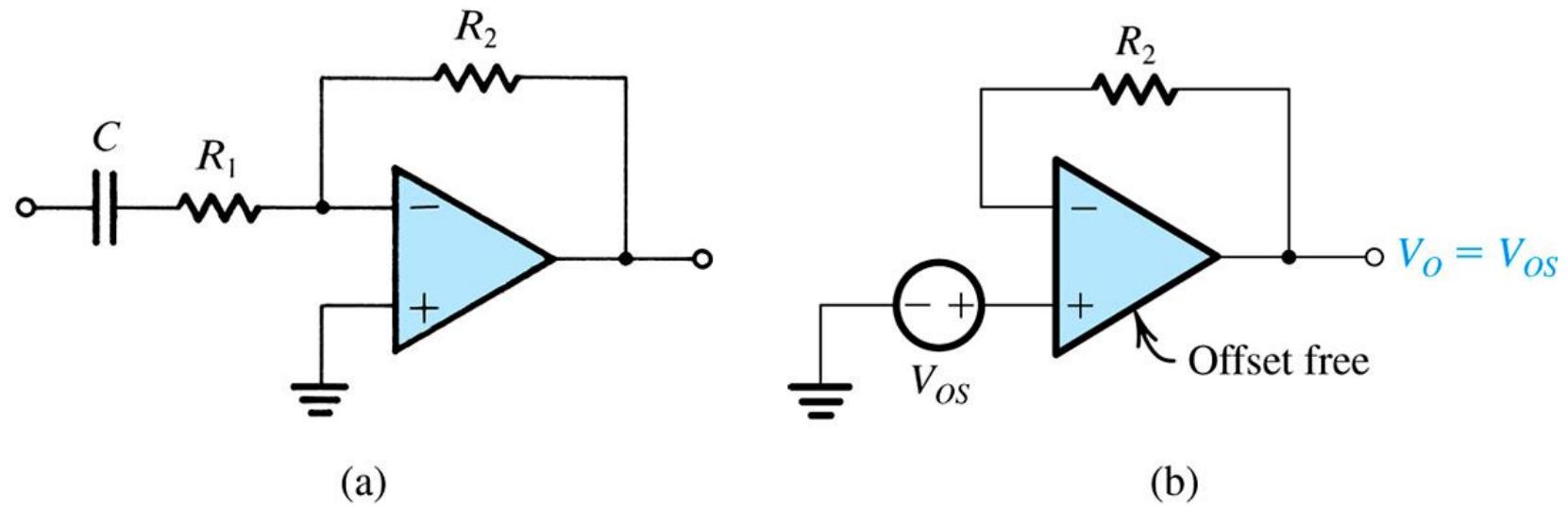


Figure 2. Input Offset Voltage Null Circuit



# Capacitively Coupling to the Amplifier



**Figure 2.31** (a) A capacitively coupled inverting amplifier. (b) The equivalent circuit for determining its dc output offset voltage  $V_O$ .



# Input Bias and Offset Currents

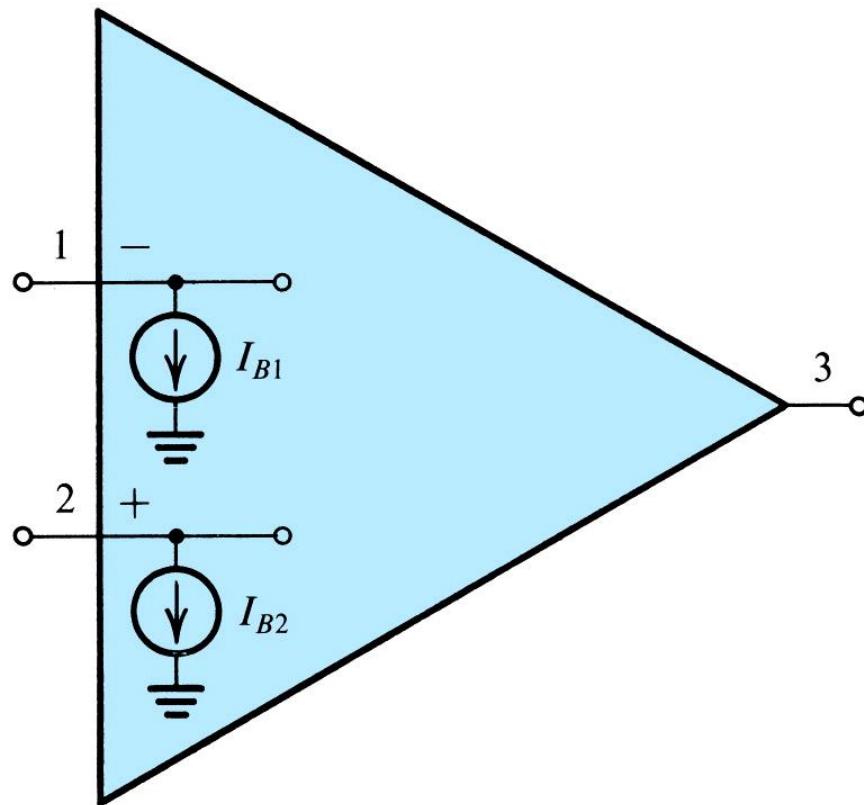


Figure 2.32 The op-amp input bias currents represented by two current sources  $I_{B1}$  and  $I_{B2}$ .

Input bias current

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

Input offset current

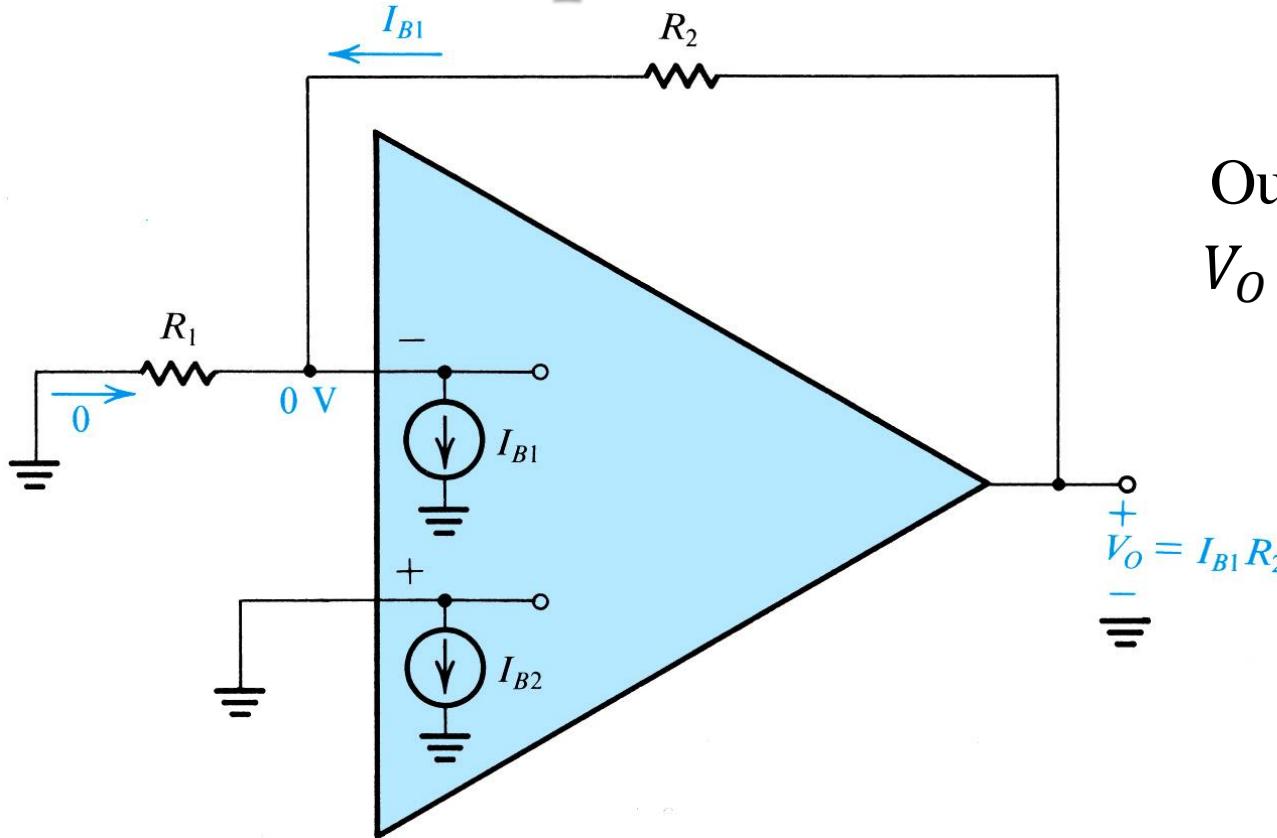
$$I_{OS} = |I_{B1} - I_{B2}|$$

Typical values for BJT  
general purpose op amps

$$I_B = 100 \text{ nA} \text{ and } I_{OS} = 10 \text{ nA}$$



# Input Bias Currents



Output DC Voltage  
 $V_O = I_{B1}R_2 \approx I_B R_2$

$$V_O = I_{B1}R_2$$

**Figure 2.33** Analysis of the closed-loop amplifier, taking into account the input bias currents.



# Compensation Resistor

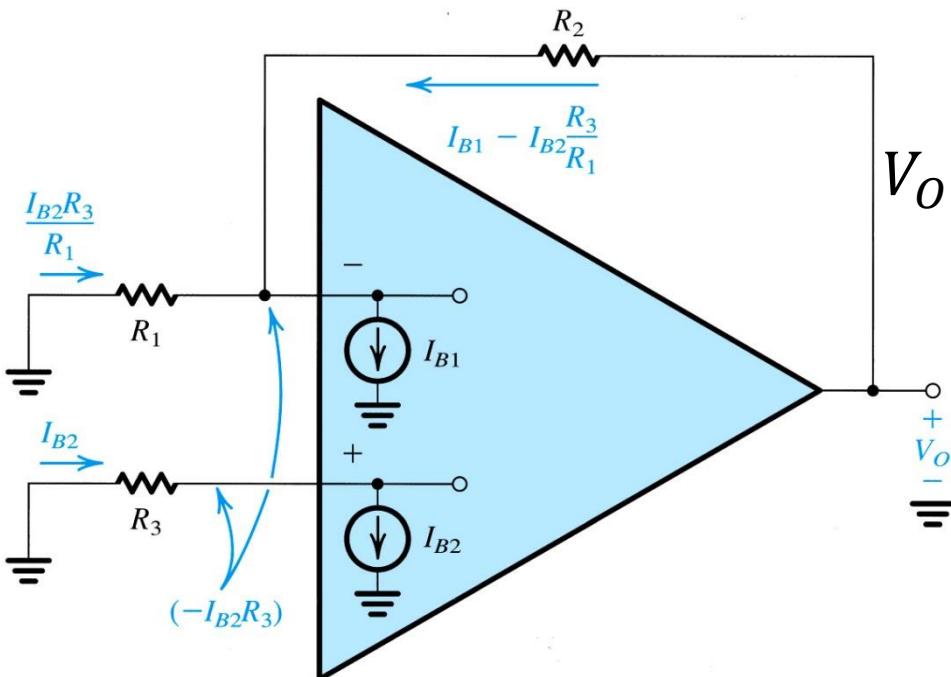


Figure 2.34 Reducing the effect of the input bias currents by introducing a resistor  $R_3$ .

Determining the appropriate value of  $R_3$

$$V_O = -I_{B2}R_3 + R_2(I_{B1} - I_{B2}R_3/R_1)$$

$$\text{If } I_{B1} = I_{B2} = I_B$$

$$V_O = I_B[R_2 - R_3(1 + R_2/R_1)]$$

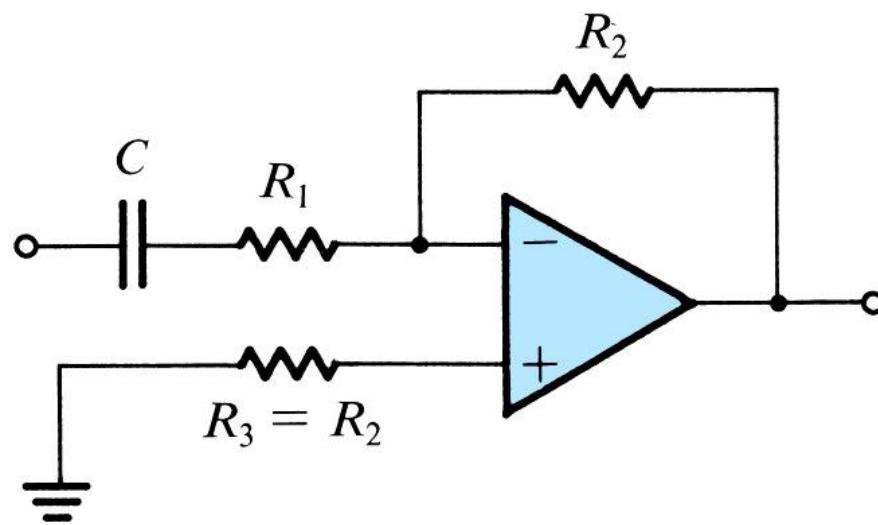
$$R_3 = \frac{R_2}{1 + R_2/R_1} = \frac{R_1R_2}{R_1 + R_2}$$

Using this value of  $R_3$  in the 1<sup>st</sup> equation

$$V_O = I_{OS}R_2$$



# Compensation Resistor



**Figure 2.35** In an ac-coupled amplifier the dc resistance seen by the inverting terminal is  $R_2$ ; hence  $R_3$  is chosen equal to  $R_2$ .

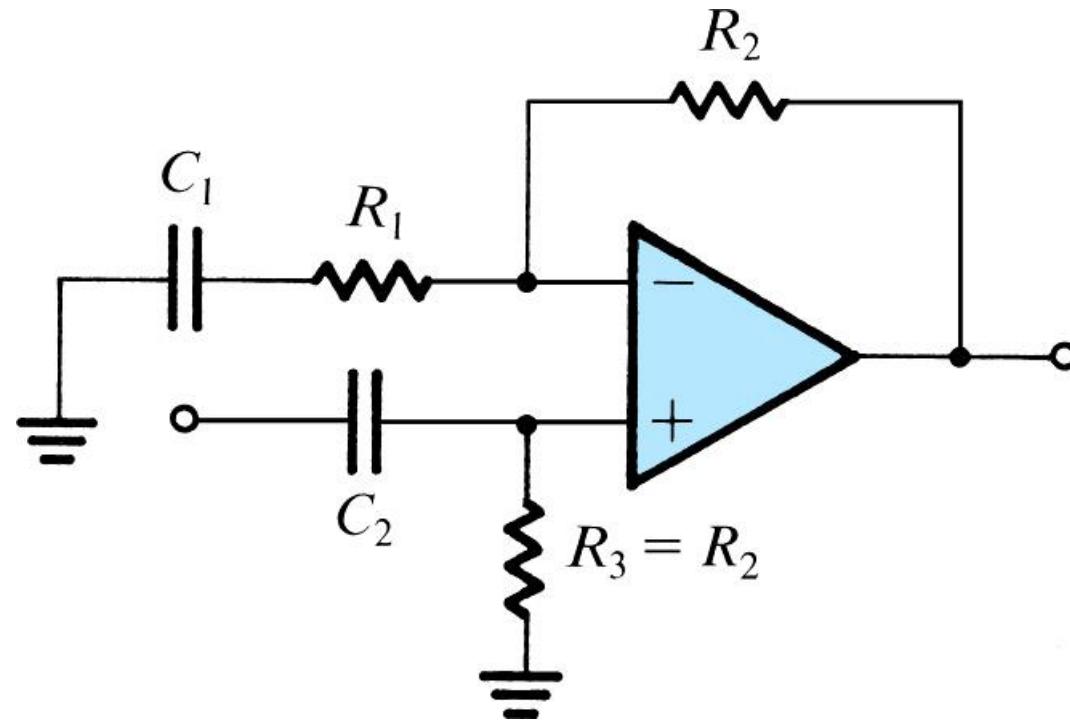
to minimize the effect of the input bias currents, one should place in the positive lead a resistance equal to the dc resistance seen by the inverting terminal. Therefore, for dc-coupled amplifier the appropriate value of  $R_3$  was found:

$$R_3 = \frac{R_2}{1 + R_2/R_1} = \frac{R_1 R_2}{R_1 + R_2}$$

For an ac-coupled amplifier the appropriate value is  $R_3 = R_2$ .



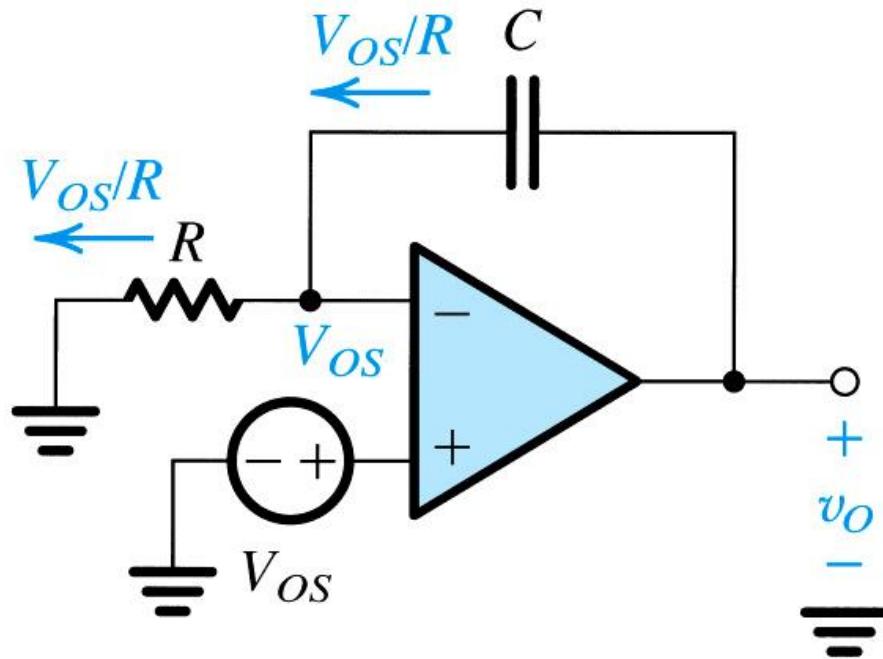
# dc Path to Ground Needed on Both Input Terminals



**Figure 2.36** Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will *not* work without resistor  $R_3$ .



# Effect of $V_{OS}$ on the Operation of the Inverting Integrator

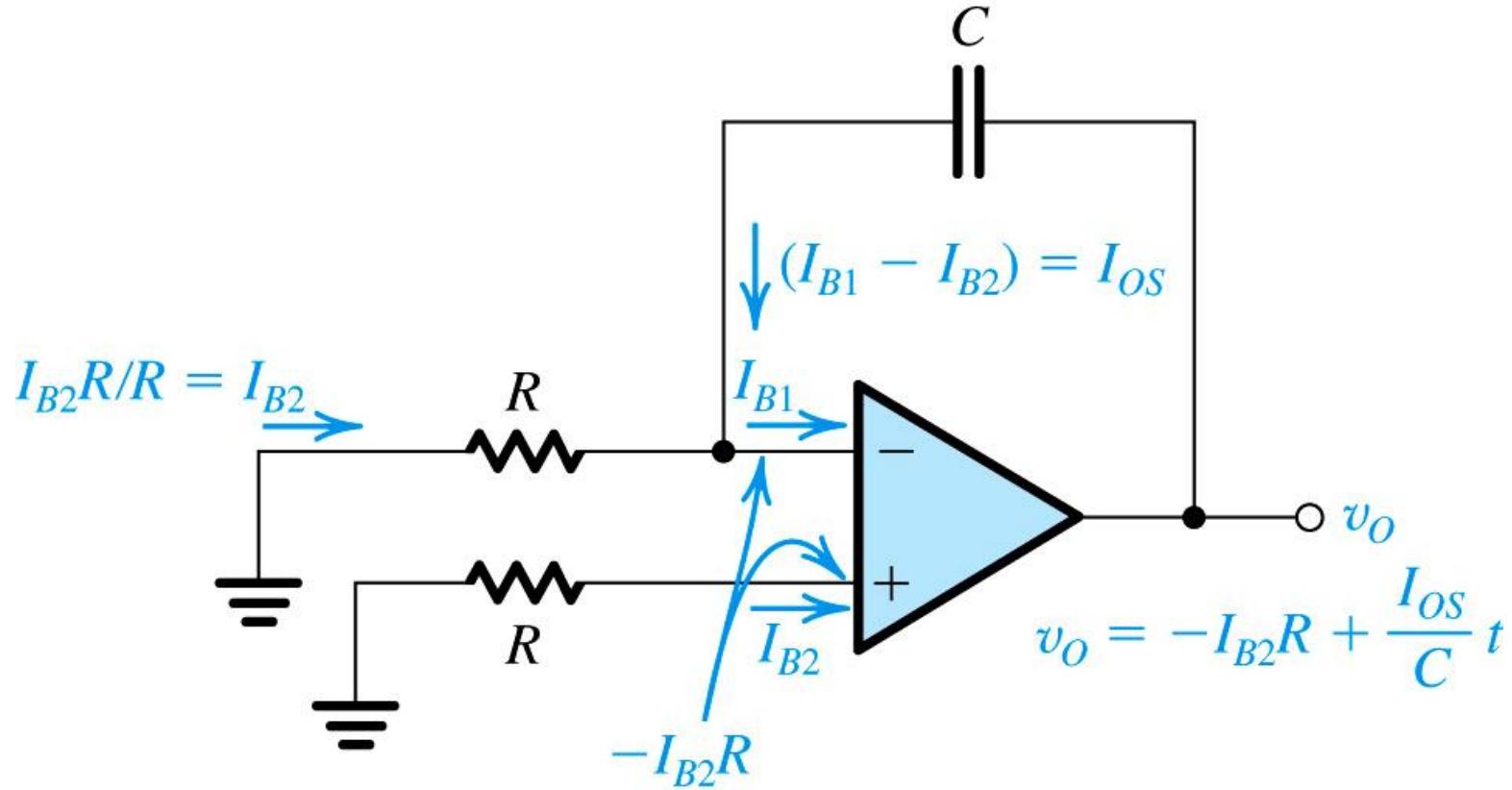


$$\begin{aligned}v_O &= V_{OS} + \frac{1}{C} \int_0^t \frac{V_{OS}}{R} dt \\&= V_{OS} + \frac{V_{OS}}{CR} t\end{aligned}$$

**Figure 2.37** Determining the effect of the op-amp input offset voltage  $V_{OS}$  on the Miller integrator circuit. Note that since the output rises with time, the op amp eventually saturates.



# Effect of $I_{OS}$ on the Operation of the Inverting Integrator



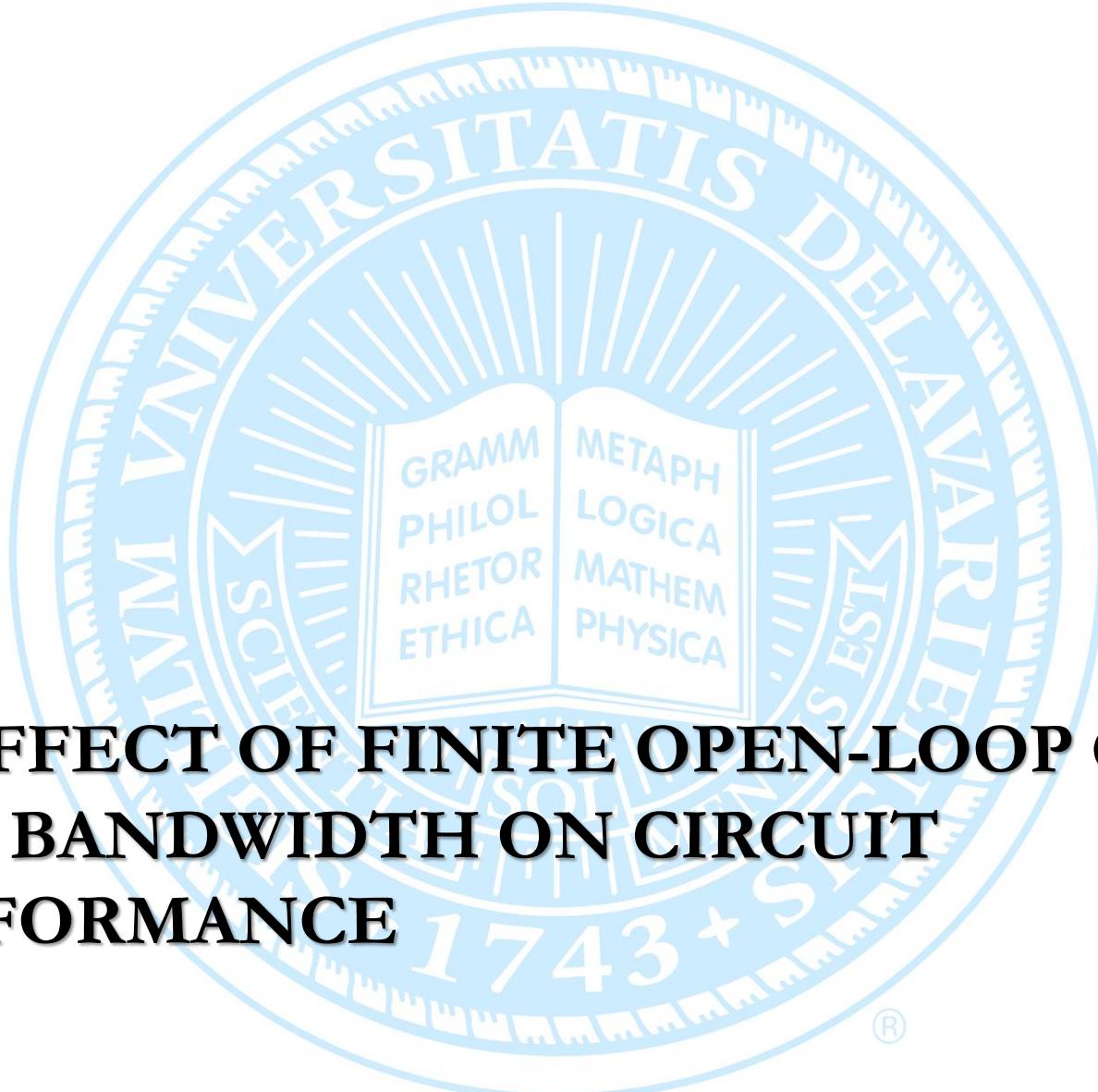
**Figure 2.38** Effect of the op-amp input bias and offset currents on the performance of the Miller integrator circuit.



# Homework #4

- Finish reading Chapter 2
- Chapter 2 Problems:
  - 2.60\*
  - 2.62
  - 2.68
  - 2.104\*
  - 2.111\*

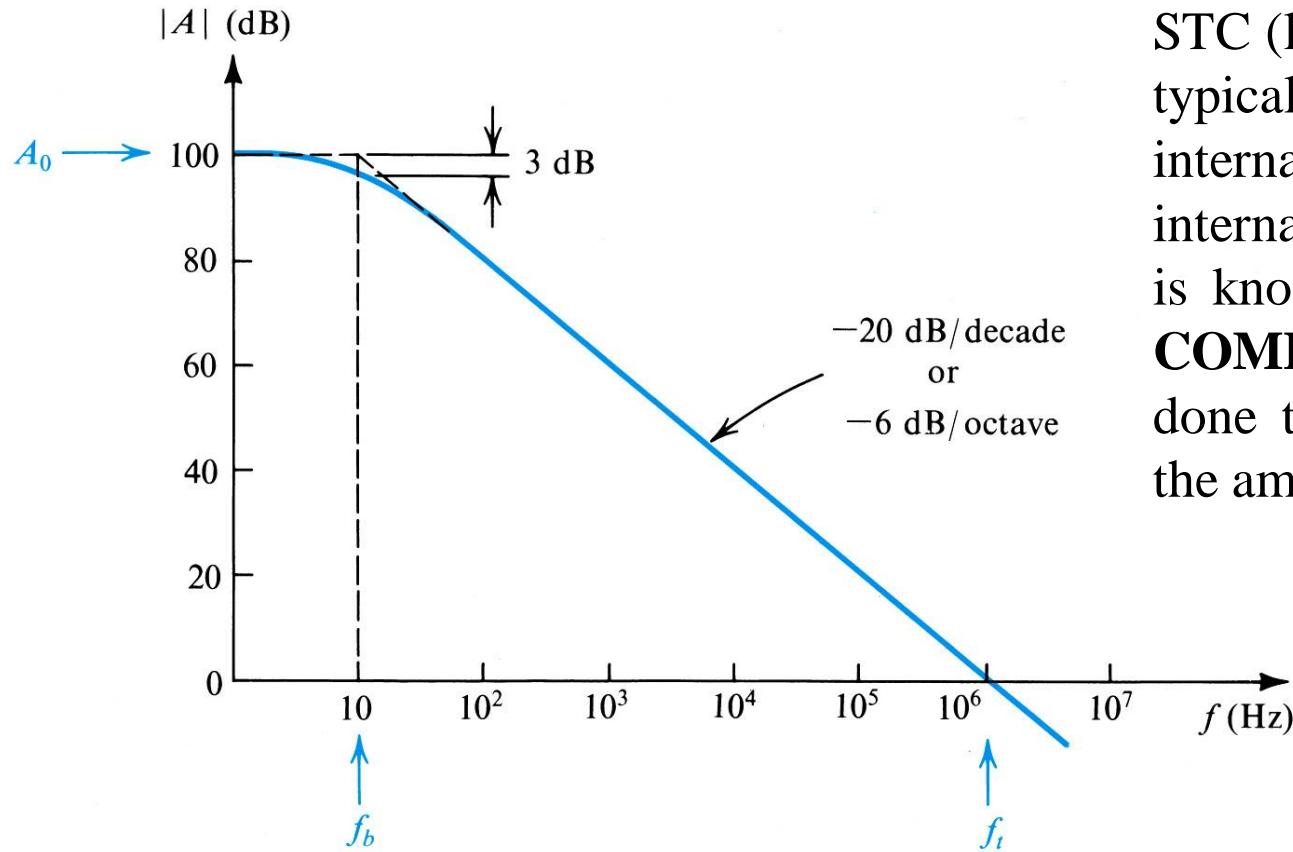
\* Answers in Appendix L



## 2.7 EFFECT OF FINITE OPEN-LOOP GAIN AND BANDWIDTH ON CIRCUIT PERFORMANCE



# Typical Open-Loop Gain, $|A|$

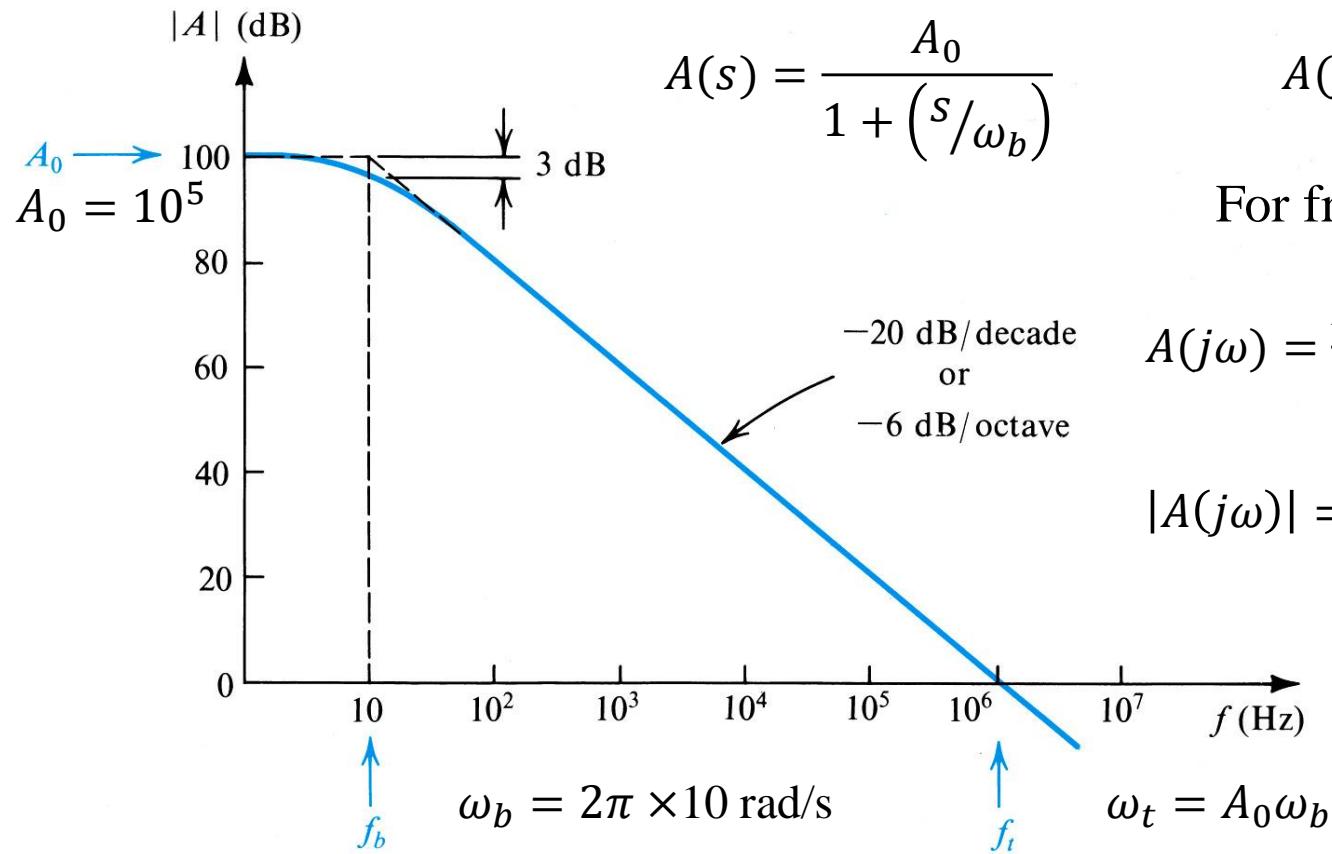


STC (low-pass) response of a typical op amp due to an internal capacitor used for internal compensation. This is known as **FREQUENCY COMPENSATION** and is done to enhance stability of the amplifier.

**Figure 2.39** Open-loop gain of a typical general-purpose internally compensated op amp.



# Typical Open-Loop Gain, $|A|$



$$A(s) = \frac{A_0}{1 + (s/\omega_b)}$$

$$A(j\omega) = \frac{A_0}{1 + j\omega/\omega_b}$$

For frequencies  $\gg \omega_b$

$$A(j\omega) = \frac{A_0 \omega_b}{j\omega}$$

$$A(j\omega) \cong \frac{\omega_t}{j\omega}$$

$$|A(j\omega)| = \frac{A_0 \omega_b}{\omega}$$

$$|A(j\omega)| \cong \frac{\omega_t}{\omega}$$

Figure 2.39 Open-loop gain of a typical general-purpose internally compensated op amp.



# Frequency Response of a Closed-Loop Inverting Amplifier

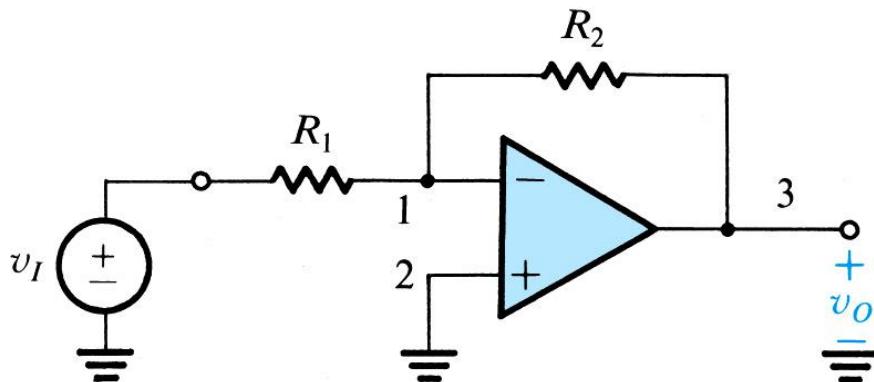


Figure 2.5 The inverting closed-loop configuration.

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

$$A(s) = \frac{A_0}{1 + (s/\omega_b)} \quad \omega_t = A_0\omega_b$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + \frac{1}{A_0} \left( 1 + \frac{R_2}{R_1} \right) + \frac{s}{\omega_t/(1 + R_2/R_1)}}$$

For  $A_0 \gg 1 + R_2/R_1$

$$\frac{V_o(s)}{V_i(s)} \approx \frac{-R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}}$$

$$\omega_{3dB} = \frac{\omega_t}{1 + R_2/R_1}$$



# Frequency Response of a Closed-Loop Noninverting Amplifier

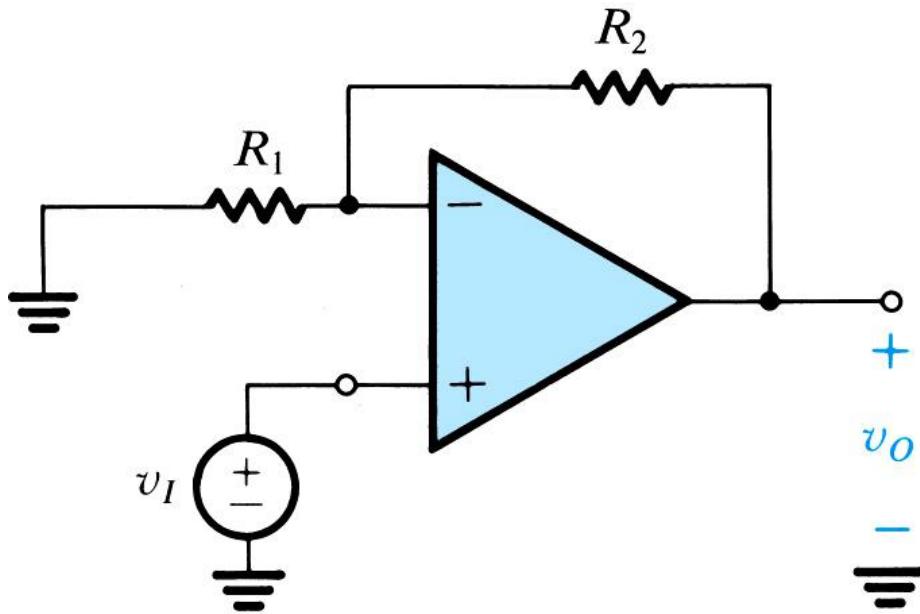


Figure 2.12 The noninverting configuration.

$$\frac{V_o}{V_i} = \frac{1 + R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

$$A(s) = \frac{A_0}{1 + (s/\omega_b)} \quad \omega_t = A_0\omega_b$$

For  $A_0 \gg 1 + R_2/R_1$

$$\frac{V_o(s)}{V_i(s)} \approx \frac{1 + R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}}$$

$$\omega_{3dB} = \frac{\omega_t}{1 + R_2/R_1}$$



## Example 2.6

Consider an op amp with  $f_t = 1$  MHz. Find the 3-dB frequency of closed-loop amplifiers with nominal gains of +1000, +100, +10, +1, -1, -10, -100, and -1000. Sketch the magnitude frequency response for the amplifiers with closed-loop gains of +10 and -10.

$$f_{3dB} = \frac{f_t}{1 + R_2/R_1}$$

$$A = 1 + \frac{R_2}{R_1}$$

$$A = -\frac{R_2}{R_1}$$

Closed Loop Gain	$R_2/R_1$	$f_{3dB}$
1000	999	1 kHz
100	99	10 kHz
10	9	100 kHz
1	0	1 MHz
-1	1	0.5 MHz
-10	10	90.9 kHz
-100	100	9.9 kHz
-1000	1000	999 Hz



## Example 2.6

Consider an op amp with  $f_t = 1$  MHz. Find the 3-dB frequency of closed-loop amplifiers with nominal gains of +1000, +100, +10, +1, -1, -10, -100, and -1000. Sketch the magnitude frequency response for the amplifiers with closed-loop gains of +10 and -10.

$$-10V/V = 20dB$$

$$f_0 = 90.9kHz$$

$$f_T = 909kHz$$

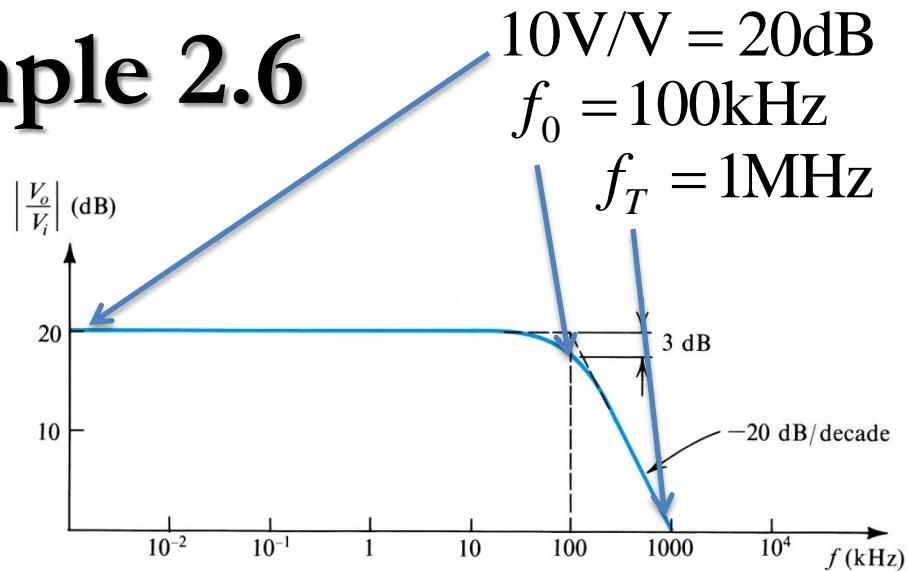


Figure 2.40 Frequency response of an amplifier with a nominal gain of +10 V/V.

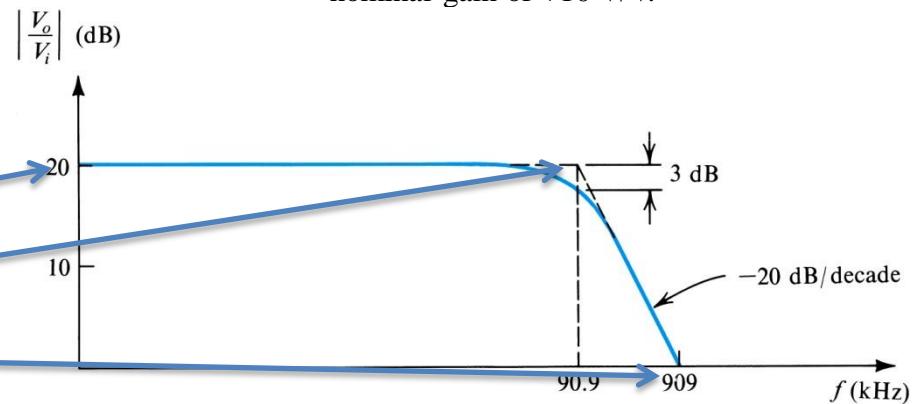
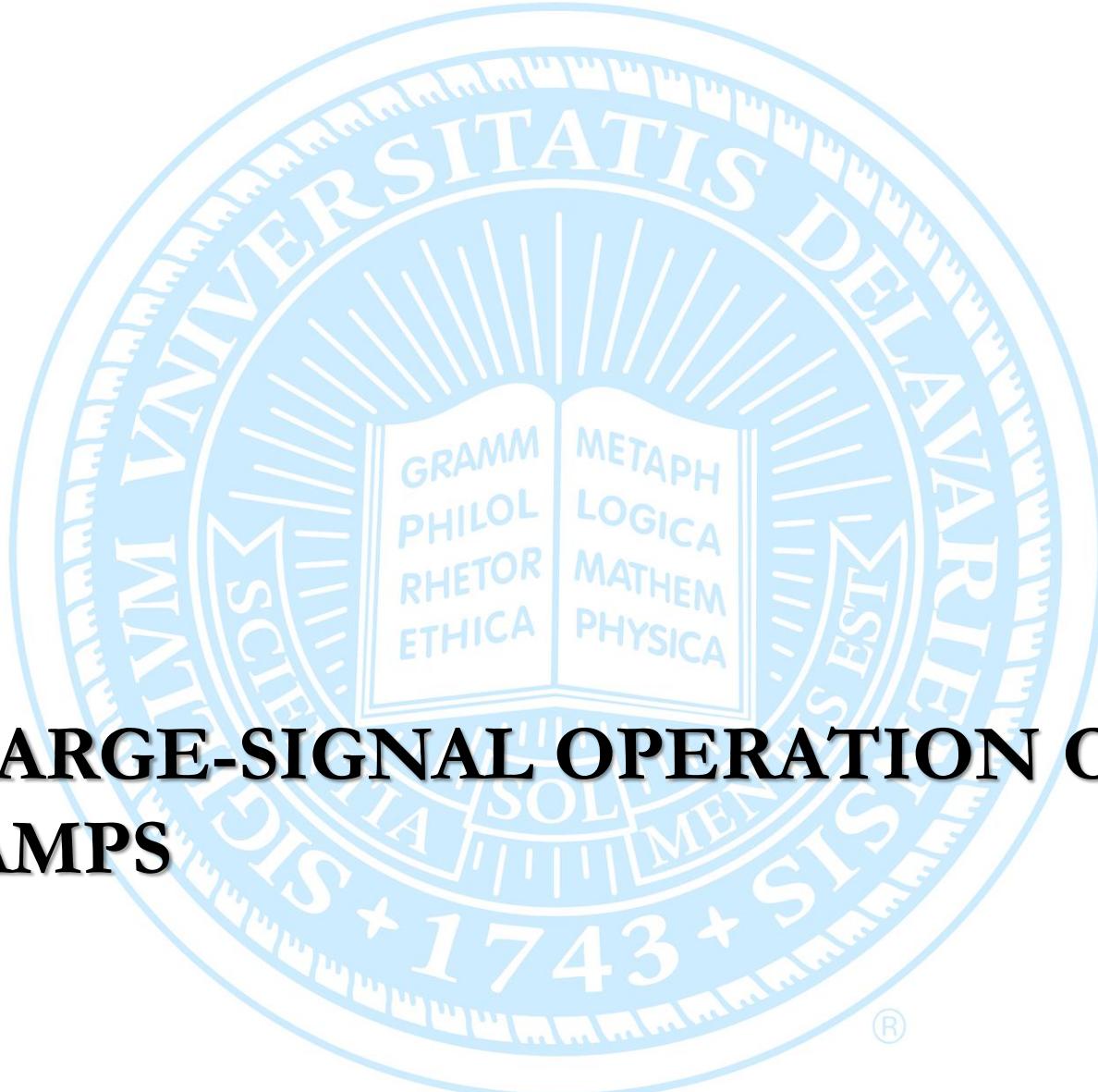


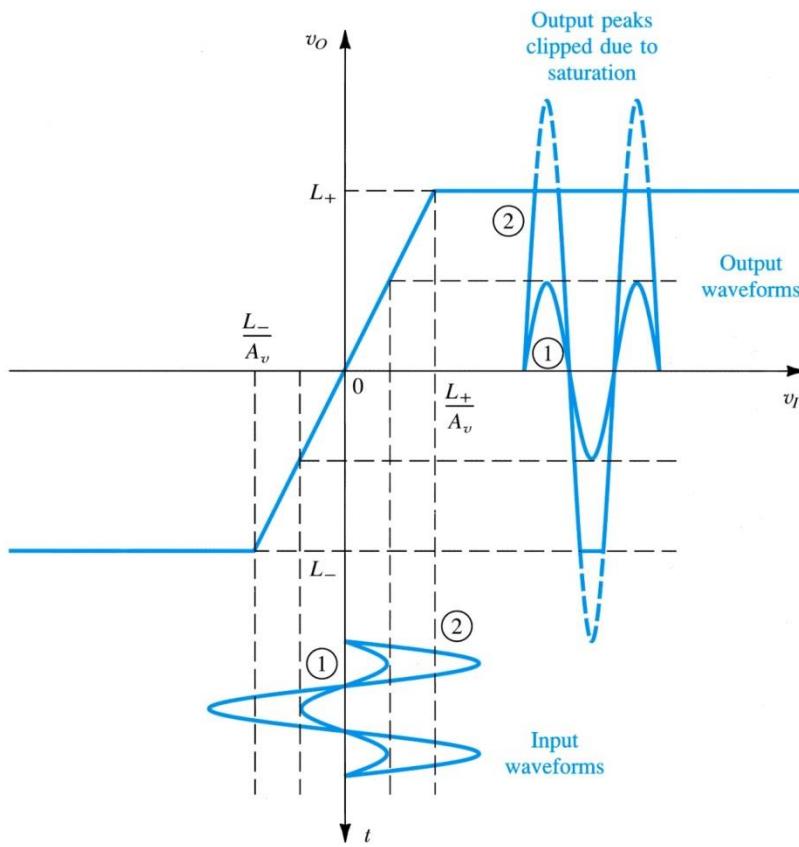
Figure 2.41 Frequency response of an amplifier with a nominal gain of -10 V/V.



## 2.8 LARGE-SIGNAL OPERATION OF OP AMPS



# Output Voltage Saturation and Current Limits

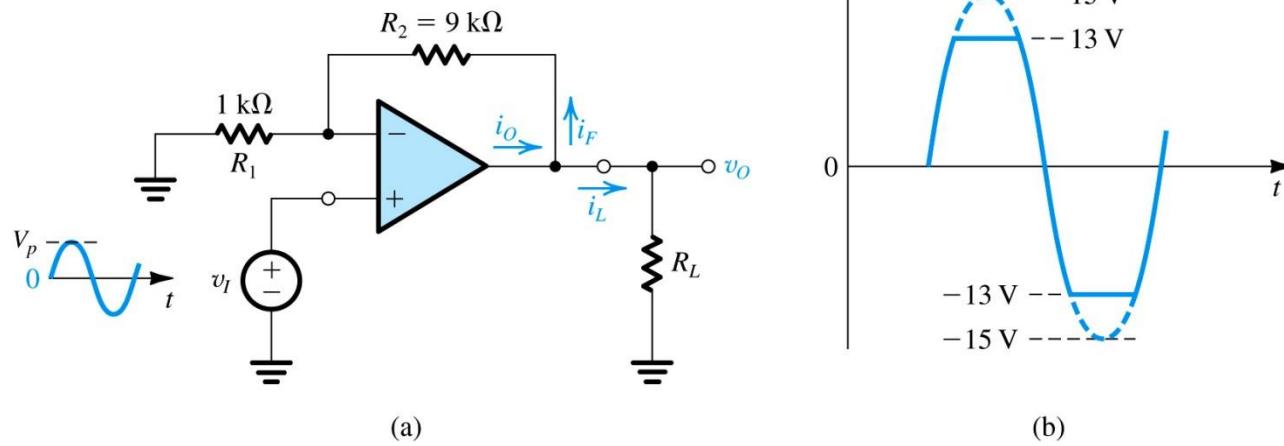


**Figure 1.14** An amplifier transfer characteristic that is linear except for output saturation.

Op amps have a **RATED OUTPUT VOLTAGE** that typically is within 1 V of the positive ( $V_{CC}$ ) or negative ( $V_{EE}$ ) supplies. Op amps also have a limit to the amount of current that they can source to the load.



# Example 2.7



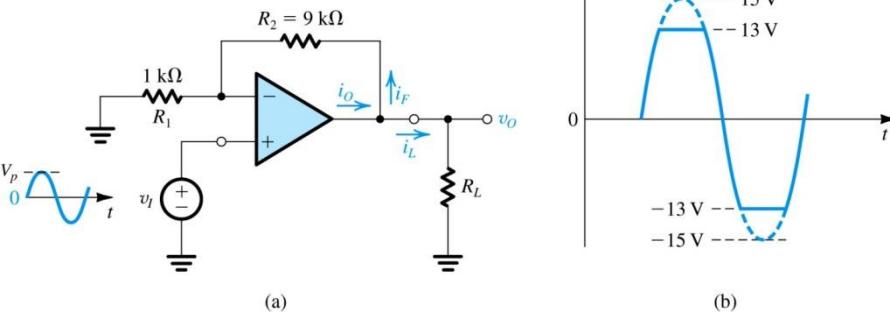
**Figure 2.42** (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at  $\pm 13$ -V output voltage and has  $\pm 20$ -mA output current limits. (b) When the input sine wave has a peak of 1.5 V, the output is clipped off at  $\pm 13$  V.

Consider the noninverting amplifier circuit shown in Fig. 2.42. As shown, the circuit is designed for a nominal gain  $(1 + R_2/R_1) = 10$  V/V. It is fed with a low-frequency sine-wave signal of peak voltage  $V_p$  and is connected to a load resistor  $R_L$ . The op amp is specified to have output saturation voltages of  $\pm 13$  V and output current limits of  $\pm 20$  mA.

- For  $V_p = 1$  V and  $R_L = 1$  kΩ, specify the signal resulting at the output of the amplifier.
- For  $V_p = 1.5$  V and  $R_L = 1$  kΩ, specify the signal resulting at the output of the amplifier.
- For  $R_L = 1$  kΩ, what is the maximum value of  $V_p$  for which an undistorted sine-wave output is obtained?
- For  $V_p = 1$  V, what is the lowest value of  $R_L$  for which an undistorted sine-wave output is obtained?



## Example 2.7 (a,b)



**Figure 2.42** (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at  $\pm 13$ -V output voltage and has  $\pm 20$ -mA output current limits. (b) When the input sine wave has a peak of 1.5 V, the output is clipped off at  $\pm 13$  V.

(a) For  $V_p = 1$  V and  $R_L = 1$  kΩ, specify the signal resulting at the output of the amplifier.

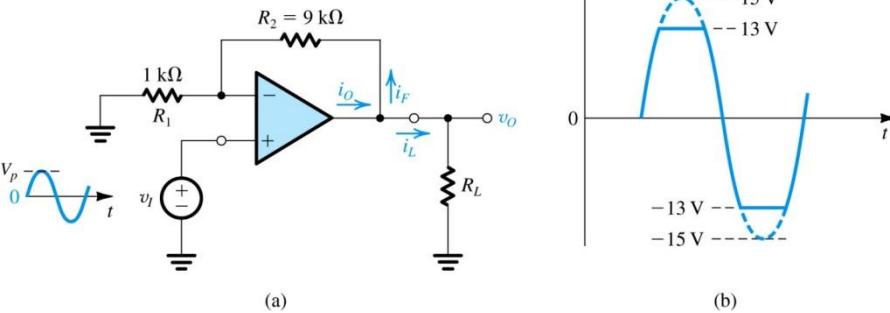
If  $V_p = 1$  V the output voltage will be 10 V so the amp will not clip. At 10V we will have 10 mA in the 1 kΩ load and 1 mA in the 10 kΩ feedback network for 11mA total < 20 mA spec.

(b) For  $V_p = 1.5$  V and  $R_L = 1$  kΩ, specify the signal resulting at the output of the amplifier.

If  $V_p = 1.5$  V the output voltage will be 15 V so the amp will clip at 13V. At 13V we will have 13 mA in the 1 kΩ load and 1.3 mA in the 10 kΩ feedback network for 14.3 mA total < 20 mA spec.



## Example 2.7 (c,d)



**Figure 2.42** (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at  $\pm 13$ -V output voltage and has  $\pm 20$ -mA output current limits. (b) When the input sine wave has a peak of 1.5 V, the output is clipped off at  $\pm 13$  V.

(c) For  $R_L = 1 \text{ k}\Omega$  what is the maximum value of  $V_p$  for which an undistorted sine-wave output is obtained?

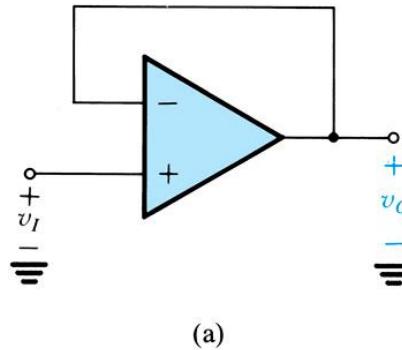
The maximum  $V_p$  will be 1.3 V to give an output voltage peak of 13 V which is at the edge of clipping.

(d) For  $V_p = 1 \text{ V}$ , what is the lowest value of  $R_L$  for which an undistorted sine-wave output is obtained?

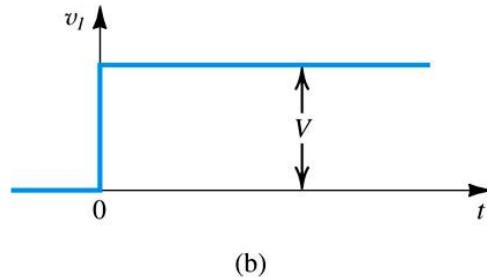
If  $V_p = 1 \text{ V}$  the output voltage will be 10 V so we will have 1 mA in the 10 kΩ feedback network so we can have 19 mA in the load so the  $R_L = 10\text{V}/19\text{mA} = 526 \Omega$ .



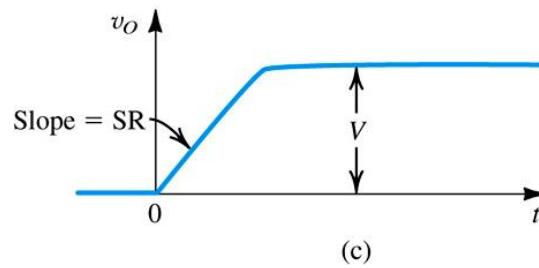
# Slew Rate



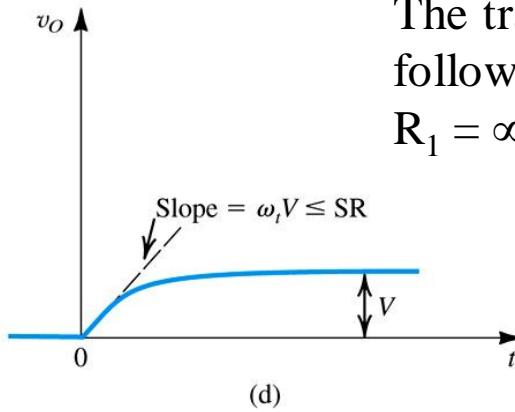
(a)



(b)



(c)



(d)

**Figure 2.43** (a) Unity-gain follower. (b) Input step waveform. (c) Linearly rising output waveform obtained when the amplifier is slew-rate limited. (d) Exponentially rising output waveform obtained when  $V$  is sufficiently small so that the initial slope ( $\omega_t V$ ) is smaller than or equal to SR.

**SLEW RATE (SR)** is the maximum rate of change at the output of the op amp.

$$SR = \frac{dv_o}{dt} \Big|_{\max}$$

The transfer function for the unity gain follower can be found by substituting  $R_1 = \infty$  and  $R_2 = 0$  into:

$$\frac{V_o(s)}{V_i(s)} \approx \frac{1 + R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + s/\omega_t}$$

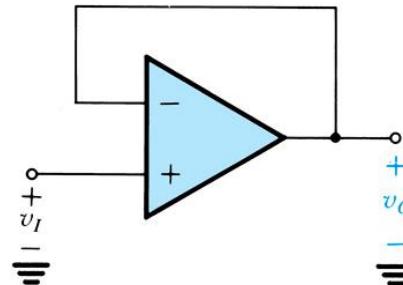
$$v_o(t) = V(1 - e^{1/\omega_t t})$$



# Full-Power Bandwidth, $f_M$

$$v_I = \hat{V}_i \sin \omega t$$

$$\frac{dv_I}{dt} = \omega \hat{V}_i \cos \omega t$$



Theoretical  
output

$$\omega_M V_{omax} = SR$$

$$\omega_M = \frac{SR}{V_{omax}}$$

$$f_M = \frac{SR}{2\pi V_{omax}}$$

$$V_o = V_{omax} \left( \frac{\omega_M}{\omega} \right)$$

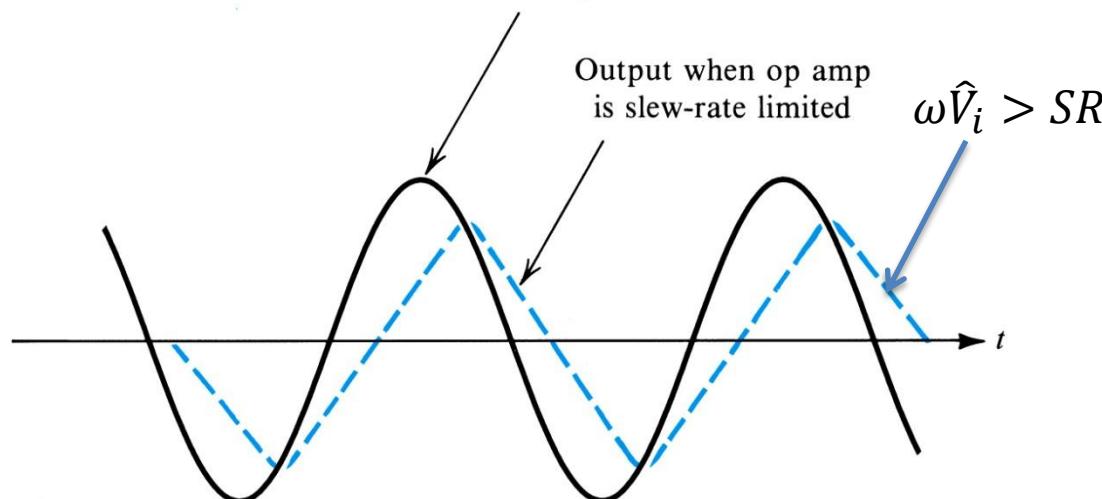


Figure 2.44 Effect of slew-rate limiting on output sinusoidal waveforms.



# Summary

- The IC op amp is a versatile circuit building block. It is easy to apply, and the performance of op-amp circuits closely matches theoretical predictions.
- The op-amp terminals are the inverting input terminal (1), the noninverting input terminal (2), the output terminal (3), the positive-supply terminal (4) to be connected to the positive power supply ( $V_{CC}$ ), and the negative-supply terminal (5) to be connected to the negative supply ( $-V_{EE}$ ). The common terminal of the two supplies is the circuit ground.
- The ideal op amp responds only to the difference input signal, that is,  $(v_2 - v_1)$  providing at the output, between terminal 3 and ground, a signal where  $A(v_2 - v_1)$ , the open-loop gain, is very large ( $10^4$  to  $10^6$ ) and ideally infinite; and has an infinite input resistance and a zero output resistance. (See Table 3.1.)



# Summary Continued

- Negative feedback is applied to an op-amp by connecting a passive component between its output terminal and its inverting (aka. negative) input terminal.
- Negative feedback causes the voltage between the two input terminals to become very small, and ideally zero. Correspondingly, a virtual short is said to exist between the two input terminals. If the positive input terminal is connected to ground, a virtual ground appears on the negative terminal.
- The two most important assumptions in the analysis of op-amp circuits, assuming negative feedback exists, are:
  - the two input terminals of the op-amp are at the same voltage potential.
  - zero current flows into the op-amp input terminals.
- With negative feedback applied and the loop closed, the gain is almost entirely determined by external components:  $V_o/V_i = -R_2/R_1$  or  $1+R_2/R_1$ .



# Summary Continued

- The non-inverting closed-loop configuration features a very high input resistance. A special case is the unity-gain follower, frequently employed as a buffer amplifier to connect a high-resistance source to a low-resistance load.
- The difference amplifier of Figure 2.16 is designed with  $R_4/R_3 = R_2/R_1$ , resulting in  $v_o = (R_2/R_1)(v_{I2} - v_{I1})$ .
- The instrumentation amplifier of Figure 2.20(b) is a very popular circuit. It provides  $v_o = (1+R_2/R_1)(R_4/R_3)(v_{I2} - v_{I1})$ . It is usually designed with  $R_3 = R_4$  and  $R_1$  and  $R_2$  selected to provide the required gain. If an adjustable gain is needed, part of  $R_1$  can be made variable.

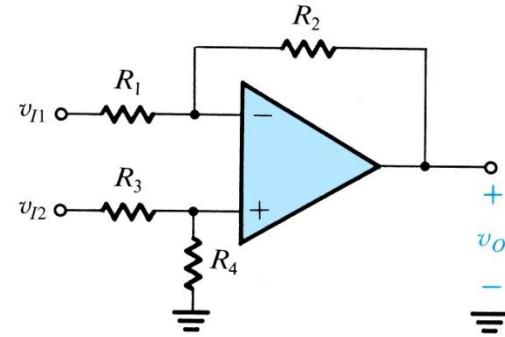


Figure 2.16

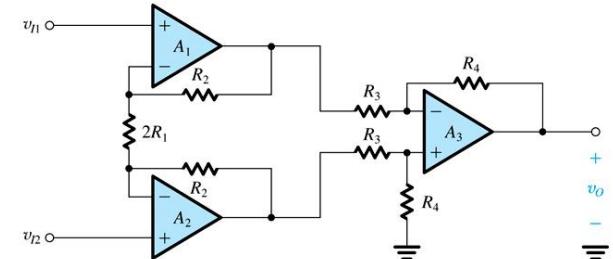


Figure 2.20(b)



# Summary Continued

- The inverting Miller Amplifier of Figure 2.24 is a popular circuit, frequently employed in analog signal-processing functions such as filters (Chapter 16) and oscillators (Chapter 17).

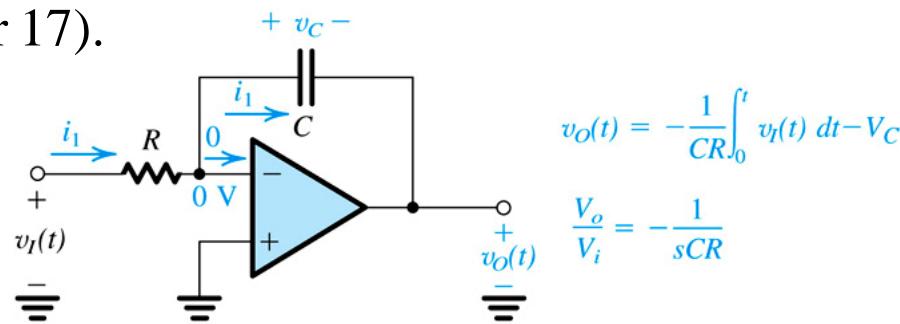


Figure 2.24

- The input offset voltage ( $V_{OS}$ ) is the magnitude of dc voltage that when applied between the op-amp input terminals, with appropriate polarity, reduces the dc offset at the output.