CPEG660-VLSI-Project2-Proposal

8_Inputs_Responder, to find which input is fastest.

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1. Total description:

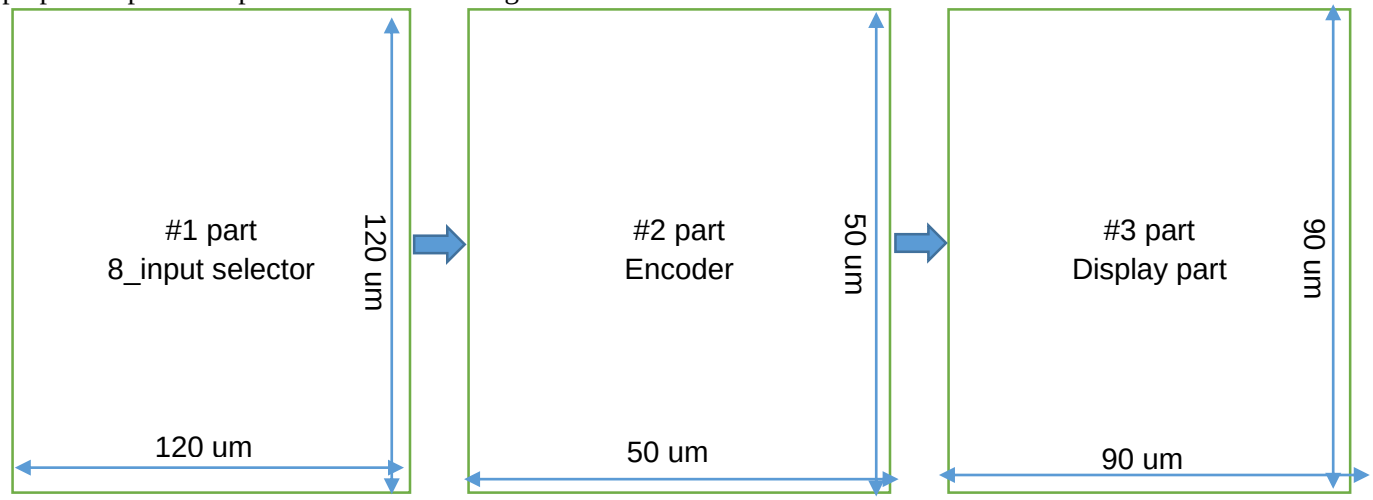
We want to design a circuit to respond which one of the eight input signal comes in first. In the first part, we use D-Flip Flop and 8-input NAND gate to lock other inputs when the fastest one comes in. In the middle part, we need to change the 8 outputs of the D-Flip flop to 4 inputs. In the last part, the fastest one is shown by how many LCD lights are lighted when attached to output circuit. (LCD lights are not included in our circuit).

2. Table of all input and output pins

I/O	Input								Output							
Name	A0	A1	A2	A3	A4	A5	A6	A7	a	b	c	d	e	f	g	h

3. Floorplan

We prepare to put three parts from left to the right.

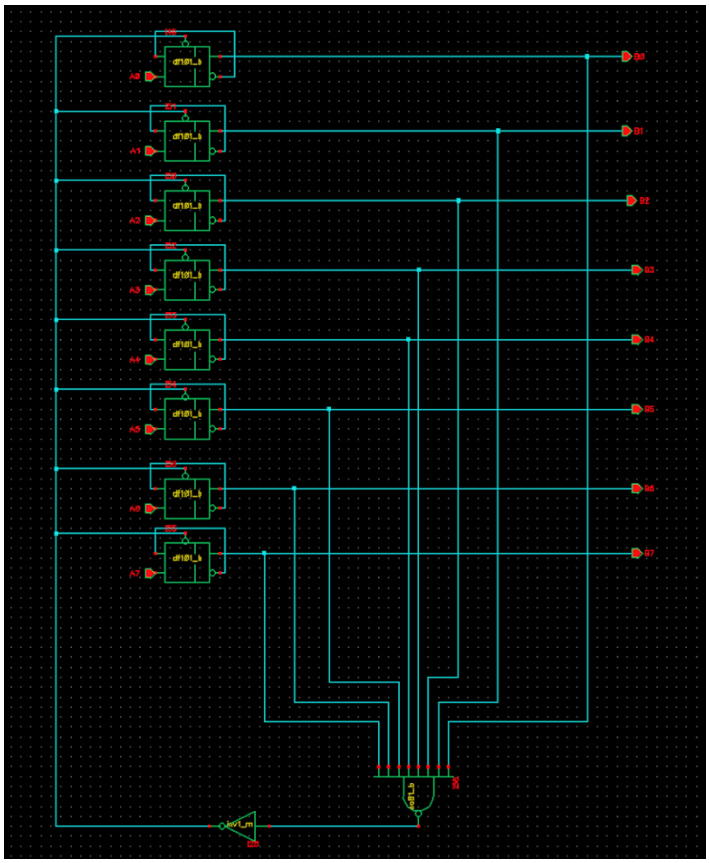


4. Introduction of each part

(i) 8_Input selector

This part is to recognize the one which catch the command more quickly after start. It mainly used D flip flop to deliver signal.

Part #1 Schematic



(ii) Encoder

This part is designed to transform the eight inputs to 4 binary bits (1 represents for high voltage and 0 represents for low voltage) to represent which one is the fastest.

Part #2 Truth Table

Input								Output			
B0	B1	B2	B3	B4	B5	B6	B7	C3	C3	C1	C0
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	1	0	1
0	0	0	0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	1	1	0	0	0

The principle of output:

C0 = B0 + B2 + B4 + B6

C1 = B1 + B2 + B5 + B6

C2 = B3 + B4 + B5 + B6

C3 = B7

(iii) Logical part to show which one is the fastest

The output will connect to 7 LCD lights and the numbers of LCD lights which are turned on represents the number of the voter. So when lights turn on, it means someone is the fastest.

Part #3 Truth Table

Input				Output							
C3	C2	C1	C0	a	b	c	d	e	f	g	h
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	1	1
0	0	1	1	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	1	1	1	1
0	1	0	1	0	0	0	1	1	1	1	1
0	1	1	0	0	0	1	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1