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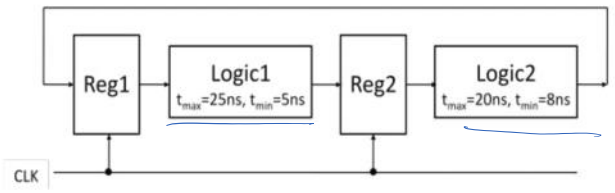
Study guide for the second exam

1. Analyze the sequential circuit shown below. Assume the registers are edge triggered with tclk-q, max = 4ns, tclk-q, min = 2ns, tsetup = 1ns, and thold = 1ns:



a. What is the maximum operating frequency of this system if there is no skew and jitter?

b. What is the maximum random clock skew that this system can tolerate?

$F = \frac{1}{T}$

Solution:

(1)

$T > t_{c-q,max} + t_{logic,max} + t_{setup}$
$T > 4ns + 25ns + 1ns = 30ns$
$T > 4ns + 20ns + 1ns = 25ns$
$\Rightarrow F_{clk\,max} = 33.3MHz$

(2)

$t_{skew} + t_{hold} < t_{c-q,min} + t_{logic,min}$
$t_{skew} < 2ns + 5ns - 1ns = 6ns$
$t_{skew} < 2ns + 8ns - 1ns = 9ns$
$\Rightarrow t_{skew,max} = 6ns$

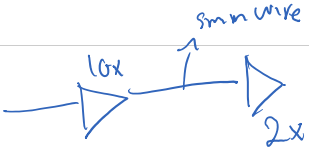
2. Consider a 5 mm-long, 1-micron wide metal2 wire in a 0.6 m process. The sheet resistance is 0.08 ohms/square, and the capacitance is 0.2 f F / m. Construct a 3-segment PI-model for the wire.

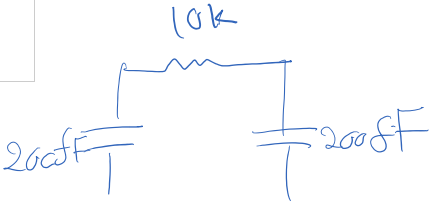
$R = R_D \frac{L}{W} = 0.08 \cdot \frac{5\times10^{-3}}{1\times10^{-6}} = 0.08 \times 5000 = 400\,\Omega$

$R = 10K$
$C = 400\,fF$

3. A 10x unit-sized inverter drives a 2x inverter at the end of the 5 mm wire from Exercise 2. Assume 1X inverter has input capacitance of 6fF and output resistance of 10KOhm. Estimate the propagation delay using the Elmore delay model; neglect diffusion capacitance.

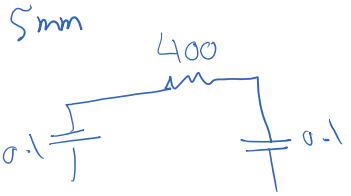
$C = 6fF$
$R = 10K$





$R = 1K$
$C = 60fF$

$R = 5K$
$C = 12fF$



0.1μF 0.1μF 100+

$D = RC$

$R_1 \cdot C_1 + (R_1 + R_2) \cdot C_2 + (R_1 + R_2 + R_N) C_N$

$1K \cdot 0.1\mu F + (1.4K)\, 0.1\mu F + 6.4K \cdot 0.12\mu F$

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Example

- Compute the sheet resistance of a 0.22 μm thick Cu wire in a 65 nm process. The resistivity of thin film Cu is 2.2 x 10-8 Ω•m. Ignore dishing.

$$R_W = \frac{\rho}{t} = \frac{2.2 \times 10^{-8}\ \Omega \cdot m}{0.22 \times 10^{-6}} = 0.1\ \frac{\Omega}{\square}$$

- Find the total resistance if the wire is 0.125 μm wide and 1 mm long. Ignore the barrier layer.

$$R = R_W \cdot \frac{L}{W} = 0.1 \frac{1}{0.128 \times 10^{-3}} = 800\ \Omega$$

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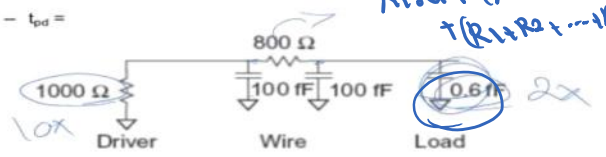
Wire RC Delay

- Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 1 mm wire. Assume wire capacitance is 0.2 fF/μm and that a unit-sized inverter has R = 10 KΩ and C = 0.1 fF.

– t_{pd} =



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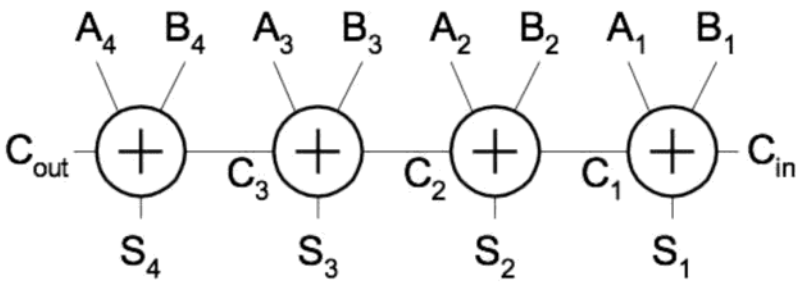
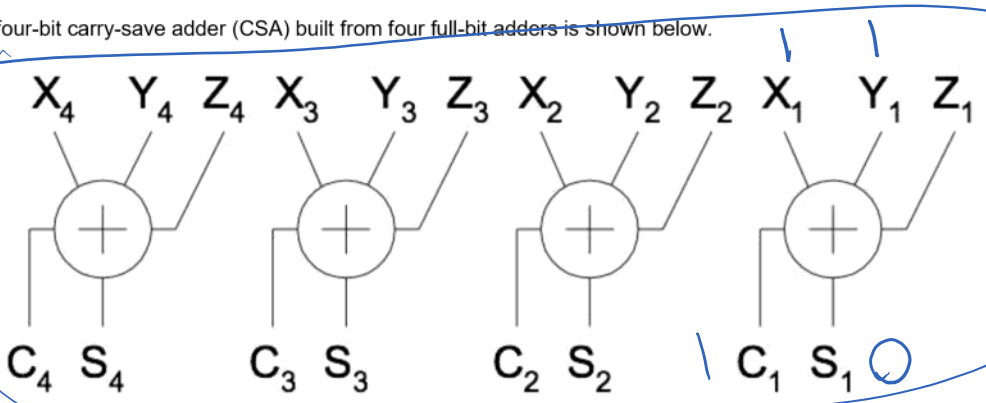
4. A four-bit carry ripple adder (CRA) built from four full-bit adders is shown below. [10]



A four-bit carry-save adder (CSA) built from four full-bit adders is shown below.



Suppose we want to add four 4-bit words (e.g. 0001 + 0111 + 1101 + 0010 = 10111). The left-side schematic shows how to do this using three CPA adders. The right-side schematic shows how to do this using two CSA adders and one CRA adder. How many full-bit adders does each circuit use? Assume that a full-adder has the longest propagation delay from any input to any output of T_0, what is the propagation delay for each circuit?

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1 full adder pd = t0

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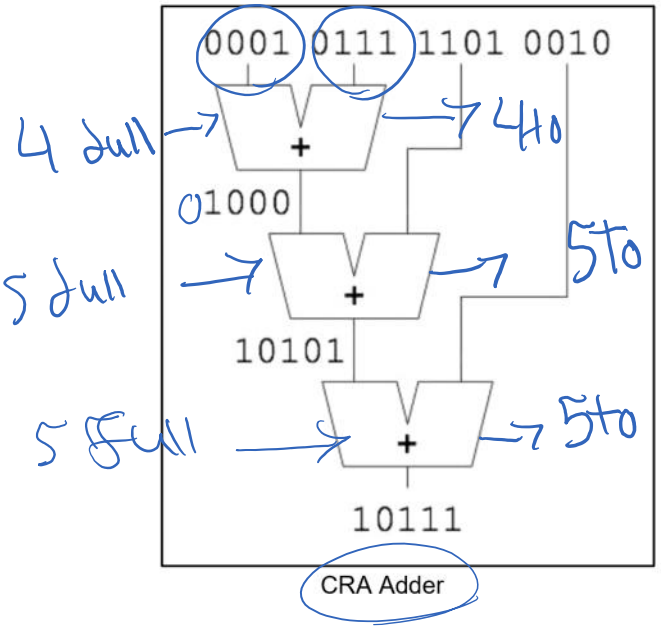
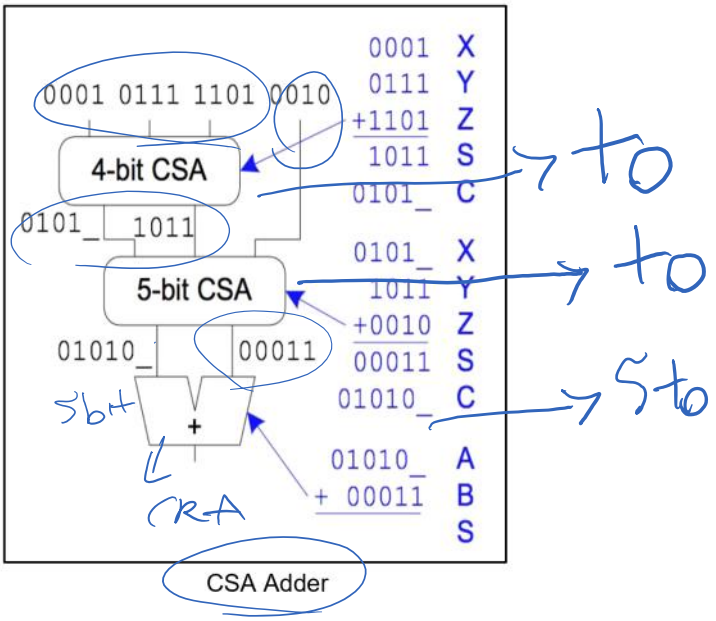


CRA Adder



CSA Adder

Full adders in CRA adder = 14

Full adders in CSA adder = 14

Propagation delay for CRA adder = 14t0

Propagation delay for CSA adder = 7t0

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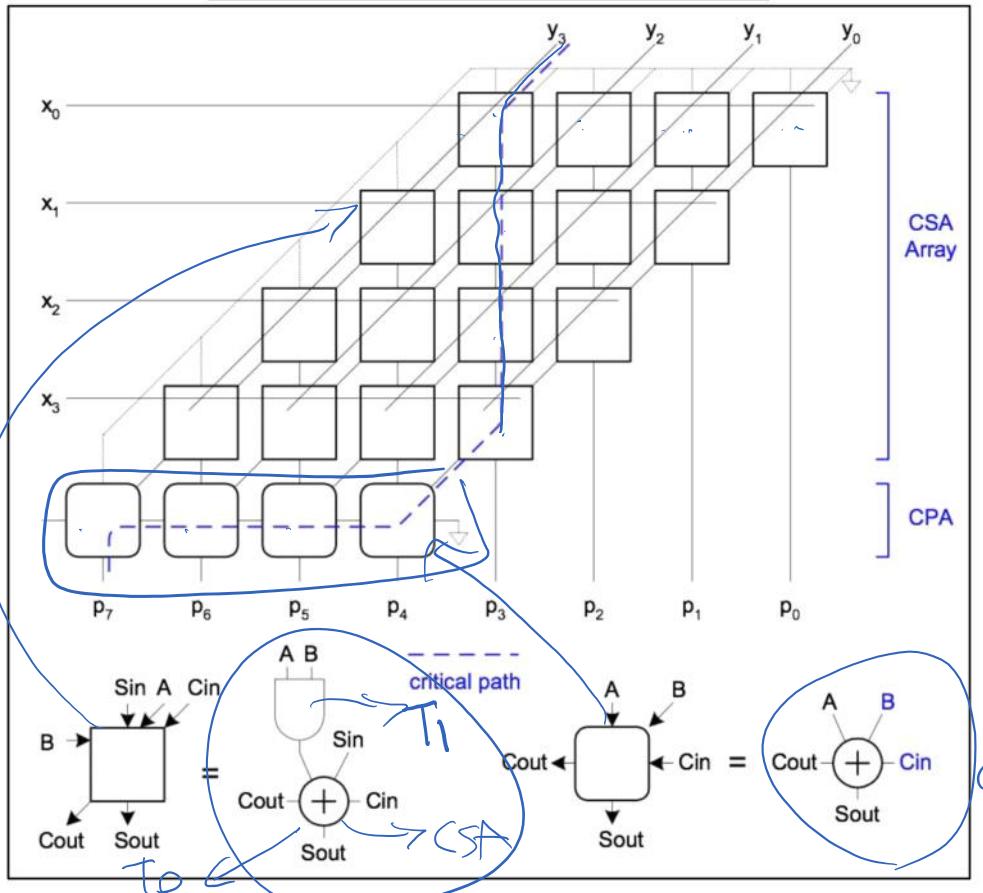
5. Suppose you want to multiply two 4-bit numbers. The circuit to realize this is shown below. How many full-bit adders does this circuit use? Assume that a full-adder has propagation delay from any input to any output of T_0, and "and" gate delay of T_1, what is the propagation delay for the highlighted critical path? [5]

```
    1100 : 12(10)      multiplicand
    0100 : 5(10)       multiplier
    1100
   0000               partial
  110000              products
 0000000
00111100 : 60(10)      product
```



Full adders in four-bit multiplier = 20

Propagation delay for four-bit multiplier = _____

$4 \cdot T_1 + 4T_0 + 4T_0 = 8T_0 + 4T_1$

$4(T_1 + T_0)$

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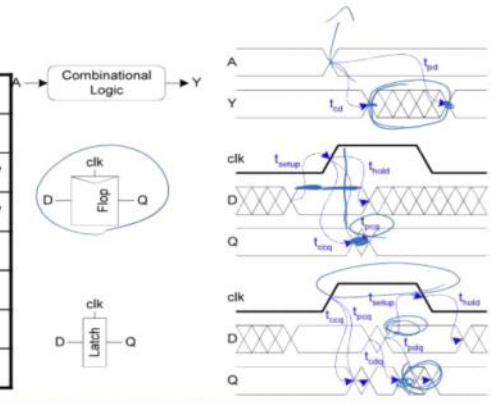
Timing Diagrams

Contamination and Propagation Delays

t_{pd}	Logic Prop. Delay
t_{cd}	Logic Cont. Delay
t_{pcq}	Latch/Flop Clk->Q Prop. Delay
t_{ccq}	Latch/Flop Clk->Q Cont. Delay
t_{pdq}	Latch D->Q Prop. Delay
t_{cdq}	Latch D->Q Cont. Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time



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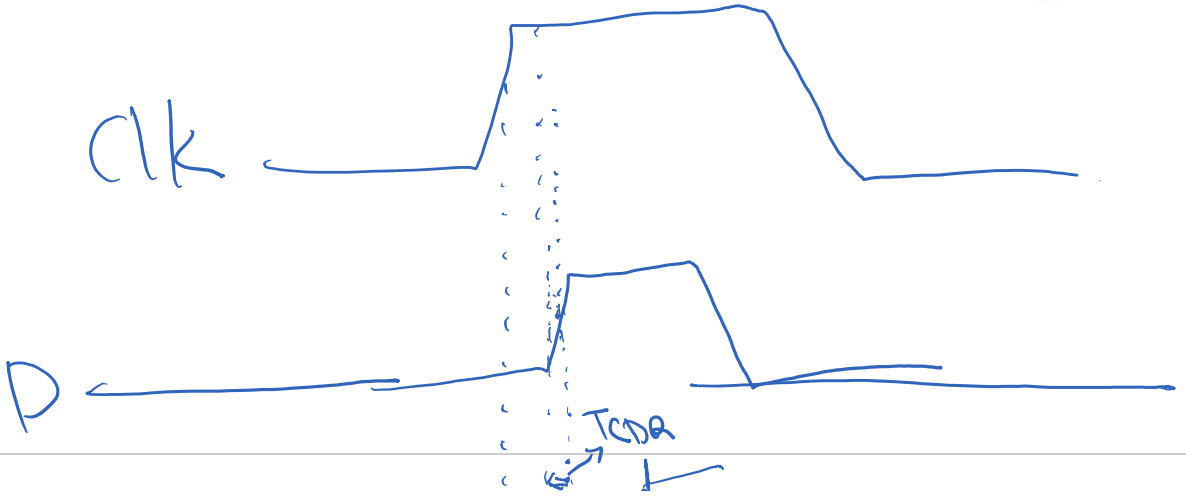
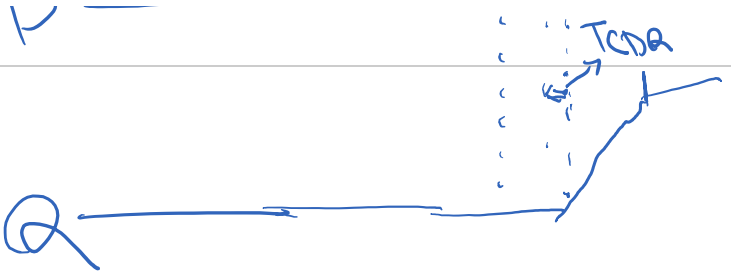
t_{pd}	Logic Propagation Delay	Longest delay from input A to output Y in logic block
t_{cd}	Logic Contamination Delay	SHORTEST
t_{pLQ}	Latch/Flop Clk->Q Prop. Delay	LONGEST delay from CLK to Q
t_{CCQ}	Latch/Flop Clk->Q Cont. Delay	SHORTEST
t_{pDQ}	Latch D->Q Prop. Delay	LONGEST delay from D to Q
t_{cdQ}	Latch D->Q Cont. Delay	SHORTEST
t_{SETUP}	Latch/Flop Setup Time	how long DATA must be stable before edge CLK
t_{HOLD}	Latch/Flop Hold Time	how long DATA stable AFTER CLK edge




TCDR

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Multiplication

- Example:

```
1100 : 12(10)      multiplicand
0101 : 5(10)       multiplier
1100
0000               partial
1100               products
0000
0111 1100          product
```

- M x N-bit multiplication
  - Produce N M-bit partial products
  - Sum these to produce M+N-bit product

18: Datapath Functional Units CMOS VLSI Design 4th Ed. 14