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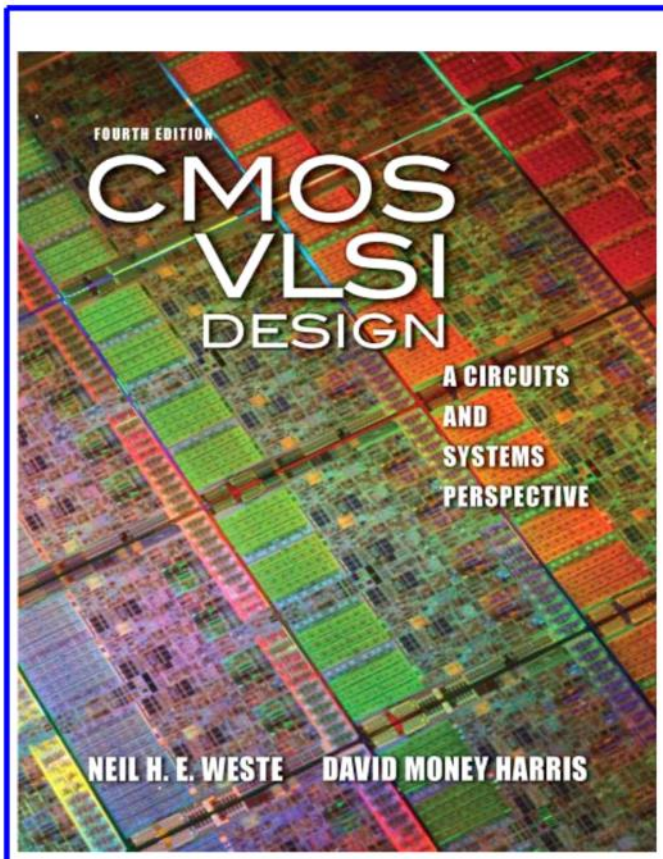

Lecture 11: Combinational Circuit Design

Project 1

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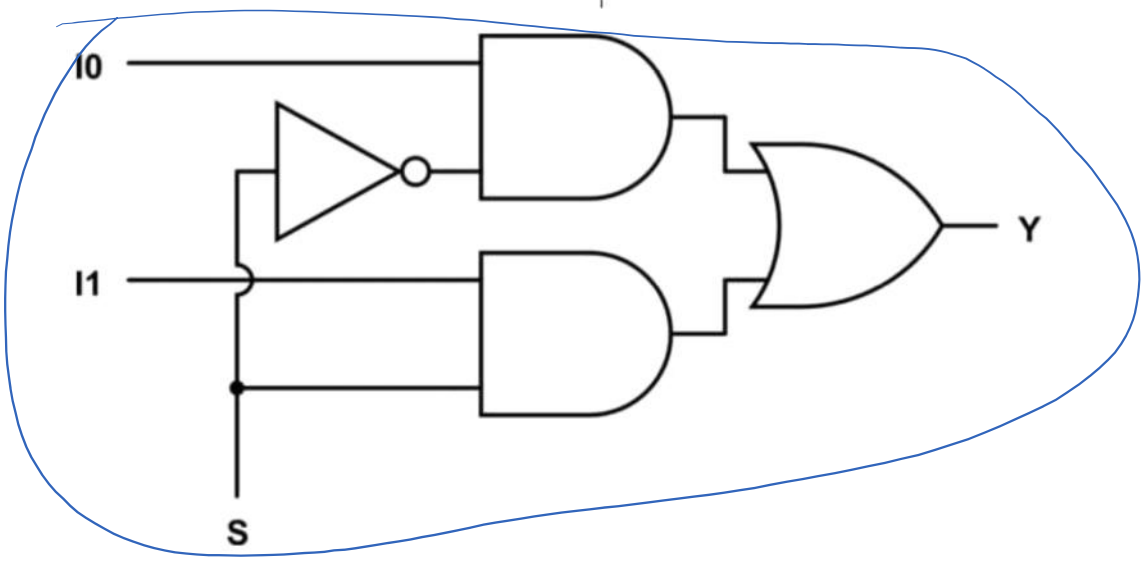
Project 1, Part 1

Create the schematic for a 2:1 MUX and simulate it.

S	Y
0	$I0$
1	$I1$



What to turn in:

1. Schematic of the 2:1 MUX
2. Schematic used to simulate the 2:1 MUX
3. Simulation Results

Reference Images:

- Images shown below are for reference only. Your schematic can look different and does not have to look identical to these images.
- For the simulation, be sure to graph the following in the 2:1 MUX
    - The selector
    - Input 1
    - Input 2
    - output

  Also, be sure to clearly mark which net represent which input or output as the reference image is shown. Failure to do this will have an impact on your grade.

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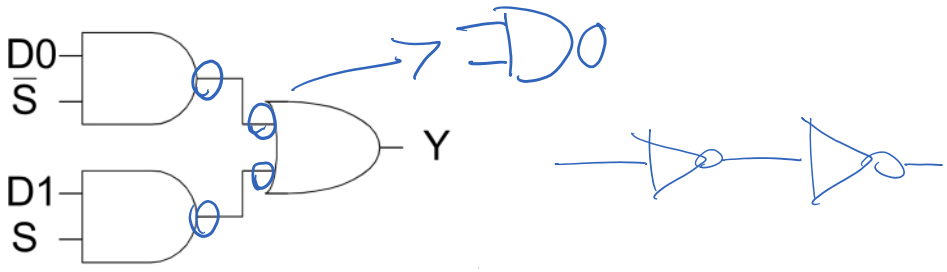
Outline

- Bubble Pushing
- Compound Gates
- Logical Effort Example
- Input Ordering
- Asymmetric Gates
- Skewed Gates
- Best P/N ratio

Example 1

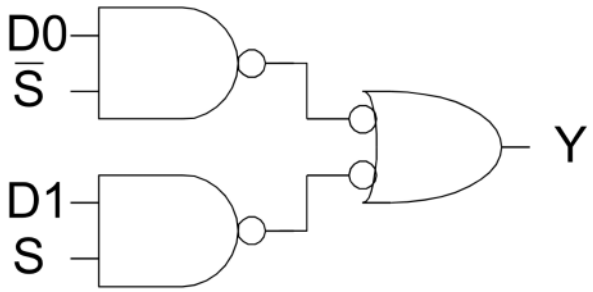
```
module mux(input  s, d0, d1,
           output y);

   assign y = s ? d1 : d0;
endmodule
```

1) Sketch a design using AND, OR, and NOT gates.



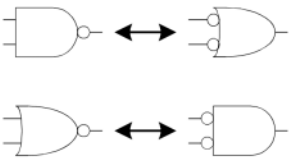
Example 2

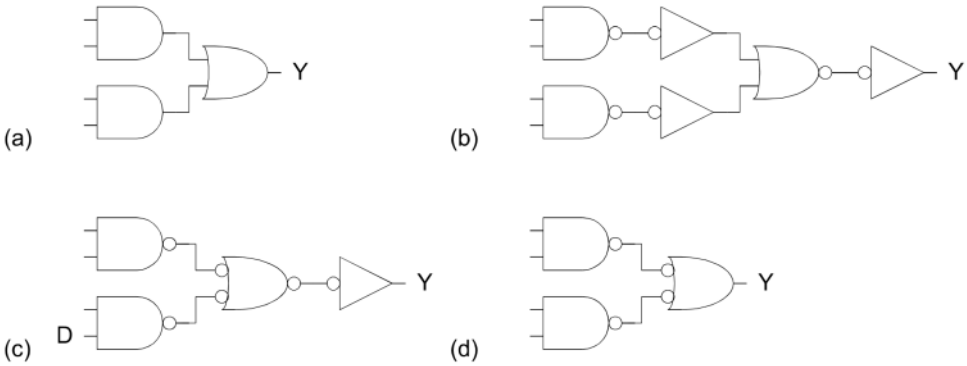
2) Sketch a design using NAND, NOR, and NOT gates.
Assume ~S is available.



Bubble Pushing

- Start with network of AND / OR gates
- Convert to NAND / NOR + inverters
- Push bubbles around to simplify logic
  - Remember DeMorgan's Law





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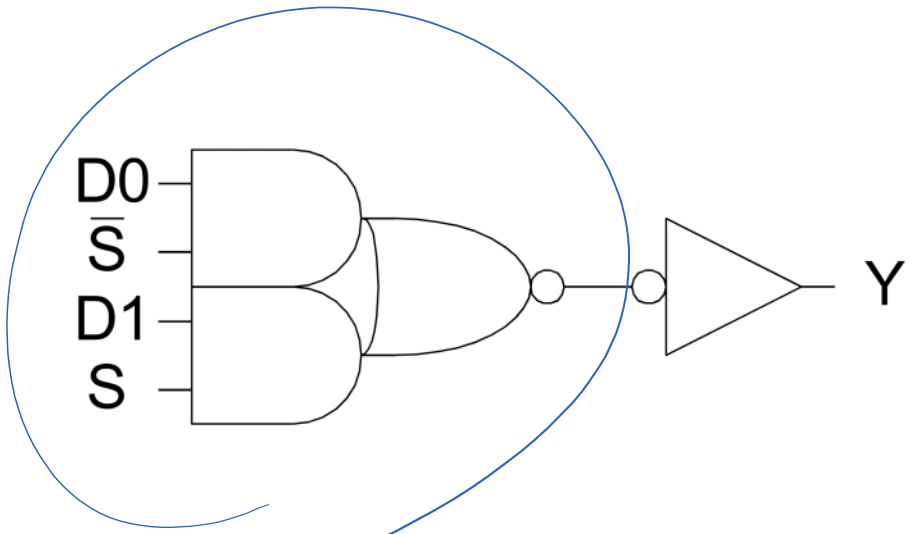
Example 3

3) Sketch a design using one compound gate and one NOT gate. Assume ~S is available.



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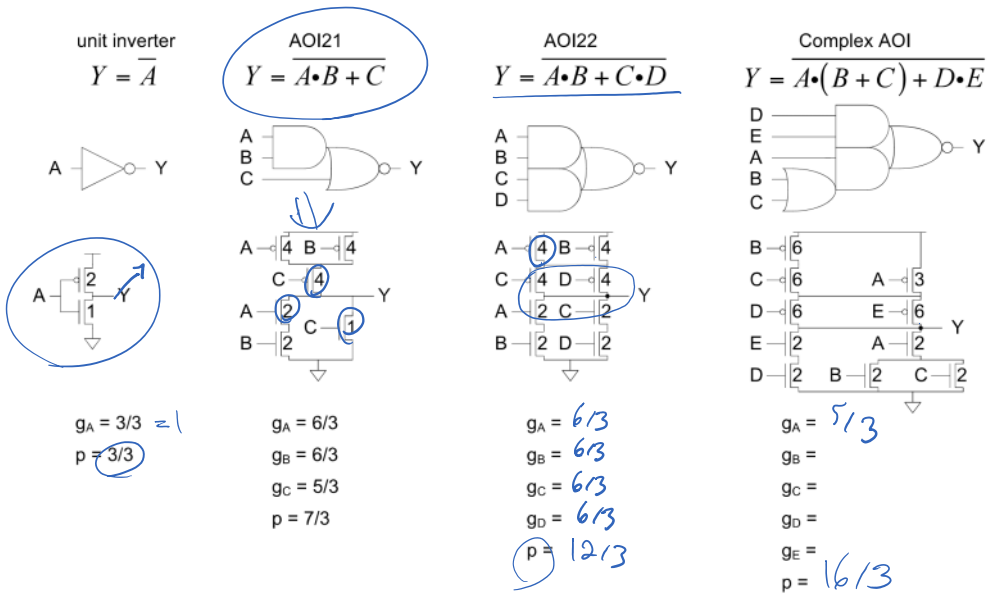
Compound Gates

- Logical Effort of compound gates



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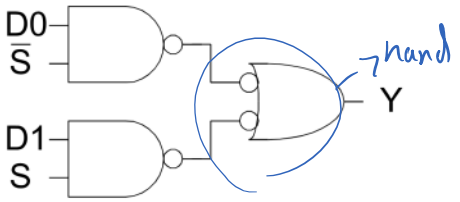
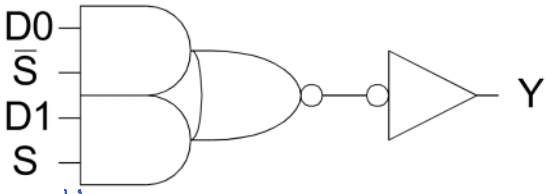
Example 4

- The multiplexer has a maximum input capacitance of 16 units on each input. It must drive a load of 160 units. Estimate the delay of the two designs.

H = 160/16 = 10 B = 1 N = 1



P = 2
G = 4/3
F = $B \cdot G \cdot H = 1 \cdot \frac{4}{3} \cdot 10 = \frac{40}{3}$
$\hat{f}$ = $F^{1/N} = 40/3$
D = $N\hat{f} + P = 1 \cdot \frac{40}{3} + 2 = \frac{46}{3}$



P = 4
G = 2
F = 1 · 2 · 10 = 20
$\hat{f}$ = 20
D = 1 · 20 + 4 = 24 (3RC)

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$\frac{46}{3}(3)RC = 46RC$ 72RC

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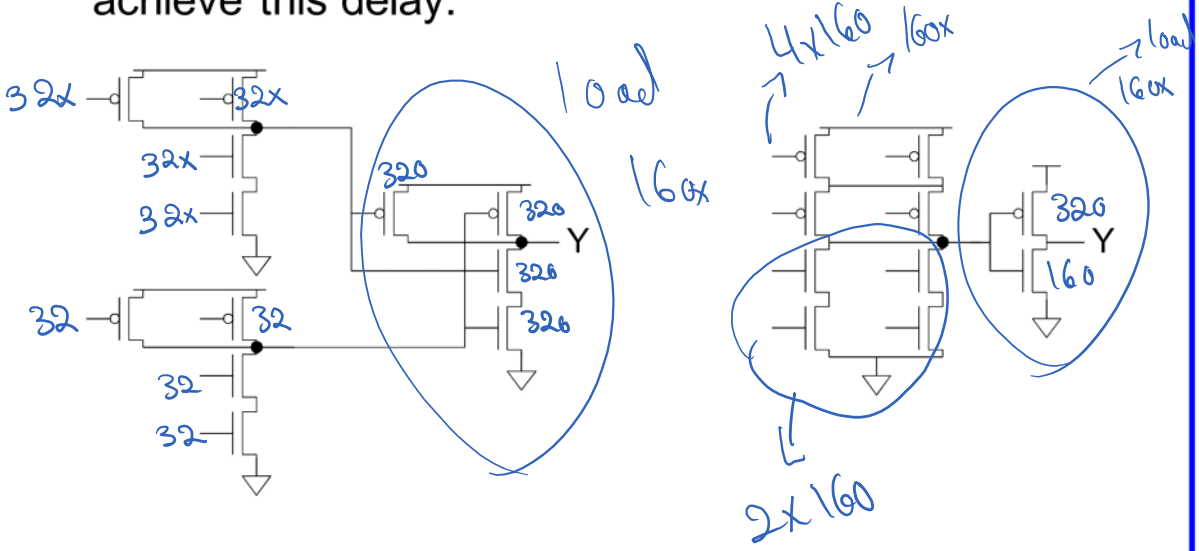
input = 16x load = 160x

Example 5

- Annotate your designs with transistor sizes that achieve this delay.



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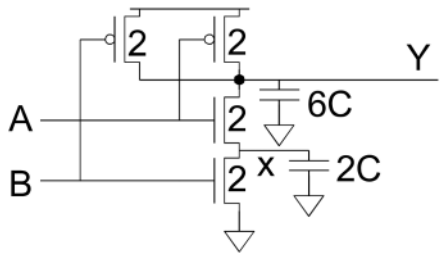
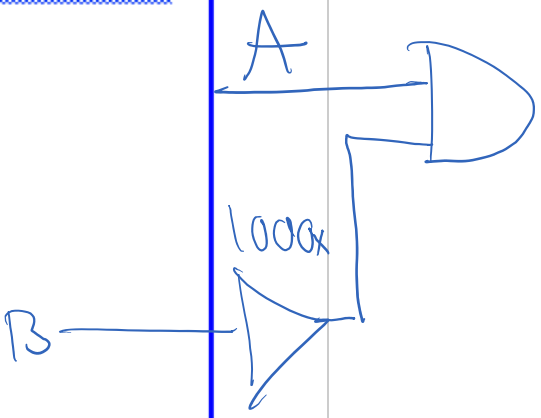
Input Order

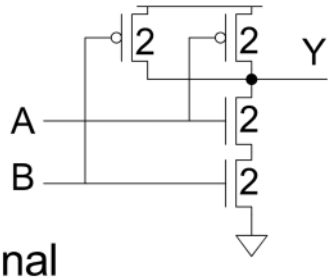
- Our parasitic delay model was too simple
  - Calculate parasitic delay for Y falling
    - If A arrives latest?
    - If B arrives latest?





Inner & Outer Inputs

- *Inner* input is closest to output (A)
- *Outer* input is closest to rail (B)



- If input arrival time is known
  - Connect latest input to inner terminal

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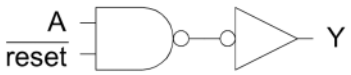
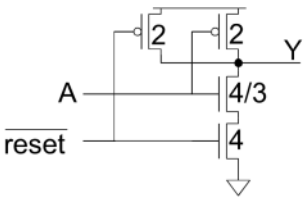
Asymmetric Gates

- Asymmetric gates favor one input over another
- Ex: suppose input A of a NAND gate is most critical
  - Use smaller transistor on A (less capacitance)
  - Boost size of noncritical input
  - So total resistance is same



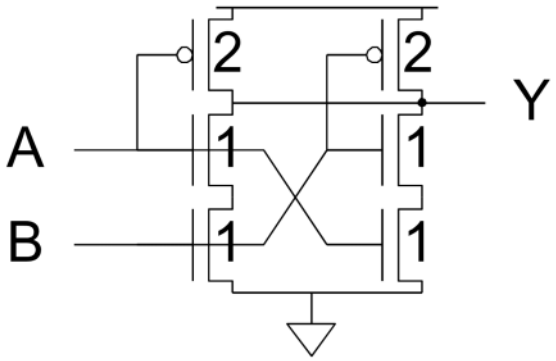
- g_A =
- g_B =
- $g_{total} = g_A + g_B$ =



- Asymmetric gate approaches g = 1 on critical input
- But total logical effort goes up

Symmetric Gates

- Inputs can be made perfectly symmetric



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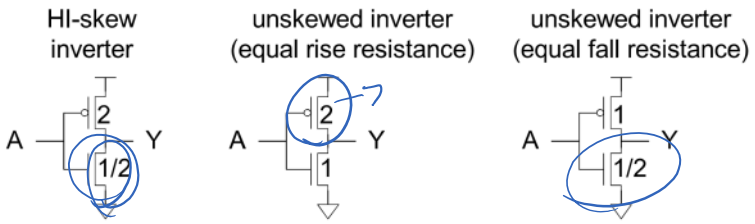
Skewed Gates

- Skewed gates favor one edge over another
- Ex: suppose rising output of inverter is most critical
  - Downsize noncritical nMOS transistor



- Calculate logical effort by comparing to unskewed inverter with same effective resistance on that edge.
  - g_u = 3/3=1
  - g_d = 2+1/2=2.5/1.5

HI- and LO-Skew

- Def: Logical effort of a skewed gate for a particular transition is the ratio of the input capacitance of that gate to the input capacitance of an unskewed inverter delivering the same output current for the same transition.

- Skewed gates reduce size of noncritical transistors
  - HI-skew gates favor rising output (small nMOS)
  - LO-skew gates favor falling output (small pMOS)
- Logical effort is smaller for favored direction
- But larger for the other direction

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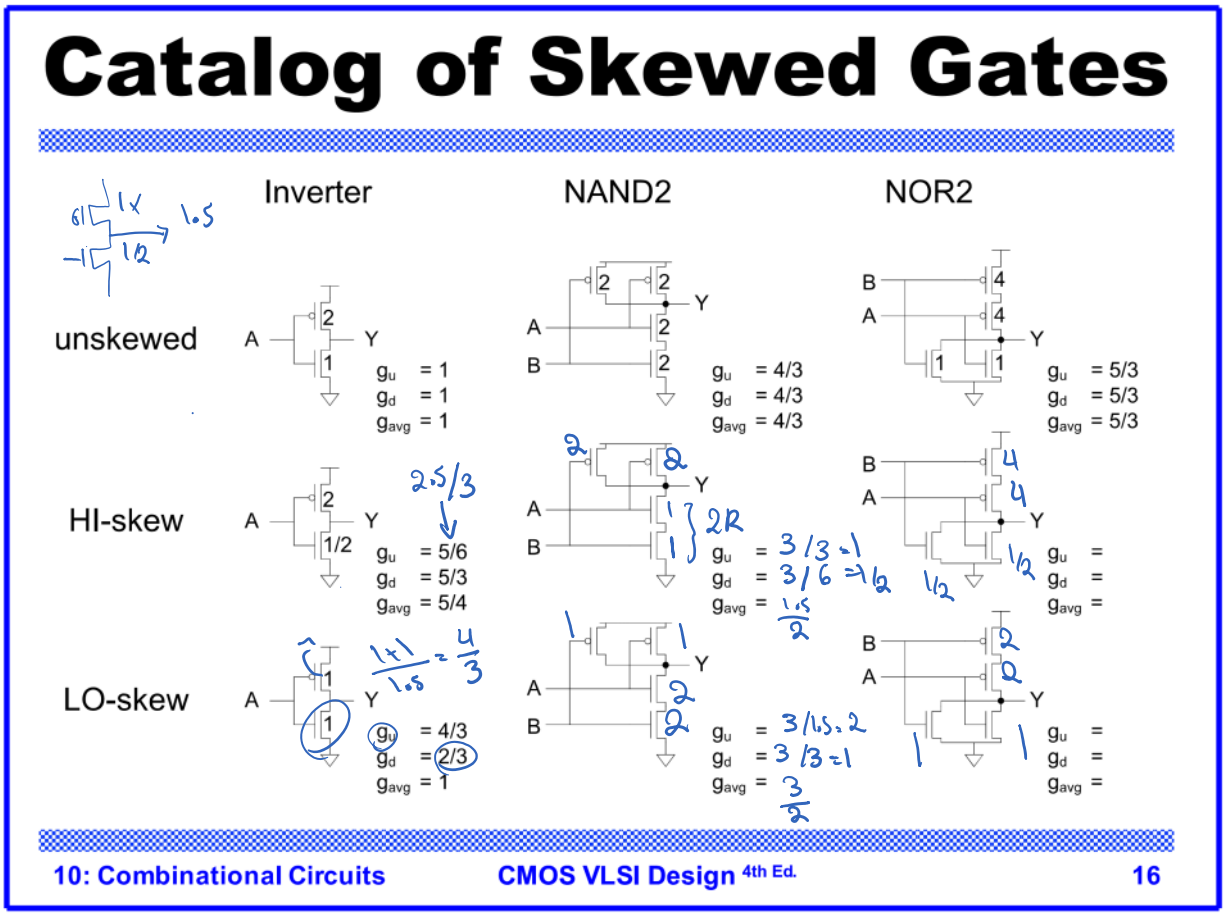
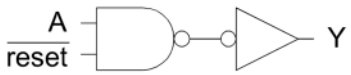
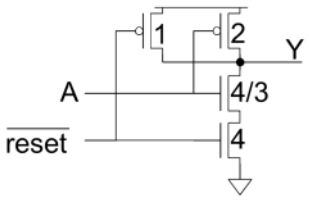
Catalog of Skewed Gates



Asymmetric Skew

- Combine asymmetric and skewed gates
  - Downsize noncritical transistor on unimportant input
  - Reduces parasitic delay for critical input





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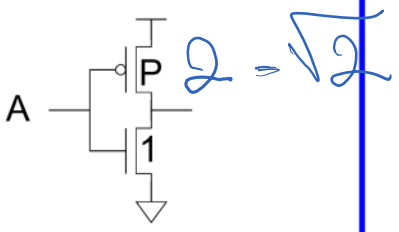
Best P/N Ratio

- We have selected P/N ratio for unit rise and fall resistance (μ = 2-3 for an inverter).
- Alternative: choose ratio for least average delay
- Ex: inverter
  - Delay driving identical inverter
  - t_{pdf} =
  - t_{pdr} =
  - t_{pd} =
  - dt_{pd} / dP =
  - Least delay for P =



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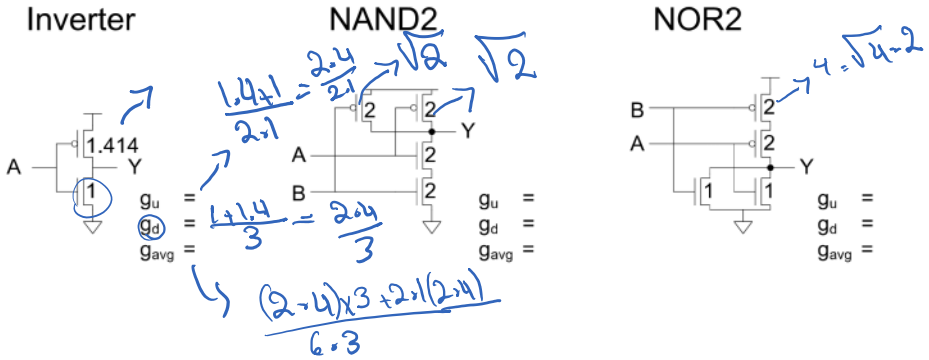
P/N Ratios

- In general, best P/N ratio is sqrt of equal delay ratio.
  - Only improves average delay slightly for inverters
  - But significantly decreases area and power

fastest P/N ratio



Observations

- For speed:
  - NAND vs. NOR
  - Many simple stages vs. fewer high fan-in stages
  - Latest-arriving input
- For area and power:
  - Many simple stages vs. fewer high fan-in stages