

## CPEG660-Project 2 Part 3-Block Layout

Qianzi Yan

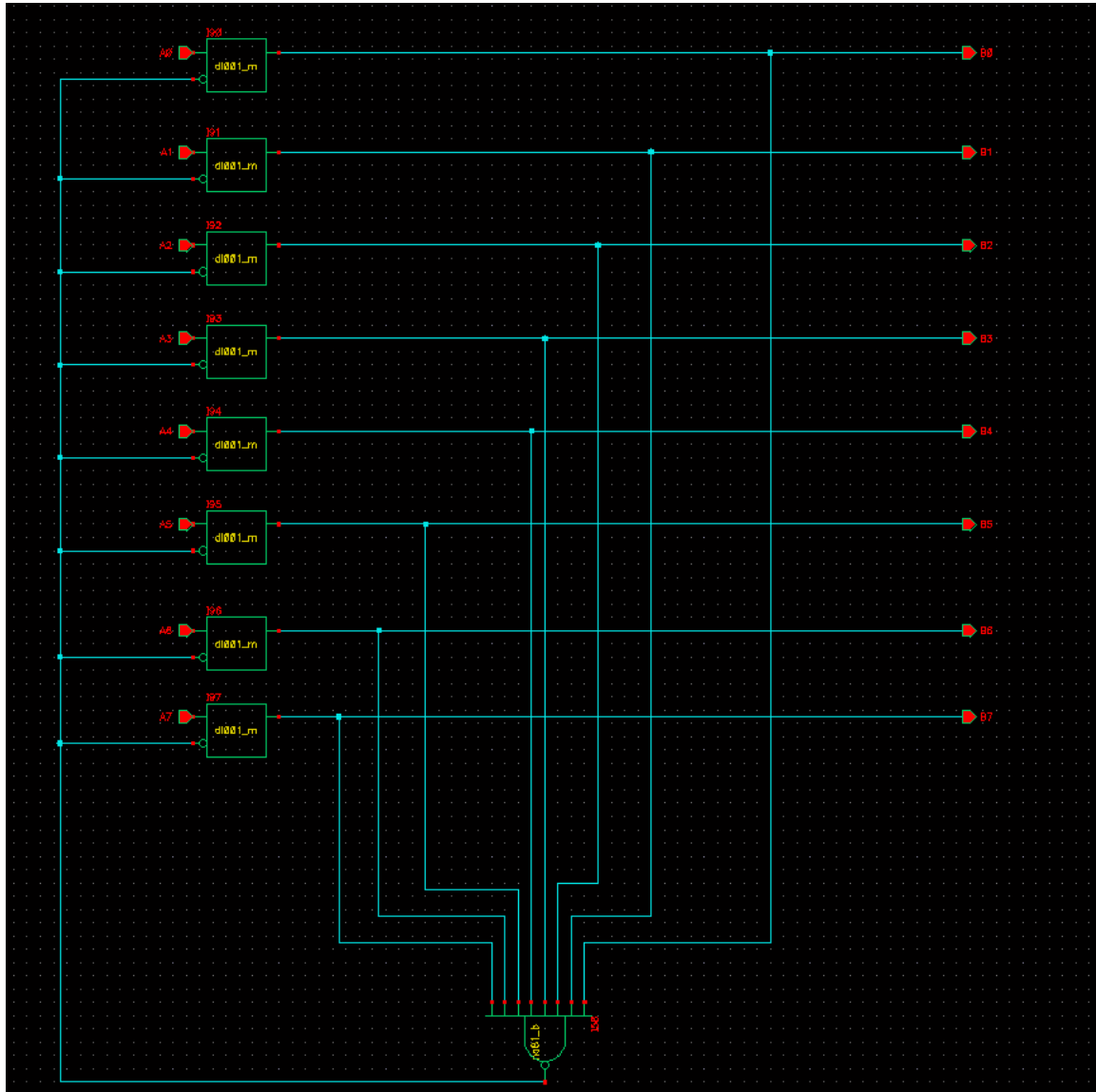
Wangqing Shen

Xiwei Zhang

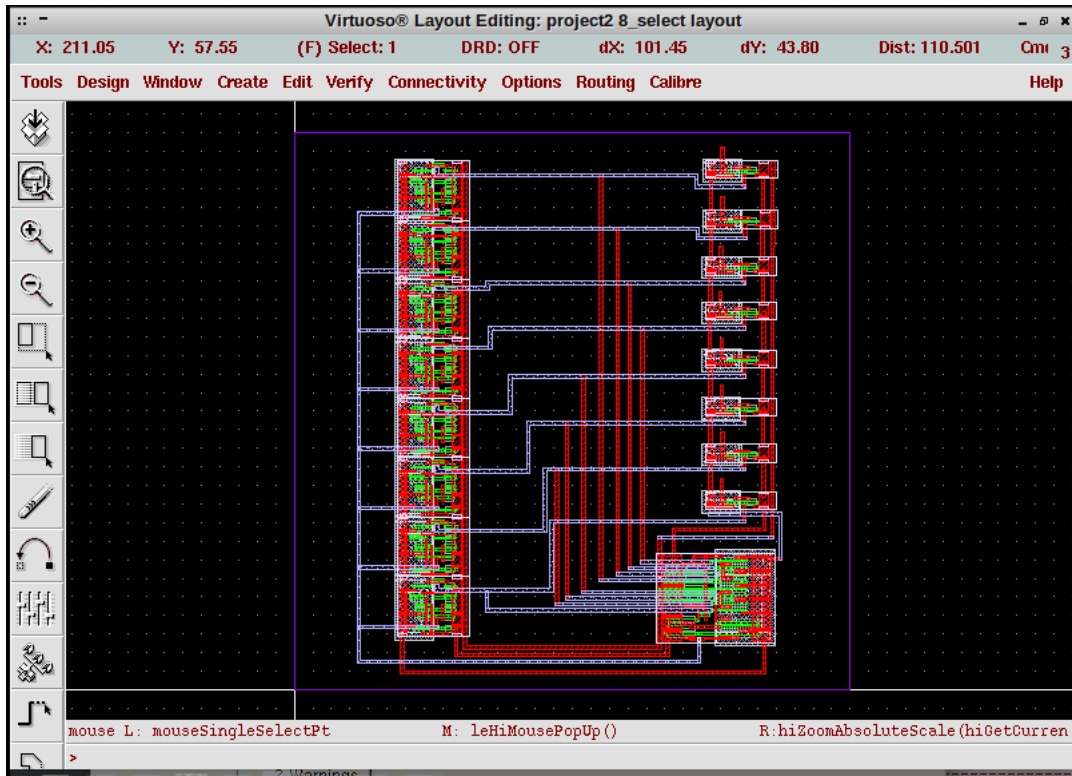
12/01/2015

Layout of each part

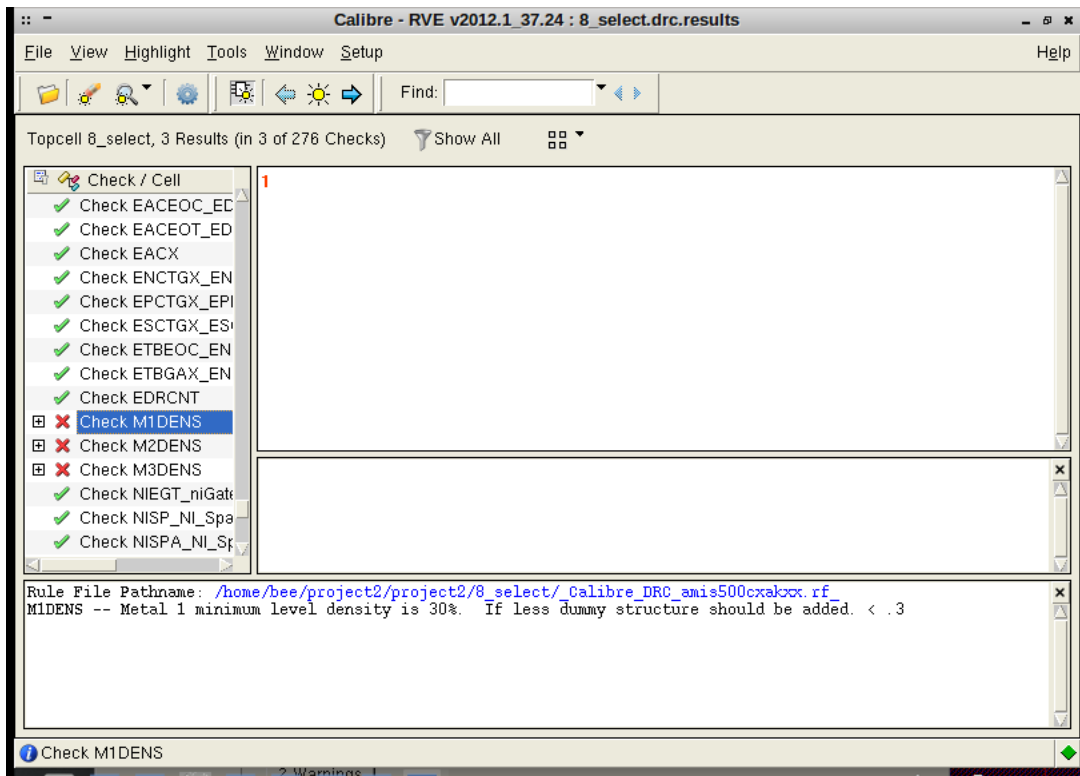
(i) schematic:



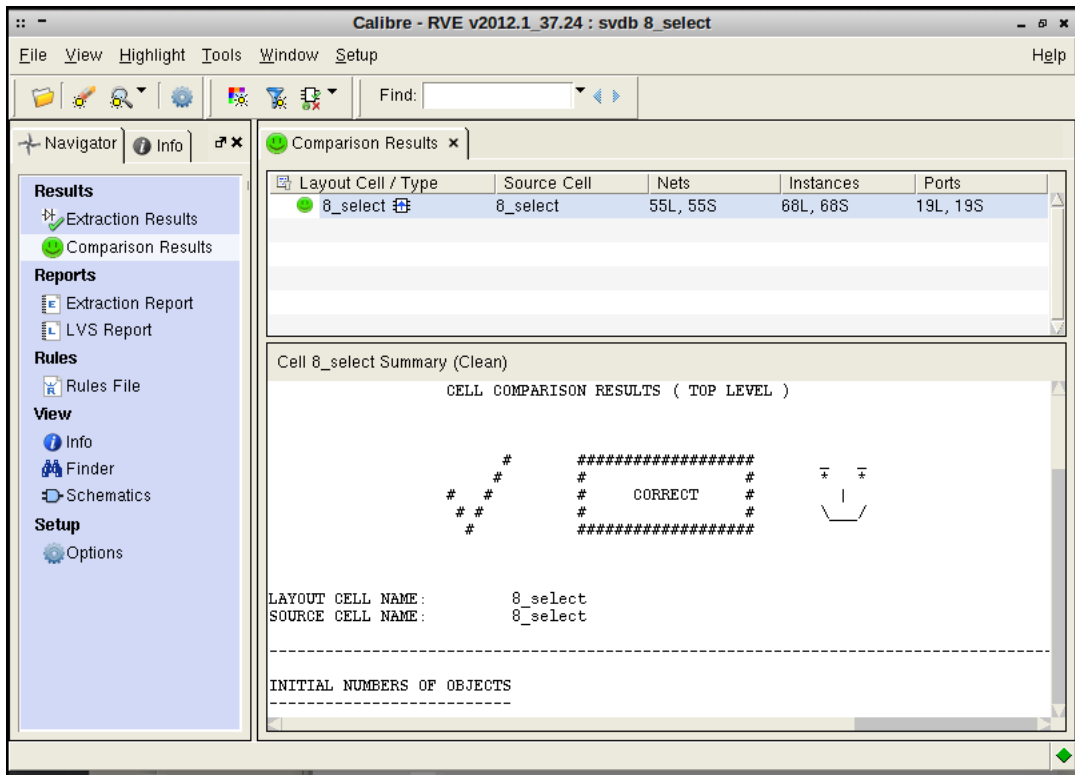
Layout:



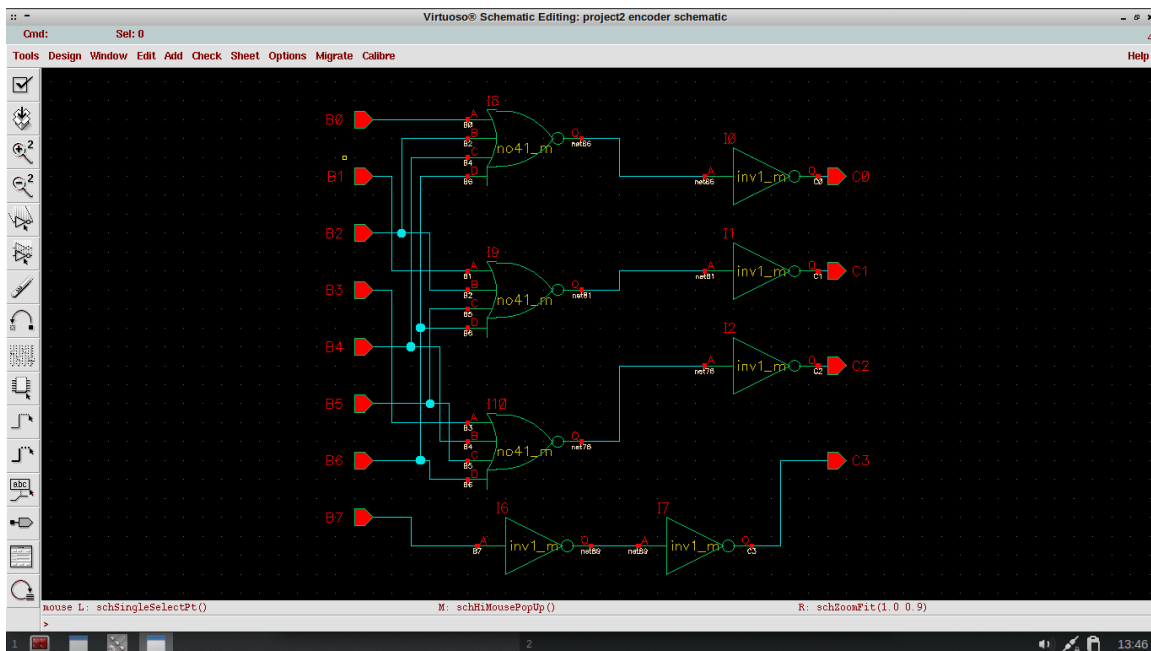
DRC:



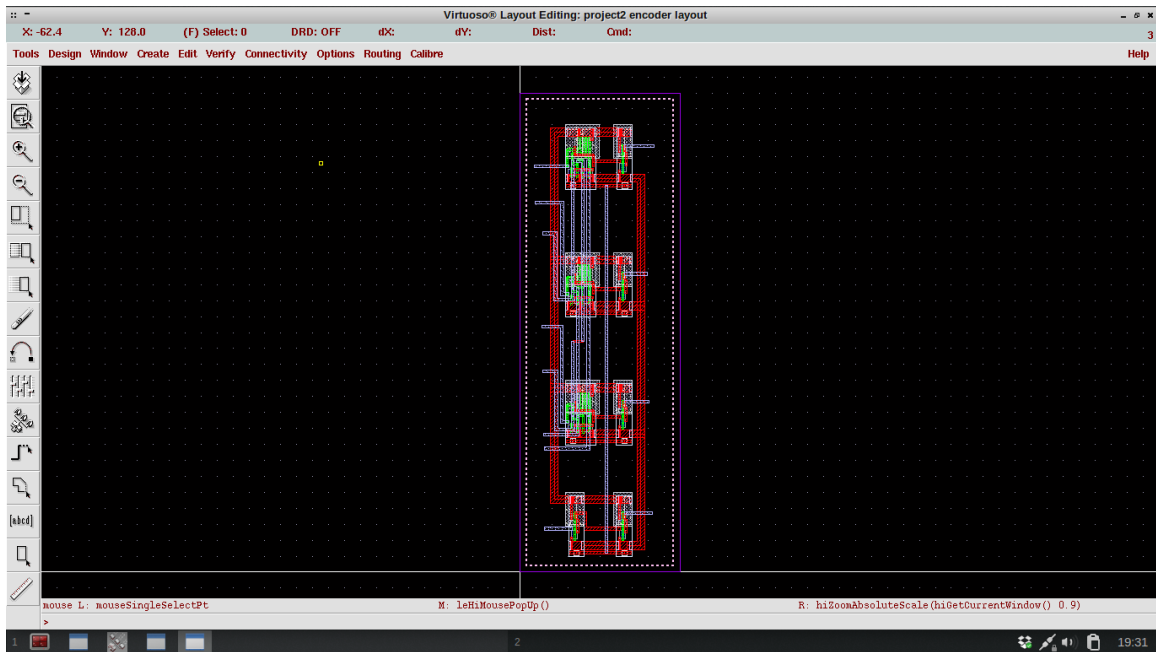
LVS:



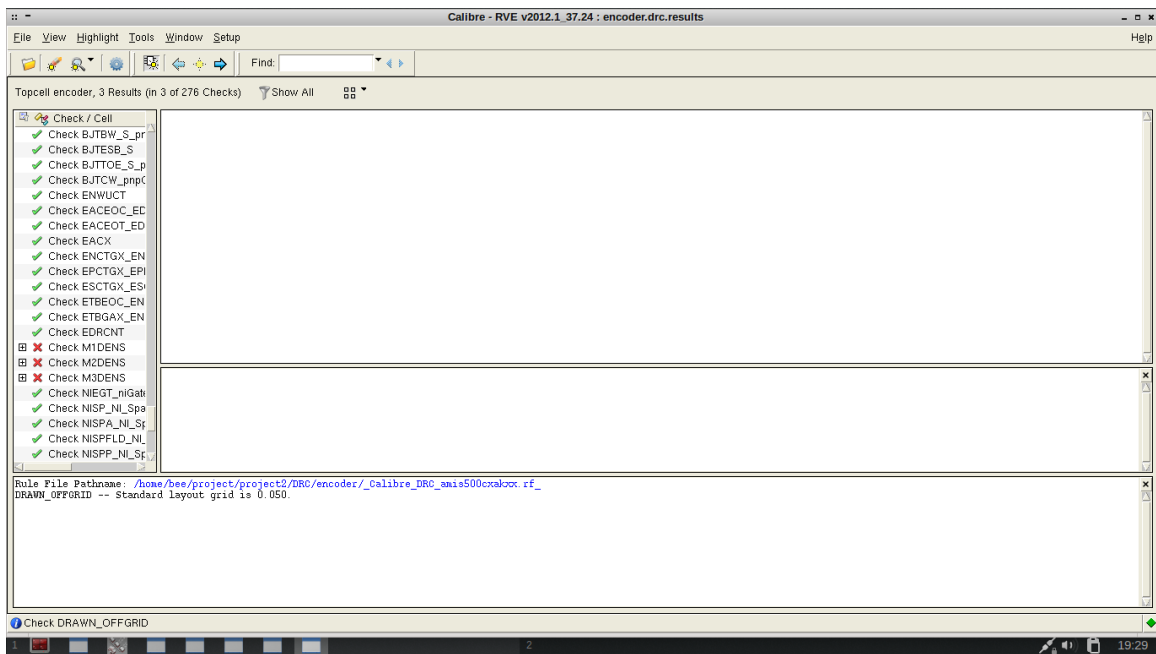
(ii) Schematic:



## Layout:



## DRC:



## LVS:

The screenshot shows the Calibre RVE v2012.1 37.24 : svdb encoder interface. The main window displays the 'Comparison Results' tab, which includes a table of layout cells and a detailed comparison summary for the 'encoder' cell.

Layout Cell / Type	Source Cell	Nets	Instances	Ports
encoder	encoder	18L, 18S	7L, 7S	15L, 15S

Cell encoder Summary (Clean)

CELL COMPARISON RESULTS ( TOP LEVEL )

#####  
# CORRECT #  
#####

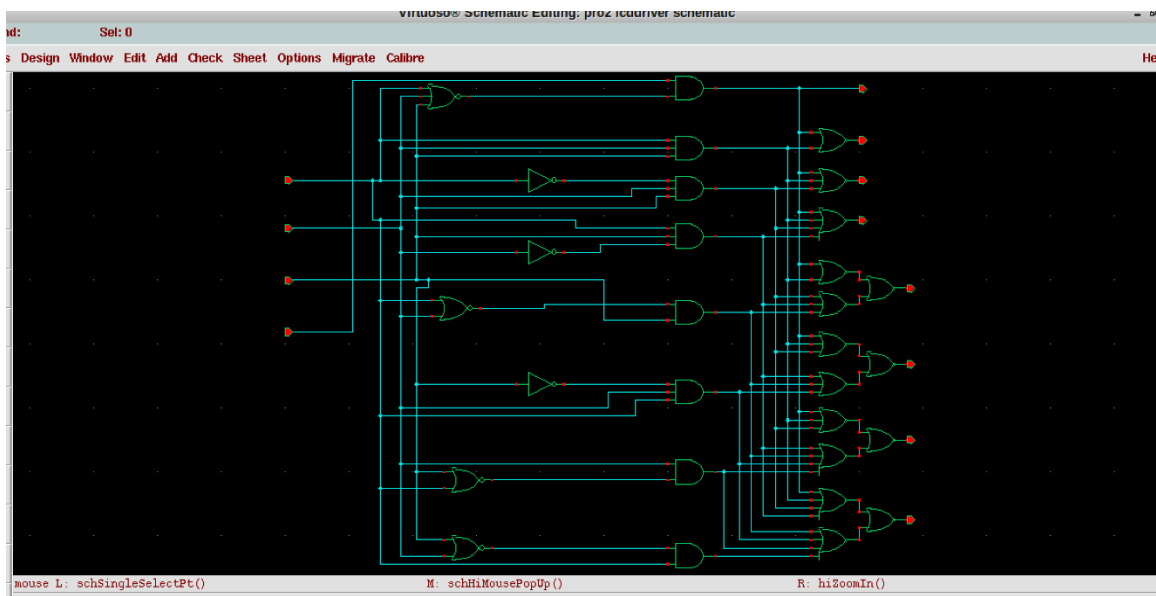
LAYOUT CELL NAME: encoder  
SOURCE CELL NAME: encoder

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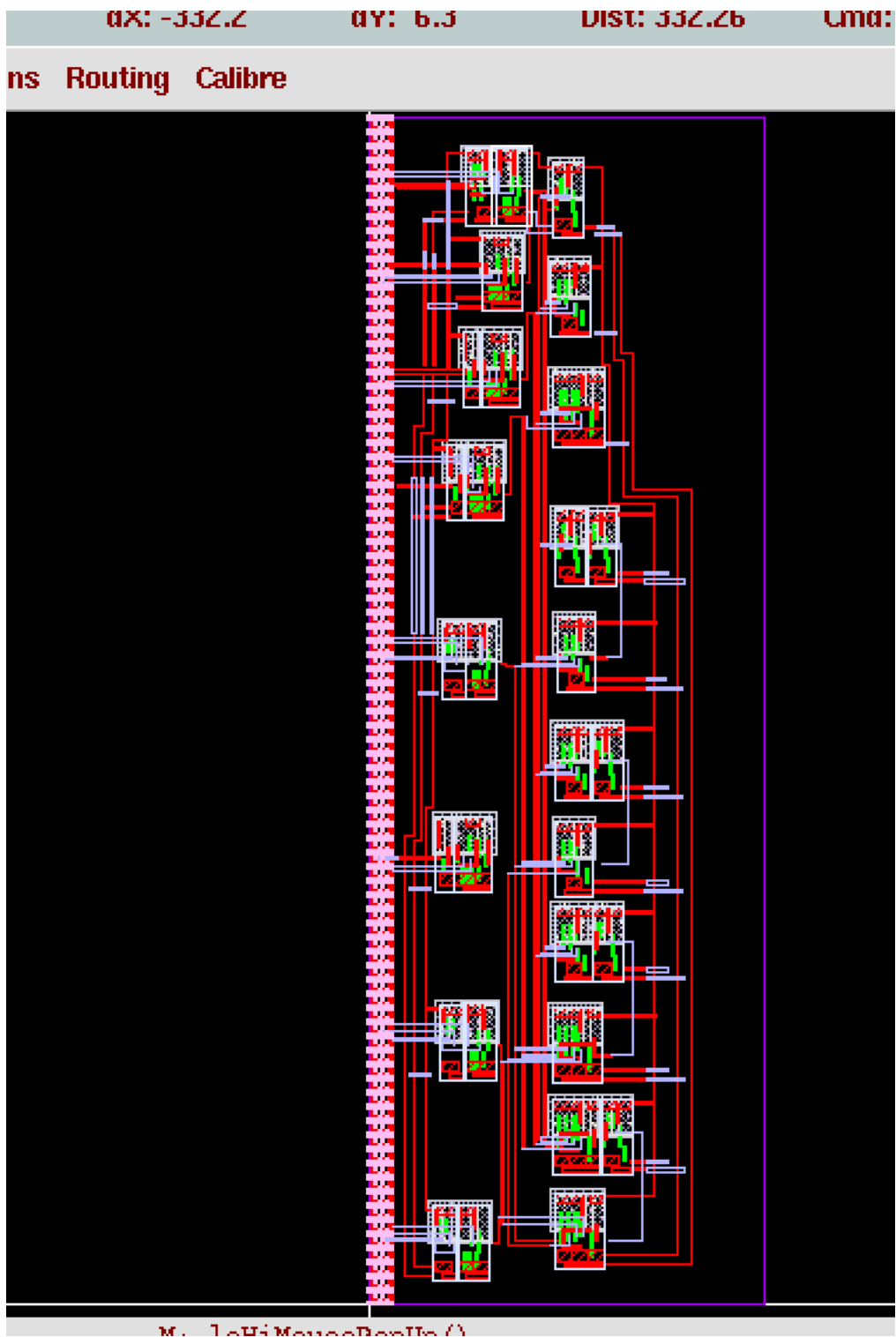
INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	15	15	
Nets:	28	28	
Instances:	17	17	MM (4 pins) MP (4 pins)

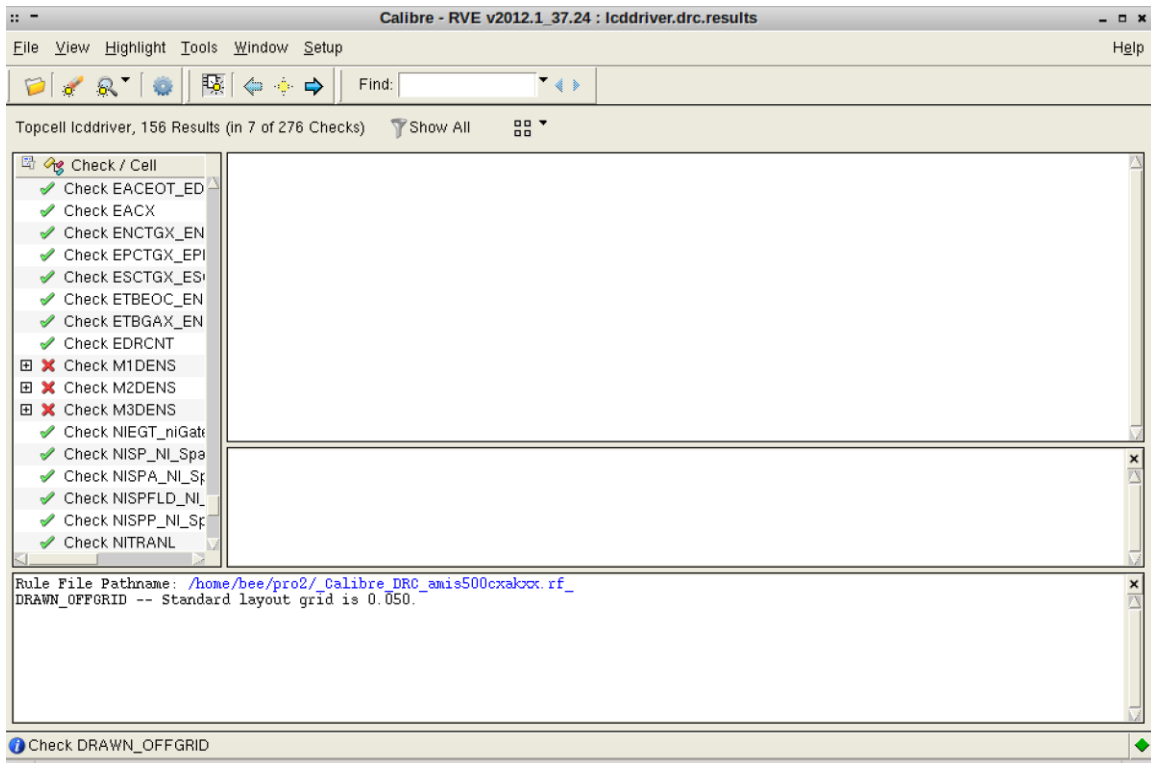
## (iii) Schematic:



Layout:



## DRC:



## LVS:

