CPEG460 VLSI Project 2

The final project is a chance for you to apply your new skills in VLSI design to a moderate sized problem of your choosing as part of a team. You should begin thinking about a project and teammate(s) right away. Your project has the following milestones:

1. Project Proposal Due - Nov. 7th on canvas
2. Schematic and Simulation Due - Nov. 14th (in class presentation and on canvas)
3. Block Layout Due - Nov. 21st (in class presentation and on canvas)
4. Nothing Due (thanksgiving break) - Nov. 25-29
5. Final Project Report - Dec. 5th (in class presentation and on canvas)

Your project must fit on a 1.5 x 1.5 mm 40-pin MOSIS “Tiny Chip”. The core of your project must fit in a 1.1mm x 1.1mm box and have exactly 40 pins. Three pins should be dedicated to VDD and three to GND, so only 34 are available as I/Os. A pad frame will be provided for your use.

Be creative when selecting your project. Your project should be bigger than a weekly lab assignment, but small enough to be doable. If in doubt, err on the side of smaller; you will receive a much better grade for a simple project that is completed and convincingly verified than a large project that is incomplete. Examples of suitable projects are listed below, but do not let the list limit your imagination!

1. High-speed adder
2. Floating point adder
3. Multiplier
4. Alarm clock
5. Encryption
6. SRAM
7. Digital-to-Analog converter
8. Stop-watch
9. LCD display driver
10. Serial-to-parallel converter
11. Parallel-to-serial converter

Deliverables

Your team is responsible for the following deliverables on the dates described above:

Project Proposal

A 2-page proposal describing what you plan to build. It must be specific enough that the instructor can determine when you demonstrate your project that it meets the specs of the proposal. The proposal should also include a table listing all the inputs, outputs, and bidirectional pins on the chip. It should include a floorplan, drawn to scale with dimensions labeled, indicating the top-level blocks. Examples can be found on canvas.

Schematic Checkoff

A presentation that will demonstrate the schematics are complete and simulate successfully. An example can be found on canvas

Block Layout

At this point, your leaf cell layouts should be complete. Pay attention to making clean and efficient layouts with no DRC or LVS errors. There will be a in class presentation that will show all the schematics and layouts and clean DRCs and LVS's. An example can be found on canvas.

Chip Layout

Demonstrate a complete layout fully routed to a pad frame. Use fat power wires were appropriate. Show that the chip passes DRC and LVS. Note that LVS does not understand the sizes of the I/O transistors in the pad frame, so check sizes in the core but not at the chip level. Show that the schematics (including the pad frame) still simulate correctly.

Final Project Report

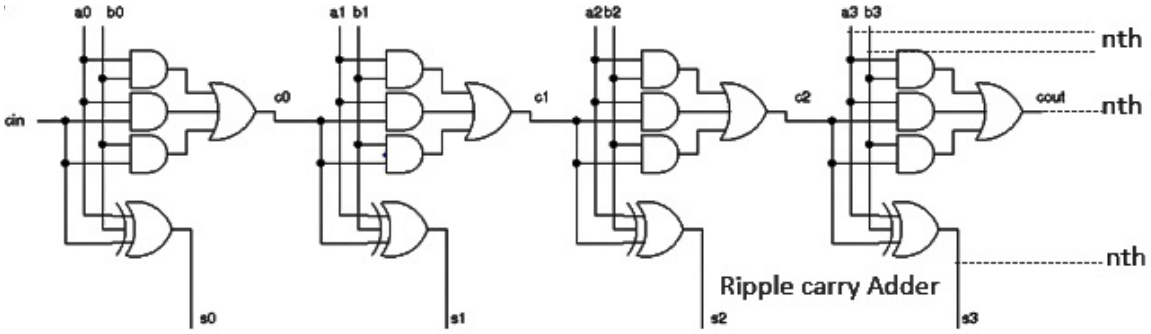
Your final report should provide all the information another engineer would need to know to understand and test your chip after fabrication. The following content is recommended:

- Cover page
  - Project title, designers, and a chip plot
- Introduction
  - A brief high-level description of the chip function and the manufacturing process
- Specifications
  - Table of inputs, outputs indicating name, direction, bus widths
  - Theory of operation of the chip relating the outputs to the inputs
- Floorplan
  - Compare the actual floorplan to the proposal and explain discrepancies
  - Slice plan for data path(s)
  - Pinout diagram indicating names and pin numbers for each pin
- Verification
  - Do schematics pass test bench?
  - Does layout pass DRC and LVS?
  - If the chip contains any analog blocks, show the HSPICE simulations
  - Explain any discrepancies or concerns
- Post-fabrication test plan
  - How will the chip be tested if it is fabricated? This needs to be as detailed as possible
- Design Time
  - Summary of design time spent on each component of the project

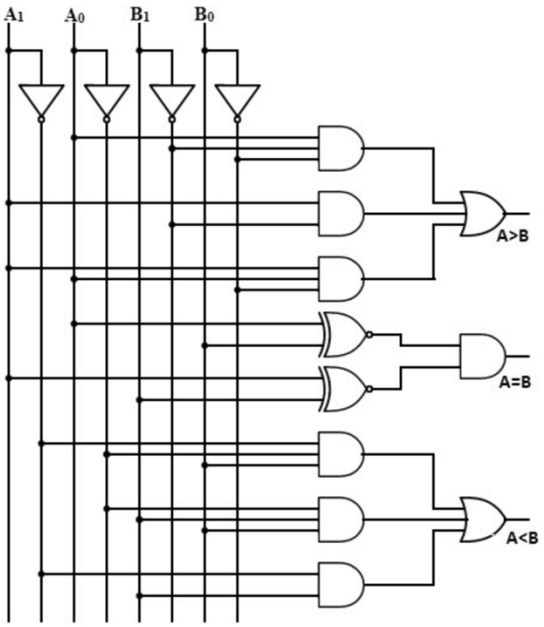
An example of the final report can be found on sakai.

Some detailed examples

1. Carry-ripple adder



2. Comparator



3. Multiplier

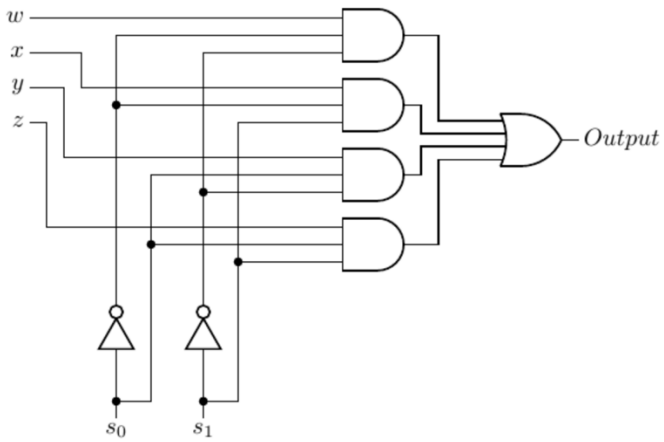
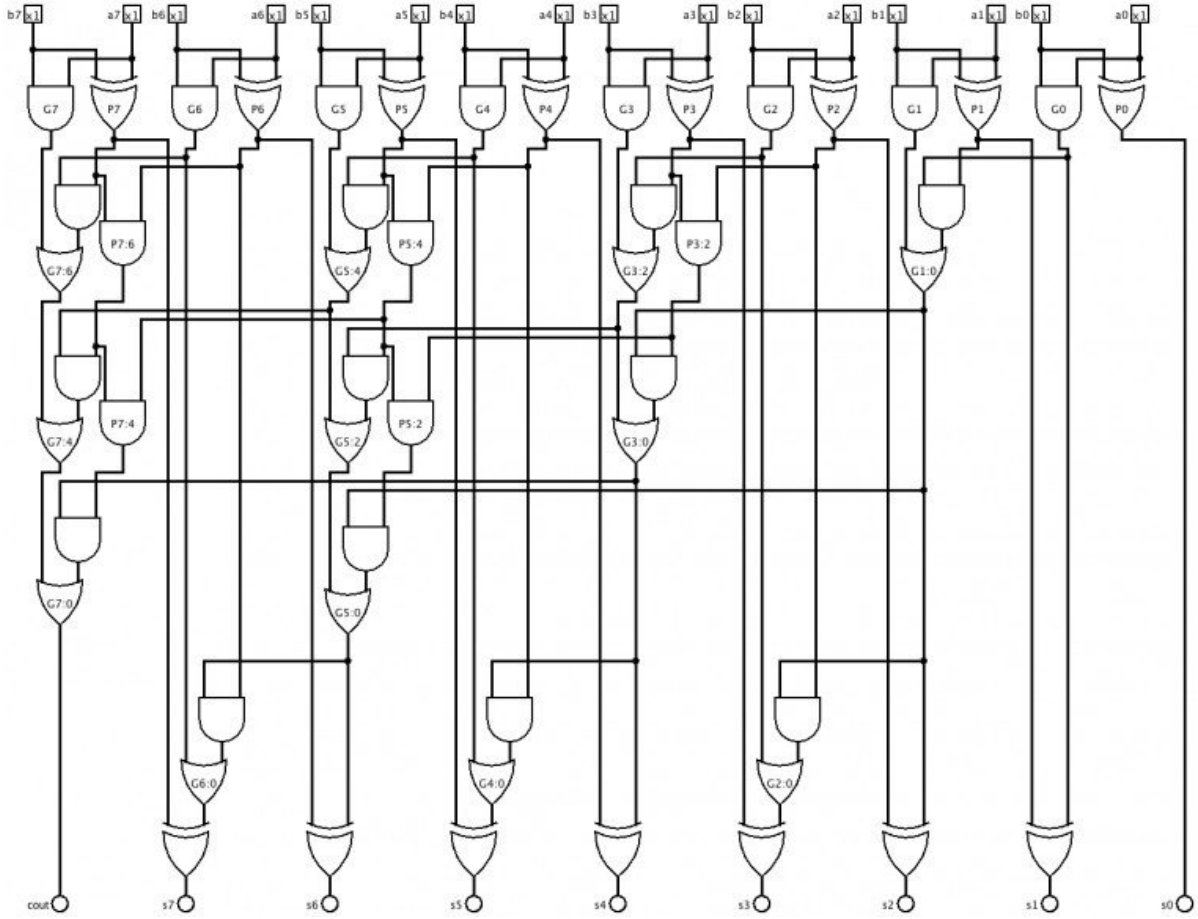
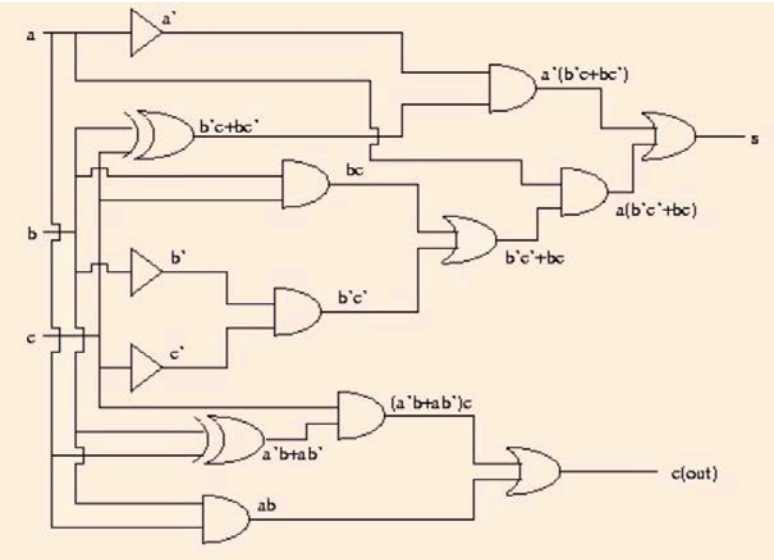


Figure 5.9: A 4-way multiplexer.

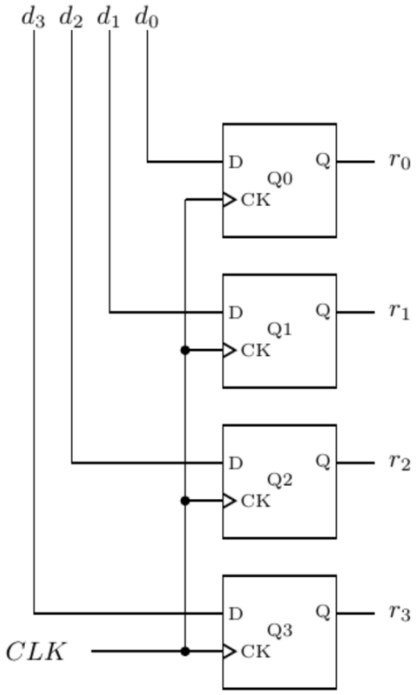
4. Calculator



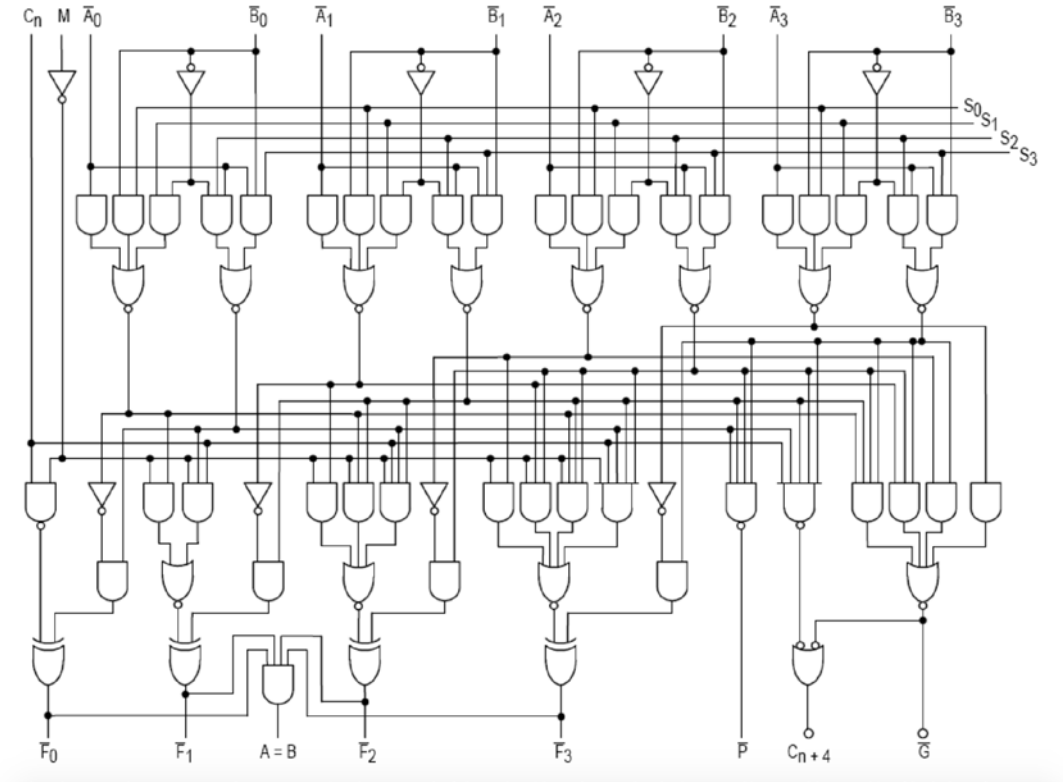
5. Full adder



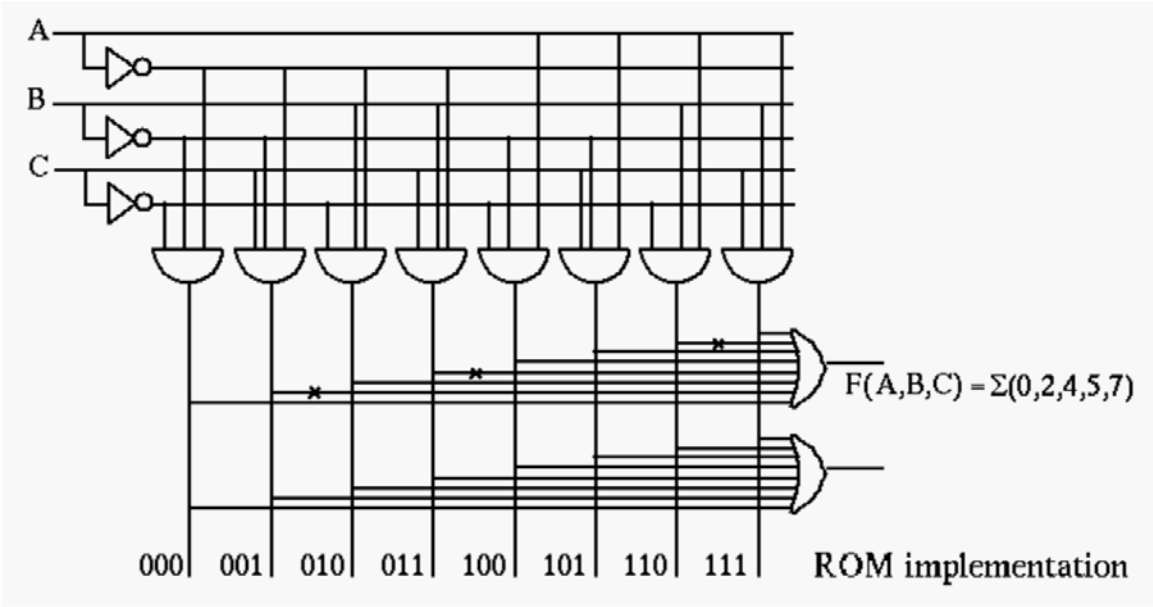
6. 4-bit register



7. Four-bit ALU



8. ROM


A
B
C
F(A,B,C) = Σ(0,2,4,5,7)
000
001
010
011
100
101
110
111
ROM implementation