CPEG 422 Project 4
Matrix multiplication

During this project, you will implement matrix multiplication that is commonly used in signal processing and machine learning. You will implement matrix multiplication in both software and hardware, and make a comparison between software and hardware implementations.

Goals of this project:

Learn how to write scalable VHDL code
Learn to do software and hardware co-design
Learn to build embedded systems

Your tasks:

Task1: Implement **n** x **n** matrix multiplication (for any given **n**) purely in software (c code). (20%)

Task2: Implement a 3x3 matrix multiplication in hardware (FPGA). (15%)

Task3: Increase the matrix size in task2, find the maximum matrix size (**N** x **N**) that can be done in parallel on the FPGA. (20%)

Task4: Compare the running time of software and hardware implementations for the same matrices. Suppose N × N is the maximum size of matrix you find in Task 3. You need to compare N different cases, ranging from 1 x 1 to N x N. Find the exact point that the hardware starts to outperform software. (20%)

Task5: Finally, submit your project report, report the amount of speed up achieved by the FPGA. (25%)

Minimal Hardware and Toolkit:

Vivado 2017.4 (For hardware IP and block design)
Zybo Z7-10 (For implementing block design and implementing communication system)
Xillinx SDK (For software control on processor side)
Serial terminal (For observing communication between the processor and the FPGA)

Matrix Multiplication:

Assume both A and B are **n × n** matrices. The multiplication result of A and B, C = AxB, is also a **n × n** matrix, defined below:

$$C=\begin{bmatrix} c_{11} & \cdots & c_{1n} \\ \vdots & \ddots & \vdots \\ c_{n1} & \cdots & c_{nn} \end{bmatrix}, c_{ij} = \sum_{k=1}^{n} a_{ik} b_{kj}$$

In this project, each element of A and B is 16-bit long, while each element of C is 32-bit long. The Multiply-Accumulate (MAC) unit can be used as the basic function unit to implement matrix multiplication. FPGA usually utilizes DSP units to perform MAC operations. Specifically, the Zynq FPGA contains 80 slices of DSPs, and each slice contains 2 basic MAC units.

Implementation details:

- **Software implementation:**

1. In task 1, use a random function to generate integer values to construct A and B.
2. Print out the result C matrix. Make sure your results are correct.

- **Hardware implementation:**

1. The VHDL implementation can be RTL style (use operator '*' and '+').
2. The processor sends A and B to the FPGA. The FPGA computes C and sends it to the processor.
3. For task 2, A, B and C are 2 x 2 matrices. For tasks 3 and 4, matrices sizes are n x n, where n ranges from 1 to N (the maximum matrix size).
4. To implement and test your design, use the steps you learned in the previous project:
    1) Finish your matrix multiplication VHDL code and package the IP.
    2) Build a block design and generate bitstream.
    3) Use SDK to program the FPGA. Write a C code to send inputs and get outputs from FPGA.
    4) Observe the results on terminal and check the correctness.

- **Software vs. Hardware:**

1. You can use system call in c to collect the running time. When you collect hardware running time, make sure to include all set up time, data send and receive time.
2. Compare your software output and hardware output for error checking.

Questions: (submit your answer together with the report)

1. Please describe your ideas to make your VHDL code scalable for different matrix size. Here "scalable" means your matrix multiplication design can be easily changed for different size of n. (Hint: define some parameters)

2. Regarding the maximum matrix size (N x N) that can be done in parallel on the FPGA, please analyze all the possible hardware resource constraints. For each possible bottleneck you find, what is the limited maximum matrix size that can be held on FPGA? In your design, what is the most constrained bottleneck, and the maximum matrix size can be held in your design? (Hint: bottleneck types are related with resource category such as LUTs, DSPs, on-board block RAM size, I/O registers. Such information can be found in the manual. For each resource, show the constraint you find and compute the maximum matrix size based on it.)

Report requirements:

1. Design summary:
    1) Summarize how you implement your software multiplication.
    2) Summarize how you implement your hardware IP with high level code.
2. Result display:
    1) Briefly describe how your C program controls the FPGA and communicates with it for hardware implementation.
    2) Snapshot or paste your c code in different tasks.
    3) Discuss possible hardware implementation bottlenecks. Describe the bottleneck in your implementation. Based on the found bottleneck of your implementation, compute the maximum matrix size. Show your steps of computation and explain the reason.
    4) Make a comparison table and chart as well. Compare the running times of hardware implementation and software implementation, from size 1 to maximum.
3. Design implementation report: You only need to report the maximum matrix hardware case.

Summarize the block design implementation report offered in Vivado. Please report:

1) Hardware utilization of post-implementation (FF,IO ,LUT, BUF…) in table format.
2) Power report (dynamic vs. static, also signal, logic and I/O).
3) Timing report (critical path delay).
4) Design schematic snapshot.

4. Summarize hardware and software implementation. Based on your design experience, give pro and cons for hardware and software implementations and some guidance for system designers.

Grading criteria:

Specific requirements for your VHDL code:

- The code should be scalable, easily handle different matrix size with small changes.
- The code should be concise and no redundant logic and signals.

Specific requirements for your C code:

- Clear division of software implementation and hardware implementation.
- Collect running time in code.
- Results are easy to observe.
- Have result checking part.

Any of the following may account for deduction of your score:

- Incorrect/unexpected operation or function
- Unfamiliarity with any aspect of your project
- Late for your submission
- Inconsistent with implementation requirement
- Sloppy, undocumented program code

Due Dates:

Design source code submission:	May 18 at noon
In-class demo:	May 18
Project report:	May 20 at midnight