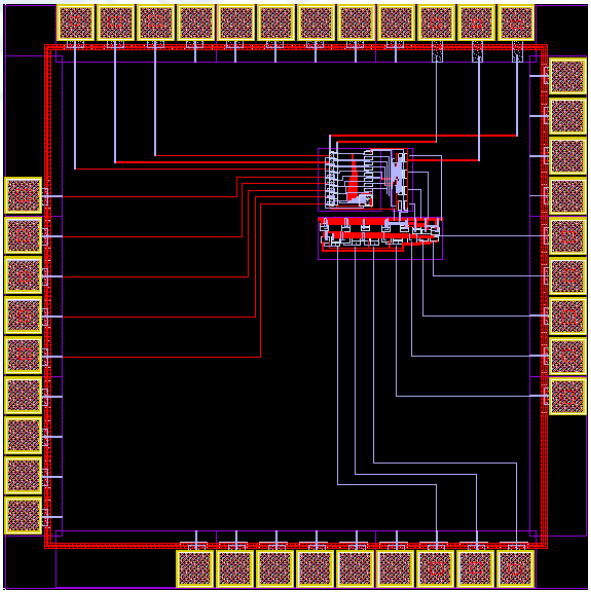
Competition Responder

CPEG 660 -- Introduction to VLSI systems --Project 2-Report

Instructor: Prof. Fouad Kiamilev



By Qianzi Yan

Wangqing Shen

Xiwei Zhang

12/10/2015

UNIVERSITY OF DELAWARE

1. Description

This system is designed for solving the problems in competition. Assume that eight competitors have to press a button to grab the chance to answer a given question. This system can recognize which one that presses answer button is the fastest.

2. Introduction

This system is combined by three parts. The first part is a select part, this part is using for recognize signals. When competitors begin to press answer button and give answer signals, this part can find the fastest signal, and pass the identity of the competitor to part2.

The second part is an encoder. Since we want to display the identity of the competitor who catches the answer chance, the encoder is designed for encoding the identity information of the competitor who catches the signal. The function of this part is transforming identity information to display part.

The third part is the display part. We design to use eight LED lights to show which competitor catches the answer signal. The number of the LED lights represent the identity of the competitor, which means the number of the competitor. The main theory of this part is decoding. Since in part 2, the system decodes the identity information of the competitor, the system should decode the code in order to get the information and could display the result.

3. Specification

(1) Table of inputs and outputs.

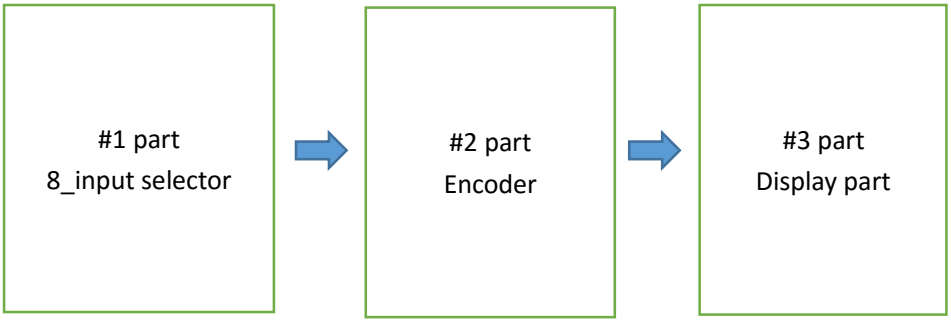
Type	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Definition	Inputs								Outputs							
Name	A0	A1	A2	A3	A4	A5	A6	A7	a	b	c	d	e	f	g	h

（2）Operation theory.

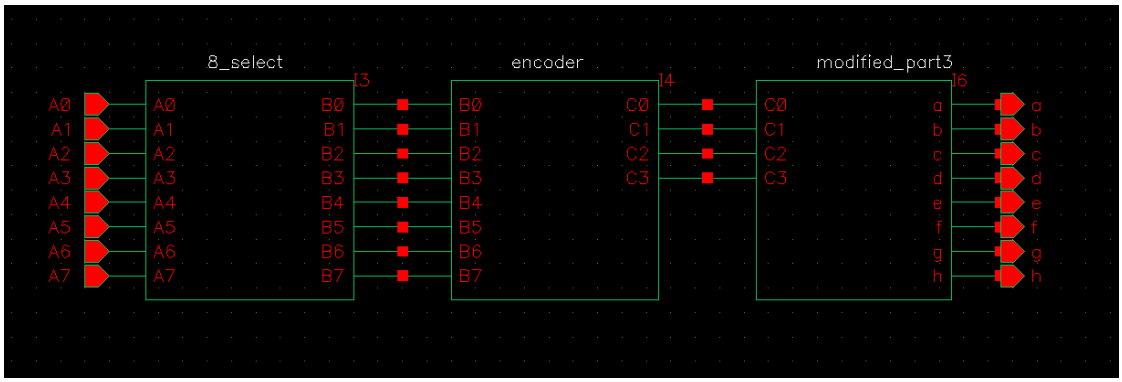
Eight inputs A0-A1 stand for eight competitors, when competitors are given answer signal, they begin to press the buttons which means given signal to A0-A1. System could recognize the fastest one who catch the signal. Outputs a-h stand for the number of the LED lights that respond to the inputs. If the A4 catch the signal, the output should be ‘e’ and there should be five LED lights be lighted.

4. Floorplan

(1) Floorplan in proposal.

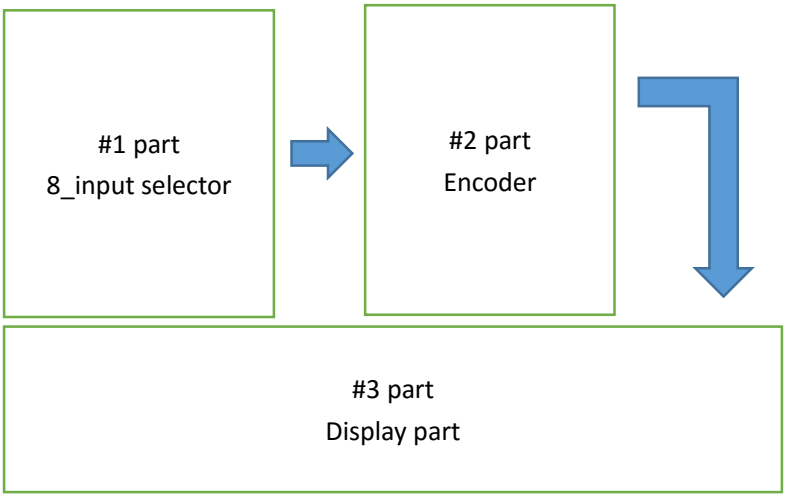


(2) Actual schematic (Total).

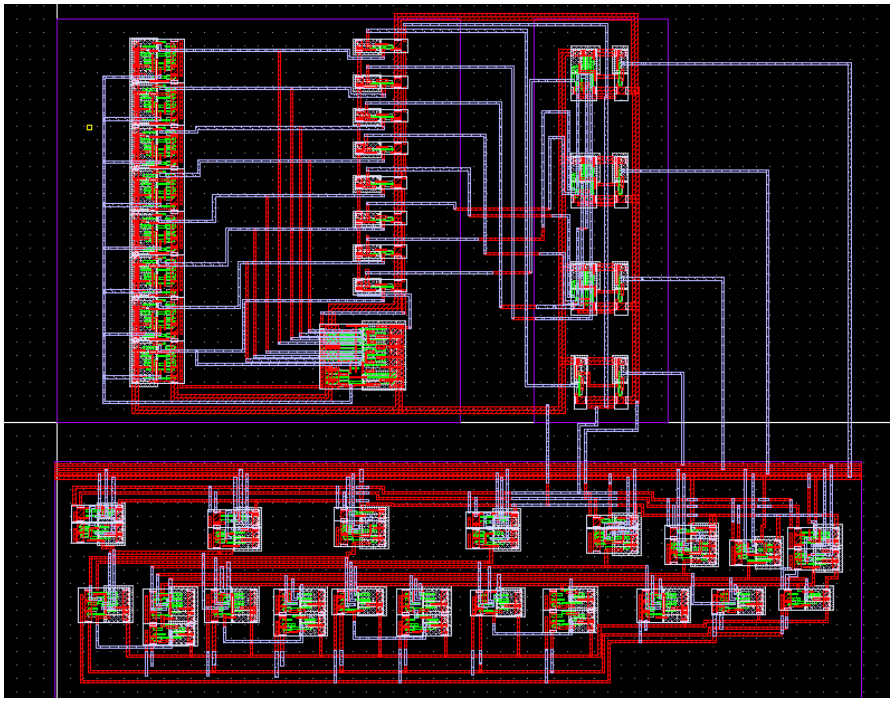


(3) Actual floorplan (Layout)

Floorplan:

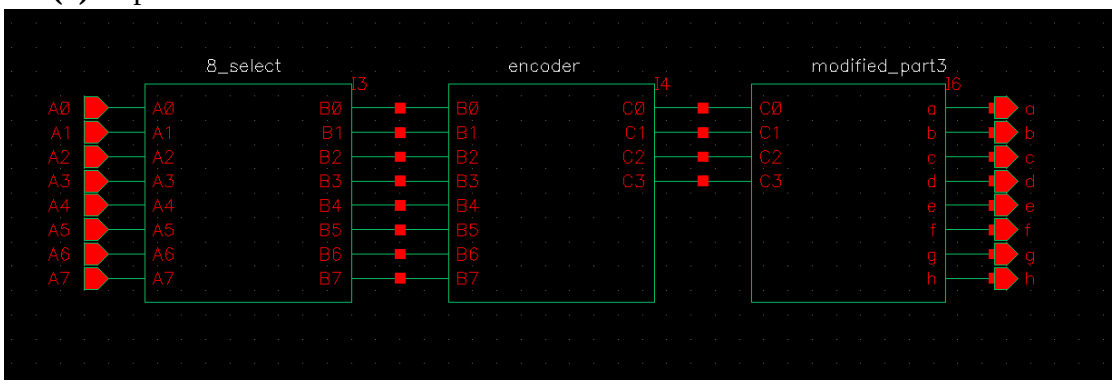


Actual layout:

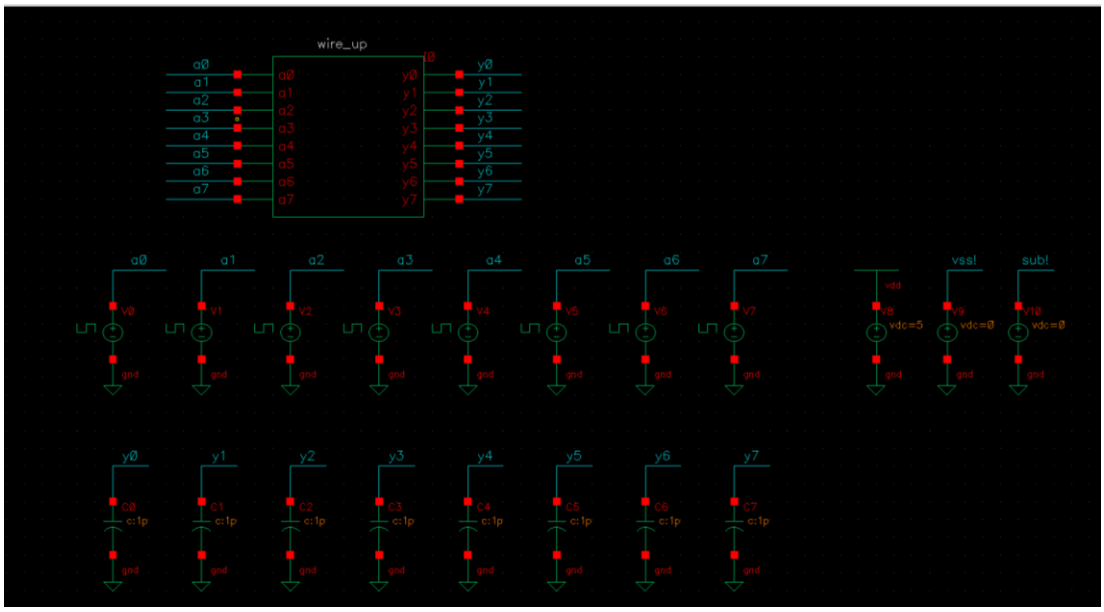


5. Verification

(1) Topcell schematic:



(2) Test bench Schematic:



Simulation result:

When given one input:

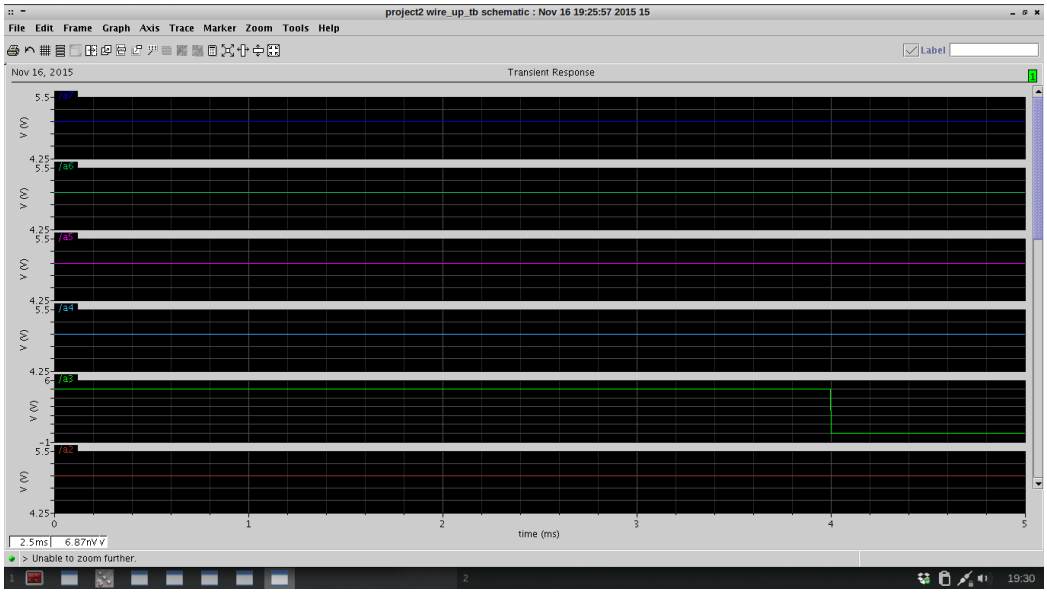
If a3=0, then four LED lights will be lighted. (Shown as the first figures below)

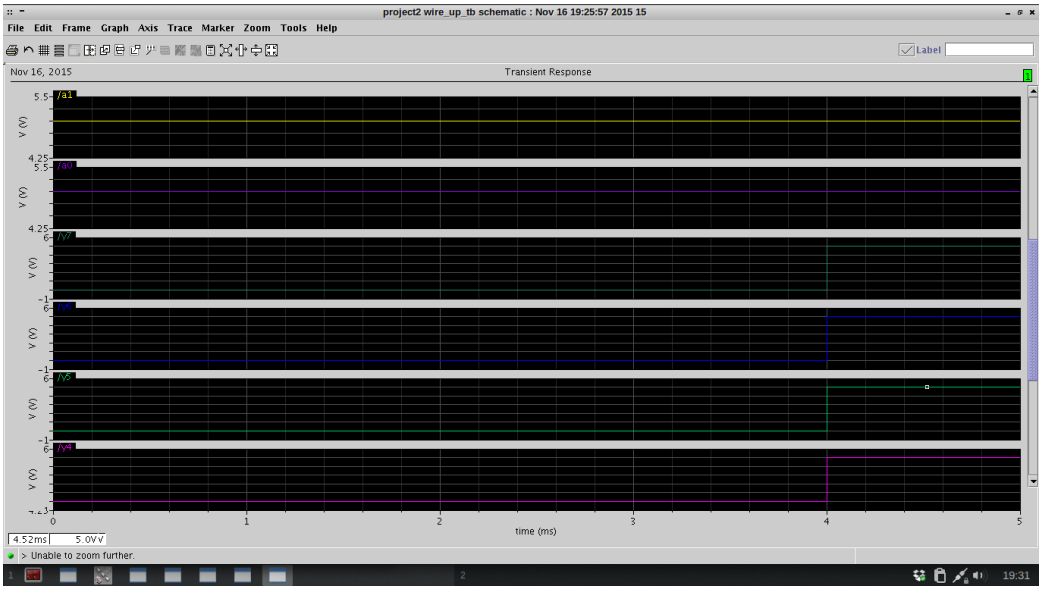
When given two different input, system could recognize which one is faster:

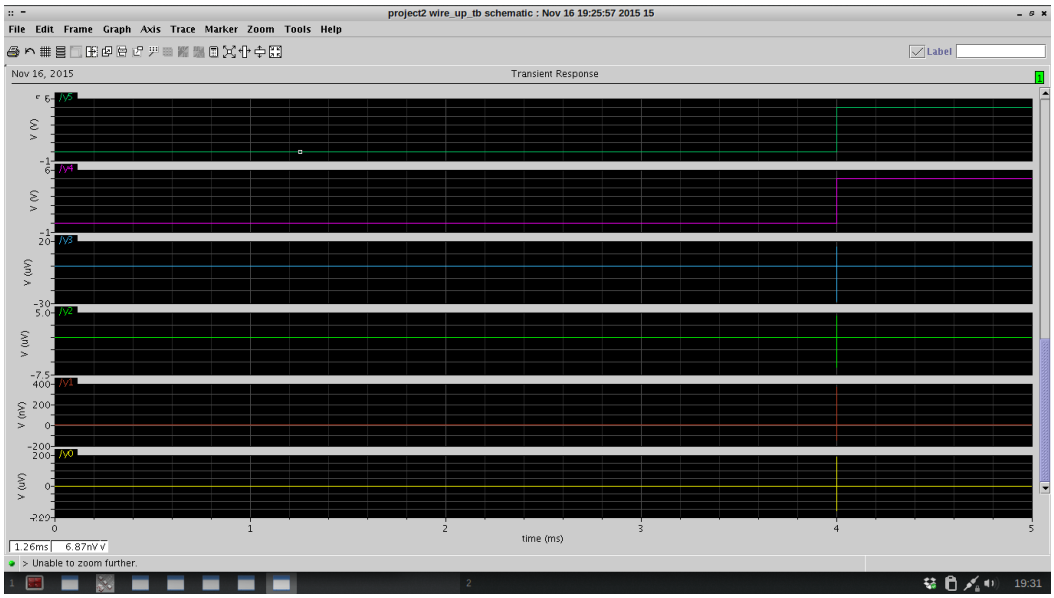
If a3 and a5 are given 0 and a5 is faster, then six LED lights will be lighted. (Shown as the last figures below)

The simulation results show that the system is designed correctly.

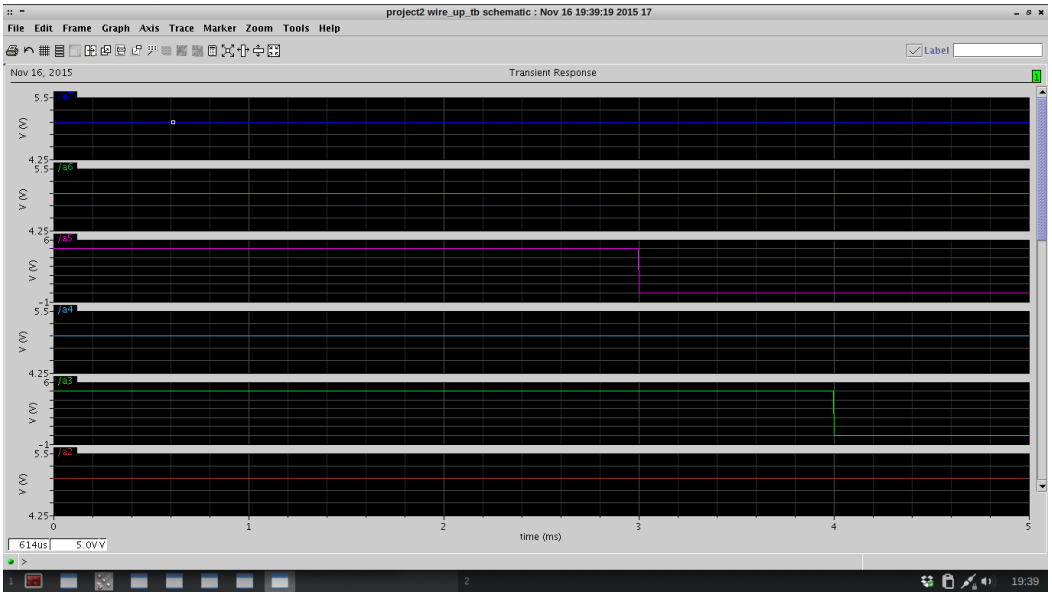
1-input simulation:

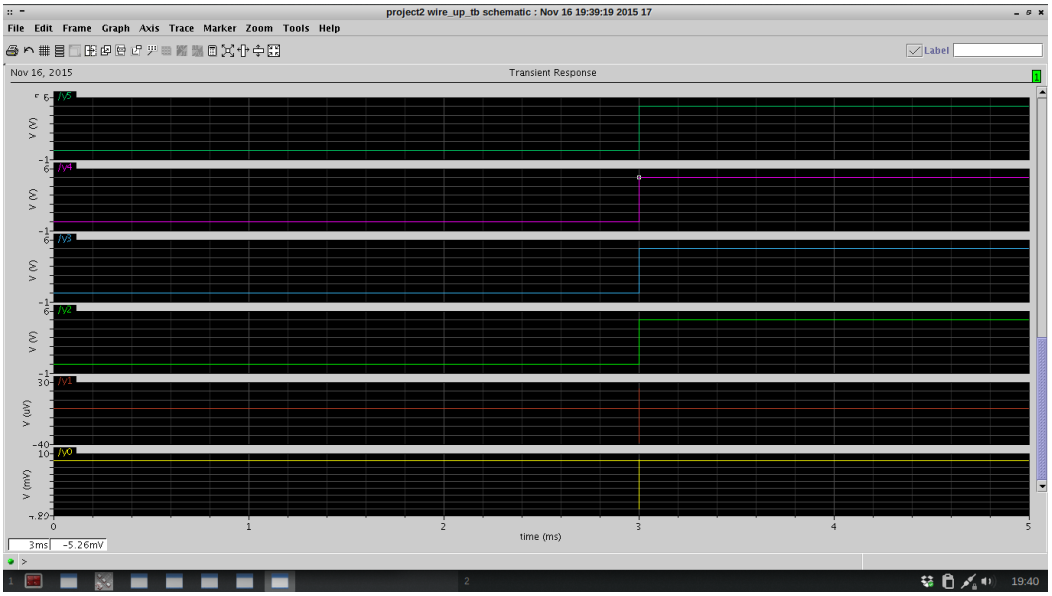


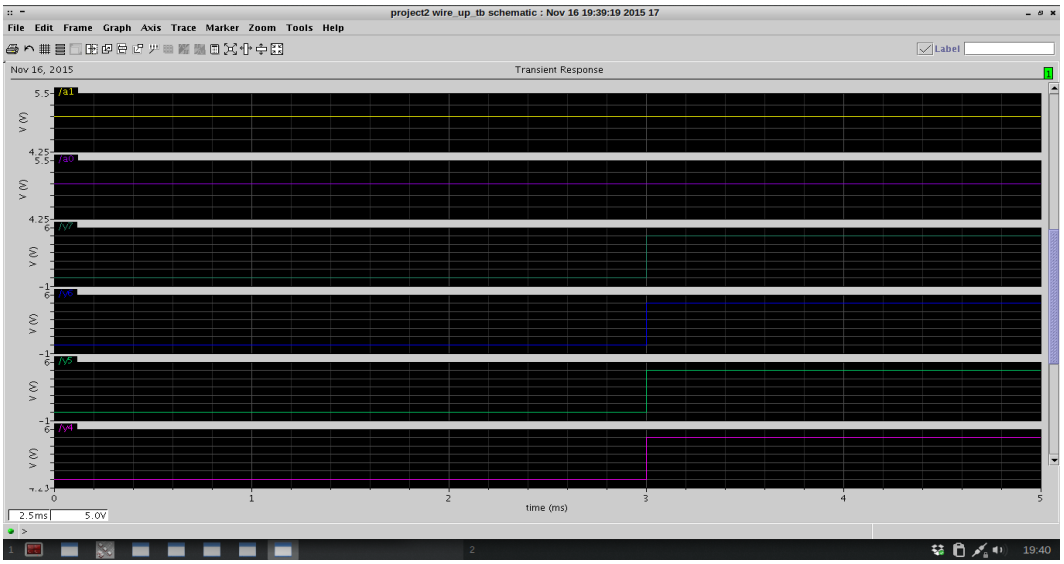




2-different-inputs simulation:

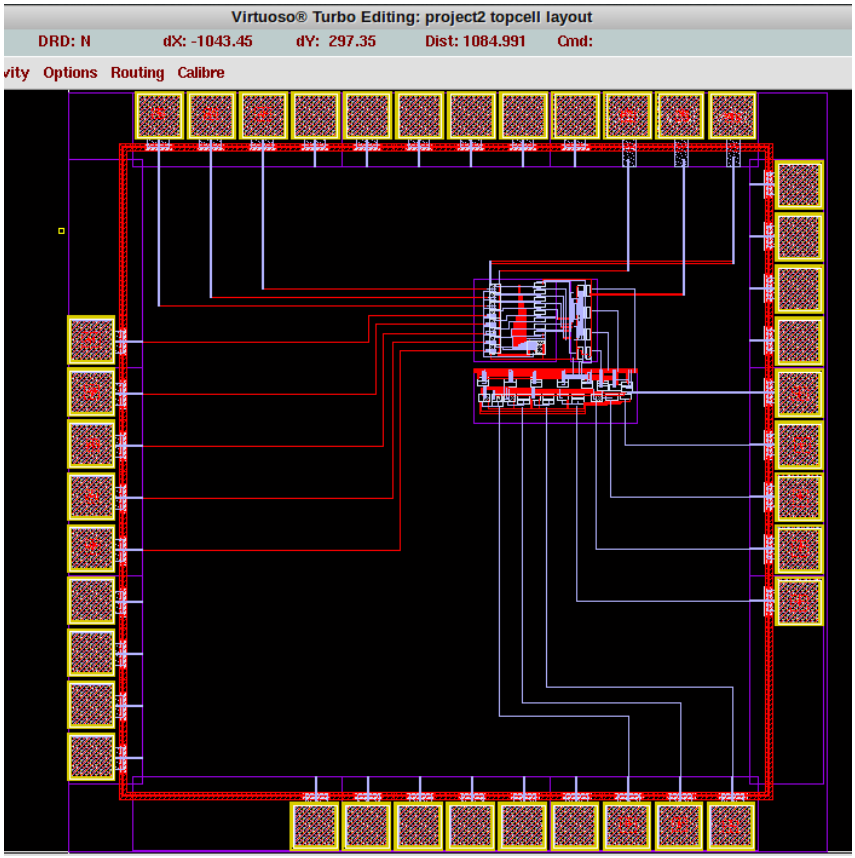




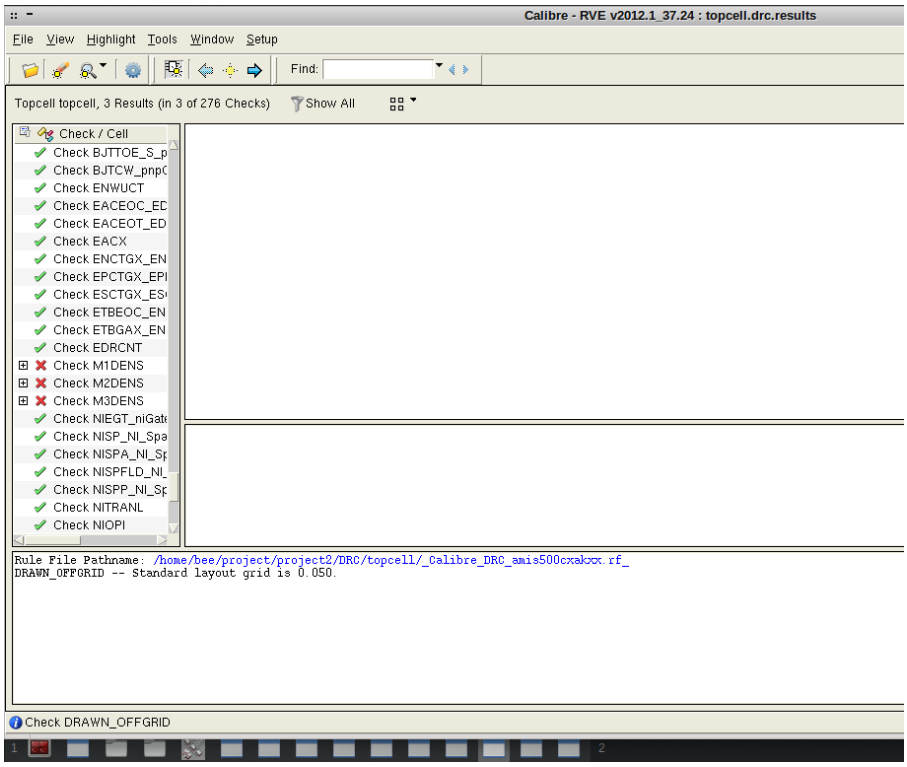


（3）Topcell

Layout:

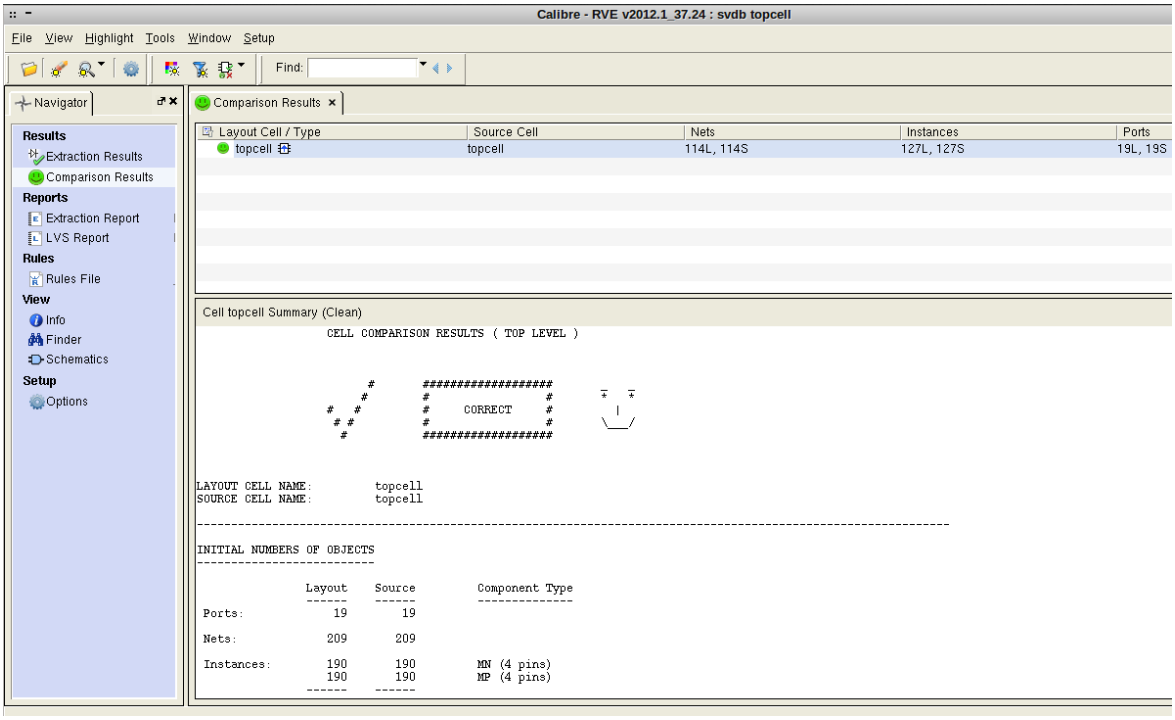


DRC:



It passed DRC only with three metal density errors which can be ignored.

LVS:



It passed LVS with no errors.

6. Post-fabrication test plan

Inputs are A0-A1, and outputs should connect LED lights.

If given one or more input differently, the system could recognized the fastest one and the corresponded number of the LED lights will be lighted.

7. Design time

Floorplan design, including system function, size and schematic.	5 hours.
Schematic design and simulation design to test the system.	5 hours.
Block layout and pass DRC & LVS.	1 day.
Chip layout design and test.	1 day.