CPEG 422/622 Spring 2020

Homework 6

Due May 6th at midnight (through canvas)
Note: The equations to be used are included in the lecture slides. To receive full credit, please show your steps.

Problem 1: The following table show manufacturing data for various processors.

	Wafer Diameter	Dies per Wafer	Defect rate	Cost per Wafer
A	16 cm	85	0.02 defects/cm^2	12
B	20 cm	100	0.03 defects/cm^2	16

a) find the yield for processor A and B.
b) find the cost per die for both processors.
c) If the number of dies per wafer is increased by 15% and the defects per area unit increase by 10%, find the new die area, yield, and cost per die.

Problem 2: The following table shows the increase in clock rate and power of eight generations of Intel processors over 28 years.

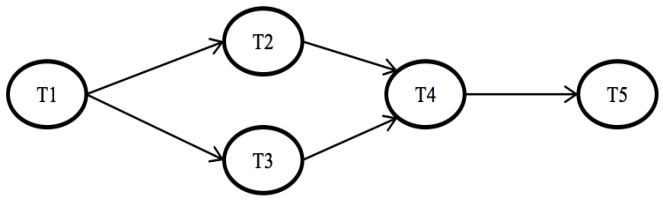
Processor	Clock rate	Voltage	Dynamic Power
80286(1982)	12.5 MHz	5	
80386(1985)	16 MHz	5	
80496(1989)	25 MHz	5	
Pentium (1993)	66 MHz	5	
Pentium Pro (1997)	200 MHz	3.3	
Pentium 4 W (2001)	2 GHz	1.75	
Pentium 4 P (2004)	3.6 GHz	1.25	
Core 2 (2007)	2.67 GHz	1.1	

Assume a capacitive load of 10^-8 for a single core and 1.6*10^-8 for two cores. Find the dynamic power consumed by each generation.

Problem 3: Although the dynamic power is the primary source of power dissipation in CMOS, leakage current produces a static power dissipation V * I_{leak}. The smaller the on-chip dimensions, the more significant is the static power.

a) Assuming for Core 2 in the previous table, the leakage power equals dynamic power. What is the value of leakage current?
b) Assuming for Pentium Pro in the previous table, the leakage power equals 25% of dynamic power. What is the value of leakage current?

Problem 4: You are given a task graph consisting of five tasks (T1, T2, T3, T4, T5) and four different hardware implementations (HW1, HW2, HW3, HW4). The table below shows the performance of these different hardware elements for all the tasks. The cost of hardware elements is $20, $16, $14, $10, respectively. Also, note that the task graph has a deadline of **40** seconds.



Tasks	HW1	HW2	HW3	HW4
T1	9	11	-	16
T2	8	15	13	18
T3	12	7	11	13
T4	10	16	7	12
T5	9	8	10	11

Provide feasible partitioning of tasks among the available hardware elements and generate the following three different schedules (for each schedule, report the start time and core assignment of each task):

a) Minimum execution time schedule.
b) Minimum cost schedule. Note that the minimum cost schedule may miss the deadline.
c) Cheapest schedule (in terms of HW cost) that meets the deadline of the graph.