

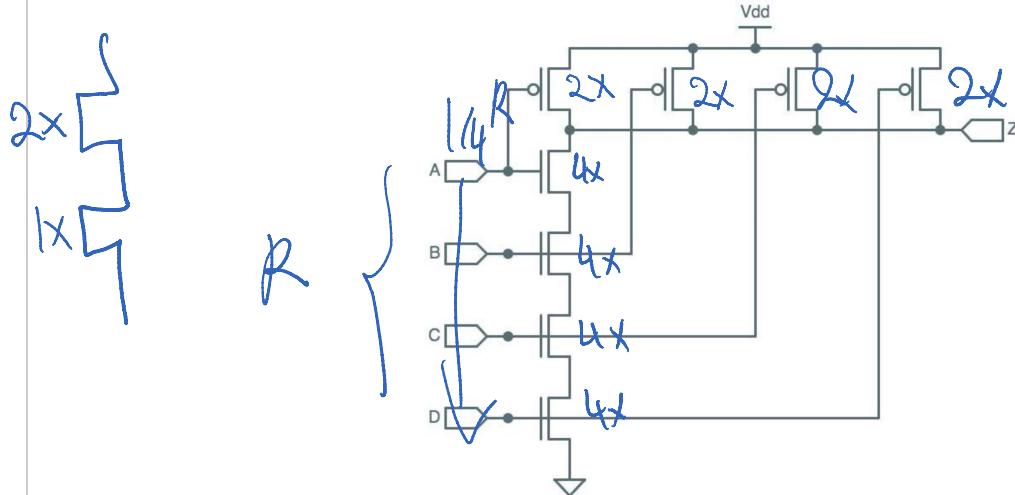
Quiz 5

Wednesday, October 2, 2019 9:30 PM

Q1. Choose transistor widths (e.g. 1, 2, etc) for equal rise/fall time.

Hint 1: CMOS inverter with equal rise/fall time has NMOS width 1 and PMOS width 2.

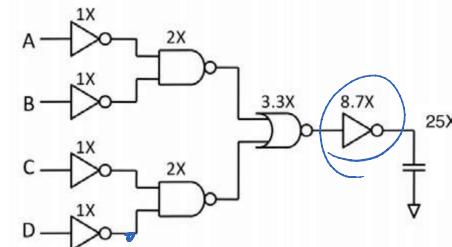
Use the smallest numbers possible

**Q2. Calculate delay (D) of the circuit below.**Hint: Formula for delay is $D = G \cdot h + P$ where $h = C_{out}/C_{in}$. G and P are given below. Assume all inputs arrive at the same time.**G Table**

Gate type	Number of inputs			
	1	2	3	4
Inverter	1			
NAND		4/3	5/3	6/3
NOR		5/3	7/3	9/3
Tristate / mux	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8

P Table

Gate type	Number of inputs			
	1	2	3	4
Inverter	1			
NAND		2	3	4
NOR		2	3	4
Tristate / mux	2	4	6	8
XOR, XNOR		4	6	8



$$D_1 = 1 \cdot \frac{2}{1} + 1 = 3$$

$$D_2 = \frac{4}{3} \cdot \frac{3 \cdot 3}{2} + 2 =$$

$$D_3 = \frac{5}{3} \cdot \frac{8 \cdot 7}{3 \cdot 3} + 2 =$$

$$D_4 = 1 \cdot \frac{25}{8 \cdot 7} + 1 =$$

$$D_T = D_1 + D_2 + D_3 + D_4 \quad (3RC)$$

$$F = G \cdot B \circ H$$

Quiz 5

Wednesday, October 2, 2019 9:33 PM

$$P = \alpha \cdot f \cdot V_{dd}^2$$

$$f_{130} = 3.6 \text{ GHz}$$

$$\alpha_{130} = \alpha_{65}$$

$$V_{dd,130} = 1.5V$$

$$P_{130} = 200W$$

Q3. A 130-nm CMOS microprocessor runs has a clock frequency of 3.6 GHz at a 1.5-volt supply voltage and consumes 200 watts of power. For this problem, assume that all gate capacitances in 65-nm CMOS are 2X smaller than in 130-nm CMOS. Using general scaling and maintaining a clock frequency of 3.2 GHz, what will the power consumption of the processor be, if it is scaled to a 65-nm CMOS process using a 1-volt supply voltage? (assume that the activity factor α is the same in both cases)

$$200 = \alpha \cdot 3.6 \text{ GHz} \cdot C_{130} \cdot 1.5^2$$

$$P_{65} = \alpha \cdot 3.2 \text{ GHz} \cdot \frac{C_{130}}{2} \cdot 1^2$$

$$P_{65} = 200 \times \frac{3.2}{3.6} \cdot \frac{1}{2} \cdot \frac{1}{1.5^2}$$

Assume MOS transistor capacitances are $C = C_g = C_s = C_d = 2 \text{ fF}/\mu\text{m}$ for $L=0.6\mu\text{m}$.

Assume $R_N=10 \text{ k}\Omega \cdot \mu\text{m}$, $R_P=20 \text{ k}\Omega \cdot \mu\text{m}$ for $L=0.6\mu\text{m}$

Q4: Calculate input capacitance of NMOS transistor with $W=1.5\mu\text{m}$ and $L=0.6\mu\text{m}$.

Hint: NMOS input capacitance is $C_g \cdot W$

$$C_N = 2 \text{ fF}/\mu\text{m} \cdot 1.5 \mu\text{m} = 3 \text{ fF}$$

Q5: Calculate resistance of NMOS transistor with $W=1.5\mu\text{m}$ and $L=0.6\mu\text{m}$.

Hint: NMOS transistor resistance is R_N/W

$$R_N = \frac{10 \text{ k}\Omega \cdot \mu\text{m}}{1.5 \mu\text{m}} = 6.67 \text{ k}\Omega$$

Q6: Calculate input capacitance of PMOS transistor with $W=1.5\mu\text{m}$ and $L=0.6\mu\text{m}$.

Hint: PMOS input capacitance is $C_g \cdot W$

$$C_P = 2 \text{ fF}/\mu\text{m} \cdot 1.5 \mu\text{m} = 3 \text{ fF}$$

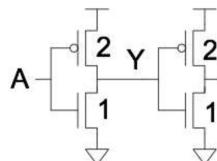
Q7: Calculate resistance of PMOS transistor with $W=1.5\mu\text{m}$ and $L=0.6\mu\text{m}$.

Hint: PMOS transistor resistance is R_P/W

$$R_P = \frac{20 \text{ k}\Omega \cdot \mu\text{m}}{1.5 \mu\text{m}} = 13.3 \text{ k}\Omega$$

Q8: Use answers from Q4-Q7 to estimate A-Y delay in nanoseconds for the circuit below.

Assume ($w=1.5\mu\text{m} = 1x$)



$$6RC$$

$$6(6.67 \text{ k}\Omega) \cdot 3 \text{ fF}$$

$$C_{65} = \frac{1}{2} C_{130}$$

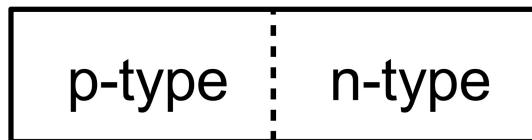
$$f_{65} = 3.2 \text{ GHz}$$

$$P_{65 \text{ nm}} = ?$$

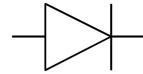
$$V_{dd,65} = 1V$$

p-n Junctions

- ❑ A junction between p-type and n-type semiconductor forms a diode.
- ❑ Current flows only in one direction

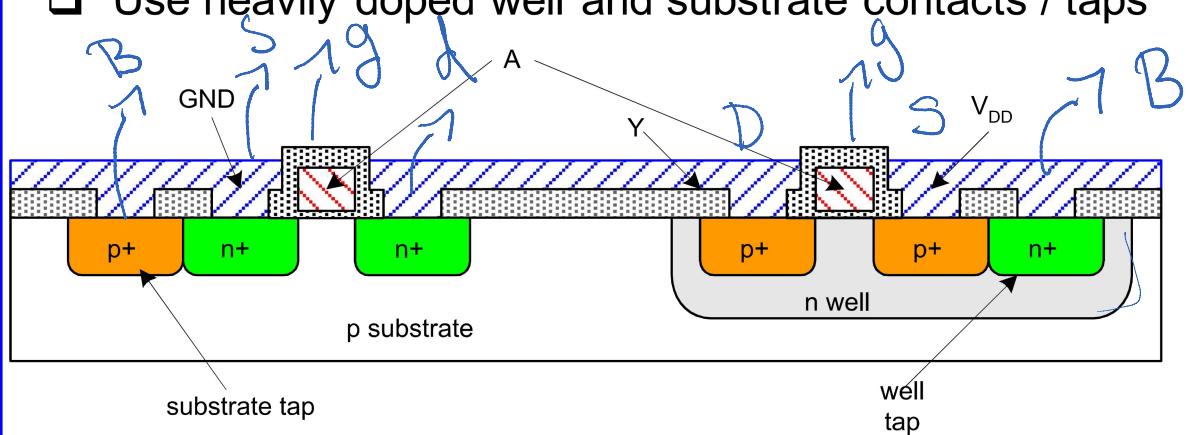


anode cathode



Well and Substrate Taps

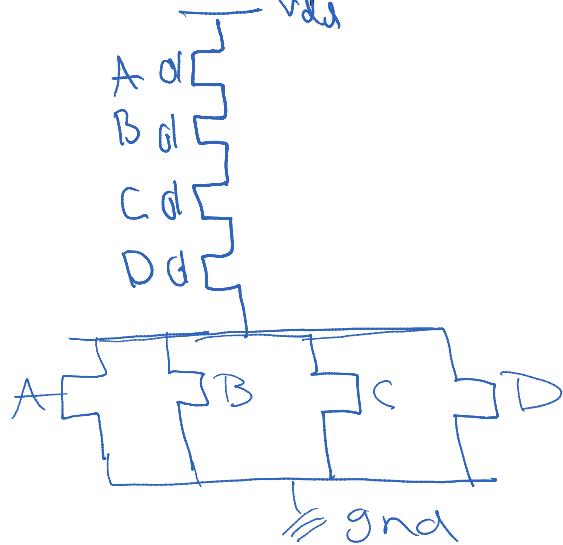
- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



CMOS Gate Design

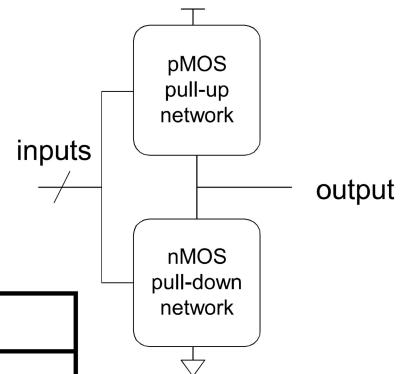
Activity:

- Sketch a 4-input CMOS NOR gate



Complementary CMOS

- Complementary CMOS logic gates
 - nMOS *pull-down network*
 - pMOS *pull-up network*
 - a.k.a. static CMOS

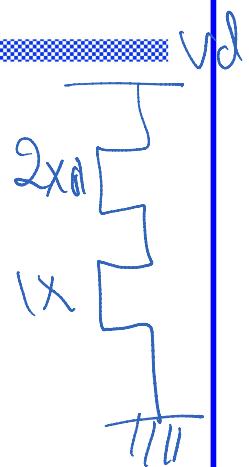
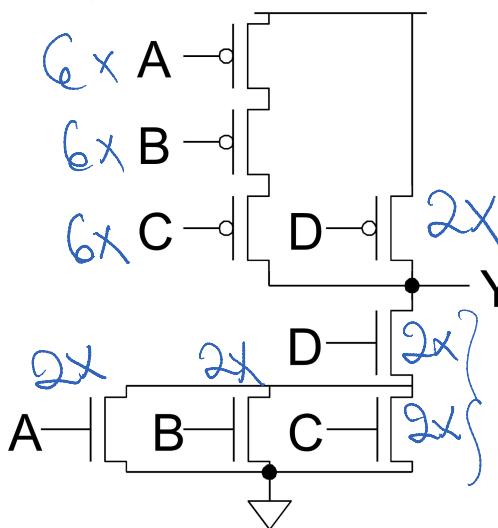


	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

Example: O3AI

□ $Y = \overline{(A + B + C)} D$

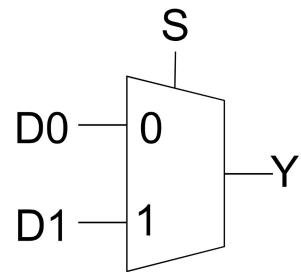
$1x$ Pmos = $2R$



Multiplexers

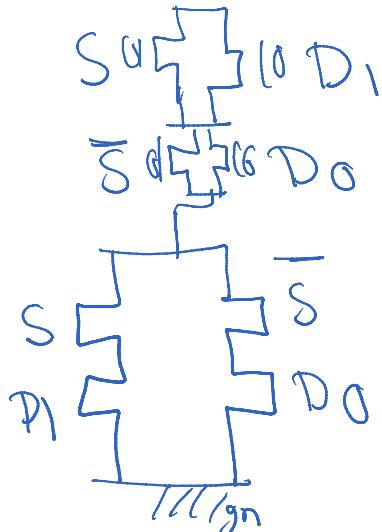
- 4:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1



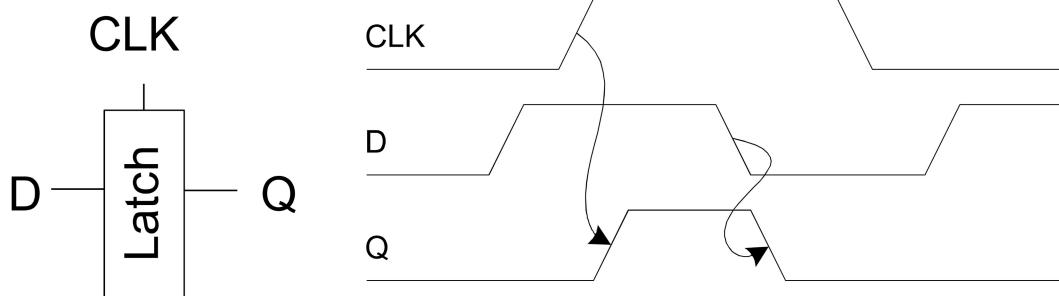
Gate-Level Mux Design

- ❑ $Y = \underline{SD_1} + \overline{SD_0}$ (too many transistors)
- ❑ How many transistors are needed?



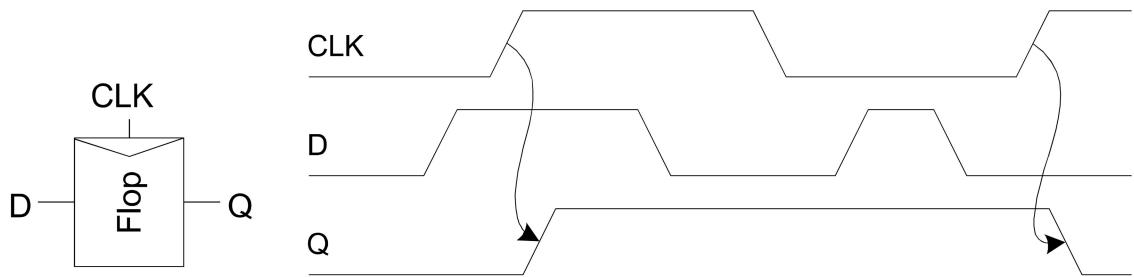
D Latch

- When $\text{CLK} = 1$, latch is *transparent*
 - D flows through to Q like a buffer
- When $\text{CLK} = 0$, the latch is *opaque*
 - Q holds its old value independent of D
- a.k.a. *transparent latch* or *level-sensitive latch*



D Flip-flop

- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. *positive edge-triggered flip-flop, master-slave flip-flop*



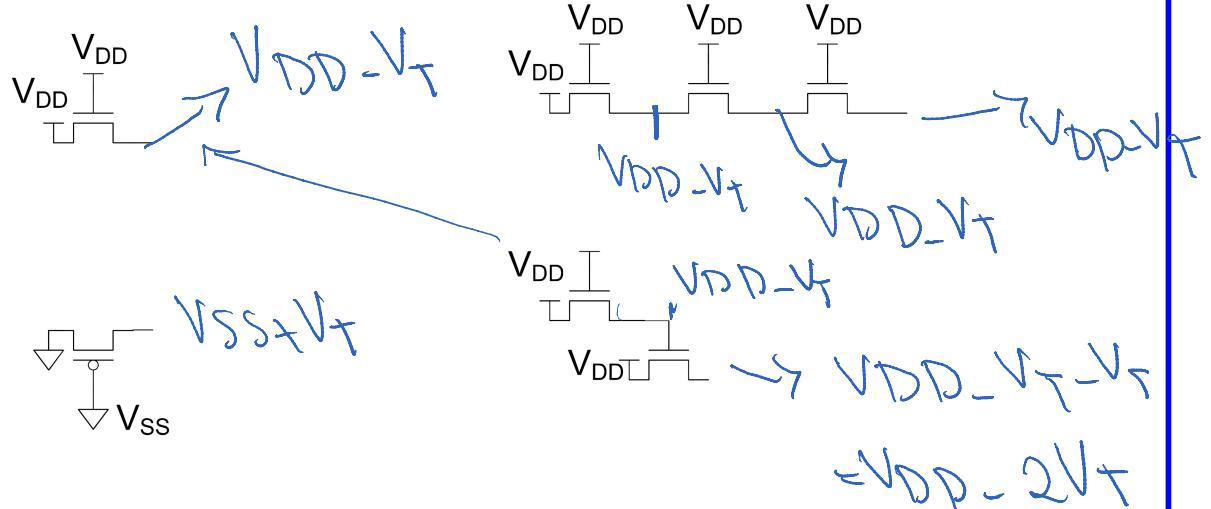
nMOS I-V Summary

- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \end{cases}$$

cutoff
linear
saturation

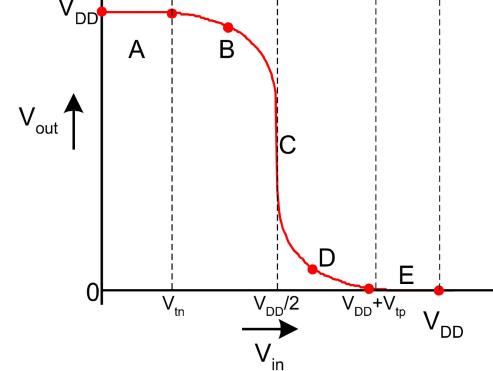
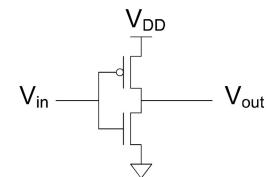
Pass Transistor Ckts



Operating Regions

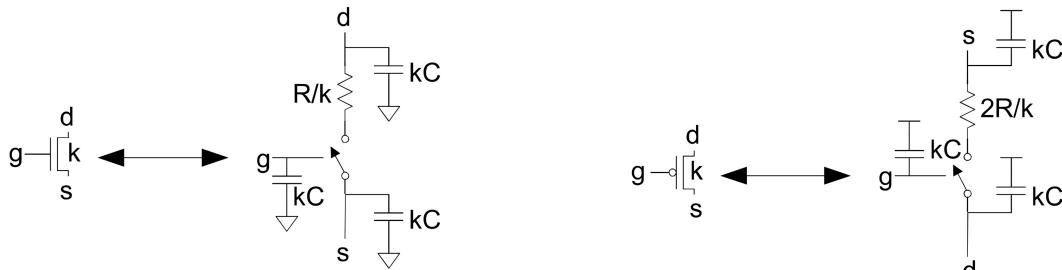
- Revisit transistor operating regions

Region	nMOS	pMOS
A	Cut	lin
B	Sat	lin
C	Sat	Sat
D	lin	Sat
E	lin	Cut



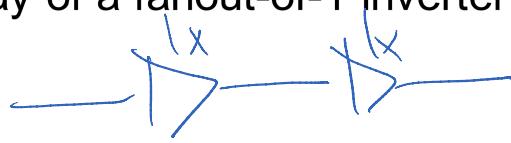
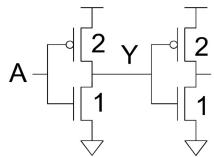
RC Delay Model

- Use equivalent circuits for MOS transistors
 - Ideal switch + capacitance and ON resistance
 - Unit nMOS has resistance R , capacitance C
 - Unit pMOS has resistance $2R$, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width



Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter

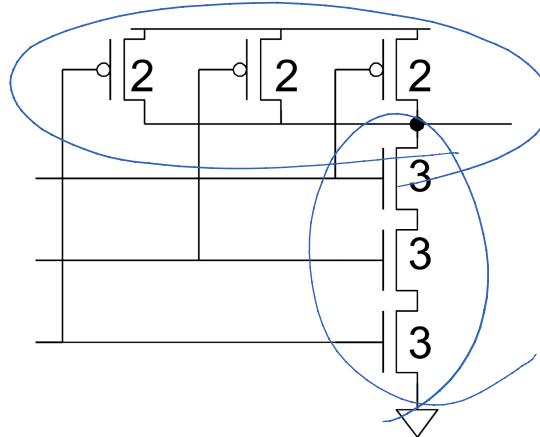


$$D_1 = 1.0 \cdot \frac{1}{f} + l = 2 \text{ (3RC)}$$

$$d = 6RC$$

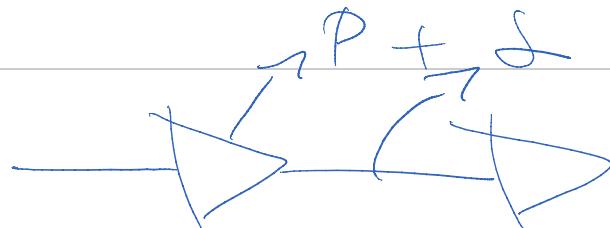
Example: 3-input NAND

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



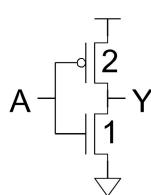
Delay in a Logic Gate

- Express delays in process-independent unit $d = \frac{d_{abs}}{\tau}$
- Delay has two components: $d = f + p$
- f : effort delay = gh (a.k.a. stage effort)
 - Again has two components
- g : logical effort
 - Measures relative ability of gate to deliver current
 - $g = 1$ for inverter
- h : electrical effort = C_{out} / C_{in}
 - Ratio of output to input capacitance
 - Sometimes called fanout
- p : parasitic delay
 - Represents delay of gate driving no load
 - Set by internal parasitic capacitance

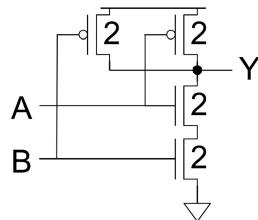


Computing Logical Effort

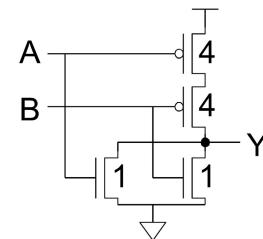
- DEF: *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current.*
- Measure from delay vs. fanout plots
- Or estimate by counting transistor widths



$$C_{in} = 3 \\ g = 3/3$$



$$C_{in} = 4 \\ g = 4/3$$



$$C_{in} = 5 \\ g = 5/3$$

Review of Definitions

Term	Stage	Path
number of stages	1	N
logical effort	g	$G = \prod g_i$
electrical effort	$h = \frac{C_{\text{out}}}{C_{\text{in}}}$	$H = \frac{C_{\text{out-path}}}{C_{\text{in-path}}}$
branching effort	$b = \frac{C_{\text{on-path}} + C_{\text{off-path}}}{C_{\text{on-path}}}$	$B = \prod b_i$
effort	$f = gh$	$F = GBH$
effort delay	f	$D_F = \sum f_i$
parasitic delay	p	$P = \sum p_i$
delay	$d = f + p$	$D = \sum d_i = D_F + P$

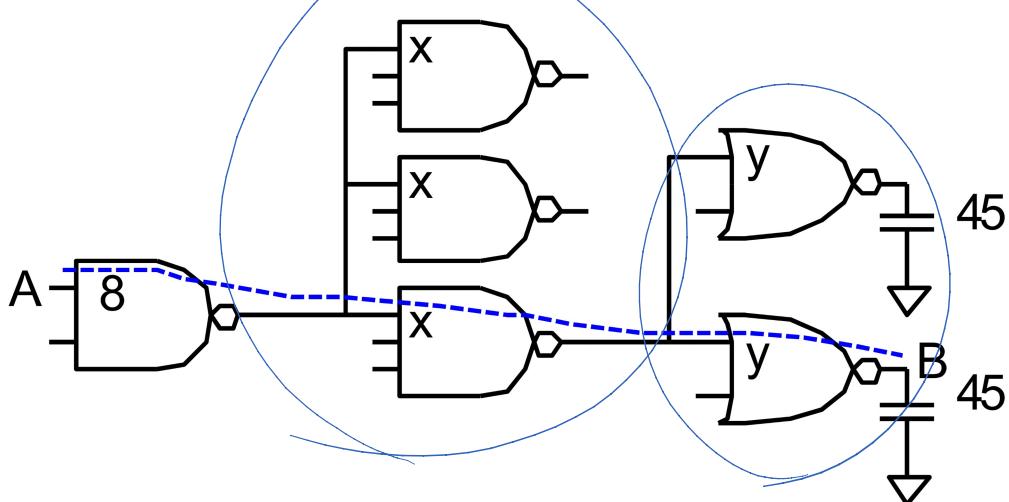
Method of Logical Effort

- 1) Compute path effort $F = GBH$
- 2) Estimate best number of stages $N = \log_4 F$
- 3) Sketch path with N stages
- 4) Estimate least delay $D = NF^{\frac{1}{N}} + P$
- 5) Determine best stage effort $\hat{f} = F^{\frac{1}{N}}$
- 6) Find gate sizes

$$C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$$

Example: 3-stage path

- Select gate sizes x and y for least delay from A to B



Power Dissipation Sources

- $P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}}$
- Dynamic power: $P_{\text{dynamic}} = P_{\text{switching}} + \underline{P_{\text{shortcircuit}}}$
 - Switching load capacitances
 - Short-circuit current
- Static power: $P_{\text{static}} = (I_{\text{sub}} + I_{\text{gate}} + I_{\text{junct}} + I_{\text{contention}})V_{\text{DD}}$
 - Subthreshold leakage
 - Gate leakage
 - Junction leakage
 - Contention current

Activity Factor

- Suppose the system clock frequency = f
- Let $f_{sw} = \alpha f$, where α = activity factor
 - If the signal is a clock, $\alpha = 1$
 - If the signal switches once per cycle, $\alpha = \frac{1}{2}$
- Dynamic power:

$$P_{\text{switching}} = \alpha C V_{DD}^2 f$$