LAB5 – Design a two input NAND gate

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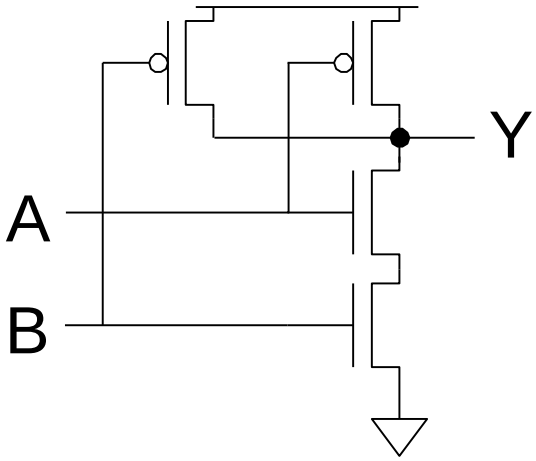

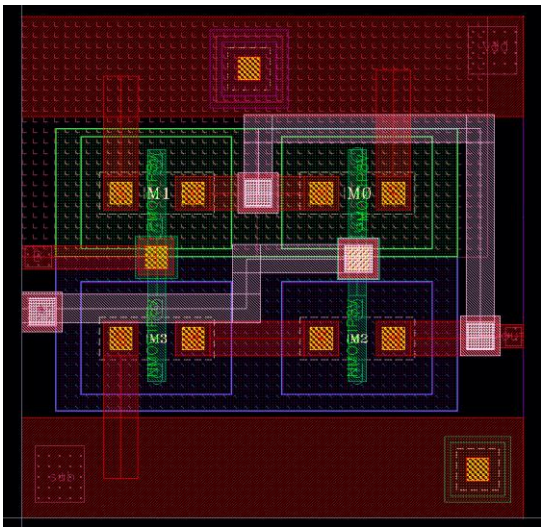

Using the skills learned in labs 1 through 4, design, layout, DRC and LVS check your own NAND gate design. Follow the following steps:

1. Capture the schematic for you circuit. Start with all four transistors having width of 0.42um for nmos and 1.47um for pmos, and length of 0.18um.
2. Layout the NAND gate. The layout should look similar to the image shown above.
3. Perform DRC and LVS verification of your layout.

What to turn in?

Schematic, layout, error free DRC and LVS screenshots.