COURSE DESCRIPTION CPEG460 –
Introduction to VLSI Systems

Course Title: Introduction to VLSI Systems
Course Number: CPEG460-010; CPEG460-080; CPEG660-010
Instructor: Peyman Barakhshan
TA: Jaclyn Singh
Office Hours: appointments only_ Evans 121
Class Time/room: Tu/Thu 11-12:15pm, Colburn 046

Catalog Description: Study of CMOS VLSI devices, circuits and systems implemented in VLSI. CAD tools for the design and simulation of VLSI Circuits. Topics include the performance and limitations of VLSI systems, low level circuit design and system design with an emphasis on digital systems. Major chip design project required

Prerequisites: Students should have previous knowledge of logic design and MOS transistor operation.

Co-requisites: N/A

Prequisite for: Students should have previous knowledge of logic design and MOS transistor operation.

Textbook and other required material: CMOS VLSI Design: A systems and circuits perspective, N. Weste, Pearson, 4th Ed. (2010)

Course Objectives:
This is a course on CMOS VLSI design for undergraduate students, generally taken by senior CPEG and ELEG students. The course introduces students to design of digital integrated circuits. At the end of the course, the students should be able to design, capture schematic, simulate schematic, layout and extract layout for a complete and high-performance digital ASIC design.

Topics Covered:
The course material covers CMOS devices and manufacturing technology along with CMOS inverters and gates. Other topics include propagation delay, noise margins, power dissipation, and regenerative logic circuits. We examine various design styles and architectures as well as the issues that designers must face, such as technology scaling and the impact of interconnect. The course starts with a detailed description and analysis of the core digital design block: the CMOS inverter. Implementation in CMOS is discussed next. Next, the design of more complex combinational gates such as NAND, NOR and XOR is discussed, looking at optimizing the speed, area, or power. The influence of interconnect parasitic on circuit performance and approaches to cope with them are treated in detail. Substantial attention is devoted to sequential circuits and clocking approaches. CAD Tools for layout, extraction, and simulation are used for assignments, and project. A design project is a major part of this course.

Material for evaluation:

Homework 10%
Quizzes 10%
Projects 50%
Midterm 15%
Final 15%

Homework are due by 5pm on due date by electronic submission on Sakai. Homework can be turned in 1 week late for 50% credit. After 1-week delay, no credit will be given.
