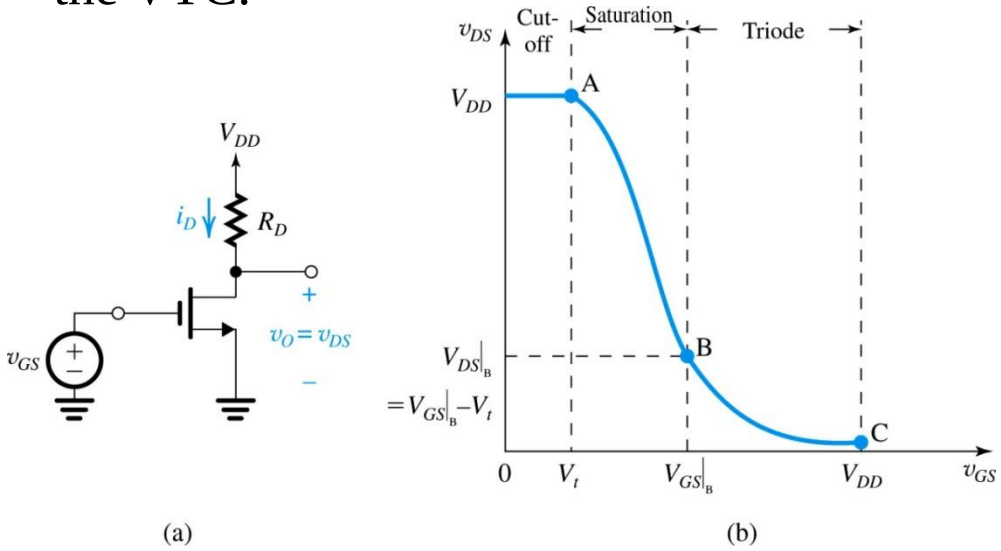
Homework #13

Problems 7.1, 7.5, 7.6, 7.10, and 7.18

Problem 7.1

For the MOS amplifier of Fig. 7.2(a) with V_{DD} = 5 V, V_t = 0.5 V, k_n= 10 mA/V^2, and R_D = 20 kΩ, determine the coordinates of the active region segment (AB) of the VTC.



Cut-off /saturation boundary (A) is where $v_{GS} = V_t = 0.5V$

$v_{DS} = 5V = V_{DD}$

saturation /triode boundary (B) is where

$$V_{GS\_B} := V_t + \frac{\sqrt{2 \cdot k_n R_D \cdot V_{DD} + 1} - 1}{k_n \cdot R_D} = 0.719V$$

$$V_{DS\_B} := V_{GS\_B} - V_t = 0.219\ V$$

Problem 7.5

Consider the amplifier of Fig. 7.4(a) for the case V_{DD} = 5 V, R_D = 24 kΩ, $k'_n(W/L)$ = 1 mA/V^2, and V_t = 1 V.

(a) Find the coordinates of the two end points of the saturation-region segment of the amplifier transfer characteristic, that is, points A and B on the sketch of Fig 7.4(b).

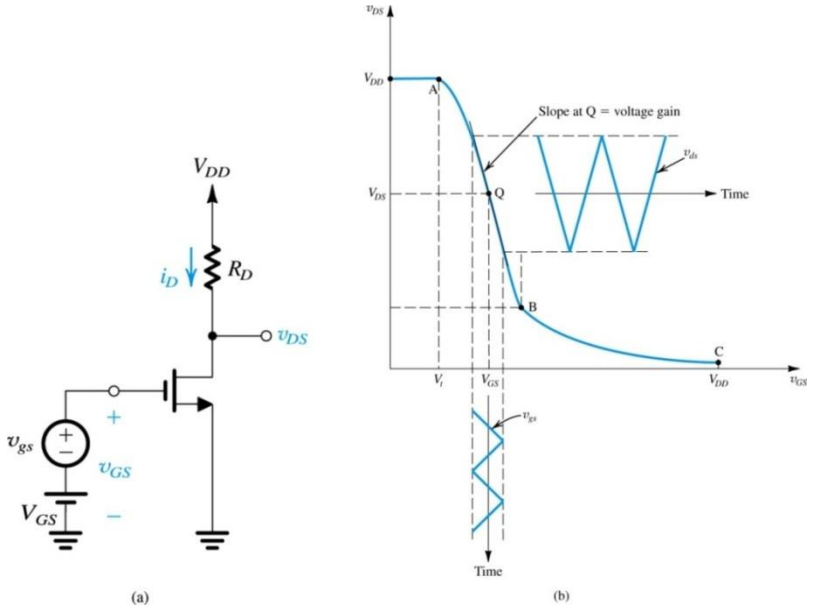
(b) If the amplifier is biased to operate with an overdrive voltage V_{OV} of 0.5 V, find the coordinates of the bias point *Q* on the transfer characteristic. Also, find the value of I_D and of the incremental gain *Av* at the bias point.

(c) For the situation in (b), and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of these amplitudes imply? By what percentage is this gain value different from the incremental gain value calculated above? Why is there a difference?

Problem 7.5a

Consider the amplifier of Fig. 7.4(a) for the case V_{DD} = 5 V, R_D = 24 kΩ, $k_n'(W/L)$ = 1 mA/V^2, and V_t = 1 V.

(a) Find the coordinates of the two end points of the saturation-region segment of the amplifier transfer characteristic, that is, points A and B on the sketch of Fig 7.4(b).



Cut-off /saturation boundary (A) is where

$$v_{GS} = V_t = 1V$$

$$v_{DS} = 5V = V_{DD}$$

saturation /triode boundary (B) is where

$$V_{GS\_B} := V_t + \frac{\sqrt{2 \cdot k_n R_D \cdot V_{DD} + 1} - 1}{k_n \cdot R_D} = 1.605V$$

$$V_{DS\_B} := V_{GS\_B} - V_t = 0.605\ V$$

Problem 7.5b

Consider the amplifier of Fig. 7.4(a) for the case V_{DD} = 5 V, R_D = 24 kΩ, $k_n'(W/L)$ = 1 mA/V^2, and V_t = 1 V.

(b) If the amplifier is biased to operate with an overdrive voltage V_{OV} of 0.5 V, find the coordinates of the bias point Q on the transfer characteristic. Also, find the value of I_D and of the incremental gain Av at the bias point.

$$V_{GS} = V_t + V_{OV} = 1.5\text{V}$$

$$I_D := \frac{1}{2} k_n \cdot V_{OV}^{\ 2} = 0.125\ mA$$

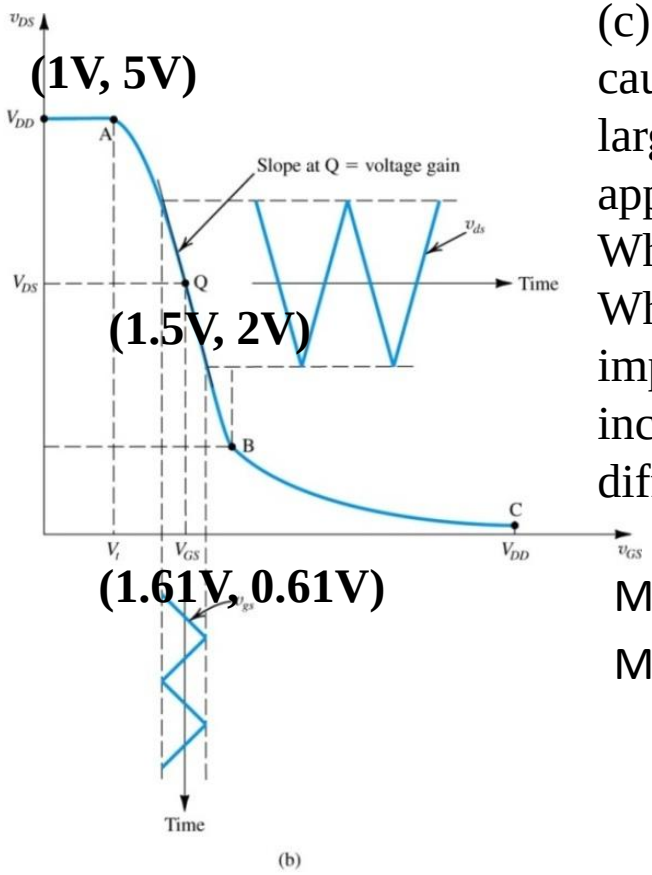
$$V_{DS} = V_{DD} - I_D R_D = 2.0\text{V}$$

$$A_v = -k_n (V_{GS} - V_t) R_D$$

$$A_v := -k_n \cdot V_{OV} \cdot R_D = -12\ \frac{V}{V}$$

Problem 7.5c

Consider the amplifier of Fig. 7.4(a) for the case V_{DD} = 5 V, R_D = 24 kΩ, $k_n'(W/L)$ = 1 mA/V^2, and V_t = 1 V.



(c) For the situation in (b), and disregarding the distortion caused by the MOSFET's square-law characteristic, what is the largest amplitude of a sine-wave voltage signal that can be applied at the input while the transistor remains in saturation? What is the amplitude of the output voltage signal that results? What gain value does the combination of these amplitudes imply? By what percentage is this gain value different from the incremental gain value calculated above? Why is there a difference?

Max input: $1.61V - 1.5V = 0.11V$

Max output (at Vin = 1.61V): $2V - 0.61V = 1.39V$

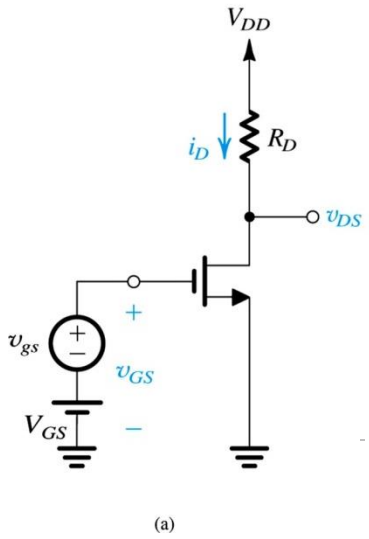
Min output (at Vin = 1.39V): $3.175V - 2V = 1.175V$

Gain = (1.39+1.175)/(0.22) =11.66 V/V

% different = 2.8%

Problem 7.6

Various measurements are made on an NMOS amplifier for which the drain resistor R_D is 20 kΩ. First, dc measurements show the voltage across the drain resistor, V_{RD}, to be 1.5 V and the gate-to-source bias voltage to be 0.7 V. Then, ac measurements with small signals show the voltage gain to be –10 V/V. What is the value of V_t for this transistor? If the process transconductance parameter k'_n is 200 μA/V^2, what is the MOSFET's W/L?



(a)

$$A_v = -k_n V_{OV} R_D = -10\,\frac{\text{V}}{\text{V}} \qquad \Rightarrow k_n = \frac{10}{V_{OV} R_D}$$

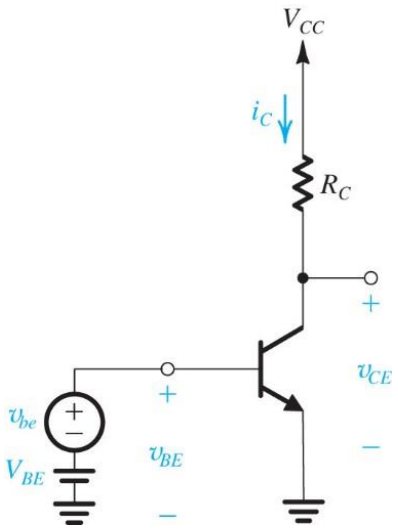
$$V_{RD} = I_D R_D = \frac{1}{2} k_n V_{OV}^2 R_D = \frac{1}{2}\left(\frac{10}{V_{OV} R_D}\right) V_{OV}^2 R_D = 1.5\text{V}$$

$$\Rightarrow V_{OV} = \frac{1.5\text{V}}{5} = 0.3\text{V} \qquad V_t = V_{GS} - V_{OV} = 0.7\text{V} - 0.3\text{V} = 0.4\text{V}$$

$$k_n := \frac{10}{0.3\,V \cdot 20\,k\Omega} = 1.667\,\frac{mA}{V^2} \qquad W\_L := \frac{k_n}{200\,\frac{\mu A}{V^2}} = 8.333$$

Problem 7.10

A BJT amplifier circuit such as that in Fig. 7.6 is operated with V_{CC} = + 5 V and is biased at V_{CE} = +1 V. Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.



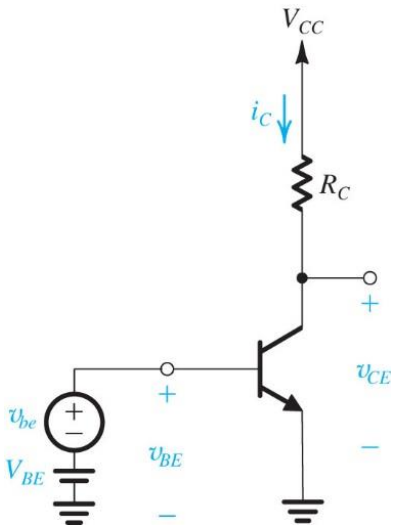
$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{CC} - V_{CE}}{V_T} = -\frac{4\text{V}}{0.025\text{V}} = -160\frac{\text{V}}{\text{V}}$$

The transistor enters saturation when $v_{CE} \leq 0.3$ V, thus the maximum allowable output voltage swing is 1 − 0.3 = 0.7 V. The corresponding maximum input signal permitted is

$$\hat{v}_{be} = \frac{\hat{v}_{ce}}{A_v} = \frac{0.7\text{V}}{160\frac{\text{V}}{\text{V}}} = 4.4\text{mV}$$

Problem 7.18

When the amplifier circuit of Fig. 7.6 is biased with a certain V_{BE}, the dc voltage at the collector is found to be +2 V. For V_{CC} = +5 V and R_C = 1 kΩ, find I_C and the small-signal voltage gain. For a change Δv_{BE} = +5 mV, calculate the resulting Δv_O. Calculate it two ways: by using the transistor exponential characteristic Δi_C, and approximately, using the small-signal voltage gain. Repeat for Δv_{BE} = −5 mV. Summarize your results in a table.



$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{5\text{V} - 2\text{V}}{1\text{k}\Omega} = 3\text{mA}$$

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{CC} - V_{CE}}{V_T} = -\frac{3\text{V}}{0.025\text{V}} = -120\frac{\text{V}}{\text{V}}$$

Δv_{BE} = +5 mV

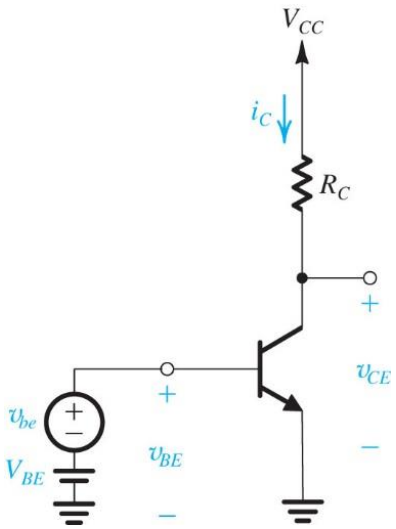
$$\frac{I_{C2}}{I_{C1}} = e^{(V_2 - V_1)/V_T} = e^{5\text{mV}/25\text{mV}} = 1.22 \Rightarrow \Delta i_C = 0.22 I_C = 0.66\text{mA}$$

$$\Delta v_O = -\Delta i_C R_C = -0.66\text{mA}\left(1\text{k}\Omega\right) = -0.66\text{V}$$

$$\Delta v_O = A_v \times \Delta v_{BE} = -120\frac{\text{V}}{\text{V}}\left(5\text{mV}\right) = -0.60\text{V}$$

Problem 7.18

When the amplifier circuit of Fig. 7.6 is biased with a certain V_{BE}, the dc voltage at the collector is found to be +2 V. For V_{CC} = +5 V and R_C = 1 kΩ, find I_C and the small-signal voltage gain. For a change Δv_{BE} = +5 mV, calculate the resulting Δv_O. Calculate it two ways: by using the transistor exponential characteristic Δi_C, and approximately, using the small-signal voltage gain. Repeat for Δv_{BE} = −5 mV. Summarize your results in a table.



$$\Delta v_{BE} = \text{-5 mV}$$

$$\frac{I_{C2}}{I_{C1}} = e^{(V_2 - V_1)/V_T} = e^{-5\text{mV}/25\text{mV}} = 0.82 \Rightarrow \Delta i_C = -0.18 I_C = 0.54\text{mA}$$

$$\Delta v_O = -\Delta i_C R_C = 0.54\text{mA}\,(1\text{k}\Omega) = 0.54\text{V}$$

$$\Delta v_O = A_v \times \Delta v_{BE} = -120\,\frac{\text{V}}{\text{V}}(-5\text{mV}) = 0.60\text{V}$$

Δv_{BE}	Δv_O (linear)	Δv_O (exponential)
+5mV	-0.6V	-0.66V
-5mV	0.6V	0.54V