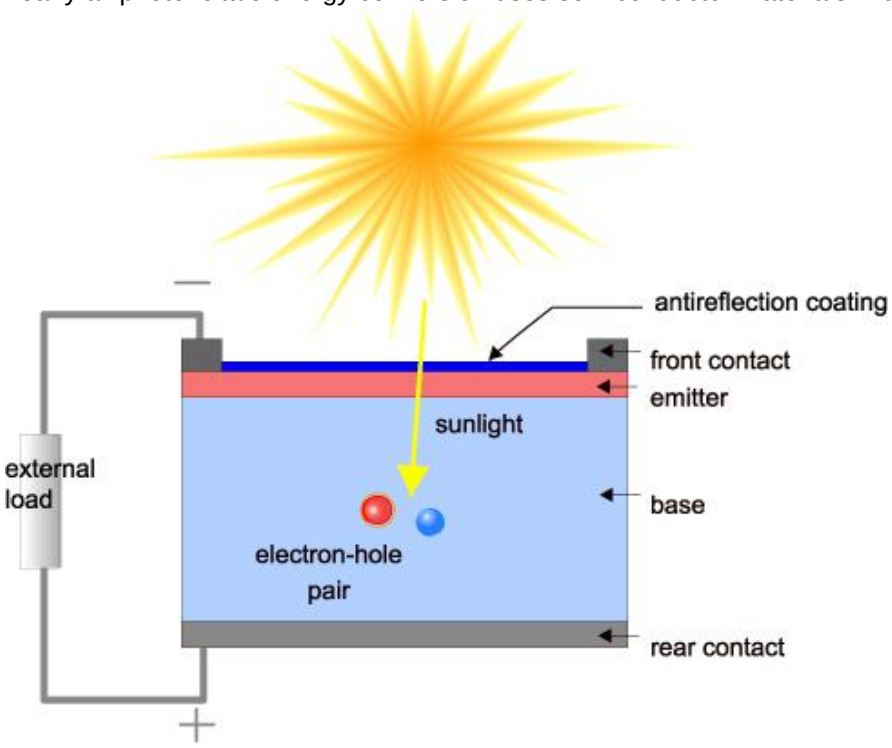
Manish Bajpai mbajpai@udel.edu

Solar cell manufacturing

We all know renewable energy is the need of the hour. I was curious to know how the solar cells are made. Even though it is not possible to give detailed description of the manufacturing process, I have tried to include as much details as possible, and concentrating on manufacturing aspects of solar cells. First few paragraphs briefly describe the operation of solar cells and the array design. Later I have described the manufacturing process of solar cells from silicon wafers. One of the processes (known as Czochralski) process is described followed by doping of the wafers and treatment of the cells.

Solar Cell Structure

A solar cell is an electronic device which directly converts sunlight into electricity. Light shining on the solar cell produces both a current and a voltage to generate electric power. This process requires firstly, a material in which the absorption of light raises an electron to a higher energy state, and secondly, the movement of this higher energy electron from the solar cell into an external circuit. The electron then dissipates its energy in the external circuit and returns to the solar cell. A variety of materials and processes can potentially satisfy the requirements for photovoltaic energy conversion, but in practice nearly all photovoltaic energy conversion uses semiconductor materials in the form of a p-n junction.



1. Refining Silicon

Silicon dioxide (SiO2) is the most abundant mineral in the earth's crust. The manufacture of the hyperpure silicon for photovoltaic starts with locating a source of silicon dioxide in the form of silica or sand. Ideally the silica has low concentrations of iron, aluminum and other metals. The silica is reduced (oxygen removed) through a reaction with carbon in the form of coal, charcoal and heating to 1500-2000 °C in an electrode arc furnace.

$$Si + 3HCl \Rightarrow SiHCl_3 + H_2$$

The resulting silicon is metallurgical grade silicon (MG-Si). It is 98% pure and is used extensively in the metallurgical industry.
A small amount of the metallurgical grade silicon is further refined for the semiconductor industry. Powdered MG-Si is reacted with anhydrous HCl at 300 °C in a fluidized bed reactor to form SiHCl3

$$Si + 3HCl \Rightarrow SiHCl_3 + H_2$$

During this reaction impurities such as Fe, Al, and B react to form their halides (e.g. FeCl3, AlCl3, and BCl3). The SiHCl3 has a low boiling point of 31.8 °C and distillation is used to purify the SiHCl3 from the impurity halides. The resulting SiHCl3 now has electrically active impurities (such as Al, P, B, Fe, Cu or Au) of less than 1 ppba.

Finally, the pure SiHCl3 is reacted with hydrogen at 1100°C for ~200 – 300 hours to produce a very pure form of silicon.

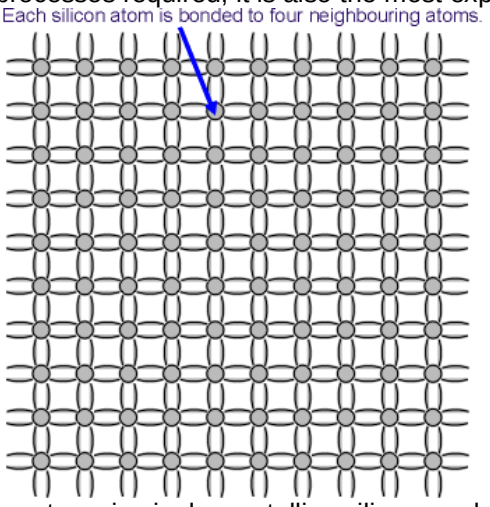
$$SiHCl_3 + H_2 \Rightarrow Si + 3HCl$$

The reaction takes place inside large vacuum chambers and the silicon is deposited onto thin polysilicon rods (small grain size silicon) to produce high-purity polysilicon rods of diameter 150-200mm. The process was first developed by Siemens in the 60's and is often referred to as the Siemens process.

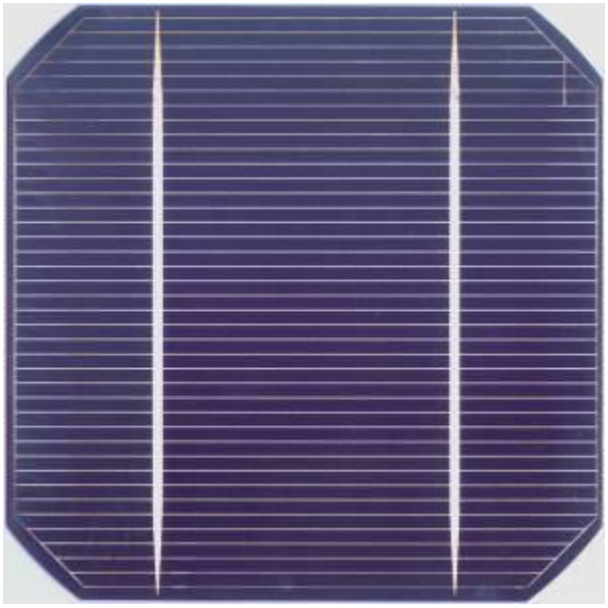
The resulting rods of semiconductor grade silicon are broken up to form the feedstock for the crystallisation process. The production of semiconductor grade silicon requires a lot of energy. Solar cells can tolerate higher levels of impurity than integrated circuits fabrication and there are proposals for alternative processes to create”solar-grade" silicon.

1.1 Single Crystalline Silicon

The majority of silicon solar cells are fabricated from silicon wafers, which may be either single-crystalline or multi-crystalline. Single-crystalline wafers typically have better material parameters but are also more expensive. Crystalline silicon has an ordered crystal structure, with each atom ideally lying in a pre-determined position. Crystalline silicon exhibits predictable and uniform behaviour but because of the careful and slow manufacturing processes required, it is also the most expensive type of silicon.



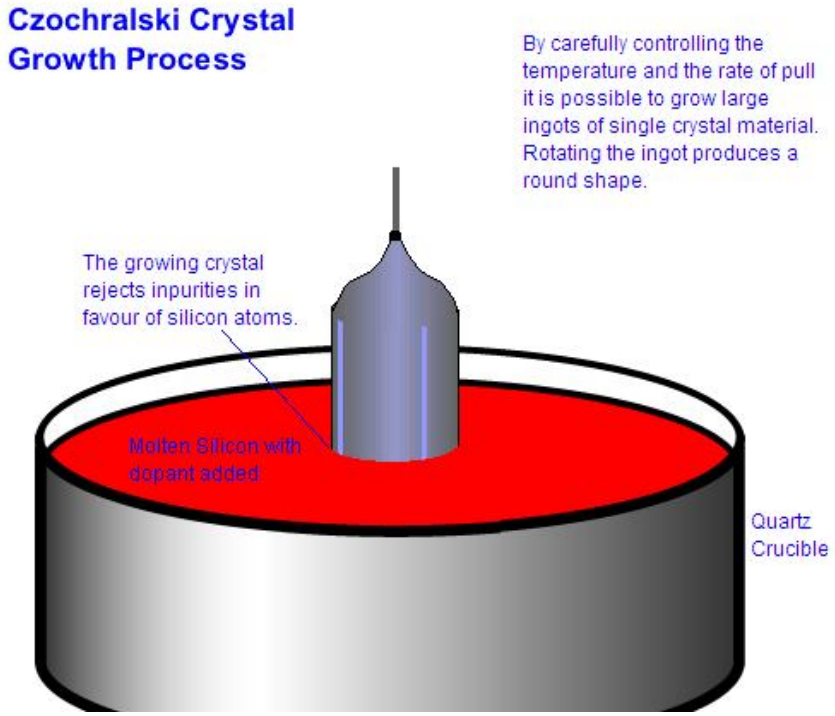
The regular arrangement of silicon atoms in single-crystalline silicon produces a well-defined band structure. Each silicon atom has four electrons in the outer shell. Pairs of electrons from neighbouring atoms are shared so each atom shares four bonds with the neighbouring atoms.



Single crystalline silicon is usually grown as a large cylindrical ingot producing circular or semi-square solar cells. The semi-square cell started out circular but has had the edges cut off so that a number of cells can be more efficiently packed into a rectangular module.

Process: Czochralski Silicon wafers

Single crystalline substrates are typically differentiated by the process by which they are made. Czochralski (CZ) wafers are the most commonly used type of silicon wafer, and are used by both the solar and integrated circuit industry. The process of making a large single crystalline silicon ingot by the Czochralski process is shown below.



2. Source Material

In the past it was common for the source material for solar cell production to be off cuts from the integrated circuit industry. The source material has to be checked for impurities and to make sure that it has the right dopant type and resistivity. Almost all cells are presently made on p-type substrates. Notable exceptions are the rear contact cells made by Sunpower and amorphous/crystalline silicon heterojunction cells manufactured by Sanyo. The solar cell industry has grown very rapidly in the past few years and now uses more silicon than the entire integrated circuit industry. The rapid expansion has pushed up the price of raw crystalline silicon feed stock from under $20/kg to over $200/kg.

Fig1. Silicon scrap comes from a wide variety of sources. One source is off cuts and scrap material from the semiconductor industry.

Fig2. Wafer scraps from the production line are recycled for growing new ingots

3. Growing ingots

The ingot growth for Multicrystalline silicon is quite simple, melt the silicon in a large crucible and let it cool slowly to form large crystal. The specifics of furnace design allow the ingot to cool slowly so that very large grains (> 1 cm) are formed.

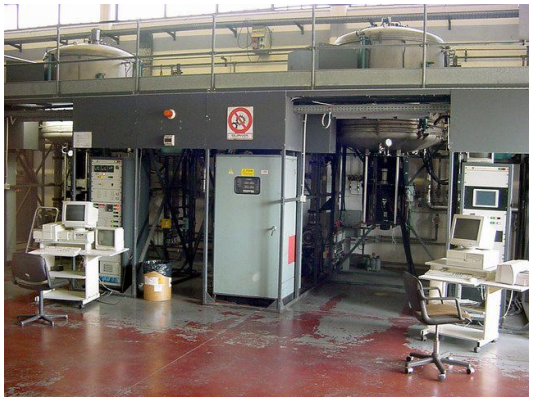


Fig 3. Tub used for growing silicon. The dimensions are about 50 cm x 50 cm x 25 cm deep. The tub has to withstand the melting point of silicon at 1415 °C. For comparison iron melts at 1538 °C.
Fig 4. Crystal growing furnaces. The system is loaded and unloaded using the hoists at the bottom

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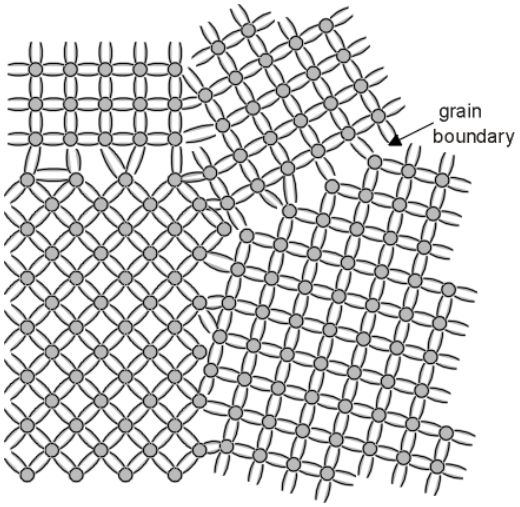
Fig 5. Loading the growth tub into the furnace.

3.1 Multicrystalline Silicon

Techniques for the production of multicrystalline silicon are simpler, and therefore cheaper, than those required for single crystal material. However, the material quality of multicrystalline material is lower than that of single crystalline material due to the presence of grain boundaries. Grain boundaries introduce high localized regions of recombination due to the introduction of extra defect energy levels into the band gap, thus reducing the overall minority carrier lifetime from the material. In addition, grain boundaries reduce solar cell performance by blocking carrier flows and providing shunting paths for current flow across the p-n junction.

To avoid significant recombination losses at grain boundaries, grain sizes on the order of at least a few millimetres are required (Card, Yang). This also allows single grains to extend from front to back of the cell, providing less resistance to carrier flow and generally decreasing the length of grain boundaries per unit of cell. Such multicrystalline material is widely used for commercial solar cell production.



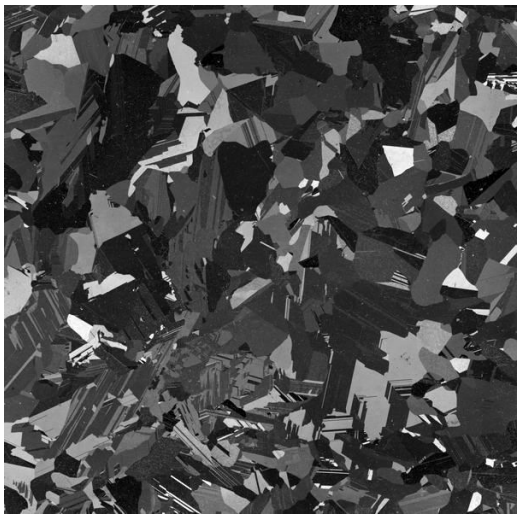


Fig 6. At the boundary between two crystal grains, the bonds are strained, degrading the electronic properties.
Fig 7. A 10 x 10 cm2 multicrystalline wafer. The wafer has been textured so that grains of different orientation show up as light and dark.

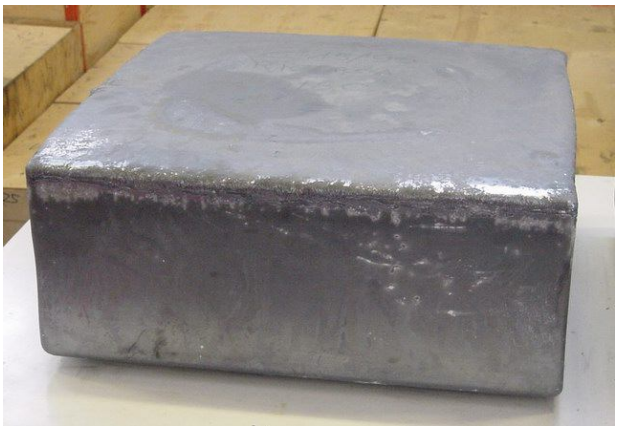


Fig 8. Finished silicon ingot.

4. Sawing the Ingot into Bricks

Once an ingot has been grown it is then sliced up into wafers. In the case of the multicrystalline silicon,

large slabs are grown which are then sliced up into smaller ingot blocks.

Fig 9.The large silicon ingot is sawn into more managable bricks.
Fig 10.The individual bricks now ready to saw up into wafers

5. Wafer Slicing

Slicing up the bricks into wafers is a delicate operation. Each wafer is up to 15 x 15 cm2 and under a third of a mm (300 µm) thick. Modern solar cell factories use wire saws rather than the internal diameter blade saws previously used for the semiconductor industry. In fact, the semiconductor industry is now moving to the wire saw due to their superior technology.

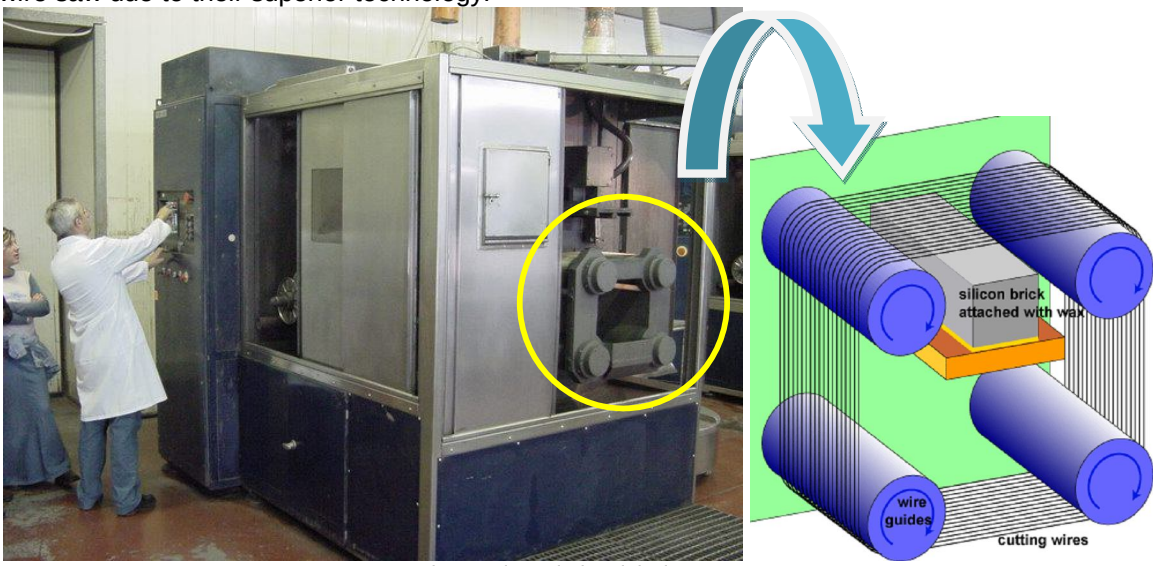


Fig11. A large industrial wire saw.

The wire sawing is is done on the right hand side but the bricks are not loaded yet. The left hand side holds the wire and the control circuitry.The wires are covered with slurry and are wound around the drums. When running the drums spin at high speed and the silicon bricks are pushed down from the top. . The feed wire is just visible coming in the top left of the spool.

6. Texturing

Cutting silicon into wafers leaves the surface covered with cutting slurry and the surface is damaged due to the action of the saw. Wafers are cleaned in a hot solution of sodium hydroxide that removes the surface contamination and the first 10 μm of damaged silicon. The wafers are then textured in a more dilute solution of sodium hydroxide with isopropanol as a wetting agent. For multicrystalline wafers, acidic texturing is often used as it gives a more uniform etch rate across gain boundaries.
After the wafers are cut into slices they are then put into cassettes for saw damage removal and texturing

Fig 12. Wafers during the texturing process.

The cassettes are further loaded into holders for moving through the production line. During the texturing process hydrogen is released and bubbles adhere to the wafer. The mesh place on top of the cassettes stops the wafers from floating out of the cassettes. Normally there is a protective blind in place to prevent sodium hydroxide splashes. The protective blind rolls back and the wafers are removed from the texturing bath. Wafers are put through several rinse cycles and an acid rinse to neutralize the sodium hydroxide. Finally the wafers are loaded into a centrifuge for a final rinse and spin dry.

7. Orientation and Doping

In single crystalline silicon material the crystal orientation is defined by Miller indices. A particular crystal plane is noted using parenthesis such as (100). Silicon has a cubic symmetrical cubic structure and so (100), (010) etc are equivalent planes and collectively referred to using braces {100}. Similarly, the crystal directions are defined using square brackets, e.g. [100] and referred collectively using triangular brackets, <100>.

In solar cells the preferred orientation is <100> as this can be easily textured to produce pyramids that reduce the surface reflectivity. However, some crystal growth processes such as dendritic web <111> produce material with other orientations.

To denote the crystal directions, single crystal wafers often have flats to denote the orientation of the wafer and the doping. The most common standard is the SEMI standard:

* If the minor flat is 180° from the major flat the wafer is n-type <100>
* If the minor flat is 90° to the left or right the wafer is p-type <100>.
* If the minor flat is 45° up on the left or right the wafer is n-type <111>
* If there are no minor flats the wafer is p-type <111>

7.1 Emitter Diffusion

The emitter diffusion process is performed in a variety of ways. In this case a phosphorous containing coating is applied to the surface. The wafers are then put in a belt furnace to diffuse a small amount of phosphorous into the silicon surface.

Fig 13. Loading the phosphorous coating.

The trend in production lines is to have as much automation as possible and to move the wafers through the lines on a belt. The loading and unloading of cassettes is a major source of yield loss.

Fig 14. Wafers moving from the diffusion coating furnace to the high temperature diffusion furnace.

The wafers travel through the diffusion furnace for roughly an hour.

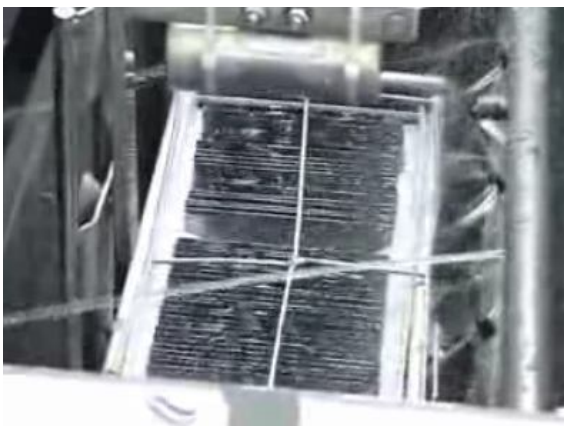


Fig15 and Fig 16 show cassettes and rinsing

Finally the wafers are loaded into a centrifuge for a final rinse and spin dry. After the diffusion process the wafers are loaded back into cassettes for an acid etch to remove the diffusion glass.

8. Plasma Edge Isolation

The edge isolation process removes the phosphorous diffusion around the edge of the cell so that the front emitter is electrically isolated from the cell rear. A common way to achieve this is to stack the wafers on top of each other then plasma etch using CF_4 and O_2

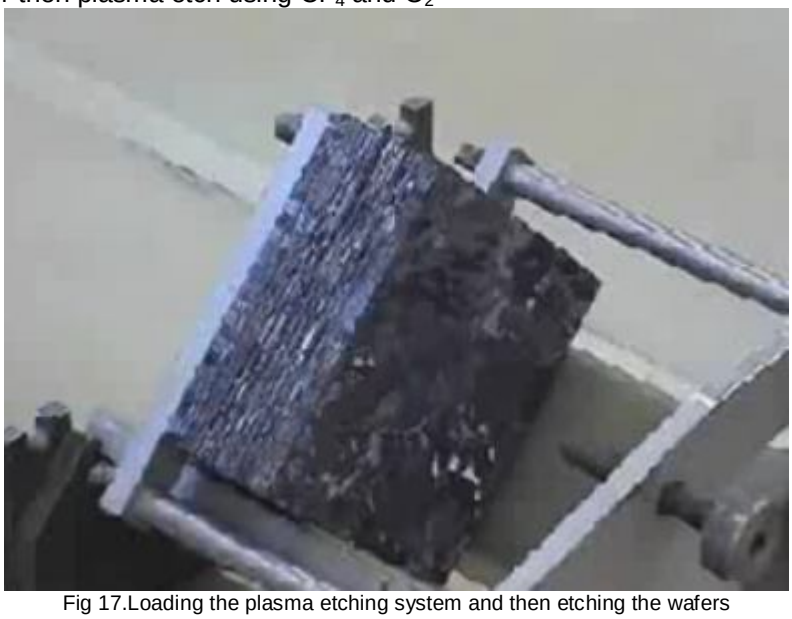


Fig 17.Loading the plasma etching system and then etching the wafers

9. Anti-Reflection Coating

An antireflection of silicon nitride is typically deposited using chemical vapor deposition process (CVD). Precursor gases of silane (SiH4) and ammonia (NH3) are fed into a chamber and break down due to temperature (LPCVD) or due to a plasma enhancement (PECVD). Other systems use microwaves to cause the silane/ammonia reaction to take place. The complete reaction is:

3SiH4 + 4NH3 -> Si3N4 + 12H2

but the usual reaction to produce a non-stoichiometric film with the incorporation of large amounts of hydrogen (SixNy:H).

Older cell designs use titanium dioxide (TiO2), which provides a good antireflection coating and is simpler to apply but does not provide surface or bulk passivation.

Fig 18.Wafers being deposited with silicon nitride antireflection coating giving a blue color.
Fig 19. A full view of the anti-reflection coating machine from loading to unloading

10. Screen-Print Front

Silver paste is forced through a patterned screen. Those areas with gaps in the pattern leave a metal pattern on the surface.

Fig 20 and Fig 21. Screen printer in operation.

The cells move along a conveyor belt. Here they enter on the right and exit on the left. Close up of the screen printing operation. The cells are undernearth the printer so are not visible from the top. After printing the paste is still wet and is easily smudged.

Fig 22 shows the wafers are loaded into a drier to evaporate off the organic binders in the paste. Driers operate at a low temperature of around 200 °C.

Fig 23. Front screen

After the wafers are dried they are loaded back onto the conveyor belt to continue their movement in through the production line. Zooming in on a cell after the front screen print is finished. At this stage, the silver still exists as a powder resting on the cell. Later firing process at high temperature bonds the silver to the silicon.

11. Screen-Print Rear

The rear is printed in two parts.

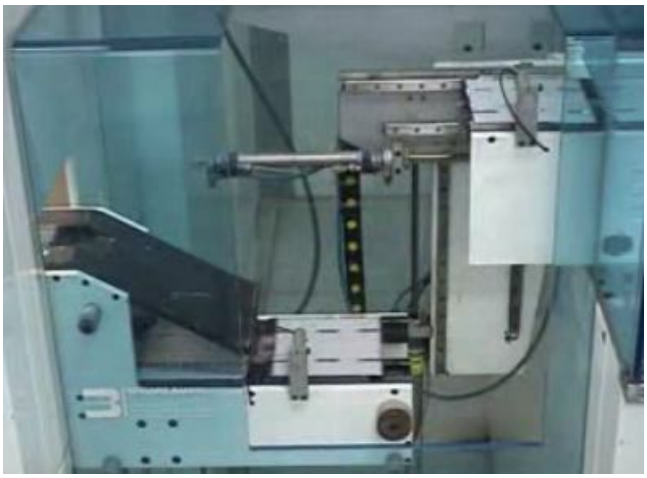
Fig.24, 25, 26 Printing the aluminum paste on the rear. The cell is just visible through the screen as it moves throughout the line.

After the front print is complete the cells are flipped over to print on the rear. The aluminum printing is an expensive step since it is very thick and covers almost the whole cell.

Fig 27.Drying the aluminum paste.

Careful handling is essential since aluminum is a p-type dopant and any paste smudges that get on the front of the cell will shunt the cell completely.

12. Screen-Print Rear Silver



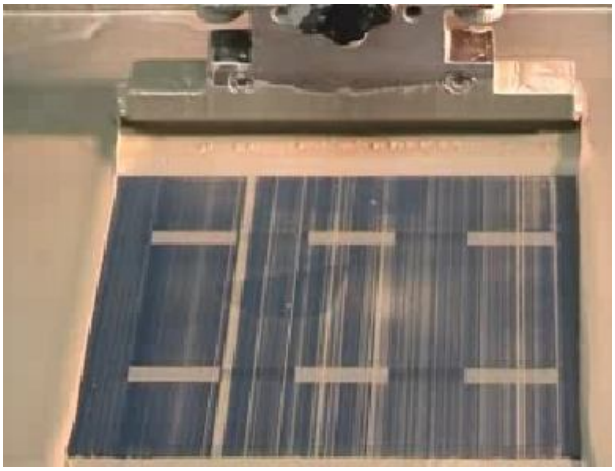


Fig 28.Transferring wafers from to the final screen printer.
Fig 29. Unloading the final dry process. Screen printing the silver on the rear.

Such automated transfer machinery greatly improves yield - a factor almost as important as efficiency in a commercial process.

13. Firing

Fig 30.Firing the metal loading and unloading

14. Testing

Testing the cells and putting them into modules

Fig 31. View of the tester loader from the other side.

Fig 32. The tester

Fig 33. Actual tester during operation, after the cells are tested they are sorted into bins

15. Module Manufacture

Individual solar cells are protected from the weather by encapsulating into a module. Each cell is only around 0.5 volts, to obtain sufficient voltage the cell are connected together in series using flat wires called tabs.