ELEG 312 Homework #4 Solutions

Problems 9.61, 9.73, 9.74, 9.77, 9.81, and 9.82

Problem 9.61

The differential amplifier circuit of Fig. P9.61 utilizes a resistor connected to the negative power supply to establish the bias current I.

(a) For $v_{B1} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{id}|$.

(b) For $v_{B1} = v_{B2} = v_{icm}$, where v_{icm} has a zero average, find the magnitude of the common-mode gain, $|v_o/ v_{icm}|$.

(c) Calculate the CMRR.

(d) If v_{B1} = 0.1 sin(2π×60t) + 0.005 sin(2π×1000t), volts, and v_{B2} = 0.1 sin (2π×60t) − 0.005 sin(2π×1000t), volts, find v_o.

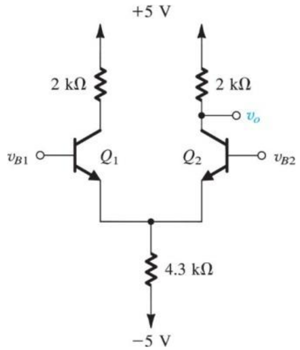


Figure P9.61

$$V_{B1} = V_{B2} = 0\text{V} \qquad V_E = V_B - V_{BE} = 0\text{V} - 0.7\text{V} = -0.7\text{V}$$

$$I = \frac{V_E - V_{EE}}{R_E} = \frac{-0.7\text{V} + 5\text{V}}{4.3\text{k}\Omega} = \frac{4.3\text{V}}{4.3\text{k}\Omega} = 1\text{mA}$$

$$I_{E1} = I_{E2} = \frac{I}{2} = \frac{1\text{mA}}{2} = 0.5\text{mA}$$

Problem 9.61a

The differential amplifier circuit of Fig. P9.61 utilizes a resistor connected to the negative power supply to establish the bias current *I*.

(a) For $v_{B1} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $|v_o/v_{id}|$.

$$I_{E1} = I_{E2} = \frac{I}{2} = \frac{1\text{mA}}{2} = 0.5\text{mA}$$

$$r_{e1} = r_{e2} = \frac{V_T}{I_E} = \frac{25\text{mV}}{0.5\text{mA}} = 50\Omega$$

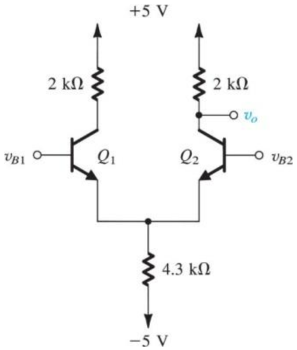


Figure P9.61

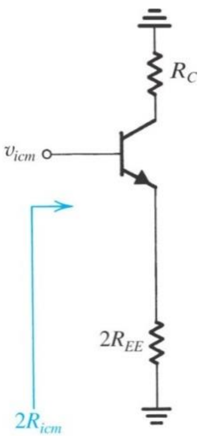
$$A_d \equiv \frac{v_o}{v_{id}} = \alpha \frac{\text{total resistance across } v_o}{\text{total emitter resistance}} = \alpha \frac{R_C}{r_{e1} + r_{e2}} \simeq \frac{2\text{k}\Omega}{0.1\text{k}\Omega} = 20\frac{\text{V}}{\text{V}}$$

Problem 9.61b,c

The differential amplifier circuit of Fig. P9.61 utilizes a resistor connected to the negative power supply to establish the bias current I.

(b) For $v_{B1} = v_{B2} = v_{icm}$, where v_{icm} has a zero average, find the magnitude of the common-mode gain, $|v_o/v_{icm}|$.

(c) Calculate the CMRR.



$$A_{cm} \equiv \frac{v_o}{v_{icm}} = \alpha \frac{\text{total resistance across } v_o}{\text{total emitter resistance}}$$

$$= -\alpha \frac{R_C}{2R_{SS} + r_{e2}} \simeq \frac{-2\text{k}\Omega}{8.6\text{k}\Omega + 0.05\text{k}\Omega}$$

$$= -0.23\frac{\text{V}}{\text{V}}$$

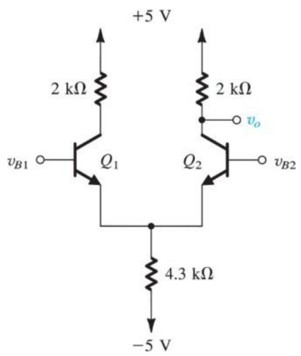


Figure P9.61

$$CMRR = 20\log\left(\frac{|A_d|}{|A_{cm}|}\right) = 20\log\left(\frac{20\,\text{V/V}}{0.23\,\text{V/V}}\right) = 38.8\text{dB}$$

Problem 9.61d

The differential amplifier circuit of Fig. P9.61 utilizes a resistor connected to the negative power supply to establish the bias current I.

(d) If v_{B1} = 0.1 sin(2π×60t) + 0.005 sin(2π×1000t), volts, and v_{B2} = 0.1 sin (2π×60t) − 0.005 sin(2π×1000t), volts, find v_o.

v_{icm} = 0.1 sin(2π×60t)

v_{B2} = 2×0.005 sin(2π×1000t) = 0.01 sin(2π×1000t)

$$A_{cm} = -0.23\frac{\text{V}}{\text{V}}$$

$$A_d = 20\frac{\text{V}}{\text{V}}$$

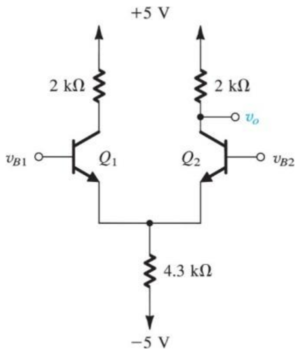


Figure P9.61

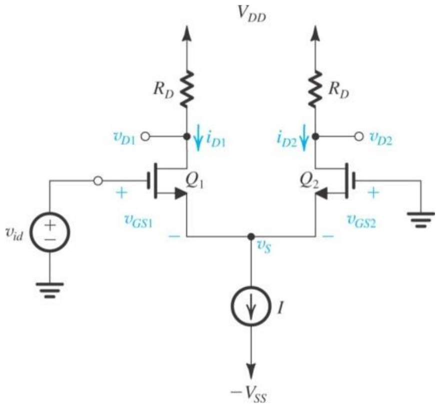
$$\Rightarrow v_o = A_{cm}v_{icm} + A_d v_{id}$$

$$= (-0.23)\big(0.1\sin(2\pi 60t)\big) + (20)\big(0.01\sin(2\pi 1000t)\big)$$

$$= -0.023\sin(2\pi 60t) + 0.2\sin(2\pi 1000t)$$

Problem 9.73a

An NMOS differential pair operating at a bias current I of 100 µA uses transistors for which k'_n = 200 uA/V^2 and W/L = 10. Find the three components of input offset voltage under the conditions that $\Delta R_D/R_D$ = 4%, $\Delta(W/L)/(W/L)$ = 4%, and ΔV_t = 5 mV. In the worst case, what might the total offset be? For the usual case of the three effects being independent, what is the offset likely to be?



$$I_{D1} = I_{D2} = \frac{I}{2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2$$

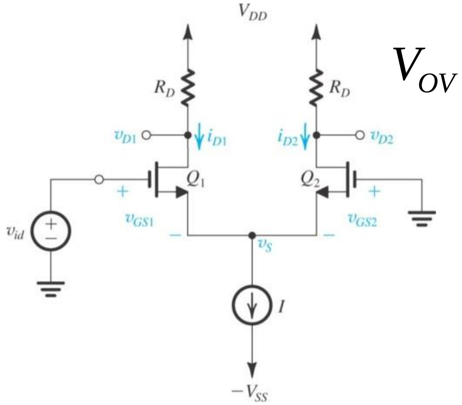
$$V_{OV} = \sqrt{I / \left[k_n' (W/L)\right]} = \sqrt{\frac{0.1\text{mA}}{0.2\frac{\text{mA}}{\text{V}^2}(10)}} = 0.224\text{V}$$

$\Delta R_D/R_D = 4\%$

$$V_{OS} = \frac{V_O}{A_d} = \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta R_D}{R_D}\right) = \left(\frac{0.224\text{V}}{2}\right)(0.04) = 4.5\text{mV}$$

Problem 9.73b

An NMOS differential pair operating at a bias current I of 100 μA uses transistors for which k'_n = 200 uA/V^2 and W/L = 10. Find the three components of input offset voltage under the conditions that $\Delta R_D/R_D$ = 4%, $\Delta(W/L)/(W/L)$ = 4%, and ΔV_t = 5 mV. In the worst case, what might the total offset be? For the usual case of the three effects being independent, what is the offset likely to be?



$$V_{OV} = 0.2\text{V}$$

$\Delta(W/L)/(W/L)$ = 4%

$$V_{OS} = \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta(W/L)}{(W/L)}\right) = \left(\frac{0.224\text{V}}{2}\right)(0.04) = 4.5\text{mV}$$

ΔV_t = 5 mV

$$V_{OS} = \Delta V_t = 5\text{mV}$$

worst case offset: $V_{OS} = V_{OS\Delta R} + V_{OS\Delta(W/L)} + V_{OS\Delta V_t} = 4.5\text{mV} + 4.5\text{mV} + 5\text{mV} = 14\text{mV}$

likely offset: $V_{OS} = \sqrt{V_{OS\Delta R}^2 + V_{OS\Delta(W/L)}^2 + V_{OS\Delta V_t}^2} = \sqrt{(4.5\text{mV})^2 + (4.5\text{mV})^2 + (5\text{mV})^2} = 8.1\text{mV}$

Problem 9.74

A bipolar differential amplifier uses two well-matched transistors but collector load resistors that are mismatched by 10%. What input offset voltage is required to reduce the differential output voltage to zero?

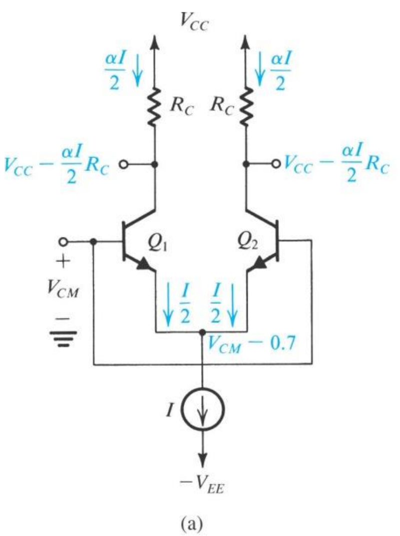


Figure 8.16: Different modes of operation of the BJT differential pair: **(a)** the differential pair with a common-mode input voltage V_{CM}.

$$V_O = V_{C2} - V_{C1} = \alpha\left(\frac{I}{2}\right)\Delta R_C \qquad A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_C$$

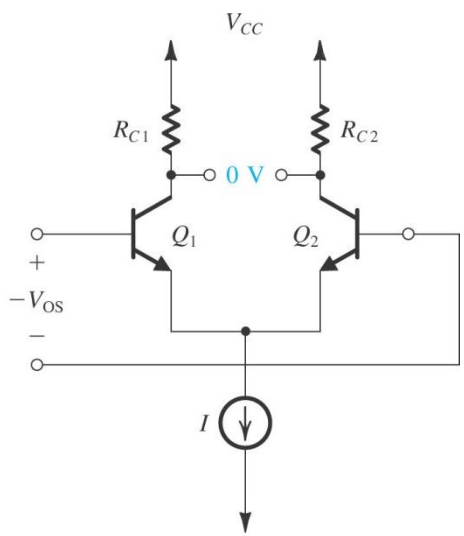
$$V_{OS} = \frac{V_O}{A_d} = \frac{\alpha \frac{I}{2} \Delta R_C}{g_m R_C} \qquad g_m = \frac{I_C}{V_T} = \frac{\alpha I_E}{V_T} \rightarrow V_T = \frac{\alpha I_E}{g_m}$$

$$V_{OS} = \frac{\alpha I_E}{g_m}\left(\frac{\Delta R_C}{R_C}\right) = V_T\left(\frac{\Delta R_C}{R_C}\right)$$

$$\left|V_{OS}\right| = V_T\left(\frac{\Delta R_C}{R_C}\right) = 25\text{mV}\left(0.1\right) = 2.5\text{mV}$$

Problem 9.77a

A differential amplifier uses two transistors whose β values are β_1 and β_2. If everything else is matched, show that the input offset voltage is approximately $V_T[(1/\beta_1)-(1/\beta_2)]$. Evaluate V_{OS} for $\beta_1 = 50$ and $\beta_2 = 100$. Assume the differential source resistance to be zero.



(b)

$$V_{C1} = V_{CC} - \frac{\alpha_1 I}{2} R_C \qquad V_{C2} = V_{CC} - \frac{\alpha_2 I}{2} R_C$$

$$V_O = V_{C2} - V_{C1} = (\alpha_1 - \alpha_2)\left(\frac{IR_C}{2}\right)$$

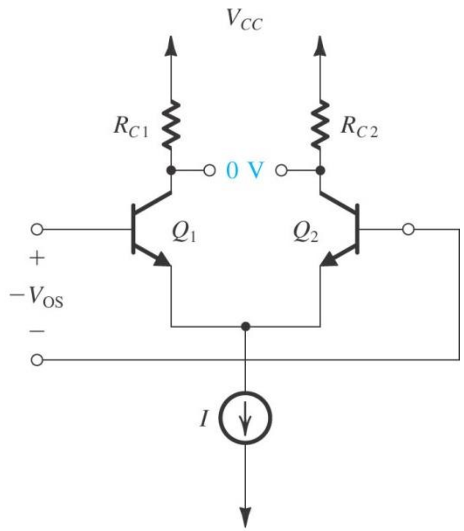
$$V_O = \left(\frac{IR_C}{2}\right)\left(\frac{\beta_1}{\beta_1+1} - \frac{\beta_2}{\beta_2+1}\right) = \left(\frac{IR_C}{2}\right)\left(\frac{\beta_1-\beta_2}{\beta_1\beta_2+\beta_1+\beta_2+1}\right)$$

$$V_O \simeq \left(\frac{IR_C}{2}\right)\left(\frac{\beta_1-\beta_2}{\beta_1\beta_2}\right) = \left(\frac{IR_C}{2}\right)\left(\frac{1}{\beta_2} - \frac{1}{\beta_1}\right)$$

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2}-v_{o1}}{v_{id}} = g_m R_C = \left(\frac{\alpha I/2}{V_T}\right) R_C$$

Problem 9.77b

A differential amplifier uses two transistors whose β values are β_1 and β_2. If everything else is matched, show that the input offset voltage is approximately $V_T[(1/\beta_1)-(1/\beta_2)]$. Evaluate V_{OS} for $\beta_1 = 50$ and $\beta_2 = 100$. Assume the differential source resistance to be zero.



(b)

$$V_O = \left(\frac{IR_C}{2}\right)\left(\frac{1}{\beta_2}-\frac{1}{\beta_1}\right) \qquad A_d = g_m R_C = \left(\frac{\alpha I/2}{V_T}\right)R_C$$

$$V_{OS} \equiv \frac{V_O}{A_d} = \frac{\left(\frac{IR_C}{2}\right)\left(\frac{1}{\beta_1}-\frac{1}{\beta_2}\right)}{\left(\frac{\alpha I/2}{V_T}\right)R_C} = \frac{V_T}{\alpha}\left(\frac{1}{\beta_1}-\frac{1}{\beta_2}\right) \simeq V_T\left(\frac{1}{\beta_1}-\frac{1}{\beta_2}\right)$$

$$V_{OS} = V_T\left(\frac{1}{\beta_2}-\frac{1}{\beta_1}\right) = 25\text{mV}\left(\frac{1}{100}-\frac{1}{50}\right) = -250\mu\text{V}$$

Problem 9.81a

One approach to "offset correction" involves the adjustment of the values of R_{C1} and R_{C2} so as to reduce the differential output voltage to zero when both input terminals are grounded. This offset-nulling process can be accomplished by utilizing a potentiometer in the collector circuit, as shown in Fig. P9.81. We wish to find the potentiometer setting, represented by the fraction x of its value connected in series with R_{C1}, that is required for nulling the output offset voltage that results from:

(a) R_{C1} being 4% higher than nominal and R_{C2} 4% lower than nominal

(b) Q_1 having an area 5% larger than nominal, while Q_2 has area 5% smaller than nominal.

$$R_{C1} + (x \times 1\text{k}\Omega) = R_{C2} + [(1-x) \times 1\text{k}\Omega]$$

$$(5\text{k}\Omega \times 1.04) + (x \times 1\text{k}\Omega) = (5\text{k}\Omega \times 0.96) + 1\text{k}\Omega - (x \times 1\text{k}\Omega)$$

$$2(x \times 1\text{k}\Omega) = 4.8\text{k}\Omega - 5.2\text{k}\Omega + 1\text{k}\Omega = 0.6\text{k}\Omega$$

$$x = 0.3$$

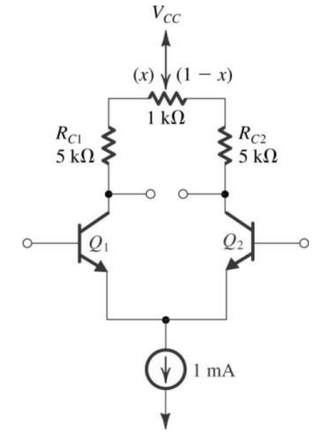


Figure P9.81

Problem 9.81b

One approach to "offset correction" involves the adjustment of the values of R_{C1} and R_{C2} so as to reduce the differential output voltage to zero when both input terminals are grounded. This offset-nulling process can be accomplished by utilizing a potentiometer in the collector circuit, as shown in Fig. P9.81. We wish to find the potentiometer setting, represented by the fraction x of its value connected in series with R_{C1}, that is required for nulling the output offset voltage that results from:

(b) Q_1 having an area 5% larger than nominal, while Q_2 has area 5% smaller than nominal.

$$I_{C1}\left[R_C + \left(x \times 1\text{k}\Omega\right)\right] = I_{C2}\left[R_C + \left(1 - x\right) \times 1\text{k}\Omega\right]$$

$$I_{C1} = \alpha I_{E1} \simeq 1.05 I_C = 1.05\left(0.5\text{mA}\right) = 0.525\text{mA}$$

$$I_{C2} \simeq \alpha I_{E2} = 0.95 I_C = 0.95\left(0.5\text{mA}\right) = 0.475\text{mA}$$

$$x \times 1\text{k}\Omega = \frac{I_{C2}\left(5\text{k}\Omega + 1\text{k}\Omega\right) R_C - \left(I_{C1} \times 5\text{k}\Omega\right)}{\left(I_{C1} + I_{C2}\right)} = \frac{2.85\text{V} - 2.625\text{V}}{1\text{mA}} = .225\text{k}\Omega$$

$$x = 0.225$$

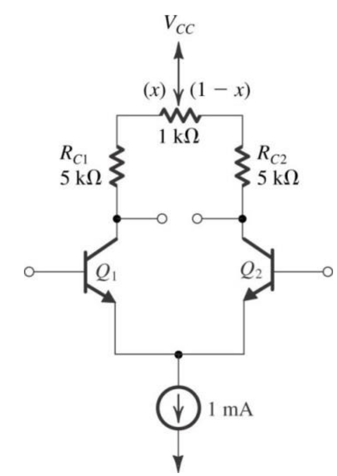


Figure P9.81

Problem 9.82a

A differential amplifier for which the total emitter bias current is 400 μA uses transistors for which β is specified to lie between 80 and 200. What is the largest possible input bias current? The smallest possible input bias current? The largest possible input offset current?

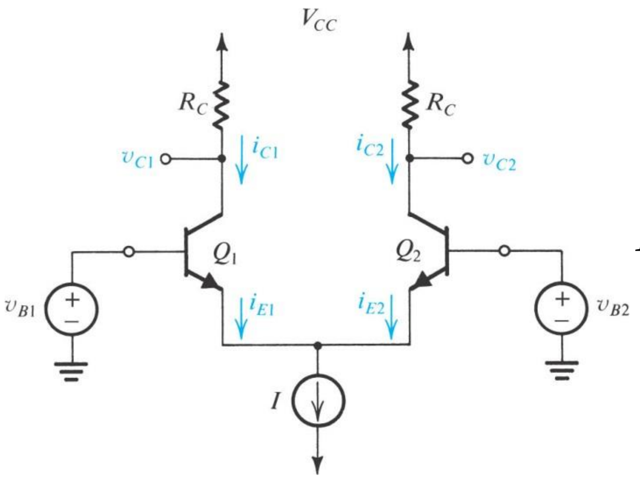


Figure 9.14: The basic BJT differential-pair configuration.

$$I_{B\max} = \frac{I}{2}\frac{1}{\beta+1+\Delta\beta/2} = \frac{I}{2}\frac{1}{\beta_{\min}+1} = \frac{400\mu\text{A}}{2}\frac{1}{80+1} = 2.5\mu\text{A}$$

$$I_{B\min} = \frac{I}{2}\frac{1}{\beta+1+\Delta\beta/2} = \frac{I}{2}\frac{1}{\beta_{\max}+1} = \frac{400\mu\text{A}}{2}\frac{1}{200+1} = 1.0\mu\text{A}$$

$$I_{OS} = I_{B\max} - I_{B\min} = 1.5\mu\text{A}$$

$$I_{OS} = \frac{I}{2(\beta+1)}\left(\frac{\Delta\beta}{\beta}\right) = \frac{400\mu\text{A}}{2(140+1)}\left(\frac{120}{140}\right) = 1.22\mu\text{A}$$