CPEG 422/622 Spring 2020

Homework 1

Due February 24th at midnight (through Canvas)
Put your name in the comment part of the code you submitted!

1. Analyze the 4-bit carry-ripple adder and the 4-bit carry look ahead (CLA) adder discussed in lecture 3, and fill in the following table about *gate count*.

	4-bit carry ripple adder	4-bit CLA adder
XOR gates		
AND gates		
OR gates		
Total gates		

2. Change the 4-bit carry-ripple adder VHDL code to implement a 4-bit carry look ahead (CLA) adder in the way described in lecture slides. Submit your VHDL code.