CPEG-323: Introduction to Computer Systems Engineering

Homework #1: Performance and Single cycle CPU (100 points)

Not a group assignment, you should work alone on this homework!

(Due on Nov. 9, in Class)

1. (40 points) Consider a single-cycle processor whose clock-cycle time is 15 ns.
   a. If the hardware is upgraded so that that ALU latency is decreased by 2 ns and the register file latency is decreased by 1 ns for reads and 1 ns for writes, how much faster would programs run on the new processor? Justify your answer.
   b. Two teams of students are optimizing a MIPS program for a single-cycle processor. Team A discovers that by unrolling loops, they can reduce the dynamic instruction count to 90% of the original value (despite increasing the static instruction count). Team B realizes that functions foo() and bar() account for 60% and 30% of the running time respectively. They are able to optimize the code so that the speedup for foo() is 1.5 times and the speedup for bar() is 1.2 times. Which team's optimizations are more effective? Justify your answer.

2. (30 points) Consider the single-cycle datapath with the following component latencies: (note that the register file and memories have different latencies for reads and writes.)

Functional Unit	**Time (ns)**
Memory (read)	4
Memory (write)	12
ALU	8
Register File (read)	4
Register File (write)	7

   a) Which instruction (add, sw, lw, beq) will take the most time to execute on this single-cycle datapath, which components of the datapath will it use, in what order will it use them?

   b) Calculate the cycle time for a single cycle datapath.

3. (30 points) Single-cycle CPU implementation

We will implement a hypothetical instruction sw+ in the single-cycle pipeline. sw+ is a "store word, with post increment" that is found in some real architectures. It is encoded as an I-type instruction and performs the following operations:

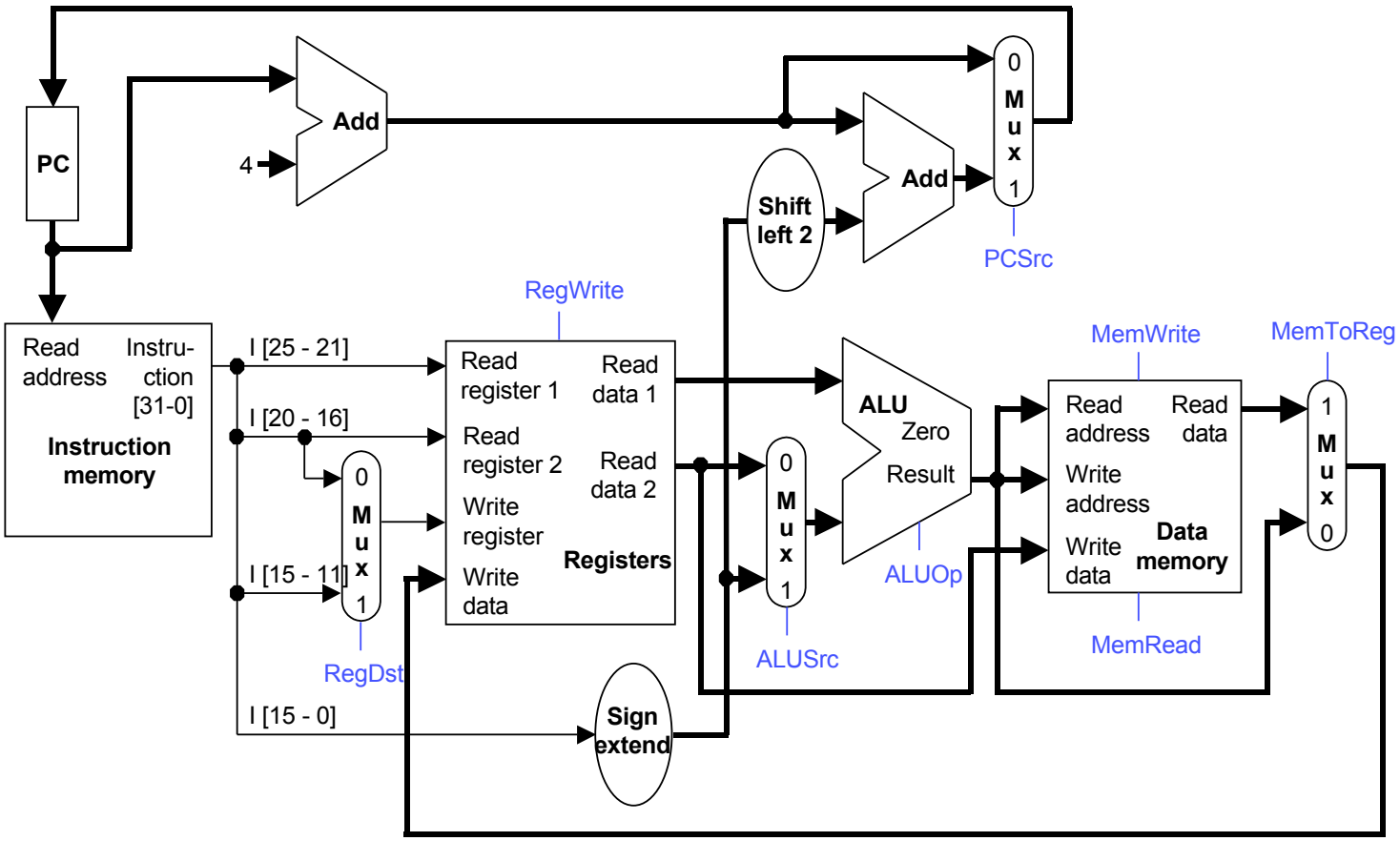
M[R[rs]] = R[rt]
R[rs] = R[rs] + imm

Field	op	rs	rt	imm
Bits	31-26	25-21	20-16	15-0

Part (a) The single-cycle datapath from the lecture is shown below. Show what changes are needed to support sw+ instruction. You should only add wires and muxes to the datapath; do no modify the main functional units themselves (the memory, register file and ALU). (20 points)

Note: Please make sure that the modification will no lengthen the clock cycle. Assume that ALU, Memory, and Register file all take 2ns, and everything else is instantaneous.

Part (b) On the diagram, write (next to the signal's name) values of all control signals required for the sw+ instruction. (10 points)


PC
Add
4
Add
Shift left 2
0
M
u
x
1
PCSrc
RegWrite
Read address
Instru-ction [31-0]
Instruction memory
I [25 - 21]
I [20 - 16]
I [15 - 11]
I [15 - 0]
0
M
u
x
1
RegDst
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
0
M
u
x
1
ALUSrc
ALU
Zero
Result
ALUOp
MemWrite
MemRead
Read address
Write address
Write data
Read data
Data memory
MemToReg
1
M
u
x
0
Sign extend