

CPEG 422/622 Spring 2020

Homework 2

**Demo due February 26th in class, code due February 26th through Canvas.
Put your name in the comment part of the code you submitted!**

1. Change the 4-bit carry-ripple adder VHDL code to implement a 4-bit adder/subtractor in the way described in lecture slides. Submit your VHDL code through Canvas.
2. Implement a 4-bit **subtractor** on the Zybo Z7-10 board. Use four LEDs (3 down to 0) for the 4-bit output. The 4-bit input A comes from four switches (3 down to 0), and the 4-bit input B comes from four buttons (3 down to 0). Submit your VHDL code and corresponding constraint file through Canvas, and bring your board to class for demo.