LAB1 – Inverter Tutorial: Schematic & Symbol Creation

Created for Peyman Barakhshan, CPEG460/660, Fall 2019, University of Delaware

Assumptions:

- -You have downloaded Cadence virtual machine and installed VMWARE on your computer.
 - Start Cadence VM and left-click on the connection icon in the lower-left corner. Select "VPN Connections" and then select "udel_common". This will connect you to the UDEL VPN server allowing you to run Cadence software.



Once done, right click anywhere on the desktop and choose Terminal

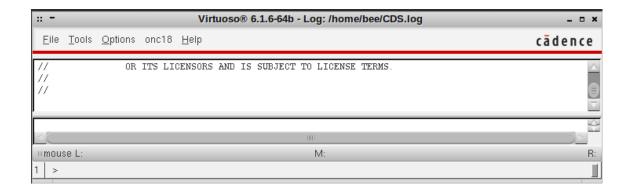


2. Start Cadence using the open terminal:

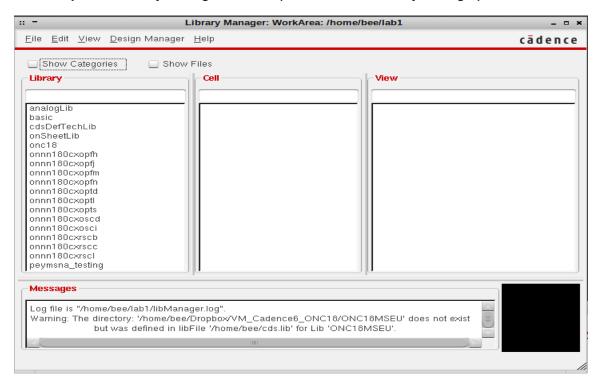
\$ virtuoso &

If you get the following window, scroll down and press ok Process Option Tool _ O X Fixed Options Variable Options Disabled - c12lm - metal1/2 c1ndr - ndrift (for nld15v3va device only) c1dnw - dnw Disabled - c13lm - metal1/2/3 c1lmc - linear MOSCAP c1lvt - LVT (low Vt) devices (1.8V/3.3V with Flow 1 and 1 Enabled - c1d3 - 1.8V/3.3V Devices c1npr - n-poly resistor Disabled - c1d5 - 1.8V/5V Devices c1ltc - low temp co resistor c1pphr - hi poly resistor Disabled - c1hv18 - 1.8V/5V/18V & HV 18V c1rdl - Flip chip - RDL c1esd - ESD mask Disabled - c1hv30 - HV 30V devices c1z5 - 5V zener Disabled - c1i45 - 1.8V/3.3V & I4T HV 30V/45V c1hal1 - Hall sensor c1bond - bond external assembly house Disabled - c1i70 - 1.8V/3.3V & I4T HV 30V/45V/70V o c1npp - no planar passivation Disabled - c1iln - 3.3V & I4T Lean c1pp - planar passivation (allows vp) c1ppt - planar passivation-thick (allows vpt) Disabled - c1lvt5 - LVT (low Vt) 5V devices Disabled - c1p100 - pocket to pocket breakdown voltage < 100V o c1svt - standard Vt:G c1hvt - high Vt:LL Disabled - c1p120 - pocket to pocket breakdown voltage < 120V o1shvt - standard and high Vt:GLL Enabled - c1s2 - 1.8V Devices c1nmim - no MIM capacitor c1mim - std MIM capacitor Enabled - c1s3 - 3.3V Devices c1hmim - high capacitive MIM c1smim - Stacked MIM (w/ 5LM or 6LM only) Disabled - c1s5 - 5V Devices c14lm - metal1/2/3/4 Disabled - c1uhvt - ultra high Vt:ULL c15lm - metal1/2/3/4/5 Disabled - c1xvt - XVT (intermediate Vt) 5V devices o16lm - metal1/2/3/4/5/6 Disabled - c1z5p5 - 5.5V zener c1t08 - 0.8um Top Metal c1t30 - 3.0um Top Metal Send email to notify users of changes Cance

- After starting cadence, check the virtuoso window (screen shot is below). Double check the
 window and ensure that there are no error messages. Hint: Click on the scroll bar on the right
 to scroll up the window.
- If you see errors, or do not see the message above, ensure you have followed all of the steps above.



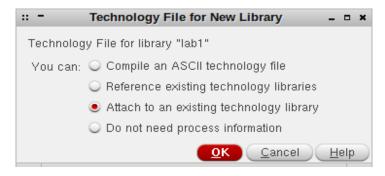
3. Open the library manager window (Select Tools->Library Manager)



- From the menu, select File -> New -> Library
- You will see the following dialog box:



In the "NAME" section type: Lab1 and click OK



- o In the next dialog box, select "Attach to existing tech library" section and click OK
- Confirm that the next dialog box is like below and click OK

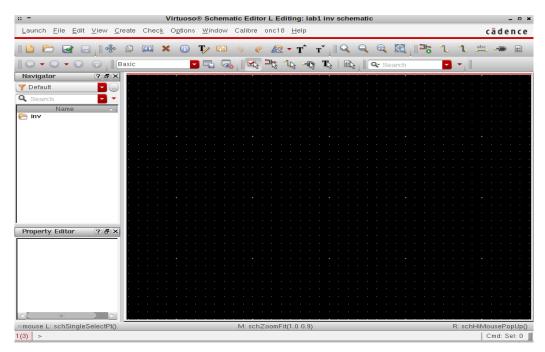


3. Creating a New Design:

- From the Library Manager, click on the "lab1" library you just created.
- From the menu, choose File → New → Cellview, and fill in the form as shown below in order to define a new schematic for our inverter.
- In the Library field, ensure lab1 is selected.
- In the Cell field, type "inv"
- From the **Type** selection drop down, choose "schematic"
- The View field will change to "schematic" automatically.
- Click OK



The Cadence Virtuoso Schematic Editor will appear with a black background.



4.1 Instancing parts to create the inverter:

- From the menu choose: Create->Instance (or press the letter lowercase i)
- Click the Browse button in the form. The Component Browser form appears.



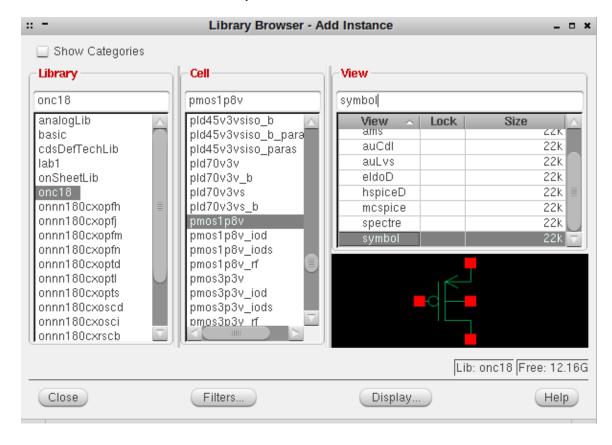
Select the following:

Under the Library selections:

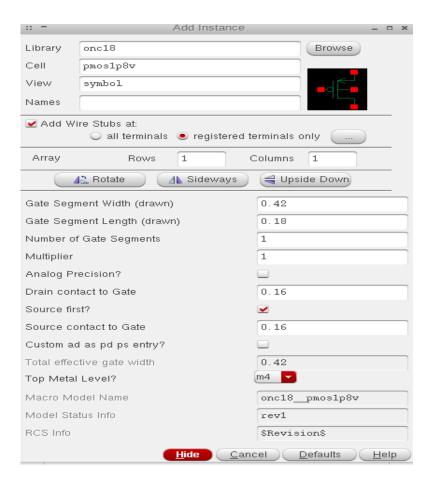
Under the *Library* column, select onc18.

Under the **Cell** column choose: **pmos1p8v** (this is the PMOS transistor)

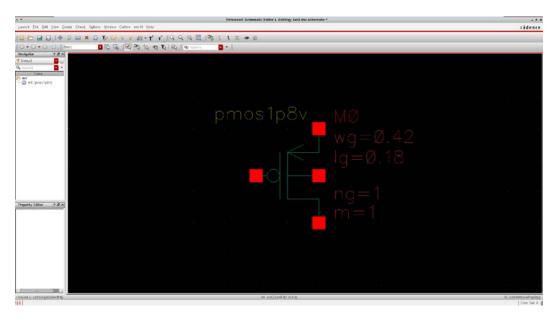
Under the View column choose: symbol.



Note that the **Add Instance** form has expanded to display various parameters for the pmos part. You can edit the pmos parameters (like it's width and length), but for now, do not change any parameters. We will use the default size for the 4 terminal PMOS, which is W/L = 0.42u/.18u

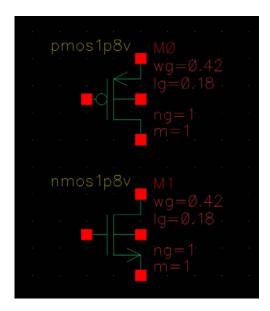


Click in the composer window to place the PMOS transistor. Your schematic should now look like this:

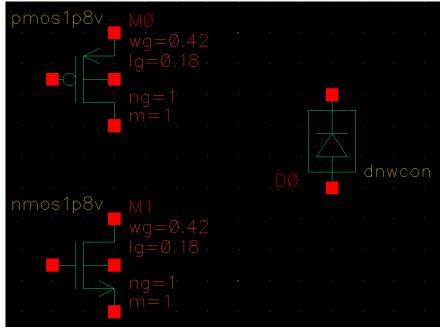


After you have placed the PMOS transistor, press <esc> to end "placement" mode.

- Add and nmos1p8v part (this is an NMOS transistor) using the same procedure. Leave the default W/L, do not modify any of the default parameters.
- Place the NMOS transistor below the PMOS transistor as shown here:



- Add one other part from the onc18 as indicated below:
 - o dnwcon
- Place it as shown:



• Press <esc> to end "placement" mode.

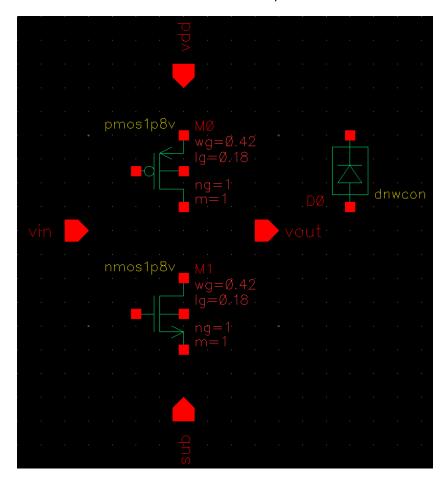
4.2 Adding the I/O Pins

- To add the input and output pins, choose: Create->Pin from the menu, or press the P key
- The **Add Pin** form appears.
- Under Pin Names, type the name of the pin: vdd sub vin

- Choose the Direction to be input



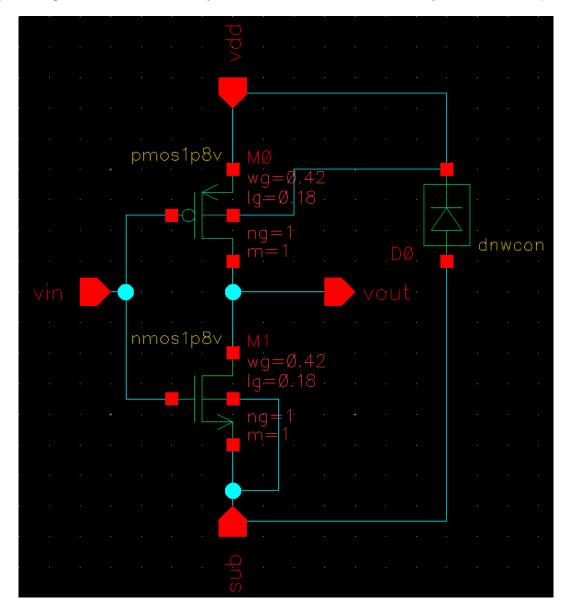
 Repeat the procedure to create an OUTPUT pin named: vout, see below (make sure you choose the DIRECTION to be "OUTPUT" on the add pin form:



4.3 Connecting Wires

- To connect wires, select **Add->Wire(narrow)** or press the w key.
- Click once where you want a wire to begin, click a second time where you want the wire to end.
- Wire the components as show below.

(Don't forget to wire the PMOS' body terminal to VDD and the NMOS' body terminal to GND.)



4.4 Checking and Saving

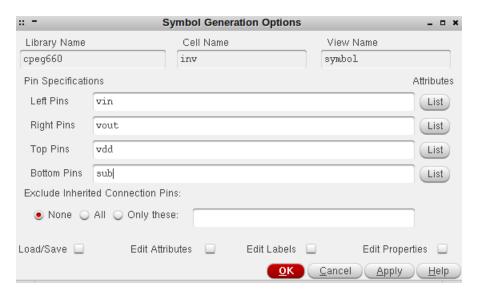
- To check and save the schematic, from the menu choose: File->Check and Save.
- Alternatively, you may click the checkmark icon on the left/top of the schematic editor.
- If Warning/Error appears, go back to the schematic and fix the problem as necessary. Warnings are not as crucial as Errors.
- Repeat until you have no Errors.
- Look in the virtuoso window (at the bottom) to ensure there are no errors.

5. Creating the Symbol Cell view

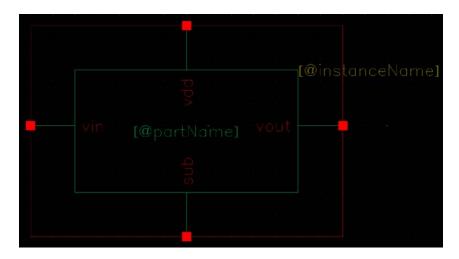
- Now we'll create a symbol (black box) to represent our circuit. The symbol Cellview will be created based on the already-available schematic Cellview. This is called *creating a Cellview* from the schematic view.
- From schematic editor's menu choose: Create→Cellview→From Cellview.
- Click OK on the form that appears, leaving all of the default values as shown below:



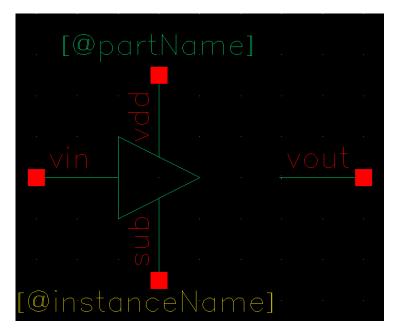
Do the following changes in the dialog box, and press OK



The "symbol editor" will open. You will see a green box surrounded by a white box. The input and output pins you defined in the schematic will appear as terminals. It is perfectly fine to use this rectangle as your symbol. But we will change the box into the symbol for an inverter, for use in future schematics.

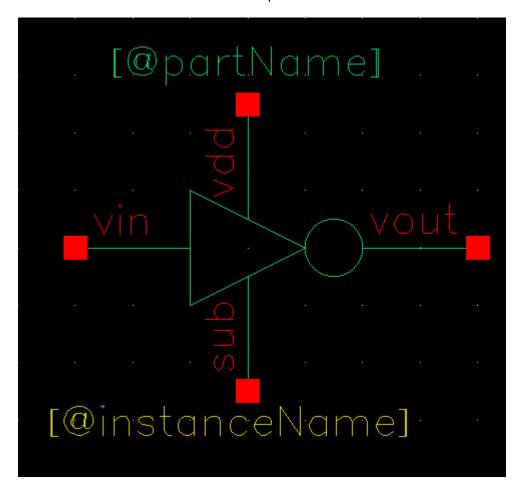


- press the **delete** key on the keyboard.
- click on the lower left hand corner of the green box.
- click on the lower left hand corner of the red box.
- press <esc> to end "delete mode"
- press the **m** key to enter "move mode"
- click on the [@partName] text and move it to the bottom of the drawing
- click on the [@instanceName] text and move it to the bottom of the drawing
- press <esc> to end "move mode"
- Select Create->Shape->polygon from the menu.
- draw a triangle as shown below (note: click where you want the verticies to be placed, do not "click and drag")



- press the <esc> key to end "polygon mode"
- Select Cretae->Shape->circle from the menu

- click on the schematic, where you wish the center of the circle to appear (see graphic below):
- click again when you have the proper radius.
- press the <esc> key to end "circle mode"
- move the red terminals and the text to be positioned as follows:



- click on the "save" icon from the top left hand toolbar
- close the symbol editor
- · close the schematic editor, saving any changes.

Note: If for any reason you have accidentally "deleted" one of the Red Pins, you must delete your symbol and start over again. You can delete the symbol from the Library Manager, by right clicking on the 'symbol' view for the "INV" cell, and choosing delete.

By creating the symbol, you have created a logical connection between the input/output pins of your schematic and this symbolic representation. In the next lab, we will use this symbol to test your schematic in a test bench.

What to turn in: Two pages - screen shot of your schematic and of the symbol.