VLSI PRACTICE EXAM 1
CPEG460/660 Fall 2019
October 8, 2019

NAME: _____

#	Problem (level of difficulty)	Points
1	Pass transistors (medium)	10
2	Sizing inverter chain (hard)	20
3	Scaling question (medium)	10
4	CMOS logic to schematic (easy)	10
5	CMOS schematic to logic (easy)	5
6	CMOS gate sizing for equal delays (easy)	10
7	Logical effort (hard)	20
8	From quiz or hw or lab	5
9	From quiz or hw or lab	5
10	From quiz or hw or lab	5

YOUR SCORE: _____ / 100

Helpful Formulas:

Method of Logical Effort

1) Compute path effort $F = GBH$
2) Estimate best number of stages $N = \log_4 F$
3) Sketch path with N stages
4) Estimate least delay $D = NF^{\frac{1}{N}} + P$
5) Determine best stage effort $\hat{f} = F^{\frac{1}{N}}$
6) Find gate sizes $C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$

Review of Definitions

Term	Stage	Path
number of stages	1	N
logical effort	g	$G = \prod g_i$
electrical effort	$h = \frac{C_{out}}{C_{in}}$	$H = \frac{C_{out\text{-}path}}{C_{in\text{-}path}}$
branching effort	$b = \frac{C_{on\text{-}path} + C_{off\text{-}path}}{C_{on\text{-}path}}$	$B = \prod b_i$
effort	$f = gh$	$F = GBH$
effort delay	f	$D_F = \sum f_i$
parasitic delay	p	$P = \sum p_i$
delay	$d = f + p$	$D = \sum d_i = D_F + P$

- Logical effort of common gates

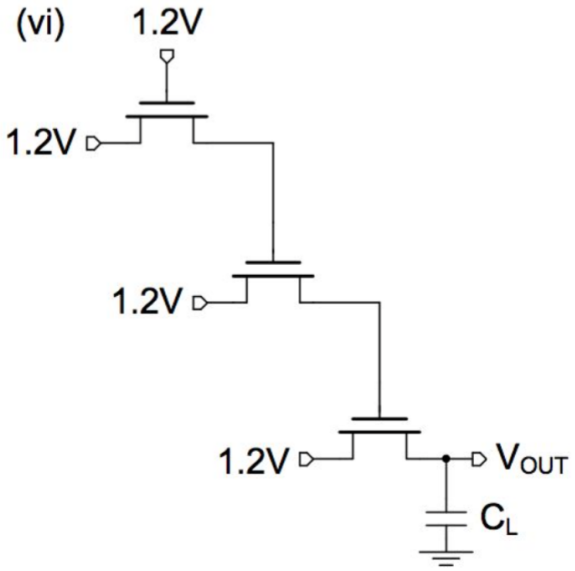
Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		4/3	5/3	6/3	(n+2)/3
NOR		5/3	7/3	9/3	(2n+1)/3
Tristate / mux	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

❑ Parasitic delay of common gates

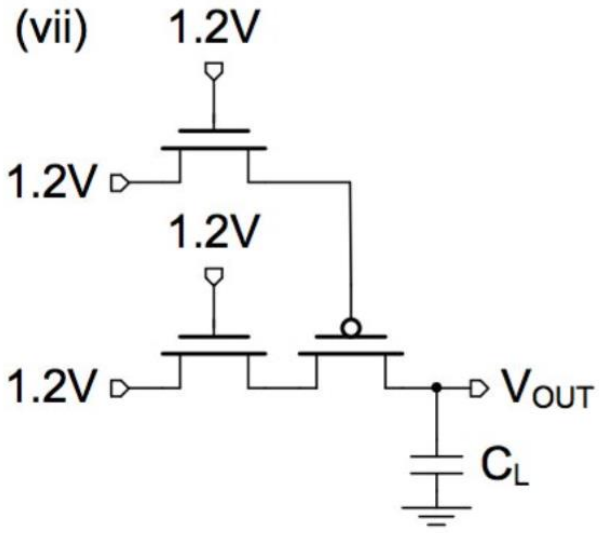
– In multiples of p_{inv} or 3RC (≈1)

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n
Tristate / mux	2	4	6	8	2n
XOR, XNOR		4	6	8	

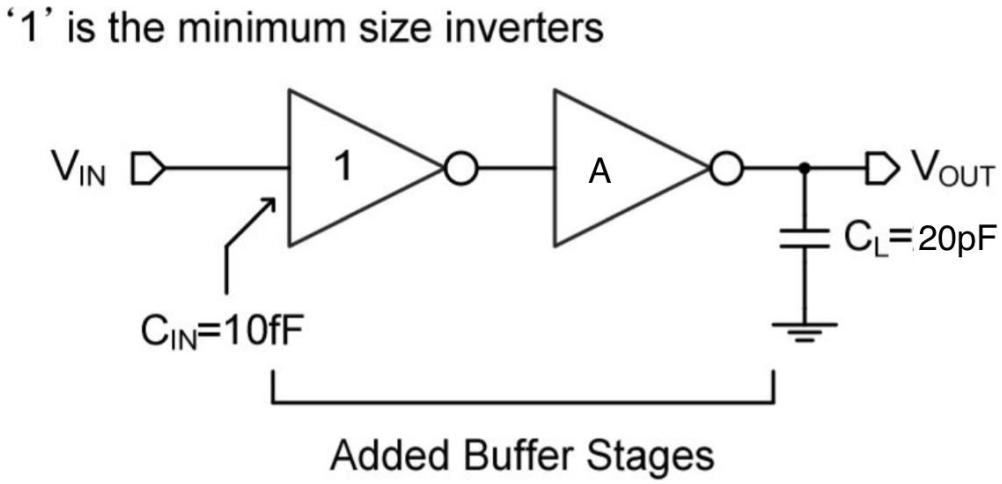
1. Find the voltage VOUT for in the figure below. Assume that VTN=|VTP|=0.3V, that and the output capacitor, CL, is initially discharged. All middle nodes are discharged initially. (10 pts)



(vii)



2. Sizing a chain of inverters. (15 pts)



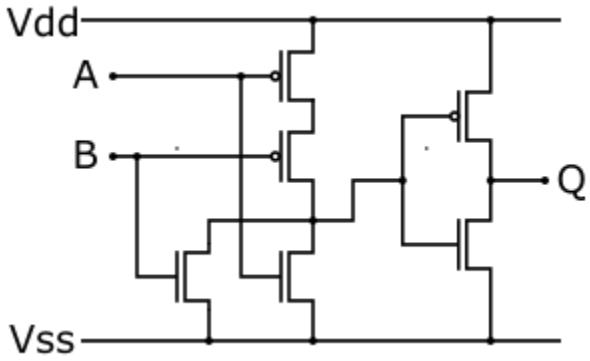
(a) In order to drive a large capacitance (CL=20pF) from a minimum size gate (with input capacitance CIN=10fF), you decide to introduce a one-stage buffer as shown in Figure above). Assume that the intrinsic propagation delay of a minimum size inverter, tinv, is 70pS. Determine the sizing of the additional stage that will minimize the propagation delay. (5 pts)

(b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? (10 pts)

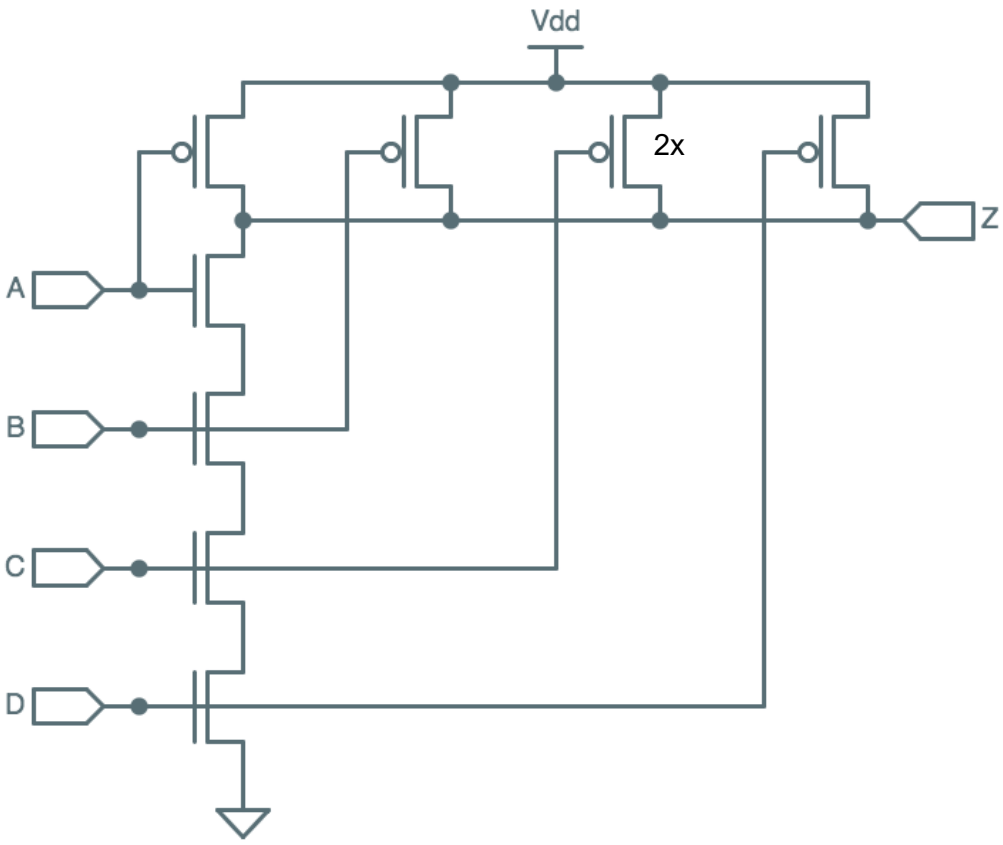
3. Scaling Question: A 130-nm CMOS microprocessor runs has a clock frequency of 3.2 GHz at a 1.2 volt supply voltage and consumes 103 watts of power. For this problem, assume that all gate capacitances in 65-nm CMOS are 2X smaller than in 130-nm CMOS. Using general scaling and maintaining a clock frequency of 3.2 GHz, how fast can the new 65-nm microprocessor be clocked using a 1 volt supply, without exceeding the power consumption of the original 1.2 V, 90-nm implementation? Assume that power is the limiting factor and not performance.? (10 pts)

4. Implement the logic function $Y = \overline{(A + B)(C + D + E)}$ in a single CMOS logic gate. (10 pts)

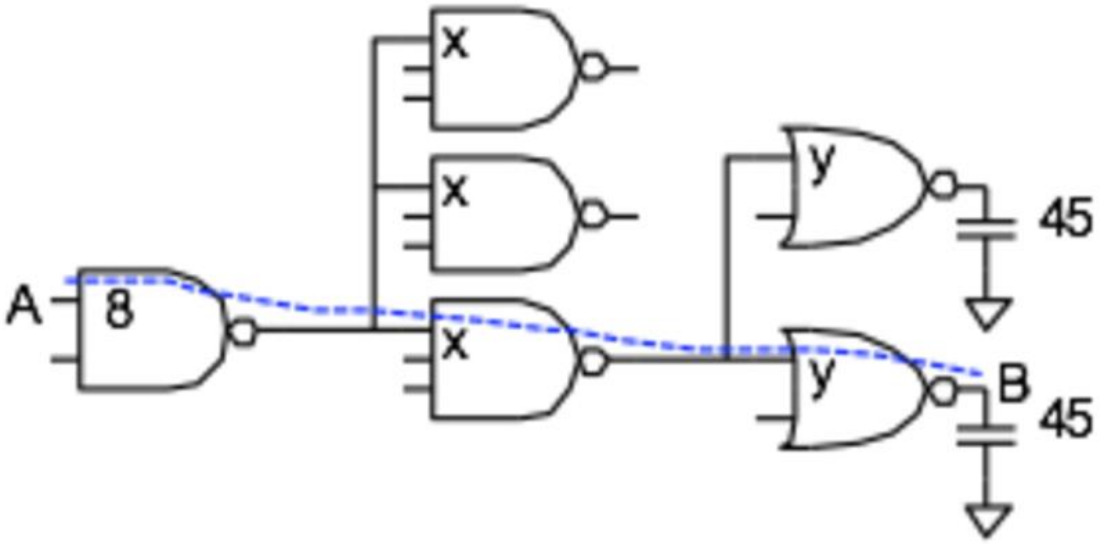
5. What is the logic function implemented by CMOS gate shown below. (5 pts)



6. Size the transistors in the CMOS gate below to achieve equal worst-case rise and fall time delay. Hint: I have correctly sized gate c for you. (10 pts)



7. For the schematic shown below, perform gate sizing to minimize the path delay. What is the delay (in units of 3RC) ? (20 pts)



8. Pick and solve your favorite quiz problem

9. Pick and solve your favorite quiz problem

10. Pick and solve your favorite quiz problem

The last 3 questions will be picked from your quizzes. these are bonus questions.