

UNIVERSITY *of* DELAWARE

# Chapter 9

## Differential and Multistage Amplifiers





# IN THIS CHAPTER YOU WILL LEARN

1. The essence of the operation of the MOS and the bipolar differential amplifiers: how they reject common-mode noise or interference and amplify differential signals.
2. The analysis and design of MOS and BJT differential amplifiers.
3. Differential-amplifier circuits of varying complexity; utilizing passive resistive loads, current-source loads, and cascodes - the building blocks we studied in Chapter 8.
4. An ingenious and highly popular differential-amplifier circuit that utilizes a current-mirror load.
5. The structure, analysis, and design of amplifiers composed of two or more stages in cascade. Two practical examples are studied in detail: a two-stage CMOS op amp and a four-stage bipolar op amp.



# Introduction

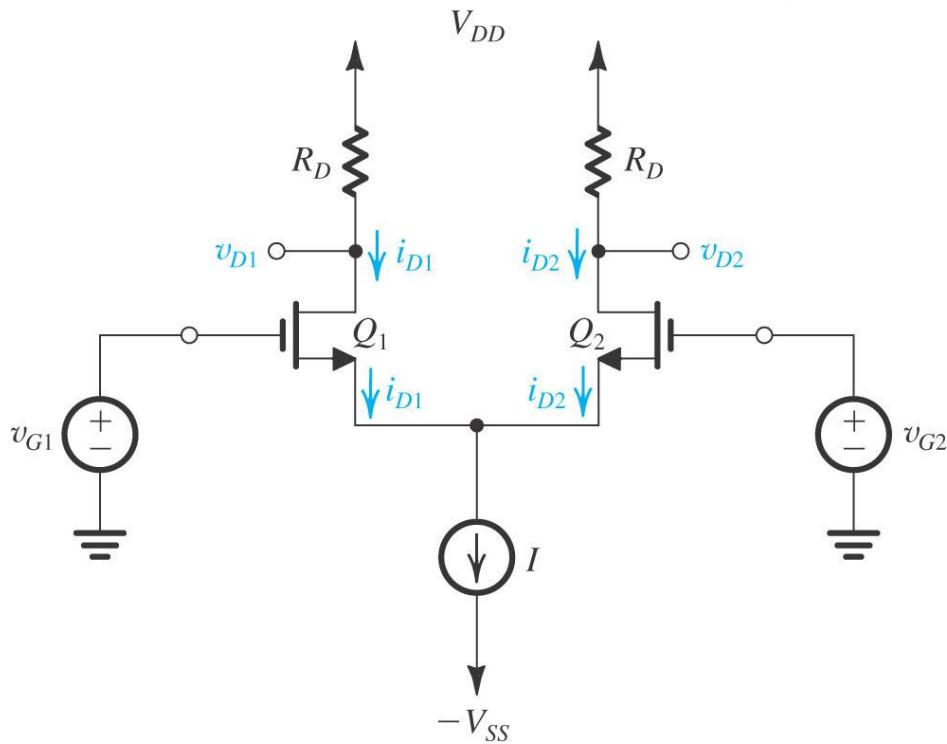
- Why use differential amplifiers?
  - Less sensitive to noise
  - Biasing enables coupling of amplifier stages
- The differential-pair of differential-amplifier configuration is widely used in IC circuit design.
- Technology was invented in 1940's for use in vacuum tubes – the basic differential-amplifier configuration was later implemented with discrete bipolar transistors.
- However, the configuration became most useful with invention of modern transistor / MOS technologies.



## 9.1 THE MOS DIFFERENTIAL PAIR



# The MOS Differential Pair



**Figure 9.1** The basic MOS differential-pair configuration.

- Two matched transistors ( $Q_1$  and  $Q_2$ ) joined and biased by a constant current source  $I$ .
- Assume the current sink is ideal.
- Shown with real loads (drain resistors but usually current source loads are used).
- FET's should not enter triode region of operation (i.e. operate in saturation).



# Operation with a Common-Mode Input Voltage

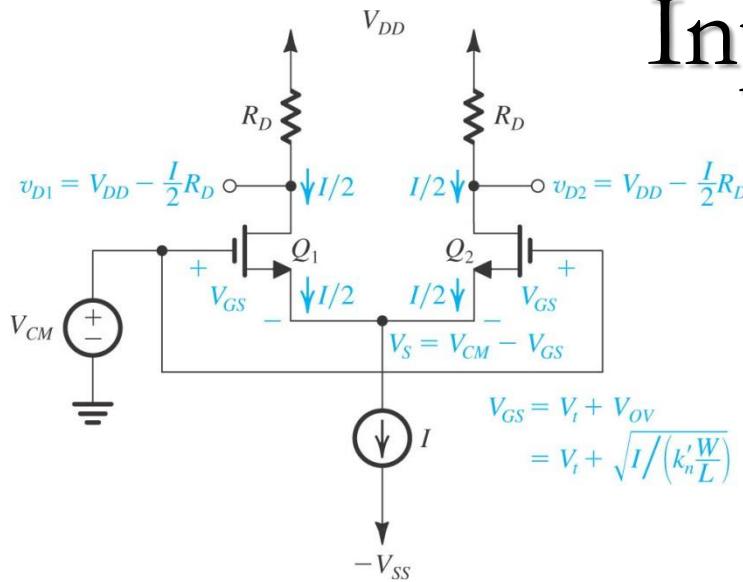


Figure 9.2 The MOS differential pair with a common-mode input voltage  $V_{CM}$ .

The voltage at each drain is :  $v_{D1} = v_{D2} = V_{DD} - \frac{I}{2}R_D$

Consider case when two gate terminals are joined together and connected to a **common-mode voltage** ( $V_{CM}$ ).  $Q_1$  and  $Q_2$  are matched so the current  $I$  will divide equally between the two transistors.

$$V_s = V_{CM} - V_{GS}$$

Where  $V_{GS}$  is the gate to source voltage corresponding to a drain current of  $I/2$ .

$$I_{D1} = I_{D2} = \frac{I}{2} = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2 = \frac{1}{2} k'_n \frac{W}{L} V_{OV}^2$$

$$V_{OV} = \sqrt{I / [k'_n (W/L)]}$$

[Neglecting channel-length modulation]



# Operation with a Common-Mode Input Voltage

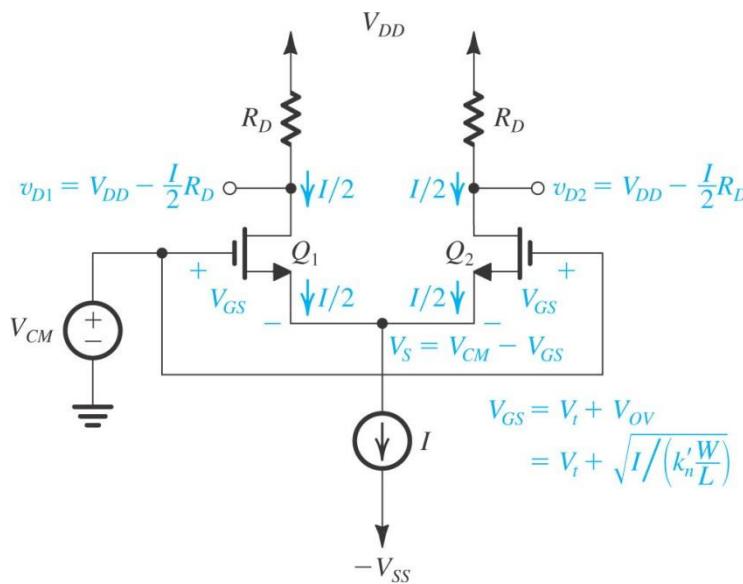


Figure 9.2 The MOS differential pair with a common-mode input voltage  $V_{CM}$ .

As we vary the common mode voltage,  $V_{CM}$ , the current will continue to be evenly divided between the two transistors (as long as they remain in saturation) and the voltages at the drains will remain constant. Thus the differential pair does not respond to (i.e. it rejects) common-mode input signals.

An important specification of a differential amplifier is its input common-mode range. This is the range of  $V_{CM}$  over which the differential pair operates properly.

$$V_{CM \max} = V_t + V_{DD} - \frac{I}{2}R_D = V_t + V_D$$

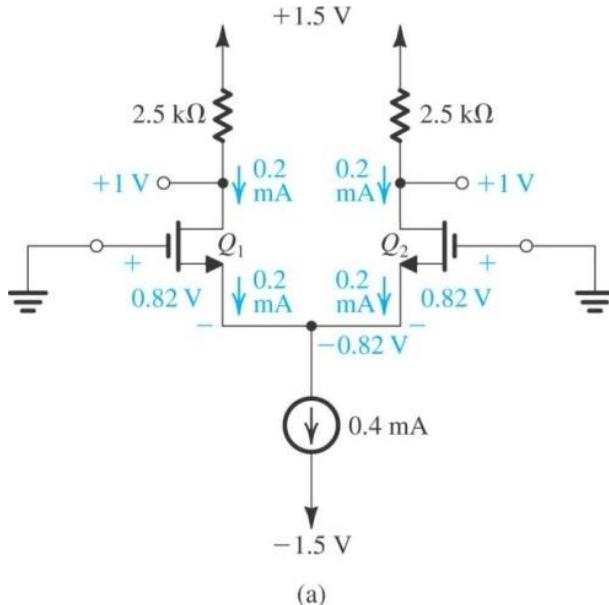
$$V_{CM \min} = -V_{SS} + V_{CS} + V_{GS}$$

Where  $V_{CS}$  is the voltage needed across the current sink for it to operate properly



# Example 9.1a

For the MOS differential pair with a common-mode voltage  $V_{CM}$  applied, as shown in Fig. 9.2, let  $V_{DD} = V_{SS} = 1.5$  V,  $k'_n(W/L) = 4$  mA/V<sup>2</sup>,  $V_t = 0.5$  V,  $I = 0.4$  mA, and  $R_D = 2.5$  kΩ, and neglect channel-length modulation. Assume that the current source  $I$  requires a minimum voltage of 0.4 V to operate properly.



(a) Find  $V_{OV}$  and  $V_{GS}$  for each transistor.

$$v_{G1} = v_{G2} = V_{CM}$$

$$I_{D1} = I_{D2} = \frac{I}{2}$$

$$V_{OV} = \sqrt{I / [k'_n(W/L)]} = \sqrt{\frac{0.4\text{mA}}{4\frac{\text{mA}}{\text{V}^2}}} = 0.316\text{V}$$

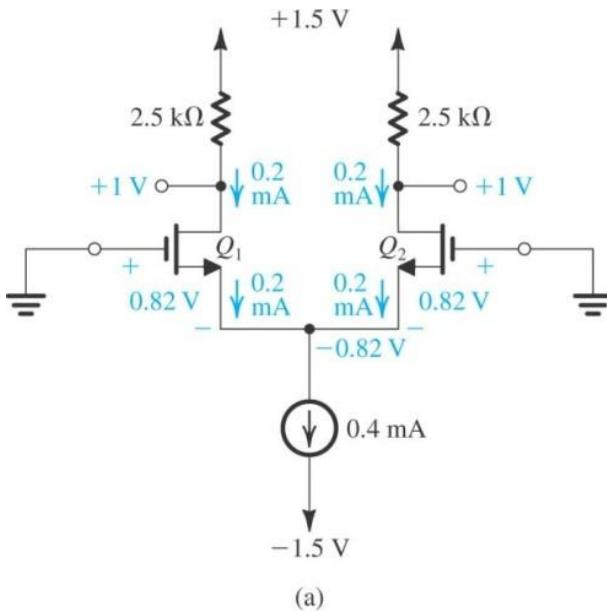
$$V_{GS} = V_t + V_{OV} = 0.5\text{V} + 0.316\text{V} = 0.816\text{V}$$

**Figure 9.3** Circuits for Example 9.1. Effects of varying  $V_{CM}$  on the operation of the differential pair.



## Example 9.1b

For the MOS differential pair with a common-mode voltage  $V_{CM}$  applied, as shown in Fig. 9.2, let  $V_{DD} = V_{SS} = 1.5$  V,  $k'_n(W/L) = 4$  mA/V<sup>2</sup>,  $V_t = 0.5$  V,  $I = 0.4$  mA, and  $R_D = 2.5$  kΩ, and neglect channel-length modulation. Assume that the current source  $I$  requires a minimum voltage of 0.4 V to operate properly.



(b) For  $V_{CM} = 0$ , find  $V_S$ ,  $I_{D1}$ ,  $I_{D2}$ ,  $V_{D1}$ , and  $V_{D2}$ .

$$v_{G1} = v_{G2} = V_{CM} \quad V_{OV} = 0.316\text{V} \quad V_{GS} = 0.816\text{V}$$

$$V_S = V_G - V_{GS} = 0\text{V} - 0.816\text{V} = -0.816\text{V}$$

$$V_{CS} = V_S - (-V_{SS}) = -0.816\text{V} + 1.5\text{V} = 0.684\text{V} \geq 0.4\text{V}$$

$$I_{D1} = I_{D2} = \frac{I}{2} = \frac{0.4\text{mA}}{2} = 0.2\text{mA}$$

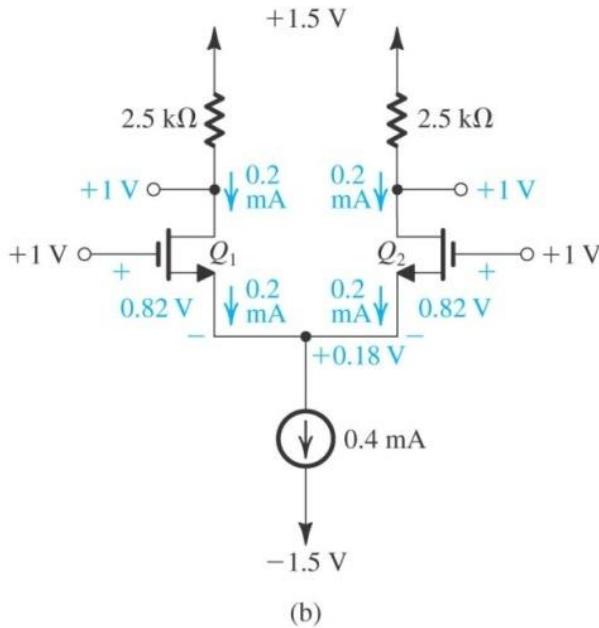
$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2} R_D = 1.5\text{V} - 0.2\text{mA} \times 2.5\text{k}\Omega = 1\text{V}$$

**Figure 9.3** Circuits for Example 9.1. Effects of varying  $V_{CM}$  on the operation of the differential pair.



## Example 9.1c

For the MOS differential pair with a common-mode voltage  $V_{CM}$  applied, as shown in Fig. 9.2, let  $V_{DD} = V_{SS} = 1.5$  V,  $k'_n(W/L) = 4$  mA/V<sup>2</sup>,  $V_t = 0.5$  V,  $I = 0.4$  mA, and  $R_D = 2.5$  k $\Omega$ , and neglect channel-length modulation. Assume that the current source  $I$  requires a minimum voltage of 0.4 V to operate properly.



(c) Repeat (b) for  $V_{CM} = +1$  V.

$$v_{G1} = v_{G2} = V_{CM} \quad V_{OV} = 0.316\text{V} \quad V_{GS} = 0.816\text{V}$$

$$V_S = V_G - V_{GS} = 1\text{V} - 0.816\text{V} = 0.184\text{V}$$

$$V_{CS} = V_S - (-V_{SS}) = 0.184\text{V} + 1.5\text{V} = 1.684\text{V} \geq 0.4\text{V}$$

$$I_{D1} = I_{D2} = \frac{I}{2} = \frac{0.4\text{mA}}{2} = 0.2\text{mA}$$

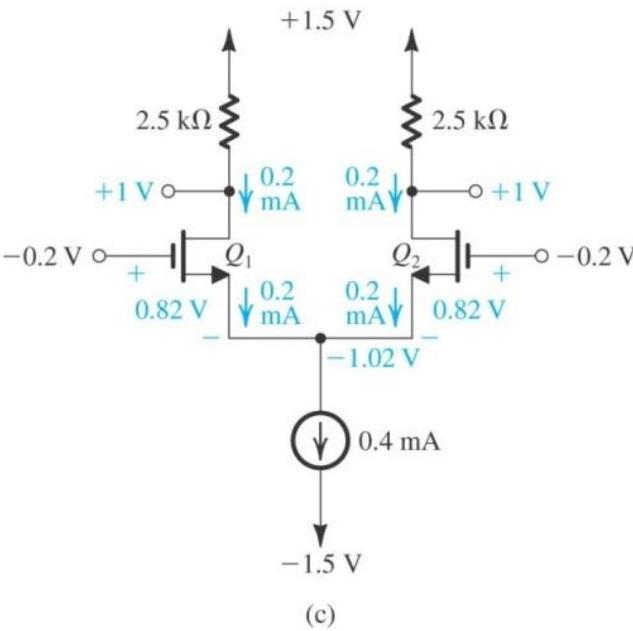
$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2} R_D = 1.5\text{V} - 0.2\text{mA} \times 2.5\text{k}\Omega = 1\text{V}$$

**Figure 9.3** Circuits for Example 9.1.  
Effects of varying  $V_{CM}$  on the operation of  
the differential pair.



## Example 9.1d

For the MOS differential pair with a common-mode voltage  $V_{CM}$  applied, as shown in Fig. 9.2, let  $V_{DD} = V_{SS} = 1.5$  V,  $k'_n(W/L) = 4$  mA/V<sup>2</sup>,  $V_t = 0.5$  V,  $I = 0.4$  mA, and  $R_D = 2.5$  k $\Omega$ , and neglect channel-length modulation. Assume that the current source  $I$  requires a minimum voltage of 0.4 V to operate properly.



(d) Repeat (b) for  $V_{CM} = -0.2$  V.

$$v_{G1} = v_{G2} = V_{CM} \quad V_{OV} = 0.316\text{V} \quad V_{GS} = 0.816\text{V}$$

$$V_S = V_G - V_{GS} = -0.2\text{V} - 0.816\text{V} = -1.016\text{V}$$

$$V_{CS} = V_S - (-V_{SS}) = -1.016\text{V} + 1.5\text{V} = 0.484\text{V} \geq 0.4\text{V}$$

$$I_{D1} = I_{D2} = \frac{I}{2} = \frac{0.4\text{mA}}{2} = 0.2\text{mA}$$

$$V_{D1} = V_{D2} = V_{DD} - \frac{I}{2}R_D = 1.5\text{V} - 0.2\text{mA} \times 2.5\text{k}\Omega = 1\text{V}$$

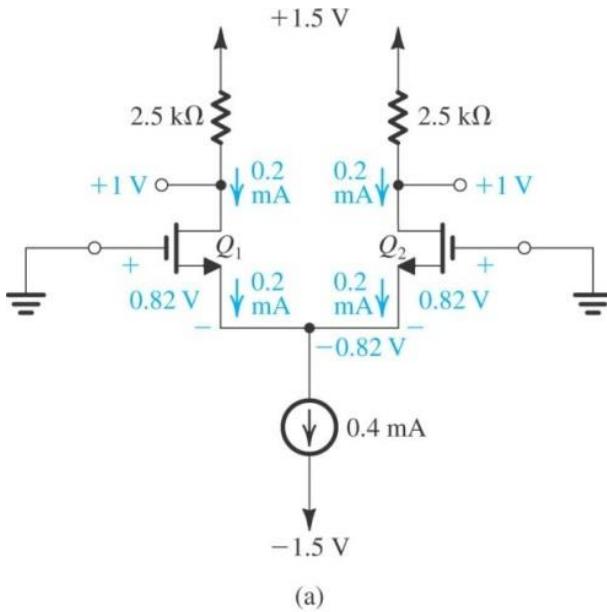
**Figure 9.3** Circuits for Example 9.1.  
Effects of varying  $V_{CM}$  on the operation of  
the differential pair.



## Example 9.1e,f

For the MOS differential pair with a common-mode voltage  $V_{CM}$  applied, as shown in Fig. 9.2, let  $V_{DD} = V_{SS} = 1.5$  V,  $k'_n(W/L) = 4$  mA/V<sup>2</sup>,  $V_t = 0.5$  V,  $I = 0.4$  mA, and  $R_D = 2.5$  k $\Omega$ , and neglect channel-length modulation. Assume that the current source  $I$  requires a minimum voltage of 0.4 V to operate properly.

- (e) What is the highest permitted value of  $V_{CM}$ ?  
(f) What is the lowest value allowed for  $V_{CM}$ ?



$$V_{CM \max} = V_t + V_D = 0.5 \text{ V} + 1.0 \text{ V} = 1.5 \text{ V}$$

$$\begin{aligned} V_{CM \min} &= -V_{SS} + V_{CS} + V_{GS} \\ &= -1.5 \text{ V} + 0.4 \text{ V} + 0.816 \text{ V} = -0.284 \text{ V} \end{aligned}$$

$$-0.284 \text{ V} \leq V_{CM} \leq +1.5 \text{ V}$$

**Figure 9.3** Circuits for Example 9.1. Effects of varying  $V_{CM}$  on the operation of the differential pair.



# Operation with a Differential Input Voltage

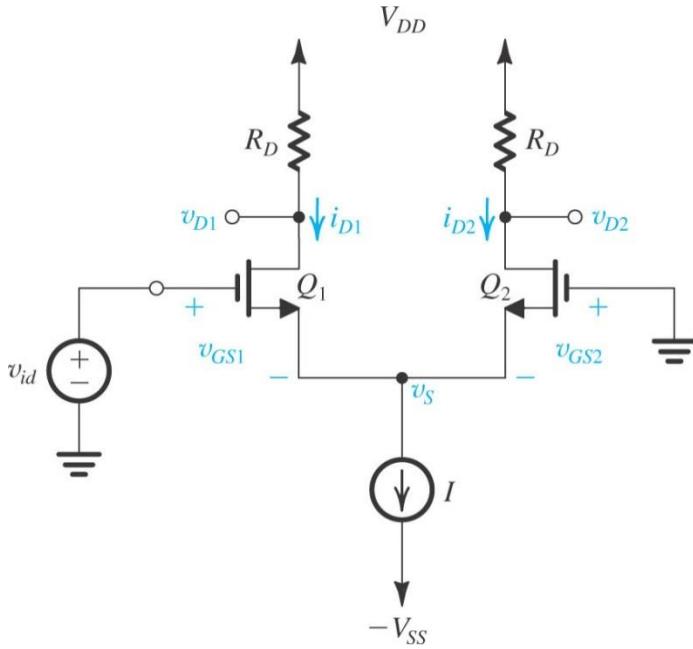


Figure 9.4: The MOS differential pair with a differential input signal  $v_{id}$  applied.

If  $v_{id}$  is applied to  $Q_1$  and  $Q_2$  is grounded, the following conditions apply:

- $v_{id} = v_{GS1} - v_{GS2} > 0$  or  $v_{id} = v_{GS1} - v_{GS2} < 0$
- $i_{D1} > i_{D2}$                                $i_{D1} < i_{D2}$

Let's assume that  $v_{id}$  ( $V_{GS1}$ ) is such that all current ( $I$ ) is flowing through  $Q_1$ . Then:

$$I = \frac{1}{2} k'_n \frac{W}{L} (v_{GS1} - V_t)^2$$

$$v_{GS1} = V_t + \sqrt{2I/[k'_n(W/L)]} = V_t + \sqrt{2}V_{OV}$$

Where  $V_{OV}$  is the overdrive voltage corresponding to a drain current of  $I/2$ .

$$V_{GS2} = V_t$$

$$v_s = -V_t$$



# Operation with a Differential Input Voltage

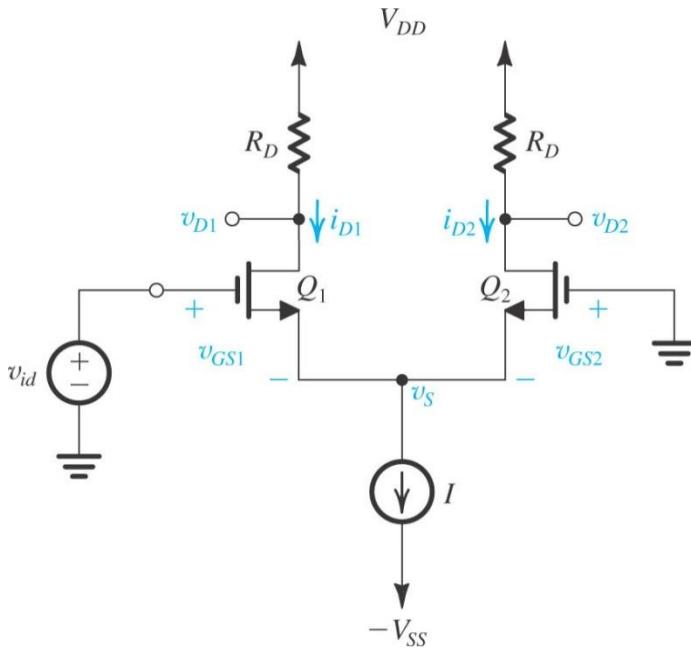


Figure 9.4: The MOS differential pair with a differential input signal  $v_{id}$  applied.

Thus the maximum input voltage (where all of the current is going through  $Q_1$ ) is where:

$$v_{id\max} = v_{GS1} + v_S = V_t + \sqrt{2}V_{OV} - V_t = \sqrt{2}V_{OV}$$

In the same manner we can show that when

$$v_{id} = -\sqrt{2}V_{OV}$$

that  $Q_1$  is turned off and all of the current flows through  $Q_2$ . Thus the current  $I$  can be steered from one transistor to the other by varying  $v_{id}$  in the range

$$-\sqrt{2}V_{OV} \leq v_{id} \leq \sqrt{2}V_{OV}$$

The differential pair responds to a **difference-mode** or **differential input signals**. Note that the transistors must remain in saturation even when only one of them is conducting current.

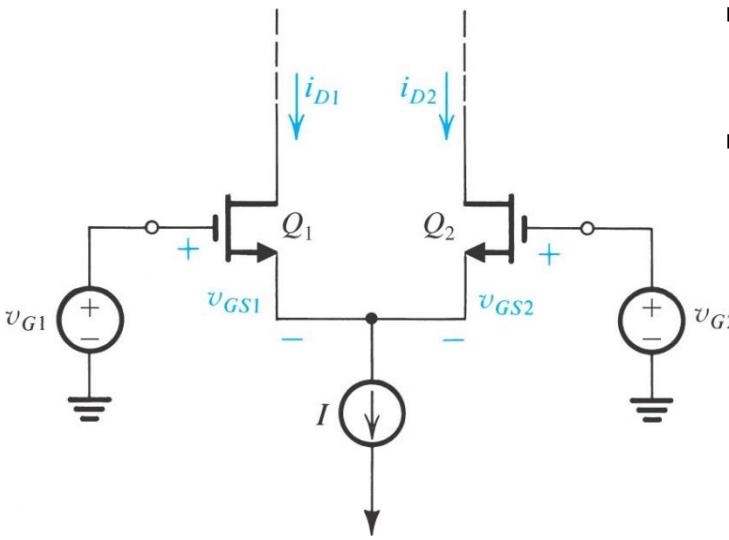


# Summary

- Two input terminals connected to a suitable dc voltage  $V_{CM}$ .
- Bias current  $I$  of a “perfectly” symmetrical differential pair divides equally.
  - Zero voltage differential between the two drains.
- To steer the current completely to one side of the pair, a difference input voltage  $v_{id}$  of at least  $\sqrt{2}V_{OV}$  is needed.
- A voltage signal  $-\Delta IR_D$  develops at one of the drains and an opposite-polarity signal,  $\Delta IR_D$ , develops at the other drain. Thus the output voltage taken between the two drains will be  $2\Delta IR_D$ , which is proportional to the differential input signal  $v_{id}$ .



# Large-Signal Operation



- Objective is to derive expressions for drain current  $i_{D1}$  and  $i_{D2}$  in terms of differential signal  $v_{id} = v_{G1} - v_{G2}$ .
- Assumptions:
  - Perfectly Matched
  - Channel-length Modulation is Neglected
  - Load Independence
  - Saturation Region

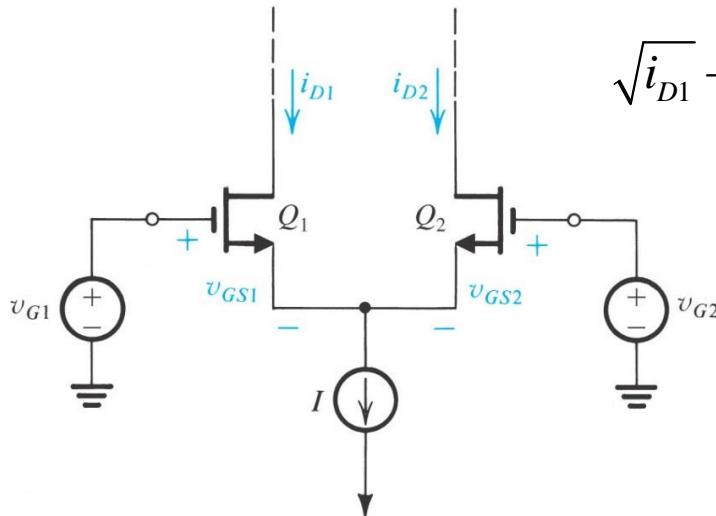
$$i_{D1} = \frac{1}{2} k'_n \frac{W}{L} (v_{GS1} - V_t)^2 \quad \sqrt{i_{D1}} = \sqrt{\frac{1}{2} k'_n \frac{W}{L} (v_{GS1} - V_t)}$$

$$i_{D2} = \frac{1}{2} k'_n \frac{W}{L} (v_{GS2} - V_t)^2 \quad \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k'_n \frac{W}{L} (v_{GS2} - V_t)}$$

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k'_n \frac{W}{L} (v_{GS1} - V_t)} - \sqrt{\frac{1}{2} k'_n \frac{W}{L} (v_{GS2} - V_t)} = \sqrt{\frac{1}{2} k'_n \frac{W}{L} (v_{GS1} - v_{GS2})}$$



# Large-Signal Operation



**Figure 9.5:** The MOSFET differential pair for the purpose of deriving the transfer characteristics,  $i_{D1}$  and  $i_{D2}$  versus  $v_{id} = v_{G1} - v_{G2}$ .

$$i_{D1} = \frac{I}{2} + \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \sqrt{1 - \left( \frac{v_{id}/2}{V_{OV}} \right)^2}$$

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k'_n \frac{W}{L}} (v_{GS1} - v_{GS2})$$

$$v_{GS1} - v_{GS2} = v_{G1} - v_{G2} = v_{id}$$

Note the constant-current bias constraint:

$$i_{D1} + i_{D2} = I$$

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k'_n \frac{W}{L}} v_{id}$$

Square both sides of the equation and use the constant current constraint:

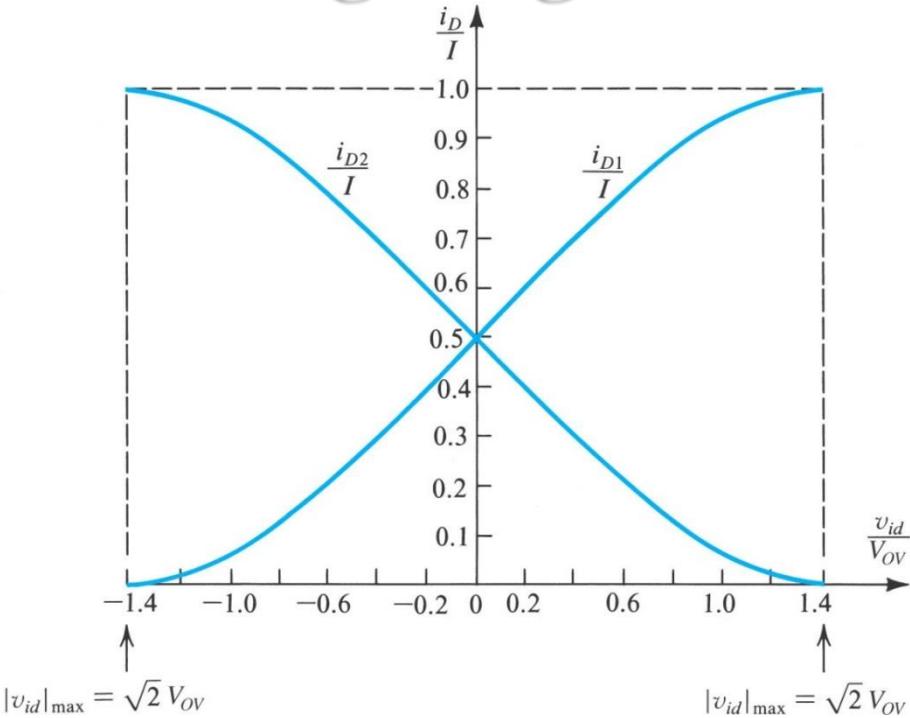
$$2\sqrt{i_{D1}i_{D2}} = I - \frac{1}{2} k'_n \frac{W}{L} v_{id}^2$$

$$i_{D2} = \frac{I}{2} - \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \sqrt{1 - \left( \frac{v_{id}/2}{V_{OV}} \right)^2}$$

Sedra and Smith  
pp. 602 - 605



# Large-Signal Transfer Characteristics



**Figure 9.6** Normalized plots of the currents in a MOSFET differential pair.

Note that  $V_{OV}$  is the overdrive voltage at which  $Q_1$  and  $Q_2$  operate when conducting drain currents equal to  $I/2$ , the equilibrium situation. Note that these graphs are universal and apply to any MOS differential pair

$$i_{D1} = \frac{I}{2} + \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \sqrt{1 - \left( \frac{v_{id}/2}{V_{OV}} \right)^2}$$

$$i_{D2} = \frac{I}{2} - \left( \frac{I}{V_{OV}} \right) \left( \frac{v_{id}}{2} \right) \sqrt{1 - \left( \frac{v_{id}/2}{V_{OV}} \right)^2}$$

Transfer characteristics are nonlinear and usually linear amplification is desirable.

If we can keep  $v_{id}/2 \ll V_{OV}$  (small-signal) we can say that

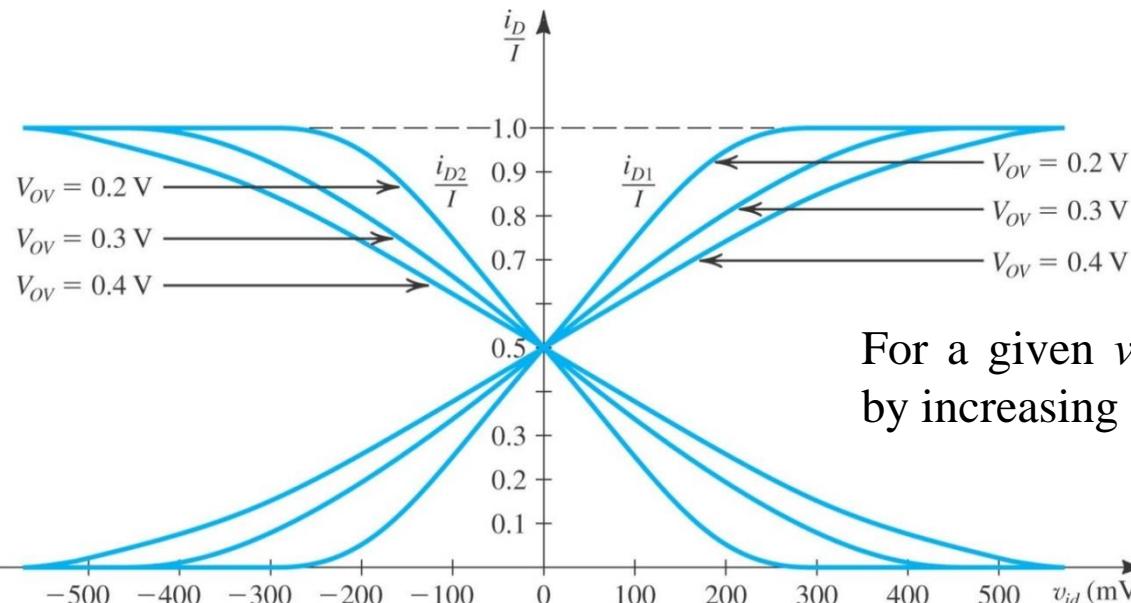
$$i_{D1} \approx \frac{I}{2} + \left( \frac{I}{V_{OV}} \right) \frac{v_{id}}{2} = \frac{I}{2} + i_d$$

$$i_{D2} \approx \frac{I}{2} - \left( \frac{I}{V_{OV}} \right) \frac{v_{id}}{2} = \frac{I}{2} - i_d$$

$$\text{where } i_d = \left( \frac{I}{V_{OV}} \right) \frac{v_{id}}{2}$$



# Large-Signal Transfer Characteristics



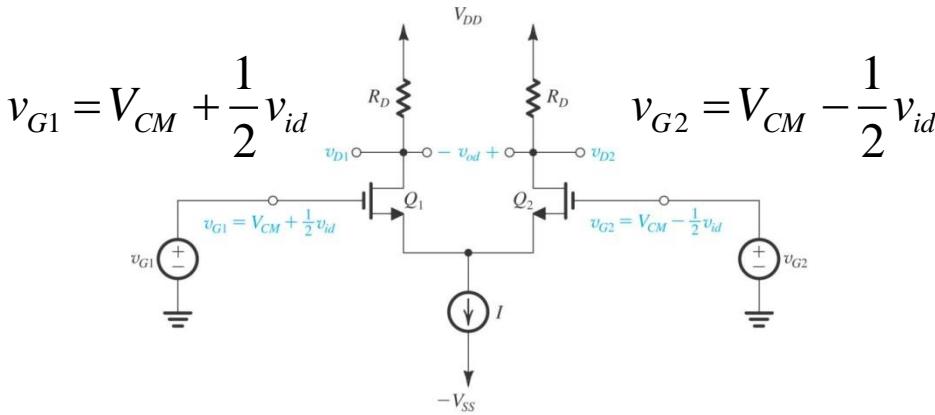
For a given  $v_{id}$ , the linearity can be improved by increasing the overdrive voltage.

**Figure 9.7** The linear range of operation of the MOS differential pair can be extended by operating the transistor at a higher value of  $V_{OV}$ .

$$i_{D2} \approx \frac{I}{2} - \left( \frac{I}{V_{OV}} \right) \frac{v_{id}}{2} = \frac{I}{2} - i_d$$
$$i_{D1} \approx \frac{I}{2} + \left( \frac{I}{V_{OV}} \right) \frac{v_{id}}{2} = \frac{I}{2} + i_d$$
$$i_d = \left( \frac{I}{V_{OV}} \right) \frac{v_{id}}{2}$$



# Small Signal Differential Gain



**Figure 9.8** Small-signal analysis of the MOS differential amplifier. (a) The circuit with a common-mode voltage applied to set the dc bias voltage at the gates and with  $v_{id}$  applied in a complementary (or balanced) manner. (b) The circuit prepared for small-signal analysis.

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}}$$

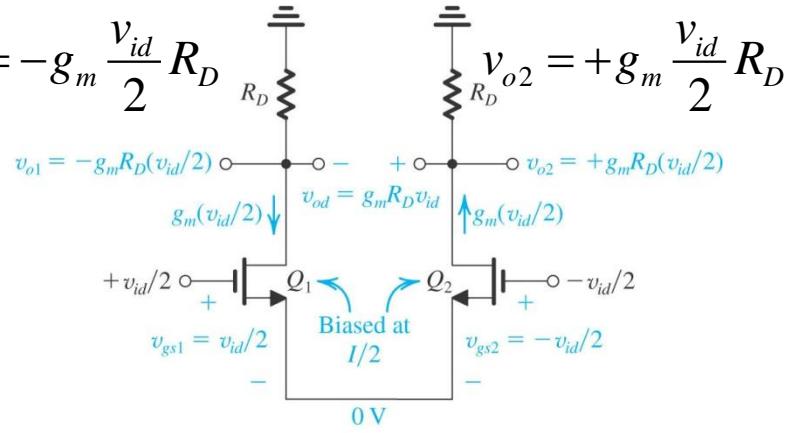
$$A_d \equiv \frac{v_{od}}{v_{id}}$$

Taking the output single-ended:

$$\frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D \quad \frac{v_{o2}}{v_{id}} = \frac{1}{2} g_m R_D$$

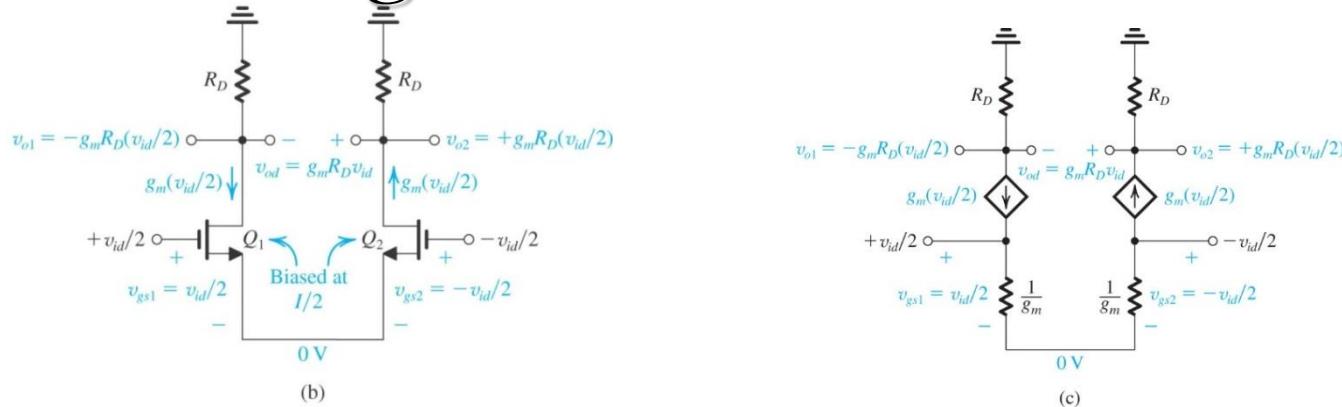
Taking the output differentially:

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$





# Small Signal Differential Gain



**Figure 9.8** Small-signal analysis of the MOS differential amplifier. (b) The circuit prepared for small-signal analysis. (c) The circuit in (b), with the MOSFETs replaced with T models.

$$v_{G1} = V_{CM} + \frac{1}{2} v_{id}$$

$$v_{G2} = V_{CM} - \frac{1}{2} v_{id}$$

$$v_{o1} = -g_m \frac{v_{id}}{2} R_D$$

$$v_{o2} = +g_m \frac{v_{id}}{2} R_D$$

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}}$$

Taking the output single-ended:

$$\frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D$$

$$\frac{v_{o2}}{v_{id}} = \frac{1}{2} g_m R_D$$

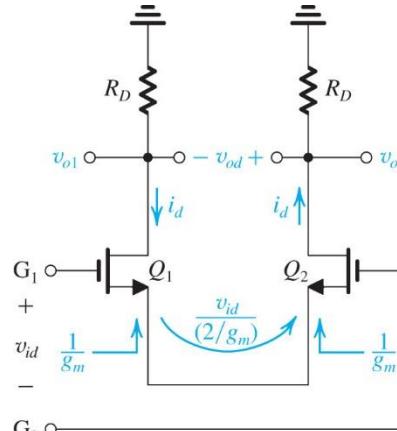
$$A_d \equiv \frac{v_{od}}{v_{id}}$$

Taking the output differentially:

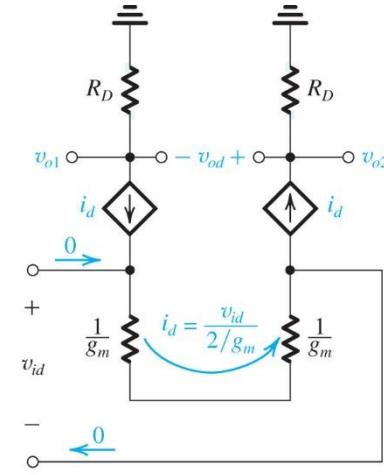
$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$



# An Alternative Circuit View



(a)



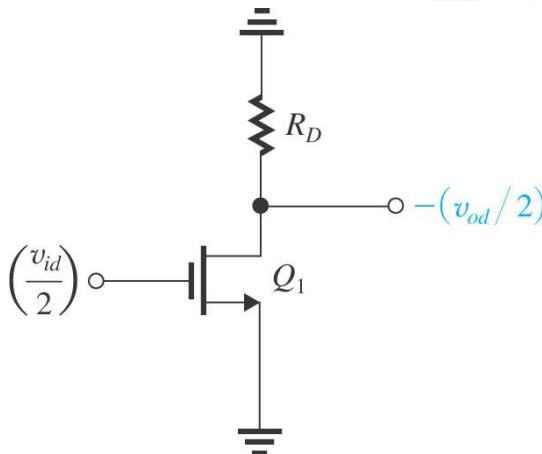
(b)

**Figure 9.9** An alternative view of the small-signal differential operation of the MOS differential pair: (a) analysis done directly on the circuit; (b) analysis using equivalent-circuit models.

An alternative and useful way of viewing the operation of the differential pair in response to a differential input signal  $v_{id}$  is illustrated in Fig. 9.9. Here we are making use of the fact that the resistance between gate and source of a MOSFET, looking into the source, is  $1/g_m$ . As a result, between  $G_1$  and  $G_2$  we have a total resistance, in the source circuit, of  $2/g_m$ . It follows that we can obtain the current  $i_d$  simply by dividing  $v_{id}$  by  $2/g_m$ , as indicated in the figure.



# Differential Half-Circuit



$$A_d = g_m (R_D \parallel r_o)$$

**Figure 9.10** The equivalent differential half-circuit of the differential amplifier of Fig. 9.8. Here  $Q_1$  is biased at  $I/2$  and is operating at  $V_{OV}$ . This circuit can be used to determine the differential voltage gain of the differential amplifier  $A_d = v_{od}/v_{id}$ .

When a symmetrical differential amplifier is fed with a differential signal in a balanced manner the performance can be determined by considering only half the circuit. Here  $Q_1$  is biased at  $I/2$  and is operating at  $V_{OV}$ .

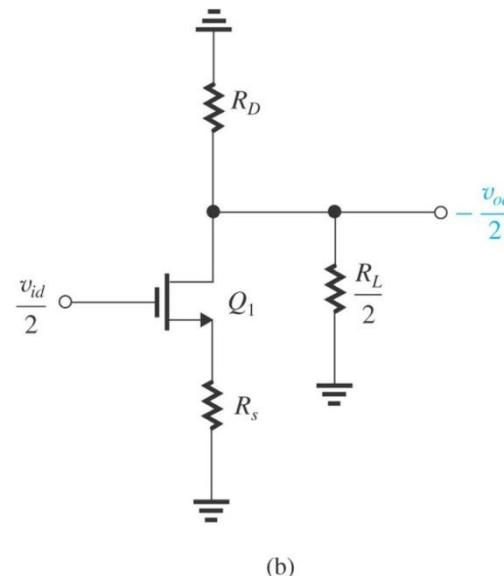
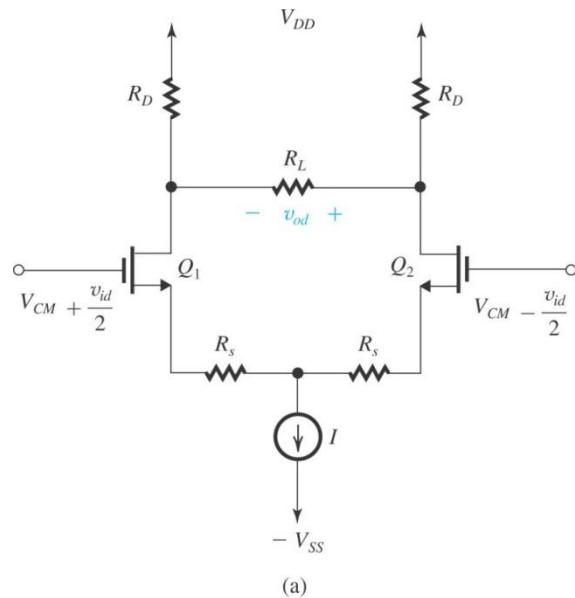
This circuit may be used to determine the differential voltage gain of the differential amplifier  $A_d = v_{od}/v_{id}$ .

More significantly, the frequency response of the differential gain can be determined by analyzing the half-circuit, as we shall do in Chapter 10.



## Example 9.2

Give the differential half-circuit of the differential amplifier shown in Fig. 9.11(a). Assume that  $Q_1$  and  $Q_2$  are perfectly matched. Neglecting  $r_o$ , determine the differential voltage gain  $A_d = v_{od}/v_{id}$ .



**Figure 9.11** (a) Differential amplifier for Example 9.2. (b) Differential half-circuit.

$$\frac{-v_{od}/2}{v_{id}/2} = \frac{R_D \parallel (R_L/2)}{1/g_m + R_S}$$

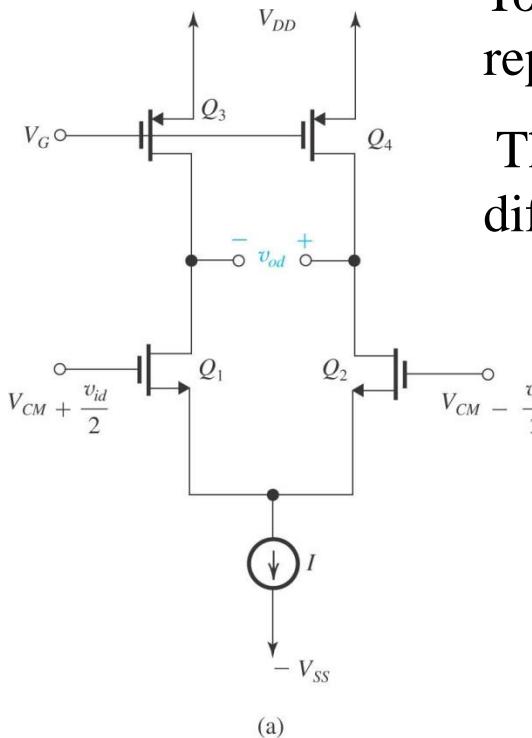
$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{R_D \parallel (R_L/2)}{1/g_m + R_S}$$



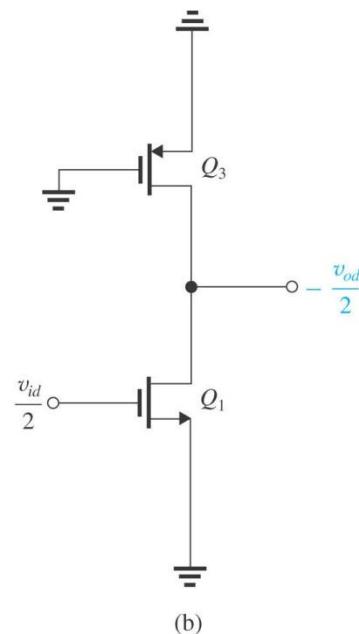
# Diff Amp with Current-Source Loads

To obtain higher gain, the passive resistances ( $R_D$ ) can be replaced with active loads/current sources.

The differential voltage gain  $A_d$  can be found from the differential half-circuit as



(a)

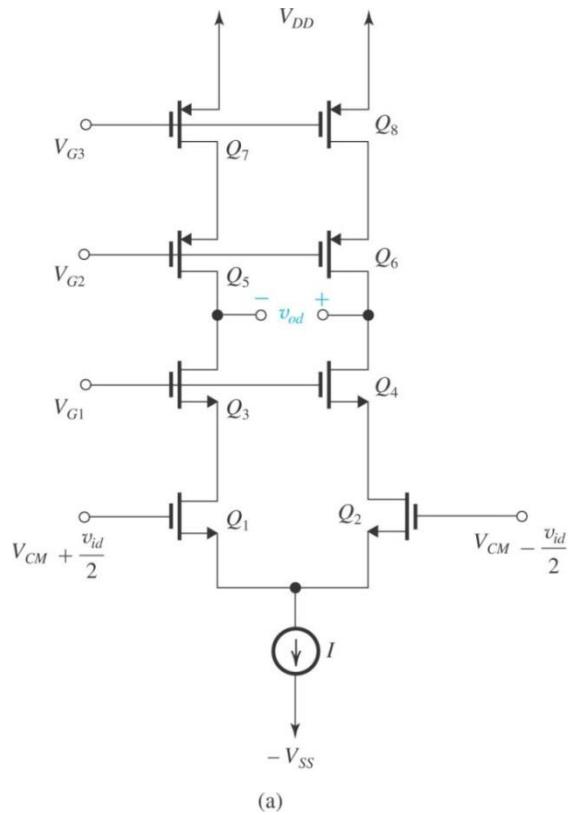


$$A_d \equiv \frac{v_{od}}{v_{id}} = g_m(r_{o1} \parallel r_{o3})$$

**Figure 9.12 (a)** Differential amplifier with current-source loads formed by  $Q_3$  and  $Q_4$ . **(b)** Differential half-circuit of the amplifier in (a).



# Cascode Differential Amplifier



Gain can be increased via cascode configuration.

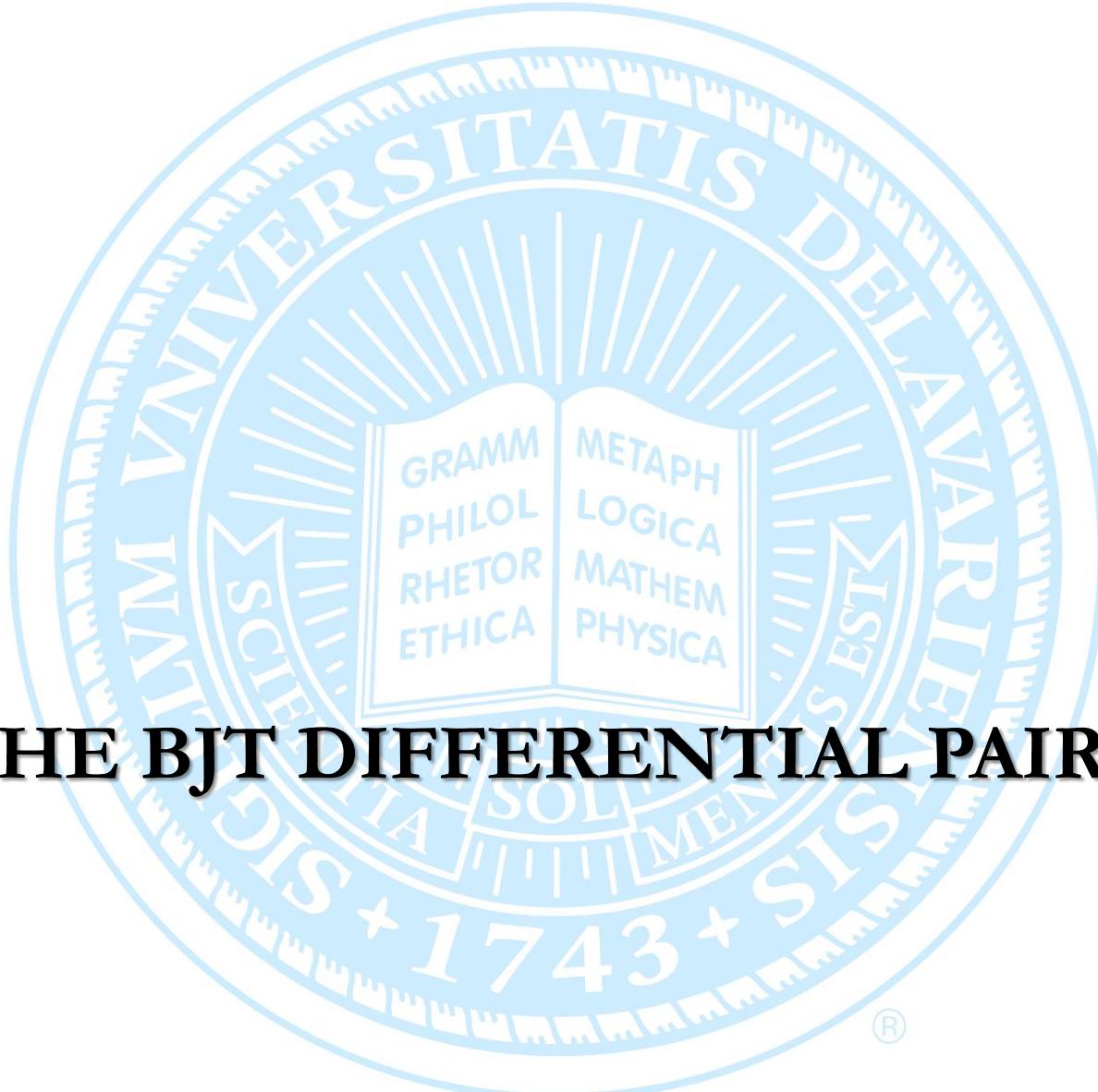
$$R_{op} = (g_{m5}r_{o5})r_{o7}$$

$$R_{on} = (g_{m3}r_{o3})r_{o1}$$

$$A_d = g_{m1}(R_{on} \parallel R_{op})$$

$$A_d = g_{m1}(g_{m3}r_{o3}r_{o1} \parallel g_{m5}r_{o5}r_{o7})$$

Figure 9.13 (a) Cascode differential amplifier; and (b) its differential half circuit.



## 9.2 THE BJT DIFFERENTIAL PAIR



# The BJT Differential Pair

Figure 9.14 shows the basic BJT differential-pair configuration.

It is similar to the MOSFET circuit – composed of two matched transistors biased by a constant-current source – and is modeled by many similar expressions.

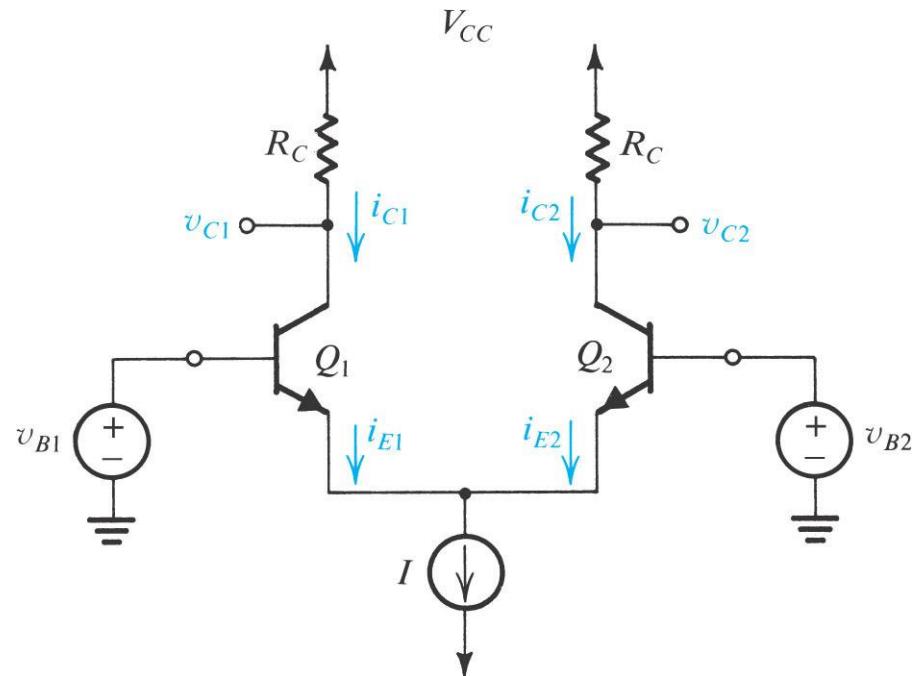


Figure 9.14 The basic BJT differential-pair configuration.



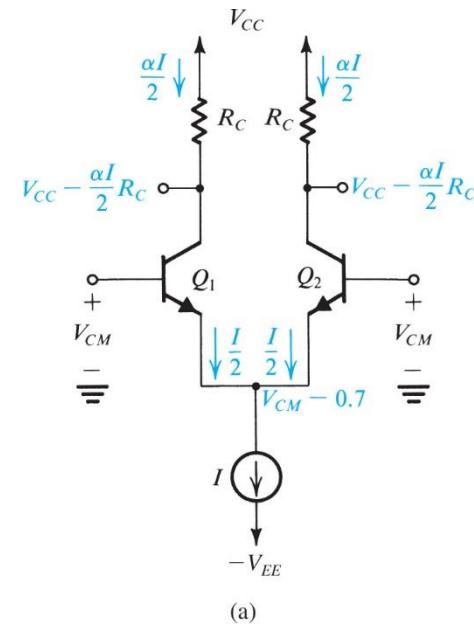
# Common Mode Operation

The allowable range of  $V_{CM}$  is determined at the upper end by  $Q_1$  and  $Q_2$  leaving the active mode and entering saturation.

$$V_{CM\max} \approx V_C + 0.4 = V_{CC} - \alpha \frac{I}{2} R_C + 0.4$$

$$V_{CM\min} = -V_{EE} + V_{CS} + V_{BE}$$

Where  $V_{CS}$  is the voltage needed across the current sink for it to operate properly



**Figure 9.15** Different modes of operation of the BJT differential pair: (a) the differential pair with a common-mode input voltage  $V_{CM}$ .



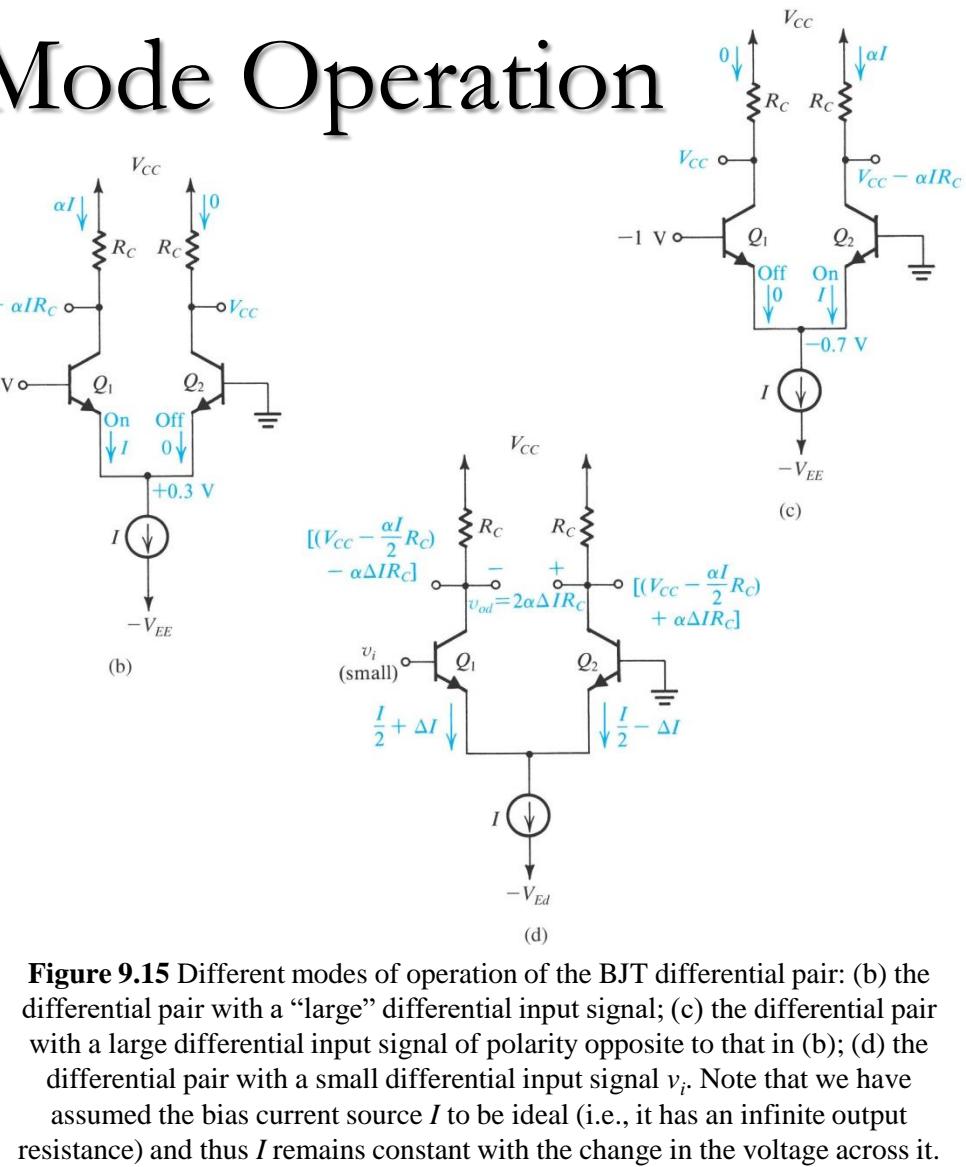
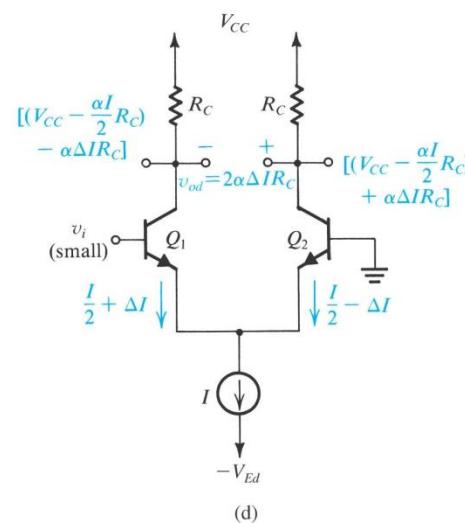
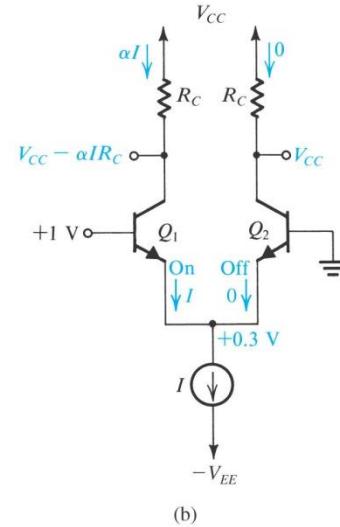
# Differential Mode Operation

- let the voltage  $v_{B2}$  be set to a constant value, say, zero (by grounding base of  $Q_2$ ), and let  $v_{B1} = +1\text{V}$ .
- It can be seen that  $Q_1$  will be on and conducting all of the current  $I$  and that  $Q_2$  will be off.

$$v_{o1} = v_{C1} = V_{CC} - \alpha R_C I$$

$$v_{o2} = v_{C2} = V_{CC}$$

$$\begin{aligned}v_{od} &= v_{o2} - v_{o1} = V_{CC} - (V_{CC} - \alpha R_C I) \\&= \alpha R_C I\end{aligned}$$

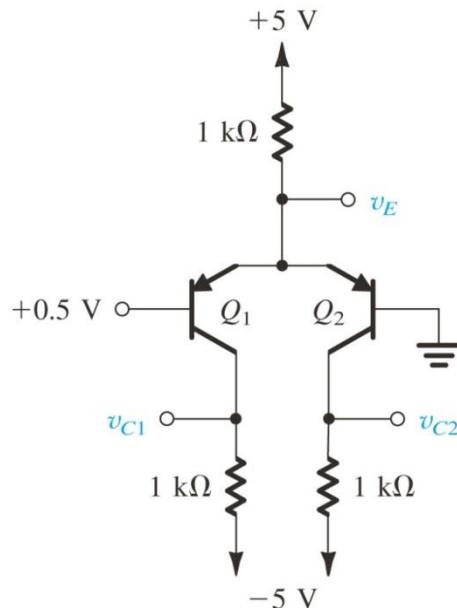


**Figure 9.15** Different modes of operation of the BJT differential pair: (b) the differential pair with a “large” differential input signal; (c) the differential pair with a large differential input signal of polarity opposite to that in (b); (d) the differential pair with a small differential input signal  $v_i$ . Note that we have assumed the bias current source  $I$  to be ideal (i.e., it has an infinite output resistance) and thus  $I$  remains constant with the change in the voltage across it.



# Exercise 9.7

Find  $v_E$ ,  $v_{C1}$ , and  $v_{C2}$  in the circuit of Fig. E9.7. Assume that  $|v_{BE}|$  of a conducting transistor is approximately 0.7 V and that  $\alpha \approx 1$ .



$$v_E = 0 + v_{BE} = 0.7V$$

$$I = \frac{5V - v_E}{1k\Omega} = \frac{5V - 0.7V}{1k\Omega} = 4.3mA$$

$$I_{Q1} = 0mA$$

$$v_{C1} = -5V + I_{Q1} \times 1k\Omega = -5V$$

$$I_{Q2} = 4.3mA$$

$$v_{C2} = -5V + I_{Q2} \times 1k\Omega = -0.7V$$

Figure E9.7



# Large-Signal Operation

$$i_{E1} = \frac{I_S}{\alpha} e^{(v_{B1}-v_E)/V_T}$$

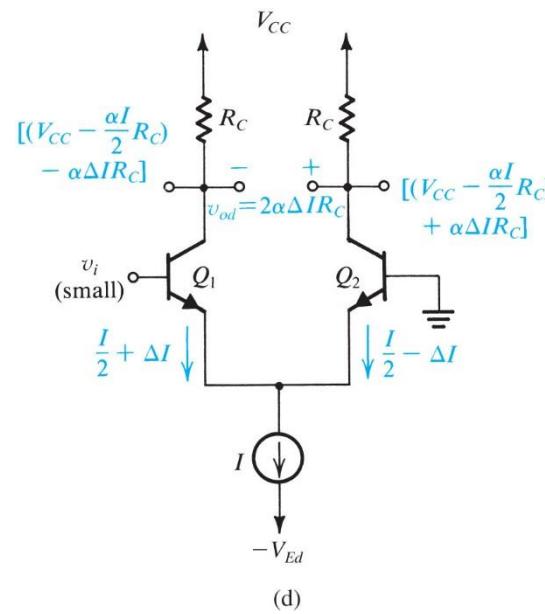
$$\begin{aligned} i_{E1} + i_{E2} &= I \\ v_{B1} - v_{B2} &= v_{id} \end{aligned}$$

$$i_{E2} = \frac{I_S}{\alpha} e^{(v_{B2}-v_E)/V_T}$$

$$\frac{i_{E1}}{i_{E2}} = e^{(v_{B1}-v_{B2})/V_T}$$

$$\frac{i_{E1}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{(v_{B2}-v_{B1})/V_T}}$$

$$i_{E1} = \frac{I}{1 + e^{-v_{id}/V_T}}$$



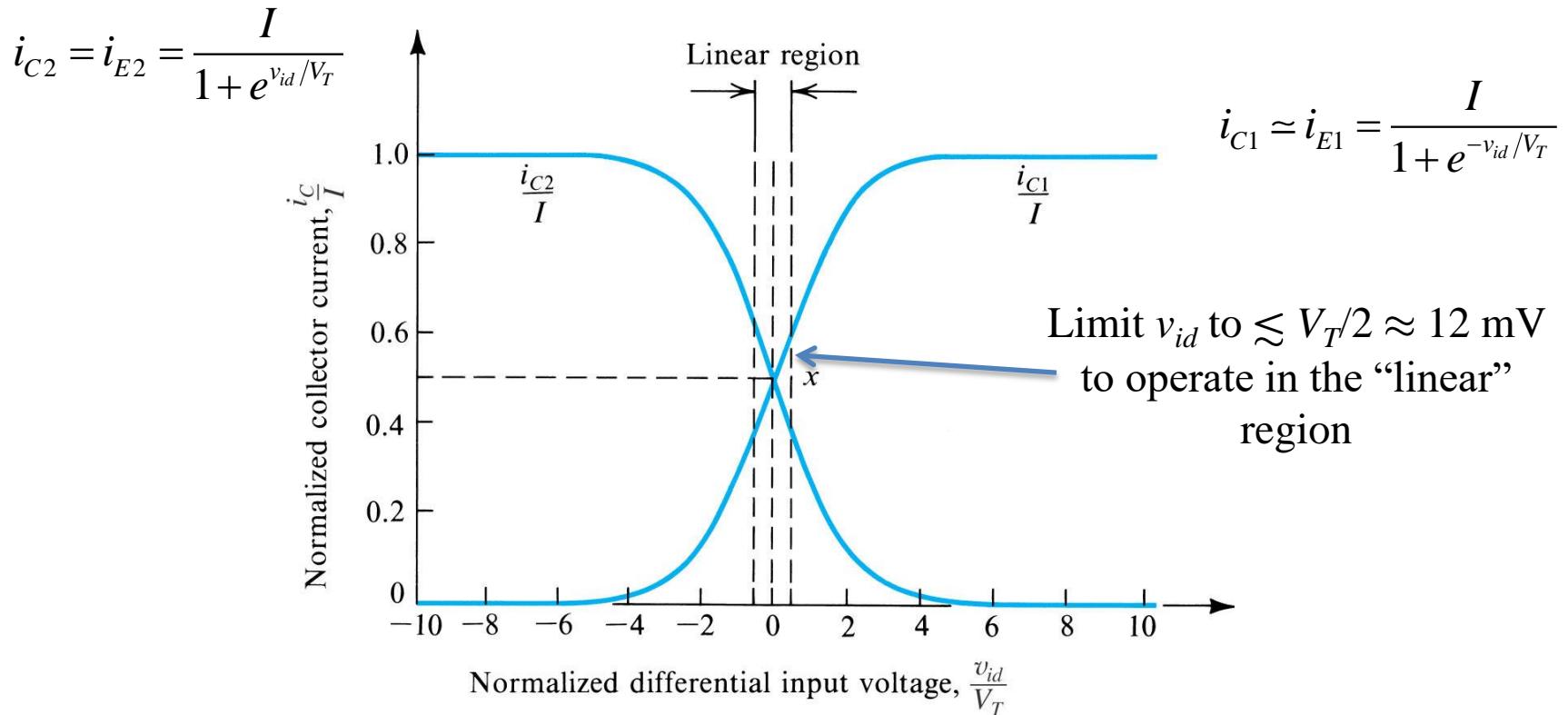
$$\frac{i_{E2}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{(v_{B1}-v_{B2})/V_T}}$$

$$i_{E2} = \frac{I}{1 + e^{v_{id}/V_T}}$$

**Figure 9.15** Different modes of operation of the BJT differential pair: (d) the differential pair with a small differential input signal  $v_i$ . Note that we have assumed the bias current source  $I$  to be ideal (i.e., it has an infinite output resistance) and thus  $I$  remains constant with the change in the voltage across it.



# Large Signal Operation



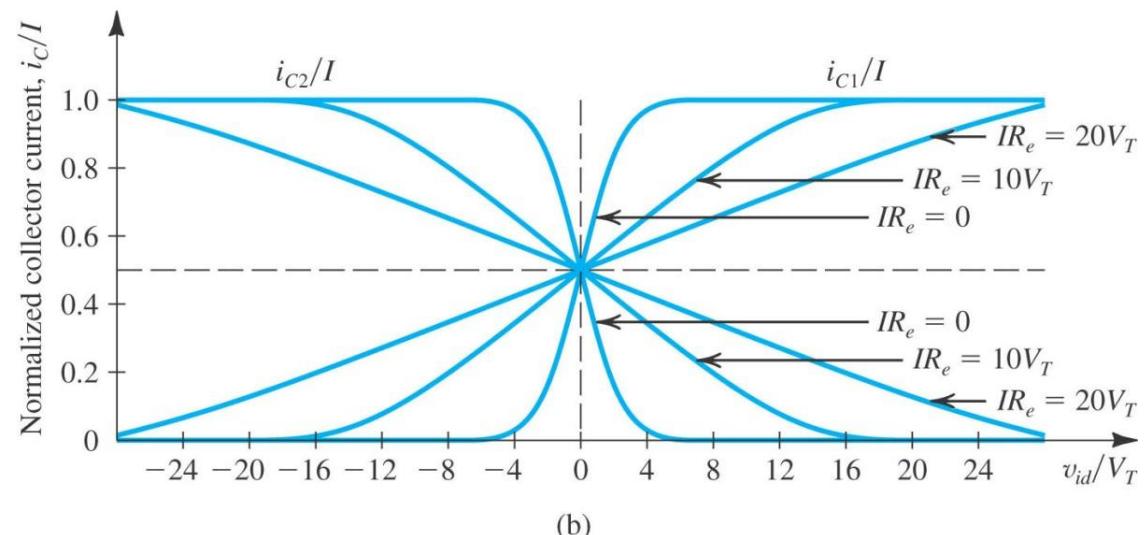
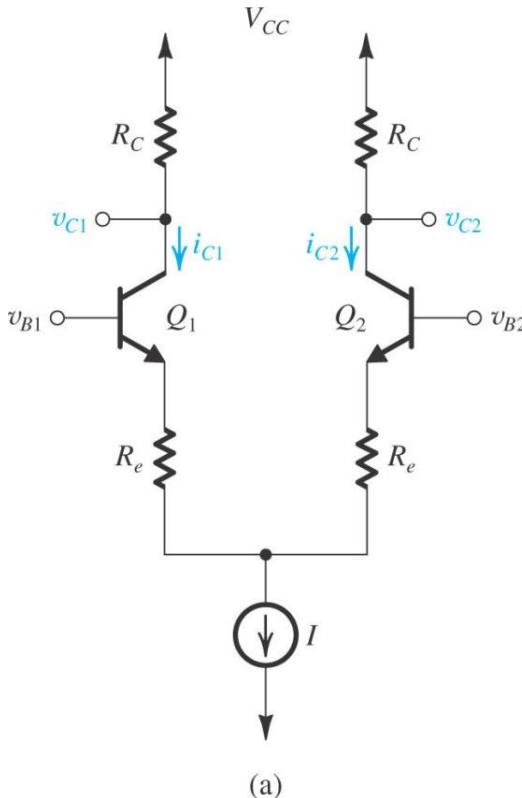
**Figure 9.16** Transfer characteristics of the BJT differential pair of Fig. 9.14 assuming  $\alpha \simeq 1$ .



# Extending the Linear Operation Range

Normalized characteristics

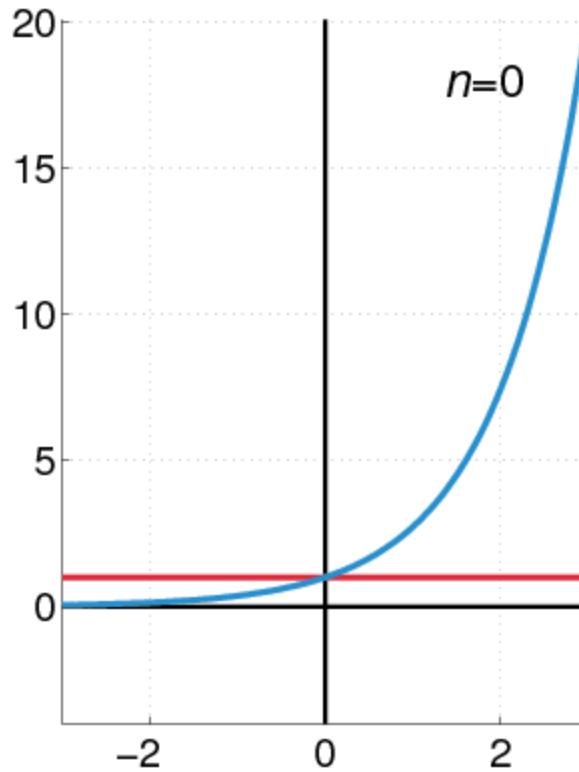
- The bias current is divided equally for  $v_{id} = 0$
- Unequal current through  $Q_1$  and  $Q_2$  for  $v_{id} \neq 0$
- A relatively small  $v_{id}$  results in complete current switching
- The linearity can be improved by emitter degeneration  $R_e$
- Transconductance and gain decrease due to emitter degeneration



**Figure 9.17** The transfer characteristics of the BJT differential pair (a) can be linearized (b) (i.e., the linear range of operation can be extended) by including resistances in the emitters.



# $e^x$ Power Series Expansion



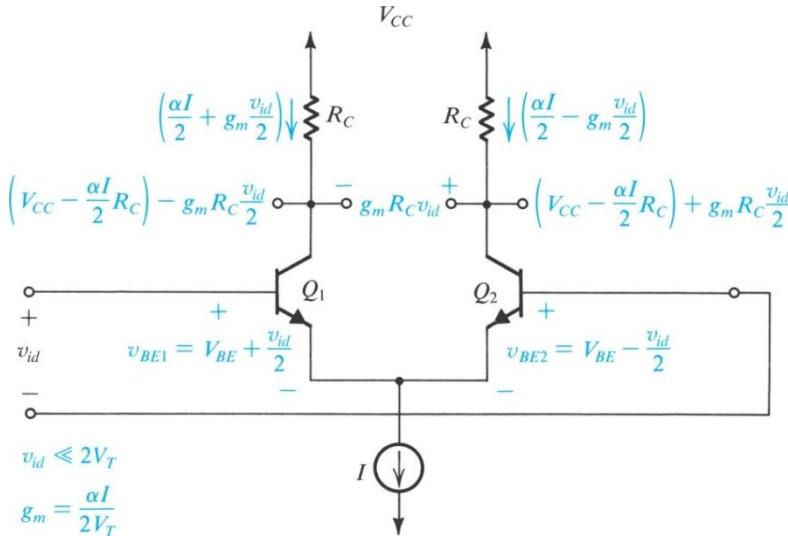
$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \dots$$

$$x = \frac{v_{id}}{2V_T}$$

[http://en.wikipedia.org/wiki/Exponential\\_function](http://en.wikipedia.org/wiki/Exponential_function)



# Small-Signal Operation



**Figure 9.18** The currents and voltages in the differential amplifier when a small differential input signal  $v_{id}$  is applied.

When  $v_{id} = 0$ , the bias current  $I$  divides equally between the two transistors of the pair. Thus each transistor is biased at an emitter current of  $I/2$ .

When a “small-signal”  $v_{id}$  is applied differentially (i.e., between the two bases), the collector current of  $Q_1$  increases by an increment  $i_c$  and that of  $Q_2$  decreases by an equal amount.

$$i_c = \frac{\alpha I}{2V_T} \frac{v_{id}}{2}$$

$$i_{C1} = \frac{\alpha I}{1 + e^{-v_{id}/V_T}}$$

$$i_{C1} = \frac{\alpha I e^{v_{id}/2V_T}}{e^{v_{id}/2V_T} + e^{-v_{id}/2V_T}}$$

$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!} = 1 + x + \frac{x^2}{2!} + \dots$$

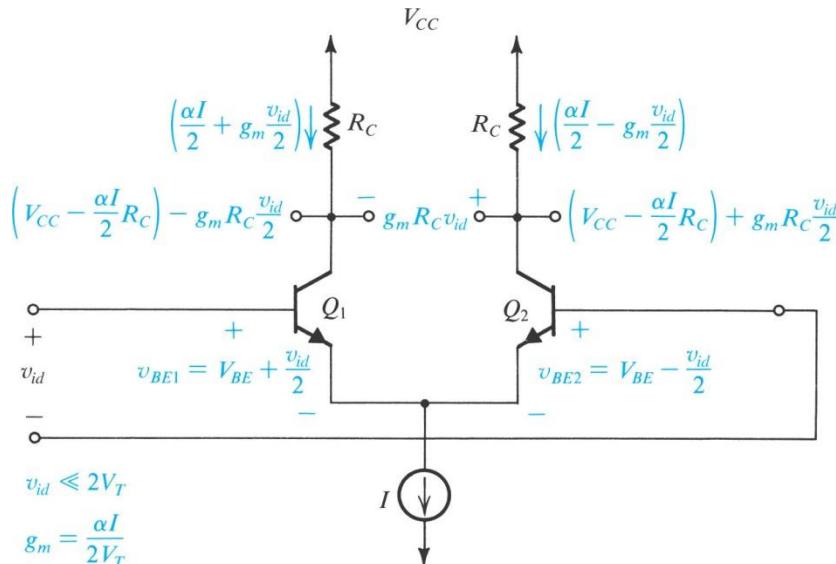
$$i_{C1} \approx \frac{\alpha I (1 + v_{id}/2V_T)}{1 + v_{id}/2V_T + 1 - v_{id}/2V_T} = \frac{\alpha I (1 + v_{id}/2V_T)}{2}$$

$$i_{C1} = \frac{\alpha I}{2} + \frac{\alpha I}{2V_T} \frac{v_{id}}{2}$$

$$i_{C2} = \frac{\alpha I}{2} - \frac{\alpha I}{2V_T} \frac{v_{id}}{2}$$



# Small-Signal Operation



**Figure 9.18** The currents and voltages in the differential amplifier when a small differential input signal  $v_{id}$  is applied.

$$i_c = \frac{\alpha I}{2V_T} \frac{v_{id}}{2}$$

$$v_{BE}|_{Q1} = V_{BE} + \frac{v_{id}}{2}$$

$$v_{BE}|_{Q2} = V_{BE} - \frac{v_{id}}{2}$$

where  $V_{BE}$  is the dc BE voltage corresponding to an emitter current of  $I/2$ . Therefore, the collector current of  $Q_1$  will increase by  $g_m v_{id}/2$  and the collector current of  $Q_2$  will decrease by  $g_m v_{id}/2$ .

$$g_m = \frac{I_C}{V_T} = \frac{\alpha I/2}{V_T}$$

$$i_c = g_m \frac{v_{id}}{2}$$



# Alternative Viewpoint

Assume the current source  $I$  to be ideal. Its incremental resistance then will be infinite. Thus the voltage  $v_{id}$  appears across a total resistance of  $2r_e$ , where

$$r_e = \frac{V_T}{I_E} = \frac{V_T}{I/2}$$

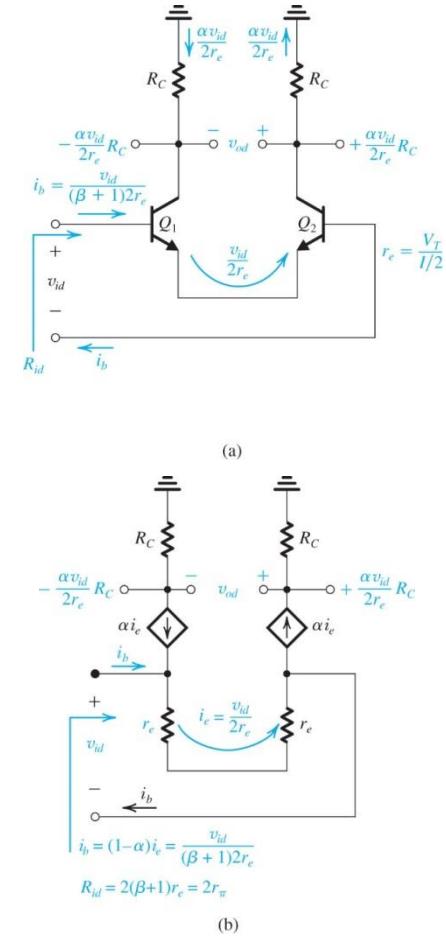
resulting in a signal current:  $i_e = \frac{v_{id}}{2r_e}$

the collector of  $Q_1$  will exhibit a current increment  $i_c$  and the collector of  $Q_2$  will exhibit a current decrement  $i_c$

$$i_c = \alpha i_e = \frac{\alpha v_{id}}{2r_e} = g_m \frac{v_{id}}{2}$$

This method of analysis is particularly useful when resistances are included in the emitters

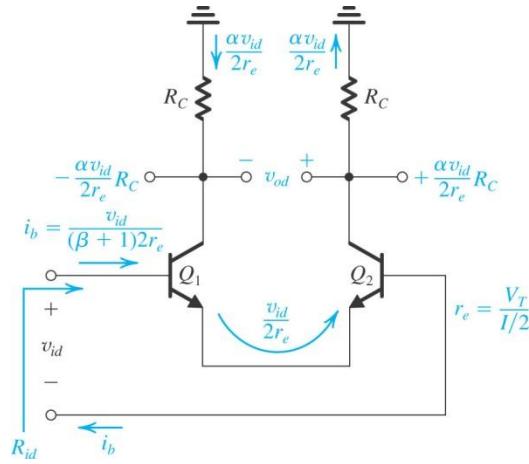
$$i_e = \frac{v_{id}}{2r_e + 2R_e}$$



**Figure 9.19** A simple technique for determining the signal currents in a differential amplifier excited by a differential voltage signal  $v_{id}$ ; dc quantities are not shown. While Fig. 9.19(a) utilizes the BJT T model implicitly, the T model of both BJTs are shown explicitly in Fig. 9.19(b).



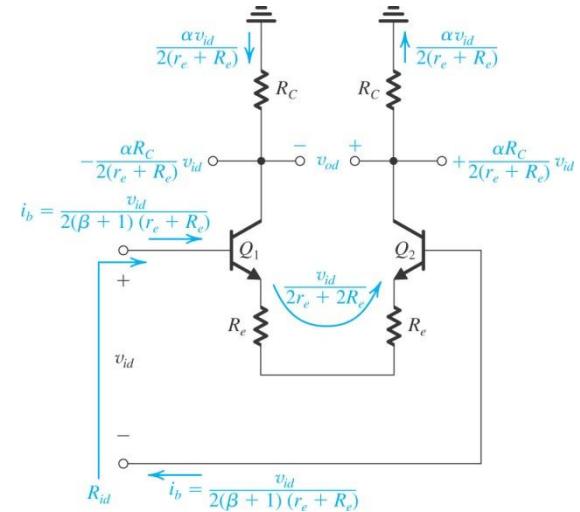
# Input Differential Resistance



**Figure 9.19** A simple technique for determining the signal currents in a differential amplifier excited by a differential voltage signal  $v_{id}$ ; dc quantities are not shown.

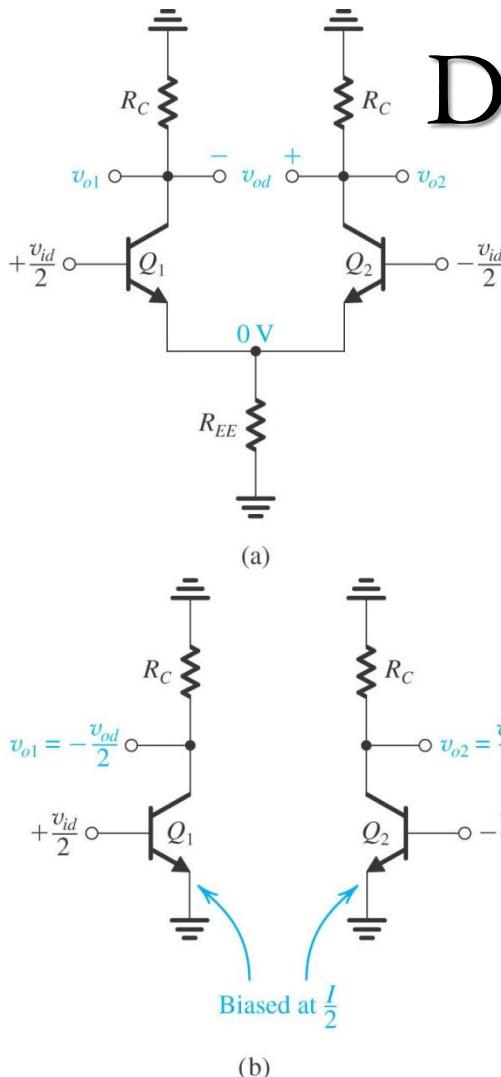
$$i_b = \frac{i_e}{\beta + 1} = \frac{v_{id}/2}{\beta + 1}$$

$$R_{id} \equiv \frac{v_{id}}{i_b} = (\beta + 1)2r_e = 2r_\pi$$



**Figure 9.20** A differential amplifier with emitter resistances. Only signal quantities are shown (in color).

$$R_{id} \equiv \frac{v_{id}}{i_b} = (\beta + 1)(2r_e + 2R_e)$$



## Differential Half-Circuit

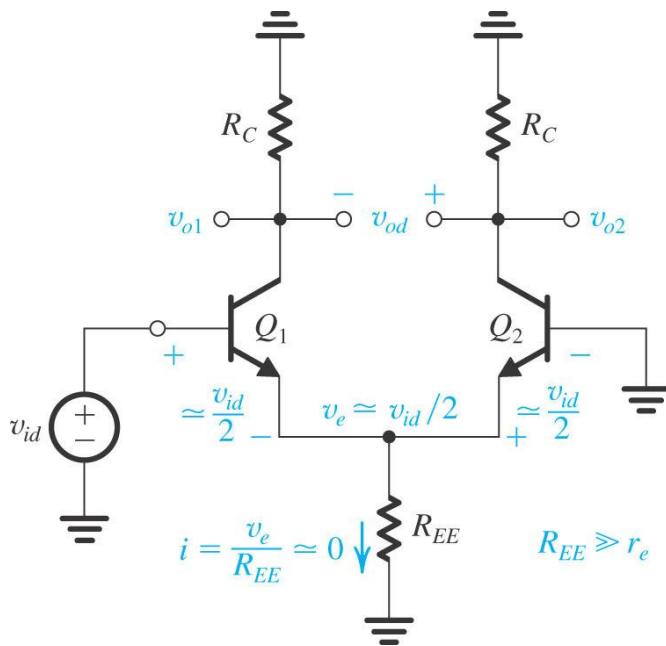
As in the MOS case, the differential gain of the BJT differential amplifier can be obtained by considering its differential half-circuit. Figure 9.21(a) shows a differential amplifier fed by a differential signal  $v_{id}$  that is applied in a complementary (push-pull or balanced) manner. That is, while the base of  $Q_1$  is raised by  $v_{id}/2$ , the base of  $Q_2$  is lowered by  $v_{id}/2$ . We have also included the output resistance  $R_{EE}$  of the bias current source. From symmetry, it follows that the signal voltage at the emitters will be zero. Thus the circuit is equivalent to the two common-emitter amplifiers shown in Fig. 9.21(b), where each of the two transistors is biased at an emitter current of  $I/2$ .

Note that the finite output resistance  $R_{EE}$  of the current source will have no effect on the operation. The equivalent circuit in Fig. 9.21(b) is valid for differential operation only.

**Figure 9.21** Equivalence of the BJT differential amplifier in (a) to the two common-emitter amplifiers in (b). This equivalence applies only for differential input signals. Either of the two common-emitter amplifiers in (b) can be used to find the differential gain, differential input resistance, frequency response, and so on, of the differential amplifier.



# Diff Amp Fed Single-Ended

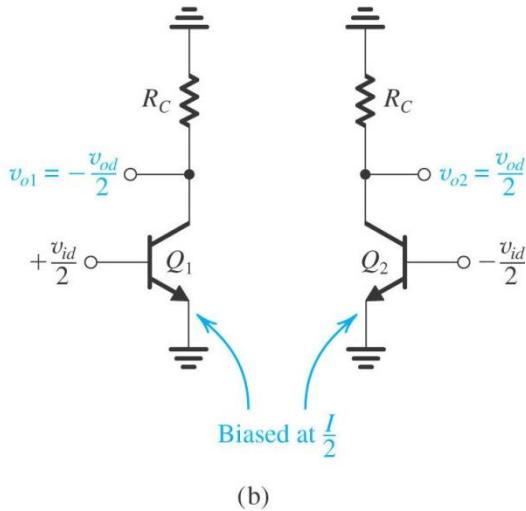


**Figure 9.22** The differential amplifier fed in a single-ended fashion.

In many applications the differential amplifier is not fed in a complementary fashion; rather, the input signal may be applied to one of the input terminals while the other terminal is grounded, as shown in Fig. 9.22. In this case the signal voltage at the emitters will not be zero, and thus the resistance  $R_{EE}$  will have an effect on the operation. Nevertheless, if  $R_{EE}$  is large ( $R_{EE} \gg r_e$ ), as is usually the case, then  $v_{id}$  will still divide equally (approximately) between the two junctions. Thus the operation of the differential amplifier in this case will be almost identical to that in the case of symmetric feed, and the common-emitter equivalence can still be employed.



# Equivalent Circuit Model



If we take the common-emitter transistor fed with  $+v_{id}/2$  as the differential half-circuit and replace the transistor with its low-frequency, equivalent-circuit model, the circuit in Fig. 9.22 results. In evaluating the model parameters  $r_\pi$ ,  $g_m$ , and  $r_o$ , we must recall that the half-circuit is biased at  $I/2$ . The voltage gain of the differential amplifier is equal to the voltage gain of the half-circuit—that is,  $v_{o1}/(v_{id}/2)$ .

$$A_d = g_m (R_C \parallel r_o)$$

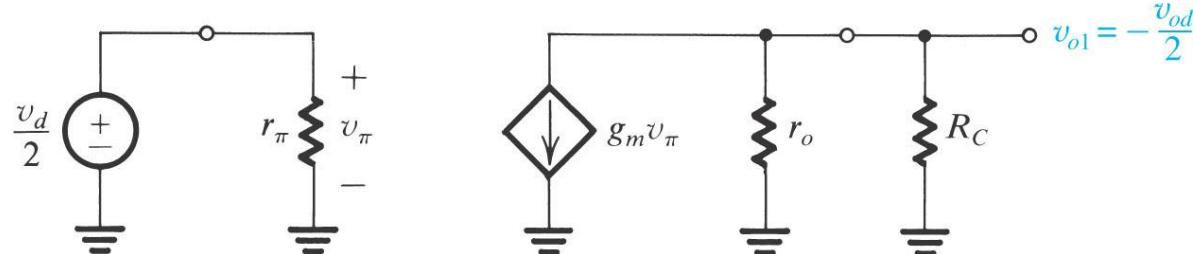


Figure 9.23 Equivalent-circuit model of the differential half-circuit formed by  $Q_1$  in Fig. 9.22(b).



# Example 9.3a

The differential amplifier in Fig. 9.24 uses transistors with  $\beta = 100$ . Evaluate the following:

- The input differential resistance  $R_{id}$ .
- The overall differential voltage gain  $v_{od}/v_{sig}$ . (neglect the effect of  $r_o$ ).

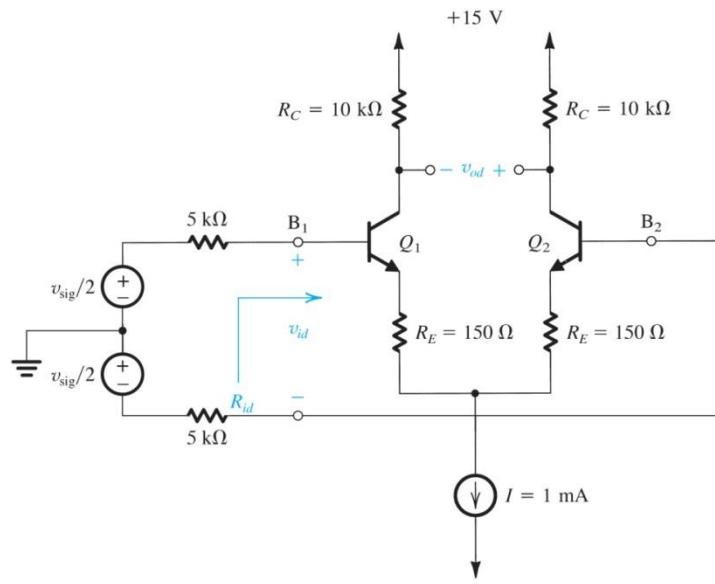


Figure 9.24 Circuit for Example 9.3.

$$r_{e1} = r_{e2} = \frac{V_T}{I_E} = \frac{25\text{mV}}{0.5\text{mA}} = 50\Omega$$

$$R_{id} \equiv \frac{v_{id}}{i_b} = (\beta + 1)(2r_e + 2R_e)$$

$$R_{id} = (101)(2 \times 50 + 2 \times 150) = 40.4\text{k}\Omega \approx 40\text{k}\Omega$$



## Example 9.3b

The differential amplifier in Fig. 9.24 uses transistors with  $\beta = 100$ . Evaluate the following:

- (b) The overall differential voltage gain  $v_{od}/v_{sig}$ . (neglect the effect of  $r_o$ ).

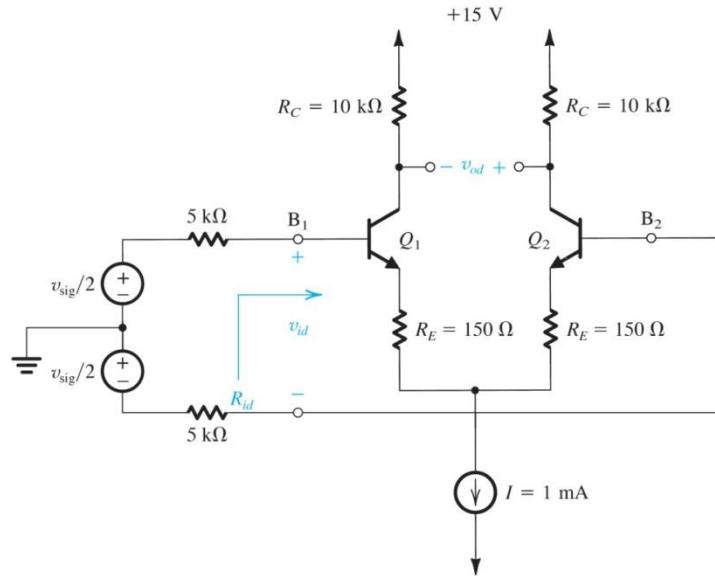


Figure 9.24 Circuit for Example 9.3.

$$\frac{v_{id}}{v_{sig}} = \frac{R_{id}}{R_{sig} + R_{id}} = \frac{40}{5+5+40} = 0.8 \text{V/V}$$

$$\frac{v_{od}}{v_{id}} = \frac{2R_C}{2(r_e + R_E)} = \frac{2 \times 10\text{k}}{2(50+150)} = 50 \text{V/V}$$

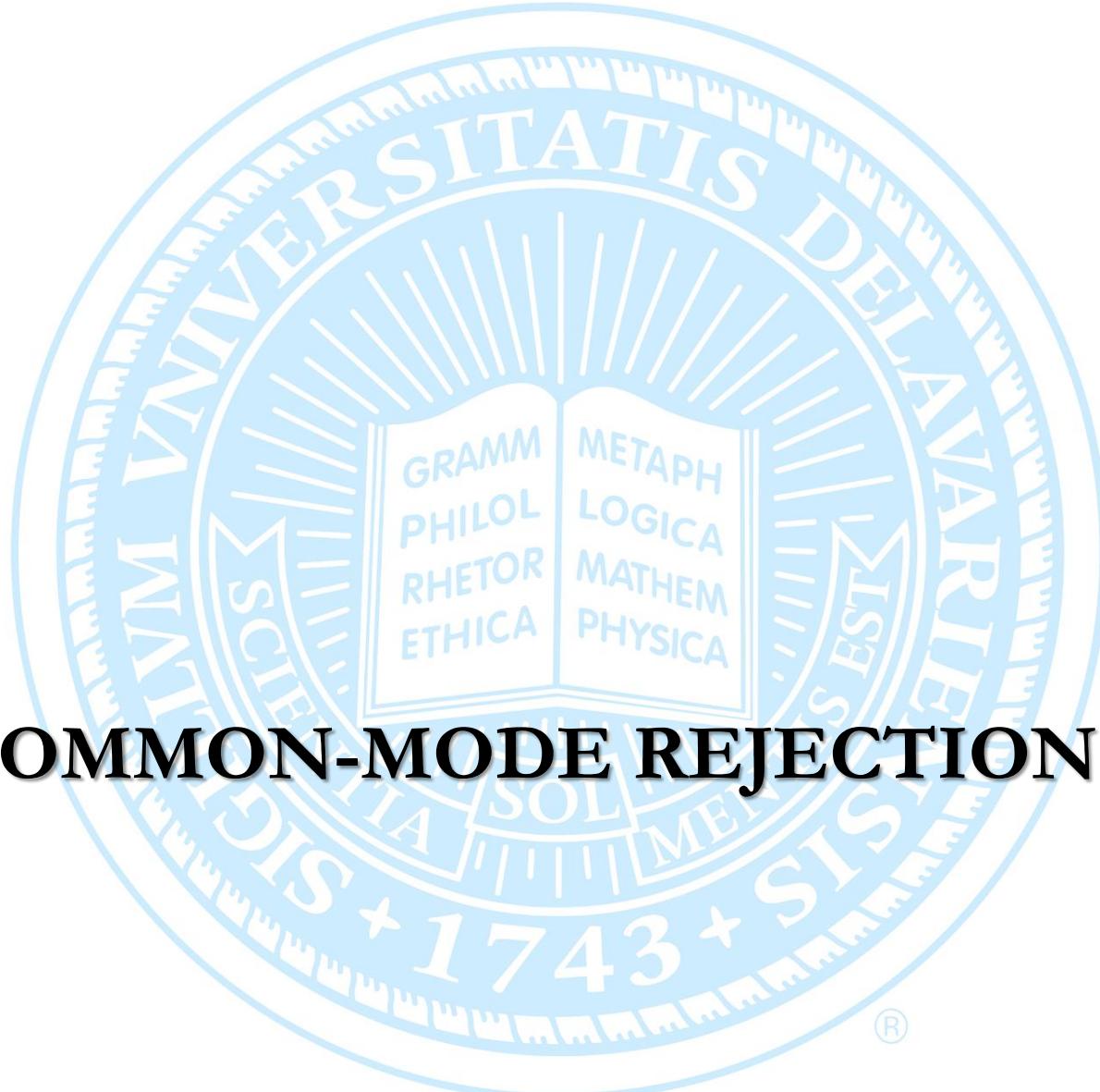
$$A_d = \frac{v_{od}}{v_{sig}} = 0.8 \text{V/V} \times 50 \text{V/V} = 40 \text{V/V}$$



# Homework #3

- Read Chapter 9
- Chapter 9 Problems:
  1. 9.1\*
  2. 9.3\*
  3. 9.5\*
  4. 9.12
  5. 9.19\*
  6. 9.26
  7. 9.28
  8. 9.34\*

\* Answers in Appendix L



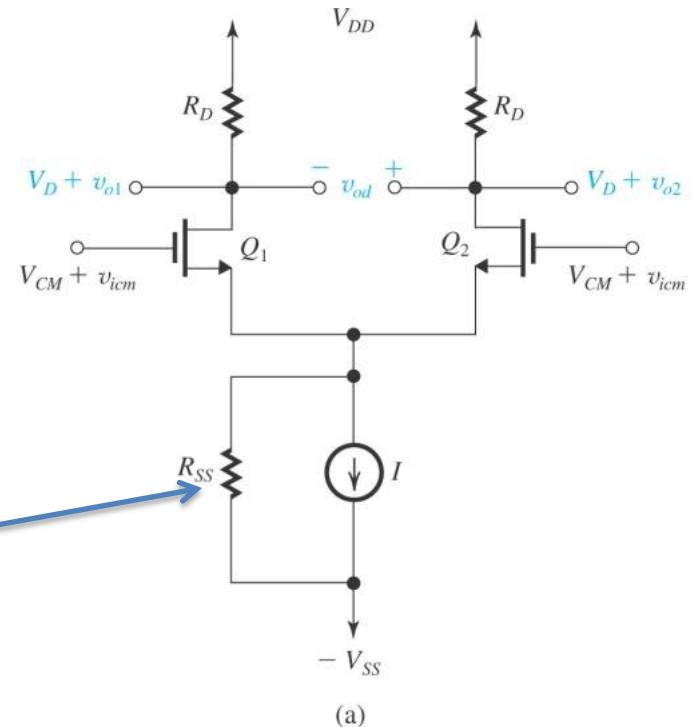
## 9.3 COMMON-MODE REJECTION



# Common-Mode Gain and Common-Mode Rejection Ratio (CMRR)

Thus far, we have seen that the differential amplifier responds to a differential input signal and completely rejects a common-mode signal. This latter point was made very clearly at the outset of our discussion of differential amplifiers and was illustrated in Example 9.1, where we saw that changes in  $V_{CM}$  over a wide range resulted in no change in the voltage at either of the two drains.

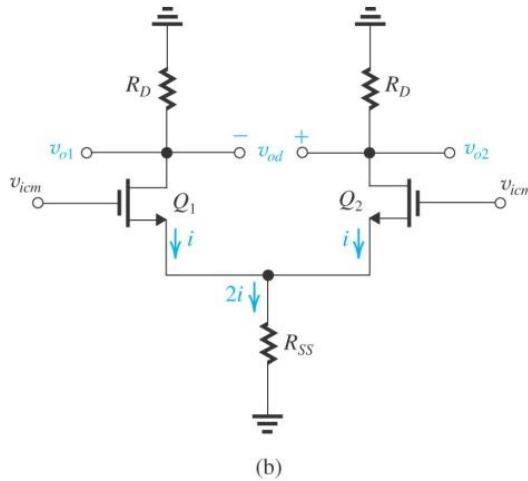
This highly desirable result is, however, a consequence of our assumption that the current source that supplies the bias current  $I$  is ideal. As we shall now show, if we consider the more realistic situation of the current source having a finite output resistance  $R_{SS}$ , the common-mode gain will no longer be zero.



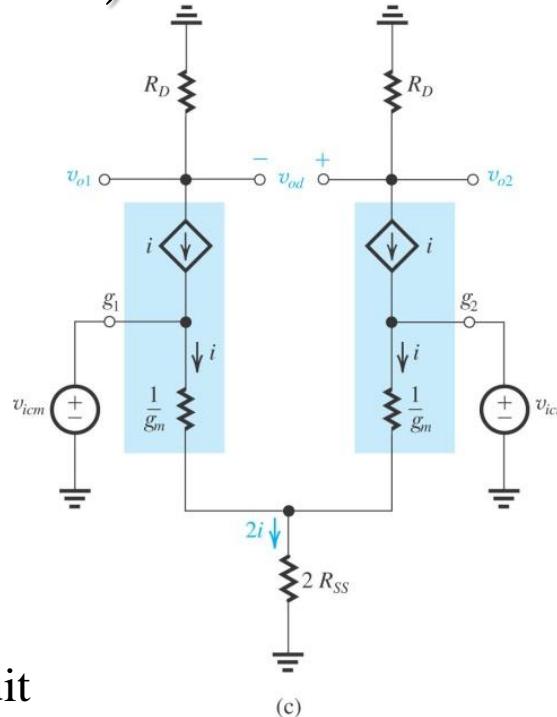
**Figure 9.25** (a) A MOS differential amplifier with a common-mode input signal  $v_{icm}$  superimposed on the input dc common-mode voltage  $V_{CM}$ .



# Common-Mode Gain and Common-Mode Rejection Ratio (CMRR)



$V_{DD}$  and  $V_{SS}$  have been replaced with a short circuit and  $I$  by an open circuit.



**Figure 9.25** (b) The amplifier circuit prepared for small-signal analysis. (c) The amplifier circuit with the transistors replaced with their T model and  $r_o$  neglected.

$$v_{icm} = \frac{i}{g_m} + 2iR_{SS}$$

$$i = \frac{v_{icm}}{1/g_m + 2R_{SS}}$$

$$v_{o1} = v_{o2} = -R_D i$$

$$v_{o1} = v_{o2} = -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm}$$

If  $2R_{SS} \gg 1/g_m$  then

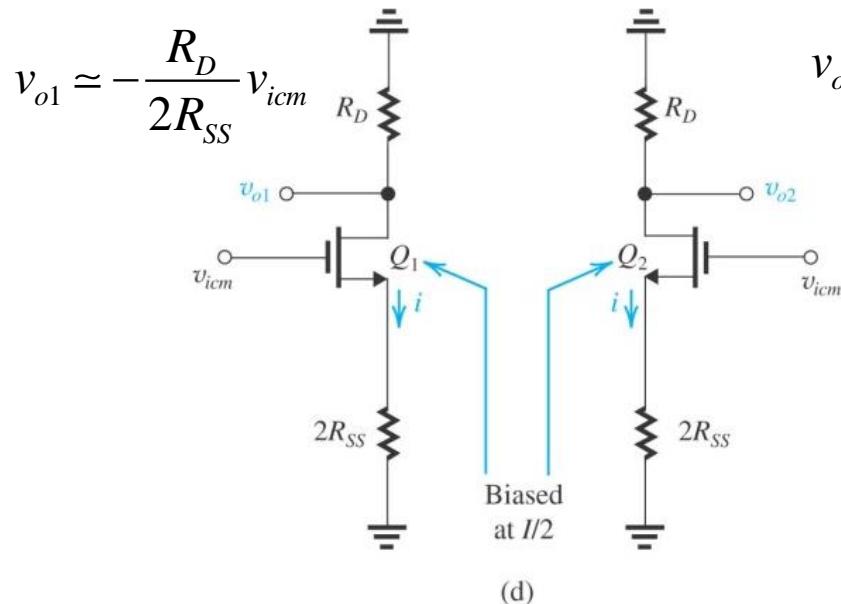
$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \approx -\frac{R_D}{2R_{SS}}$$

$$v_{od} = v_{o2} - v_{o1} = 0$$



# Common-Mode Half-Circuit

Effect of  $R_D$  mismatch ( $\Delta R_D$ )



**Figure 9.25** (d) The circuit in (b) split into its two halves; each half is said to be a “CM half-circuit.”

$$v_{o1} \simeq -\frac{R_D}{2R_{SS}} v_{icm}$$

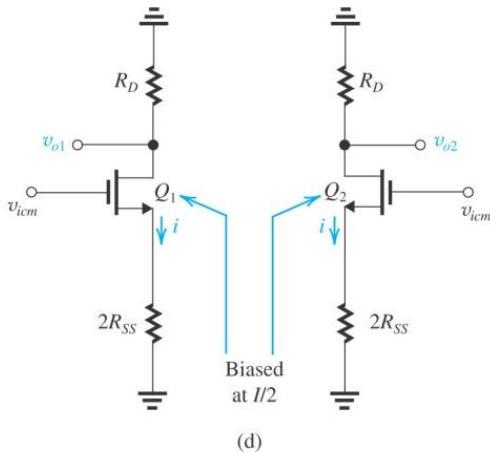
$$v_{o2} \simeq -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$$

$$v_{od} = v_{o2} - v_{o1} = \frac{-\Delta R_D}{2R_{SS}} v_{icm}$$

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = \frac{-\Delta R_D}{2R_{SS}} = \left( \frac{-R_D}{2R_{SS}} \right) \left( \frac{\Delta R_D}{R_D} \right)$$



# Common-Mode Gain and Common-Mode Rejection Ratio (CMRR)

Effect of  $R_D$  mismatch ( $\Delta R_D$ )

The **common-mode rejection ratio (CMRR)** is a measure of the effectiveness of the differential amplifier in amplifying differential-mode signals and rejecting common-mode interference is the ratio of the magnitude of its differential gain to the magnitude of its common-mode gain .

$$CMRR \equiv \frac{|A_d|}{|A_{cm}|}$$

$$CMRR(\text{dB}) = 20 \log \frac{|A_d|}{|A_{cm}|}$$

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = \frac{-\Delta R_D}{2R_{SS}} = \left( \frac{-R_D}{2R_{SS}} \right) \left( \frac{\Delta R_D}{R_D} \right)$$

$$\text{CMRR} = \frac{2g_m R_{SS}}{\Delta R_D / R_D}$$

Ideally we would want a current source with a high output resistance and a small variation in the drain resistors.



# Common-Mode Gain and Common-Mode Rejection Ratio (CMRR)

Effect of  $g_m$  Mismatch

$$g_{m1} = g_m + \frac{1}{2}\Delta g_m \quad g_{m2} = g_m - \frac{1}{2}\Delta g_m \quad g_{m1} - g_{m2} = \Delta g_m$$

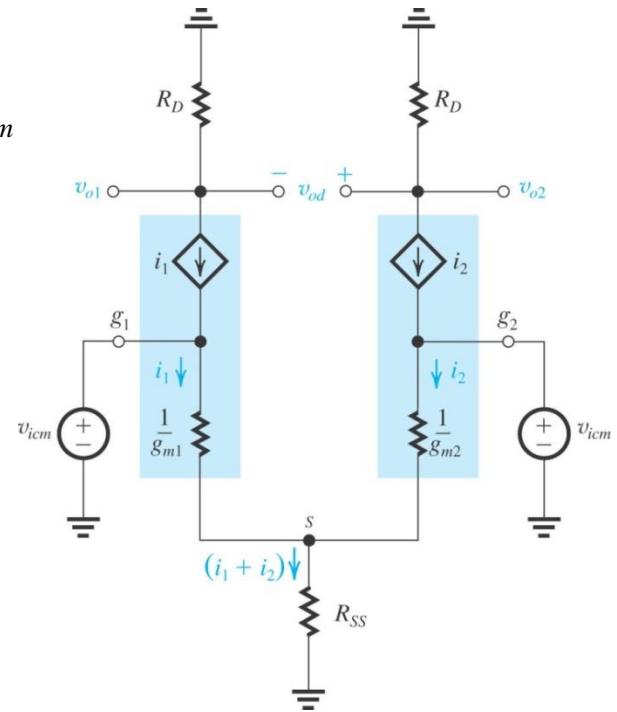
Since the circuit is no longer symmetrical, we cannot employ the common-mode half-circuit. Rather, we shall return to the original circuit of Fig. 9.25(a) and replace each of  $Q_1$  and  $Q_2$  with its T equivalent-circuit model.

$$i_1(1/g_{m1}) = i_2(1/g_{m2})$$

$$i_1 + i_2 = i_1 \left( 1 + \frac{g_{m2}}{g_{m1}} \right)$$

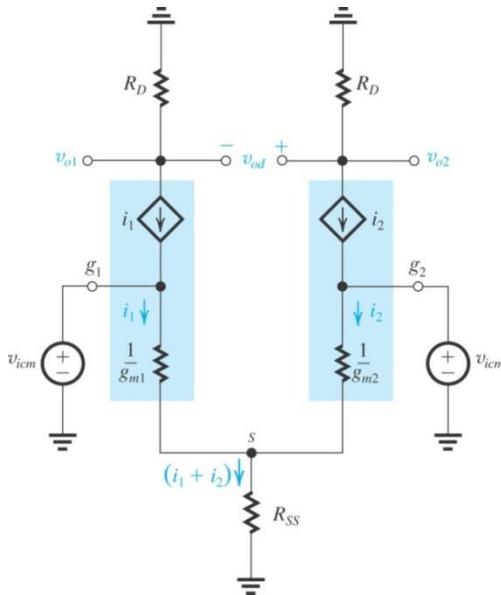
$$v_{icm} = \frac{i_1}{g_{m1}} + (i_1 + i_2)R_{SS}$$

$$= \frac{i_1}{g_{m1}} + i_1 \left( 1 + \frac{g_{m2}}{g_{m1}} \right) R_{SS}$$





# Common-Mode Gain and Common-Mode Rejection Ratio (CMRR)



**Figure 9.25 (c)** The amplifier circuit with the transistors replaced with their T model and  $r_o$  neglected.

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = \frac{\Delta g_m R_D}{1 + 2g_m R_{SS}}$$

Effect of  $g_m$  Mismatch

$$v_{icm} = \frac{i_1}{g_{m1}} + i_1 \left( 1 + \frac{g_{m2}}{g_{m1}} \right) R_{SS}$$

$$i_1 = \frac{g_{m1} v_{icm}}{1 + (g_{m1} + g_{m2}) R_{SS}}$$

$$i_2 = \frac{g_{m2} v_{icm}}{1 + (g_{m1} + g_{m2}) R_{SS}}$$

$$v_{o1} = -i_1 R_D = -\frac{g_{m1} R_D}{1 + (g_{m1} + g_{m2}) R_{SS}} v_{icm}$$

$$v_{o2} = -i_2 R_D = -\frac{g_{m2} R_D}{1 + (g_{m1} + g_{m2}) R_{SS}} v_{icm}$$

$$v_{od} = v_{o2} - v_{o1} = \frac{(g_{m1} - g_{m2}) R_D}{1 + (g_{m1} + g_{m2}) R_{SS}} v_{icm} = \frac{\Delta g_m R_D}{1 + 2g_m R_{SS}} v_{icm}$$

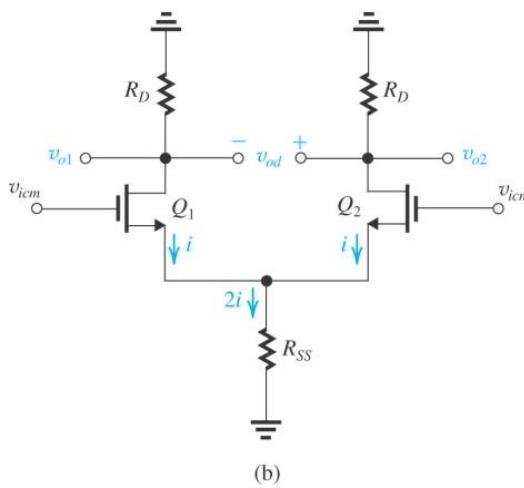
$$A_{cm} \approx \left( \frac{R_D}{2R_{SS}} \right) \left( \frac{\Delta g_m}{g_m} \right)$$

$$\text{CMRR} = \left( 2g_m R_{SS} \right) \left/ \left( \frac{\Delta g_m}{g_m} \right) \right.$$



## Example 9.4a

In this example we consider the design of the current source that supplies the bias current of a MOS differential amplifier. Let it be required to achieve a CMRR of 100 dB and assume that the only source of mismatch between  $Q_1$  and  $Q_2$  is a 2% mismatch in their  $W/L$  ratios. Let  $I = 200 \mu\text{A}$  and assume that all transistors are to be operated at  $V_{OV} = 0.2 \text{ V}$ . For the 0.18- $\mu\text{m}$  CMOS fabrication process available,  $V_A' = 5 \text{ V}/\mu\text{m}$ . If a simple current source is utilized for  $I$ , what channel length is required? If a cascode current source is utilized, what channel length is needed for the two transistors in the cascode?



$$g_m = \sqrt{2(\mu_n c_{ox}) \left( \frac{W}{L} \right) I_D} \quad \frac{\Delta g_m}{g_m} = \frac{\sqrt{1.02}}{\sqrt{1}} = 1.01 = 1\%$$

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{0.2 \text{ mA}}{0.2 \text{ V}} = 1 \text{ mA/V}$$

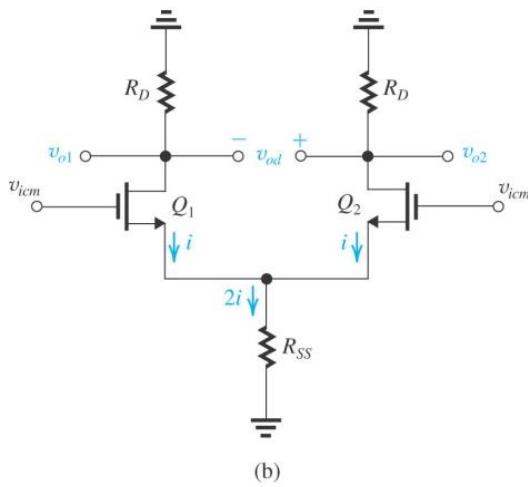
$$\text{CMRR} = \left( 2g_m R_{SS} \right) \left/ \left( \frac{\Delta g_m}{g_m} \right) \right. = 100 \text{ dB} = 10^5$$

$$R_{SS} = 10^5 \left( \frac{\Delta g_m}{g_m} \right) \left( \frac{1}{2g_m} \right) = 10^5 (0.01) \left( \frac{1 \text{ V}}{2 \text{ mA}} \right) = 500 \text{ k}\Omega$$



## Example 9.4b

In this example we consider the design of the current source that supplies the bias current of a MOS differential amplifier. Let it be required to achieve a CMRR of 100 dB and assume that the only source of mismatch between  $Q_1$  and  $Q_2$  is a 2% mismatch in their  $W/L$  ratios. Let  $I = 200 \mu\text{A}$  and assume that all transistors are to be operated at  $V_{OV} = 0.2 \text{ V}$ . For the 0.18- $\mu\text{m}$  CMOS fabrication process available,  $V'_A = 5 \text{ V}/\mu\text{m}$ . If a simple current source is utilized for  $I$ , what channel length is required? If a cascode current source is utilized, what channel length is needed for the two transistors in the cascode?



**Simple current source**

$$r_o = R_{SS} = 500 \text{ k}\Omega$$

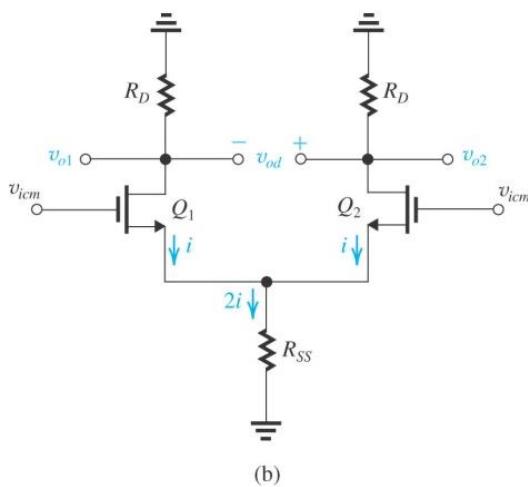
$$V_A = r_o I = 500 \text{ k}\Omega \times 0.2 \text{ mA} = 100 \text{ V}$$

$$L = \frac{100\text{V}}{5\text{V}/\mu\text{m}} = 20\mu\text{m}$$



## Example 9.4c

In this example we consider the design of the current source that supplies the bias current of a MOS differential amplifier. Let it be required to achieve a CMRR of 100 dB and assume that the only source of mismatch between  $Q_1$  and  $Q_2$  is a 2% mismatch in their  $W/L$  ratios. Let  $I = 200 \mu\text{A}$  and assume that all transistors are to be operated at  $V_{OV} = 0.2 \text{ V}$ . For the 0.18- $\mu\text{m}$  CMOS fabrication process available,  $V_A' = 5 \text{ V}/\mu\text{m}$ . If a simple current source is utilized for  $I$ , what channel length is required? If a cascode current source is utilized, what channel length is needed for the two transistors in the cascode?



**Cascode current source**

$$g_m = \frac{2I}{V_{OV}}$$

$$R_{ss} = (g_m r_0) r_0 = 500 \text{ k}\Omega$$

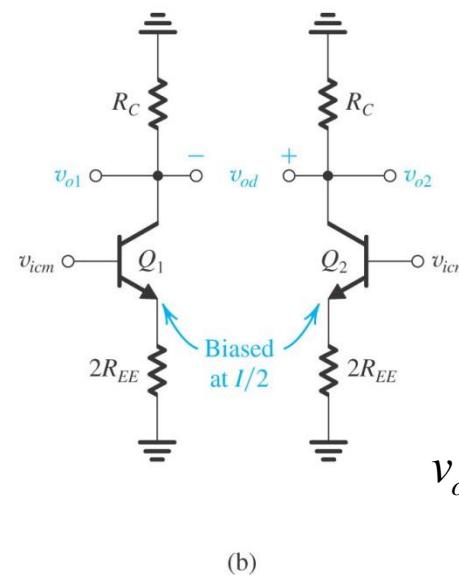
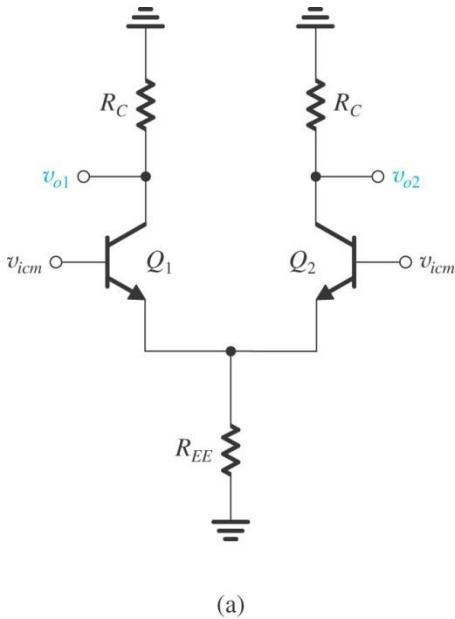
$$r_o = \sqrt{\frac{R_{ss}}{g_m}} = \sqrt{\frac{500 \text{ k}\Omega}{2 \text{ mA/V}}} = 15.81 \text{ k}\Omega$$

$$V_A = r_o I = 15.81 \text{ k}\Omega \times 0.2 \text{ mA} = 3.16 \text{ V}$$

$$L = \frac{3.16 \text{ V}}{5 \text{ V}/\mu\text{m}} = 0.63 \text{ }\mu\text{m}$$



# BJT Common-Mode Gain and CMRR



**Figure 9.26** (a) The differential amplifier fed by a common-mode input signal  $v_{icm}$ . (b) Equivalent “half-circuits” for common-mode calculations.

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = -\frac{\alpha \Delta R_C}{2R_{EE} + r_e} \approx -\left(\frac{R_C}{2R_{EE}}\right)\left(\frac{\Delta R_C}{R_C}\right)$$

$$A_d = \frac{v_{od}}{v_{id}} = \frac{v_{c2} - v_{c1}}{v_{id}} = g_m R_C$$

$$v_{o1} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \quad v_{o2} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm}$$

$$v_{od} = v_{o2} - v_{o1} = 0 \quad A_{cm} = 0$$

If the collector resistors are not exact matches

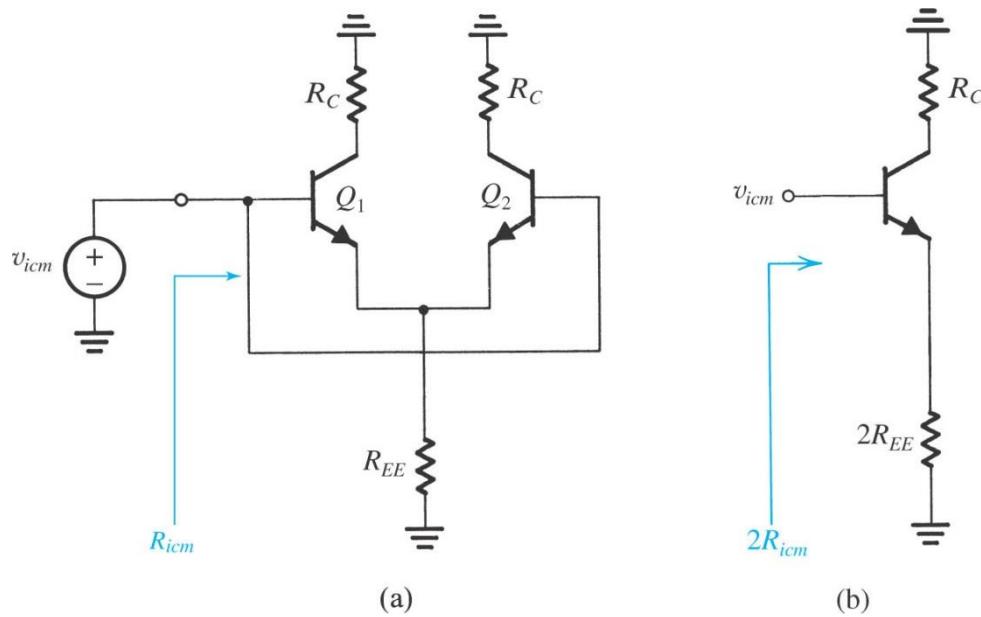
$$v_{o1} = -\frac{\alpha R_C}{r_e + 2R_{EE}} v_{icm} \quad v_{o2} = -\frac{\alpha (R_C + \Delta R_C)}{r_e + 2R_{EE}} v_{icm}$$

$$v_{od} = v_{o2} - v_{o1} = -\frac{\alpha \Delta R_C}{2R_{EE} + r_e} v_{icm}$$

$$CMRR = \frac{|A_d|}{|A_{cm}|} = \frac{\left(2g_m R_{EE}\right)}{\left(\frac{\Delta R_C}{R_C}\right)}$$



# Common-Mode Input Resistance



**Figure 9.27** (a) Definition of the input common-mode resistance  $R_{icm}$ . (b) The equivalent common-mode half-circuit.

The definition of the common-mode input resistance  $R_{icm}$  is illustrated in Fig. 9.27(a). Figure 9.27(b) shows the equivalent common-mode half-circuit; its input resistance is  $2R_{icm}$ . The value of  $2R_{icm}$  can be determined by analyzing the circuit of Fig. 9.27(b) while taking  $r_o$  into account (because  $R_{EE}$  and  $R_C$  can be equal to, or larger than,  $r_o$ ).

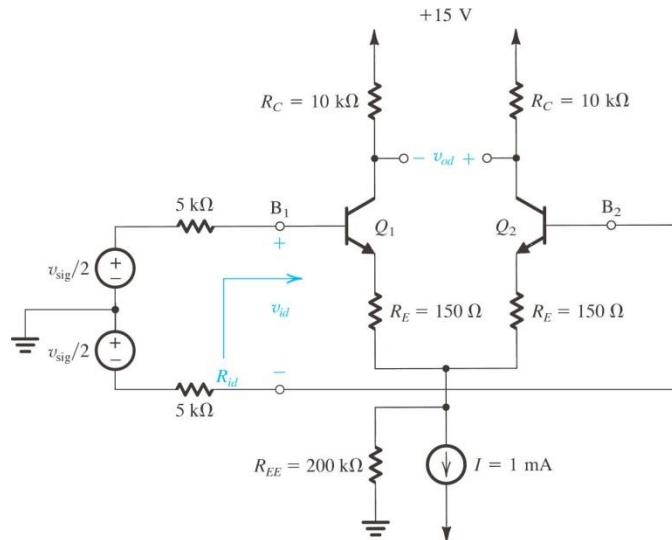
$$R_{icm} \simeq \beta R_{EE} \frac{1 + R_C / \beta r_o}{1 + \frac{R_C + 2R_{EE}}{r_o}}$$



# Example 9.5a

For the differential amplifier analyzed in Example 9.3, let the bias-current source have an output resistance  $R_{EE} = 200 \text{ k}\Omega$ . Evaluate:

- the worst-case common-mode gain if the two collector resistances are accurate to within  $\pm 1\%$ .
- the CMRR in dB.
- the input common-mode resistance (assuming the Early voltage  $V_A = 100 \text{ V}$ ).



$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = \frac{\alpha \Delta R_C}{2R_{EE} + r_e}$$
$$A_{cm} \cong \left( \frac{R_C}{2R_{EE}} \right) \left( \frac{\Delta R_C}{R_C} \right)$$
$$\Delta R_{C \max} = 0.02 R_C$$
$$A_{cm} = \left( \frac{10 \text{ k}\Omega}{2(200 \text{ k}\Omega)} \right) \left( \frac{0.02 R_C}{R_C} \right) = \frac{10}{400} (0.02) = 5 \times 10^{-4} \frac{\text{V}}{\text{V}}$$

Figure 9.24 Circuit for Example 9.3.



## Example 9.5b

For the differential amplifier analyzed in Example 9.3, let the bias-current source have an output resistance  $R_{EE} = 200 \text{ k}\Omega$ . Evaluate:

- (a) the worst-case common-mode gain if the two collector resistances are accurate to within  $\pm 1\%$ .  
(b) the CMRR in dB.

$$A_d = \frac{v_{od}}{v_{sig}} = 40 \text{ V/V} \quad A_{cm} = 5 \times 10^{-4} \frac{\text{V}}{\text{V}}$$

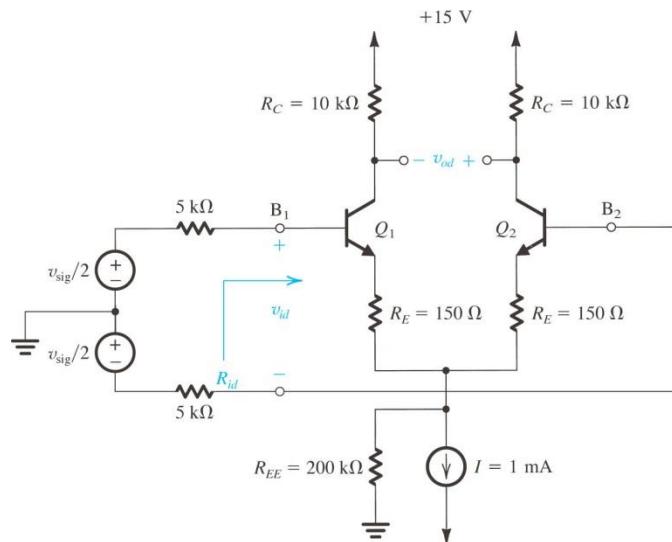


Figure 9.24 Circuit for Example 9.3.

$$\text{CMRR} = 20 \log \left( \frac{|A_d|}{|A_{cm}|} \right) = 20 \log \left( \frac{|40 \text{ V/V}|}{|5 \times 10^{-4} \text{ V/V}|} \right) = 98.06 \text{ dB}$$

- (c) the input common-mode resistance (assuming the Early voltage  $V_A = 100 \text{ V}$ ).

$$r_o = \frac{V_A}{I_C} = \frac{2V_A}{I} = \frac{2(100 \text{ V})}{1 \text{ mA}} = 200 \text{ k}\Omega$$

$$R_{icm} \simeq \beta R_{EE} \frac{1 + R_C / \beta r_o}{1 + \frac{R_C + 2R_{EE}}{r_o}} = 6.6 \text{ M}\Omega$$

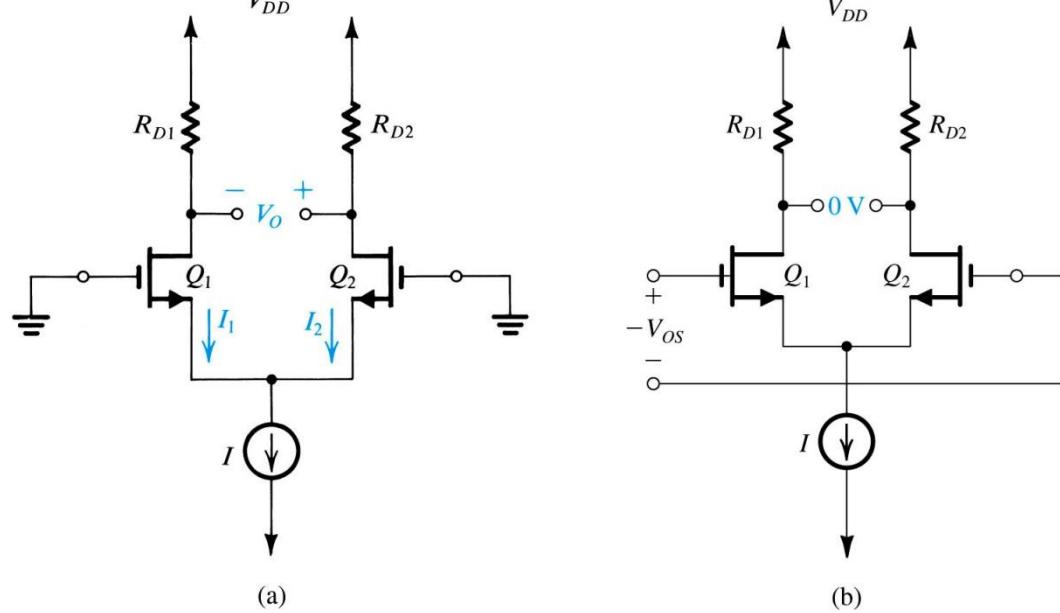


## 9.4 DC OFFSET



# Input Offset Voltage – MOSFET Pair

practical circuits exhibit mismatches that result in a dc output voltage  $V_O$  even with both inputs grounded. We call  $V_O$  the output dc offset voltage. More commonly, we divide  $V_O$  by the differential gain of the amplifier,  $A_d$ , to obtain a quantity known as the input offset voltage,  $V_{OS}$ ,



**Figure 9.28** (a) The MOS differential pair with both inputs grounded. Owing to device and resistor mismatches, a finite dc output voltage  $V_O$  results. (b) Application of a voltage equal to the input offset voltage  $V_{OS}$  to the input terminals with opposite polarity reduces  $V_O$  to zero.

$$V_{OS} = \frac{V_O}{A_d}$$

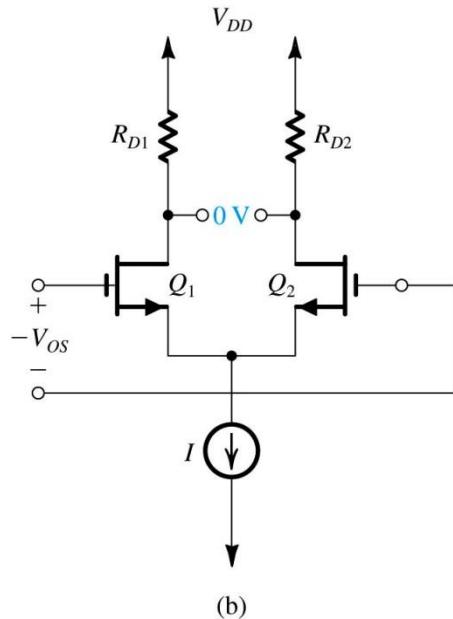
Three factors contribute to the dc offset voltage of the MOS differential pair:

1. mismatch in load resistances,
2. mismatch in  $W/L$ ,
3. mismatch in  $V_t$ .

We shall consider the three contributing factors one at a time.



# Mismatch in Load Resistances - FET



$$R_{D1} = R_D + \frac{\Delta R_D}{2} \quad R_{D2} = R_D - \frac{\Delta R_D}{2}$$

Because  $Q_1$  and  $Q_2$  are matched, the current  $I$  will split equally between them.

$$V_{D1} = V_{DD} - \frac{I}{2} \left( R_D + \frac{\Delta R_D}{2} \right) \quad V_{D2} = V_{DD} - \frac{I}{2} \left( R_D - \frac{\Delta R_D}{2} \right)$$

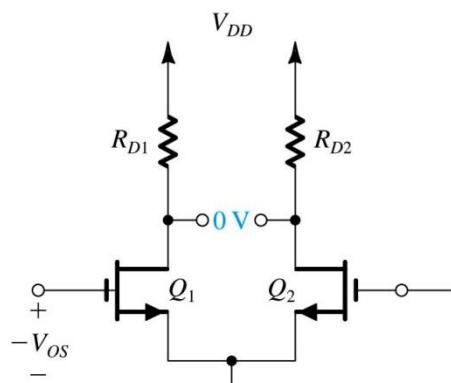
$$V_O = V_{D2} - V_{D1} = \left( \frac{I}{2} \right) \Delta R_D$$

$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

$$V_{OS} = \frac{V_O}{A_d} = \left( \frac{V_{OV}}{2} \right) \left( \frac{\Delta R_D}{R_D} \right)$$



# Mismatch in $W/L$ Ratios



$$\left(\frac{W}{L}\right)_1 = \frac{W}{L} + \frac{1}{2}\Delta\left(\frac{W}{L}\right) \quad \left(\frac{W}{L}\right)_2 = \frac{W}{L} - \frac{1}{2}\Delta\left(\frac{W}{L}\right)$$

Such a mismatch causes the current  $I$  to no longer divide equally between  $Q_1$  and  $Q_2$ . Rather, because  $V_{GS1} = V_{GS2}$ , the current conducted by each of  $Q_1$  and  $Q_2$  will be proportional to its  $W/L$  ratio:

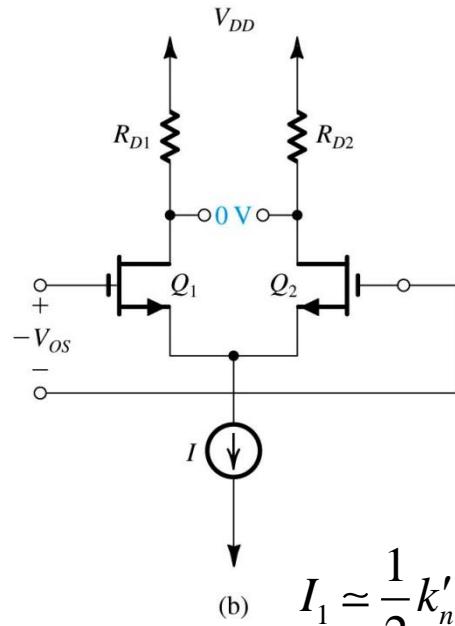
$$I_1 = \frac{I}{2} \left( 1 + \frac{\Delta(W/L)}{2(W/L)} \right) \quad I_2 = \frac{I}{2} \left( 1 - \frac{\Delta(W/L)}{2(W/L)} \right)$$

$$I_2 - I_1 = \frac{I}{2} \frac{\Delta(W/L)}{(W/L)}$$

$$V_{OS} = \left( \frac{V_{OV}}{2} \right) \left( \frac{\Delta(W/L)}{(W/L)} \right)$$



# Mismatch in Threshold Voltages



$$V_{t1} = V_t + \frac{\Delta V_t}{2}$$

$$V_{t1} = V_t - \frac{\Delta V_t}{2}$$

$$I_1 = \frac{1}{2} k'_n \frac{W}{L} \left( V_{GS} - V_t - \frac{\Delta V_t}{2} \right)^2$$

$$= \frac{1}{2} k'_n \frac{W}{L} \left( V_{GS} - V_t \right)^2 \left[ 1 - \frac{\Delta V_t}{2(V_{GS} - V_t)} \right]^2$$

$$(b) \quad I_1 \approx \frac{1}{2} k'_n \frac{W}{L} \left( V_{GS} - V_t \right)^2 \left( 1 - \frac{\Delta V_t}{V_{GS} - V_t} \right) \quad I_2 \approx \frac{1}{2} k'_n \frac{W}{L} \left( V_{GS} - V_t \right)^2 \left( 1 + \frac{\Delta V_t}{V_{GS} - V_t} \right)$$

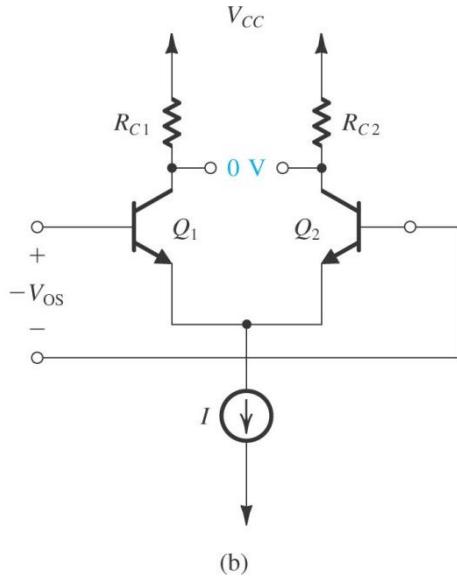
$$\frac{1}{2} k'_n \frac{W}{L} \left( V_{GS} - V_t \right)^2 = \frac{I}{2}$$

$$\Delta I = I_2 - I_1 = \frac{I}{2} \frac{\Delta V_t}{V_{GS} - V_t} = \frac{I}{2} \frac{\Delta V_t}{V_{OV}}$$

$$V_{OS} = \Delta V_t$$



# Mismatch in Load Resistances - BJT



$$R_{C1} = R_C + \frac{\Delta R_C}{2} \quad R_{C2} = R_C - \frac{\Delta R_C}{2}$$

Because  $Q_1$  and  $Q_2$  are matched, the current  $I$  will split equally between them.

$$V_{C1} = V_{CC} - \frac{\alpha I}{2} \left( R_C + \frac{\Delta R_C}{2} \right) \quad V_{C2} = V_{CC} - \frac{\alpha I}{2} \left( R_C - \frac{\Delta R_C}{2} \right)$$

$$V_O = V_{C2} - V_{C1} = \alpha \left( \frac{I}{2} \right) \Delta R_C$$

$$A_d \equiv \frac{V_{od}}{V_{id}} = \frac{V_{o2} - V_{o1}}{V_{id}} = g_m R_C$$

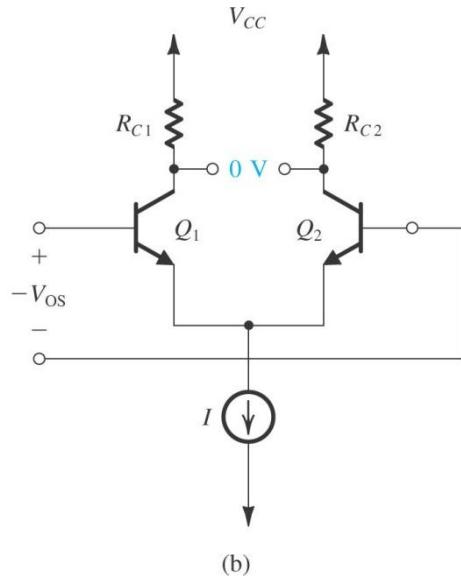
$$V_{OS} = \frac{V_O}{A_d} = \frac{\alpha \frac{I}{2} \Delta R_C}{g_m R_C}$$

$$|V_{OS}| = V_T \left( \frac{\Delta R_C}{R_C} \right)$$

**Figure 9.29** (a) The BJT differential pair with both inputs grounded. Device mismatches result in a finite dc output  $V_O$ .  
(b) Application of the input offset voltage  $V_{OS} \equiv V_O/A_d$  to the input terminals with opposite polarity reduces  $V_O$  to zero.



# Mismatch in EBJ Area Ratios



Such an area mismatch causes the scale current  $I_S$  to no longer be the same.

$$I_{S1} = I_S + \frac{\Delta I_S}{2}$$

$$I_{S2} = I_S - \frac{\Delta I_S}{2}$$

$$I_{E1} = \frac{I}{2} \left( 1 + \frac{\Delta I_S}{2I_S} \right)$$

$$I_{E2} = \frac{I}{2} \left( 1 - \frac{\Delta I_S}{2I_S} \right)$$

$$V_o = \alpha \left( \frac{I}{2} \right) \left( \frac{\Delta I_S}{I_S} \right) R_C$$

$$|V_{os}| = V_T \left( \frac{\Delta I_s}{I_s} \right)$$



# Input Bias and Offset Currents of the Bipolar Differential Amplifier

In a perfectly symmetric differential pair the two input terminals carry equal dc currents;

$$I_{B1} = I_{B2} = \frac{I/2}{\beta + 1} \quad I_B \equiv \frac{I_{B1} + I_{B2}}{2}$$

Mismatches in the amplifier circuit and most importantly a mismatch in  $\beta$  make the two input dc currents unequal. The resulting difference is the **input offset current**,  $I_{OS}$ , given as  $I_{OS} = |I_{B1} - I_{B2}|$

$$\beta_1 = \beta + \frac{\Delta\beta}{2} \quad I_{B1} = \frac{I}{2} \frac{1}{\beta + 1 + \Delta\beta/2} \approx \frac{I}{2} \frac{1}{\beta + 1} \left(1 - \frac{\Delta\beta}{2\beta}\right)$$

$$\beta_2 = \beta - \frac{\Delta\beta}{2} \quad I_{B2} = \frac{I}{2} \frac{1}{\beta + 1 - \Delta\beta/2} \approx \frac{I}{2} \frac{1}{\beta + 1} \left(1 + \frac{\Delta\beta}{2\beta}\right)$$

$$I_{OS} = \frac{I}{2(\beta + 1)} \left( \frac{\Delta\beta}{\beta} \right) = I_B \left( \frac{\Delta\beta}{\beta} \right)$$



# Comparison for MOS and BJT Differential Pairs

## MOSFET Diff Pairs

$$V_{os} = \sqrt{\left(\frac{V_{ov}}{2} \frac{\Delta R_D}{R_D}\right)^2 + \left(\frac{V_{ov}}{2} \frac{\Delta(W/L)}{(W/L)}\right)^2 + (\Delta V_t)^2}$$

## BJT Diff Pairs

$$V_{os} = V_T \sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2}$$

Bipolar differential pair typically has smaller input offset voltage

$$I_{os} = I_B \left( \frac{\Delta \beta}{\beta} \right)$$

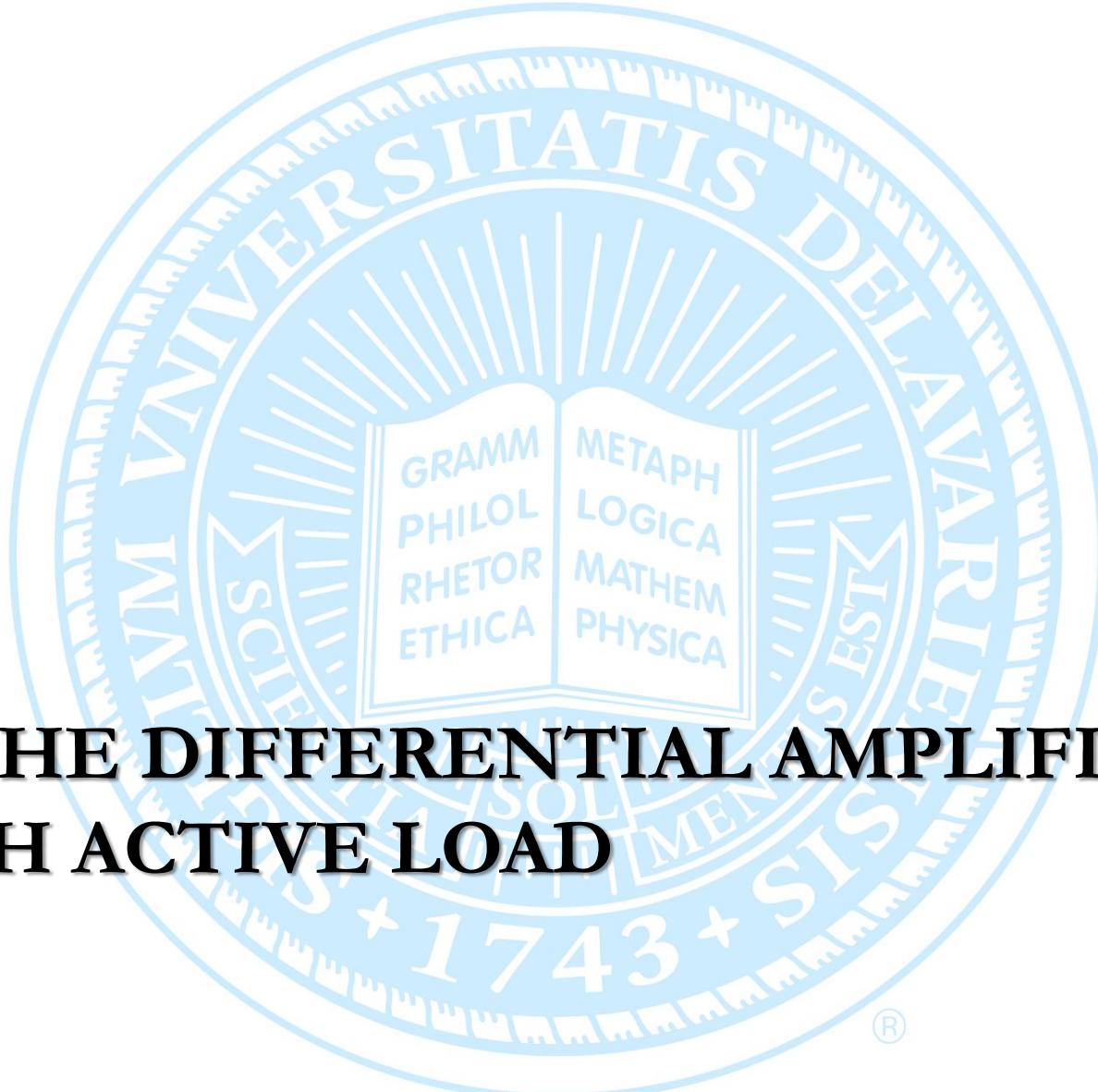
Bipolar differential pair suffers from input offset current



# Homework #4

- Read Chapter 9
- Chapter 9 Problems:
  1. 9.61\*
  2. 9.73
  3. 9.74\*
  4. 9.77\*
  5. 9.81\*
  6. 9.82

\* Answers in Appendix L



## 9.5 THE DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

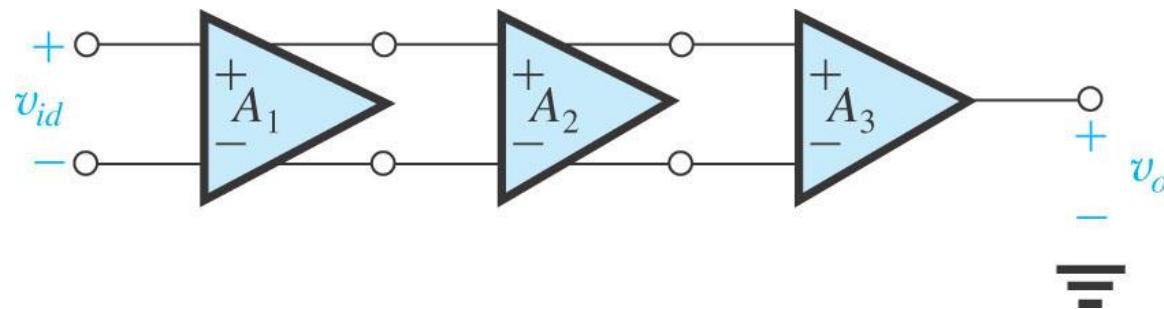


# Differential Amplifiers

Taking the output differentially has two major advantages:

1. It decreases the common-mode gain and increases the common-mode rejection ratio (CMRR) dramatically. Recall that while the drain (collector) voltages change somewhat in response to a common-mode input signal, the difference between the drain (collector) voltages remains essentially zero except for a small change due to the mismatches inevitably present in the circuit.
2. It increases the differential gain by a factor of 2 (6 dB) because the output is the difference between two voltages of equal magnitude and opposite sign.

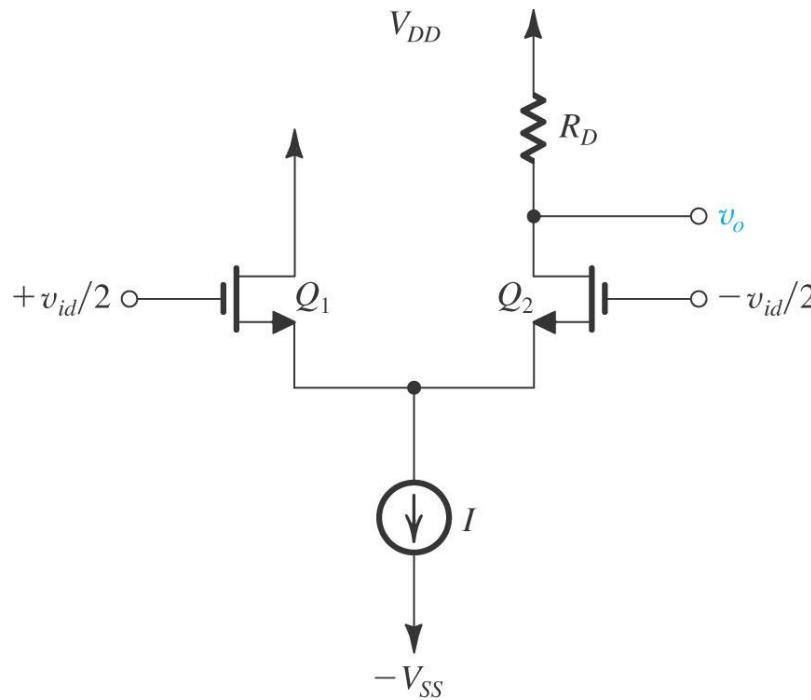
These advantages are sufficiently compelling that at least the first stage in an IC amplifier such as an op amp is differential-in, differential-out.



**Figure 9.30** A three-stage amplifier consisting of two differential-in, differential-out stages,  $A_1$  and  $A_2$ , and a differential-in, single-ended-out stage  $A_3$ .



# Differential to Single-Ended Conversion

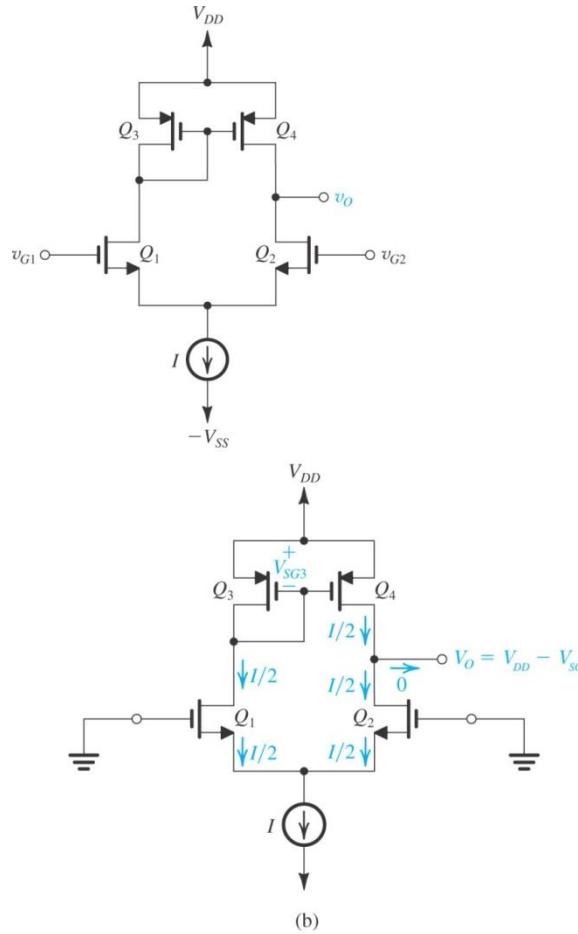


**Figure 9.31** A simple but inefficient approach for differential to single-ended conversion.

Figure 9.31 illustrates the simplest, most basic approach for differential-to-single-ended conversion. It consists of simply ignoring the drain current signal of  $Q_1$  and eliminating its drain resistor altogether, and taking the output between the drain of  $Q_2$  and ground. The obvious drawback of this scheme is that we lose a factor of 2 (or 6 dB) in gain as a result of “wasting” the drain signal current of  $Q_1$ .



# Active-Loaded MOS Differential Pair

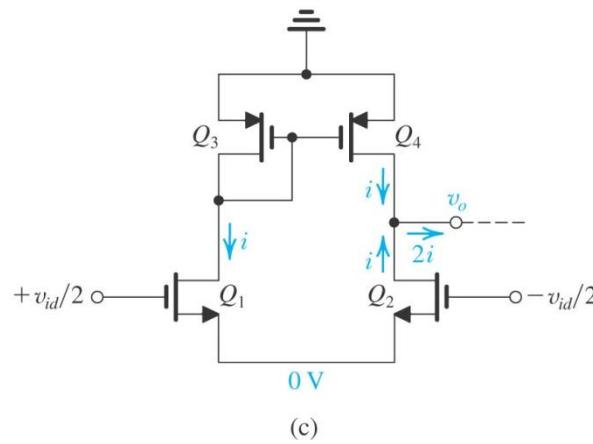


**Figure 9.32 (a)** The active-loaded MOS differential pair.  
**(b)** The circuit at equilibrium assuming perfect matching.

Figure 9.32(a) shows a MOS differential pair formed by transistors  $Q_1$  and  $Q_2$ , loaded by a current mirror formed by transistors  $Q_3$  and  $Q_4$ . First consider the quiescent or equilibrium state with the two input terminals connected to a dc voltage equal to the common-mode equilibrium value, in this case 0 V, as shown in Fig. 9.32(b). Assuming perfect matching, the bias current  $I$  divides equally between  $Q_1$  and  $Q_2$ . The drain current of  $Q_1$ ,  $I/2$ , is fed to the input transistor of the mirror,  $Q_3$ . Thus, a replica of this current is provided by the output transistor of the mirror,  $Q_4$ . Observe that at the output node the two currents balance each other out, leaving a zero current to flow out to the next stage or to a load (not shown). If  $Q_4$  is perfectly matched to  $Q_3$ , its drain voltage will track the voltage at the drain of  $Q_3$ ; thus in equilibrium the voltage at the output will be  $V_{DD} - V_{SG3}$ .



# Active-Loaded MOS Differential Pair

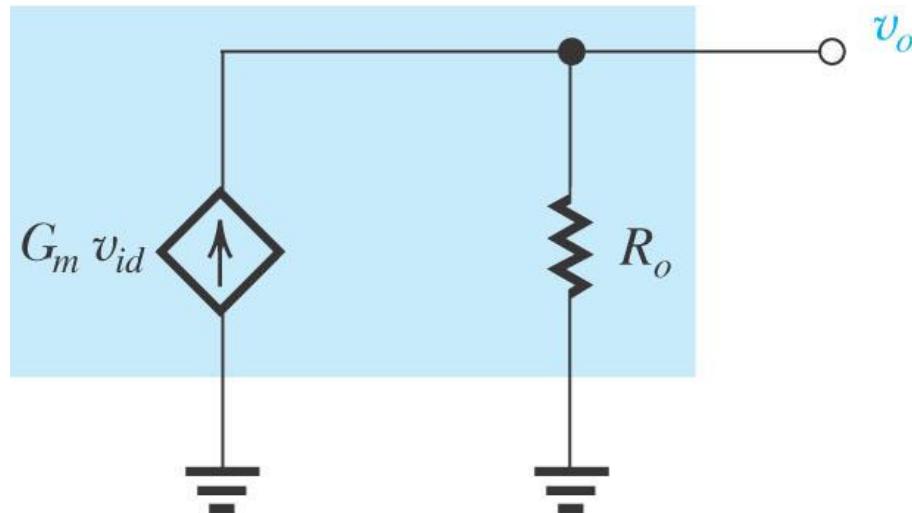


**Figure 9.32 (c)** The circuit with a differential input signal applied and neglecting the  $r_o$  of all transistors.

Next, consider the circuit with a differential input signal  $v_{id}$  applied to the input. Since we are now investigating the small-signal operation of the circuit, we have removed the dc supplies (including the current source  $I$ ). Also, for the time being let us ignore  $r_o$  of all transistors. As Fig. 9.32(c) shows, a virtual ground will develop at the common-source terminal of  $Q_1$  and  $Q_2$ . Transistor  $Q_1$  will conduct a drain signal current  $i = g_m v_{id}/2$ , and transistor  $Q_2$  will conduct an equal but opposite current  $i$ . The drain signal current  $i$  of  $Q_1$  is fed to the input of the  $Q_3 - Q_4$  mirror, which responds by providing a replica in the drain of  $Q_4$ . Now, at the output node we have two currents, each equal to  $i$ , which sum together to provide an output current  $2i$ .



# Differential Gain of the Active-Loaded MOS Pair



**Figure 9.33** Output equivalent circuit of the amplifier in Fig. 9.32(a) for differential input signals.

$$G_m = g_m$$

$$R_o \equiv \frac{v_x}{i_x} = r_{o2} \parallel r_{o4}$$

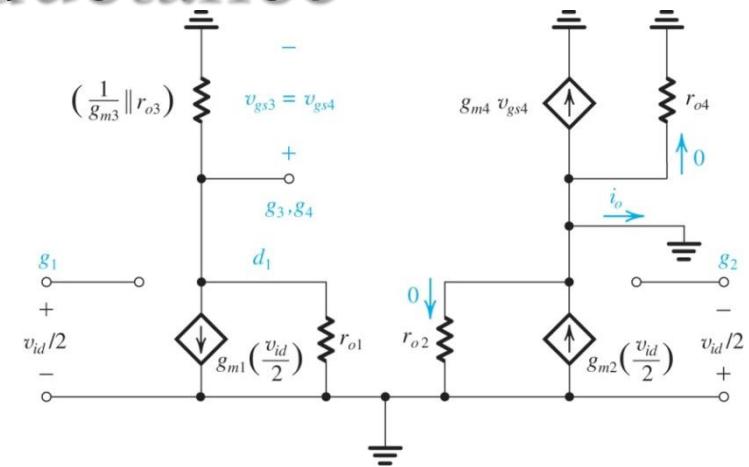
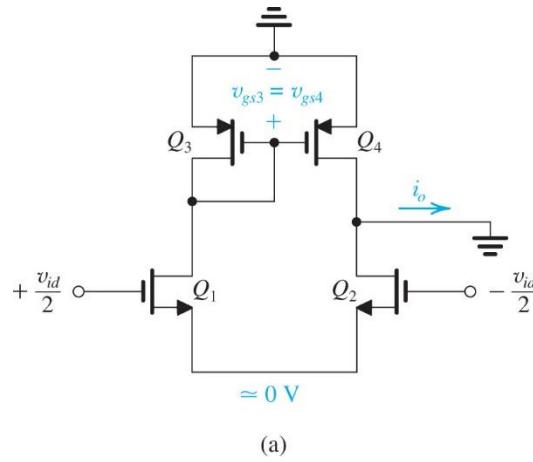
$$A_d \equiv \frac{v_{od}}{v_{id}} = G_m R_o = g_m (r_{o2} \parallel r_{o4})$$

$$\text{if } r_{o2} = r_{o4} = r_o$$

$$A_d = \frac{1}{2} g_m r_o = \frac{A_0}{2}$$



# Determining the short-circuit Transconductance



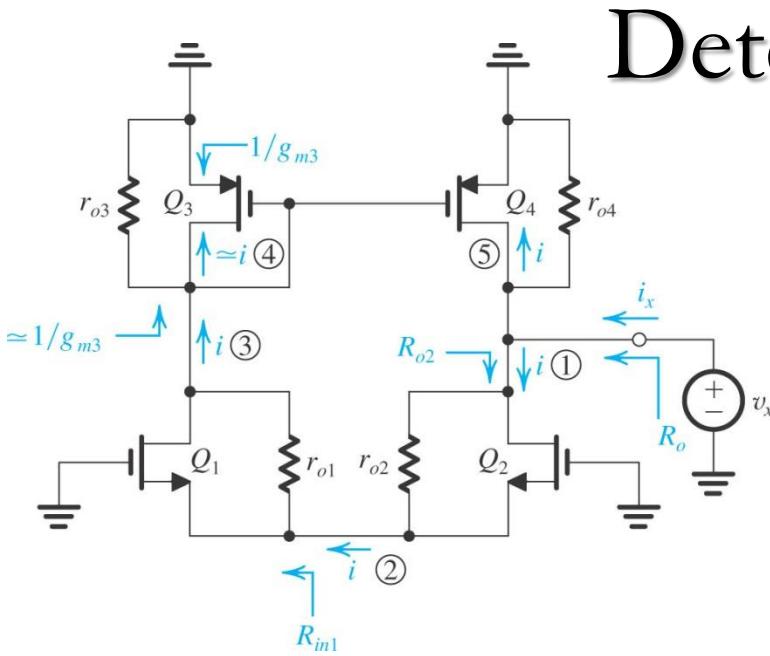
**Figure 9.34** Derivation of the short-circuit transconductance  $G_m \equiv i_o/v_{id}$ .

$$v_{g3} = -g_{m1} \left( \frac{v_{id}}{2} \right) \left( \frac{1}{g_{m3}} \parallel r_{o3} \parallel r_{o1} \right) \approx - \left( \frac{g_{m1}}{g_{m3}} \right) \left( \frac{v_{id}}{2} \right)$$

$$g_{m3} = g_{m4}; g_{m1} = g_{m2} = g_m$$

$$i_o = -g_{m1}v_{g3} + g_{m2} \left( \frac{v_{id}}{2} \right) = g_{m1} \left( \frac{g_{m4}}{g_{m3}} \right) \left( \frac{v_{id}}{2} \right) + g_{m2} \left( \frac{v_{id}}{2} \right)$$

$$i_o = g_m v_{id} \quad G_m = g_m$$



**Figure 9.35** Circuit for determining  $R_o$ . The circled numbers indicate the order of the analysis steps.

$$R_o \equiv \frac{v_x}{i_x}$$

# Determining $R_o$

$$i = \frac{v_x}{R_{o2}}$$

$$R_{o2} = R_{in1} + r_{o2} + g_{m2}r_{o2}R_{in1}$$

$$R_{in1} = \frac{r_{o1} + R_L}{g_{m1}r_{o1}} = \frac{1}{g_{m1}} + \frac{1/g_{m3}}{g_{m1}r_{o1}} \approx \frac{1}{g_{m1}}$$

$$R_{o2} = \frac{1}{g_{m1}} + r_{o2} + \left( \frac{g_{m2}}{g_{m1}} \right) r_{o2}$$

$$g_{m1} = g_{m2} = g_m; g_{m2}r_{o2} \gg 1$$

$$R_{o2} \approx 2r_{o2}$$

$$i_x = i + i + \frac{v_x}{r_{o4}} = 2i + \frac{v_x}{r_{o4}} = 2\frac{v_x}{r_{o4}} + \frac{v_x}{r_{o4}}$$

$$R_o \equiv \frac{v_x}{i_x} = r_{o2} \parallel r_{o4}$$



# Problem 9.91

Figure P9.91 shows the active-loaded MOS differential amplifier prepared for small-signal analysis. To help the reader we have already indicated approximate values for some of the node voltages. For instance, the output voltage  $v_o = 0.5(g_m r_o) v_{id}$ , which we have derived in the text. The voltage at the common sources has been found to be approximately  $+v_{id}/4$ , which is very far from the virtual ground one might assume. Also, the voltage at the gate of the mirror is approximately  $-v_{id}/4$  confirming our contention that the voltage there is vastly different from the output voltage, hence the lack of balance in the circuit and the unavailability of a differential half-circuit. Find the currents labeled  $i_1$  to  $i_{13}$ . Determine their values in the sequence of their numbering and reflect on the results. You will find that there is some inconsistency, which is a result of the approximations we have made. Note that all transistors are assumed to be operating at the same  $|V_{ov}|$ .

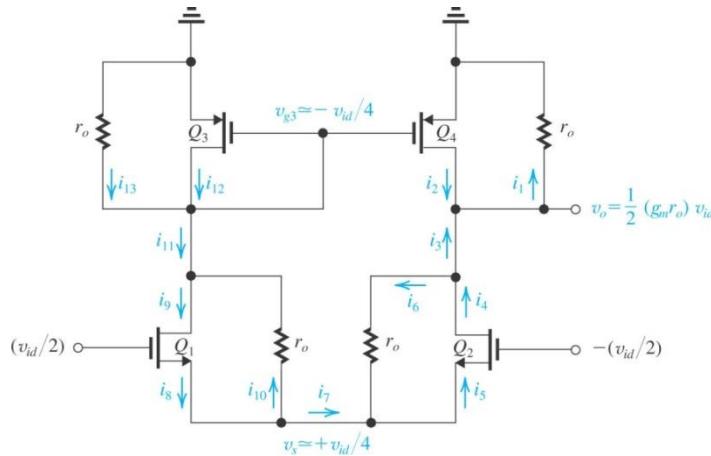


Figure P9.91



# Problem 9.91

$$i_{13} = i_{11} - i_{12} = 0$$

$$i_{12} = g_{m3}v_{sg3} = \frac{1}{4}g_m v_{id}$$

$$i_{11} = i_9 - i_{10} = \frac{1}{4}g_m v_{id}$$

$$i_{10} = i_8 - i_7 = 0$$

$$i_9 = i_8 = \frac{1}{4}g_m v_{id} \quad (v_{id}/2)$$

$$i_8 = g_{m1}v_{gs1} = g_m \left[ \frac{v_{id}}{2} - \frac{v_{id}}{4} \right] = \frac{1}{4}g_m v_{id}$$

$$i_7 = i_5 - i_6 = \frac{1}{4}g_m v_{id}$$

- The voltage at the common sources has been found to be

$$v_{g3} \simeq -\frac{v_{id}}{4},$$

$$v_s \simeq +\frac{v_{id}}{4}$$

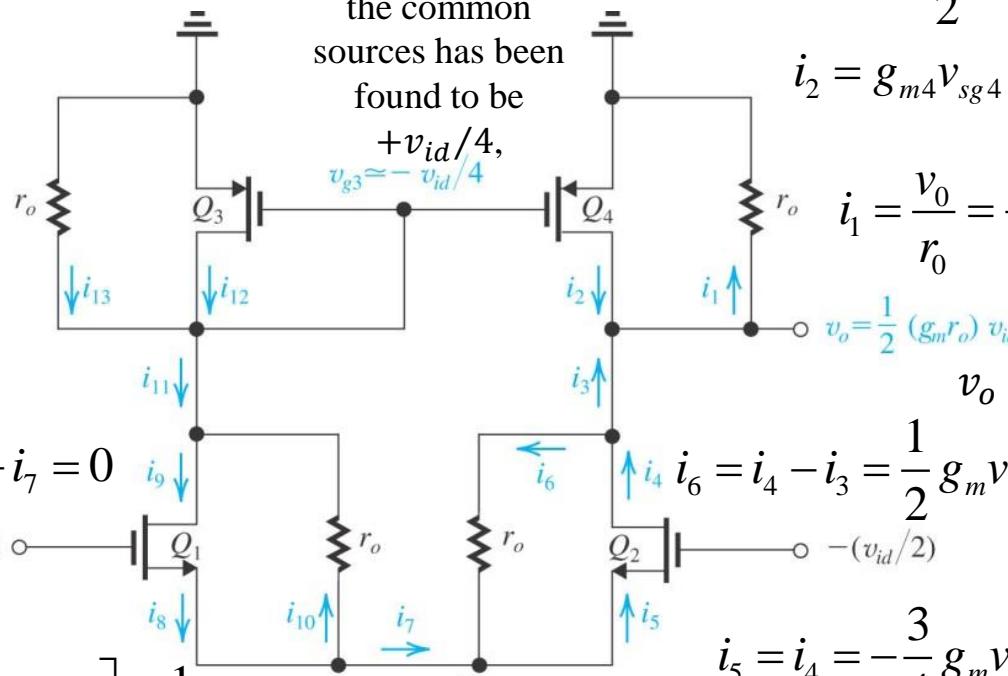


Figure P9.91

$$i_3 = i_1 - i_2 = \frac{g_m v_{id}}{2} - \frac{g_{m4} v_{id}}{4} = \frac{1}{4}g_m v_{id}$$

$$i_2 = g_{m4}v_{sg4} = \frac{1}{4}g_m v_{id}$$

$$i_1 = \frac{v_0}{r_0} = \frac{g_m r_o v_{id}}{2r_0} = \frac{1}{2}g_m v_{id}$$

$$v_o = \frac{1}{2}(g_m r_o) v_{id}$$

$$v_o = 0.5(g_m r_o) v_{id},$$

$$i_6 = i_4 - i_3 = \frac{1}{2}g_m v_{id}$$

$$i_5 = i_4 = -\frac{3}{4}g_m v_{id}$$

$$i_4 = -g_{m2}v_{gs2} = -g_{m2} \left[ -\frac{v_{id}}{2} - \frac{v_{id}}{4} \right] = -\frac{3}{4}g_m v_{id}$$

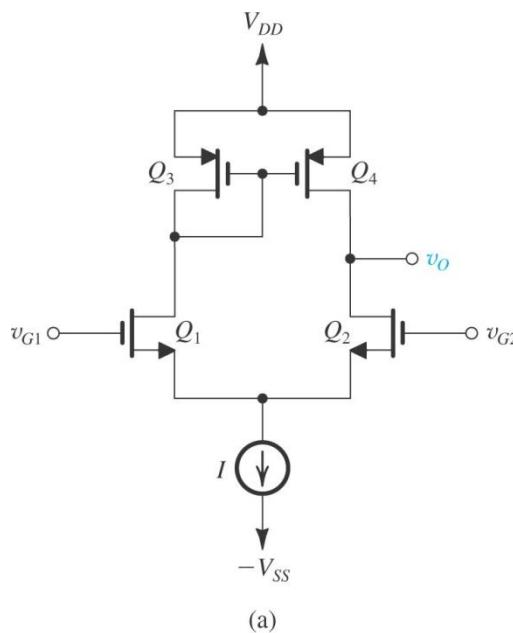
the voltage at the gate of the mirror is approximately  $-v_{id}/4$

Note that all transistors are assumed to be operating at the same  $|V_{OV}|$ .



## Problem 9.92

A current-mirror-loaded NMOS differential amplifier operates with a bias current  $I$  of  $200 \mu\text{A}$ . The NMOS transistors are operated at  $V_{OV} = 0.2 \text{ V}$  and the PMOS devices at  $|V_{OV}| = 0.3 \text{ V}$ . The Early voltages are  $20 \text{ V}$  for the NMOS and  $12 \text{ V}$  for the PMOS transistors. Find  $G_m$ ,  $R_o$ , and  $A_d$ . For what value of load resistance is the gain reduced by a factor of 2?



$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I}{2} = 100 \mu\text{A}$$

$$G_m = g_{m1} = g_{m2} = \frac{2I_D}{V_{OV}} = \frac{2 \cdot 100 \mu\text{A}}{0.2 \text{ V}} = 1.0 \text{ mA/V}$$

$$r_{o1} = r_{o2} = \frac{V_{AN}}{I_D} = \frac{20 \text{ V}}{1.0 \text{ mA}} = 200 \text{ k}\Omega \quad r_{o3} = r_{o4} = \frac{|V_{AP}|}{I_D} = \frac{12 \text{ V}}{1 \text{ mA}} = 120 \text{ k}\Omega$$

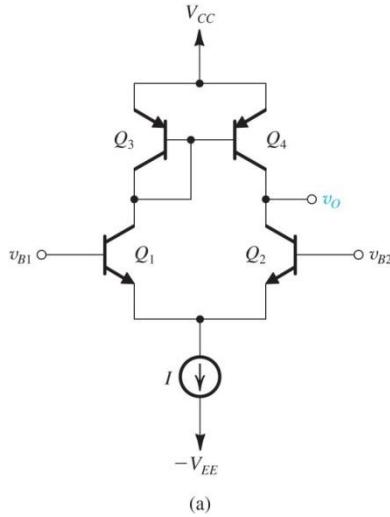
$$R_o = r_{o2} \parallel r_{o4} = 200 \text{ k}\Omega \parallel 120 \text{ k}\Omega = 75 \text{ k}\Omega$$

$$A_d = G_m R_o = 1 \text{ mA/V} \times 75 \text{ k}\Omega = 75 \text{ V/V}$$

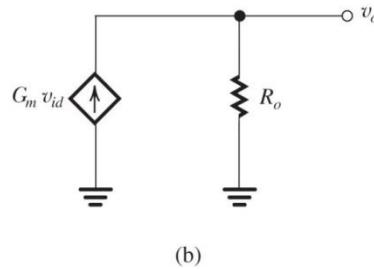
Gain is reduced in half if  $R_L = R_o = 75 \text{ k}\Omega$



# BJT Diff Pair with Active Load



(a)



(b)

**Figure 9.36** (a) Current-mirror-loaded bipolar differential pair. (b) Small-signal equivalent circuit of the amplifier output when a differential signal  $v_{id} \equiv v_{B1} - v_{B2}$  is applied.

$$G_m = g_m$$

$$R_o \equiv \frac{v_x}{i_x} = r_{o2} \parallel r_{o4}$$

$$A_d \equiv \frac{v_{od}}{v_{id}} = G_m R_o = g_m (r_{o2} \parallel r_{o4})$$

if  $r_{o2} = r_{o4} = r_o$

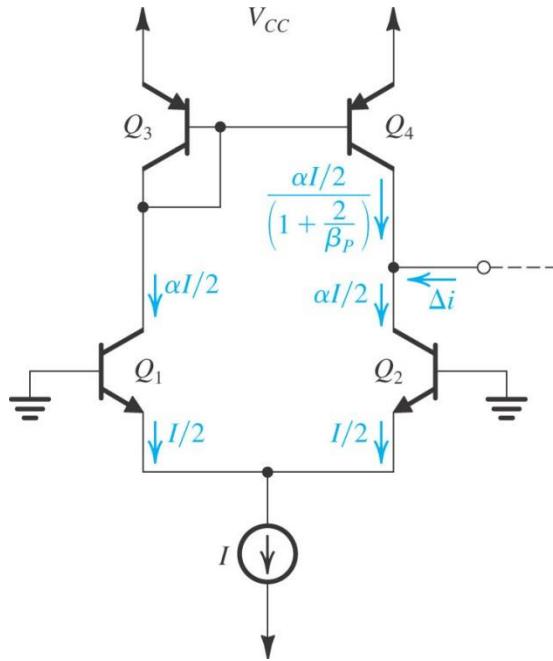
$$A_d = \frac{1}{2} g_m r_o = \frac{A_0}{2}$$

Derivation: Sedra and Smith pages 651 - 652

Although this expression is identical to that found for the MOS circuit, the gain here is much larger because  $g_m r_o$  for the BJT is more than an order of magnitude greater than of a MOSFET. The downside, however, lies in the low input resistance of BJT amplifiers. Indeed, the circuit of Fig. 9.36(a) indicates that, as expected, the differential input resistance of the differential amplifier is equal to  $2r_\pi$ .



# Active-Loaded BJT Diff Pair Input Offset Voltage



$$\frac{I_4}{I_3} = \frac{1}{1 + \frac{2}{\beta_P}}$$

$$I_4 = \frac{\alpha I / 2}{1 + \frac{2}{\beta_P}}$$

where  $\beta_P$  is the value of  $\beta$  of the *pnp* transistors  $Q_3$  and  $Q_4$ .

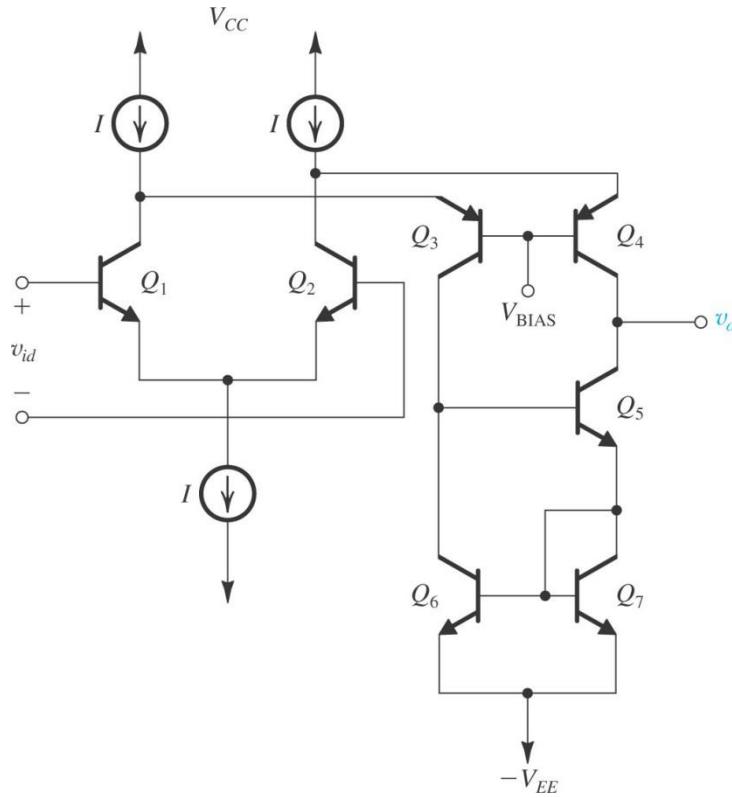
$$\Delta i = \frac{\alpha I}{2} - \frac{\alpha I / 2}{1 + \frac{2}{\beta_P}} \approx \frac{\alpha I}{\beta_P}$$

$$V_{OS} = -\frac{\Delta i}{G_m} = -\frac{\alpha I / \beta_P}{\alpha I / 2V_T} = -\frac{2V_T}{\beta_P}$$

**Figure 9.37** The current-mirror-loaded BJT differential pair suffers from a systematic input offset voltage resulting from the error in the current-transfer ratio of the current mirror.

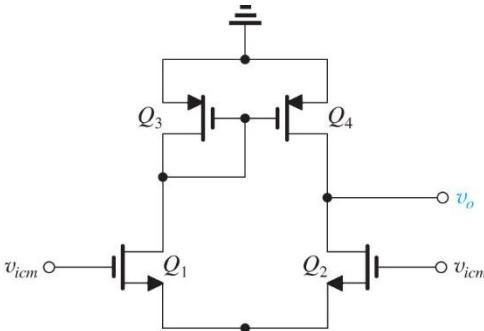


# Using Folded Cascode

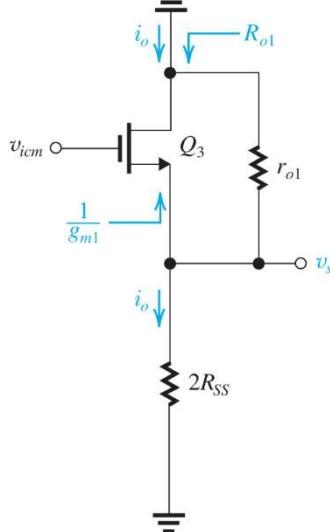


**Figure 9.38** An active-loaded bipolar differential amplifier employing a folded cascode stage ( $Q_3$  and  $Q_4$ ) and a Wilson current-mirror load ( $Q_5$ ,  $Q_6$ , and  $Q_7$ ).

To reduce  $V_{OS}$ , an improved current mirror such as the Wilson circuit studied in Section 8.6.2 should be used. Such a circuit provides the added advantage of increased output resistance and hence voltage gain. However, to realize the full advantage of the higher output resistance of the active load, the output resistance of the differential pair should be raised by utilizing a cascode stage. Figure 9.38 shows such an arrangement: A folded cascode stage formed by *pnp* transistors  $Q_3$  and  $Q_4$  is utilized to raise the output resistance looking into the collector of  $Q_4$  to  $\beta_4 r_{o4}$ . A Wilson mirror formed by transistors  $Q_5$ ,  $Q_6$ , and  $Q_7$  is used to implement the active load.

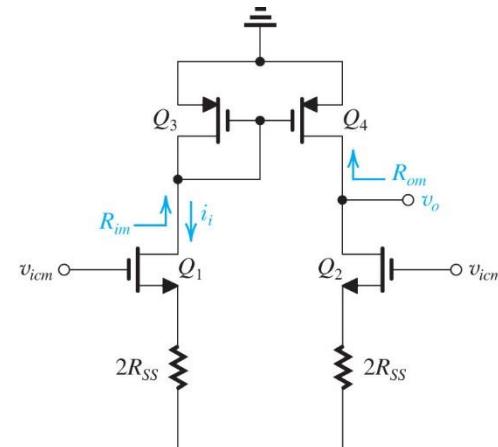


(a)

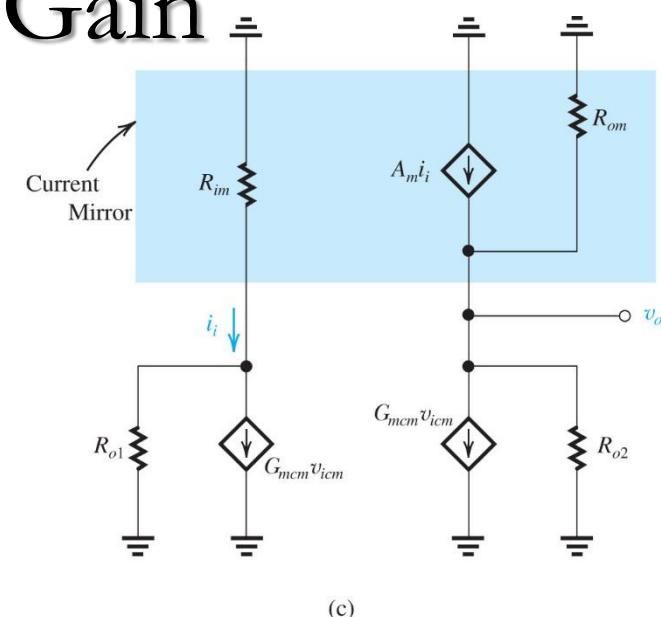


(d)

# Common-Mode Gain



(b)



(c)

**Figure 9.39** Analysis of the current-mirror-loaded MOS differential amplifier to determine its common-mode gain.

$$v_s = v_{icm} \frac{(2R_{SS} \parallel r_{o1})}{(2R_{SS} \parallel r_{o1}) + (1/g_{m1})} \approx v_{icm}$$

$$i_o = \frac{v_{icm}}{2R_{SS}}$$

$$G_{mcm} \equiv \frac{i_o}{v_{icm}} = \frac{1}{2R_{SS}}$$

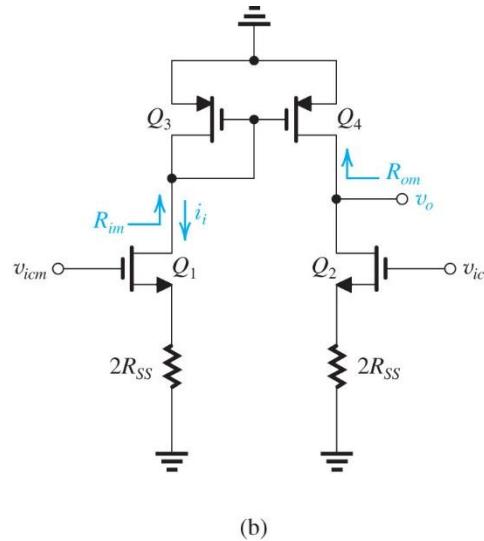


# Common-Mode Gain

$$G_{mcm} = \frac{1}{2R_{SS}}$$

$$R_{o1} = 2R_{SS} + r_{o1} + (g_{m1}r_{o1})(2R_{SS})$$

$$R_{o2} = 2R_{SS} + r_{o2} + (g_{m2}r_{o2})(2R_{SS})$$



**Figure 9.39** Analysis of the current-mirror-loaded MOS differential amplifier to determine its common-mode gain.

$$R_{o2} \gg r_{o4}; R_{o1} \gg r_{o3}; g_{m4} = g_{m3}$$

$$A_{CM} \equiv \frac{v_o}{v_{icm}} \simeq -\frac{r_{o4}}{2R_{SS}} \frac{1}{1 + g_{m3}r_{o3}}$$

$$g_{m3}r_{o3} \gg 1; r_{o3} = r_{o4}$$

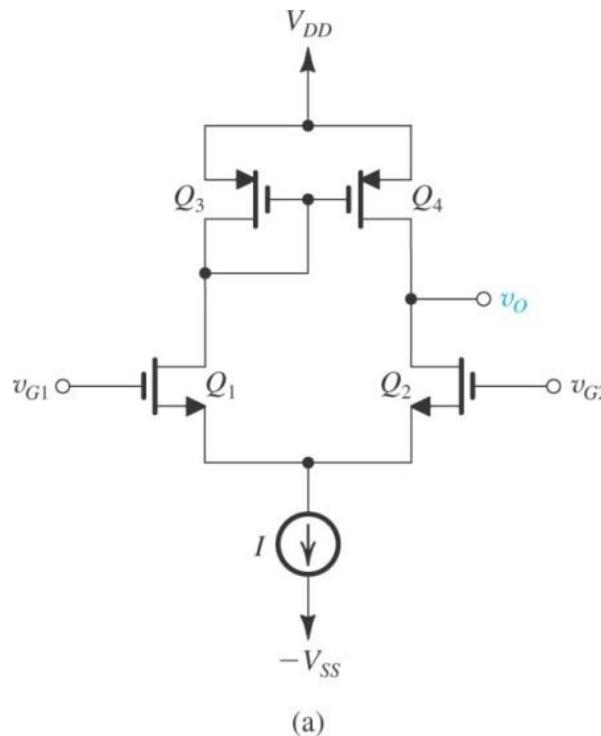
$$A_{CM} \simeq -\frac{1}{2g_{m3}R_{SS}}$$

$$v_{g3} = -G_{mcm}v_{icm} \left( R_{o1} \parallel r_{o3} \parallel \frac{1}{g_{m3}} \right)$$

$$i_4 = g_{m4}v_{gs3} = g_{m4}v_{g3} = -g_{m4}G_{mcm}v_{icm} \left( R_{o1} \parallel r_{o3} \parallel \frac{1}{g_{m3}} \right)$$

$$G_{mcm}v_{icm} + i_4 + \frac{v_o}{R_2} + \frac{v_o}{r_{o4}} = 0$$

$$v_o = -v_{icm} \frac{r_{o4} \parallel R_{o2}}{2R_{SS}} \left[ 1 - g_{m4} \left( R_{o1} \parallel r_{o3} \parallel \frac{1}{g_{m3}} \right) \right]$$



**Figure 9.32 (a)** The current-mirror-loaded MOS differential pair.

$$A_d = \frac{1}{2} g_m r_o = \frac{A_0}{2}$$

# CMMR

$$A_d \equiv \frac{v_{od}}{v_{id}} = G_m R_o = g_m (r_{o2} \parallel r_{o4})$$

$$A_{CM} \equiv \frac{v_o}{v_{icm}} \simeq -\frac{1}{2g_{m3}R_{SS}}$$

$$CMRR \equiv \frac{|A_d|}{|A_{cm}|} = \frac{\left[ g_m (r_{o2} \parallel r_{o4}) \right]}{\left[ 1/(2g_{m3}R_{SS}) \right]} = \left[ g_m (r_{o2} \parallel r_{o4}) \right] [2g_{m3}R_{SS}]$$

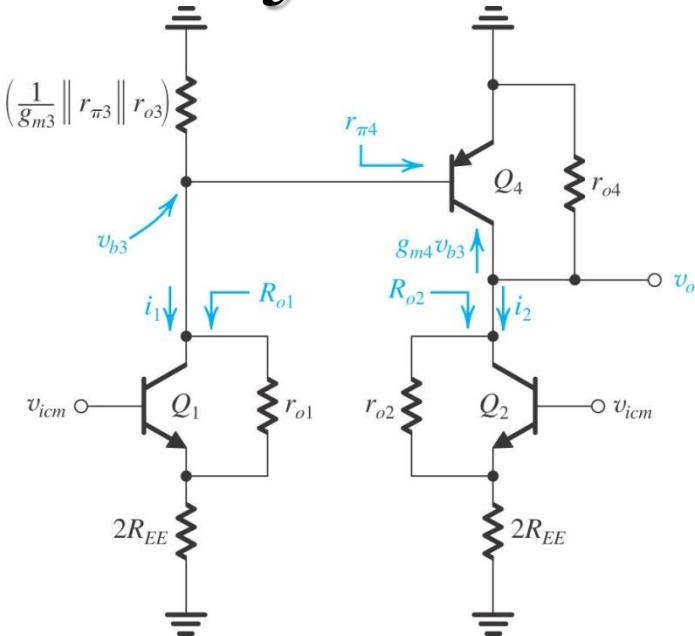
if  $r_{o2} = r_{o4} = r_o; g_{m3} = g_m$

$$CMRR = (g_m r_o) (g_m R_{SS})$$

We observe that to obtain a large CMRR, we select an implementation of the biasing current source  $I$  that features a high output resistance.



# BJT Common Mode Gain, CMRR



Derivation: Sedra and Smith pages 655 - 658

$$A_{CM} \equiv \frac{v_o}{v_{icm}} = \frac{r_{o4}}{2R_{EE}} \left[ g_{m4} \left( \frac{1}{g_{m3}} \| r_{\pi3} \| r_{o3} \| r_{\pi4} \right) - 1 \right]$$

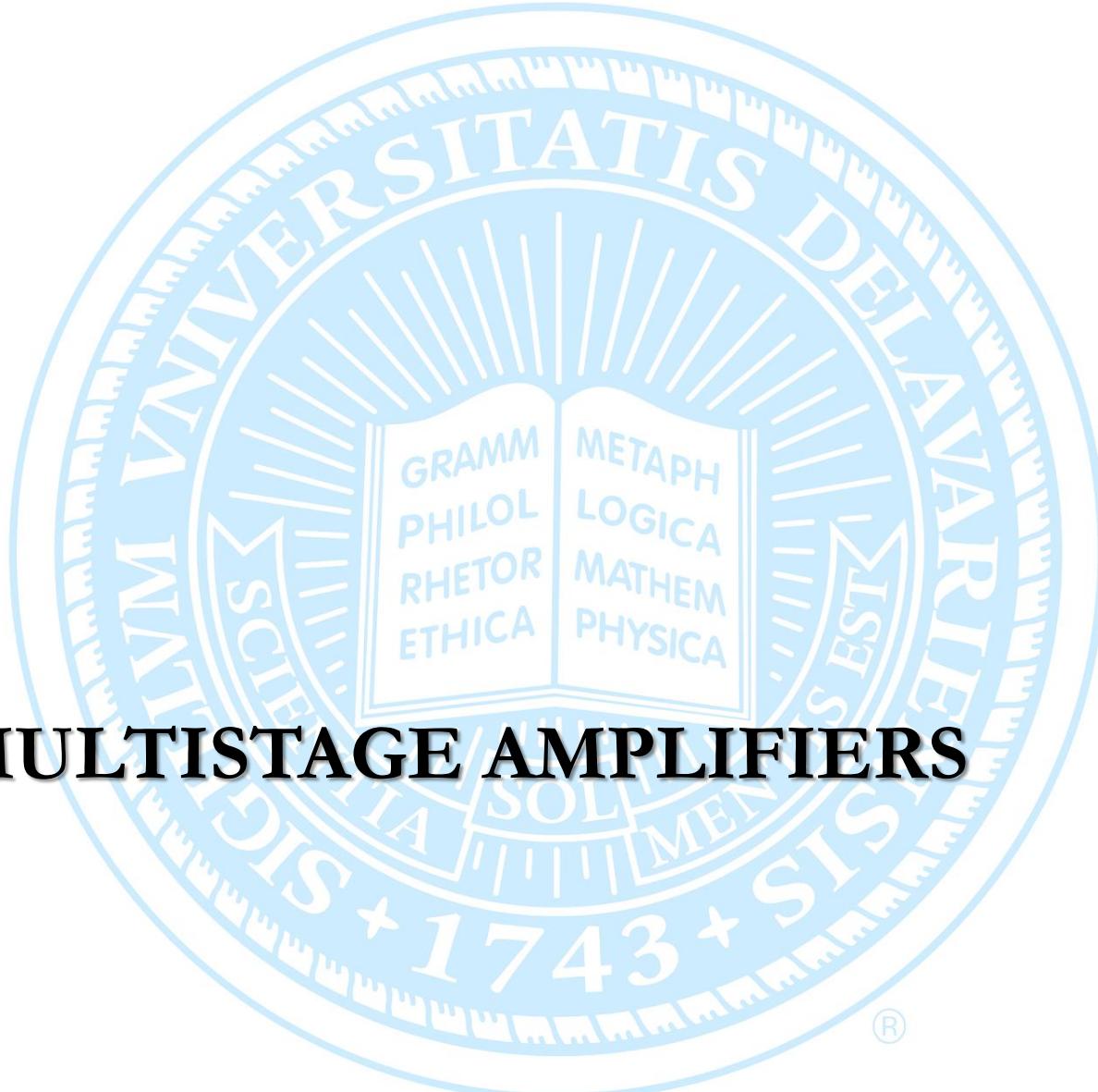
$$g_{m3} = g_{m4}; r_{\pi4} = r_{\pi3}; r_{o3} \gg r_{\pi3}, r_{\pi4}$$

$$A_{CM} \simeq -\frac{r_{o4}}{\beta_3 R_{EE}}$$

$$CMRR \equiv \frac{|A_d|}{|A_{cm}|} = g_m (r_{o2} \| r_{o4}) \left( \frac{\beta_3 R_{EE}}{r_{o4}} \right)$$

$$\text{if } r_{o2} = r_{o4} = r_o$$

$$CMRR = \frac{1}{2} \beta_3 g_m R_{EE}$$



## 9.6 MULTISTAGE AMPLIFIERS



# Two-stage CMOS Op Amp

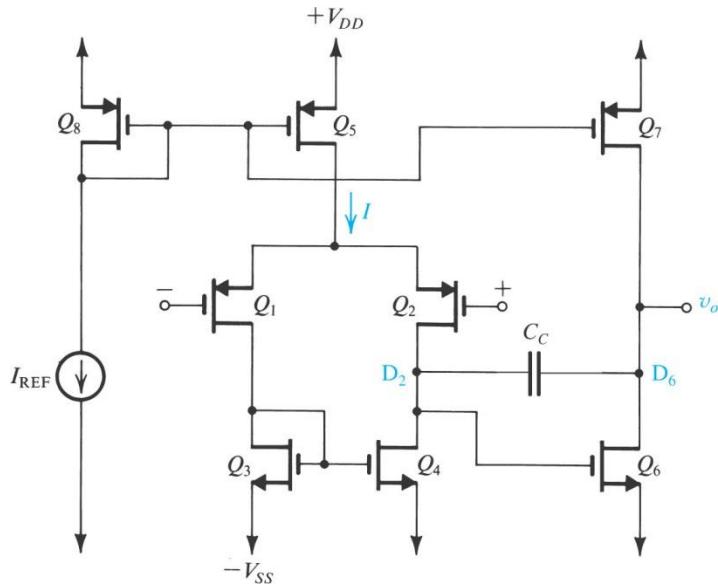


Figure 9.40 Two-stage CMOS op-amp configuration.

- The second stage consists of  $Q_6$ , which is a common-source amplifier loaded with the current-source transistor  $Q_7$ . A capacitor  $C_C$  is included in the negative-feedback path of the second stage.

two-stage CMOS op amps configuration.

- The circuit utilizes two power supplies, which can range from  $\pm 2.5$  V for the 0.5- $\mu\text{m}$  technology down to  $\pm 0.9$  V for the 0.18- $\mu\text{m}$  technology.
- A reference bias current  $I_{REF}$  is generated either externally or using on-chip circuits.
- The current mirror formed by  $Q_8$  and  $Q_5$  supplies the differential pair  $Q_1 - Q_2$  with bias current. The W/L ratio of  $Q_5$  is selected to yield the desired value for the input-stage bias current  $I$  (or  $I/2$  for each of  $Q_1$  and  $Q_2$ ).
- The input differential pair is actively loaded with the current mirror formed by  $Q_3$  and  $Q_4$ .



# Two-stage CMOS Op Amp

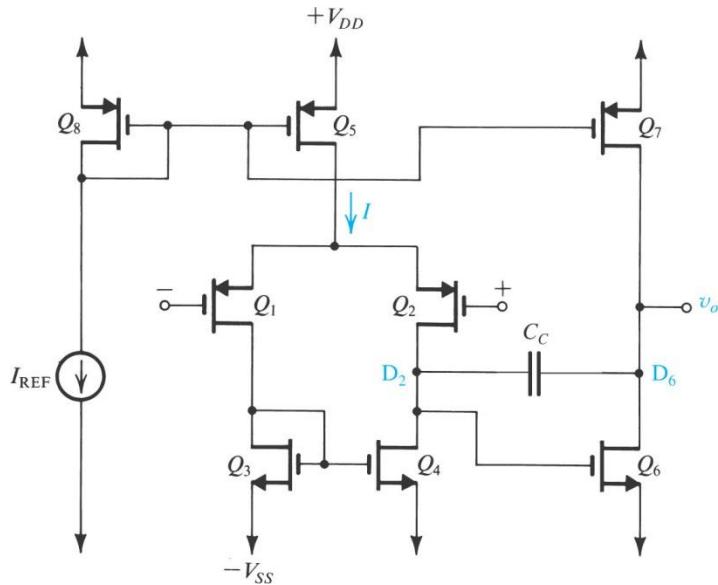


Figure 9.40 Two-stage CMOS op-amp configuration.

Voltage Gain

$$A_1 = -g_{m1} (r_{o2} \parallel r_{o4})$$

$$A_2 = -g_{m6} (r_{o6} \parallel r_{o7})$$

$$A_v = A_1 A_2 = g_{m1} (r_{o2} \parallel r_{o4}) g_{m6} (r_{o6} \parallel r_{o7})$$

Input Offset Voltage

$$I_6 = \frac{(W/L)_6}{(W/L)_4} \left( \frac{I}{2} \right) \quad I_7 = \frac{(W/L)_7}{(W/L)_5} I$$

Condition to have  $I_6 = I_7$ :

$$\frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_7}{(W/L)_5}$$



# Four Stage Bipolar Op Amp

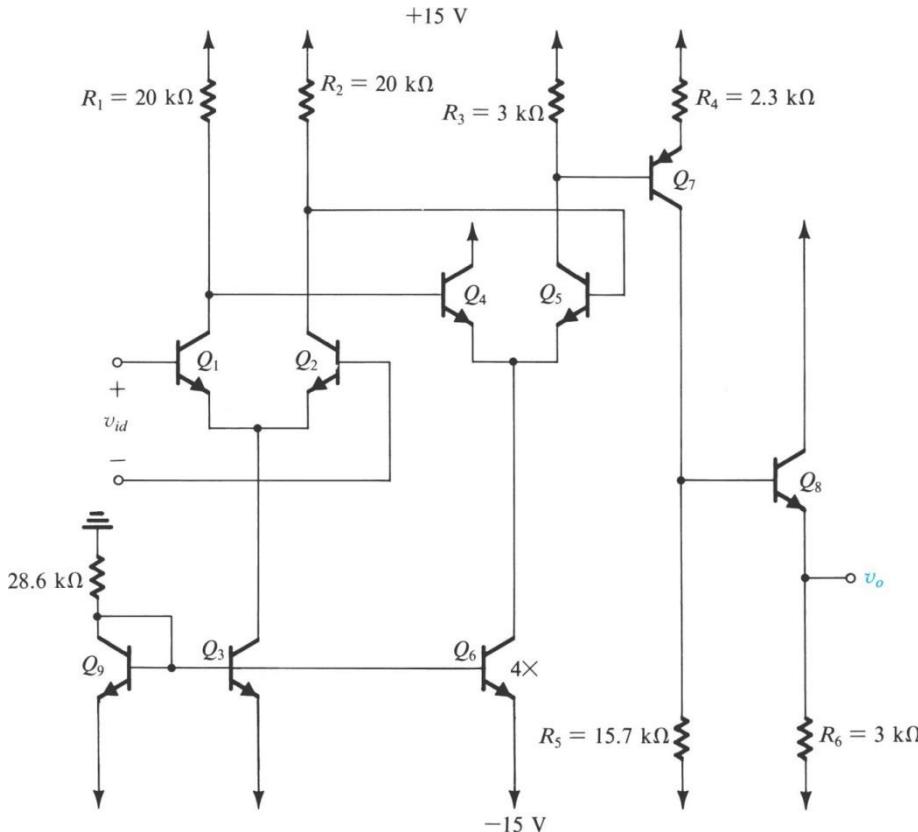


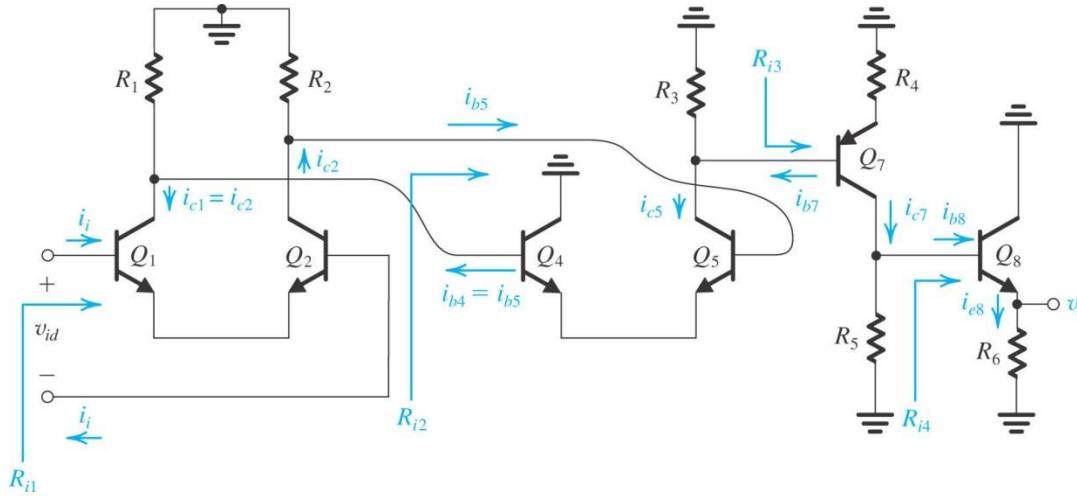
Figure 9.41 A four-stage bipolar op amp.

four-stage bipolar op amp configuration.

- 1<sup>st</sup> stage – differential-in, differential-out.
- 2<sup>nd</sup> stage – differential-in, single-ended out.
- 3<sup>rd</sup> stage - single-ended in, single-ended out, level shifting.
- 4<sup>th</sup> stage – single-ended in, single ended out, emitter follower.
- The circuit utilizes two power supplies at  $\pm 15$  V.
- A reference bias current  $I_{REF}$  is generated by the resistor attached to  $Q_9$ .



# Analysis Using Current Gains



**Figure 9.47** The circuit of the multistage amplifier of Fig. 9.41 prepared for small-signal analysis. Indicated are the signal currents throughout the amplifier and the input resistances of the four stages.

$$v_o = R_6 i_{e8}$$

$$v_{id} = R_{i1} i_i$$

$$A_d = \frac{v_o}{v_{id}} = \frac{R_6}{R_{i1}} \frac{i_{e8}}{i_i} \quad \frac{i_{e8}}{i_i} = \frac{i_{e8}}{i_{b8}} \times \frac{i_{b8}}{i_{c7}} \times \frac{i_{c7}}{i_{b7}} \times \frac{i_{b7}}{i_{c5}} \times \frac{i_{c5}}{i_{b5}} \times \frac{i_{b5}}{i_{c2}} \times \frac{i_{c2}}{i_i}$$

$$\frac{i_{e8}}{i_{b8}} = \beta_8 + 1$$

$$\frac{i_{b8}}{i_{c7}} = \frac{R_5}{R_5 + R_{i4}}$$

$$\frac{i_{c7}}{i_{b7}} = \beta_7$$

$$\frac{i_{b7}}{i_{c5}} = \frac{R_3}{R_3 + R_{i3}}$$

$$\frac{i_{c5}}{i_{b5}} = \beta_5$$

$$\frac{i_{b5}}{i_{c2}} = \frac{(R_1 + R_2)}{(R_1 + R_2) + R_{i2}}$$

$$\frac{i_{c2}}{i_i} = \beta_2$$



# Summary

- The differential-pair or differential-amplifier configuration is most widely used building block in analog IC designs. The input stage of every op-amp is a differential amplifier.
- There are two reasons for preferring differential to single-ended amplifiers:
  1. differential amplifiers are insensitive to interference and
  2. they do not need bypass and coupling capacitors.
- For a MOS (bipolar) pair biased by a current source  $I$ , each device operates at a drain (collector, assuming  $\alpha = 1$ ) current of  $I/2$  and a corresponding overdrive voltage  $V_{OV}$  (no analog in bipolar). Each device has  $g_m=1/V_{OV}$  ( $\alpha I/2V_T$  for bipolar).
- With the two input terminals connected to a suitable dc voltage  $V_{CM}$ , the bias current  $I$  of a perfectly symmetrical differential pair divides equally between the two transistors of the pair, resulting in zero voltage difference between the two drains (collectors). To steer the current completely to one side of the pair, a difference input voltage  $v_{id}$  of at least  $2^{1/2}V_{OV}$  is needed.



# Summary

- Superimposing a differential input signal  $v_{id}$  on the dc common-mode input voltage  $V_{CM}$  such that  $v_{I1} = V_{CM} + v_{id}/2$  and  $v_{I2} = V_{CM} - v_{id}/2$  causes a virtual signal ground to appear on the common-source (common-emitter) connection.
- The analysis of a differential amplifier to determine differential gain, differential input resistance, frequency response of differential gain, and so on is facilitated by employing the differential half-circuit which is a common-source (common-emitter) transistor biased at  $I/2$ .
- An input common-mode signal  $v_{icm}$  gives rise to drain (collector) voltage signals that are ideally equal and given by  $-v_{icm}(R_D/2R_{SS})$  [ $-v_{icm}(R_C/2R_{EE})$  for the bipolar pair], where  $R_{SS}$  ( $R_{EE}$ ) is the output resistance of the current source that supplies the bias current  $I$ .



# Summary

- While the input differential resistance  $R_{id}$  of the MOS pair is infinite, that for the bipolar pair is only  $2r_\pi$  but can be increased to  $2(\beta+1)(r_e+R_e)$  by including resistances  $R_e$  in the two emitters. The latter action, however, lowers  $A_d$ .
- Mismatches between the two sides of a differential pair result in a differential dc output voltage ( $V_o$ ) even when the two input terminals are tied together and connected to a dc voltage  $V_{CM}$ . This signifies the presence of an input offset voltage  $V_{OS} = V_o/A_d$ . In a MOS pair, there are three main sources for  $V_{OS}$ . Two exist for the bipolar pair.