UNIVERSITY *of* DELAWARE

Chapter 3
Semiconductors

SPRING SEMESTER 2017

IN THIS CHAPTER YOU WILL LEARN

1. The basic properties of semiconductors and in particular silicon, which is the material used to make most of today's electronic circuits.

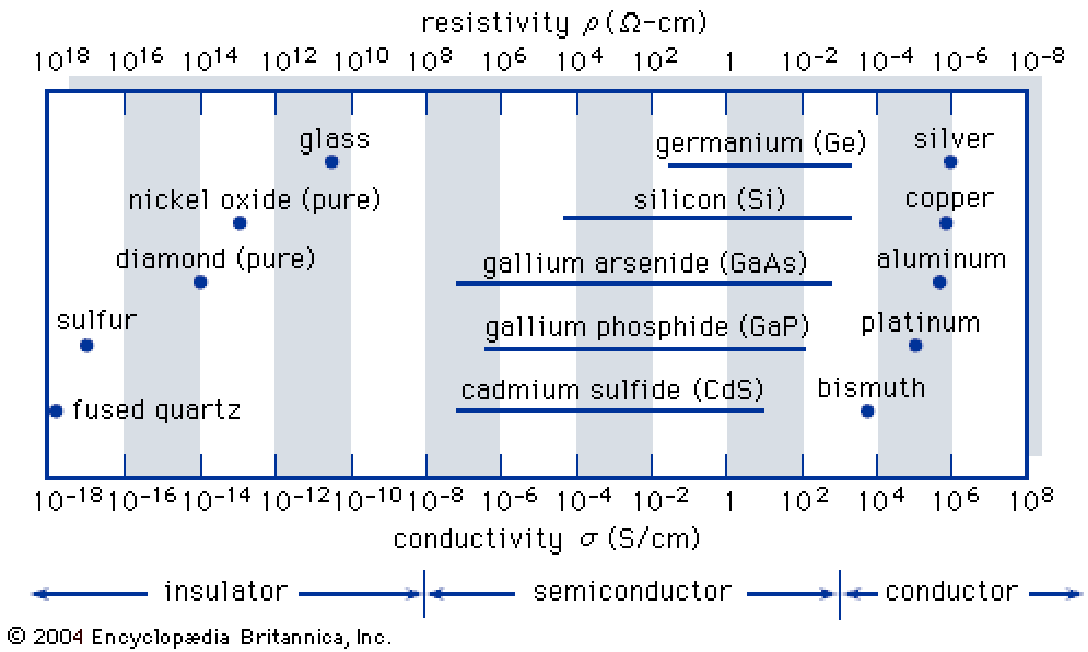
2. How doping a pure silicon crystal dramatically changes its electrical conductivity, which is the fundamental idea underlying the use of semiconductors In the implementation of electronic devices.

3. The two mechanisms by which current flows in semiconductors: drift and diffusion of charge carriers.

4. The structure and operation of the *pn* junction; a basic semiconductor structure that implements the diode and plays a dominant role in transistors.

3.1 INTRINSIC SEMICONDUCTORS

Introduction



Semiconductors are materials whose electrical properties lie between Conductors and Insulators.

Ex : Silicon and Germanium

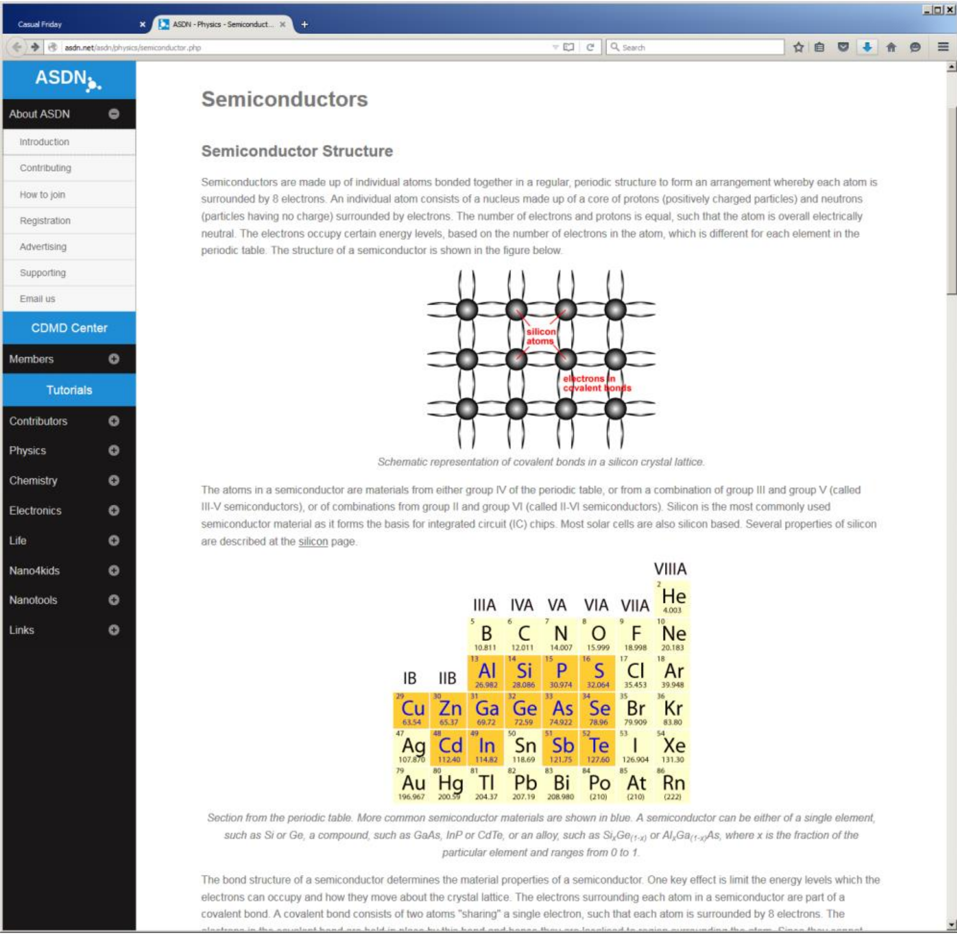
Semiconductor Elements

IB	IIB	IIIA	IVA	VA	VIA	VIIA	VIIIA
							2 He 4.003
		5 B 10.811	6 C 12.011	7 N 14.007	8 O 15.999	9 F 18.998	10 Ne 20.183
		13 Al 26.982	14 Si 28.086	15 P 30.974	16 S 32.064	17 Cl 35.453	18 Ar 39.948
29 Cu 63.54	30 Zn 65.37	31 Ga 69.72	32 Ge 72.59	33 As 74.922	34 Se 78.96	35 Br 79.909	36 Kr 83.80
47 Ag 107.870	48 Cd 112.40	49 In 114.82	50 Sn 118.69	51 Sb 121.75	52 Te 127.60	53 I 126.904	54 Xe 131.30
79 Au 196.967	80 Hg 200.59	81 Tl 204.37	82 Pb 207.19	83 Bi 208.980	84 Po (210)	85 At (210)	86 Rn (222)

- Section from the periodic table.
- More common semiconductor materials are shown in blue.
- A semiconductor can be either of a single element, such as Si or Ge, a compound, such as GaAs, InP or CdTe, or an alloy, such as $Si_xGe_{(1-x)}$ or $Al_xGa_{(1-x)}As$, where x is the fraction of the particular element and ranges from 0 to 1.

http://asdn.net/asdn/physics/semiconductor.shtml

http://asdn.net/asdn/physics/semiconductor.php



Semiconductors

Semiconductor Structure

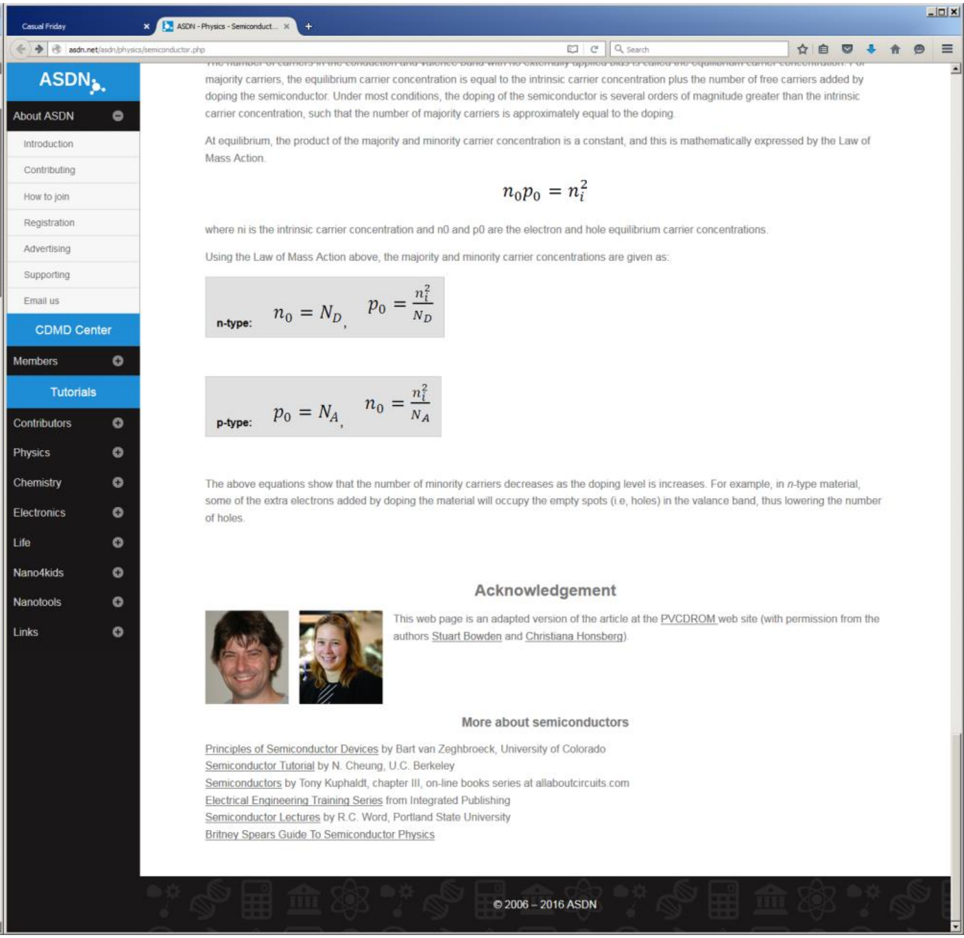
Semiconductors are made up of individual atoms bonded together in a regular, periodic structure to form an arrangement whereby each atom is surrounded by 8 electrons. An individual atom consists of a nucleus made up of a core of protons (positively charged particles) and neutrons (particles having no charge) surrounded by electrons. The number of electrons and protons is equal, such that the atom is overall electrically neutral. The electrons occupy certain energy levels, based on the number of electrons in the atom, which is different for each element in the periodic table. The structure of a semiconductor is shown in the figure below.

Schematic representation of covalent bonds in a silicon crystal lattice.

The atoms in a semiconductor are materials from either group IV of the periodic table, or from a combination of group III and group V (called III-V semiconductors), or of combinations from group II and group VI (called II-VI semiconductors). Silicon is the most commonly used semiconductor material as it forms the basis for integrated circuit (IC) chips. Most solar cells are also silicon based. Several properties of silicon are described at the silicon page.

Section from the periodic table. More common semiconductor materials are shown in blue. A semiconductor can be either of a single element, such as Si or Ge, a compound, such as GaAs, InP or CdTe, or an alloy, such as $Si_xGe_{(1-x)}$ or $Al_xGa_{(1-x)}As$, where x is the fraction of the particular element and ranges from 0 to 1.

The bond structure of a semiconductor determines the material properties of a semiconductor. One key effect is limit the energy levels which the electrons can occupy and how they move about the crystal lattice. The electrons surrounding each atom in a semiconductor are part of a covalent bond. A covalent bond consists of two atoms "sharing" a single electron, such that each atom is surrounded by 8 electrons. The



majority carriers, the equilibrium carrier concentration is equal to the intrinsic carrier concentration plus the number of free carriers added by doping the semiconductor. Under most conditions, the doping of the semiconductor is several orders of magnitude greater than the intrinsic carrier concentration, such that the number of majority carriers is approximately equal to the doping.

At equilibrium, the product of the majority and minority carrier concentration is a constant, and this is mathematically expressed by the Law of Mass Action.

$$n_0 p_0 = n_i^2$$

where ni is the intrinsic carrier concentration and n0 and p0 are the electron and hole equilibrium carrier concentrations.

Using the Law of Mass Action above, the majority and minority carrier concentrations are given as:

n-type: $n_0 = N_D, \quad p_0 = \frac{n_i^2}{N_D}$

p-type: $p_0 = N_A, \quad n_0 = \frac{n_i^2}{N_A}$

The above equations show that the number of minority carriers decreases as the doping level is increases. For example, in *n*-type material, some of the extra electrons added by doping the material will occupy the empty spots (i.e, holes) in the valance band, thus lowering the number of holes.

Acknowledgement

This web page is an adapted version of the article at the PVCDROM web site (with permission from the authors Stuart Bowden and Christiana Honsberg).

More about semiconductors

Principles of Semiconductor Devices by Bart van Zeghbroeck, University of Colorado
Semiconductor Tutorial by N. Cheung, U.C. Berkeley
Semiconductors by Tony Kuphaldt, chapter III, on-line books series at allaboutcircuits.com
Electrical Engineering Training Series from Integrated Publishing
Semiconductor Lectures by R.C. Word, Portland State University
Britney Spears Guide To Semiconductor Physics

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Intrinsic Semiconductors (Silicon)

silicon atom

- four valence electrons
- requires four more to complete outermost shell
- each pair of shared forms a covalent bond
- the atoms form a lattice structure

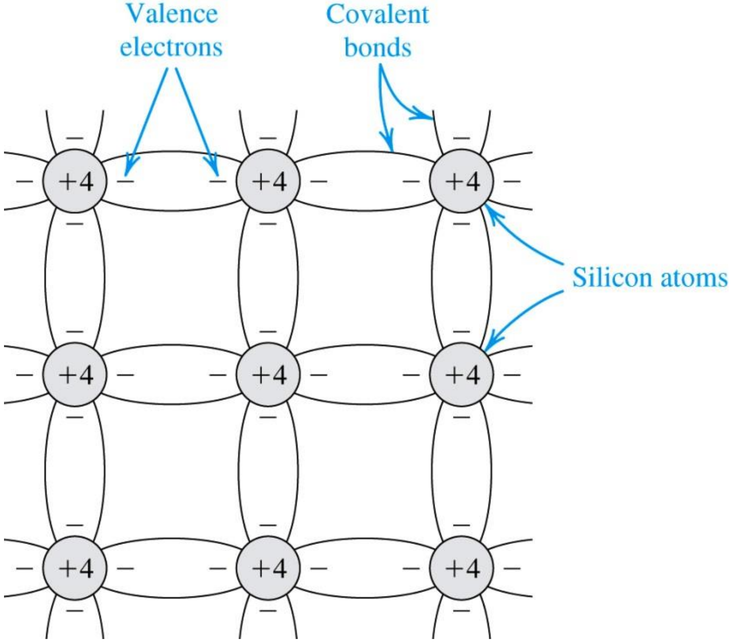

Figure 3.1 Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of +4*q*, which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons. At 0 K, all bonds are intact and no free electrons are available for current conduction.

Silicon Crystal Structure

0 Kelvin

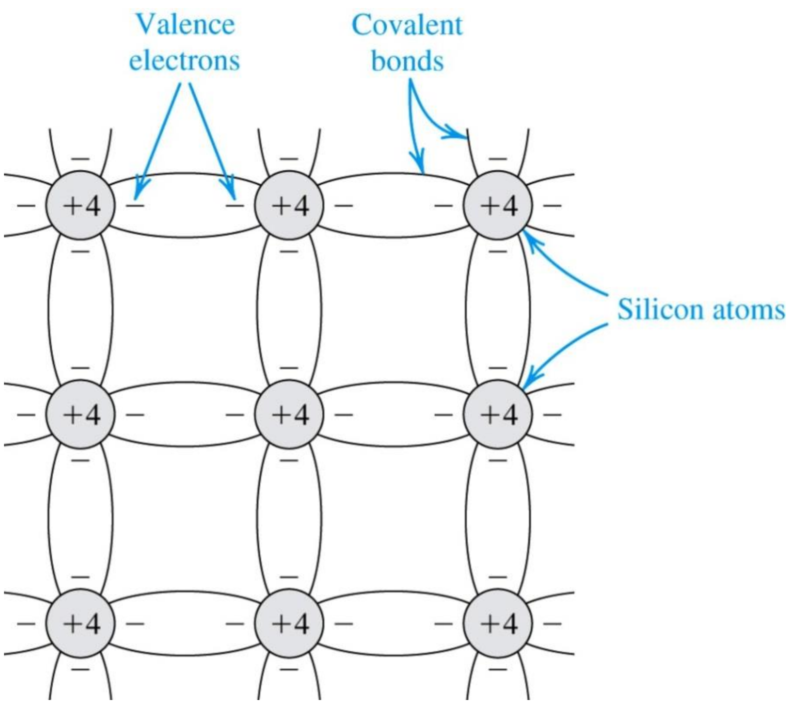

Figure 3.1 Two-dimensional representation of the silicon crystal. The circles represent the inner core of silicon atoms, with +4 indicating its positive charge of $+4q$, which is neutralized by the charge of the four valence electrons. Observe how the covalent bonds are formed by sharing of the valence electrons. At 0 K, all bonds are intact and no free electrons are available for current conduction.

300 Kelvin/RT

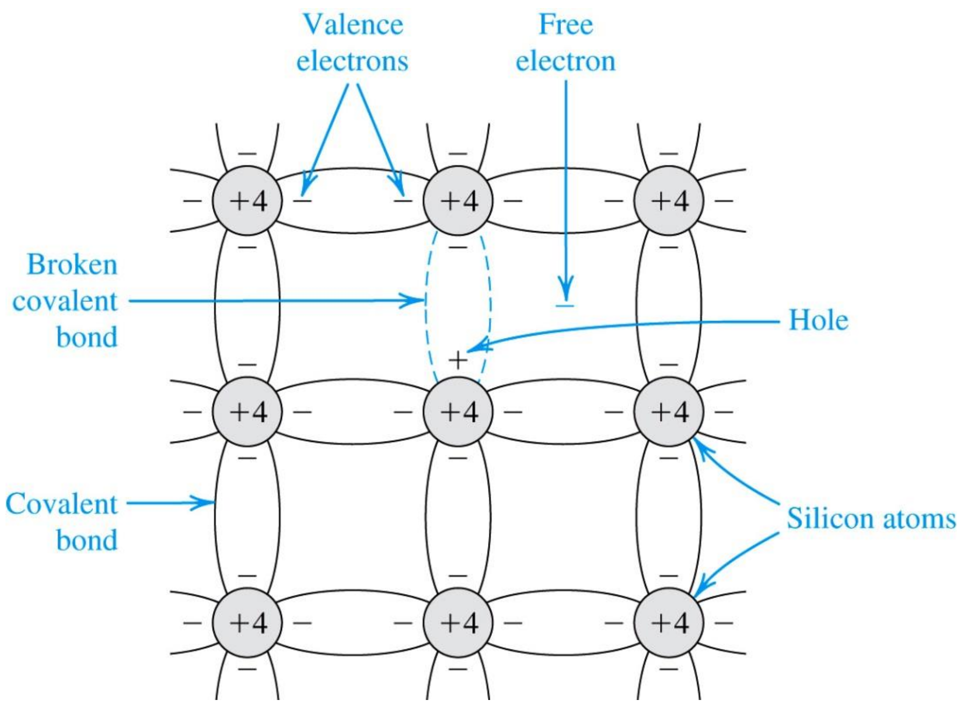

Figure 3.2 At room temperature, some of the covalent bonds are broken by thermal generation. Each broken bond gives rise to a free electron and a hole, both of which become available for current conduction.

Intrinsic Semiconductors

Sedra and Smith
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Thermal generation results in free electrons and holes in equal numbers and hence equal concentrations, where concentration refers to the number of charge carriers per unit volume (cm^3). The free electrons and holes move randomly through the silicon crystal structure, and in the process some electrons may fill some of the holes. This process, called **recombination**, results in the disappearance of free electrons and holes. The recombination rate is proportional to the number of free carriers, which is determined by the **thermal generation rate**.

At thermal equilibrium:

$$n = p = n_i$$

Semiconductor Physics

From Semiconductor Physics:

$$n = p = n_i = BT^{3/2} e^{-E_g/2kT}$$

Where: B is a material dependent parameter

$B = 7.3 \times 10^{15} \text{cm}^{-3}\text{K}^{-3/2}$ for silicon

T is the temperature in Kelvin

E_g is the bandgap energy

$E_g = 1.12$ eV for silicon

k is Boltzmann's constant = 8.62×10^{-5} eV/K

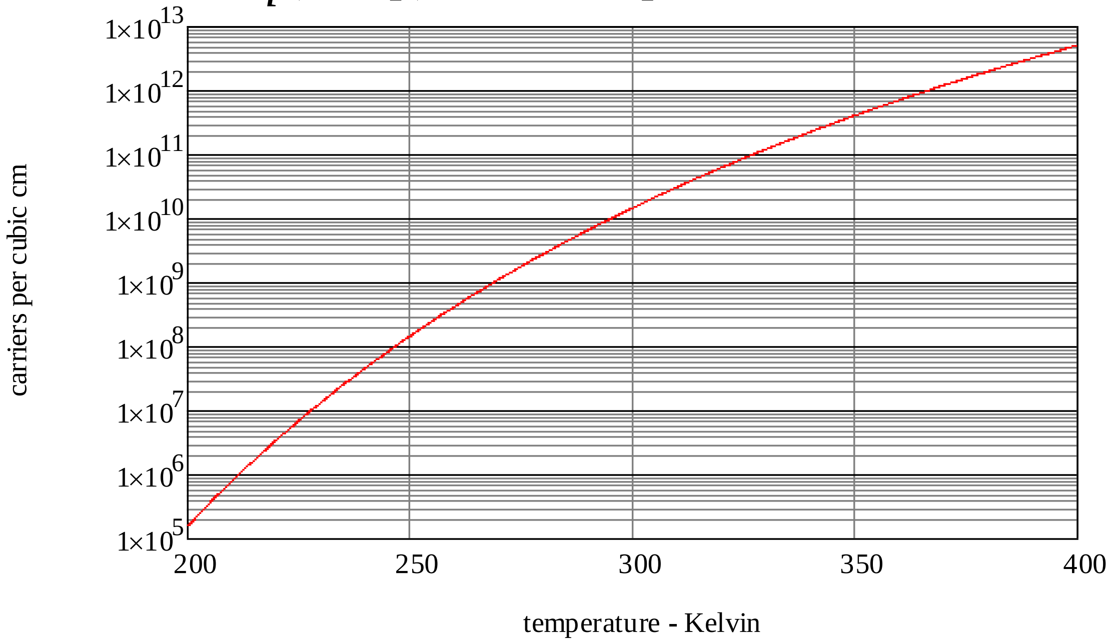
Intrinsic Carrier Concentration of Silicon as a Function of Temperature

$$n_i = BT^{3/2} e^{-E_g/2kT}$$

Kelvin	°Celsius	n_i – cm^{-3}
400	126.85	5.163×10^{12}
300	26.85	1.494×10^{10}
200	-73.15	1.614×10^{5}
147.59	-125.56	1.001
100	-173.15	4.460×10^{-10}
50	-223.15	9.632×10^{-39}
0	-273.15	0

Silicon has approximately
5×10^{22} atoms/cm^3

$$n_i(Temp) := B \cdot Temp^{\frac{3}{2}} e^{\frac{-E_g}{2 \cdot k_b \cdot Temp}}$$



300 K = 80.33 °F ~ room temperature

Product of holes and electrons

It is useful for future purposes to express the product of the hole and free-electron concentration as:

$$pn = {n_i}^2$$

where for Silicon at room temperature $n_i \approx 1.5 \times 10^{10}/\text{cm}^3$. This relationship extends to extrinsic, or doped, silicon as well.

$$n_i(300K) = 1.494 \times 10^{10} \frac{1}{\text{cm}^3}$$

3.2 DOPED SEMICONDUCTORS

Doping Semiconductors

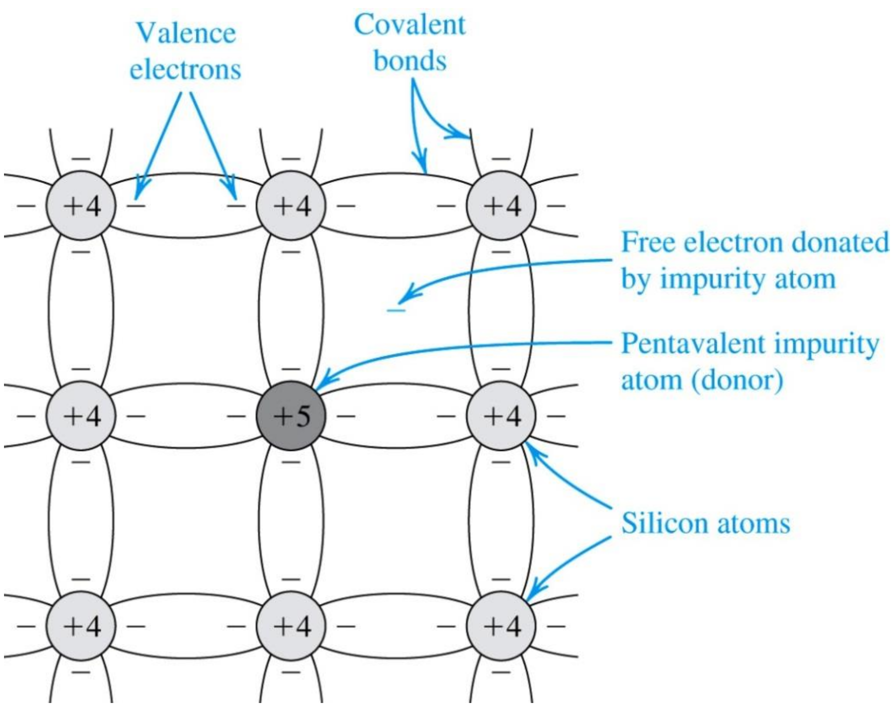


Figure 3.3 A silicon crystal doped by a pentavalent element. Each dopant atom donates a free electron and is thus called a donor. The doped semiconductor becomes *n* type.

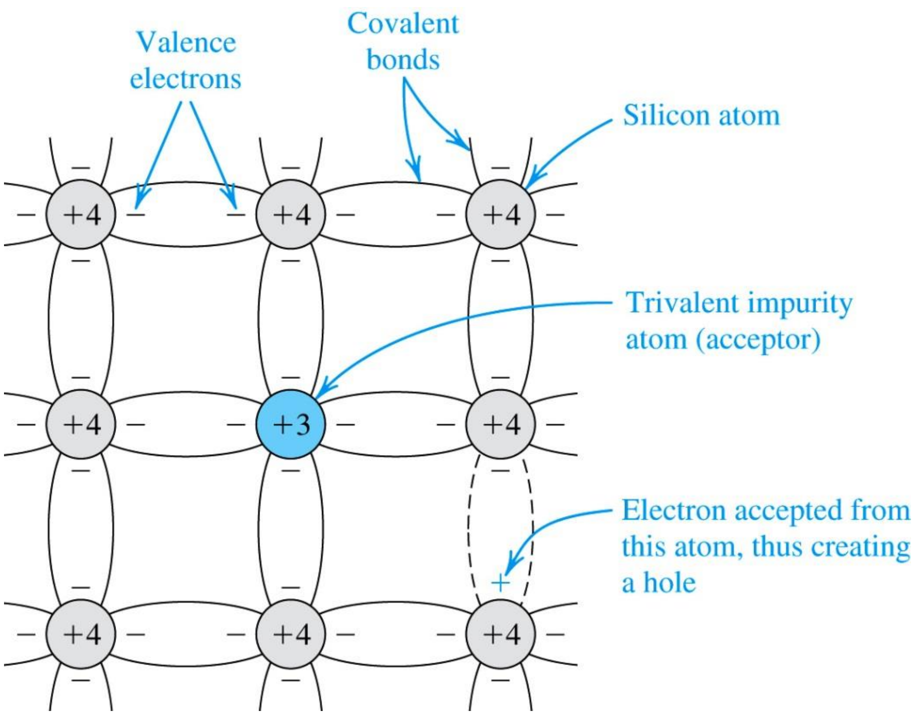


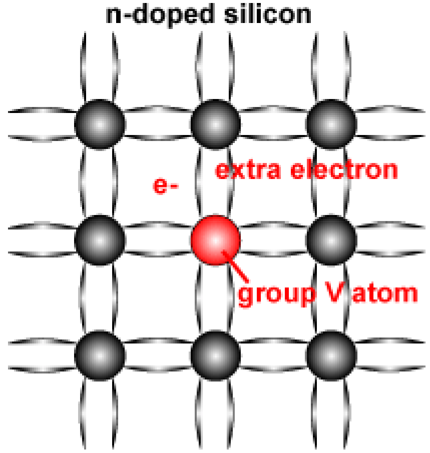
Figure 3.4 A silicon crystal doped with a trivalent impurity. Each dopant atom gives rise to a hole, and the semiconductor becomes *p* type.

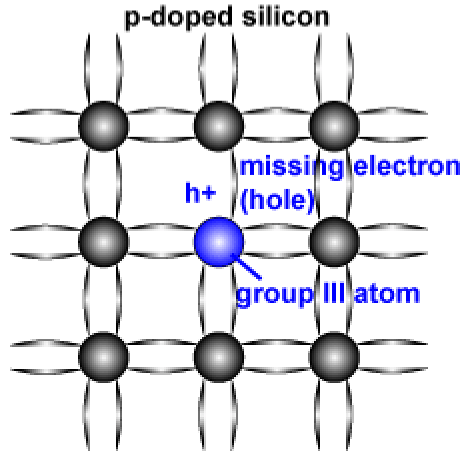
Doping Semiconductors

Table summarizing the properties of semiconductor types.

	P-type (positive)	N-type (negative)
Dopant	Group III (e.g. Boron)	Group V (e.g. Phosphorous)
Bonds	Missing Electrons (Holes)	Excess Electrons
Majority Carriers	Holes	Electrons
Minority Carriers	Electrons	Holes

In a typical semiconductor there might be 10^{17} cm^{-3} majority carriers and 10^6 cm^{-3} minority carriers. Expressed in a different form, the ratio of minority to majority carriers is less than one person to the entire population of the planet. Minority carriers are created either thermally or by incident photons.





http://asdn.net/asdn/physics/semiconductor.shtml

What are *P*-type and *N*-type ?

- Semiconductors are classified in to *P*-type and *N*-type semiconductor
- *P*-type: A *P*-type material is one in which holes are majority carriers i.e. they are positively charged materials (++++)
- *N*-type: A *N*-type material is one in which electrons are majority charge carriers i.e. they are negatively charged materials (-----)

n-type silicon

N_D is the concentration of **donor** atoms (P), usually >> n_i

The concentration of free electrons in the n-type silicon will be $n_n \approx N_D$ where the subscript n denotes n-type silicon. Thus n_n is determined by the doping concentration and not the temperature. This is not the case, however, for the hole concentration. All the holes in the n-type silicon are generated by thermal ionization. Their concentration is given by

$$p_n n_n = {n_i}^2 \qquad p_n \approx \frac{{n_i}^2}{N_D} \qquad n_n \gg p_n$$

electrons are the **majority** charge carriers and **holes** are the **minority** charge carrier.

p-type silicon

N_A is the concentration of **acceptor** atoms (B), usually >> n_i

The concentration of free holes in the *p*-type silicon will be $p_p \approx N_A$ where the subscript *p* denotes *p*-type silicon. Thus p_p is determined by the doping concentration and not the temperature. This is not the case, however, for the electron concentration. All the electrons in the *p*-type silicon are generated by thermal ionization. Their concentration is given by

$$p_p n_p = {n_i}^2 \qquad n_p \approx \frac{{n_i}^2}{N_A} \qquad p_p \gg n_p$$

holes are the **majority** charge carriers and **electronics** are the **minority** charge carrier.

Example 3.2

Consider an n-type silicon for which the dopant concentration $N_D = 10^{17}/\text{cm}^3$. Find the electron and hole concentrations at $T = 300$ K.

$$n_n \approx N_D = 10^{17}/\text{cm}^3$$

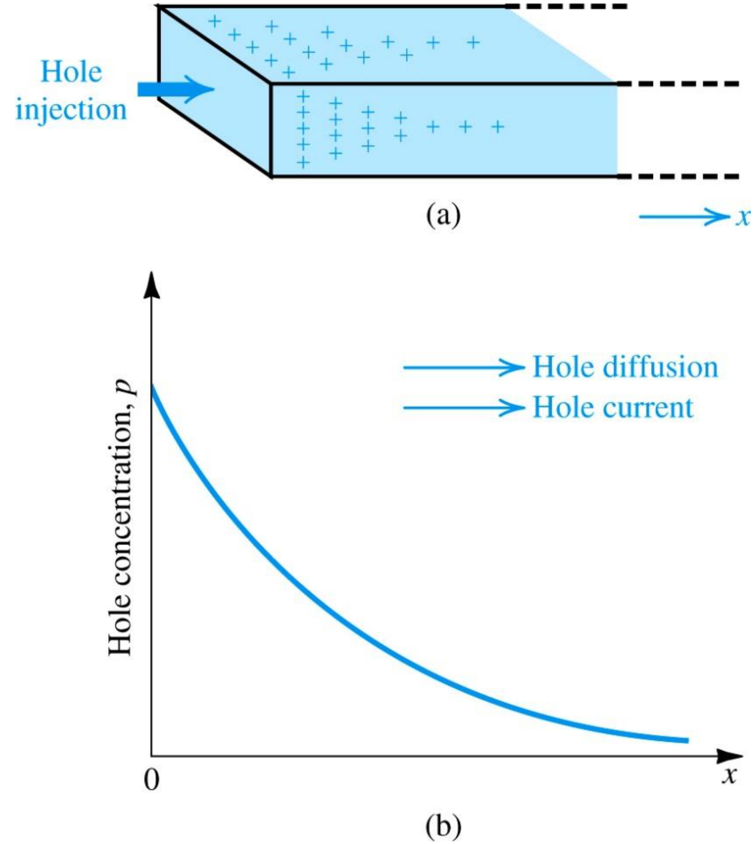
$$\text{at } T = 300 \text{ K}, \; n_i = 1.5 \times 10^{10}/\text{cm}^3$$

$$p_n \approx \frac{{n_i}^2}{N_D} = \frac{(1.5 \times 10^{10})^2}{10^{17}} = 2250 /_{\text{cm}^3}$$

3.3 CURRENT FLOW IN SEMICONDUCTORS

Current Flow in Semiconductors

1. Drift
2. Diffusion



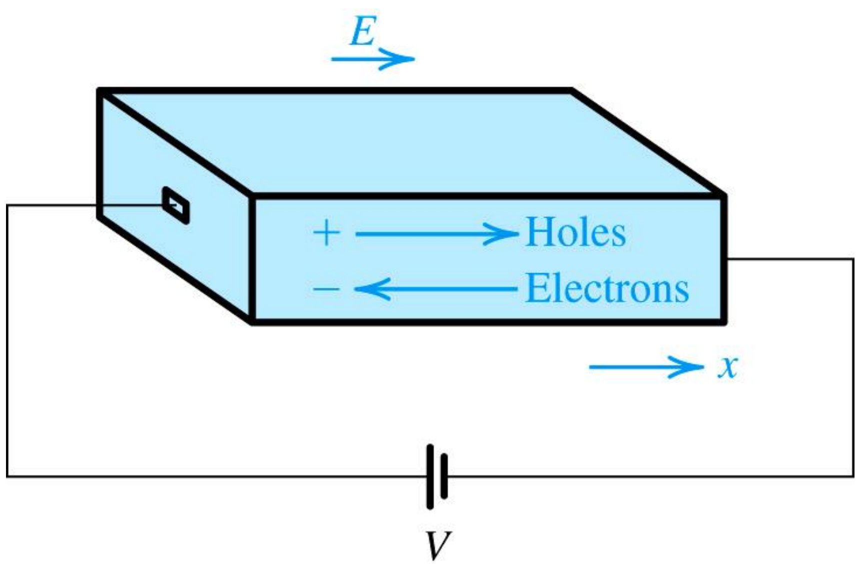


Figure 3.5 An electric field *E* established in a bar of silicon causes the holes to drift in the direction of *E* and the free electrons to drift in the opposite direction. Both the hole and electron drift currents are in the direction of *E*.

Figure 3.6 A bar of silicon **(a)** into which holes are injected, thus creating the hole concentration profile along the *x* axis, shown in **(b)**. The holes diffuse in the positive direction of *x* and give rise to a hole-diffusion current in the same direction. Note that we are not showing the circuit to which the silicon bar is connected.

1) Drift current

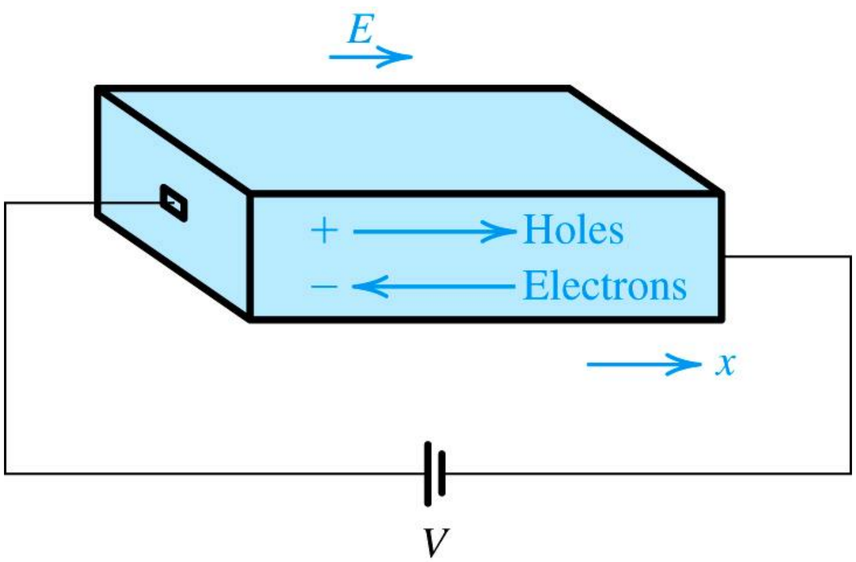


Figure 3.5 An electric field E established in a bar of silicon causes the holes to drift in the direction of E and the free electrons to drift in the opposite direction. Both the hole and electron drift currents are in the direction of E.

Drift speed/velocity for holes

$$v_{p-drift} = \mu_p E$$

Drift speed/velocity for electrons

$$v_{n-drift} = -\mu_n E$$

Where

ν is the velocity in cm/s

E is the electric field (V/cm)

μ is the mobility ($cm^2/(V\ s)$)

For intrinsic silicon

$$\mu_p = 480 \frac{\text{cm}^2}{V \cdot s}$$ **hole mobility**

$$\mu_n = 1350 \frac{\text{cm}^2}{V \cdot s}$$ **electron mobility**

Si Carrier Mobility vs Temperature and Doping

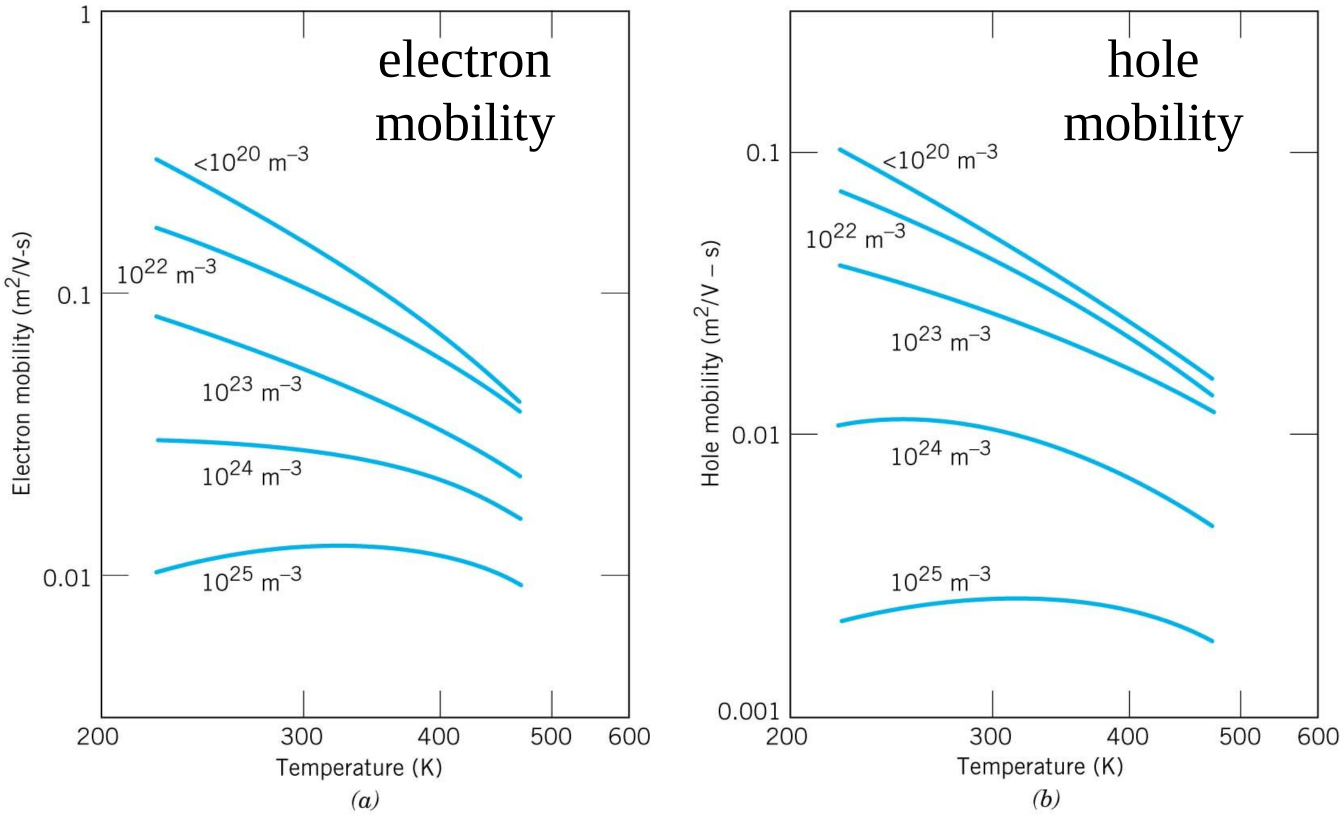


FIGURE 18.18 Temperature dependence of (*a*) electron and (*b*) hole mobilities for silicon that has been doped with various donor and acceptor concentrations. Both sets of axes are scaled logarithmically. (From W. W. Gärtner, "Temperature Dependence of Junction Transistor Parameters," *Proc. of the IRE,* **45,** 667, 1957. Copyright © 1957 IRE now IEEE.)

1) Drift Current

The hole component of the drift current

$$I_p = Aqpv_{p-drift}$$

$$I_p = Aqp\mu_p E$$

$$J_p = \frac{I_p}{A} = qp\mu_p E$$ current density

The electron component of the drift current

$$I_n = -Aqnv_{n-drift}$$

$$I_n = Aqn\mu_n E$$

$$J_n = \frac{I_n}{A} = qn\mu_n E$$ current density

$$J = J_p + J_n = q(p\mu_p + n\mu_n)E$$ total current density

$$\mathrm{J} = \sigma E$$

$$\mathrm{J} = \frac{E}{\rho}$$

$$\mathrm{J} = \sigma E \qquad \sigma = q(p\mu_p + n\mu_n)$$

where σ is the **conductivity** [S/cm]

$$\mathrm{J} = \frac{E}{\rho} \qquad \rho \equiv \frac{1}{\sigma} = \frac{1}{q(p\mu_p + n\mu_n)}$$

where ρ is the **resistivity** [ohm·cm]

Resistivity vs Dopant Concentration for Si at RT

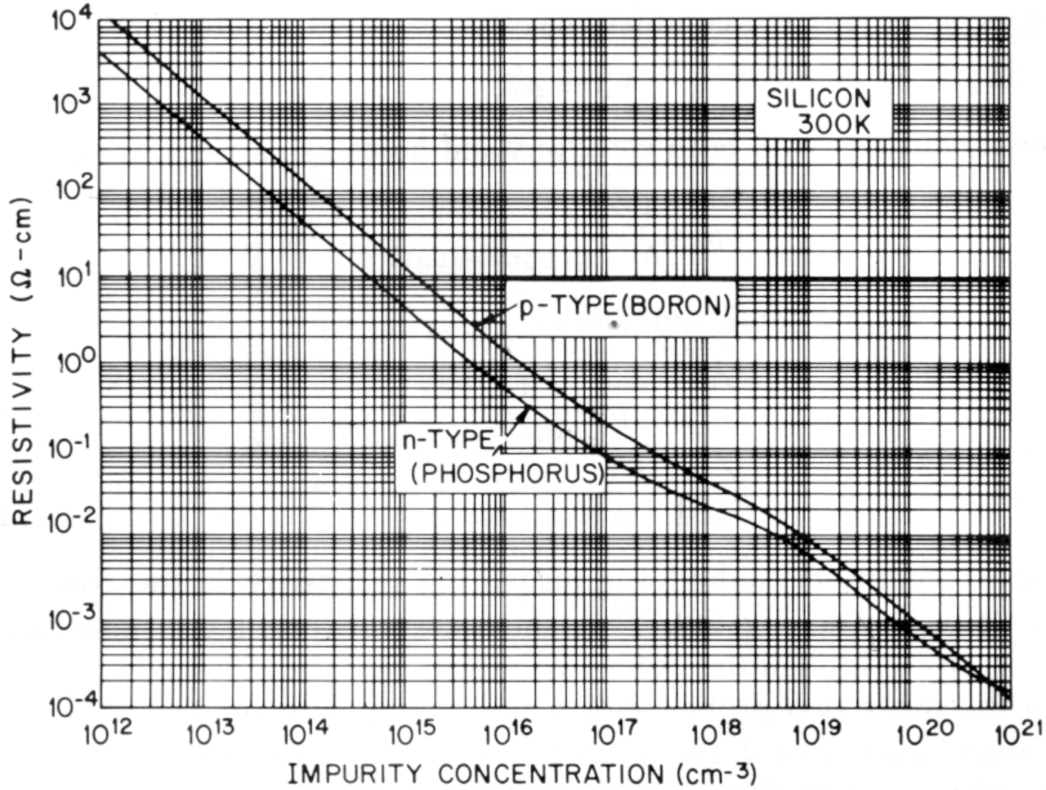


Fig. 21 Resistivity versus impurity concentration for silicon at 300 K. (After Beadle, Plummer, and Tsai, Ref. 38.)

Example 3.3

Find the resistivity of (a) intrinsic silicon and (b) *p*-type silicon with $N_A = 10^{16}$ /cm^3. Use $n_i = 1.5 \times 10^{10}$/cm^3, and assume that for intrinsic silicon μ_n= 1350 cm^2/Vs and μ_p= 480 cm^2/Vs, and for doped silicon μ_n= 1110 cm^2/Vs and μ_p= 400 cm^2/Vs. (Note that doping results in reduced carrier mobilities).

intrinsic Silicon

$$\mu_n := 1350 \frac{\mathrm{cm}^2}{\mathrm{V \cdot s}} \qquad \mu_p := 480 \frac{\mathrm{cm}^2}{\mathrm{V \cdot s}}$$

$$n_i := \frac{1.5 \cdot 10^{10}}{\mathrm{cm}^3} \qquad p_i := \frac{1.5 \cdot 10^{10}}{\mathrm{cm}^3}$$

$$\rho := \frac{1}{q \cdot \left(p_i \cdot \mu_p + n_i \cdot \mu_n\right)} = 2.27 \times 10^5 \, \Omega \cdot \mathrm{cm}$$

Example 3.3

Find the resistivity of (a) intrinsic silicon and (b) *p*-type silicon with $N_A = 10^{16}$ /cm^3. Use $n_i = 1.5 \times 10^{10}$/cm^3, and assume that for intrinsic silicon $\mu_n = 1350$ cm^2/Vs and $\mu_p = 480$ cm^2/Vs, and for doped silicon $\mu_n = 1110$ cm^2/Vs and $\mu_p = 400$ cm^2/Vs. (Note that doping results in reduced carrier mobilities).

Doped p type Silicon

$$N_A := \frac{1 \cdot 10^{16}}{\mathrm{cm}^3} \qquad \mu_n := 1110 \frac{\mathrm{cm}^2}{\mathrm{V \cdot s}} \qquad \mu_p := 400 \frac{\mathrm{cm}^2}{\mathrm{V \cdot s}}$$

$$p_p := N_A = 1 \times 10^{16} \frac{1}{\mathrm{cm}^3} \qquad n_p := \frac{{n_i}^2}{N_A} = 2.25 \times 10^4 \frac{1}{\mathrm{cm}^3}$$

$$\rho := \frac{1}{q \cdot \left(p_p \cdot \mu_p + n_p \cdot \mu_n\right)} = 1.558 \,\Omega \cdot \mathrm{cm}$$

2) Diffusion Current

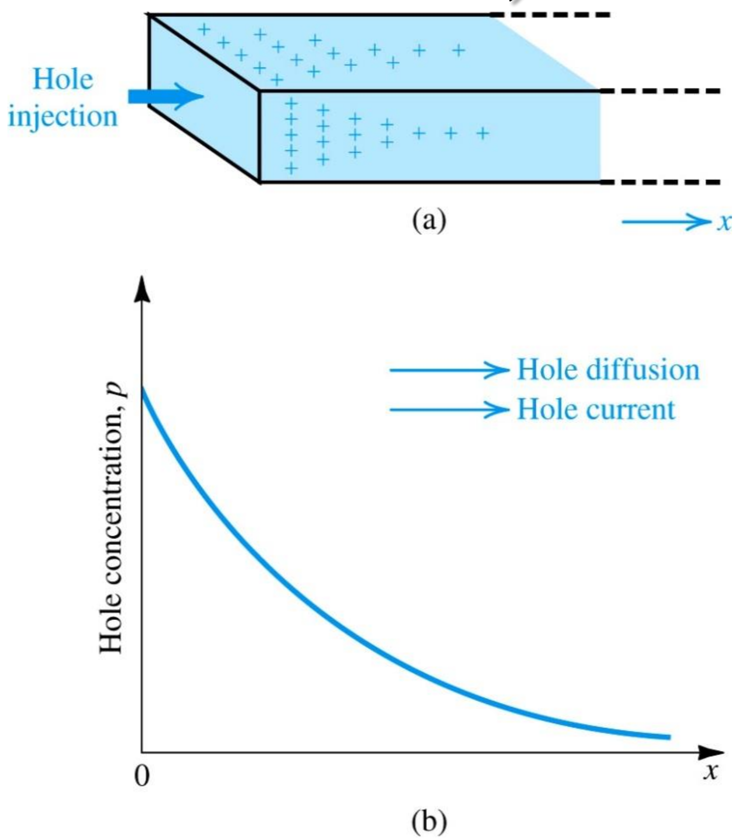


Figure 3.6 A bar of silicon **(a)** into which holes are injected, thus creating the hole concentration profile along the *x* axis, shown in **(b)**. The holes diffuse in the positive direction of *x* and give rise to a hole-diffusion current in the same direction. Note that we are not showing the circuit to which the silicon bar is connected.

The magnitude of the current at any point is proportional to the slope of the concentration profile, or **concentration gradient**, at that point.

The hole diffusion current density $\left[\mathrm{A/cm^2}\right]$

$$J_p = -qD_p \frac{dp(x)}{dx}$$

Where

q is the magnitude of the electron charge

D_p is the **diffusion constant** ($\mathrm{cm^2/s}$)

$p(x)$ is the hole concentration at point x

Electron Current Density due to Diffusion

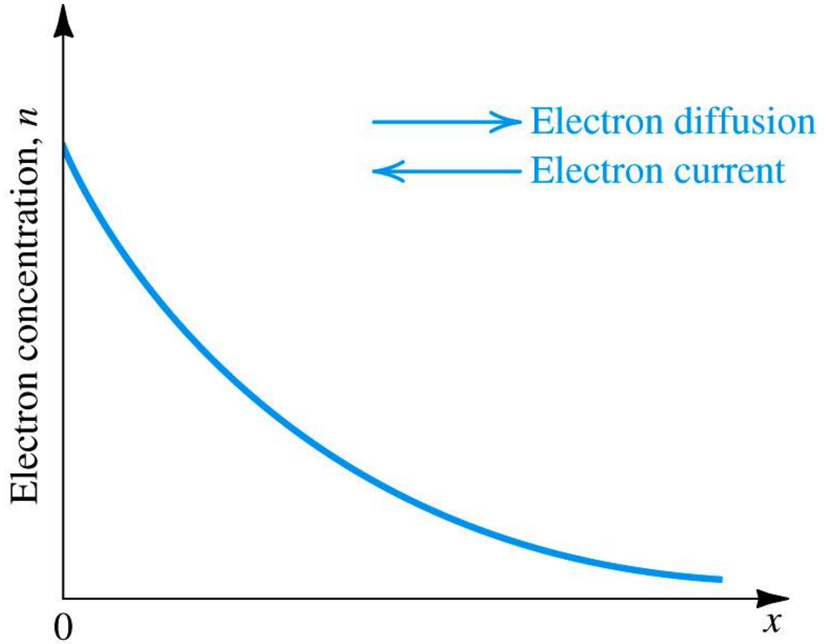


Figure 3.7 If the electron-concentration profile shown is established in a bar of silicon, electrons diffuse in the *x* direction, giving rise to an electron-diffusion current in the negative -*x* direction.

The electron current density $\left[\mathrm{A/cm^2}\right]$

$$J_n = qD_n \frac{dn(x)}{dx}$$

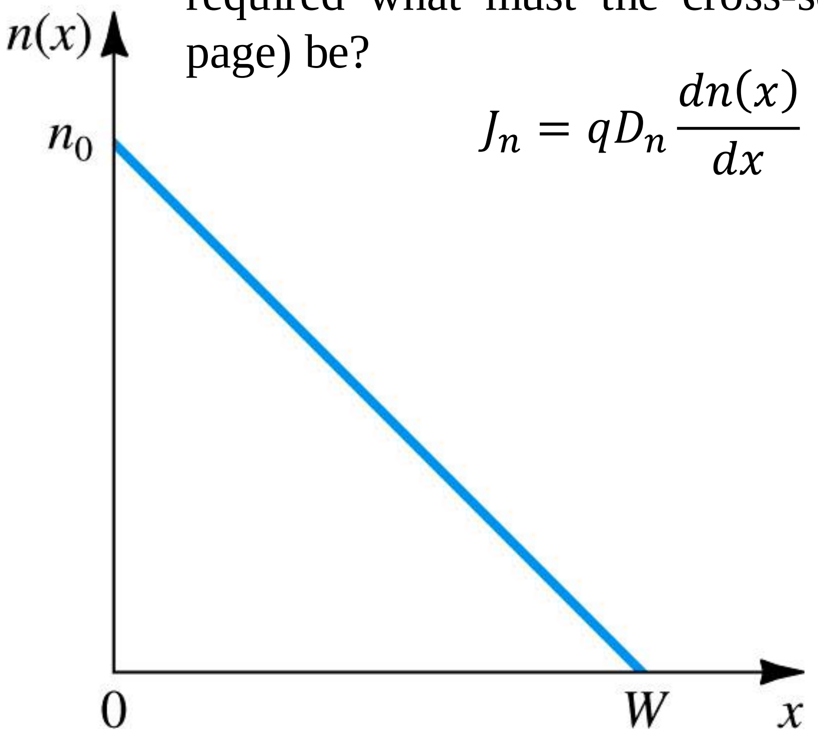
Where
q is the magnitude of the electron charge
D_n is the **diffusion constant** ($\mathrm{cm^2/s}$)
$n(x)$ is the electron concentration at point x

For intrinsic silicon typical values of the diffusion constant are:

$$D_p = 12\ \mathrm{cm^2/s}$$
$$D_n = 35\ \mathrm{cm^2/s}$$

Exercise 3.5 (p.147)

The linear electron-concentration profile shown in Fig. E3.5 has been established in a piece of silicon. If $n_0 = 10^{17}$ / cm^3 and $W = 1\mu$m, find the electron-current density in micro amperes per micron squared (μA/μm^2). If a diffusion current of 1 mA is required what must the cross-sectional area (in a direction perpendicular to the page) be?



$$J_n = qD_n \frac{dn(x)}{dx}$$

For intrinsic silicon typical values of the diffusion constant are: $D_p = 12$ cm^2/s
$D_n = 35$ cm^2/s

$$J_n := q \cdot D_n \cdot \frac{10^{17} \cdot \frac{1}{\text{cm}^3}}{1\mu\text{m}} = 56.175 \frac{\mu\text{A}}{\mu\text{m}^2}$$

$$Area := \frac{1 \cdot mA}{J_n} = 17.802\mu\text{m}^2$$

Diffusion Constant, D, and mobility, μ

A simple but powerful relationship ties the diffusion constant with the mobility

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T$$ **Einstein Relationship**

Where $V_T = \frac{kT}{q}$ is known as the **thermal voltage**

k is the Boltzmann constant [8.617×10^{-5} eV/K]
T is the temperature in Kelvin
q is the magnitude of the electrical charge on the electron [1.602×10^{-19} C]

At room temperature (~300K) V_T = 25.9 mV

$$k_b := 8.617 \cdot 10^{-5} \frac{\mathrm{eV}}{\mathrm{K}} \qquad q := 1.602 \cdot 10^{-19} \mathrm{C} \qquad V_T := \frac{k_b \cdot 300K}{q} = 25.851 \cdot \mathrm{mV}$$

Homework #5

- Read Chapter 3
- Chapter 3 Problems:
  - 3.1*
  - 3.3*
  - 3.5*
  - 3.8
  - 3.11

* Answers in Appendix L

3.4 THE *pn* JUNCTION

Simplified *pn* Junction

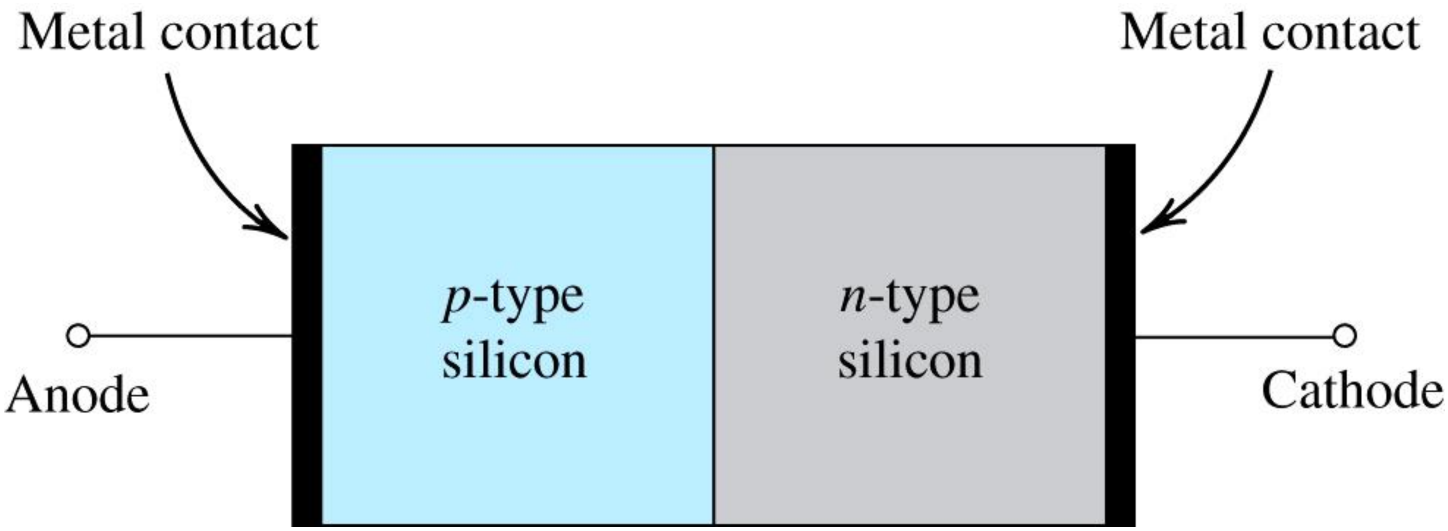


Figure 3.8 Simplified physical structure of the *pn* junction. (Actual geometries are given in Appendix A.) As the *pn* junction implements the junction diode, its terminals are labeled anode and cathode.

Operation with Open Circuit Terminals

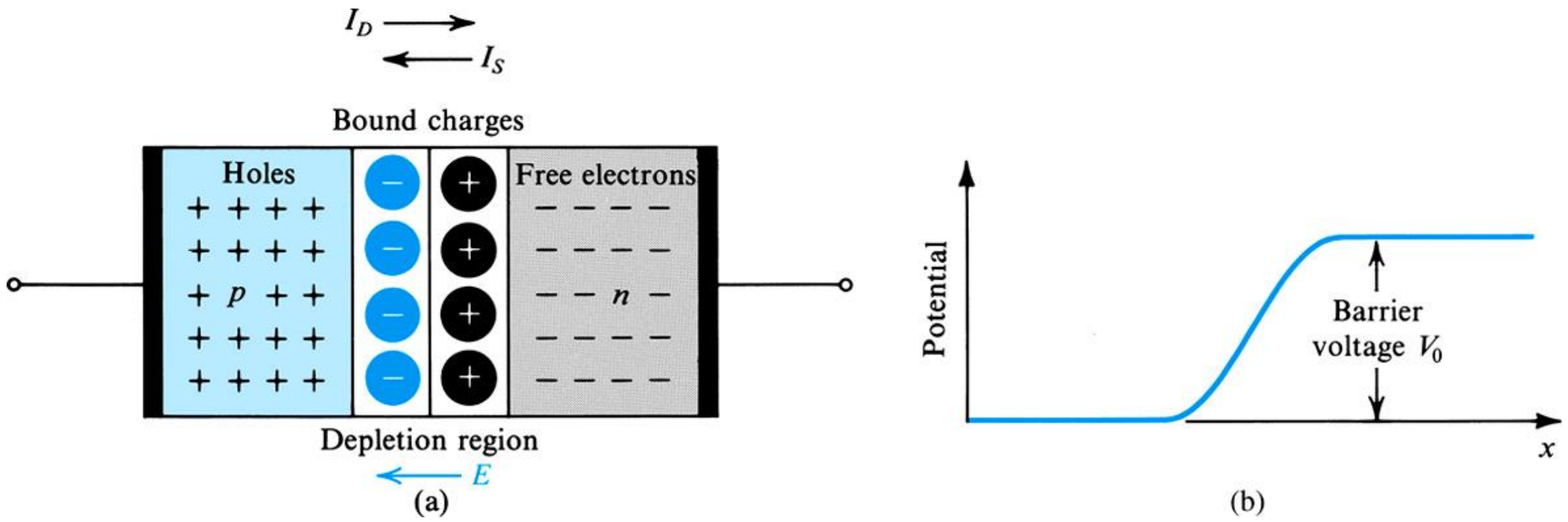


Figure 3.9 (a) The *pn* junction with no applied voltage (open-circuited terminals). **(b)** The potential distribution along an axis perpendicular to the junction.

a **carrier-depletion region** will exist on both sides of the junction, with the *n* side of this region positively charged and the *p* side negatively charged. This **carrier-depletion region** or, simply, **depletion region** is also called the **space-charge region**. The charges on both sides of the depletion region cause an electric field *E* to be established across the region in the direction indicated in Fig. 3.9.

Operation with Open Circuit Terminals

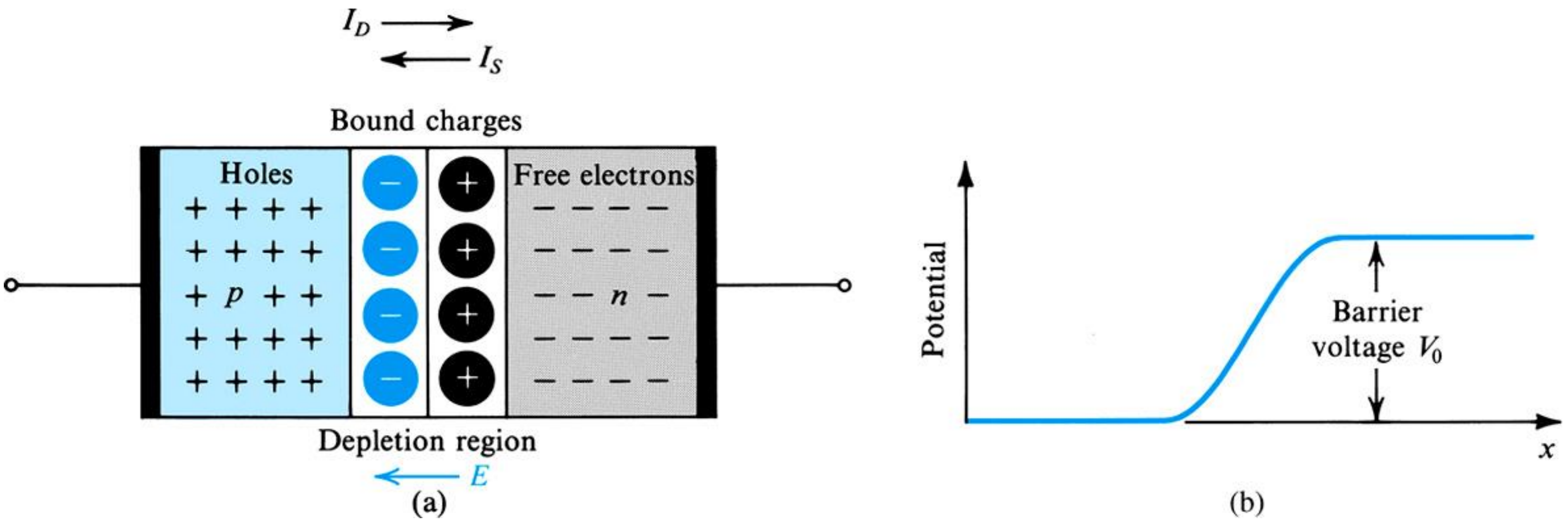


Figure 3.9 (a) The *pn* junction with no applied voltage (open-circuited terminals). **(b)** The potential distribution along an axis perpendicular to the junction.

the resulting electric field opposes the diffusion of holes into the *n* region and electrons into the *p* region. In fact, the voltage drop across the depletion region acts as a **barrier** that has to be overcome for holes to diffuse into the *n* region and electrons to diffuse into the *p* region. The larger the barrier voltage, the smaller the number of carriers that will be able to overcome the barrier and hence the lower the magnitude of diffusion current.

Drift and Diffusion Currents and Equilibrium

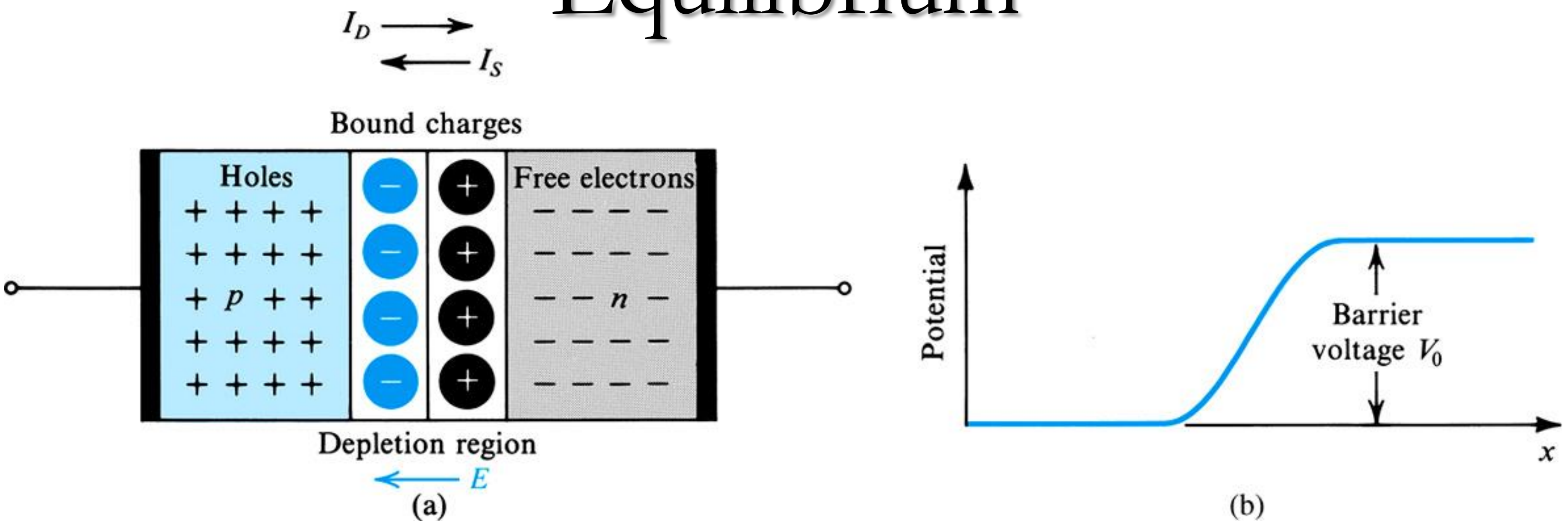


Figure 3.9 (a) The *pn* junction with no applied voltage (open-circuited terminals). **(b)** The potential distribution along an axis perpendicular to the junction.

I_D is the majority-carrier diffusion current. I_S is the minority-carrier drift current.

Under open-circuit conditions no external current exists; thus the two opposite currents across the junction must be equal in magnitude.

$$I_D = I_S$$

Drift and Diffusion Currents and Equilibrium

$$I_D = I_S$$

This equilibrium condition is maintained by the barrier voltage V_0. Thus, if for some reason I_D exceeds I_S then more bound charge will be uncovered on both sides of the junction, the depletion layer will widen, and the voltage across it (V_0) will increase. This in turn causes I_D to decrease until equilibrium is achieved with $I_D = I_S$. On the other hand, if I_S exceeds I_D , then the amount of uncovered charge will decrease, the depletion layer will narrow, and the voltage across it (V_0) will decrease. This causes I_D to increase until equilibrium is achieved with $I_D = I_S$.

$$V_0 = V_T \ln\left(\frac{N_A N_D}{{n_i}^2}\right)$$ **Junction built-in voltage**

The junction built-in voltage, V_0, depends both on doping concentrations and on temperature. Typically, for Silicon at room temperature, V_0 is in the range of 0.6 V to 0.9 V.

The Depletion Region

$$qAx_nN_D = qAx_pN_A$$

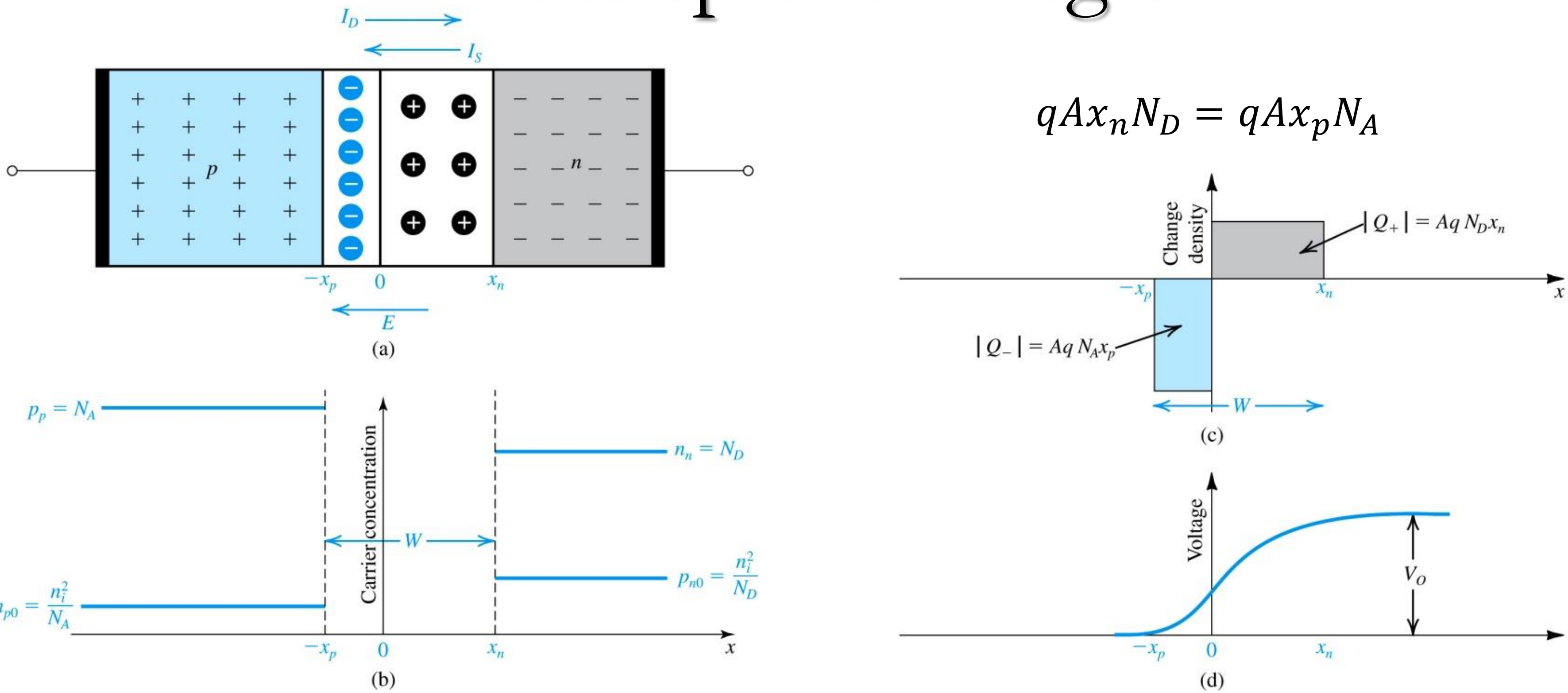


Figure 3.10 (a) A *pn* junction with the terminals open-circuited. (b) Carrier concentrations; note that $N_A > N_D$. (c) The charge stored in both sides of the depletion region; $Q_J = |Q_+| = |Q_-|$. (d) The built-in voltage V_0.

$$\frac{x_n}{x_p} = \frac{N_A}{N_D}$$

The Depletion Region Width

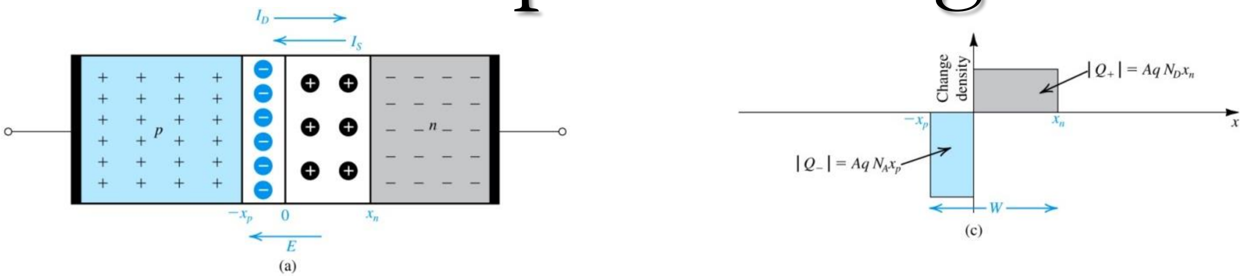


Figure 3.10 (a) A *pn* junction with the terminals open-circuited. (c) The charge stored in both sides of the depletion region; $Q_J = |Q_+| = |Q_-|$.

$$qAx_nN_D = qAx_pN_A$$

$$\frac{x_n}{x_p} = \frac{N_A}{N_D}$$

In actual practice, it is usual for one side of the junction to be much more heavily doped than the other, With the result that the depletion region exists almost entirely on one side (the lightly doped side).

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$$

ε_S is the electrical permittivity of Si
$= 11.7\ \varepsilon_0$
$= 11.7 \times 8.85 \times 10^{-14}$ F/cm
$= 1.04 \times 10^{-12}$ F/cm

$$x_n = W\frac{N_A}{N_A + N_D} \qquad x_p = W\frac{N_D}{N_A + N_D}$$

The Depletion Region Charge

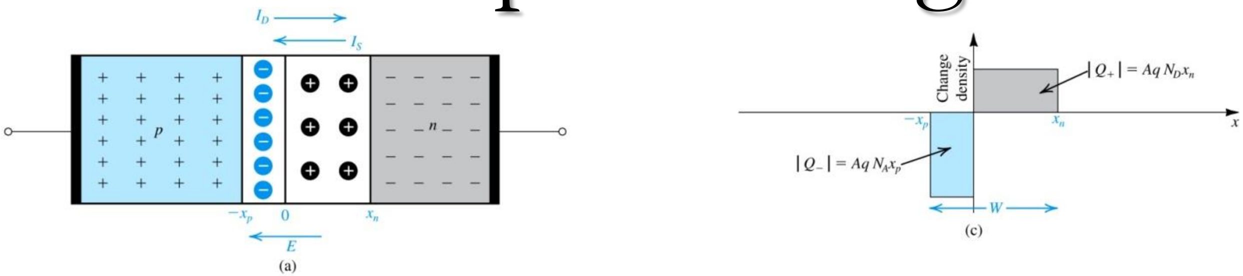


Figure 3.10 (a) A *pn* junction with the terminals open-circuited. (c) The charge stored in both sides of the depletion region; $Q_J = |Q_+| = |Q_-|$.

$$qAx_nN_D = qAx_pN_A$$

$$\frac{x_n}{x_p} = \frac{N_A}{N_D}$$

The charge stored on either side of the depletion region can be expressed in terms of *W*.

$$Q_J = |Q_+| = |Q_-|$$

$$Q_J = Aq\left(\frac{N_AN_D}{N_A + N_D}\right)W$$

$$Q_J = A\sqrt{2\varepsilon_S q\left(\frac{N_AN_D}{N_A + N_D}\right)V_0}$$

Example 3.5

Consider a *pn* junction in equilibrium at room temperature (T = 300 K) for which the doping concentrations are $N_A = 10^{18}/\text{cm}^3$ and $N_D = 10^{16}/\text{cm}^3$ and the cross-sectional area $A = 10^{-4}$ cm^2. Calculate p_p, n_{p0}, n_n, p_{n0}, V_0, W, x_n, x_p, and Q_j. Use n_i = 1.5 x $10^{10}/\text{cm}^3$.

$$p_p n_p = p_n n_n = n_i^2 = (1.5 \text{ x } 10^{10}/\text{cm}^3)^2$$

$$N_A := 1\cdot 10^{18}\cdot\frac{1}{\text{cm}^3} \qquad N_D := 1\cdot 10^{16}\cdot\frac{1}{\text{cm}^3} \qquad n_i := 1.5\cdot 10^{10}\cdot\frac{1}{\text{cm}^3}$$

$$p_p := N_A = 1\times 10^{18}\frac{1}{\text{cm}^3} \qquad n_p := \frac{n_i^2}{N_A} = 225\frac{1}{\text{cm}^3}$$

$$n_n := N_D = 1\times 10^{16}\frac{1}{\text{cm}^3} \qquad p_n := \frac{n_i^2}{N_D} = 2.25\times 10^{4}\frac{1}{\text{cm}^3}$$

$$V_T := 25.9\text{mV} \qquad V_0 := V_T\cdot ln\left(\frac{N_A\cdot N_D}{n_i^2}\right) = 0.814\cdot\text{V}$$

Example 3.5

Consider a *pn* junction in equilibrium at room temperature (T = 300 K) for which the doping concentrations are $N_A = 10^{18}/\text{cm}^3$ and $N_D = 10^{16}/\text{cm}^3$ and the cross-sectional area $A = 10^{-4}\ \text{cm}^2$. Calculate p_p, n_{p0}, n_n, p_{n0}, V_0, W, x_n, x_p, and Q_j. Use $n_i = 1.5 \times 10^{10}/\text{cm}^3$.

$$\varepsilon_{Si} := 11.7 \cdot \varepsilon_0 \qquad Area := 10^{-4}\text{cm}^2$$

$$Width := \sqrt{\frac{2 \cdot \varepsilon_{Si}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) \cdot V_0} = 325.8 \cdot \text{nm}$$

$$x_n := Width \cdot \frac{N_A}{N_A + N_D} = 322.5 \cdot \text{nm} \qquad x_p := Width \cdot \frac{N_D}{N_A + N_D} = 3.2 \cdot \text{nm}$$

$$Q_J := Area \cdot q \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot Width = 5.177 \times 10^{-12} \cdot \text{C}$$

$$Q_J = 5.177 \cdot \text{pC}$$

3.5 THE *pn* JUNCTION WITH APPLIED VOLTAGE

pn Junction Under Three Different Bias Conditions

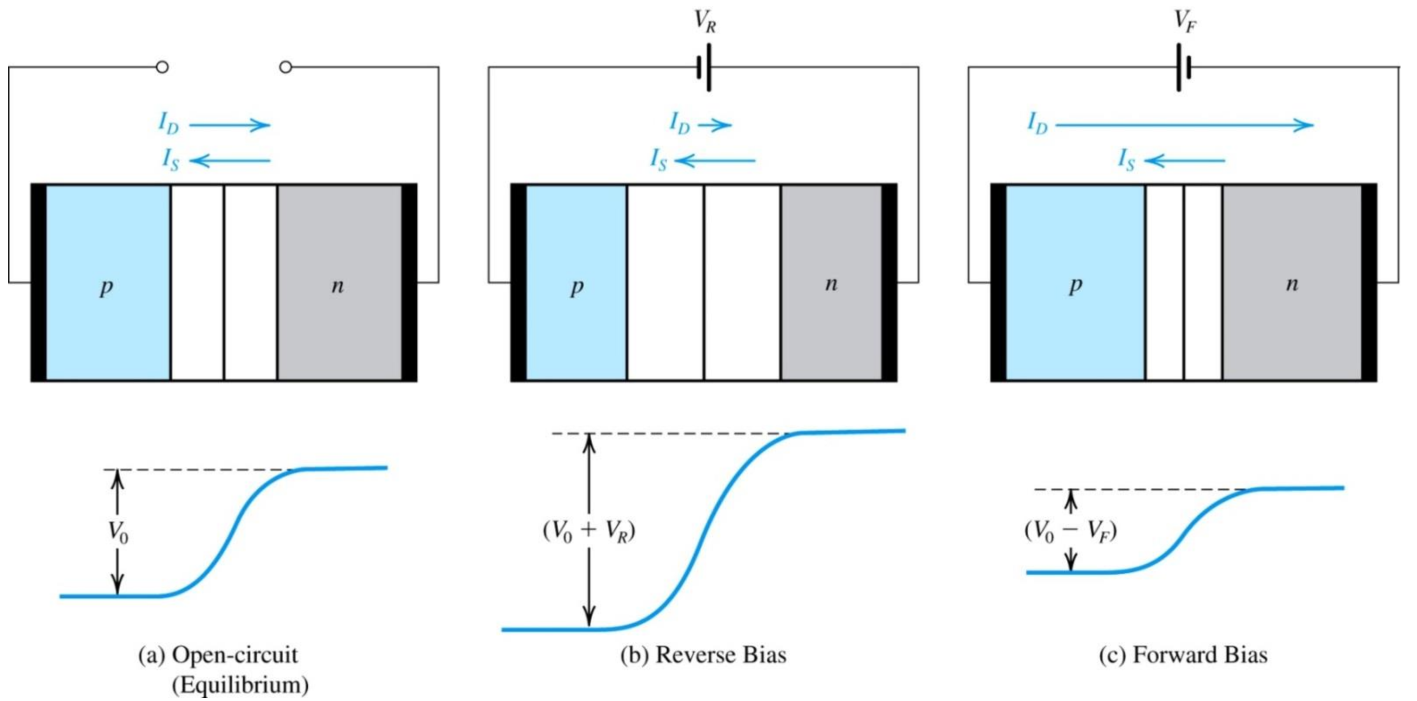


Figure 3.11 The *pn* junction in: **(a)** equilibrium; **(b)** reverse bias; **(c)** forward bias.

$V = V_0$	$V = V_0 + V_R$	$V = V_0 - V_F$
$I = 0$	$I \approx I_S$	$I = I_D - I_S \approx I_D$

The Current-Voltage Relationship of the Junction

The concentration of holes in the *n* region at the edge of the depletion region will increase considerably. In fact, an important result from device physics shows that the steady-state concentration at the edge of the depletion region will be

$$p_n(x_n) = p_{n0} e^{V/V_T}$$

We describe this situation as follows: The forward-bias voltage *V* results in an **excess concentration** of minority holes at $x = x_n$, given by

Excess concentration at $x = x_n$ $= p_{n0} e^{V/V_T} - p_{n0} = p_{n0}\left(e^{V/V_T} - 1\right)$

$$p_n(x) = p_{n0} + (\text{excess concentration}) e^{-(x-x_n)/L_p}$$

$$p_n(x) = p_{n0} + p_{n0}\left(e^{V/V_T} - 1\right) e^{-(x-x_n)/L_p}$$

L_p is the **diffusion length** of holes in the *n* material

The *I-V* Relationship of the Junction

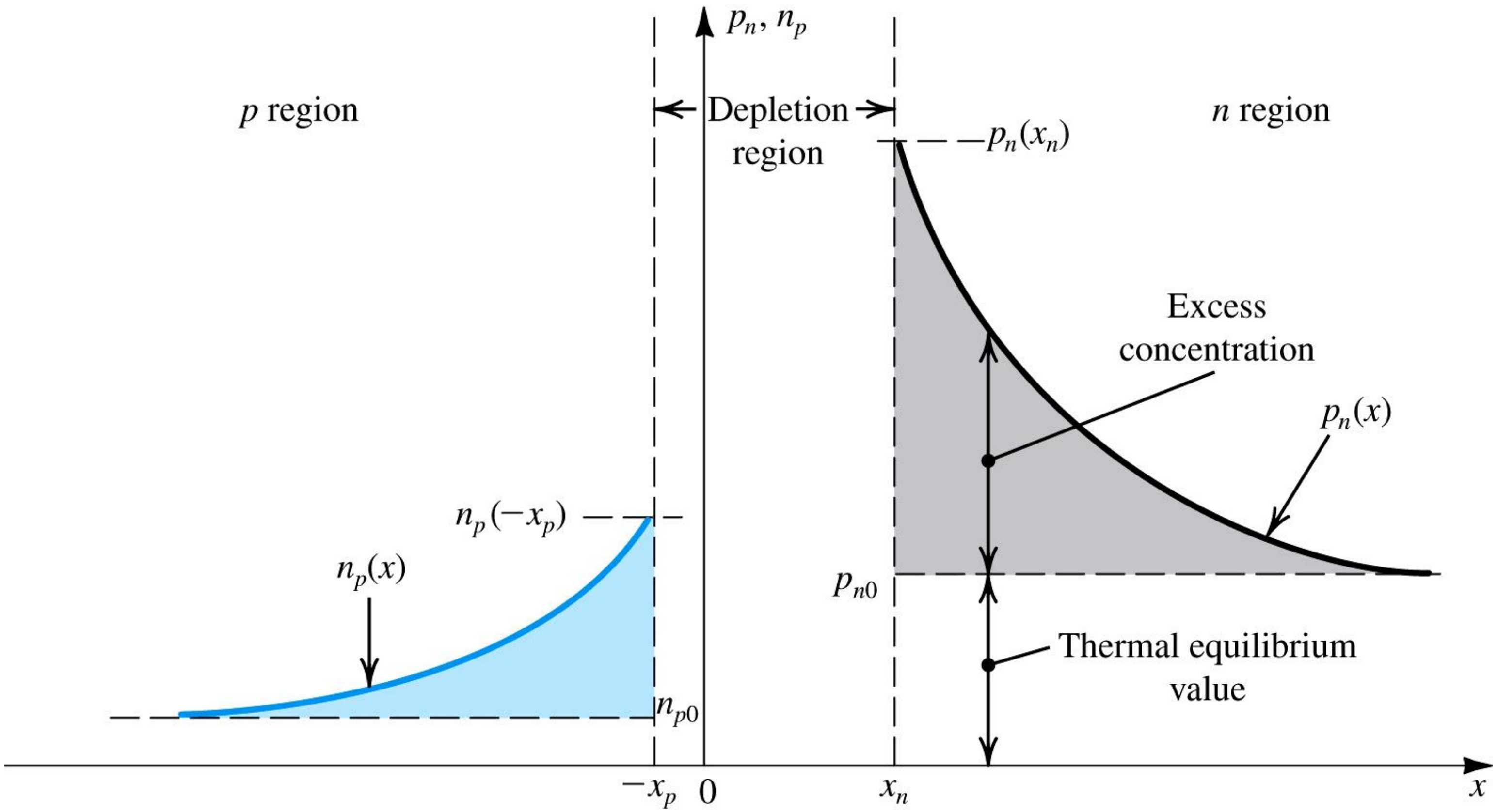


Figure 3.12 Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region; $N_A \gg N_D$.

The *I-V* Relationship of the Junction

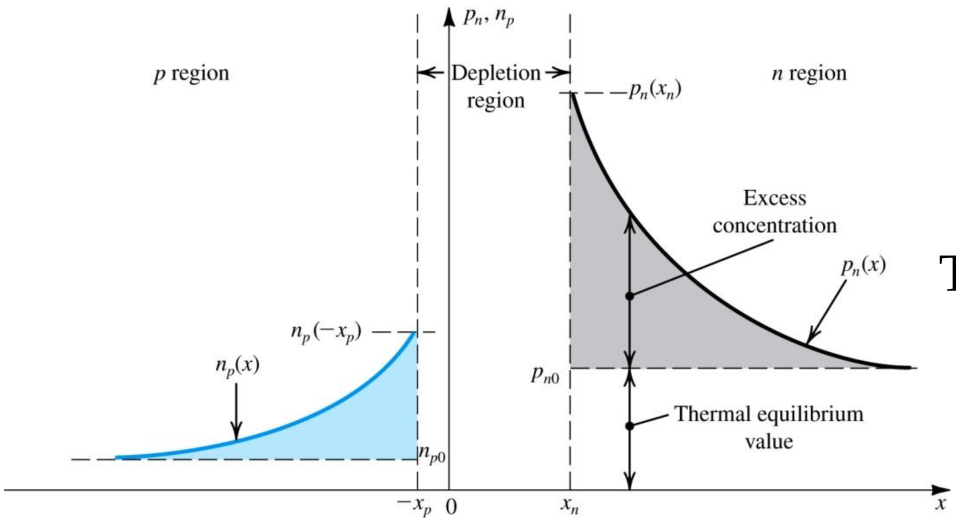


Figure 3.12 Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region; $N_A \gg N_D$.

$$p_n(x) = p_{n0} + p_{n0}\left(e^{V/V_T} - 1\right)e^{-(x-x_n)/L_p}$$

The hole diffusion current density $\left[\mathrm{A/cm^2}\right]$

$$J_p = -qD_p \frac{dp(x)}{dx}$$

$$J_p(x) = q\left(\frac{D_p}{L_p}\right)p_{n0}\left(e^{V/V_T} - 1\right)e^{-(x-x_n)/L_p}$$

Maximum at $x = x_n$ is

$$J_p(x_n) = q\left(\frac{D_p}{L_p}\right)p_{n0}\left(e^{V/V_T} - 1\right)$$

The electron diffusion current density at $x = -x_p$ is

$$J_n(-x_p) = q\left(\frac{D_n}{L_n}\right)n_{p0}\left(e^{V/V_T} - 1\right)$$

The *I-V* Relationship of the Junction

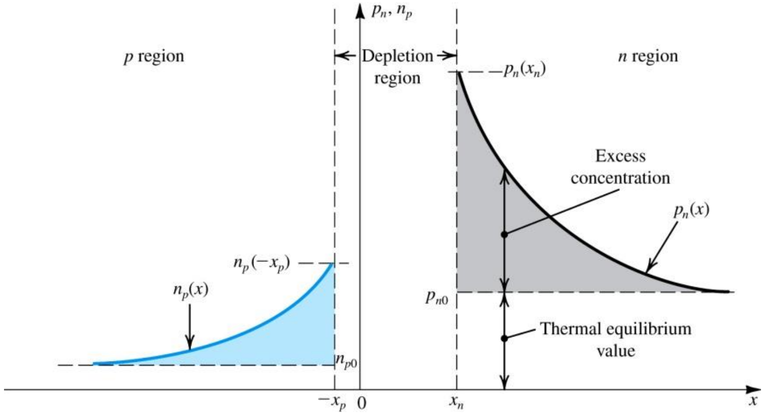


Figure 3.12 Minority-carrier distribution in a forward-biased *pn* junction. It is assumed that the *p* region is more heavily doped than the *n* region; $N_A \gg N_D$.

current densities $[\mathrm{A/cm^2}]$

$$J_p(x_n) = q\left(\frac{D_p}{L_p}\right) p_{n0}\left(e^{V/V_T} - 1\right)$$

$$J_n(-x_p) = q\left(\frac{D_n}{L_n}\right) n_{p0}\left(e^{V/V_T} - 1\right)$$

current [A]

$$I = A\left(J_p + J_n\right)$$

$$I = Aq\left(\frac{D_p}{L_p} p_{n0} + \frac{D_n}{L_n} n_{p0}\right)\left(e^{V/V_T} - 1\right)$$

$$I = Aq{n_i}^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)\left(e^{V/V_T} - 1\right)$$

The *I-V* Relationship of the Junction

$$I = Aqn_i{}^2\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)\left(e^{V/V_T} - 1\right)$$

If we define the **saturation current** or **scale current**, I_S, as:

$$I_S = Aqn_i{}^2\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)$$

$$I = I_S\left(e^{V/V_T} - 1\right)$$

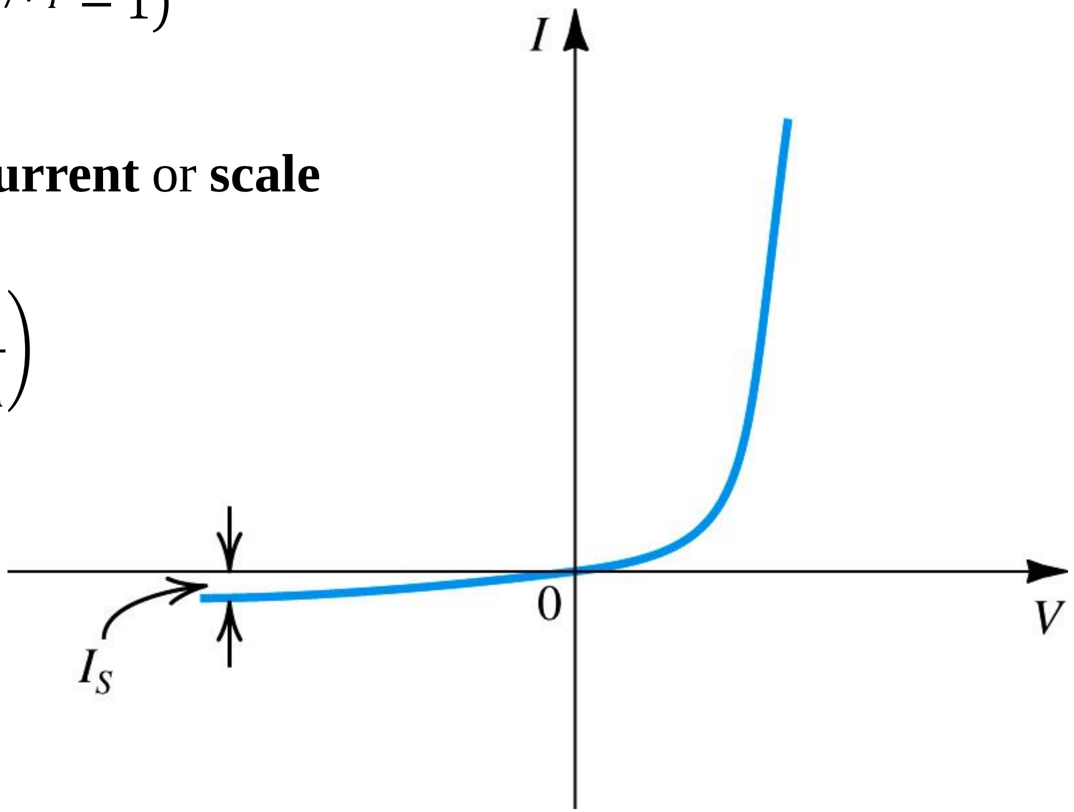


Figure 3.13 The *pn* junction *I–V* characteristic.

Shockley Equation

$$i_D = I_s\left[\exp\left(\frac{V}{nV_T}\right)-1\right] \qquad V_T = \frac{kT}{q}$$

I_s is the saturation current ~10 $^{-14}$ A
V is the diode voltage
n – emission coefficient (varies from 1 - 2)
$k = 1.38 \times 10^{-23}$ J/K is Boltzmann's constant
$q = 1.60 \times 10^{-19}$ C is the electrical charge of an electron.

At a temperature of 300 K, we have $V_T \cong 26\,\text{mV}$

Example 3.6 (a,b)

For the *pn* junction considered in Example 3.5 for which $N_A = 10^{18}/\text{cm}^3$, $N_D = 10^{16}/\text{cm}^3$, $A = 10^{-4}\ \text{cm}^2$, $n_i = 1.5 \times 10^{10}/\text{cm}^3$, let $L_p = 5\ \mu\text{m}$, $L_n = 10\ \mu\text{m}$, D_p (in the n region) $= 10\ \text{cm}^2/\text{s}$, and D_n (in the p region) $= 18\ \text{cm}^2/\text{s}$. The *pn* junction is forward biased and conducting a current $I = 0.1$ mA. Calculate (a) I_S; (b) the forward-bias voltage V; and (c) the component of the current due to hole injection and that due to electron injection across the junction.

(a)

$$I_S := Area \cdot q \cdot n_i^{\,2} \cdot \left(\frac{D_p}{L_p \cdot N_D} + \frac{D_n}{L_n \cdot N_A} \right) = 7.274\,\text{fA}$$

(b)

$$I = I_S\left(e^{V/V_T} - 1\right)$$

$$\ln\left(\frac{I}{I_S} + 1\right) = \ln e^{V/V_T}$$

$$V = V_T \ln\left(\frac{I}{I_S} + 1\right)$$

$$V_{fb} := V_T \cdot ln\left(\frac{0.1\text{mA}}{I_S} + 1\right) = 604.613\text{mV}$$

Example 3.6 (c)

For the *pn* junction considered in Example 3.5 for which $N_A = 10^{18}/\text{cm}^3$, $N_D = 10^{16}/\text{cm}^3$, $A = 10^{-4}\ \text{cm}^2$, $n_i = 1.5 \times 10^{10}/\text{cm}^3$, let $L_p = 5\ \mu\text{m}$, $L_n = 10\ \mu\text{m}$, D_p (in the *n* region) = 10 cm²/s, and D_n (in the *p* region) = 18 cm²/s. The *pn* junction is forward biased and conducting a current $I = 0.1$ mA. Calculate (a) I_S; (b) the forward-bias voltage *V*; and (c) the component of the current due to hole injection and that due to electron injection across the junction.

(c)

$$I_p := Area \cdot q \cdot \frac{D_p}{L_p} \cdot \frac{{n_i}^2}{N_D} \cdot \left(e^{\frac{V_{fb}}{V_T}} - 1 \right) = 99.108 \cdot \mu A$$

$$I_n := Area \cdot q \cdot \frac{D_n}{L_n} \cdot \frac{{n_i}^2}{N_A} \cdot \left(e^{\frac{V_{fb}}{V_T}} - 1 \right) = 0.892 \cdot \mu A$$

Reverse Breakdown

When $V = V_Z$ we have a phenomenon known as junction breakdown.

There are two possible mechanisms for *pn* junction breakdown:

1. zener effect.
   (breakdown voltage $V_Z < 5$ V)
2. avalanche effect.
   (breakdown voltage $V_Z > 7$ V)

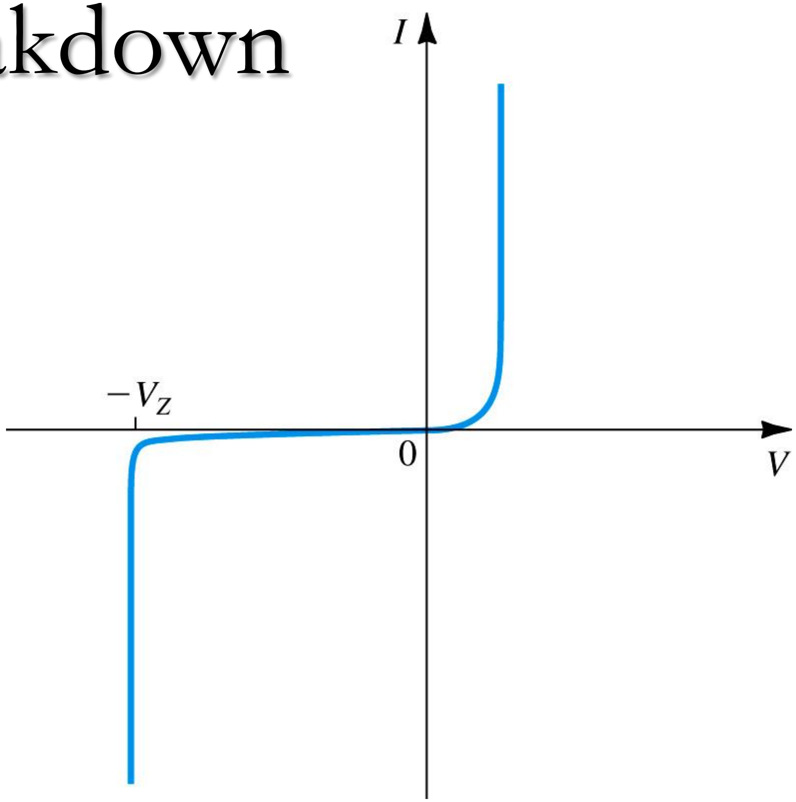


Figure 3.14 The *I-V* characteristic of the *pn* junction showing the rapid increase in reverse current in the breakdown region.

Reverse Breakdown

Zener breakdown occurs when the electric field in the depletion layer increases to the point of breaking covalent bonds and generating electron-hole pairs. The electrons generated in this way will be swept by the electric field into the *n* side and the holes into the *p* side. Thus these electrons and holes constitute a reverse current across the junction. Once the **zener effect** starts, a large number of carriers can be generated, with a negligible increase in the junction voltage.

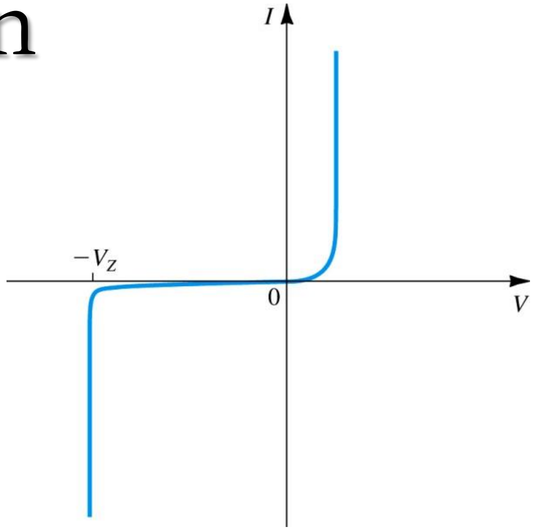


Figure 3.14 The *I*-*V* characteristic of the *pn* junction showing the rapid increase in reverse current in the breakdown region.

Avalanche breakdown occurs when the minority carriers that cross the depletion region under the influence of the electric field gain sufficient kinetic energy to be able to break covalent bonds in atoms with which they collide. The carriers liberated by this process may have sufficiently high energy to be able to cause other carriers to be liberated in another ionizing collision. This process keeps repeating in the fashion of an avalanche, with the result that many carriers are created that are able to support any value of reverse current, as determined by the external circuit, with a negligible change in the voltage drop across the junction.

Zener Diodes

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Features

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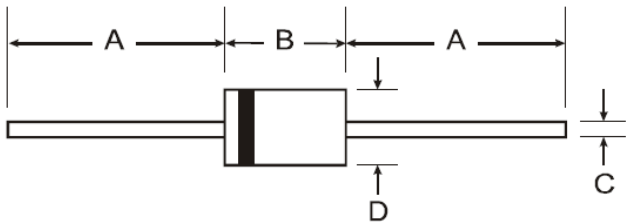


Mechanical Data

- Case: DO-41
- Case Material: Glass. UL Flammability Classification Rating 94V-0
- Terminals: Finish — Sn96.5Ag3.5. Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Marking: Type Number
- Weight: 0.35 grams (approximate)

DO-41 Glass		
Dim	**Min**	**Max**
A	26.0	—
B	—	4.10
C	—	0.86
D	—	2.60
All Dimensions in mm		

3.6 CAPACITIVE EFFECTS IN THE *pn* JUNCTION

Charge Storage in the *pn* Junction

There are two charge storage mechanisms in the *pn* junction.

1. Depletion or Junction Capacitance
   - Related to the charge stored in the depletion region
   - easy to see when the *pn* junction is **reverse biased**.

2. Diffusion Capacitance.
   - Charge associated with the minority carrier charge stored in the depletion region.
   - result of the carrier concentration profiles established by the carrier injection and only in effect when the junction is **forward biased.**

1) Depletion or Junction Capacitance

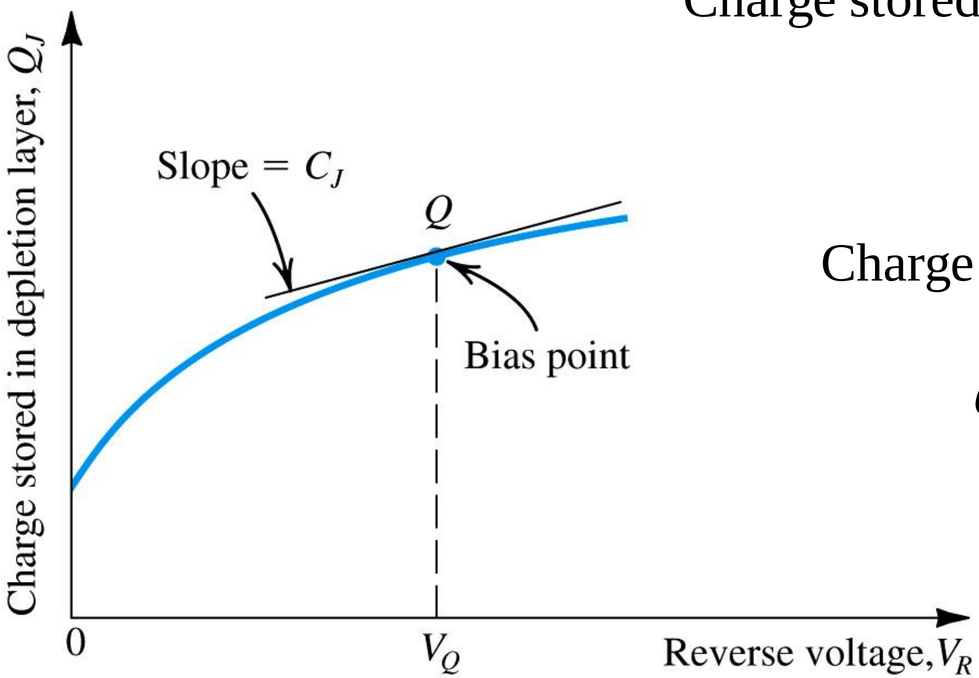


Figure 3.15 The charge stored on either side of the depletion layer as a function of the reverse voltage V_R.

Charge stored on either side of the depletion region

$$Q_J = A\sqrt{2\varepsilon_S q\left(\frac{1}{N_A}+\frac{1}{N_D}\right)V_0}$$

Charge stored on when reverse biased by V_R

$$Q_J = A\sqrt{2\varepsilon_S q\left(\frac{N_A N_D}{N_A+N_D}\right)(V_0+V_R)}$$

Define: $$\alpha = A\sqrt{2\varepsilon_S q\left(\frac{N_A N_D}{N_A+N_D}\right)}$$

$$Q_J = \alpha\sqrt{V_0+V_R}$$

1) Depletion or Junction Capacitance

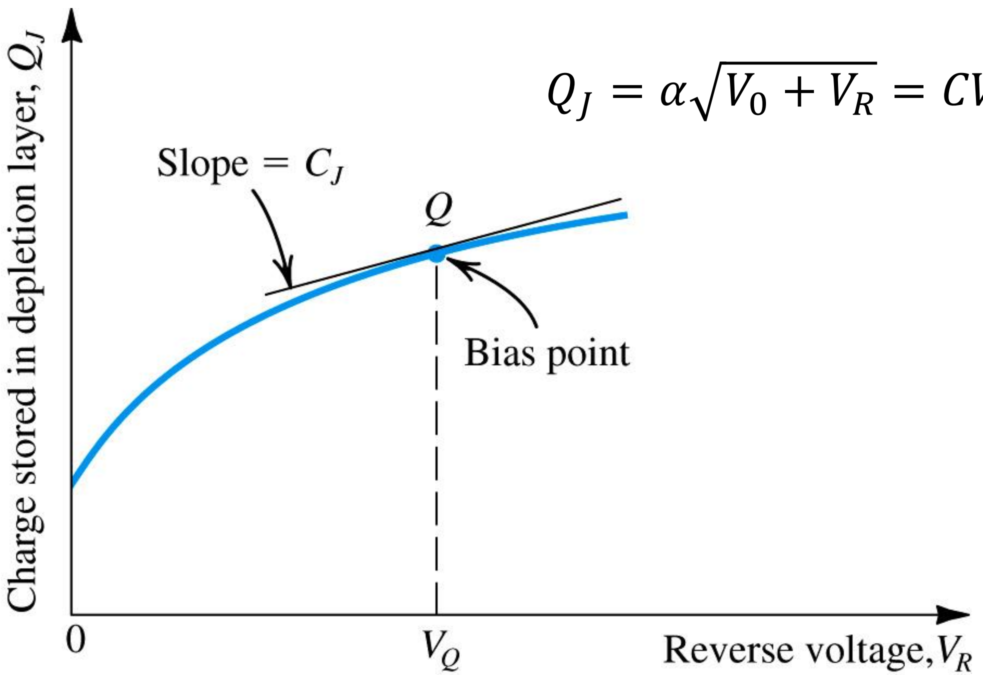


Figure 3.15 The charge stored on either side of the depletion layer as a function of the reverse voltage V_R.

$$Q_J = \alpha\sqrt{V_0 + V_R} = CV$$

$$C_j = \left.\frac{dQ_J}{dV_R}\right]_{V_R=V_Q}$$

$$C_j = \frac{\alpha}{2\sqrt{V_0 + V_R}}$$

Capacitance at 0V reverse biased (V_R =0)

$$C_{j0} = \frac{\alpha}{2\sqrt{V_0}} = A\sqrt{\left(\frac{\varepsilon_S q}{2}\right)\left(\frac{N_A N_D}{N_A+N_D}\right)\left(\frac{1}{V_0}\right)}$$

Then: $$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}}$$

1) Depletion or Junction Capacitance

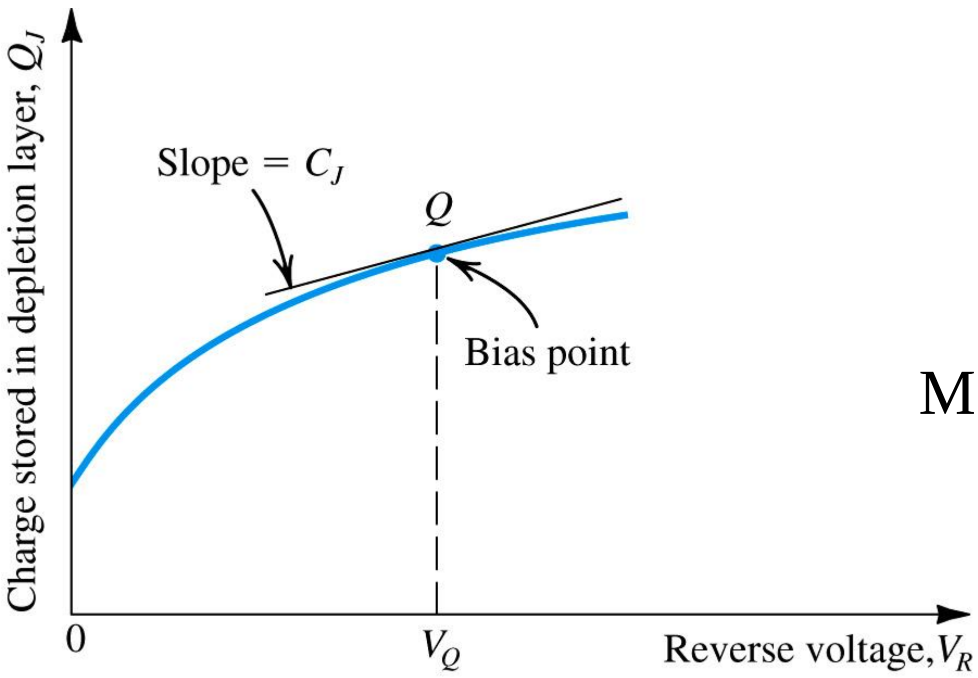


Figure 3.15 The charge stored on either side of the depletion layer as a function of the reverse voltage V_R.

Capacitance for an **abrupt junction**

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}}$$

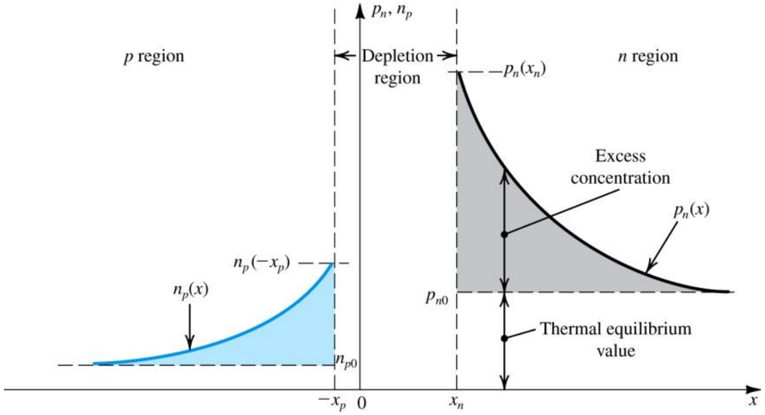
More generally, capacitance for an **graded junction** is given by:

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{V_0}\right)^m}$$

Where m is known as the **grading coefficient** which typically is in the range of 1/3 to 1/2.

2) Diffusion Capacitance

Forward bias minority carrier distributions



$Q_p = Aq \times$ shaded area under the $p_n(x)$curve

$$Q_p = Aq[p_n(x) - p_{n0}]L_p$$

using $\quad p_n(x_n) = p_{n0}e^{V/V_T}$

and $\quad J_p(x_n) = q\left(\frac{D_p}{L_p}\right)p_{n0}\left(e^{V/V_T} - 1\right)$

$$Q_p = \frac{{L_p}^2}{D_p} I_p = \tau_p I_p$$

where $\quad \tau_p = \frac{{L_p}^2}{D_p}$ is known as the **minority carrier (hole) lifetime** and is the average time it takes for a hole injected into the *n* region to recombine with a majority electron.

2) Diffusion Capacitance

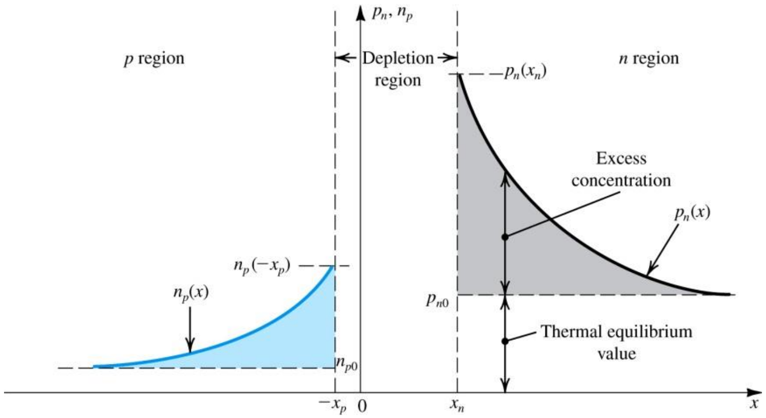
Forward bias minority carrier distributions

$Q_n = Aq \times$ shaded area under the $n_p(x)$curve

$Q_n = Aq\left[n_p(x) - n_{p0}\right]L_p$

using $n_p(x_n) = n_{p0}e^{V/V_T}$

and $J_n(-x_p) = q\left(\frac{D_n}{L_n}\right)n_{p0}\left(e^{V/V_T} - 1\right)$



$Q_n = \frac{{L_n}^2}{D_n} I_n = \tau_n I_n$ where $\tau_n = \frac{{L_n}^2}{D_n}$

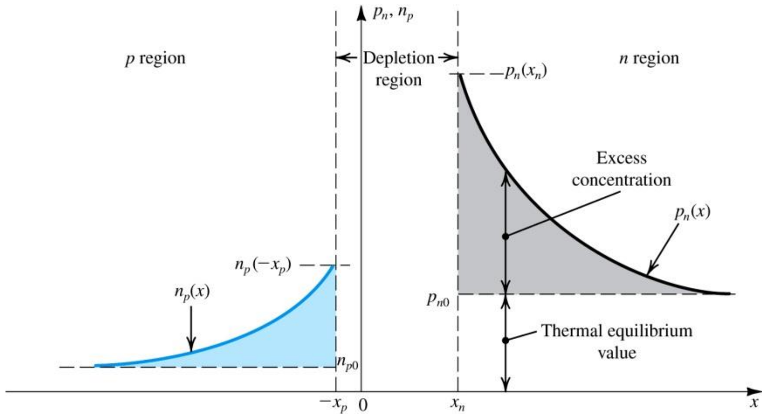
is known as the **minority carrier (electron) lifetime** and is the average time it takes for an electron injected into the *p* region to recombine with a majority hole.

2) Diffusion Capacitance

The total excess minority charge

$$Q = Q_p + Q_n = \tau_p I_p + \tau_n I_n$$

$Q = \tau_T I$ where τ_T is called the **mean transit time** of the junction.



In most practical devices, one side of the junction is much more heavily doped than the other.

If $N_A >> N_D$

$I_p \gg I_n$ $\qquad I \simeq I_p$

$Q_p \gg Q_n$ $\qquad Q \simeq Q_p$

$\tau_T \simeq \tau_p$

If $N_D >> N_A$

$I_n \gg I_p$ $\qquad I \simeq I_n$

$Q_n \gg Q_p$ $\qquad Q \simeq Q_n$

$\tau_T \simeq \tau_n$

Incremental Diffusion Capacitance

For small changes around a bias point, we can define an **incremental diffusion capacitance** C_d as:

$$C_d = \frac{dQ}{dV}$$

and can show that

$$C_d = \left(\frac{\tau_T}{V_T}\right) I$$

Note that C_d is directly proportional to the forward current and transit time.

Homework #6

- Finish reading Chapter 3
- Chapter 3 Problems:
  - 3.12*
  - 3.13
  - 3.17
  - 3.21
  - 3.24*

* Answers in Appendix L

Summary of Important Equations pp. 169 - 170

Quantity	Relationship	Values of Constants and Parameters (for intrinsic Si at T = 300 K)
Carrier concentration in intrinsic silicon (cm^{-3})	$n_i = BT^{3/2}e^{-E_g/2kT}$	B = 7.3 E15 $cm^{-3}K^{-3/2}$ E_g = 1.12 eV k = 8.62 E-5 eV/K n_i = 1.5 E10 /cm^3
Diffusion current density (A/cm^2)	$J_p = qD_p \frac{dp}{dx}$ $J_n = qD_n \frac{dn}{dx}$	q = 1.60 E-19 coloumb D_p = 12 cm^2/s D_n = 34 cm^2/s
Drift current density (A/cm^2)	$J_{drift} = q(p\mu_p + n\mu_n)\mathrm{E}$	μ_p = 480 $cm^2/(V{\cdot}s)$ μ_n = 1350 $cm^2/(V{\cdot}s)$
Resistivity ($\Omega{\cdot}cm$)	$\rho = 1 / [q(p\mu_p + n\mu_n)]$	μ_p and μ_n decrease with the increase in doping concentration
Relationship between mobility and diffusivity	$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T$	$V_T = kT/q$ ~ 25.9 mV

Summary of Important Equations cont. pp. 169 - 170

Quantity	Relationship	Values of Constants and Parameters (for intrinsic Si at T = 300 K)
Carrier concentration in *n*-type silicon (cm^{-3})	$n_{n0} \simeq N_D$ $p_{n0} = n_i^2/N_D$	
Carrier concentration in *p*-type silicon (cm^{-3})	$p_{p0} \simeq N_A$ $n_{p0} = n_i^2/N_A$	
Junction built-in voltage (V)	$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$	
Width of depletion region (cm)	$\frac{x_n}{x_p} = \frac{N_A}{N_D}$ $W = x_n + x_p$ $W = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$	$\varepsilon_S = 11.7\varepsilon_0$ $\varepsilon_0 = 8.854$ E-14 F/cm
Charge stored in depletion layer (coulomb)	$Q_J = q\frac{N_A N_D}{N_A + N_D}AW$	

Summary of Important Equations cont. pp. 169 - 170

Quantity	Relationship	Values of Constants and Parameters (for intrinsic Si at T = 300 K)
Forward current (A)	$I = I_p + I_n$ $I_n = Aqn_i^2 \dfrac{D_p}{L_p N_D}\left(e^{V/V_T} - 1\right)$ $I_p = Aqn_i^2 \dfrac{D_n}{L_n N_A}\left(e^{V/V_T} - 1\right)$	
Saturation current (A)	$I_S = Aqn_i^2 \left(\dfrac{D_p}{L_p N_D} + \dfrac{D_n}{L_n N_A}\right)$	
I-V Relationship	$I = I_S\left(e^{V/V_T} - 1\right)$	
Minority-carrier lifetime (s)	$\tau_p = L_p^2 / D_p$ $\tau_n = L_n^2 / D_n$	L_p, L_n = 1μm to 100 μm τ_p, τ_n = 1ns to 10^4 ns
Minority-carrier charge storage (coulomb)	$Q_p = \tau_p I_p$ $Q_n = \tau_n I_n$ $Q = Q_p + Q_n = \tau_T I$	

Summary of Important Equations cont. pp. 169 - 170

Quantity	Relationship	Values of Constants and Parameters (for intrinsic Si at T = 300 K)
Depletion capacitance (F)	$C_{j0} = A\sqrt{\left(\frac{\varepsilon_S q}{2}\right)\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\frac{1}{V_0}\right)}$ $C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{V_0}\right)^m}$	m = 1/3 to 1/2
Diffusion capacitance (F)	$C_d = \left(\frac{\tau_T}{V_T}\right) I$	

Summary

- Today's microelectronics technology is almost entirely based on the semiconductor silicon. If a circuit is to be fabricated as a monolithic integrated circuit (IC), it is made using a single silicon crystal, no matter how large the circuit is.
- In a crystal of intrinsic or pure silicon, the atoms are held in position by covalent bonds. At very low temperatures, all the bonds are intact; No charge carriers are available to conduct current. As such, at these low temperatures, silicone acts as an insulator.
- At room temperature, thermal energy causes some of the covalent bonds to break, thus generating free electrons and holes that become available to conduct electricity.
- Current in semiconductors is carried by free electrons and holes. Their numbers are equal and relatively small in intrinsic silicon.

Summary Continued

- The conductivity of silicon may be increased drastically by introducing small amounts of appropriate impurity materials into the silicon crystal – via process called doping.
- There are two kinds of doped semiconductor: *n*-type in which electrons are abundant, *p*-type in which holes are abundant.
- There are two mechanisms for the transport of charge carriers in a semiconductor: drift and diffusion.
- Carrier drift results when an electric field (E) is applied across a piece of silicon. The electric field accelerates the holes in the direction of E and electrons oppositely. These two currents sum to produce drift current in the direction of E.

Summary Continued

- Carrier diffusion occurs when the concentration of charge carriers is made higher in one part of a silicon crystal than others. To establish a steady-state diffusion current, a carrier concentration must be maintained in the silicon crystal.
- A basic semiconductor structure is the *pn*-junction. It is fabricated in a silicon crystal by creating a *p*-region in proximity to an *n*-region. The *pn*-junction is a diode and plays a dominant role in the structure and operation of transistors.

Summary Continued

- When the terminals of the *pn*-junction are left open, no current flows externally. However, two equal and opposite currents (I_D and I_S) flow across the junction. Equilibrium is maintained by a built-in voltage (V_0). Note, however, that the voltage across an open junction is 0V, since V_0 is cancelled by potentials appearing at the metal-to-semiconductor connection interfaces.
- The voltage V_0 appears across the depletion region, which extends on both sides of the junction.
- The drift current I_S is carried by thermally generated minority electrons in the *p*-material that are swept across the depletion region into the n-side. The opposite occurs in the *n*-material. I_S flows from *n* to *p*, in the reverse direction of the junction. Its value is a strong function of temperature, but independent of V_0.

Summary Continued

- Forward biasing of the *pn*-junction, that is applying an external voltage that makes *p* more positive than *n*, reduces the barrier voltage to V_0 - V and results in an exponential increase in I_D (while I_S remains unchanged).
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- Forward biasing of the *pn*-junction, that is applying an external voltage that makes *p* more positive than *n*, reduces the barrier voltage to V_0 - V and results in an exponential increase in I_D (while I_S remains unchanged).