

Lecture 7: DC & Transient Response

Assignment for 9/19

- Continue working on Lab 3
- Prepare for quiz on Thursday (covers lecture 5)
- Text book reading sections 2.5, 4.1-4.3

Outline

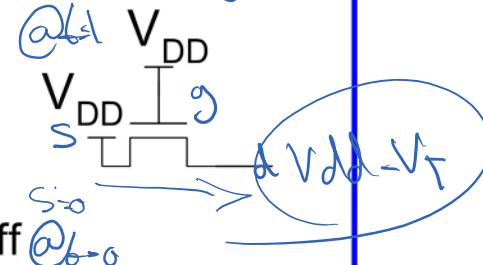
- Pass Transistors
- DC Response
- Logic Levels and Noise Margins
- Transient Response
- RC Delay Models
- Delay Estimation

$$V_{DD} = 5V \quad V_{Tn} = 0.7V$$

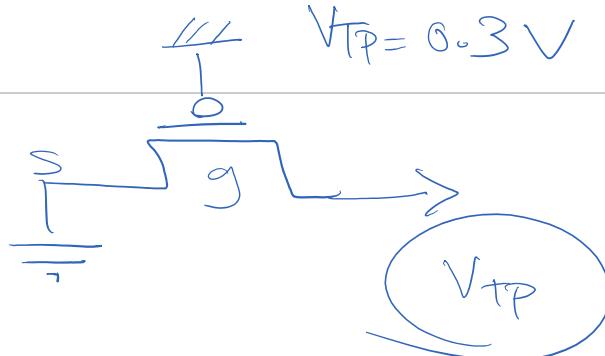
$$V_{DD} > V_T$$

Pass Transistors

- We have assumed source is grounded
- What if source > 0?
 - e.g. pass transistor passing V_{DD}
- $V_g = V_{DD}$
 - If $V_s > V_{DD} - V_t$, $V_{gs} < V_t$
 - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD} - V_{tn}$
 - Called a degraded “1”
 - Approach degraded value slowly (low I_{ds})
- pMOS pass transistors pull no lower than V_{tp}
- Transmission gates are needed to pass both 0 and 1

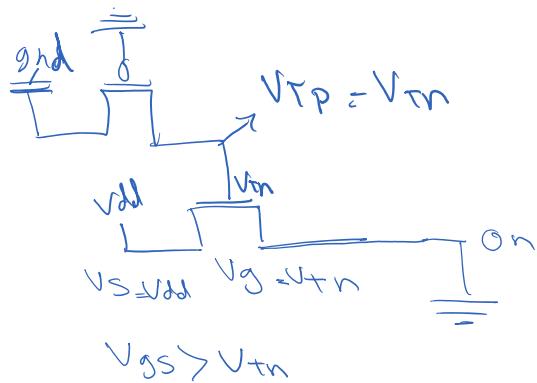
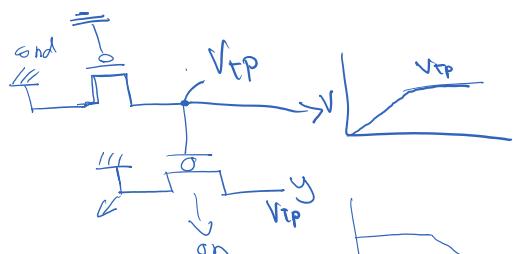
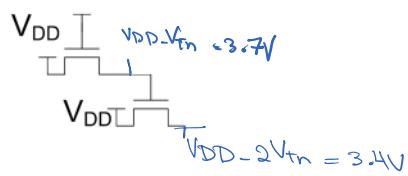
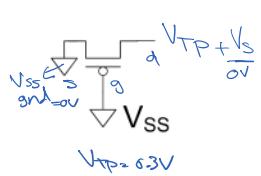
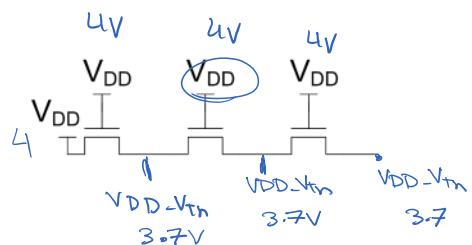
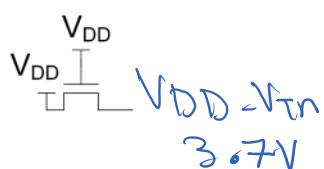


$$V_{TP} = 0.3V$$



$$V_{DD} = 4V \quad V_{TP} = 0.3V \quad V_{TN} = 0.3V$$

Pass Transistor Ckts



DC Response

- DC Response: V_{out} vs. V_{in} for a gate

- Ex: Inverter

- When $V_{in} = 0$ $\rightarrow V_{out} = V_{DD}$

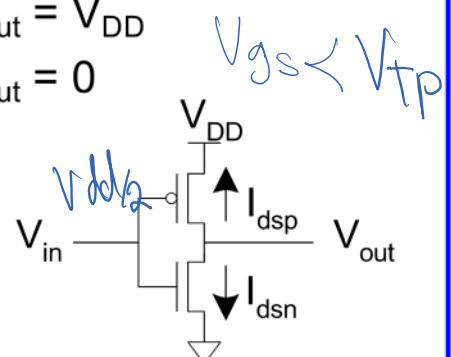
- When $V_{in} = V_{DD}$ $\rightarrow V_{out} = 0$

- In between, V_{out} depends on transistor size and current

- By KCL, must settle such that $I_{dsn} = |I_{dsp}|$

- We could solve equations

- But graphical solution gives more insight



$$V_{in} > V_{gs} - V_T$$

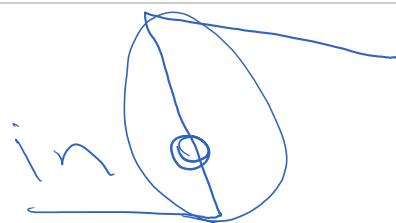
$$\textcircled{V} = IR$$

$P_{mos} = 0$

$n_{mos} = 0$

$P_{mos} = Sat$

$n_{mos} = Sat$



Transistor Operation

- Current depends on region of transistor behavior
- For what V_{in} and V_{out} are nMOS and pMOS in
 - Cutoff?
 - Linear?
 - Saturation?

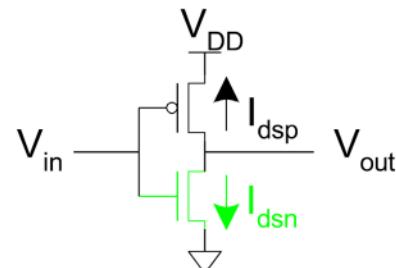
nMOS Operation

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{dsn} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{dsn} > V_{in} - V_{tn}$

$$V_g \approx V_{in}$$

$$V_s = 0$$

$$V_{gs} = V_{in} - \sigma = V_{in}$$



pMOS Operation

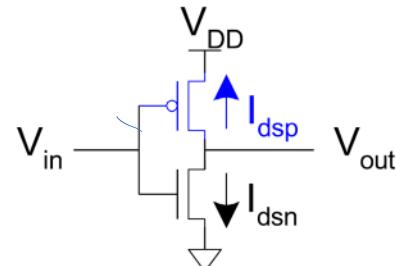
Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
$V_{in} > V_{DD} + V_{tp}$	$V_{in} < V_{DD} + V_{tp}$	$V_{in} < V_{DD} + V_{tp}$
$\sqrt{S} \approx \sqrt{V_{dd}}$	$V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

$$\sqrt{S} \approx \sqrt{V_{dd}}$$

$$V_{gsp} = V_{in} - V_{DD}$$

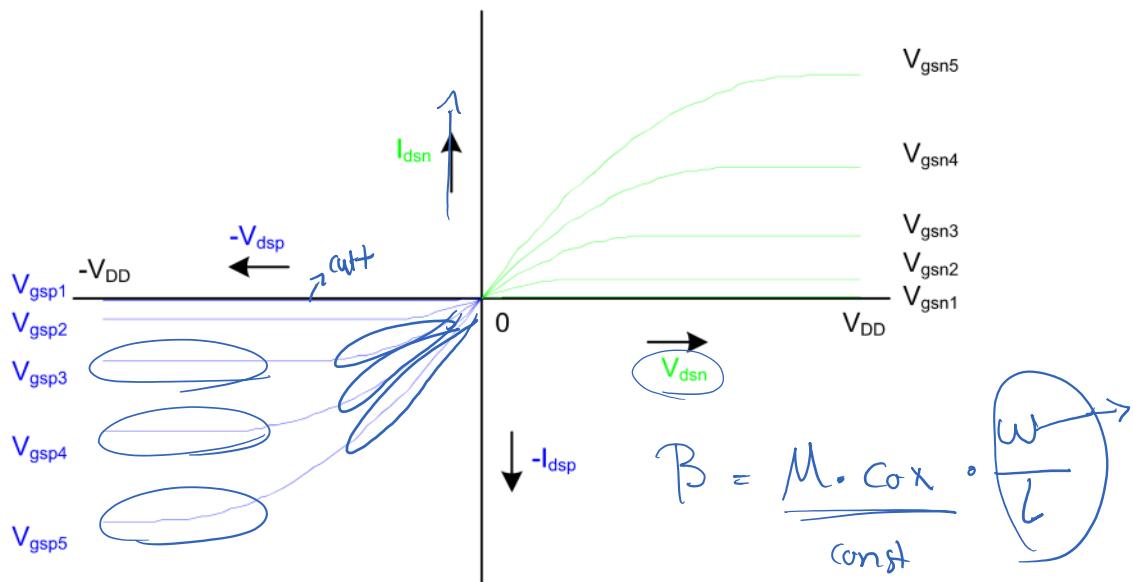
$$V_{tp} < 0$$

$$V_{dsp} = V_{out} - V_{DD}$$



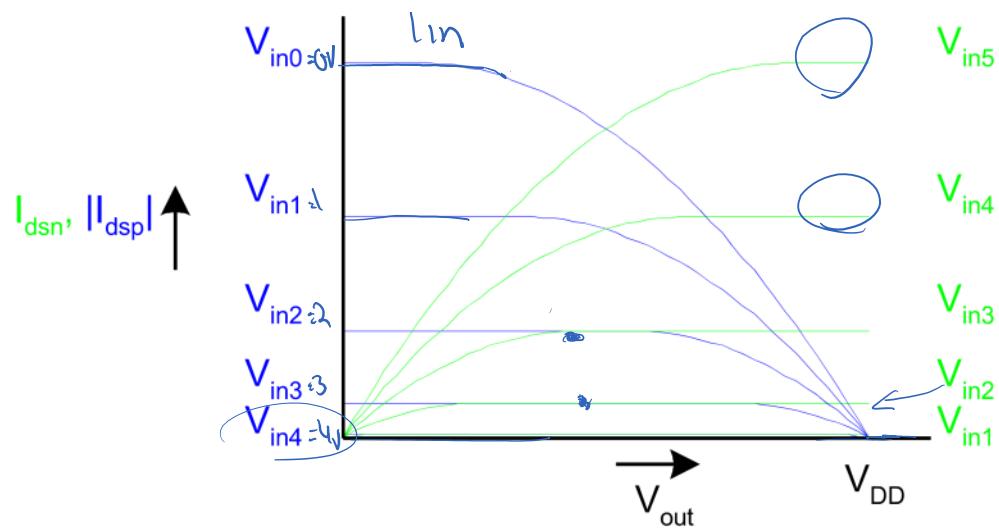
I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$



$$\beta_n \approx \beta_p$$

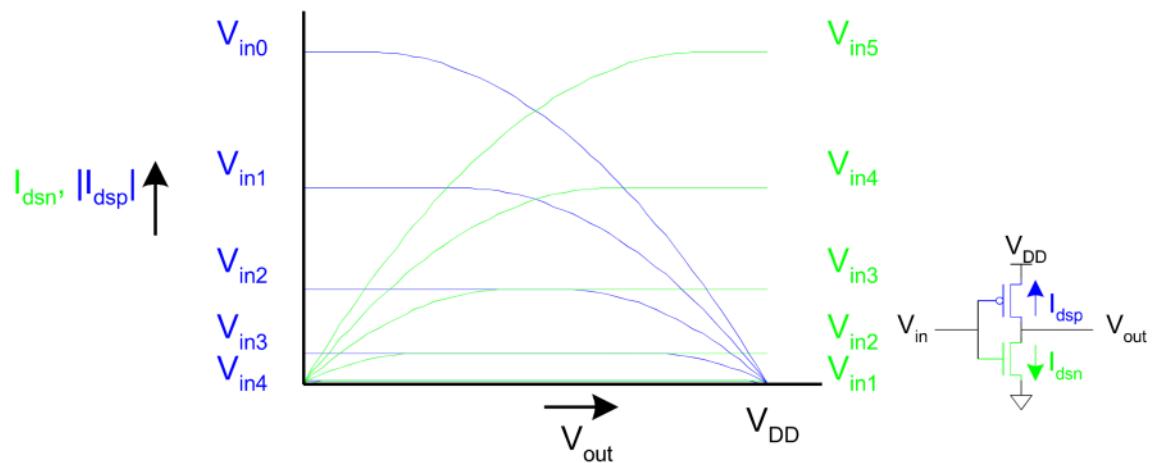
Current vs. V_{out} , V_{in}



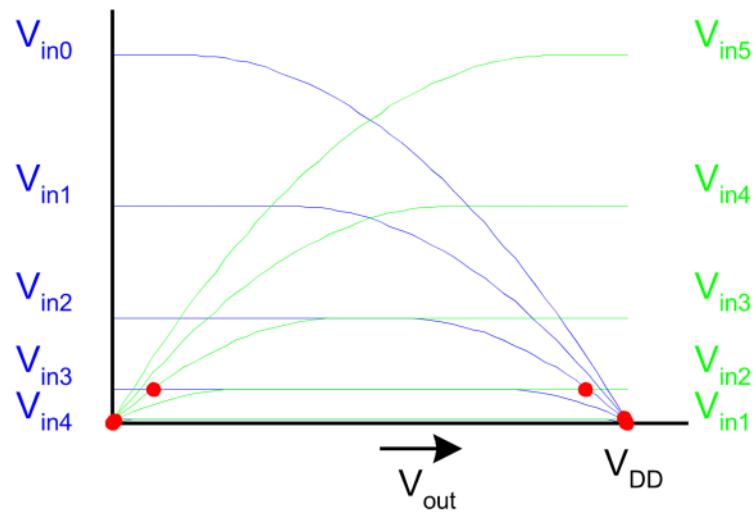
Load Line Analysis

□ For a given V_{in} :

- Plot I_{dsn} , $|I_{dsp}|$ vs. V_{out}
- V_{out} must be where $|currents|$ are equal in

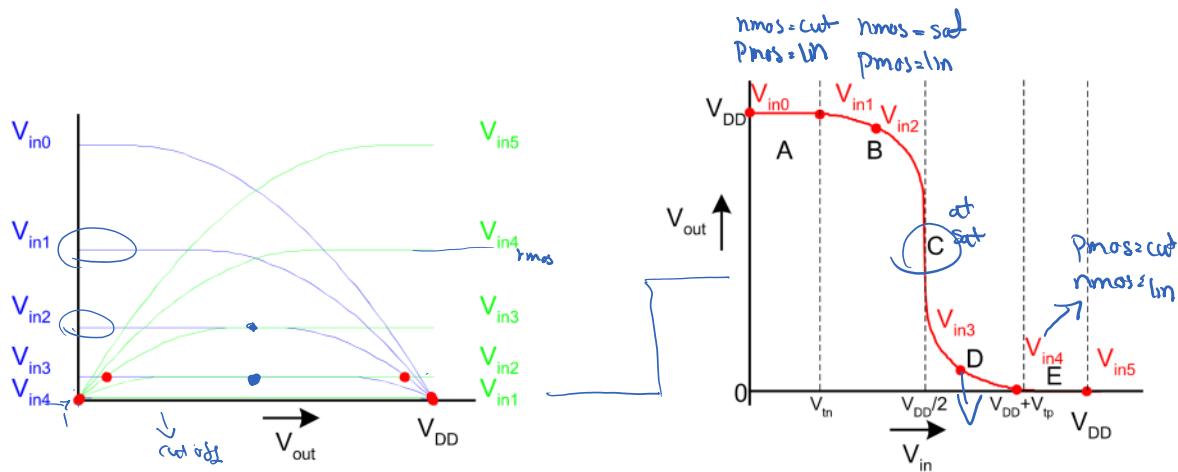


Load Line Analysis



DC Transfer Curve

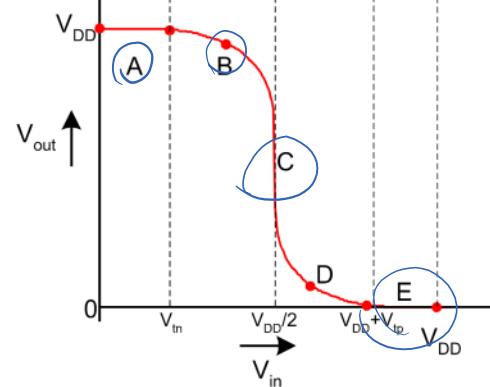
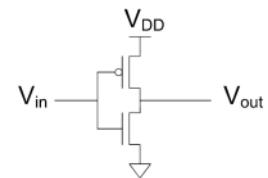
- Transcribe points onto V_{in} vs. V_{out} plot



Operating Regions

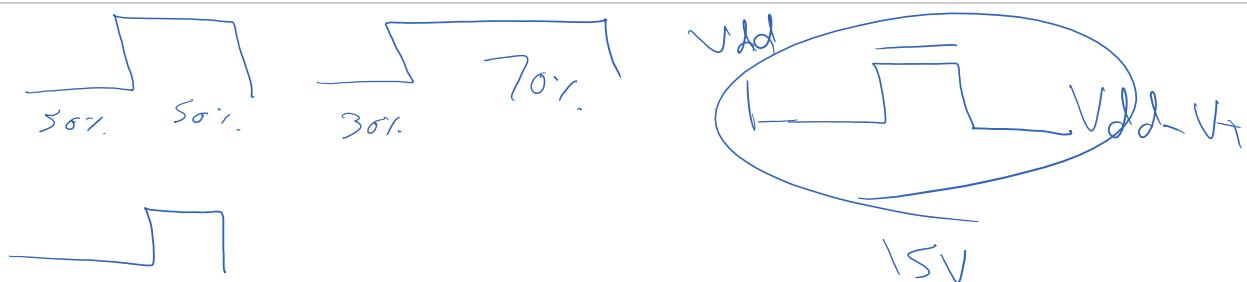
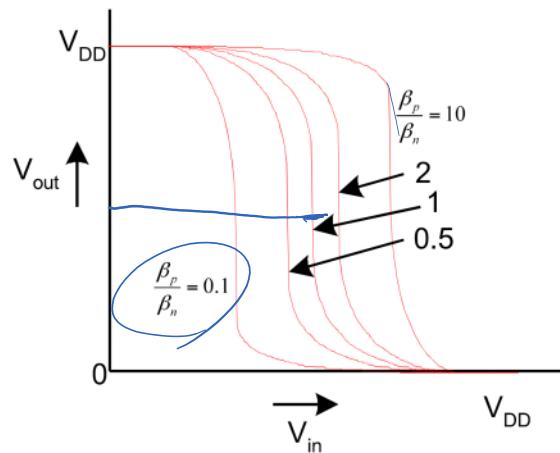
- Revisit transistor operating regions

Region	nMOS	pMOS
A	cut	lin
B	sat	lin
C	sat	sat
D	lin	sat
E	lin	cut



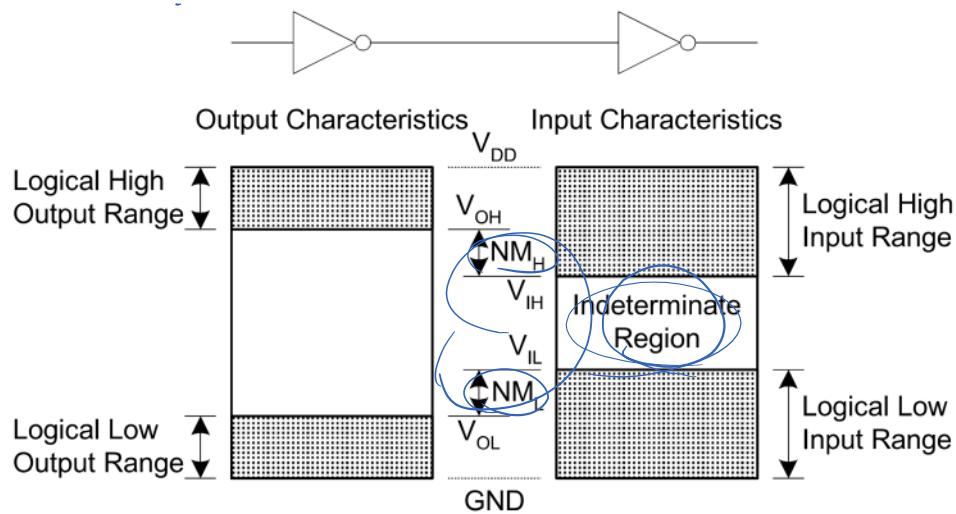
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed gate*
- Other gates: collapse into equivalent inverter



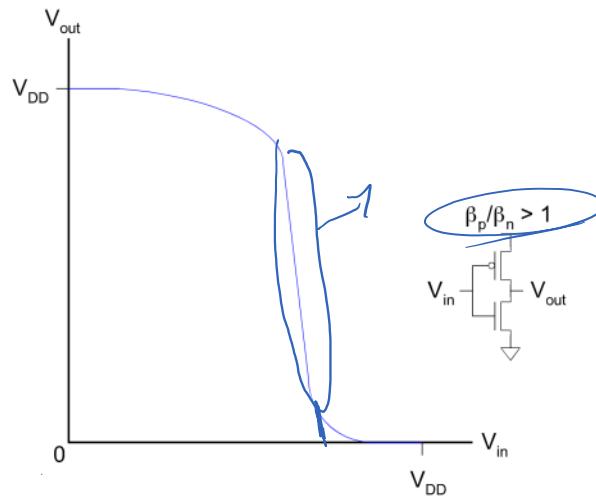
Noise Margins

- ❑ How much noise can a gate input see before it does not recognize the input?



Logic Levels

- To maximize noise margins, select logic levels at
 - unity gain point of DC transfer characteristic

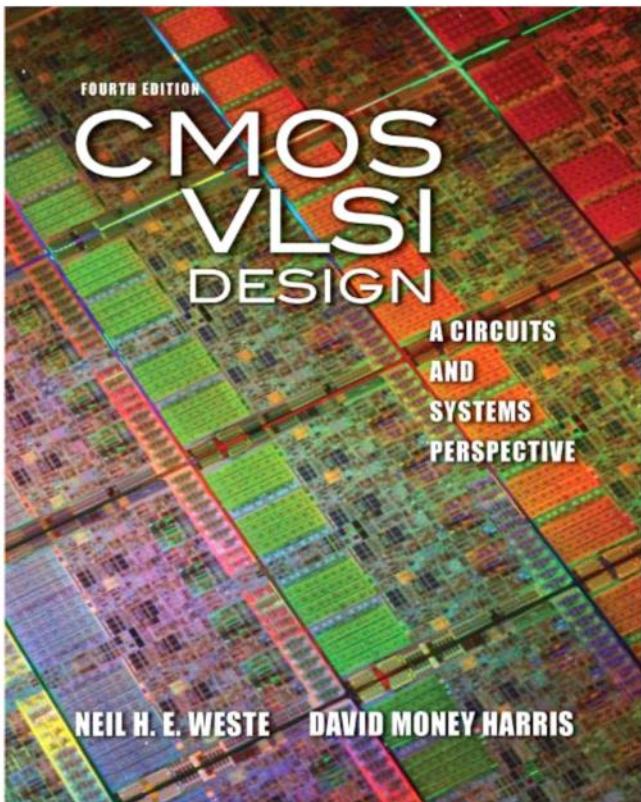


Transient Response

- DC analysis tells us V_{out} if V_{in} is constant
- Transient analysis tells us $V_{out}(t)$ if $V_{in}(t)$ changes
 - Requires solving differential equations
- Input is usually considered to be a step or ramp
 - From 0 to V_{DD} or vice versa

Lecture 8

Wednesday, September 18, 2019 9:12 PM



Lecture 8: DC & Transient Response

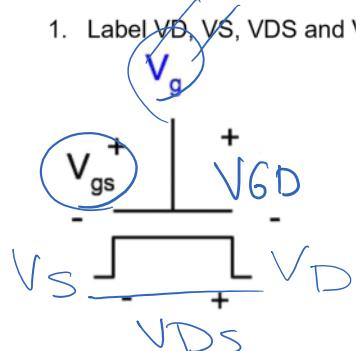
Assignments

Wednesday, September 18, 2019 9:13 PM

Assignment for 9/24

- Lab 4 is due 9/26
- Prepare for quiz on Tuesday (covers lecture 7&8)
- Text book reading sections 2.5, 4.1e 4.3

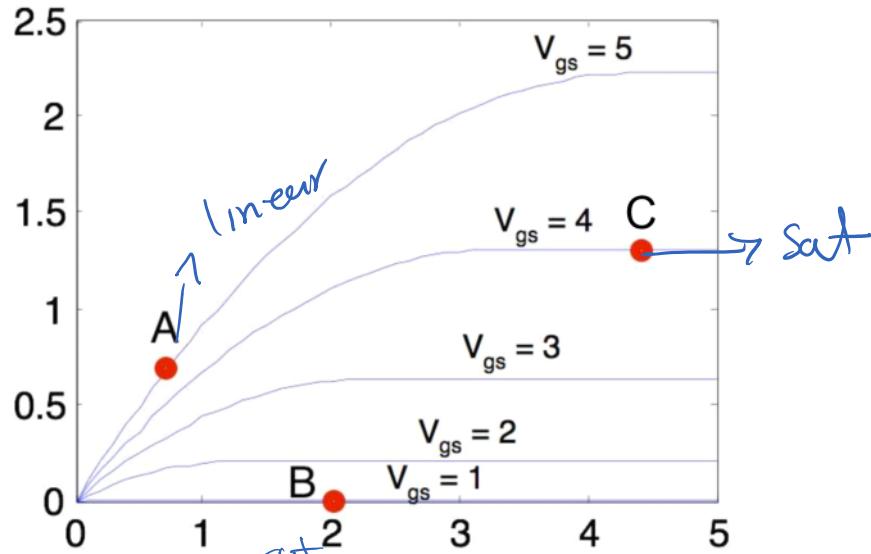
1. Label V_D , V_S , V_{DS} and V_{GD} .



2. For equation below, fill in the box. Also label equation as **cutoff**, **linear** and **saturation**.

$$I_{ds} = \begin{cases} 0 & V_{gs} \square V_t \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} \square V_{dsat} \text{ lin} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} \square V_{dsat} \text{ sat} \end{cases}$$

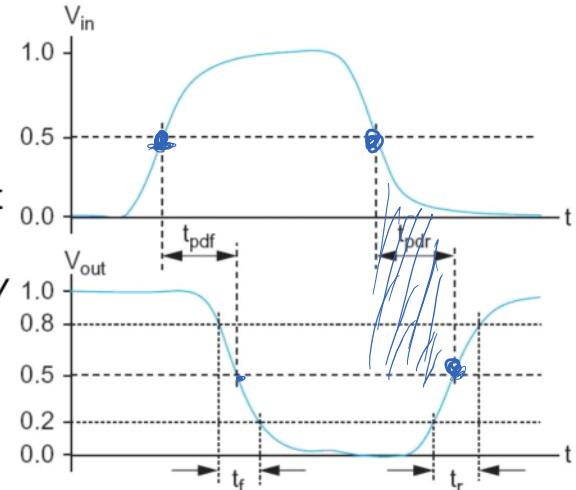
3. Label X and Y axis. Label points A,B and C as being in **cutoff**, **linear** or **saturation**.



4. Why do we typically make PMOS 2X wider than NMOS in CMOS inverters?

Delay Definitions

- t_{pdr} : rising propagation delay**
 - From input to rising output crossing $V_{DD}/2$
- t_{pdf} : falling propagation delay**
 - From input to falling output crossing $V_{DD}/2$
- t_{pd} : average propagation delay**
 - $t_{pd} = (t_{pdr} + t_{pdf})/2$
- t_r : rise time**
 - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
- t_f : fall time**
 - From output crossing 0.8 V_{DD} to 0.2 V_{DD}

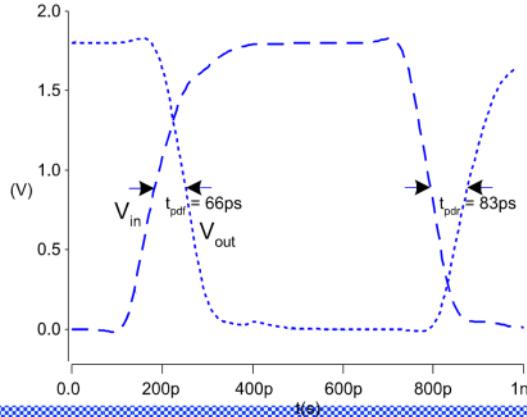


Delay Definitions

- t_{cdr} : *rising contamination delay*
 - From input to rising output crossing $V_{DD}/2$
- t_{cdf} : *falling contamination delay*
 - From input to falling output crossing $V_{DD}/2$
- t_{cd} : *average contamination delay*
 - $t_{pd} = (t_{cdr} + t_{cdf})/2$

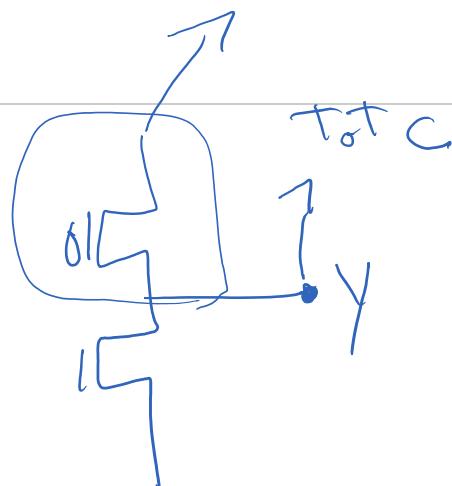
Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
 - Uses more accurate I-V models too!
- But simulations take time to write, may hide insight



Delay Estimation

- We would like to be able to easily estimate delay
 - Not as accurate as simulation
 - But easier to ask “What if?”
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
 - C = total capacitance on output node
 - Use *effective resistance R*
 - So that $t_{pd} = RC$
- Characterize transistors by finding their effective R
 - Depends on average current as gate switches

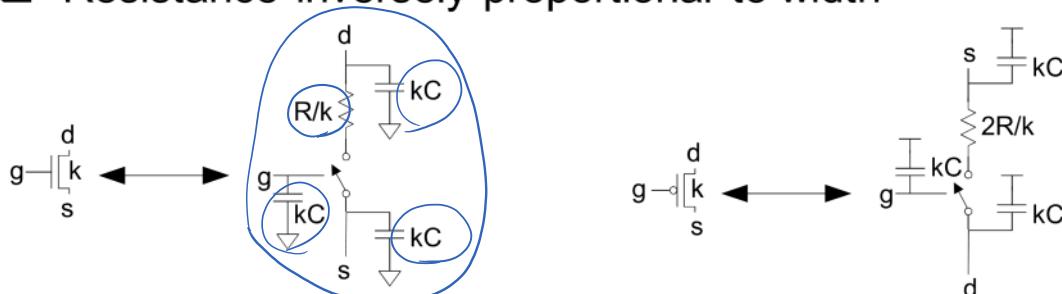


Effective Resistance

- Shockley models have limited value
 - Not accurate enough for modern transistors
 - Too complicated for much hand analysis
- Simplification: treat transistor as resistor
 - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R
 - $I_{ds} = V_{ds}/R$
 - R averaged across switching of digital gate
- Too inaccurate to predict current at any given time
 - But good enough to predict RC delay

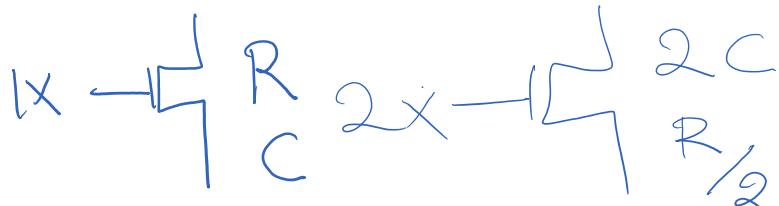
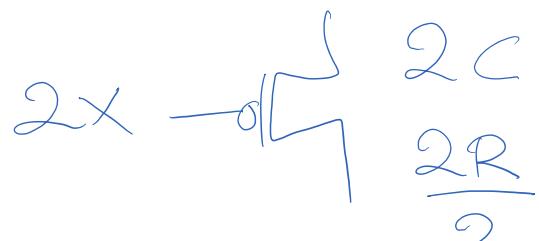
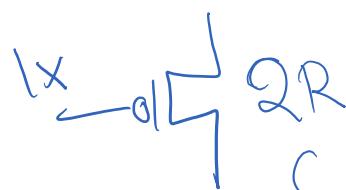
RC Delay Model

- Use equivalent circuits for MOS transistors
 - Ideal switch + capacitance and ON resistance
 - Unit nMOS has resistance R , capacitance C
 - Unit pMOS has resistance $2R$, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width



$$V = IR$$

$$R = \frac{V}{I}$$

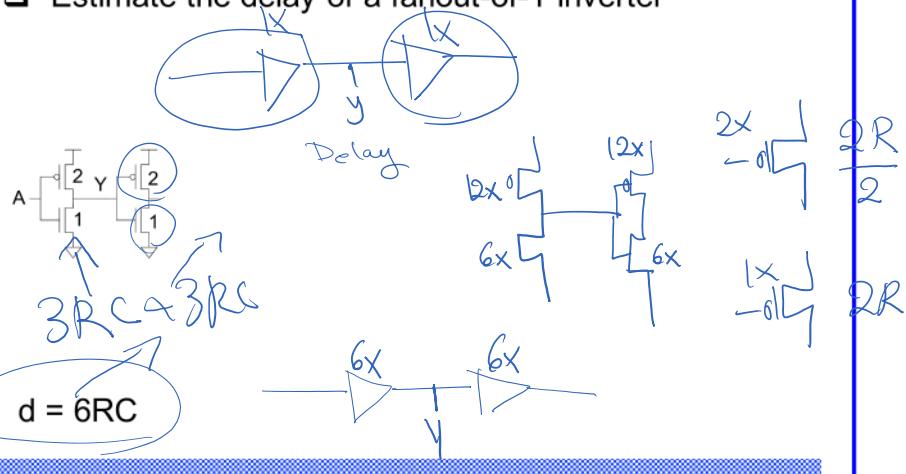


RC Values

- Capacitance
 - $C = C_g = C_s = C_d = 2 \text{ fF}/\mu\text{m}$ of gate width in $0.6 \mu\text{m}$
 - Gradually decline to $1 \text{ fF}/\mu\text{m}$ in 65 nm
- Resistance
 - $R \approx 10 \text{ K}\Omega \cdot \mu\text{m}$ in $0.6 \mu\text{m}$ process
 - Improves with shorter channel lengths
 - $1.25 \text{ K}\Omega \cdot \mu\text{m}$ in 65 nm process
- Unit transistors
 - May refer to minimum contacted device ($4/2 \lambda$)
 - Or maybe $1 \mu\text{m}$ wide device
 - Doesn't matter as long as you are consistent

Inverter Delay Estimate

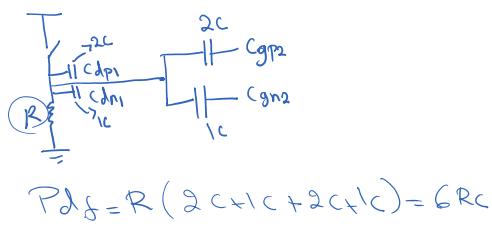
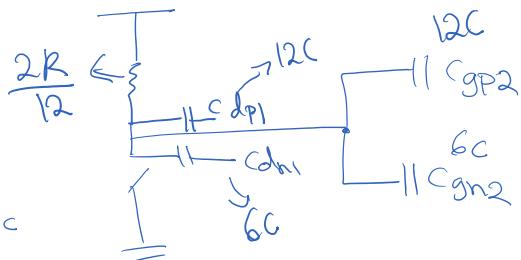
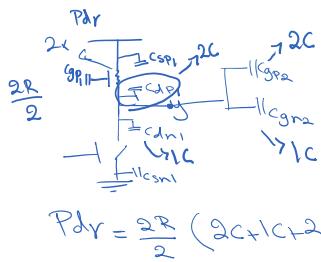
- Estimate the delay of a fanout-of-1 inverter



7: DC and Transient Response

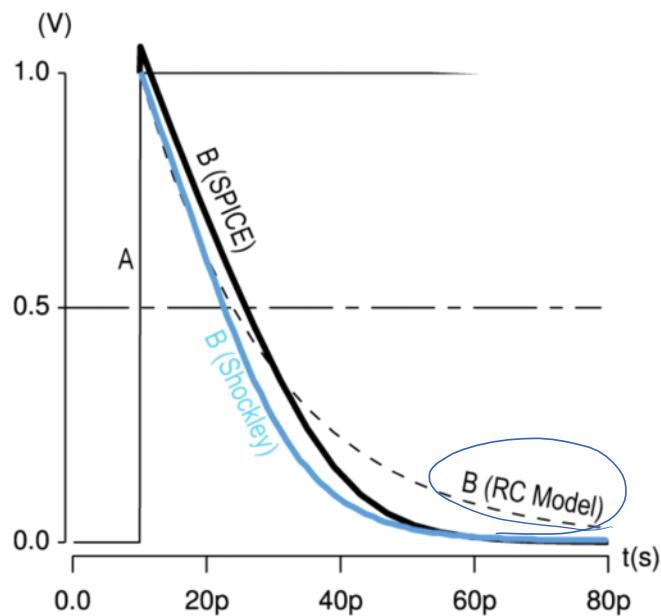
CMOS VLSI Design 4th Ed.

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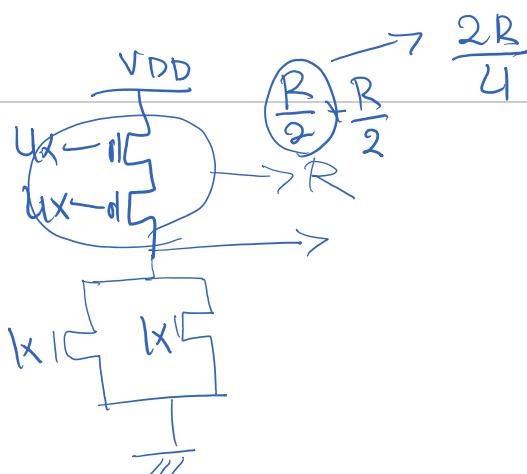
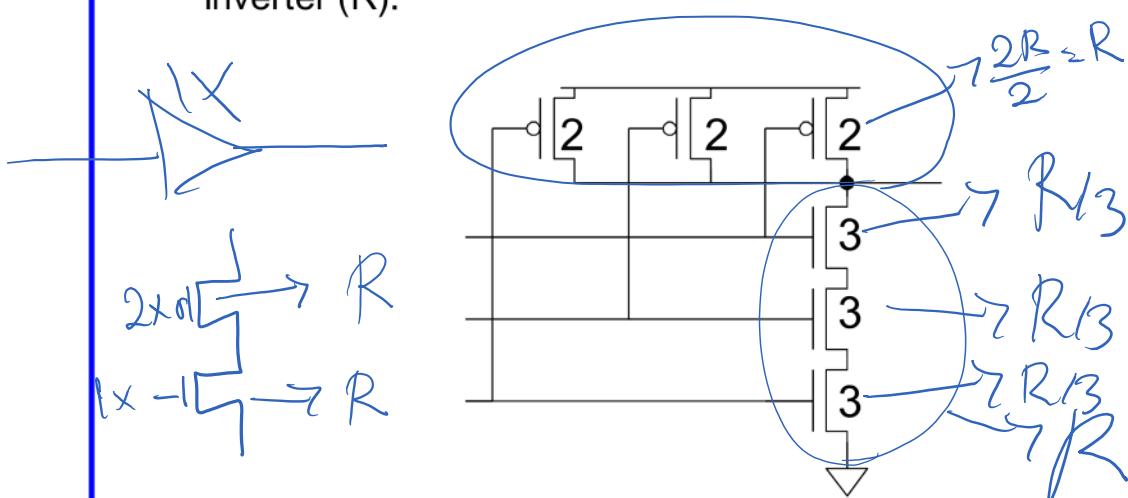
$$P_d = \frac{P_{dr} + P_{df}}{2} = 6RC$$

Delay Model Comparison



Example: 3-input NAND

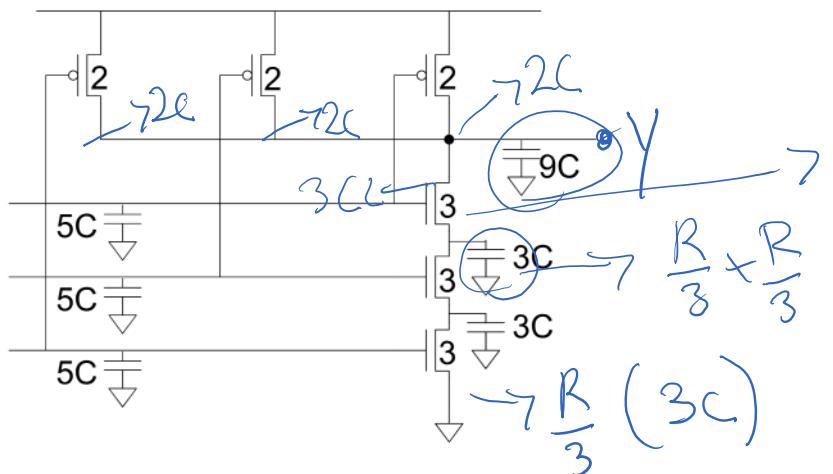
- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



$$\text{Equivalent circuit: } \frac{R}{R+R} = \frac{1}{2} \quad \text{Final result: } R = \frac{1}{\frac{1}{R} + \frac{1}{R}} = \frac{1}{2}R$$

3-input NAND Caps

- Annotate the 3-input NAND gate with gate and diffusion capacitance.

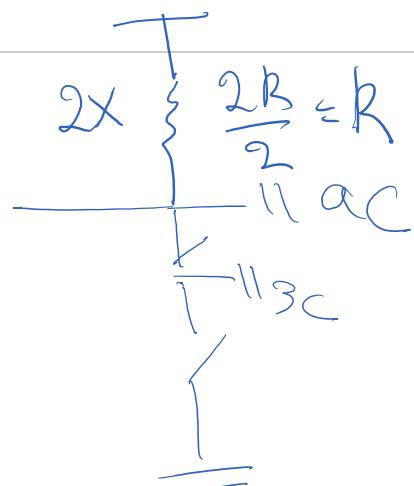
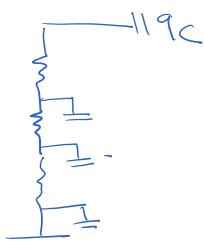


(3C)

(3C)

(3C)

$$t_{PD}\approx qC(R) = qRC$$



$$t_{PD} = \left(\frac{R}{3}(3C) + \frac{2R}{3}(3C) + \frac{3R}{3}(qC) \right)$$

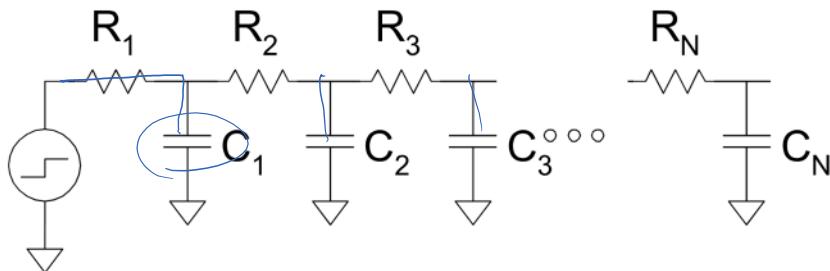
$$RC + 2R + qRC = 12RC$$

$$t_{PD} = \frac{q+12}{2} RC$$

Elmore Delay

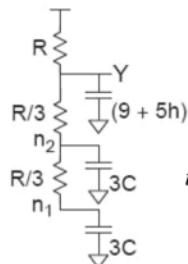
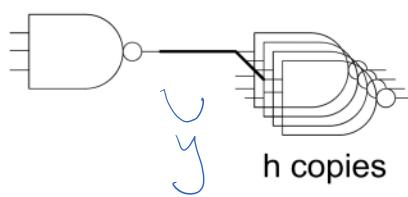
- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-\text{to-source}} C_i$$
$$= R_1 C_1 + (R_1 + R_2) C_2 + \dots + (R_1 + R_2 + \dots + R_N) C_N$$

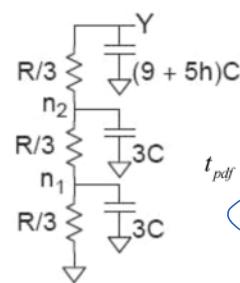
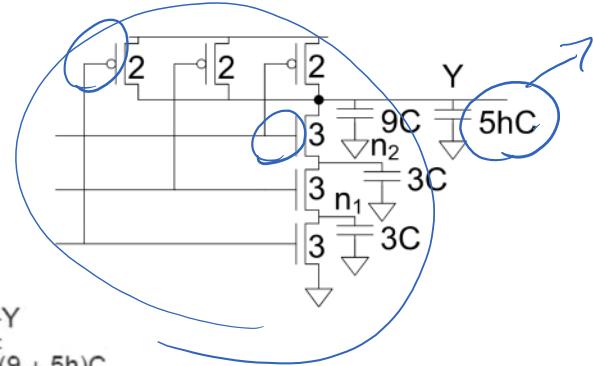


Example: 3-input NAND

- Estimate worst-case rising and falling delay of 3-input NAND driving h identical gates.



$$t_{pd} = (9 + 5h)RC$$



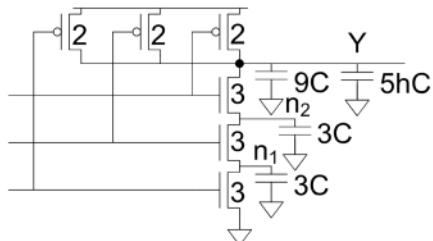
$$\begin{aligned} t_{pdf} &= \left(3C\right)\left(\frac{R}{3}\right) + \left(3C\right)\left(\frac{R}{3} + \frac{R}{3}\right) + \left[(9 + 5h)C\right]\left(\frac{R}{3} + \frac{R}{3} + \frac{R}{3}\right) \\ &= (12 + 5h)RC \end{aligned}$$

Delay Components

- Delay has two parts
 - *Parasitic delay*
 - 9 or 12 RC
 - Independent of load
 - *Effort delay*
 - $5h$ RC
 - Proportional to load capacitance

Contamination Delay

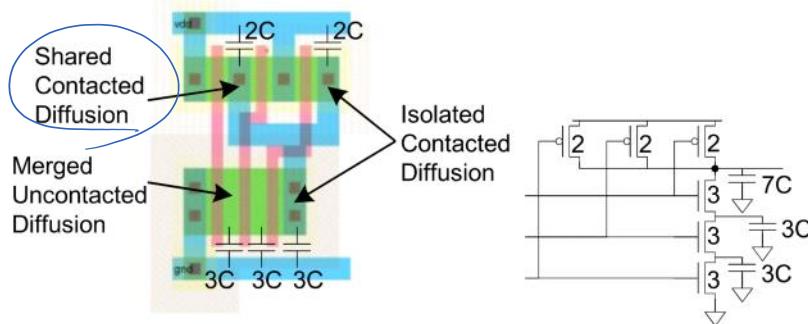
- Best-case (contamination) delay can be substantially less than propagation delay.
- Ex: If all three inputs fall simultaneously



$$t_{cdr} = [(9 + 5h)C] \left(\frac{R}{3} \right) = \left(3 + \frac{5}{3}h \right) RC$$

Diffusion Capacitance

- We assumed contacted diffusion on every s / d.
- Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
 - Reduces output capacitance by $2C$
 - Merged uncontacted diffusion might help too



Layout Comparison

□ Which layout is better?

