CPEG 422/622 Spring 2020

Homework 6

Due May 6th at midnight (through canvas)
Note: The equations to be used are included in the lecture slides. To receive full credit, please show your steps.

Problem 1:

The necessary equations are:

$$wafer\ area = \pi(d/2)^2$$

$$die\ area = \frac{\text{wafer area}}{\text{Dies per wafer}}$$

$$cost\ per\ die = \frac{\text{cost per wafer}}{\text{Dies per wafer} \times \text{yield}}$$

$$yield = \frac{1}{(1 + \frac{Defects\ per\ area \times die\ area}{2})^2}$$

For processor A, $wafer\ area = 201.06cm^2, die\ area = 2.36cm^2$

For processor B, $wafer\ area = 314.16cm^2, die\ area = 3.14cm^2$

a)

$$yieldA = \frac{1}{(1+\frac{0.02\times2.36}{2})^2} = 0.954$$

$$yieldB = \frac{1}{(1+\frac{0.03\times3.14}{2})^2} = 0.912$$

b)

$$Cost\ per\ dieA = \frac{12}{85 \times 0.954} = 0.148$$

$$Cost\ per\ dieB = \frac{16}{100 \times 0.912} = 0.175$$

c) The number of dies per wafer increased by 15% means the die area shrinks by 15%.

For Processor A:

new number of dies per wafer is 85×1.15 = 98

die area is $2.36cm^2/1.15 = 2.05cm^2$

new number of defects per area is 0.02×1.1 = 0.022

For Processor B:

new number of dies per wafer is 100×1.15 = 115

die area is 3.14cm^2/1.15 = 2.73cm^2

new number of defects per area is 0.03×1.1 = 0.033

$$yieldA = \frac{1}{(1+\frac{0.022\times 2.05}{2})^2} = 0.956$$

$$yieldB = \frac{1}{(1+\frac{0.033\times 2.73}{2})^2} = 0.916$$

$$Cost\ per\ dieA = \frac{12}{98 \times 0.956} = 0.128$$

$$Cost\ per\ dieB = \frac{16}{115 \times 0.916} = 0.152$$

Problem 2:

To calculate dynamic power, the equation is $P_{dyn} = C \times V^2 \times$Clock rate. The results are shown in the table.

Processor	Clock rate	Voltage	Dynamic power
80286(1982)	12.5 MHz	5 V	3.125 W
80386(1985)	16 MHz	5 V	4 W
80496(1989)	25 MHz	5 V	6.25 W
Pentium (1993)	66 MHz	5 V	16.5 W
Pentium Pro (1997)	200 MHz	3.3 V	21.78 W
Pentium 4 W (2001)	2 GHz	1.75 V	61.25 W
Pentium 4 P (2004)	3.6 GHz	1.25 V	56.25 W
Core 2 (2007)	2.67 GHz	1.1 V	51.69 W

Problem 3:

a) Static power P=I×V

I_{leak} =51.69/1.1=46.99 A

b) Leakage power is 21.78W×0.25 = 5.445W. Hence I_{leak} = 5.445/3.3 = 1.65A

Problem 4:

a) Each task is executed on the fastest core. The core assignment is shown in the table.

Task	1	2	3	4	5
HW	1	1	2	3	2

Cost = $HW1_{cost}$ + $HW2_{cost}$ + $HW3_{cost}$ = \$20 + \$16 + \$14 = \$50
Tasks 2 and 3 are executed in parallel by different units. Therefore:
Execution time = 9 + max(8, 7) + 7 + 8 = 32s

b) HW1, HW2 and HW4 are able to execute all tasks. We can run every task on HW4, the cheapest core. Cost = \$10
Now there is only one core therefore tasks cannot be executed in parallel. Therefore:
Execution time = 16 + 18 + 13 + 12 + 11 = 70s

c) First, we try to use one core to execute all the tasks. HW1 is the fastest among all the cores.
Execution time = 9 + 8 + 12 + 10 + 9 = 48s.
It exceeds the deadline. Therefore one core is insufficient.

Next, we try to use two cores. This allows us to execute T2 and T3 in parallel. We use the cheapest core, HW4, in addition to HW1. The core assignment is shown in the Table.

Task	1	2	3	4	5
HW	1	1	4	1	1

Cost = \$20 + \$10 = \$30
Execution time = 9 + max(8, 13) + 10 + 9 = 41s. It still does not meet the deadline. We need to go for another solution. Note that the cost of HW2 and HW3 is also 30. Let us try this option. The core assignment is shown in the Table.

Task	1	2	3	4	5
HW	2	3	2	3	2

Cost = \$16+ \$14 = \$30
Execution time = 11 + max (13, 7) +7 + 8 = 39s. This meets the deadline.
Final schedule: T1 -> 2, start time = 0;
T2 -> 3, start time = 11;
T3 -> 2, start time = 11;
T4 -> 3, start time = 24;
T5 -> 2, start time = 31;