

UNIVERSITY *of* DELAWARE

Chapter 8

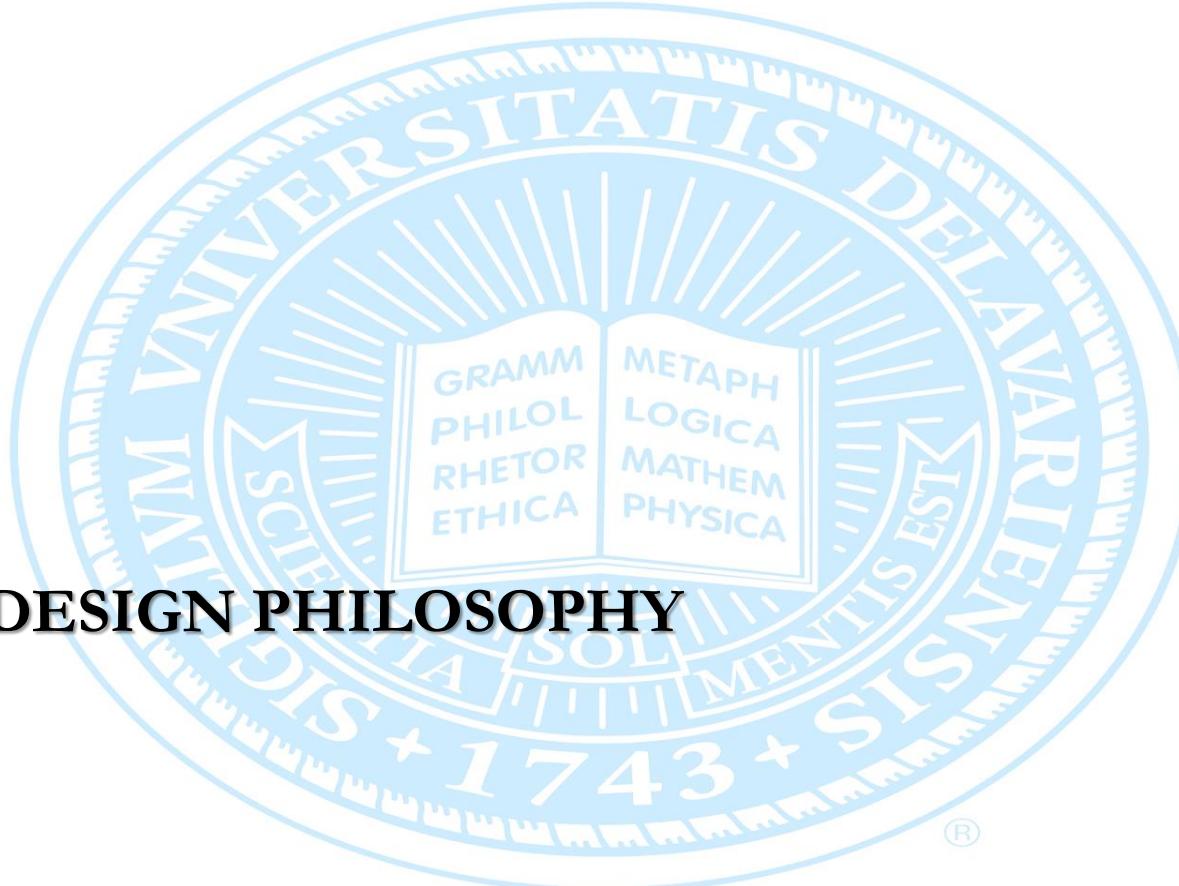
Building Blocks of Integrated-Circuit Amplifiers





IN THIS CHAPTER YOU WILL LEARN

1. The basic integrated-circuit (IC) design philosophy and how it differs from that for discrete-circuit design.
2. How current sources are used to bias IC amplifiers and how the reference current generated in one location is replicated at various other locations on the IC chip by using current mirrors.
3. The basic gain cells of IC amplifiers, namely, the CS and CE amplifiers with current-source loads.
4. How the CG and CB amplifiers act as current buffers.
5. How to increase the gain realized in the basic gain cells by employing the principle of cascoding.
6. Analysis and design of the cascode amplifier and the cascode current source in both their MOS and bipolar forms.
7. Some ingenious analog circuit design techniques that result in current mirrors with vastly improved characteristics.
8. How to pair transistors to realize amplifiers with characteristics superior to those obtained from a single-transistor stage.



8.1 IC DESIGN PHILOSOPHY



Discrete vs Integrated Circuits

Resistors

Capacitors

Power Supplies

Device Variety

Bipolar Technology

CMOS Technology

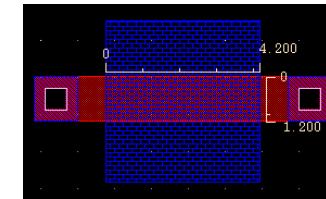
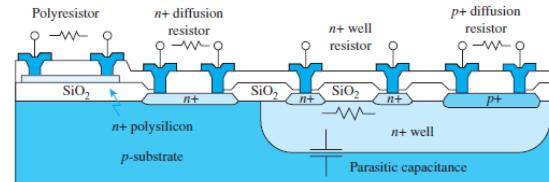


Figure A.7 Cross sections of various resistor types available from a typical *n*-well CMOS process.

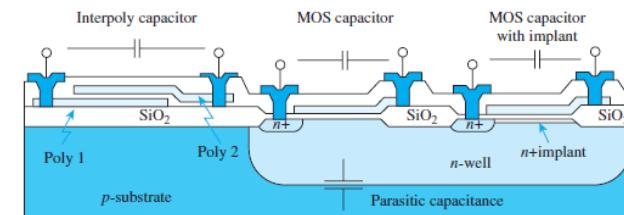
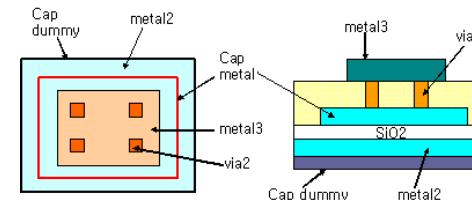


Figure A.8 Interpoly and MOS capacitors in an *n*-well CMOS process.





Device Technologies

- MOS Metal Oxide Semiconductors
- FET Field Effect Transistor
- CMOS Complementary MOS
- BJT Bipolar Junction Transistor
- BiCMOS

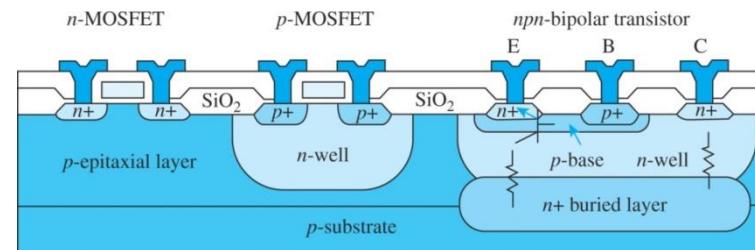
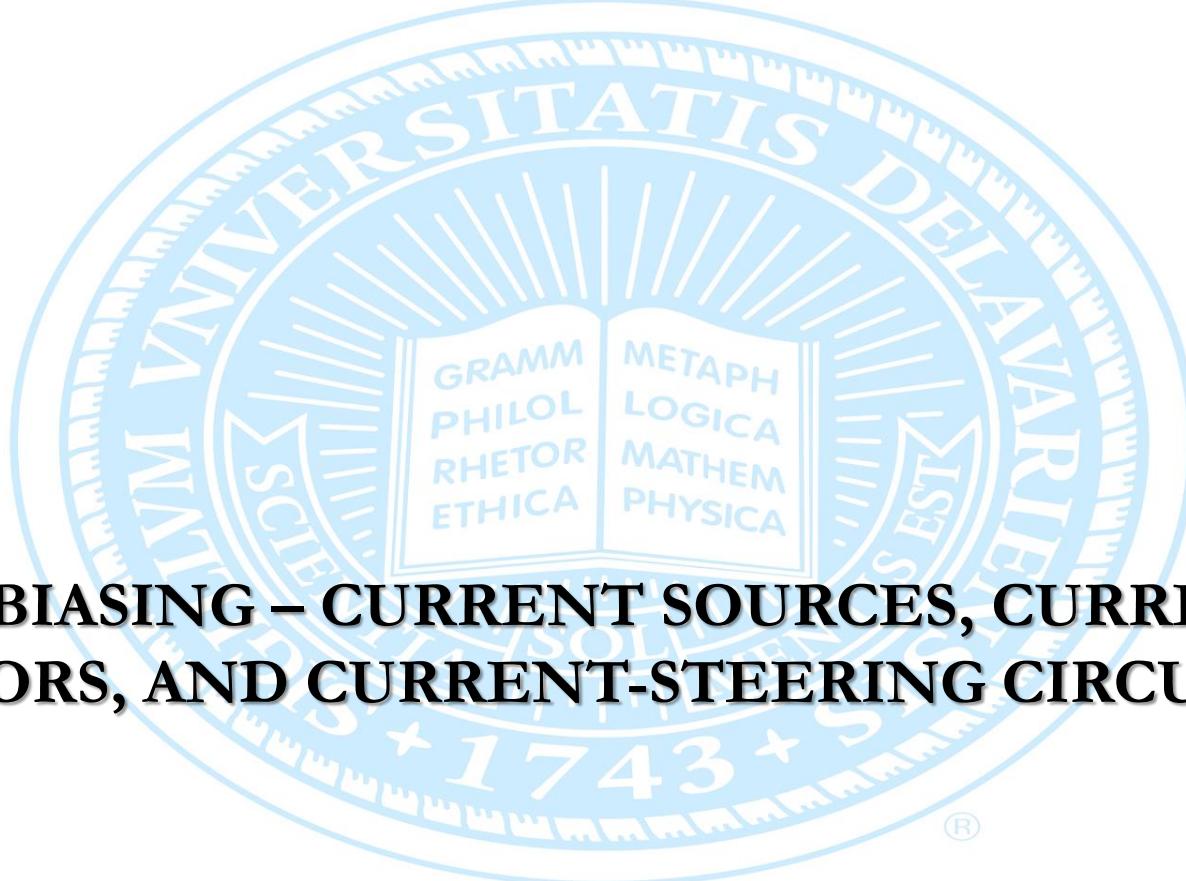


Figure A.10 Cross-sectional diagram of a BiCMOS process.



8.2 IC BIASING – CURRENT SOURCES, CURRENT MIRRORS, AND CURRENT-STEERING CIRCUITS



The Basic MOSFET Current Source

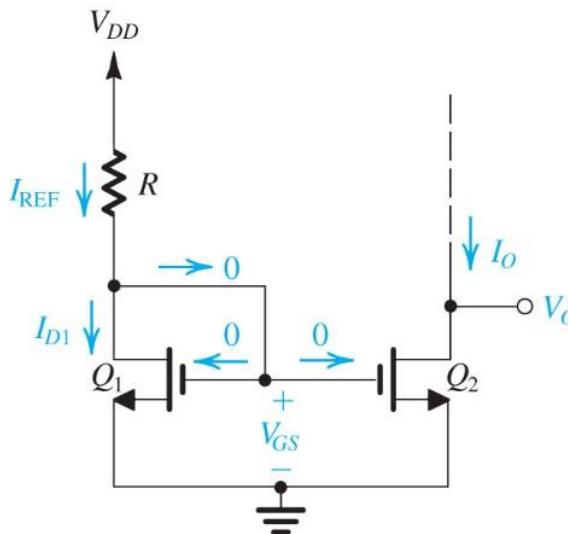


Figure 8.1 Circuit for a basic MOSFET constant-current source. For proper operation, the output terminal, that is, the drain of Q_2 , must be connected to a circuit that ensures that Q_2 operates in saturation.

A circuit for implementing the constant-current source I is shown in Fig. 8.1. The heart of the circuit is transistor Q_1 whose drain is shorted to its gate, and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 (V_{GS} - V_{tn})^2$$

where we have neglected channel-length modulation. The drain current (reference current) of Q_1 is supplied by V_{DD} through resistor R . Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R} = \frac{V_{DD} - V_{GS}}{R}$$

Now consider transistor Q_2 : It has the same V_{GS} as Q_1 ; thus if we assume that it is operating in saturation, its drain current is

$$I_O = I_{D2} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_2 (V_{GS} - V_{tn})^2$$



Basic MOSFET Current Mirror

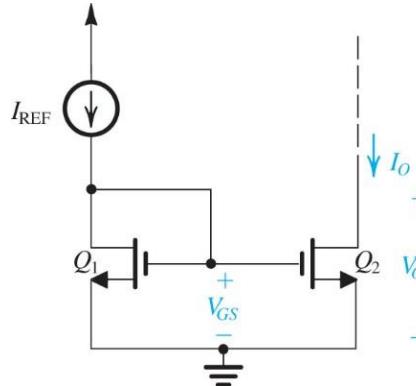


Figure 8.2 Basic MOSFET current mirror.

$$I_O = I_{D2} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_2 (V_{GS} - V_{m_2})^2$$

$$I_{REF} = I_{D1} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 (V_{GS} - V_{m_1})^2$$

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

This is known as the **current gain** or **current transfer ratio** of the current mirror

The FETs must be operating in saturation which means that the drain voltage, V_O , must satisfy the relationship

$$V_O \geq V_{GS} - V_{m_1} = V_{OV}$$

Which means that the current source will operate properly as long as the output voltage is above the overdrive voltage, typically a few tenths of a volt.

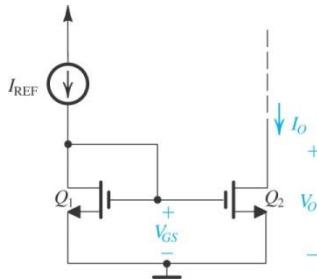


Figure 8.2 Basic MOSFET current mirror.

Effect of V_O on I_O

Channel length modulation can have a significant effect on the operation of the current source.

$$I_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (V_{GS} - V_m)(1 + \lambda V_{DS}) = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (V_{GS} - V_m) \left(1 + \frac{V_o}{V_{A2}} \right)$$

Consider the case where $Q_1 = Q_2$. The drain current of Q_2 , I_O , will equal the current in Q_1 , I_{REF} , at the value of V_O that causes the two devices to have the same V_{DS} , that is, at $V_O = V_{GS}$. As V_O is increased above this value I_O will increase according to the incremental output resistance, r_{o2} , of Q_2 .

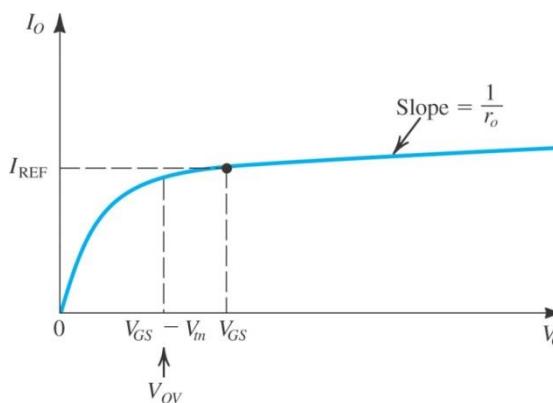


Figure 8.3 Output characteristic of the current source in Fig. 8.1 and the current mirror of Fig. 8.2 for the case of Q_2 matched to Q_1 .

$$R_o \equiv \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O}$$

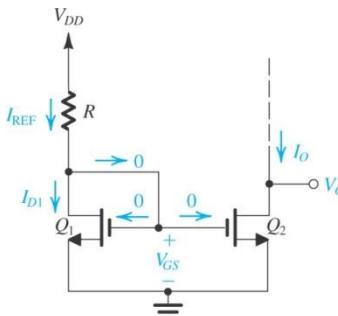
$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF} \left(1 + \frac{V_o - V_{GS}}{V_{A2}} \right)$$



Example 8.1a

Given $V_{DD} = 3$ V and using $I_{REF} = 100$ uA, design the circuit of Fig. 8.1 to obtain an output current whose nominal value is 100 uA. Find R if Q_1 and Q_2 are matched and have channel lengths of 1 um, channel widths of 10 um, $V_t = 0.7$ V, and $k_n' = 200$ uA/V². What is the lowest possible value of V_O ? Assuming that for this process technology, the Early voltage $V'_A = 20$ V/um, find the output resistance of the current source. Also, find the change in output current resulting from a +1-V change in V_O .

$$I_{D1} = I_{REF} = \frac{1}{2} k_n' \left(\frac{W}{L} \right)_1 V_{OV}^2 \Rightarrow 100\mu\text{A} = \left(\frac{1}{2} \right) \left(200 \frac{\mu\text{A}}{\text{V}^2} \right) \left(\frac{10\mu\text{m}}{1\mu\text{m}} \right) V_{OV}^2$$
$$\Rightarrow V_{OV} = \sqrt{0.1\text{V}^2} = 0.316\text{V}$$



$$V_{GS} = V_t + V_{OV} = 0.7\text{V} + 0.316\text{V} = 1.016\text{V}$$

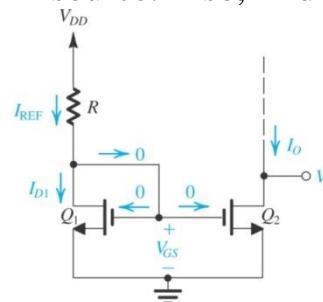
$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{3\text{V} + 1.016\text{V}}{0.1\text{mA}} = 19.84\text{k}\Omega$$



Example 8.1b

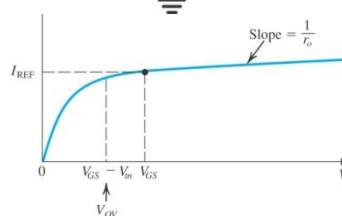
Given $V_{DD} = 3$ V and using $I_{REF} = 100$ uA, design the circuit of Fig. 8.1 to obtain an output current whose nominal value is 100 uA. Find R if Q_1 and Q_2 are matched and have channel lengths of 1 um, channel widths of 10 um, $V_t = 0.7$ V, and $k_n' = 200$ uA/V². What is the lowest possible value of V_O ? Assuming that for this process technology, the Early voltage $V_A' = 20$ V/um, find the output resistance of the current source. Also, find the change in output current resulting from a +1-V change in V_O .

$$V_{O\min} = V_{OV} = 0.316V$$



For transistors with channel lengths of 1 um

$$V_A = V_A' L = \left(20 \frac{V}{\mu m}\right)(1\mu m) = 20V \quad r_{o2} = \frac{V_A}{I_D} = \frac{20V}{0.1mA} = 200k\Omega$$



$I_O = 100$ uA at $V_O = V_{GS} = 1.016V$ for a +1 V increase in V_O

$$\Delta I_O = \frac{\Delta V_O}{r_{o2}} = \frac{1V}{200k\Omega} = 5\mu A$$



MOS Current-Steering Circuits

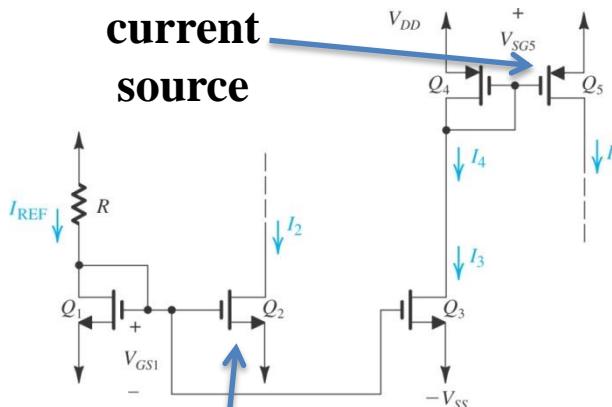


Figure 8.4 A current-steering circuit.

current sink

Once a constant current has been generated, it can be replicated to provide dc bias or load currents for the various amplifier stages in an IC. Current mirrors can obviously be used to implement this current-steering function.

$$I_2 = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{GS1} - V_{tn}$$

or $V_{D2}, V_{D3} \geq -V_{SS} + V_{OVI}$

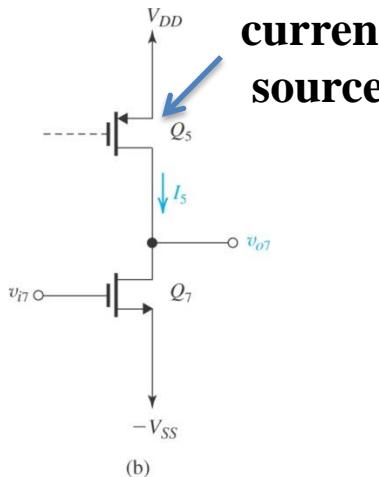
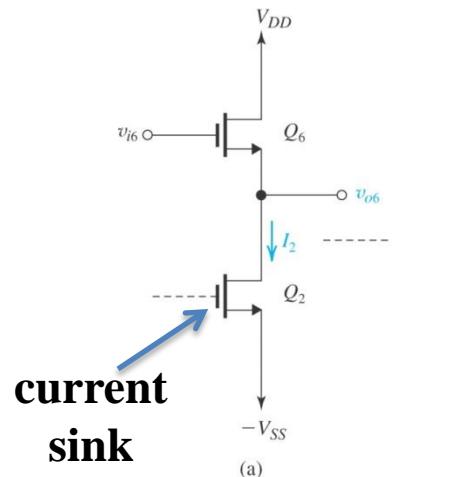
$$I_3 = I_{REF} \frac{(W/L)_3}{(W/L)_1}$$

$$I_4 = I_3 = I_{REF} \frac{(W/L)_3}{(W/L)_1} \quad V_{D5} \leq V_{DD} - |V_{OV5}|$$

$$I_5 = I_4 \frac{(W/L)_5}{(W/L)_4} = I_{REF} \frac{(W/L)_3}{(W/L)_1} \frac{(W/L)_5}{(W/L)_4}$$



Current Source/Sink



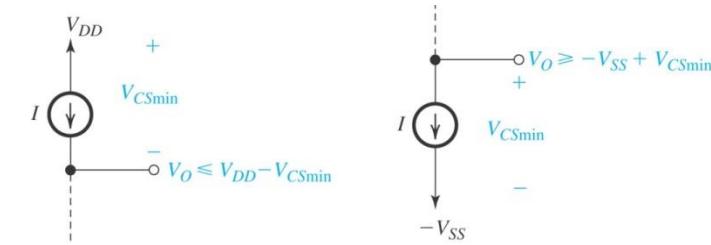
**current
sink**

(a)

**current
source**

(b)

Figure 8.5 Application of the constant currents I_2 and I_5 generated in the current-steering circuit of Fig. 8.4. Constant-current I_2 is the bias current for the source follower Q_6 , and constant-current I_5 is the load current for the common-source amplifier Q_7 .



(a)

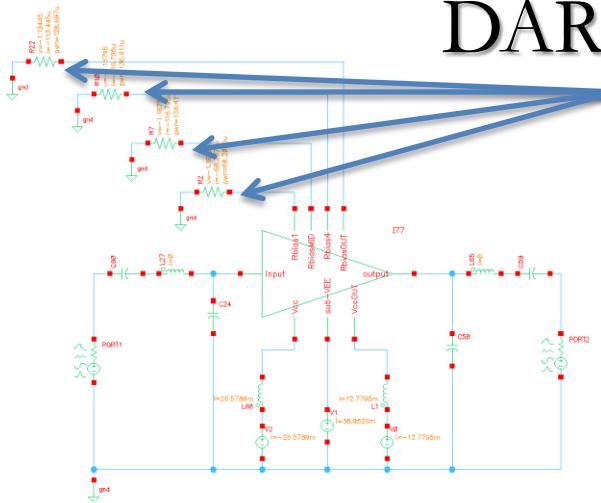
(b)

Figure 8.6 (a) A current source; and (b) a current sink.

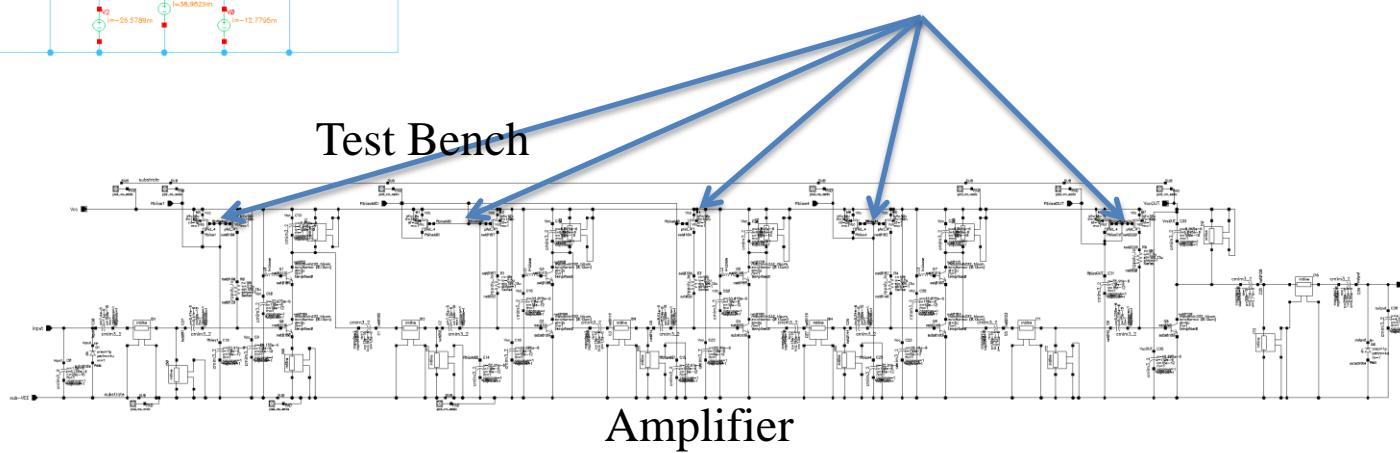
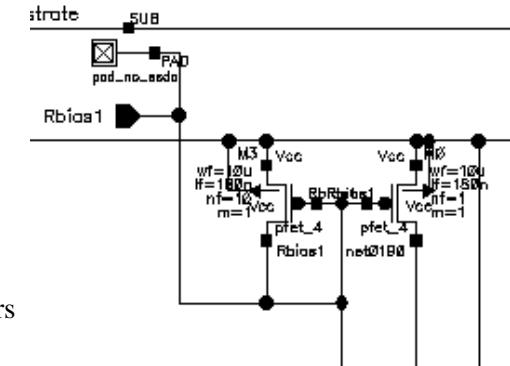
Q₂ pulls its current I₂ from a circuit while Q₅ pushes its current I₅ into a circuit



DARPA 95 GHz SiGe LNA

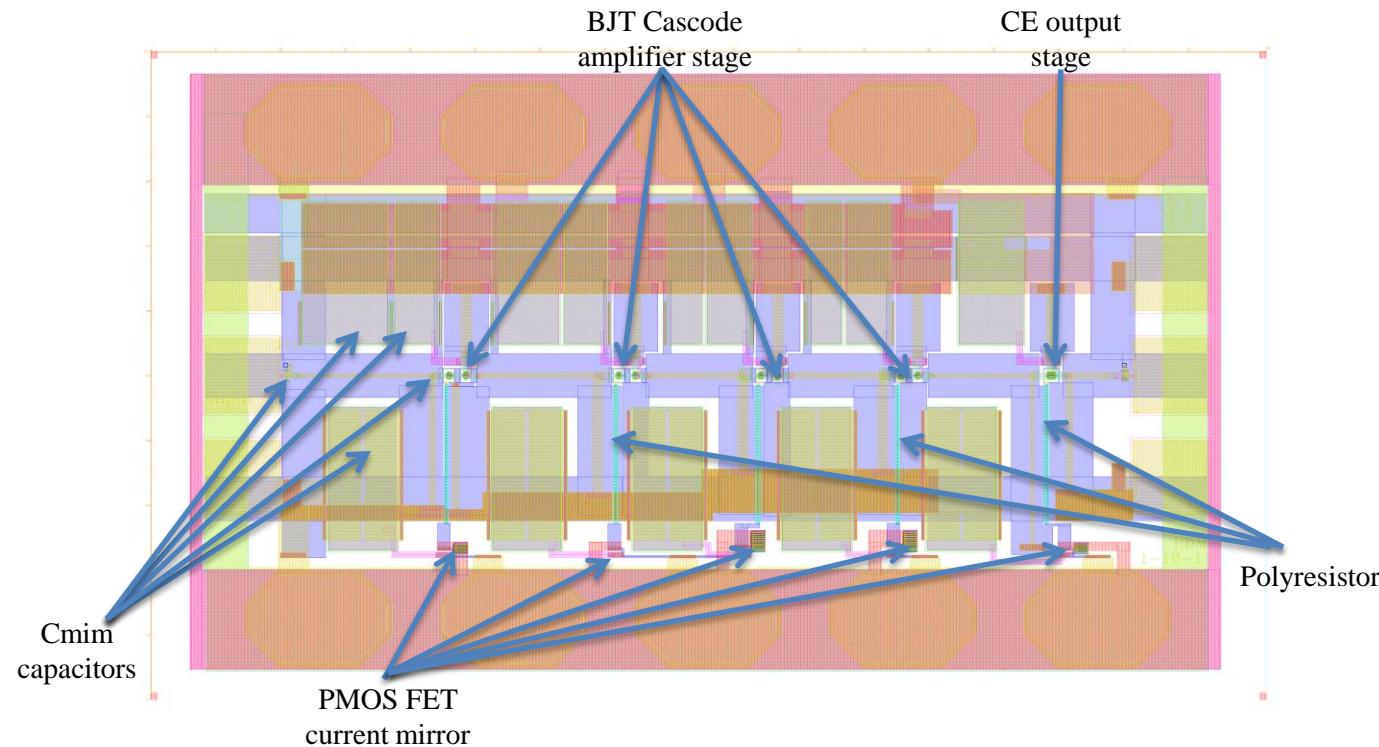


Off chip resistors to set bias currents.
Implemented using Digitally Controlled Potentiometers (DCPs) over an I2C bus.





DARPA 95 GHz SiGe LNA



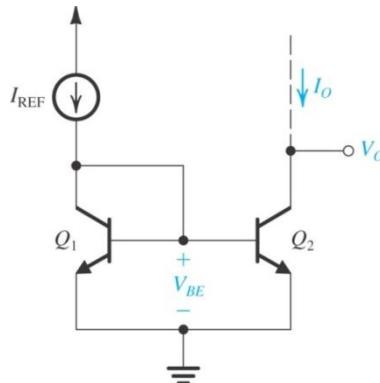


Figure 8.7 The basic BJT current mirror.

consider the case of β sufficiently high that we can neglect the base currents. If the EBJ area of $Q_1 = Q_2$ (i.e. matched) then $I_O = I_{REF}$

For this to happen, however, Q_2 must be operating in the active mode, which in turn is achieved as long as the collector voltage V_o is 0.3 V higher than that of the emitter.

To obtain a current transfer ratio other than unity, say m , we simply arrange that the area of the EBJ of Q_2 is m times that of Q_1 . In this case $I_O = m I_{REF}$. In general,

$$\frac{I_O}{I_{REF}} = \frac{I_{S2}}{I_{S1}} = \frac{\text{Area of EBJ of } Q_2}{\text{Area of EBJ of } Q_1} = m$$

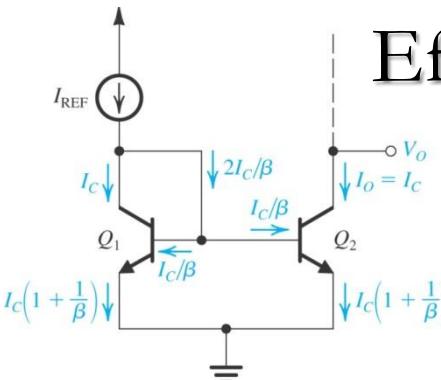
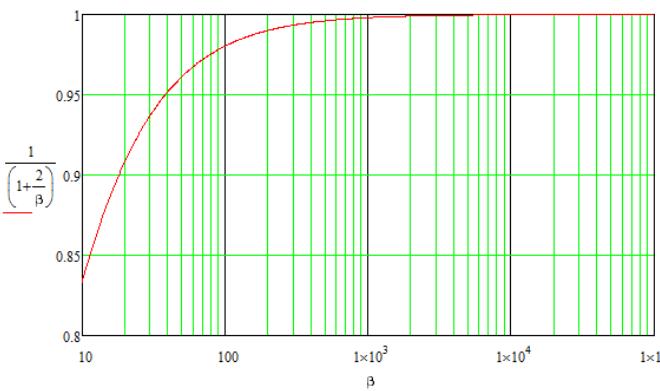


Figure 8.8 Analysis of the current mirror taking into account the finite β of the BJTs.



Effect of β on a BJT Current Mirror

Consider the effect of finite transistor β on the current transfer ratio. The analysis for the case in which the current transfer ratio is nominally unity (i.e. Q_1 matched to Q_2). Therefore Q_1 and Q_2 have the same V_{BE} and I_C ($I_O = I_C$).

$$I_{\text{REF}} = I_C + 2I_C/\beta = I_C \left(1 + \frac{2}{\beta}\right)$$

$$\frac{I_O}{I_{\text{REF}}} = \frac{I_C}{I_C \left(1 + \frac{2}{\beta}\right)} = \frac{1}{\left(1 + \frac{2}{\beta}\right)}$$

$$\frac{I_O}{I_{\text{REF}}} = \frac{m}{1 + \frac{m+1}{\beta}}$$

actual current transfer ratio of the BJT current mirror for a nominal current transfer ratio of m



Effect of finite R_o

In common with the MOS current mirror, the BJT mirror has a finite output resistance R_o

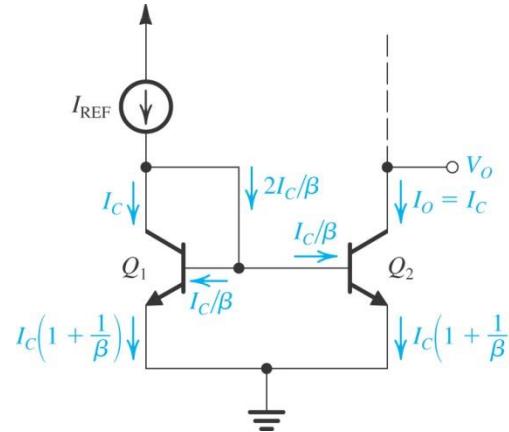


Figure 8.8 Analysis of the current mirror taking into account the finite β of the BJTs.

$$R_o \equiv \frac{\Delta V_o}{\Delta I_o} = r_{o2} = \frac{V_{A2}}{I_o}$$

$$I_o = I_{\text{REF}} \left(\frac{m}{1 + \frac{m+1}{\beta}} \right) \left(1 + \frac{V_o - V_{BE}}{V_{A2}} \right)$$

error term due to
finite β

error term due to the
Early effect



A Simple BJT Current Source

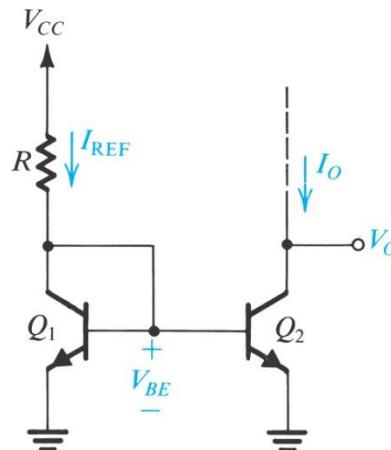


Figure 8.9 A simple BJT current source.

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}$$

where V_{BE} is the base-emitter voltage corresponding to the desired value of I_{REF} . The output current I_O is given by

$$I_O = I_{REF} \left(\frac{1}{1 + \frac{2}{\beta}} \right) \left(1 + \frac{V_o - V_{BE}}{V_A} \right)$$

$$R_o = r_{o2} \approx \frac{V_A}{I_O} \approx \frac{V_A}{I_{REF}}$$



Exercise 8.3

Consider a BJT current mirror with a nominal current transfer ratio of unity. Let the transistors have $I_S = 10^{-15}\text{A}$, $\beta = 100$, and $V_A = 100\text{ V}$. For $I_{\text{REF}} = 1\text{ mA}$, find I_O when $V_O = 5\text{ V}$. Also, find the output resistance.

$$I_O = I_{\text{REF}} \left(\frac{1}{1 + \frac{2}{\beta}} \right) \left(1 + \frac{V_O - V_{BE}}{V_A} \right)$$

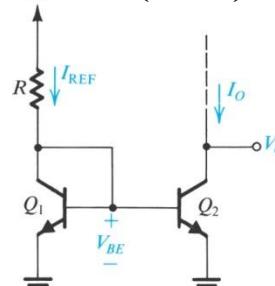


Figure 8.9 A simple BJT current source.

$$I_O = I_D = I_S e^{(V_{BE}/V_T)}$$

$$V_{BE} = V_T \ln \left(\frac{I_D}{I_S} \right) = (25\text{mV}) \ln \left(\frac{10^{-3}\text{A}}{10^{-15}\text{A}} \right) = 518.08\text{mV}$$

$$I_O|_{5\text{V}} = 1\text{mA} \left(\frac{1}{1 + \frac{2}{100}} \right) \left(1 + \frac{5 - 0.518}{100} \right) = 1.025\text{mA}$$

$$R_o = r_{o2} \approx \frac{V_A}{I_O} = \frac{100\text{V}}{1.025\text{mA}} = 97.56\text{k}\Omega$$



Exercise D8.4

Assuming the availability of BJTs with scale currents $I_s = 10^{-15}$ A, $\beta = 100$, and $V_A = 50$ V, design the current-source circuit of Fig. 8.9 to provide an output current $I_O = 0.5$ mA at $V_O = 2$ V. The power supply $V_{CC} = 5$ V. Give the values of I_{REF} , R , and V_{Omin} . Also, find I_O at $V_O = 5$ V.

$$V_{BE} = V_T \ln\left(\frac{I_O}{I_S}\right) = (25\text{mV}) \ln\left(\frac{0.5 \times 10^{-3} \text{A}}{10^{-15} \text{A}}\right) = 0.673\text{V}$$
$$I_O|_{2\text{V}} = 0.5\text{mA} = I_{REF} \left(\frac{1}{1 + \frac{2}{\beta}} \right) \left(1 + \frac{V_O - V_{BE}}{V_A} \right) = I_{REF} \left(\frac{1}{1 + \frac{2}{100}} \right) \left(1 + \frac{2 - 0.7}{50} \right)$$
$$\Rightarrow I_{REF} = 0.497\text{mA}$$
$$I_{REF} = \frac{V_{CC} - V_{BE}}{R} \quad R = \frac{V_{CC} - V_{BE}}{I_{REF}} = \frac{5 - 0.673}{0.497\text{mA}} = 8.71\text{k}\Omega$$

Figure 8.9 A simple BJT current source.

$$V_{Omin} = V_{CESat} = 0.3\text{V}$$

$$I_O|_{5\text{V}} = 0.497\text{mA} \left(\frac{1}{1 + \frac{2}{100}} \right) \left(1 + \frac{5 - 0.673}{50} \right) = 0.53\text{mA}$$



Generating Multiple Current Sinks/Sources

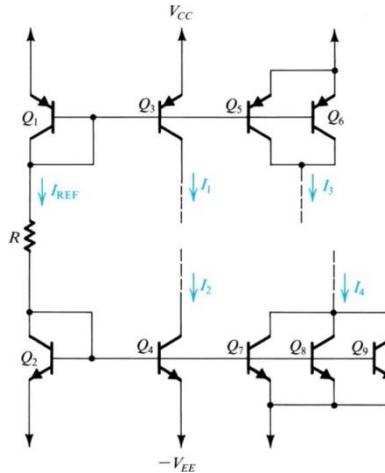


Figure 8.10 Generation of a number of constant currents of various magnitudes.

The dc reference current I_{REF} is generated in the branch that consists of the diode-connected transistor Q_1 resistor R , and the diode-connected transistor Q_2 :

$$I_{REF} = \frac{V_{CC} + V_{EE} - V_{EB1} - V_{BE2}}{R}$$

assuming high β (i.e. $I_B = 0$ mA) and no Early effect

$$I_1 = I_2 = I_{REF}$$

$$I_3 = 2I_{REF}$$

$$I_4 = 3I_{REF}$$



Exercise D8.5

Figure E8.5 shows an N -output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

$$I_1 = I_2 = \dots = I_N = \frac{I_{\text{REF}}}{1 + (N+1)/\beta}$$

For $\beta = 100$, find the maximum number of outputs for an error not exceeding 10%.

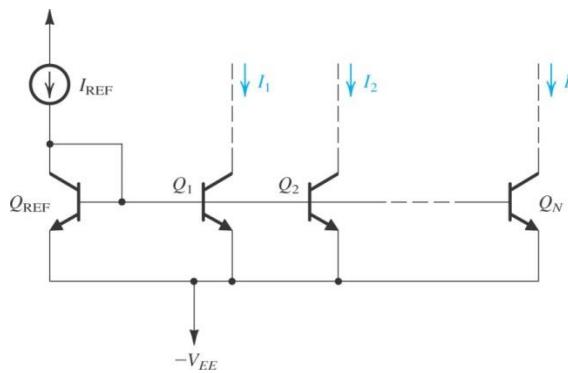


Figure E8.5

$$\begin{aligned} I_{\text{REF}} &= I_C|_{Q_{\text{REF}}} + I_B|_{Q_{\text{REF}}} + (N)I_B|_{Q_N} = I_C|_{Q_{\text{REF}}} + (N+1)I_B|_{Q_{\text{REF}}} \\ &= I_C|_{Q_{\text{REF}}} + \frac{(N+1)}{\beta} I_C|_{Q_{\text{REF}}} = I_C|_{Q_{\text{REF}}} \left[1 + \frac{(N+1)}{\beta} \right] \\ \Rightarrow I_1 &= I_2 = \dots = I_N = I_C|_{Q_{\text{REF}}} = \frac{I_{\text{REF}}}{1 + \frac{(N+1)}{\beta}} \end{aligned}$$

$$0.1 = \frac{N+1}{\beta} = \frac{N+1}{100} \quad N = (100 \times 0.1) - 1 = 9$$



A Bipolar Mirror with Base-Current Compensation

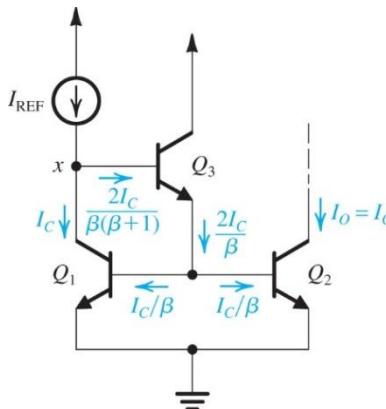


Figure 8.11 A current mirror with base-current compensation.

Figure 8.11 shows a bipolar current mirror with a current transfer ratio that is much less dependent on β than that of the simple current mirror. The reduced dependence on β is achieved by including transistor Q_3 , the emitter of which supplies the base currents of Q_1 and Q_2 . The sum of the base currents is then divided by $(\beta_3 + 1)$, resulting in a much smaller error current that has to be supplied by I_{REF} . Detailed analysis is shown on the circuit diagram; it is based on the assumption that Q_1 and Q_2 are matched and thus have equal collector currents, I_C .

$$I_O = I_C \quad I_{REF} = I_C \left[1 + \frac{2}{\beta(\beta+1)} \right] \quad \Rightarrow \frac{I_O}{I_{REF}} = \frac{1}{1 + 2/(\beta^2 + \beta)} \approx \frac{1}{1 + 2/\beta^2}$$

If we connect node x to the power supply, V_{CC} , through a resistance R .

$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R}$$



Small-Signal Operation of Current Mirrors

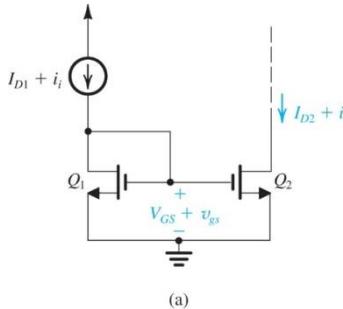


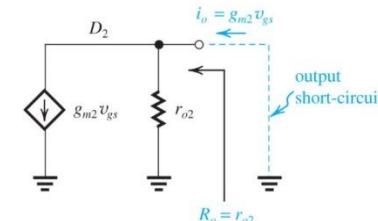
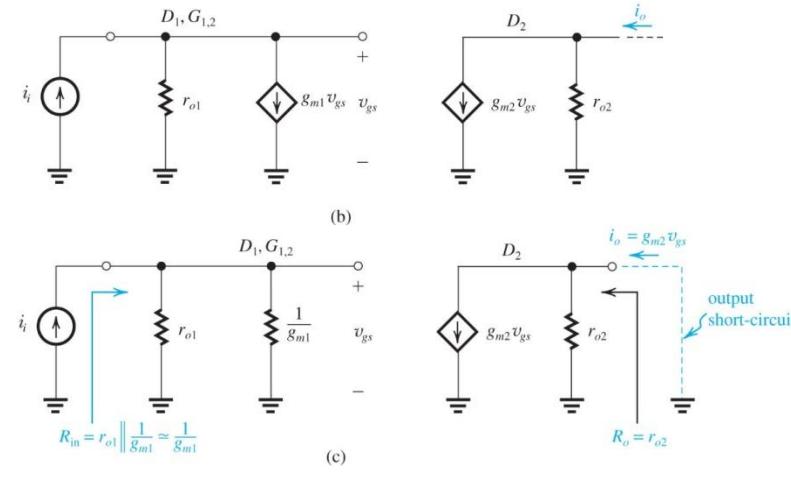
Figure 8.12 Obtaining the small-signal parameters of the MOS current mirror as a current amplifier.

$$R_{in} = r_{o1} \parallel \frac{1}{g_{m1}} \simeq \frac{1}{g_{m1}}$$

$$A_{is} \equiv \left. \frac{i_o}{i_i} \right|_{v_{d2}=0} = \frac{g_{m2} v_{gs}}{i_i} \simeq \frac{g_{m2} (i_i / g_{m1})}{i_i} = \frac{g_{m2}}{g_{m1}}$$

$$g_{m1,2} = \mu_n C_{ox} (W/L)_{1,2} V_{OV} \Rightarrow A_{is} = \frac{(W/L)_2}{(W/L)_1}$$

Insert small signal
transistor models



$$R_o = r_{o2}$$

Short-circuit current gain is equal
to the DC current gain



Exercise D8.6

The MOSFETs in the current mirror of Fig. 8.12(a) have equal channel lengths, $\mu_n C_{ox} = 400 \mu\text{A}/\text{V}^2$, and $V_A' = 20 \text{ V}/\mu\text{m}$. If the input bias current is $100 \mu\text{A}$, find W_1 , W_2 , L_1 , and L_2 to obtain a short-circuit current gain of 5, an input resistance of $1 \text{ k}\Omega$, and an output resistance of $40 \text{ k}\Omega$.

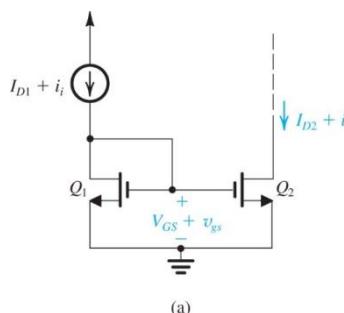


Figure 8.12

$$\begin{aligned} R_{in} = 1\text{k}\Omega &= \frac{1}{g_{m1}} \quad \Rightarrow g_{m1} = \frac{1\text{mA}}{\text{V}} \\ g_{m1} &= \sqrt{2(\mu_n C_{0x}) \left(\frac{W}{L} \right)_1 I_{D1}} = \sqrt{2 \left(0.4 \frac{\text{mA}}{\text{V}} \right) \left(\frac{W}{L} \right)_1 0.1\text{mA}} = \frac{1\text{mA}}{\text{V}} \\ \Rightarrow \left(\frac{W}{L} \right)_1 &= 12.5 \quad A_{is} = 5 = \frac{(W/L)_2}{(W/L)_1} \Rightarrow \left(\frac{W}{L} \right)_2 = 5 \times 12.5 = 62.5 \end{aligned}$$

$$R_O = r_{o2} = \frac{V_{A2}}{I_{D2}} = \frac{V_{A2}}{5I_{D1}} = 40\text{k}\Omega \quad \Rightarrow V_{A2} = V_A' L = (5I_{D1}) 40\text{k}\Omega = 20\text{V}$$

$$\Rightarrow L_2 = \frac{V_{A2}}{V_A'} = \frac{20\text{V}}{20\text{V}/\mu\text{m}} = 1\mu\text{m} \quad W_2 = 62.5\mu\text{m} \quad L_1 = 1\mu\text{m} \quad L_1 = 12.5\mu\text{m}$$



Homework #1

Read Chapter 8

Chapter 8 Problems:

1. 8.1*
2. 8.5
3. 8.9
4. 8.13
5. 8.14*
6. 8.17*

* Answers in Appendix L



8.3 THE BASIC GAIN CELL



Basic Gain Cells

The basic gain cell in an IC amplifier is a common-source (CS) or common-emitter (CE) transistor loaded with a constant-current source. These circuits are similar to the CS and CE amplifiers studied in ELEG 309, except that here we have replaced the resistances R_D and R_C with constant-current sources.

- 1). Precise resistors are hard to create on ICs
- 2). Supply voltages are low
- 3). Current Sources have high effective load resistance

These circuits are said to be **current-source loaded** or **active loaded**.



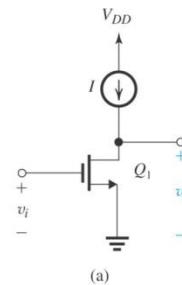
Basic Gain Cells

Common-Source Amplifier

$$R_{in} = \infty$$

$$A_{vo} = -g_m r_o$$

$$R_o = r_o$$



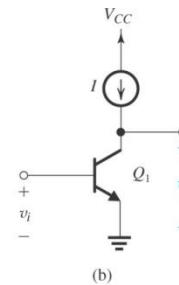
(a)

Common-Emitter Amplifier

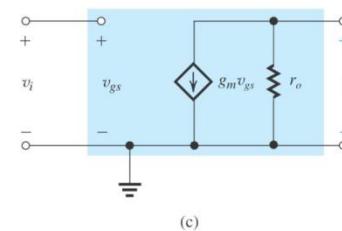
$$R_{in} = r_\pi$$

$$A_{vo} = -g_m r_o$$

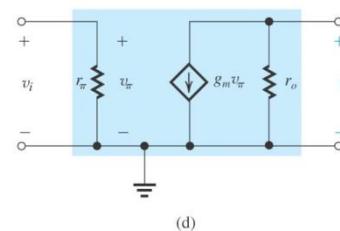
$$R_o = r_o$$



(b)



(c)



(d)

Figure 8.13 The basic gain cells of IC amplifiers: (a) current-source or active-loaded common-source amplifier; (b) current-source or active-loaded common-emitter amplifier; (c) small-signal equivalent circuit of (a); and (d) small-signal equivalent circuit of (b).

Both circuits realize a voltage gain of magnitude $g_m r_o$. Since this is the maximum gain obtainable in a CS or CE amplifier, we refer to it as the **intrinsic gain** and give it the symbol A_0 .



The Intrinsic Gain of a CE Amplifier

$$A_{vo} = -g_m r_o$$

$$g_m = \frac{I_C}{V_T}$$

$$r_o = \frac{V_A}{I_C}$$

$$A_0 = |A_{vo}| = g_m r_o = \left(\frac{I_C}{V_T} \right) \left(\frac{V_A}{I_C} \right) = \frac{V_A}{V_T}$$

Thus A_0 is simply the ratio of the Early voltage V_A , which is a technology-determined parameter, and the thermal voltage V_T , which is a physical parameter (approximately 25 mV at room temperature). The value of V_A ranges from 5 V to 35 V for modern IC fabrication processes to 100 V to 130 V for the older, so-called high-voltage processes.

As a result, the value of A_0 will be in the range of 200 V/V to 5000 V/V, with the lower values characteristic of modern small-feature-size devices.



Intrinsic Gain of a CS Amplifier

$$g_m = \frac{2I_D}{V_{OV}} \quad r_o = \frac{V_A}{I_D} = \frac{V'_A L}{I_D} \quad A_0 = |A_{vo}| = g_m r_o = \left(\frac{2I_D}{V_{OV}} \right) \left(\frac{V_A}{I_D} \right) = \frac{2V_A}{V_{OV}} = \frac{2V'_A L}{V_{OV}}$$

1. The quantity in the denominator is $V_{OV}/2$, which is a design parameter. Although the value of V_{OV} that designers use for modern submicron technologies has been steadily decreasing, it is still about 0.15 V to 0.3 V. Thus $V_{OV}/2$ is 0.075 V to 0.15 V, which is 3 to 6 times higher than V_T .
2. The numerator quantity is both process dependent (through V'_A) and device dependent (through L), and its value has been steadily decreasing with the scaling down of the technology.
3. For a given technology (i.e., a given value of V'_A) the intrinsic gain A_0 can be increased by using a longer MOSFET and operating it at a lower V_{OV} . As usual, however, there are design trade-offs.

As a result, the intrinsic gain realized in a MOSFET fabricated in a modern short-channel technology is only 20 V/V to 40 V/V, an order of magnitude lower than that for a BJT.



Intrinsic Gain of a CS Amplifier

$$g_m = \sqrt{2\mu_n C_{ox} (W/L)} \sqrt{I_D}$$

$$A_0 = \frac{V'_A \sqrt{2\mu_n C_{ox} (WL)}}{\sqrt{I_D}}$$

An alternative expression for the MOSFET A_0 reveals that for a given process technology ($V'_A L$ and $\mu_n C_{ox}$) and a given device (W and L), the intrinsic gain is inversely proportional to $\sqrt{I_D}$.

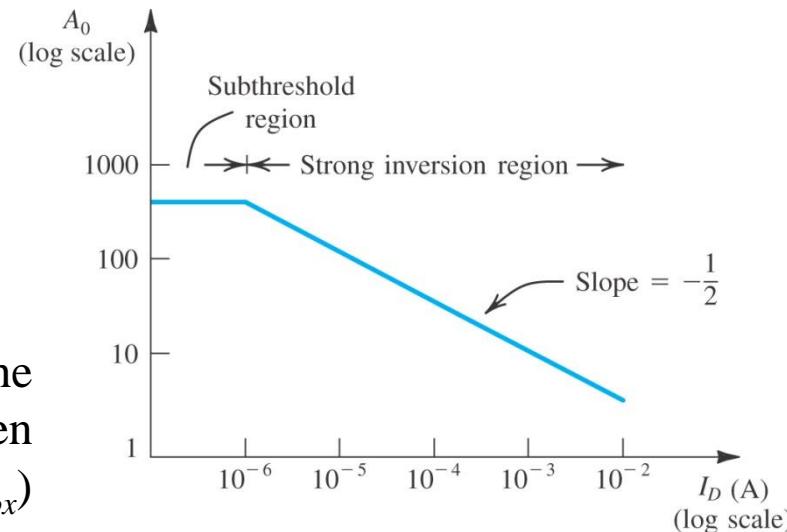


Figure 8.14 The intrinsic gain of the MOSFET versus bias current I_D . Outside the subthreshold region, this is a plot of $A_0 = V'_A \sqrt{2\mu_n C_{ox} WL / I_D}$ for the case: $\mu_n C_{ox} = 20 \mu\text{A/V}^2$, $V'_A = 20 \text{ V}/\mu\text{m}$, $L = 2 \mu\text{m}$, and $W = 20 \mu\text{m}$.



Example 8.2

We wish to compare the values of g_m , R_{in} , R_o , and A_0 for a CS amplifier that is designed using an NMOS transistor with $L = 0.4 \mu\text{m}$ and $W = 4 \mu\text{m}$ and fabricated to a $0.25\text{-}\mu\text{m}$ technology specified to have $\mu_n C_{ox} = 267 \mu\text{A/V}^2$ and $V_A' = 10 \text{ V}/\mu\text{m}$, with those for a CE amplifier designed using a BJT fabricated in a process with $\beta = 100$ and $V_A = 10 \text{ V}$. Assume that both devices are operating at a drain (collector) current of $100 \mu\text{A}$.

Common-Source Amplifier

$$I_D = 100 \mu\text{A}$$

$$\frac{W}{L} = \frac{4 \mu\text{m}}{0.4 \mu\text{m}} = 10$$

$$\mu_n C_{ox} = 267 \mu\text{A/V}^2$$

$$I_D = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) [V_{OV}]^2$$

$$V_{OV} = 0.27 \text{ V}$$

Common-Emitter Amplifier

$$I_C = 100 \mu\text{A}$$

$$\beta = 100$$

$$V_A = 10 \text{ V}$$



Example 8.2

Common-Source Amplifier

$$g_m = \frac{I_D}{V_{OV}/2} = 0.74 \text{ mA/V}$$

$$R_{in} = \infty$$

$$V'_A = 10 \text{ V}/\mu\text{A}$$

$$r_o = \frac{V_A}{I_D} = \frac{V'_A L}{I_D} = 40 \text{ k}\Omega$$

$$R_o = r_o = 40 \text{ k}\Omega$$

$$A_0 = g_m r_o = 29.6 \text{ V/V}$$

Common-Emitter Amplifier

$$g_m = \frac{I_C}{V_T} = 4 \text{ mA/V}$$

$$R_{in} = r_\pi = \frac{\beta}{g_m} = 25 \text{ k}\Omega$$

$$V_A = 10 \text{ V}$$

$$r_o = \frac{V_A}{I_C} = 100 \text{ k}\Omega$$

$$R_o = r_o = 100 \text{ k}\Omega$$

$$A_0 = g_m r_o = 400 \text{ V/V}$$



Problem 8.27

Find the intrinsic gain of an NMOS transistor fabricated in a process for which $k'_n = 400 \text{ } \mu\text{A/V}^2$ and $V_A' = 10 \text{ V}/\mu\text{m}$. The transistor has a 0.5 μm channel length and is operated at $V_{OV} = 0.2 \text{ V}$. If a 2-mA/V transconductance is required, what must I_D and W be?

$$A_0 = g_m R_o = \left(\frac{2I_D}{V_{OV}} \right) \left(\frac{V_A'}{I_D} \right) = \frac{2V_A'L}{V_{OV}} = \frac{2 \left(10 \frac{\text{V}}{\mu\text{m}} \right) .5\mu\text{m}}{.2\text{V}} = 50 \frac{\text{V}}{\text{V}}$$

$$g_m = \frac{2I_D}{V_{OV}} \Rightarrow I_D = \frac{g_m V_{OV}}{2} = \frac{\left(2 \frac{\text{mA}}{\text{V}} \right) .2\text{V}}{2} = 0.2\text{mA}$$

$$I_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) V_{OV}^2 \Rightarrow W = \frac{2I_DL}{k'_n V_{OV}^2} = \frac{2(0.2\text{mA}) .5\mu\text{m}}{.4 \frac{\text{mA}}{\text{V}^2} (0.2\text{V})^2} = \frac{0.2\mu\text{m}}{0.016} = 12.5\mu\text{m}$$



Common Source Amplifier with an Active Load

PMOS active load
biased in saturation to
current I

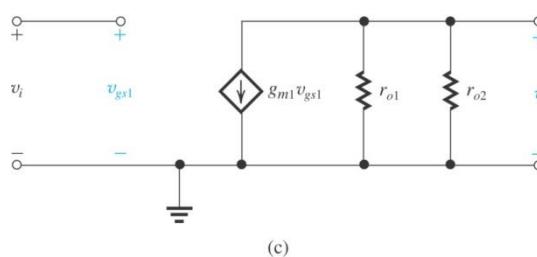
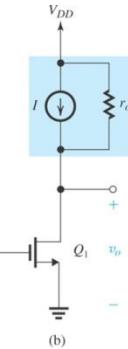
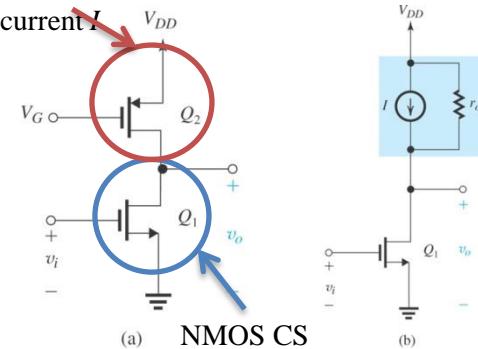


Figure 8.15 (a) The CS amplifier with the current-source load implemented with a *p*-channel MOSFET Q_2 ; (b) the circuit with Q_2 replaced with its large-signal model; and (c) small-signal equivalent circuit of the amplifier.

$$I = \frac{1}{2}(\mu_n C_{ox}) \left(\frac{W}{L} \right)_2 [V_{DD} - V_G - |V_{tp}|]^2$$

$$r_{o2} = \frac{|V_{A2}|}{I}$$

$$A_v \equiv \frac{v_o}{v_i} = -g_{m1}(r_{o1} \parallel r_{o2})$$

If Q_2 has an Early voltage equal to that of Q_1 , $r_{o2} = r_{o1}$ and the gain is reduced by half.

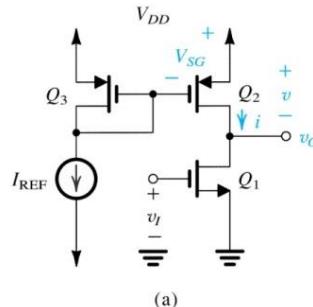
$$A_v = -\frac{1}{2} g_m r_o$$

$$|A_v| = \frac{A_0}{2}$$



Example 8.4a

Consider the CMOS common-source amplifier in Fig. 8.16(a) for the case $V_{DD} = 3$ V, $V_{tn} = |V_{tp}| = 0.6$ V, $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, and $\mu_p C_{ox} = 65 \mu\text{A/V}^2$. For all transistors, $L = 0.4 \mu\text{m}$ and $W = 4 \mu\text{m}$. Also, $V_{An} = 20$ V, $|V_{Ap}| = 10$ V, and $I_{REF} = 100 \mu\text{A}$. Find the small-signal voltage gain. Also, find the coordinates of the extremities of the amplifier region of the transfer characteristic- that is, points A and B.



$$g_m = \sqrt{2\mu_n C_{ox} (W/L) I_{REF}} = \sqrt{2 \left(.2 \frac{\text{mA}}{\text{V}^2} \right) 0.1\text{mA}} = 0.63 \frac{\text{mA}}{\text{V}}$$

$$r_{o1} = \frac{V_{An}}{I_{D1}} = \frac{20\text{V}}{0.1\text{mA}} = 200\text{k}\Omega$$

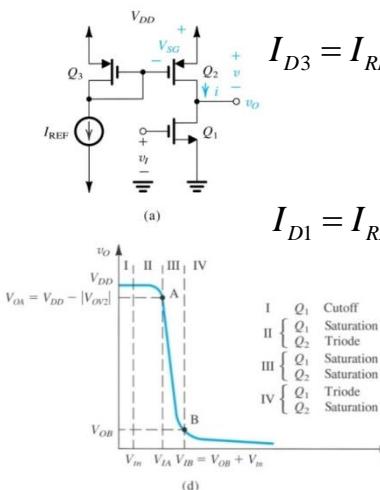
$$r_{o2} = \frac{|V_{Ap}|}{I_{D2}} = \frac{10\text{V}}{0.1\text{mA}} = 100\text{k}\Omega$$

$$A_v = -g_m (r_{o1} \parallel r_{o2}) = -0.63 \frac{\text{mA}}{\text{V}} (200\text{k}\Omega \parallel 100\text{k}\Omega) = -42 \frac{\text{V}}{\text{V}}$$



Example 8.4b

Consider the CMOS common-source amplifier in Fig. 8.16(a) for the case $V_{DD} = 3$ V, $V_{tn} = |V_{tp}| = 0.6$ V, $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, and $\mu_p C_{ox} = 65 \mu\text{A/V}^2$. For all transistors, $L = 0.4 \mu\text{m}$ and $W = 4 \mu\text{m}$. Also, $V_{An} = 20$ V, $|V_{Ap}| = 10$ V, and $I_{REF} = 100 \mu\text{A}$. Find the small-signal voltage gain. Also, find the coordinates of the extremities of the amplifier region of the transfer characteristic - that is, points A and B.



$$I_{D3} = I_{REF} = \frac{1}{2} (\mu_p C_{ox}) \left(\frac{W}{L} \right)_3 |V_{OV3}|^2 = 0.1 \text{mA} \quad |V_{OV3}|^2 = 2 \frac{0.1 \text{mA}}{(\mu_p C_{ox}) \left(\frac{W}{L} \right)_3} = \frac{0.2 \text{mA}}{\left(65 \frac{\mu\text{A}}{\text{V}^2} \right) \left(\frac{4}{0.4} \right)} \quad |V_{OV3}| = 0.55 \text{V}$$

$$I_{D1} = I_{REF} = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right)_1 |V_{OV1}|^2 = 0.1 \text{mA} \quad |V_{OV1}|^2 = 2 \frac{0.1 \text{mA}}{(\mu_n C_{ox}) \left(\frac{W}{L} \right)_1} = \frac{0.2 \text{mA}}{\left(200 \frac{\mu\text{A}}{\text{V}^2} \right) \left(\frac{4}{0.4} \right)} \quad |V_{OV1}| = 0.32 \text{V}$$

point A

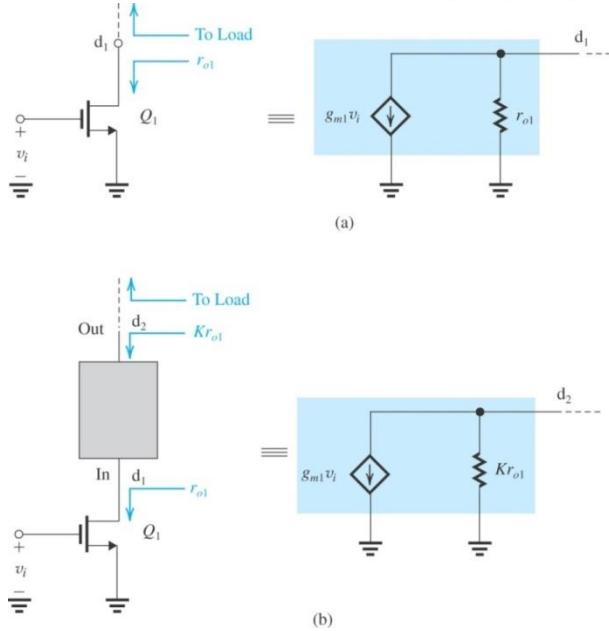
$$V_{OA} = V_{DD} - |V_{OV3}| = 2.45 \text{V}$$

point B

$$V_{OB} = V_{OV1} = 0.32 \text{V}$$



Increasing the Gain of the Basic Cell



We could increase the gain by increasing the resistance while passing the current – i.e. a **current buffer**.

Two important comments:

1. It is not sufficient to raise the output resistance of the amplifying transistor only. We also need to raise the output resistance of the current-source load. Obviously, we can use a current buffer to do this also.
2. Placing a CG (or a CB) circuit on top of the CS (or CE) amplifying transistor to implement the current-buffering action is called **cascoding**.

Figure 8.17 To increase the voltage gain realized in the basic gain cell shown in (a), a functional block, shown as a black box in (b), is connected between d_1 and the load. This new block is required to pass the current $g_m v_i$ right through but raise the resistance level by a factor K . The functional block is a current buffer and can be realized with a common-gate transistor, as demonstrated in the next section.



8.4 THE COMMON-GATE AND COMMON-BASE AMPLIFIERS



The Common Gate (CG) Circuit

Input Resistance

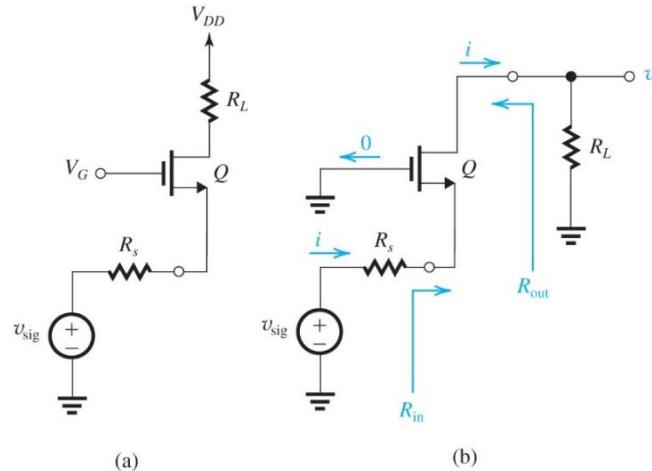


Figure 8.18 (a) A CG amplifier with the bias arrangement only partially shown. (b) The circuit with the dc sources eliminated.

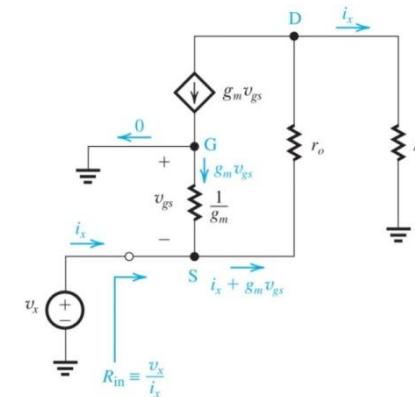


Figure 8.19 Determining the input resistance R_{in} of the CG amplifier.

$$R_{in} \equiv \frac{v_x}{i_x} = \frac{r_o + R_L}{1 + g_m r_o}$$

If $g_m r_o \gg 1$

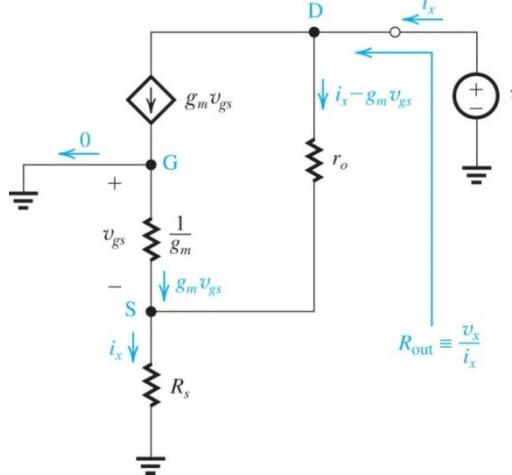
$$R_{in} \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o}$$

$$R_{in} \equiv \frac{v_x}{i_x}$$

$$\begin{aligned} v_x &= (i_x + g_m v_{gs}) r_o + i_x R_L \\ &= (i_x - g_m v_x) r_o + i_x R_L \\ &= \frac{i_x (r_o + R_L)}{1 + g_m r_o} \end{aligned}$$



CG Output Resistance



$$R_{out} \equiv \frac{v_x}{i_x}$$

Output Resistance

$$\begin{aligned}v_x &= (i_x - g_m v_{gs}) r_o + i_x R_s \\&= (i_x + g_m i_x R_s) r_o + i_x R_s \\&= i_x (r_o + g_m r_o R_s + R_s)\end{aligned}$$

$$\begin{aligned}R_{out} &\equiv \frac{v_x}{i_x} = r_o + R_s + g_m r_o R_s \\&= r_o + (1 + g_m r_o) R_s\end{aligned}$$

If $g_m r_o \gg 1$

$$R_{out} \approx r_o + g_m r_o R_s \approx (g_m r_o) R_s$$

Figure 8.20 Determining the output resistance R_{out} of the CG amplifier.



Impedance Transformation

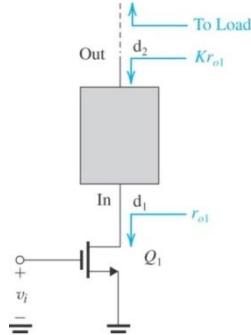


Figure 8.17

To summarize:

- the CG circuit has a unity current gain;
- a low input resistance, obtained by dividing R_L by $g_m r_o$;
- and a high output resistance, obtained by multiplying R_s by $g_m r_o$.

Thus it makes for an excellent current buffer and can be used to implement the shaded functional box in Fig. 8.17. As a useful summary, Fig. 8.21 illustrates the impedance transformation properties of the common-gate amplifier.

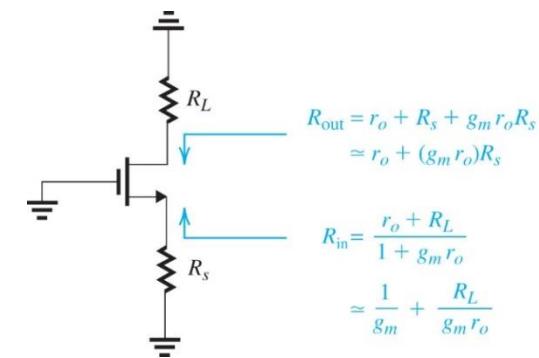
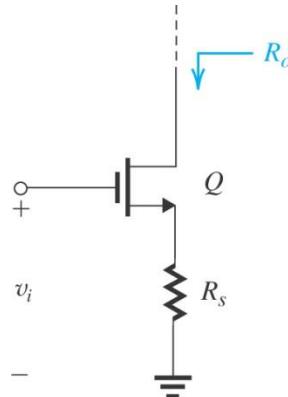


Figure 8.21 The impedance transformation properties of the common-gate amplifier. Depending on the values of R_s and R_L , we can sometimes write $R_{in} \approx R_L/(g_m r_o)$ and $R_o \approx (g_m r_o)R_s$. However, such approximations are not always justified.



Output Resistance of a Source-Degenerated Common Source Amplifier



$$\begin{aligned}R_o &= R_s + r_o + g_m r_o R_s \\&\simeq (1 + g_m R_s) r_o\end{aligned}$$

Figure 8.22 The output resistance expression of the CG amplifier can be used to find the output resistance of a source-degenerated common-source amplifier. Here, a useful interpretation of the result is that R_s increases the output resistance by the factor $(1 + g_m R_s)$.

$$R_o = R_s + r_o + g_m r_o R_s$$

$$\text{Since } g_m r_o \gg 1 \quad R_o \simeq (1 + g_m R_s) r_o$$

Thus source degeneration increases the output resistance of the CS amplifier from r_o to $(1 + g_m R_s) r_o$

In Chapter 11, we will find that R_s introduces negative (degenerative) feedback of an amount $(1 + g_m R_s)$.



The Body Effect

Since in the CG amplifier the source cannot be connected to the substrate, the body effect plays a role in the operation. Taking the body effect into account in the analysis of the CG circuit is a very simple matter. Refer to Fig. 8.23(a) and recall that the body terminal acts as another gate for the MOSFET. Thus, just as a signal voltage v_{gs} between the gate and the source gives rise to a drain current signal $g_m v_{gs}$, a signal voltage v_{bs} between the body and the source gives rise to a drain current signal $g_{mb} v_{bs}$. Thus the drain signal current becomes $(g_m v_{gs} + g_{mb} v_{bs})$, where the body transconductance g_{mb} is a small fraction χ of g_m ; $g_{mb} = \chi g_m$ and $\chi = 0.1$ to 0.2 . For the CG circuit, $v_{bs} = v_{gs}$, thus the two current signals can be combined as $(g_m + g_{mb})v_{gs}$ or $g_m(1 + \chi)v_{gs}$. Thus, the body effect can be taken into account by simply replacing g_m by $g_m(1 + \chi)$ as illustrated in the T equivalent model shown in Fig. 8.23(b). Normally, however, we will not bother with the factor $(1 + \chi)$ in our calculations.

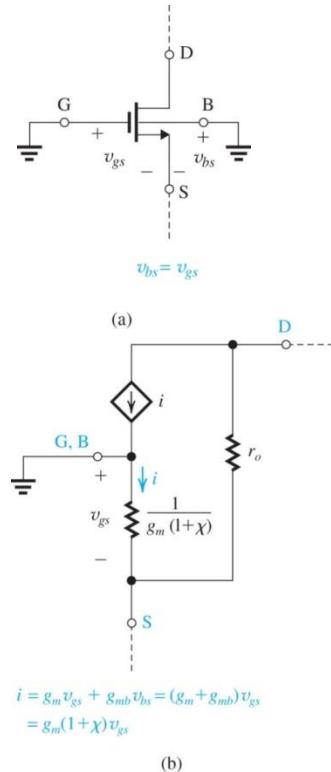


Figure 8.23 The body effect can be easily taken into account in the analysis of the CG circuit by replacing g_m by $(1 + \chi)g_m$, where $\chi = g_{mb}/g_m = 0.1$ to 0.2 .



The Common Base (CB) Circuit

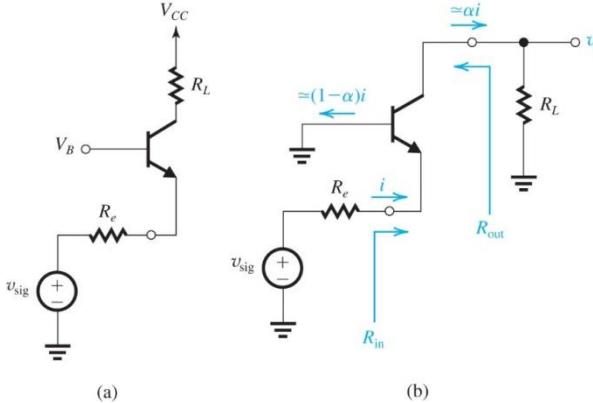
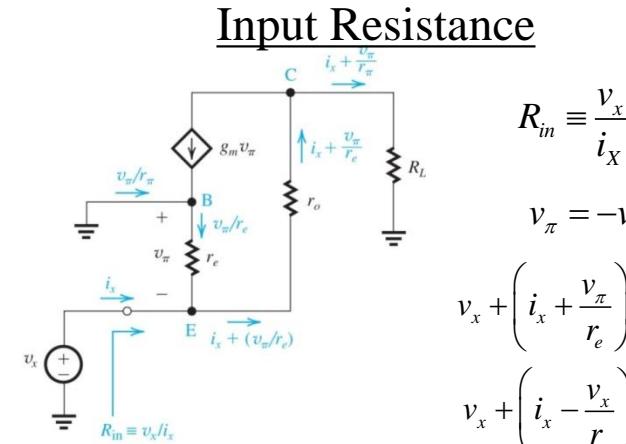


Figure 8.24 (a) A CB amplifier with the bias arrangement only partially shown. (b) The circuit with the dc sources eliminated.

$$R_{in} \equiv \frac{v_x}{i_x} = \frac{r_o + R_L}{1 + \frac{r_o}{r_e} + \frac{R_L}{r_\pi}} = \frac{r_o + R_L}{1 + \frac{r_o}{r_e} + \frac{R_L}{(\beta+1)r_e}}$$

$$R_{in} \approx r_e \frac{r_o + R_L}{r_o + \frac{R_L}{(\beta+1)}}$$



$$R_{in} \equiv \frac{v_x}{i_x}$$

$$v_\pi = -v_x$$

$$v_x + \left(i_x + \frac{v_\pi}{r_e} \right) r_o + \left(i_x + \frac{v_\pi}{r_\pi} \right) R_L = 0$$

$$v_x + \left(i_x - \frac{v_x}{r_e} \right) r_o + \left(i_x - \frac{v_x}{r_\pi} \right) R_L = 0$$

Figure 8.25 Determining the input resistance R_{in} of the CB amplifier.

Note: If $r_o = \infty$ then $R_{in} = r_e$;

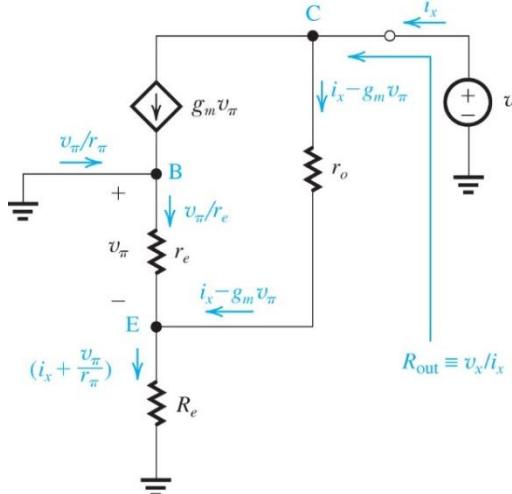
If $R_L = 0$ then $R_{in} = r_e$;

$$R_{in}|_{\max} = (\beta+1)r_e = r_\pi \text{ when } R_L = \infty$$



The Common Base (CB) Circuit

Output Resistance



$$R_{out} \equiv \frac{v_x}{i_x}$$

$$\begin{aligned} R_{out} &\equiv \frac{v_x}{i_x} = r_o + (R_e \parallel r_\pi) + (R_e \parallel r_\pi) g_m r_o \\ &= r_o + (1 + g_m r_o)(R_e \parallel r_\pi) \end{aligned}$$

If $g_m r_o \gg 1$

$$R_{out} \approx r_o + g_m r_o (R_e \parallel r_\pi)$$

$$R_{out}|_{\max} = r_o + g_m r_o r_\pi = (\beta + 1) r_o$$

Figure 8.26 Determining the output resistance R_{out} of the CB amplifier.

The CB circuit has a current gain of nearly unity, a relatively low input resistance, and a high output resistance; thus it makes for an excellent current buffer.



CG/CB Impedance Transformation

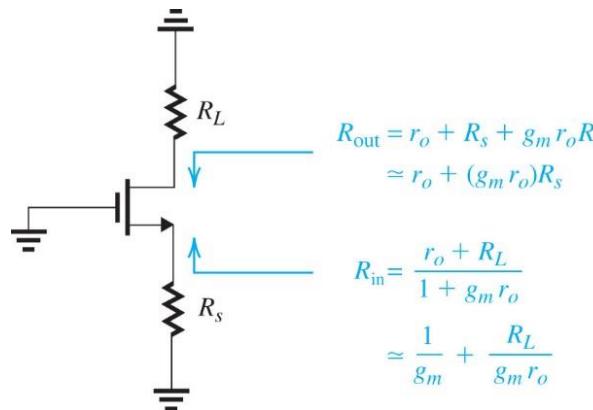


Figure 8.21 The impedance transformation properties of the common-gate amplifier. Depending on the values of R_s and R_L , we can sometimes write $R_{\text{in}} \approx R_L/(g_m r_o)$ and $R_o \approx (g_m r_o)R_s$. However, such approximations are not always justified.

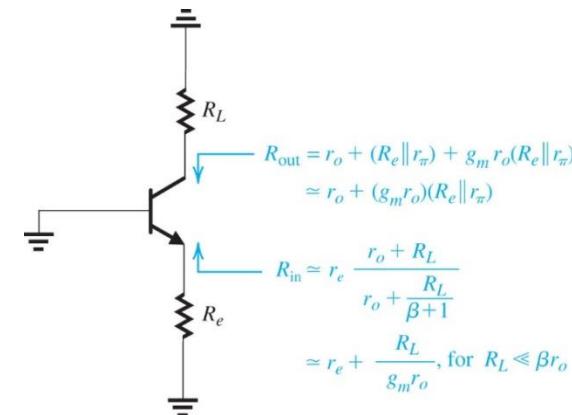
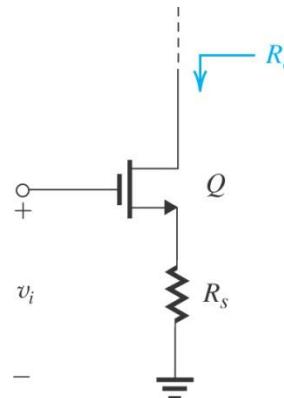


Figure 8.27 The impedance transformation properties of the CB amplifier. Note that for $\beta = \infty$, these formulas reduce to those for the MOSFET case (Fig. 8.21).



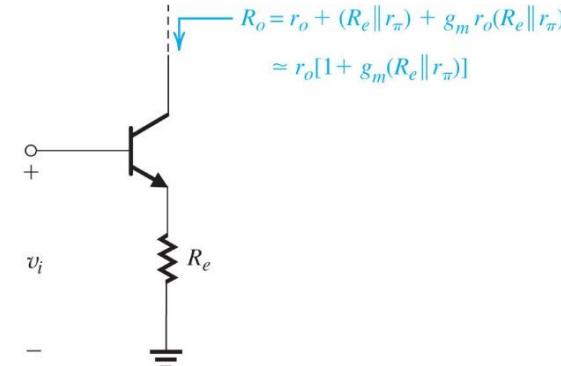
Output Resistance of Degenerated CS/CE Amplifiers



$$R_o = R_s + r_o + g_m r_o R_s \\ \simeq (1 + g_m R_s) r_o$$

Figure 8.22 The output resistance expression of the CG amplifier can be used to find the output resistance of a source-degenerated common-source amplifier. Here, a useful interpretation of the result is that R_s increases the output resistance by the factor $(1 + g_m R_s)$.

$$R_o \simeq (1 + g_m R_s) r_o$$



$$R_o = r_o + (R_e \parallel r_\pi) + g_m r_o (R_e \parallel r_\pi) \\ \simeq r_o [1 + g_m (R_e \parallel r_\pi)]$$

Figure 8.28 Output resistance of a CE amplifier with an emitter resistance R_e .

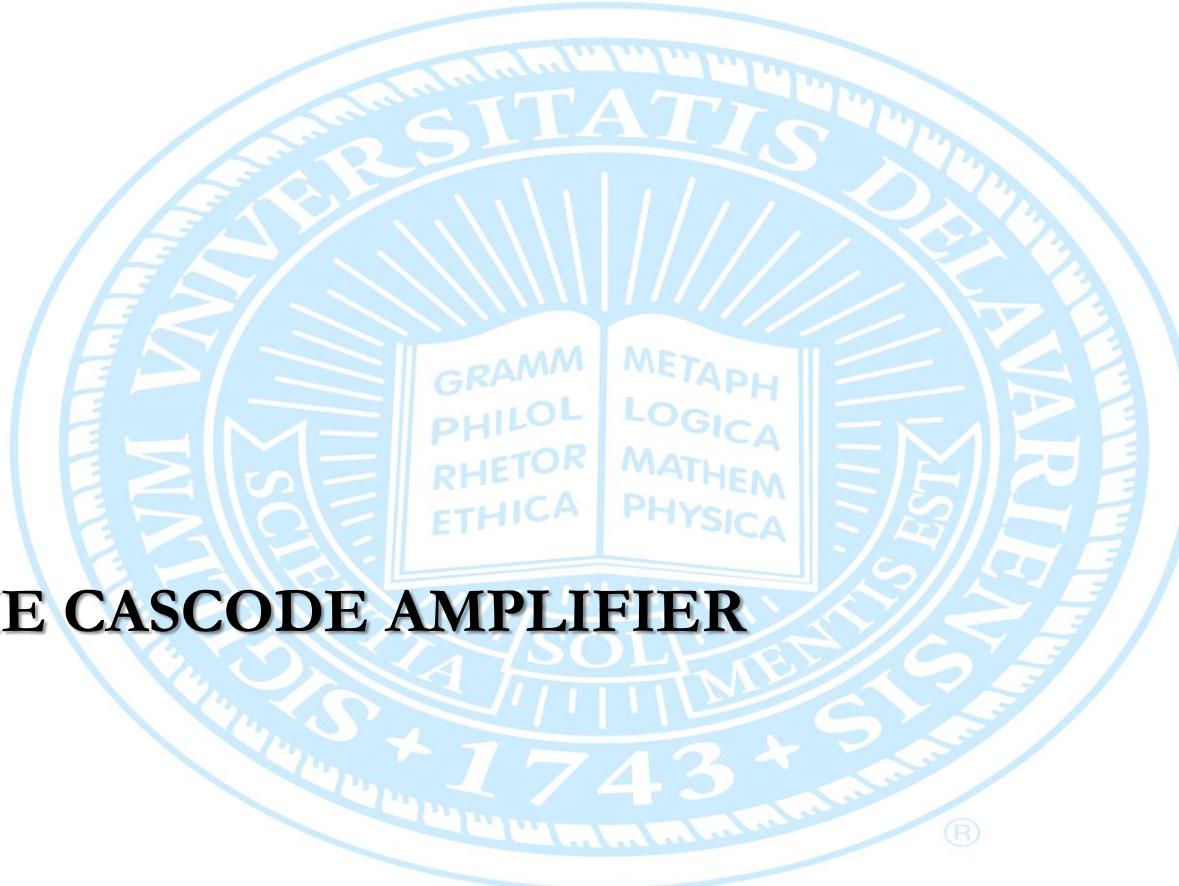
$$R_o \simeq r_o + g_m r_o (R_e \parallel r_\pi) \\ = [1 + g_m (R_e \parallel r_\pi)] r_o$$



End Lecture #2

No Homework Problems for Labor Day weekend

Finish reading Chapter 8



8.5 THE CASCODE AMPLIFIER

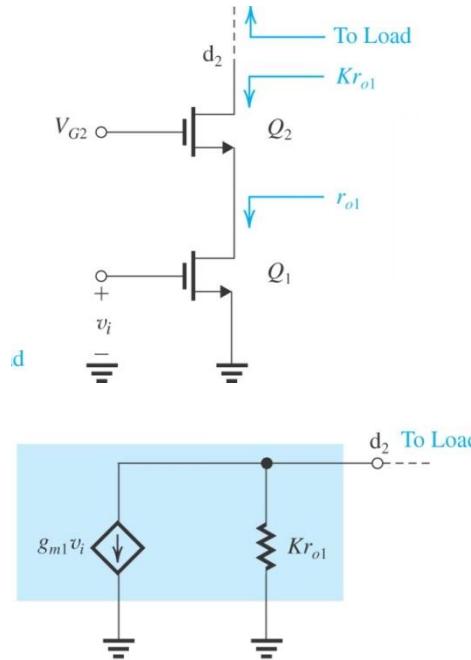


Figure 8.29 The current-buffering action of Fig. 8.17(b) is implemented using a transistor Q_2 connected in the CG configuration. Here V_{G2} is a dc bias voltage. The output equivalent circuit indicates that the CG transistor passes the current $g_{m1}v_i$ through but raises the resistance level by a factor K . Transistor Q_2 is called a cascode transistor.

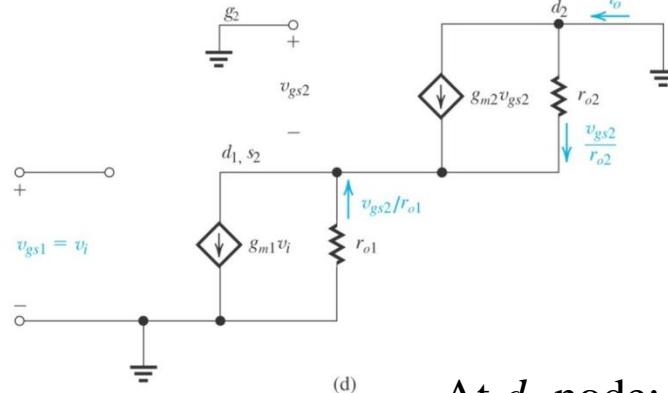
Cascoding

Cascoding refers to the use of a transistor connected in the common-gate (or the common-base) configuration to provide current buffering for the output of a common-source (or a common-emitter) amplifying transistor.

Figure 8.29 illustrates the technique for the MOS case. Here the CS transistor Q_1 is the amplifying transistor and Q_2 connected in the CG configuration with a dc bias voltage V_{G2} , (signal ground) at its gate, is the cascode transistor.



The MOS Cascode (finding G_m)



At d_1, s_2 node:

$$g_{m2}v_{gs2} + \frac{v_{gs2}}{r_{o1}} + \frac{v_{gs2}}{r_{o2}} = g_{m1}v_i$$

$$v_{gs2} \left(g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right) = g_{m1}v_i$$

If $g_{m2} \gg r_{o1}^{-1}, r_{o2}^{-2}$ then $g_{m2}v_{gs2} \approx g_{m1}v_i$

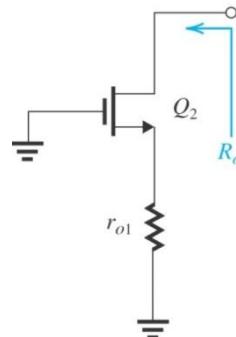
At d_2 node:

$$i_o = g_{m2}v_{gs2} + \frac{v_{gs2}}{r_{o2}} = v_{gs2} \left(g_{m2} + \frac{1}{r_{o2}} \right)$$

$$\approx g_{m2}v_{gs2} = g_{m1}v_i$$

$$\Rightarrow G_m \equiv \frac{i_o}{v_i} = g_{m1}$$

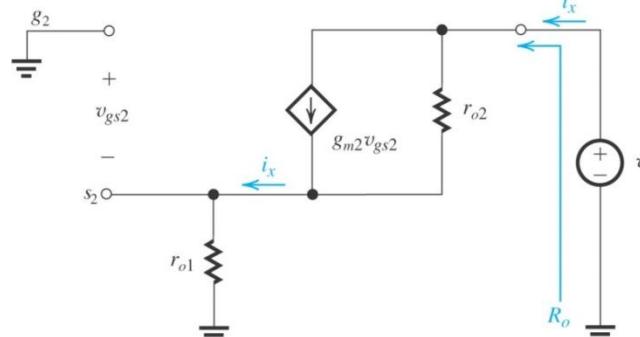
The CG transistor Q_2 doesn't change the overall transconductance of the CS amplifier



$$R_{out} \equiv \frac{v_x}{i_x}$$

$$-v_{gs2} = i_x r_{o1}$$

$$\begin{aligned} v_x &= (i_x - g_{m2}v_{gs2})r_{o2} + i_x r_{o1} \\ &= i_x(r_{o1} + r_{o2} + g_{m2}r_{o2}r_{o1}) \end{aligned}$$



(b)

The MOS Cascode (finding R_o)

$$\begin{aligned} R_{out} &\equiv \frac{v_x}{i_x} = \frac{i_x(r_{o1} + r_{o2} + g_{m2}r_{o2}r_{o1})}{i_x} \\ &= r_{o1} + r_{o2} + g_{m2}r_{o2}r_{o1} \\ &\approx (g_{m2}r_{o2})r_{o1} = A_{02}r_{o1} \end{aligned}$$

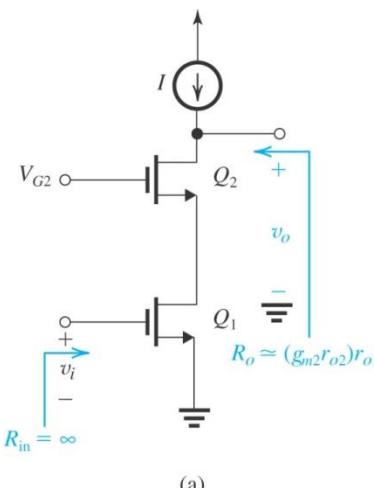
The CG transistor Q_2 raises the output resistance of the amplifier by the factor A_{02}



The MOS Cascode (finding A_{vo})

$$A_{vo} \equiv \frac{v_o}{v_i} = -G_m R_o = -g_{m1} R_o \approx -g_{m1} (g_{m2} r_{o2}) r_{o1}$$

$$A_{vo} = -(g_{m1} r_{o1})(g_{m2} r_{o2})$$



For the case $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$

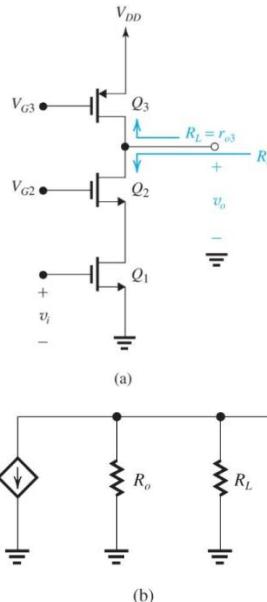
$$A_{vo} = -(g_m r_o)^2 = -A_0^2$$

The CG/cascode transistor Q_2 raises the gain magnitude of the amplifier from A_0 to A_0^2

Figure 8.30 (a) A MOS cascode amplifier with an ideal current-source load; (b) equivalent circuit representation of the cascode output.



Implementation of the Constant-Current Source Load



If the current source load is implemented with a PMOS transistor (which can be part of a PMOS current mirror) as shown in Fig. 8.31(a), the load resistance R_L will be equal to the output resistance of Q_3 , r_{o3} ,

$$R_L = r_{o3}$$

$$A_v = -g_{m1} (R_o \parallel R_L) = -g_{m1} \{ [(g_{m2} r_{o2}) r_{o1}] \parallel r_{o3} \}$$

since $R_o \gg R_L$

$$A_v \approx -g_{m1} r_{o3} \Rightarrow |A_v| \approx A_0$$

The gain magnitude will be back to A_0 , of the same order as that realized by a CS amplifier. In other words, the use of a simple current-source load with a relatively low output resistance has in effect destroyed the cascoding advantage of increased output resistance. Nevertheless, it turns out that this cascode amplifier exhibits a much wider bandwidth (Chapter 10).

Figure 8.31 (a) A MOS cascode amplifier loaded in a simple PMOS current source Q_3 .
(b) Equivalent circuit at the amplifier output.



Cascoding the Current Source

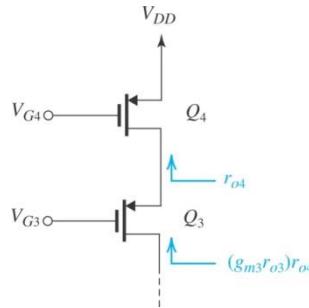


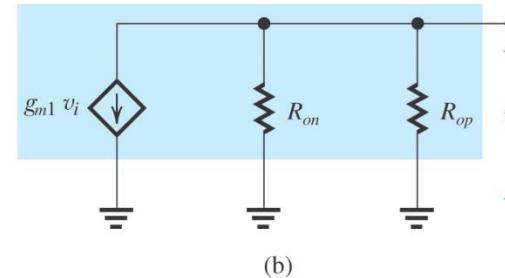
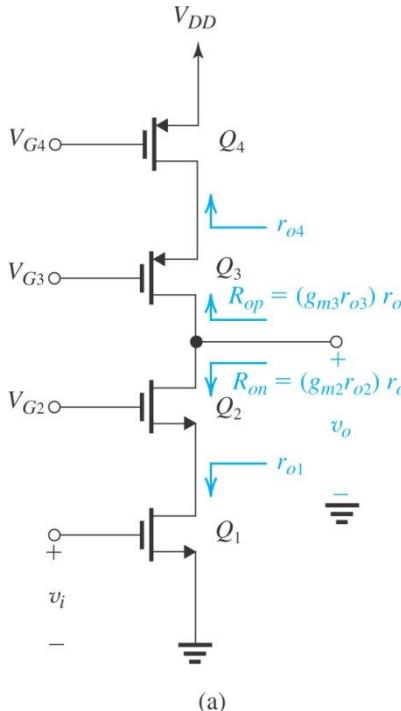
Figure 8.32 Employing a cascode transistor Q_3 to raise the output resistance of the current source Q_4 .

Cascoding can also be employed to raise the output resistance of the current-source load as shown in Fig. 8.32. Here Q_4 is the current-source transistor, and Q_3 is the CG cascade transistor. Voltages V_{G3} and V_{G4} are dc bias voltages. The cascade transistor Q_3 multiplies the output resistance of Q_4 , r_{o4} by $(g_{m3}r_{o3})$ to provide an output resistance for the cascade current source of:

$$R_o = (g_{m3}r_{o3})r_{o4}$$



Cascode Amplifier with Cascode Current Source



$$R_{on} = (g_{m2} r_{o2}) r_{o1}$$

$$R_{op} = (g_{m3} r_{o3}) r_{o4}$$

$$A_v \equiv \frac{v_o}{v_i} = -g_{m1} [R_{on} \parallel R_{op}]$$

$$= -g_{m1} [(g_{m2} r_{o2}) r_{o1} \parallel (g_{m3} r_{o3}) r_{o4}]$$

If all transistors are identical:

$$A_v = -\frac{1}{2} (g_m r_o)^2 = -\frac{1}{2} A_0^2$$

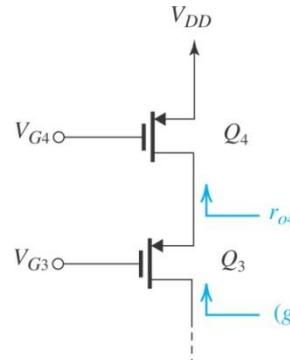
The cascode amplifier with cascaded current-source load increases the gain by a factor of A_0 versus a CS amp with current source load

Figure 8.33 A cascode amplifier with a cascode current-source load.



Example 8.5a

It is required to design the cascode current-source of Fig. 8.32 to provide a current of 100 uA and an output resistance of 500 kΩ. Assume the availability of a 0.18-um CMOS technology for which $V_{DD} = 1.8$ V, $V_{tp} = -0.5$ V, $\mu_p C_{ox} = 90$ uA/V² and $V'_A = -5$ V/um. Use $|V_{OV}| = 0.3$ V and determine L and W/L for each transistor, and the values of the bias voltages V_{G3} and V_{G4} .



$$R_{op} = (g_{m3}r_{o3})r_{o4} \quad \text{If } Q_3 = Q_4$$

$$R_{op} = (g_m r_o) r_o = \frac{|V_A|}{|V_{OV}|/2} \times \frac{|V_A|}{I_D}$$

$$500\text{k}\Omega = \frac{|V_A|}{0.15\text{V}} \times \frac{|V_A|}{0.1\text{mA}}$$

$$|V_A| = 2.74\text{V}$$

$$|V_A| = |V'_A|L$$

$$L = \frac{2.74\text{V}}{5\text{V}} = 0.55\text{um}$$

$$I_D = \frac{1}{2} (\mu_p C_{ox}) \left(\frac{W}{L} \right) |V_{OV}|^2 \left(1 + \frac{V_{SD}}{|V_A|} \right)$$

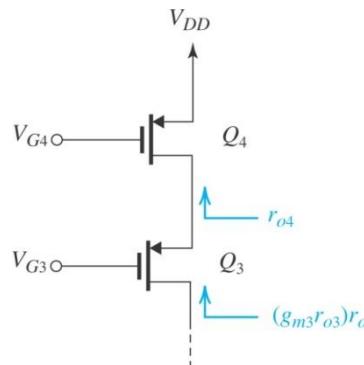
$$100\text{uA} = \frac{1}{2} \times 90 \frac{\text{uA}}{\text{V}^2} \times \left(\frac{W}{L} \right) 0.3^2 \text{V}^2 \left(1 + \frac{0.3\text{V}}{2.74\text{V}} \right)$$

$$\frac{W}{L} = 22.3$$



Example 8.5b

It is required to design the cascode current-source of Fig. 7.10 to provide a current of 100 uA and an output resistance of 500 kΩ. Assume the availability of a 0.18-um CMOS technology for which $V_{DD} = 1.8$ V, $V_{tp} = -0.5$ V, $\mu_p C_{ox} = 90$ uA/V² and $V_A' = -5$ V/um. Use $|V_{ov}| = 0.3$ V and determine L and W/L for each transistor, and the values of the bias voltages V_{G3} and V_{G4} .



$$V_{SG4} = |V_t| + |V_{ov}| = 0.8\text{V}$$

$$V_{G4} = V_{DD} - V_{SG4} = 1.0\text{V}$$

$$V_{G3} = V_{DD} - |V_{ov}| - V_{SG3} = 0.7\text{V}$$



Distribution of Voltage Gain in a Cascode Amplifier

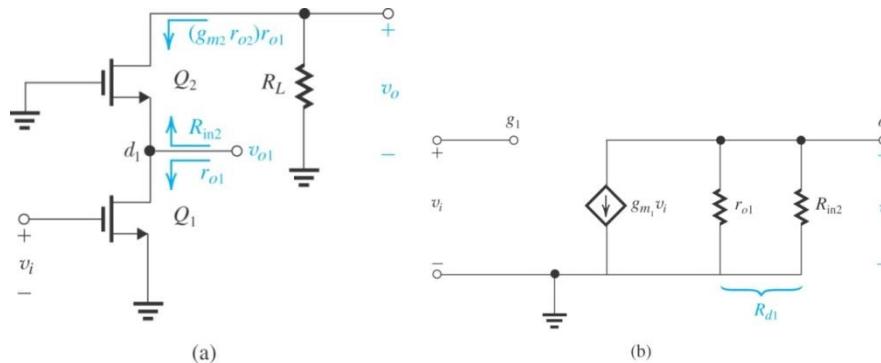


Figure 8.34 (a) The cascode amplifier with a load resistance R_L . Only signal quantities are shown. (b) Determining v_{o1} .

$$\begin{aligned} A_v &= -g_{m1} [R_O \parallel R_L] \\ &= -g_{m1} [(g_{m2}r_{o2})r_{o1} \parallel R_L] \end{aligned}$$

$$A_v = A_{v1}A_{v2} = \left(\frac{v_{o1}}{v_i} \right) \left(\frac{v_o}{v_{o1}} \right)$$

$$A_{v1} = \left(\frac{v_{o1}}{v_i} \right) = -g_{m1}R_{d1} = -g_{m1}(r_{o1} \parallel R_{in2})$$

$$R_{in2} \approx \frac{R_L}{g_{m2}r_{o2}} + \frac{1}{g_{m2}}$$

$$\begin{aligned} A_{v2} &= \frac{A_v}{A_{v1}} = \frac{-g_{m1}[(g_{m2}r_{o2})r_{o1} \parallel R_L]}{-g_{m1}(r_{o1} \parallel R_{in2})} = \frac{(g_{m2}r_{o2})r_{o1} \parallel R_L}{\left[r_{o1} \parallel \left(\frac{R_L}{g_{m2}r_{o2}} + \frac{1}{g_{m2}} \right) \right]} \end{aligned}$$



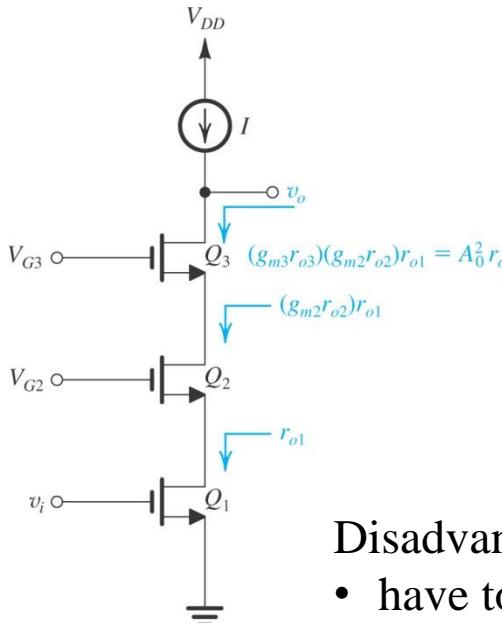
Table 8.1 MOS Cascode Amplifier

$$r_{o1} = r_{o2} = r_o$$

Case	R_L	R_{in2}	R_{d1}	A_{v1}	A_{v2}	A_v
1. Ideal current source load	∞	∞	r_o	$-g_m r_o$	$g_m r_o$	$-(g_m r_o)^2$ $= -A_0^2$
2. Cascode current source load	$(g_m r_o) r_o$	r_o	$\frac{r_o}{2}$	$-\frac{g_m r_o}{2}$	$g_m r_o$	$-\frac{(g_m r_o)^2}{2}$ $= -\frac{A_0^2}{2}$
3. Simple current source load	r_o	$\frac{2}{g_m}$	$\frac{2}{g_m}$	-2	$\frac{g_m r_o}{2}$	$-g_m r_o$ $= -A_0$
4. Output short circuit load	0	$\frac{1}{g_m}$	$\frac{1}{g_m}$	-1	0	0



Double Cascoding



If a still higher output resistance and correspondingly higher gain are required, it is possible to add another level of cascoding, as illustrated in Fig. 8.35. Observe that Q_3 is the second cascode transistor, and it raises the output resistance by $(g_{m3}r_{o3})(g_{m2}r_{o2})r_{o1} = A_0^2 r_o$. For the case of identical transistors, the output resistance will be $(g_m r_o)^2 r_o$ and the voltage gain, assuming an ideal current source load, will be $(g_m r_o)$ or A_0 . Of course, we have to generate another dc bias voltage for the second cascode transistor, Q_3 .

Disadvantages:

- have to generate another dc bias voltage for Q_3 .
- current-source load will also need to use double cascoding with an additional transistor.
- Requires a higher V_{DD} since a certain minimum V_{DS} (at least equal to V_{OV}), is required to be in saturation mode.

Figure 8.35 Double cascoding.



The Folded Cascode

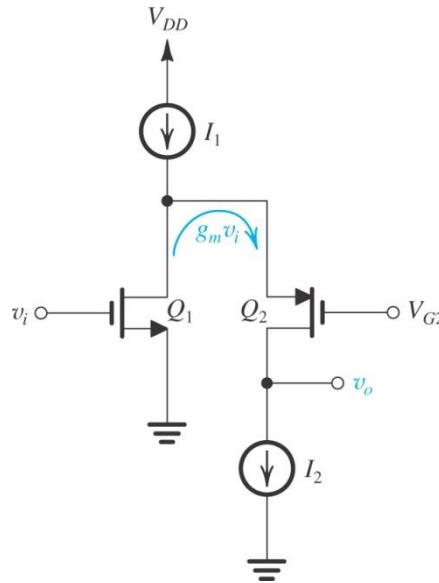
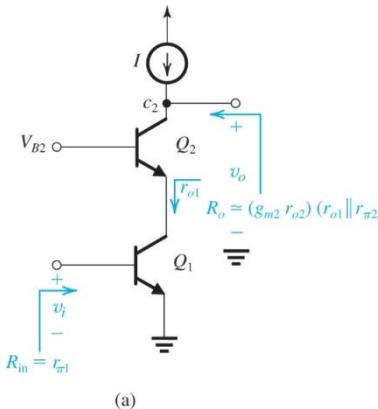


Figure 8.36 The folded cascode.

To avoid the problem of stacking a large number of transistors across a low-voltage power supply, one can use a PMOS transistor for the cascode device, as shown in Fig. 8.36. Here, as before, the NMOS transistor Q_1 is operating in the CS configuration, but the CG stage is implemented using the PMOS transistor Q_2 . An additional current source I_2 is needed to bias Q_2 and provide it with its active load. Note that Q_1 is now operating at a bias current of $(I_1 - I_2)$. Finally, a dc voltage V_{G2} is needed to provide an appropriate dc level for the gate of the cascode transistor Q_2 . Its value has to be selected so that Q_2 and Q_1 operate in the saturation region.



The BJT Cascode



The input resistance of the bipolar cascode amplifier is finite:

$$R_{in} = r_{\pi 1}$$

The output resistance is:

$$R_o \approx r_{o2} + (g_{m2} r_{o2})(r_{o1} \parallel r_{\pi 2}) = r_{o2} [1 + g_{m2}(r_{o1} \parallel r_{\pi 2})]$$

Since $g_m(r_{o1} \parallel r_{\pi 2}) \gg 1$

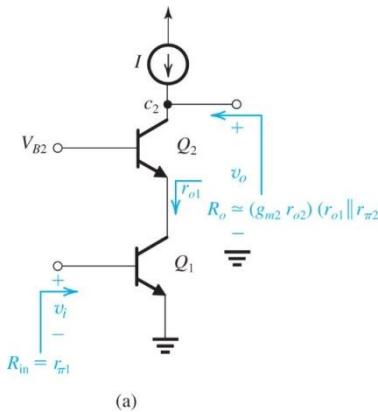
$$R_o \approx (g_{m2} r_{o2})(r_{o1} \parallel r_{\pi 2})$$

because of the finite β of the BJT, we have $r_{\pi 2}$ appearing in parallel with r_{o1} . This poses a very significant constraint on R_o of the BJT cascode.

$$R_o|_{max} = (g_{m2} r_{\pi 2}) r_{o2} = \beta_2 r_{o2}$$

Thus the maximum output resistance realizable by cascading is $\beta_2 r_{o2}$. This means that unlike the MOS case, double cascading with a BJT would not be useful.

Figure 8.37 (a) A BJT cascode amplifier with an ideal current-source load; (b) small-signal, equivalent-circuit representation of the output of the cascode amplifier.



The BJT Cascode

The open-circuit voltage gain of the bipolar cascode can be found using the equivalent circuit of Fig. 8.37(b) as

$$\begin{aligned} A_{vo} &= \frac{v_o}{v_i} = -g_{m1} R_o \\ &= -g_{m1} (g_{m2} r_{o2}) (r_{o1} \parallel r_{\pi2}) \end{aligned}$$

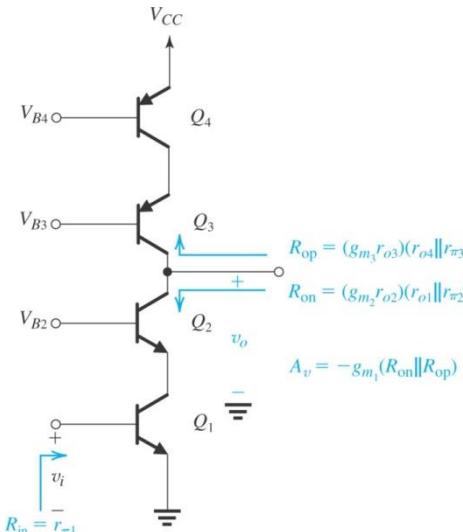
If $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$ then:

$$A_{vo} = -(g_m r_o) [g_m (r_o \parallel r_\pi)]$$

Figure 8.37 (a) A BJT cascode amplifier with an ideal current-source load; (b) small-signal, equivalent-circuit representation of the output of the cascode amplifier.



Cascode BJT Amplifier with Cascode Current Source



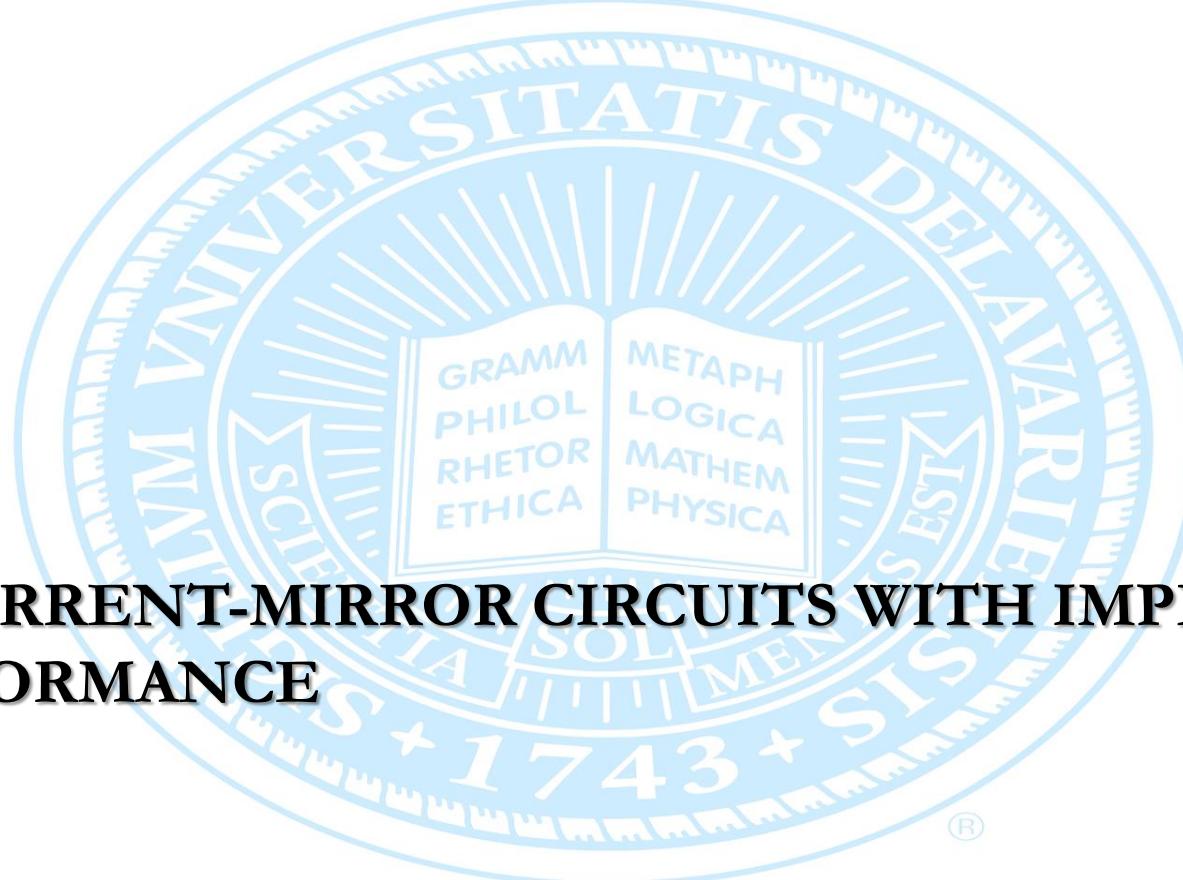
$$A_{vo} = -(g_m r_o) [g_m (r_o \parallel r_\pi)]$$

which will be less than $(g_m r_o)^2$ in magnitude. In fact, the maximum possible gain magnitude is obtained when $r_o \gg r_\pi$ and is given by

$$|A_{vo}|_{max} = \beta g_m r_o = \beta A_0$$

To be able to realize gains approaching this level the current-source load must also be cascaded. Figure 8.38 shows a cascode BJT amplifier with a cascode current-source load.

Figure 8.38 A BJT cascode amplifier with a cascode current source.



8.6 CURRENT-MIRROR CIRCUITS WITH IMPROVED PERFORMANCE

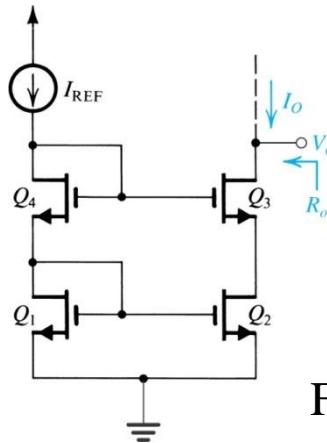


Figure 8.39 A cascode MOS current mirror.

Cascode Current Mirror

The accuracy of the current transfer ratio suffers particularly from the finite β of the BJT. The output resistance, which in the simple circuits is limited to r_o of the MOSFET and the BJT, also reduces accuracy and, much more seriously, severely limits the gain available from cascode amplifiers.

Figure 8.39 shows the basic cascode current mirror. Observe that in addition to the diode connected transistor Q_1 which forms the basic mirror Q_1-Q_2 , another diode-connected transistor, Q_4 , is used to provide a suitable bias voltage for the gate of the cascode transistor Q_3 . To determine the output resistance of the cascode mirror at the drain of Q_3 , we assume that the voltages across Q_1 and Q_4 are constant, and thus the signal voltages at the gates of Q_2 and Q_3 will be zero. Thus R_o will be that of the cascode current source formed by Q_2 and Q_3 , $R_o \approx g_{m3}r_{o3}r_{o2}$

Here the output resistance is increased by the factor $g_{m3}r_{o3}$.

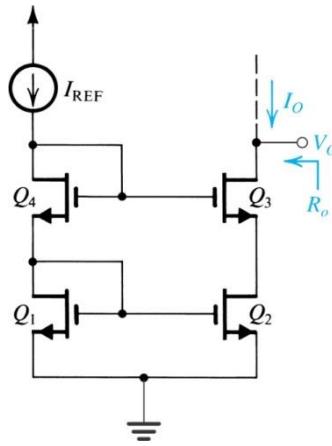


Figure 8.39 A cascode MOS current mirror.

Cascode Current Mirror

A drawback of the cascode current mirror is that it consumes a relatively large portion of the steadily shrinking supply voltage V_{DD} . While the simple MOS mirror operates properly with a voltage as low as V_{OV} across its output transistor, the cascode circuit of Fig. 8.39 requires a minimum voltage of $V_t + 2V_{OV}$. This is because the gate of Q_3 is at $2V_{GS} = 2V_t + 2V_{OV}$. Thus the minimum voltage required across the output of the cascode mirror is 1 V or so. This obviously limits the signal swing at the output of the mirror (i.e., at the output of the amplifier that utilizes this current source as a load).



The Wilson BJT Current Mirror

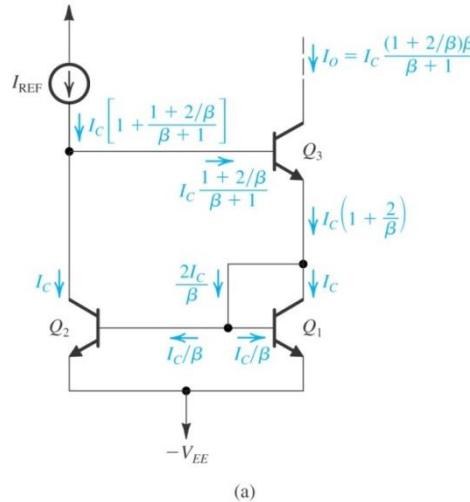


Figure 8.40 The Wilson bipolar current mirror: (a) circuit showing analysis to determine the current transfer ratio;

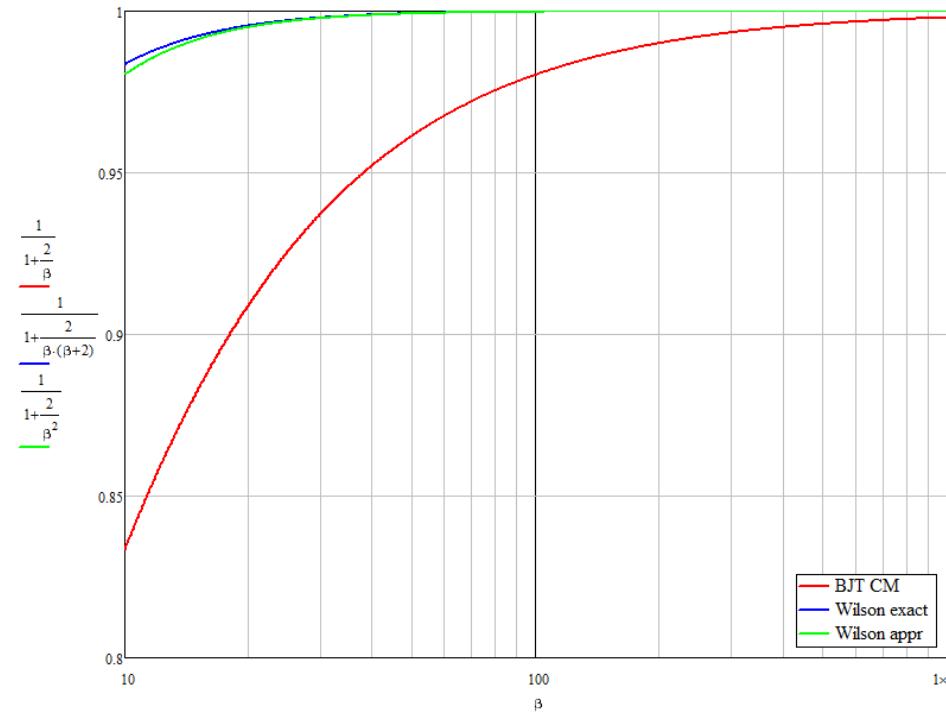
$$\frac{I_O}{I_{REF}} = \frac{1}{\left(1 + \frac{2}{\beta}\right)} \quad \text{Standard BJT current mirror}$$

$$\begin{aligned} \frac{I_O}{I_{REF}} &= \frac{I_C \left(1 + \frac{2}{\beta}\right) \beta / (\beta + 1)}{I_C \left[1 + \left(1 + \frac{2}{\beta}\right) / (\beta + 1)\right]} \\ &= \frac{1}{1 + \frac{2}{\beta(\beta + 2)}} \approx \frac{1}{1 + \frac{2}{\beta^2}} \quad \text{Wilson BJT current mirror} \end{aligned}$$

assuming that Q_1 and Q_2 conduct equal collector currents. There is, however, a slight problem with this assumption: The collector-to-emitter voltages of Q_1 and Q_2 are not equal, which introduces a current offset or a systematic error. The problem can be solved by adding a diode-connected transistor in series with the collector of Q_2 .



Wilson BJT 1:1 Current Mirror





The Wilson BJT Current Mirror

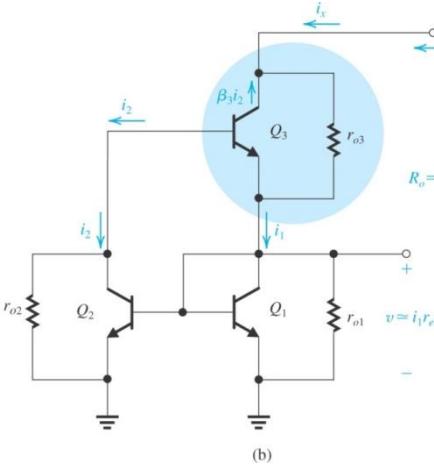
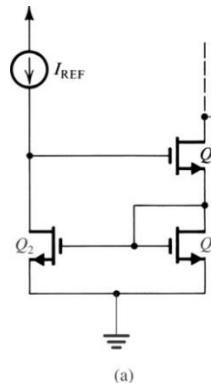


Figure 8.40 The Wilson bipolar current mirror: (b) determining the output resistance.

To determine the output resistance of the Wilson mirror, we set $I_{\text{REF}} = 0$ and apply a test voltage v_x to the output node, as shown in Fig. 8.40(b). The circuit can be analyzed to show (Sedra and Smith page 561-562) that the output resistance is: $R_o = \beta_3 r_{o3}/2$

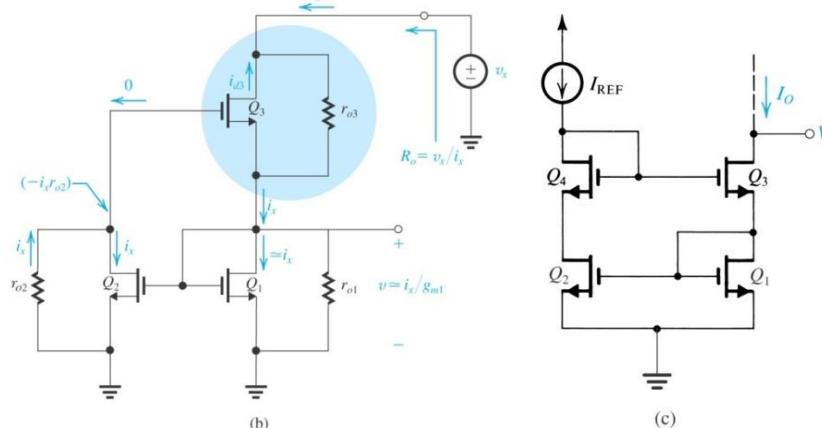
The Wilson current mirror has an output resistance $\beta_3/2$ times higher than that of Q_3 alone. This is a result of the negative feedback obtained by feeding the collector current of Q_2 (i_2) back to the base of Q_3 . This feedback results in increasing the current through r_{o3} to approximately $1/2\beta_3 i_x$, and thus the voltage across r_{o3} and the output resistance increase by the same factor, $1/2\beta_3$. The Wilson mirror is preferred over the cascode circuit because the latter has the same dependence on β as the simple mirror. However, like the cascode mirror, the Wilson mirror requires an additional V_{BE} drop for its operation.



$$R_o = (g_m r_{o3}) r_{o2}$$

Wilson MOS Mirror

The Wilson MOS mirror exhibits an increase of output resistance by a factor ($g_m r_{o3}$) an identical result to that achieved in the cascode mirror. Here the increase in R_o is a result of the negative feedback obtained by connecting the drain of Q_2 to the gate of Q_3 .



to balance the two branches of the mirror and thus avoid the systematic current error resulting from the difference in V_{DS} between Q_1 and Q_2 , the circuit can be modified as shown in Fig. 8.41(c).

Figure 8.41 The Wilson MOS mirror: (a) circuit; (b) analysis to determine output resistance; (c) modified circuit.

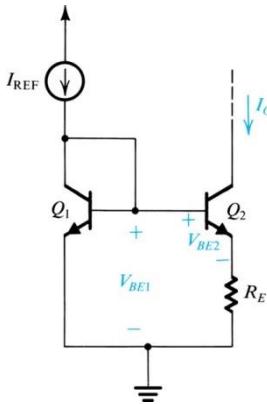


Figure 8.42 The Widlar current source.

The Widlar Current Source

The Widlar current source, is shown in Fig. 8.42. It differs from the basic current mirror circuit in that a resistor R_E is included in the emitter lead of Q_2 . Neglecting base currents and assuming the transistors are matched we can write

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right) \quad V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right)$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \quad V_{BE1} = V_{BE2} + I_O R_E$$

$$\Rightarrow I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$$

the Widlar circuit allows the generation of a small constant current using relatively small resistors. Another important characteristic is that its output resistance is high. The increase in the output resistance above that achieved in the basic current source is due to the emitter-degeneration resistance R_E .

$$R_{out} \approx [1 + g_m (R_E \parallel r_\pi)] r_o$$



Example 8.6

The two circuits for generating a constant current $I_O = 10 \mu\text{A}$ shown in Fig. 8.43 operate from a 10-V supply. Determine the values of the required resistors, assuming that V_{BE} is 0.7 V at a current of 1 mA and neglecting the effect of finite β .

basic current-source circuit

$$V_{BE1} = 0.7 + V_T \ln \left(\frac{10 \mu\text{A}}{1 \text{mA}} \right)$$

$$V_{BE1} = 0.58$$

$$R_1 = \frac{10 - 0.58}{0.01} = 942 \text{k}\Omega$$

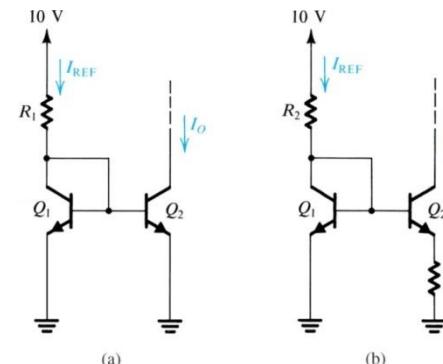


Figure 8.43 Circuits for Example 8.6.

Widlar current-source circuit

$$V_{BE1} = 0.7$$

$$R_1 = \frac{10 - 0.7}{1} = 9.3 \text{k}\Omega$$

$$I_O R_E = V_T \ln \left(\frac{I_{REF}}{I_O} \right)$$

$$R_3 = \frac{0.25 \ln \left(\frac{1 \text{mA}}{10 \mu\text{A}} \right)}{10 \times 10^{-6}}$$

$$R_3 = 11.5 \text{k}\Omega$$



8.7 SOME USEFUL TRANSISTOR PAIRINGS



Table 7.4 Characteristics of MOSFET Amplifiers

Amplifier type	R_{in}	A_{vo}	R_o	A_v	G_v
Common source	∞	$-g_m R_D$	R_D	$-g_m (R_D \parallel R_L)$	$\frac{-g_m (R_D \parallel R_L)}{1 + g_m R_S}$
Common source with R_S	∞	$\frac{g_m R_D}{1 + g_m R_S}$	R_D	$-\frac{g_m (R_D \parallel R_L)}{1 + g_m R_S}$	$-\frac{g_m (R_D \parallel R_L)}{1 + g_m R_S}$
Common gate	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m (R_D \parallel R_L)$	$\frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Common drain or source follower	∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$



Table 7.5 BJT Amplifier Summary

	R_{in}	A_{vo}	R_o	A_v	G_v
common emitter	$(\beta + 1)r_e$	$g_m R_C$	R_C	$-g_m(R_C \parallel R_L)$ $-\alpha \frac{R_C \parallel R_L}{r_e}$	$-\beta \frac{(R_C \parallel R_L)}{R_{sig} + (\beta + 1)r_e}$
common emitter with R_e	$(\beta + 1)(r_e + R_e)$	$-\frac{g_m R_C}{1 + g_m R_e}$	R_C	$-\frac{g_m(R_C \parallel R_L)}{1 + g_m R_e}$ $-\alpha \frac{R_C \parallel R_L}{r_e + R_L}$	$-\beta \frac{(R_C \parallel R_L)}{R_{sig} + (\beta + 1)(r_e + R_e)}$
common base	r_e	$g_m R_C$	R_C	$g_m(R_C \parallel R_L)$ $\alpha \frac{R_C \parallel R_L}{r_e}$	$\alpha \frac{R_C \parallel R_L}{R_{sig} + r_e}$
emitter follower	$(\beta + 1)(r_e + R_L)$	1	r_e	$\frac{R_L}{R_L + r_e}$	$\frac{R_L}{R_L + r_e + R_{sig}/(\beta + 1)}$ $G_{vo} = 1$ $R_{out} = r_e + \frac{R_{sig}}{\beta + 1}$



The IC Source Follower

Figure 8.45(a) shows a source follower formed by transistor Q_1 and biased by a constant-current supplied by the current mirror Q_2-Q_3 . Observe that since the source of Q_1 cannot be connected to the body (which is at signal ground potential) a voltage signal v_{bs} develops between body and source and gives rise to a current signal $g_{mb}v_{bs}$, as indicated in the equivalent circuit in Fig. 8.45(b). The equivalent circuit shows also the output resistance r_{o3} of the bias current source Q_3 , which acts as a load resistance for the follower Q_1 .

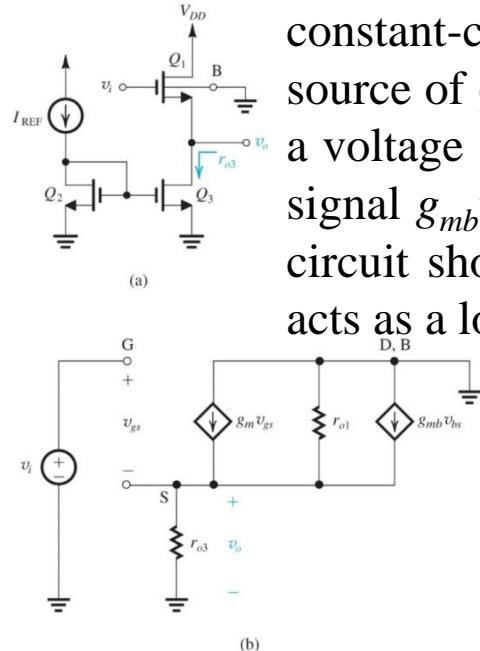


Figure 8.45 (a) A source follower biased with a current mirror Q_2-Q_3 and with the body terminal indicated. Note that the source cannot be connected to the body and thus the body effect should be taken into account. (b) Equivalent circuit.

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + \frac{1}{g_m}} \quad \text{where} \quad R_L = r_{o1} \parallel r_{o2} \parallel \frac{1}{g_{mb}}$$

$$\text{if } \frac{1}{g_{mb}} \ll r_{o1}, r_{o2} \Rightarrow R_L \simeq \frac{1}{g_{mb}} \quad \Rightarrow \frac{v_o}{v_i} \simeq \frac{g_{mb}}{g_m + g_{mb}}$$

$$g_{mb} = \chi g_m \quad \Rightarrow \frac{v_o}{v_i} \simeq \frac{1}{1 + \chi}$$



The CC-CE, CD-CS, and CD-CE Configurations

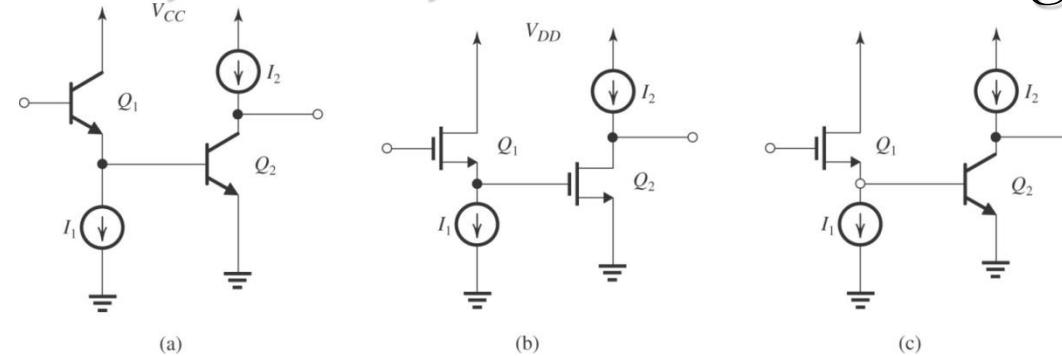


Figure 8.44 (a) CC-CE amplifier; (b) CD-CS amplifier; (c) CD-CE amplifier.

Figure 8.44(a) shows an amplifier formed by cascading a common-collector (emitter follower) transistor Q_1 with a common-emitter transistor Q_2 . This circuit has two main advantages over the CE amplifier. First, the emitter follower increases the input resistance by a factor equal to $(\beta_1 + 1)$. As a result, the overall voltage gain is increased, especially if the resistance of the signal source is large. Second, it will be shown in Chapter 10 that the CC-CE amplifier can exhibit much wider bandwidth than that obtained with the CE amplifier.



Example 8.7a

For the CC-CE amplifier in Fig. 8.44(a) let $I_1 = I_2 = 1 \text{ mA}$ and assume identical transistors with $\beta = 100$. Find the input resistance R_{in} and the overall voltage gain obtained when the amplifier is fed with a signal source having $R_{sig} = 4 \text{ k}\Omega$ and loaded with a resistance $R_L = 4 \text{ k}\Omega$. Compare the results with those obtained with a common-emitter amplifier operating under the same conditions. Ignore r_o .

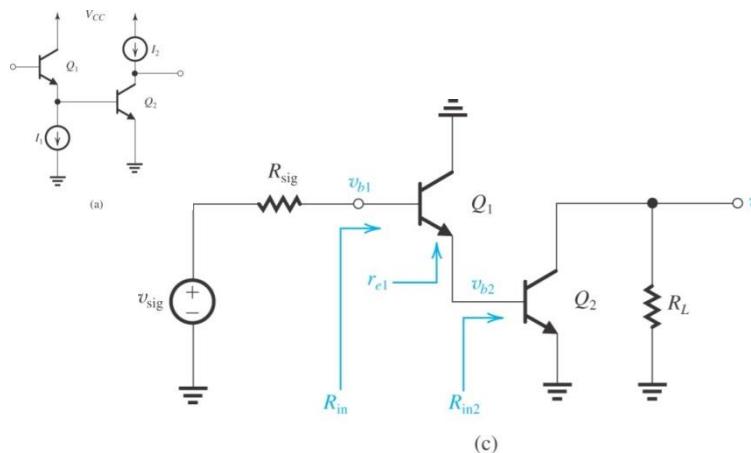


Figure 8.46 Circuit for Example 8.7.

$$g_m = \frac{I}{V_T} = \frac{1\text{mA}}{25\text{mV}} = 40\text{mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{40\text{mA/V}} = 2.5\text{k}\Omega$$

$$r_e \equiv \frac{v_{be}}{i_e} = \frac{V_T}{I_E} = \frac{25\text{mV}}{1\text{mA}} = 25\Omega$$

$$R_{in2} = r_{\pi2} = 2.5\text{k}\Omega$$

$$R_{in} = (\beta_1 + 1)(r_{e1} + R_{in2}) = 255\text{k}\Omega$$



Example 8.7b

For the CC-CE amplifier in Fig. 8.44(a) let $I_1 = I_2 = 1$ mA and assume identical transistors with $\beta = 100$. Find the input resistance R_{in} and the overall voltage gain obtained when the amplifier is fed with a signal source having $R_{sig} = 4$ k Ω and loaded with a resistance $R_L = 4$ k Ω . Compare the results with those obtained with a common-emitter amplifier operating under the same conditions. Ignore r_o .

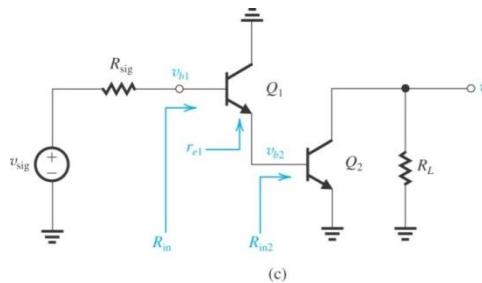


Figure 8.46 Circuit for Example 8.7.

For the CC-CE amplifier

$$\frac{v_{b1}}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{255\text{k}\Omega}{255\text{k}\Omega + 4\text{k}\Omega} = 0.98\text{V/V}$$

$$\frac{v_{b2}}{v_{b1}} = \frac{R_{in2}}{R_{in2} + r_{e1}} = \frac{2.5\text{k}\Omega}{2.5\text{k}\Omega + 0.025\text{k}\Omega} = 0.99\text{V/V}$$

$$\frac{v_o}{v_{b2}} = -g_m R_L = -40 \frac{\text{mA}}{\text{V}} \times 4\text{k}\Omega = -160\text{V/V}$$

$$G_v = \frac{v_o}{v_{sig}} = -160 \times 0.99 \times 0.98 = -155\text{V/V}$$



Example 8.7c

For the CC-CE amplifier in Fig. 8.44(a) let $I_1 = I_2 = 1 \text{ mA}$ and assume identical transistors with $\beta = 100$. Find the input resistance R_{in} and the overall voltage gain obtained when the amplifier is fed with a signal source having $R_{sig} = 4 \text{ k}\Omega$ and loaded with a resistance $R_L = 4 \text{ k}\Omega$. Compare the results with those obtained with a common-emitter amplifier operating under the same conditions. Ignore r_o .

For the CE amplifier

$$R_{in} = r_\pi = 2.5\text{k}\Omega$$

$$G_V = \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} (-g_m R_L)$$

$$G_V = \frac{2.5\text{k}\Omega}{2.5\text{k}\Omega + 4\text{k}\Omega} \left(-40 \frac{\text{mA}}{\text{V}} \times 4\text{k}\Omega \right) = -61.5\text{V/V}$$



The Darlington Configuration

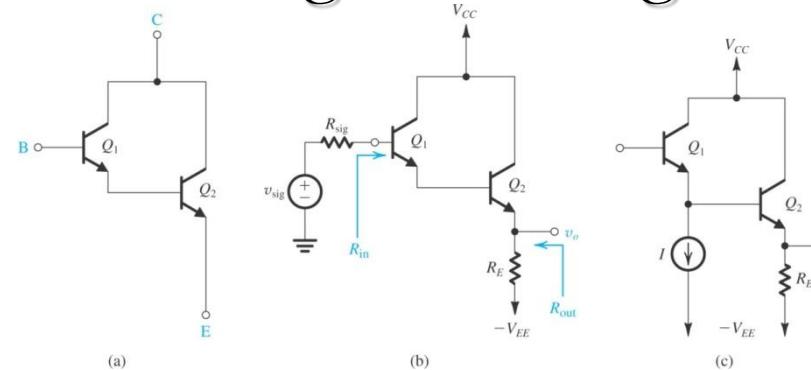


Figure 8.47 (a) The Darlington configuration; (b) voltage follower using the Darlington configuration; (c) the Darlington follower with a bias current I supplied to Q_1 to ensure that its β remains high.

Figure 8.47(a) shows a popular BJT circuit known as the Darlington configuration. It can be thought of as a variation of the CC-CE circuit with the collector of Q_1 connected to that of Q_2 . Alternatively, the Darlington pair can be thought of as a composite transistor with $\beta = \beta_1\beta_2$. It can therefore be used to implement a high-performance voltage follower, as illustrated in Fig. 8.47(b). Note that in this application the circuit can be considered as the cascade connection of two common-collector transistors (i.e., a CC-CC configuration).



The CC-CB and CD-CG Configurations

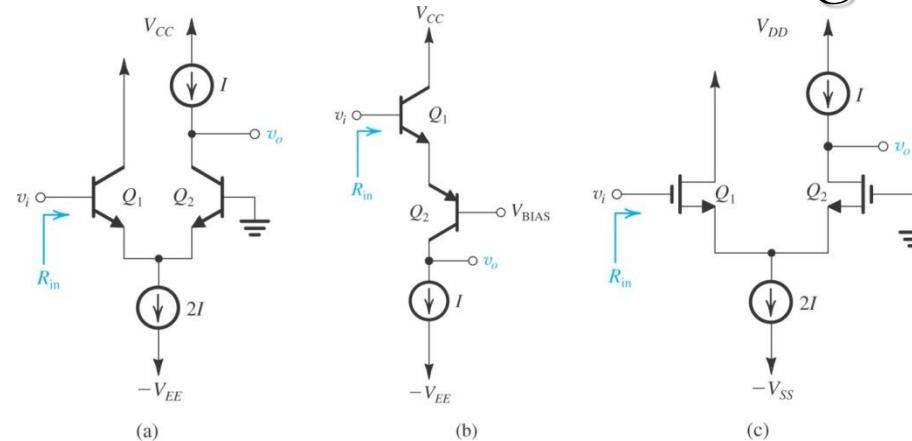


Figure 8.48 (a) A CC-CB amplifier. (b) Another version of the CC-CB circuit with Q_2 implemented using a *pnp* transistor. (c) The MOSFET version of the circuit in (a).

Cascading an emitter follower with a common-base amplifier, as shown in Fig. 8.48 (a) results in a circuit with a low-frequency gain approximately equal to that of the CB but with the problem of the low input resistance of the CB solved by the buffering action of the CC stage. It will be shown in Chapter 10 that this circuit exhibits wider bandwidth than that obtained with a CE amplifier of the same gain.



Example 8.8

For the CC-CB amplifiers in Fig. 8.49(a) and (b), find R_{in} , v_o/v_i , and v_o/v_{sig} when each amplifier is fed with a signal source having a resistance R_{sig} and a load resistance R_L is connected at the output. For simplicity, neglect r_o .

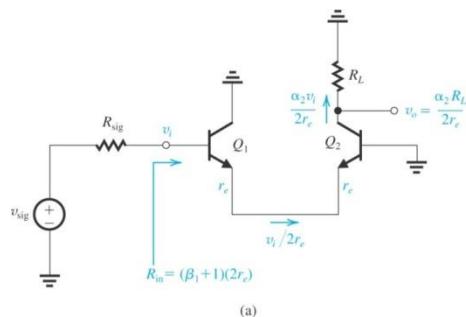
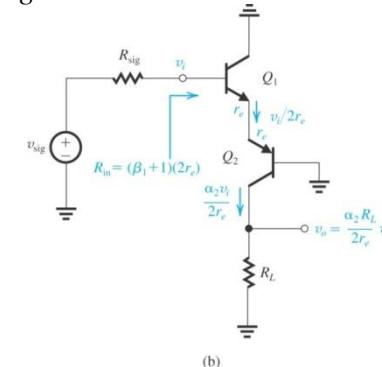


Figure 8.49 Circuits for Example 8.8.



$$R_{inCB} = R_{LCC} = r_e$$

$$R_{inCC} = (\beta + 1)(r_e + R_L) = (\beta + 1)2r_e$$

$$A_{v1} = \frac{R_L}{R_L + r_e} = \frac{1}{2}$$

$$A_{v2} = \alpha_2 \frac{R_L}{r_e}$$

$$A_v = \frac{v_o}{v_i} = A_{v1} \times A_{v2} = \frac{\alpha_2 R_L}{2r_e}$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}} \frac{\alpha_2 R_L}{2r_e}$$

---- R. MARTIN ----



Example 8.8a

For the CC-CB amplifiers in Fig. 8.48(a) and (b), find R_{in} , v_o/v_i , and v_o/v_{sig} when each amplifier is fed with a signal source having a resistance R_{sig} and a load resistance R_L is connected at the output. For simplicity, neglect r_o .

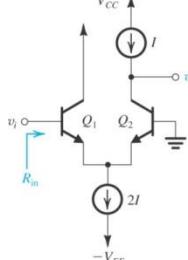


Figure 8.48 (a) A CC-CB amplifier.

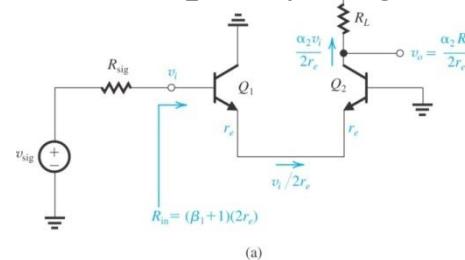
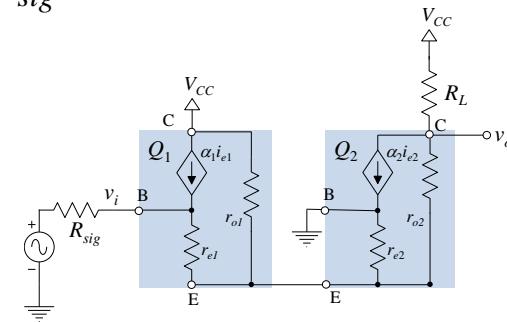


Figure 8.49 Circuits for Example 8.8.



A_v for a CC amplifier is: A_v for a CB amplifier is:

$$A_{v1} = \frac{R_L}{R_L + r_e} = \frac{r_e}{r_e + r_e} = \frac{1}{2}$$

$$A_{v2} = \alpha \frac{R_C \parallel R_L}{r_e} = \alpha_2 \frac{R_L}{r_e}$$

Ignoring r_o , R_{in} for a CC amplifier with load resistor R_L is: $R_{in} = (\beta+1)(r_e + R_L)$

$$\Rightarrow R_{in} = (\beta+1)(r_{e1} + r_{e2}) = 2(\beta+1)r_e = 2r_\pi$$

$$\Rightarrow A_v = \frac{v_o}{v_i} = A_{v1} \times A_{v2} = \frac{\alpha_2 R_L}{2r_e}$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}} \frac{\alpha_2 R_L}{2r_e}$$



Example 8.8b

For the CC-CB amplifiers in Fig. 8.48(a) and (b), find R_{in} , v_o/v_i , and v_o/v_{sig} when each amplifier is fed with a signal source having a resistance R_{sig} and a load resistance R_L is connected at the output. For simplicity, neglect r_o .

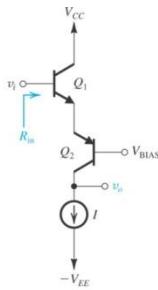


Figure 8.48 (b) Another version of the CC-CB circuit with Q_2 implemented using a *pnp* transistor.

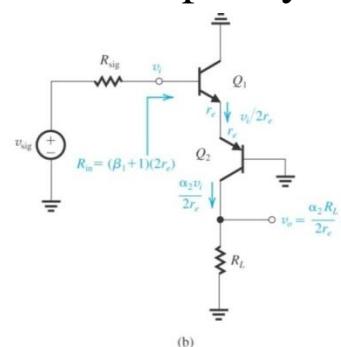
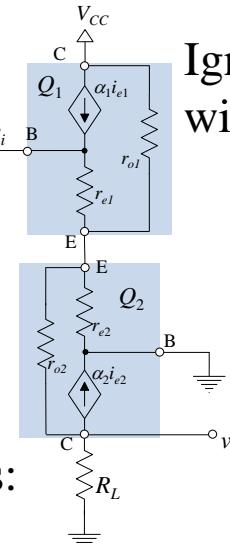


Figure 8.49 Circuits for Example 8.8.

A_v for a CC amplifier is: A_v for a CB amplifier is:

$$A_{v1} = \frac{R_L}{R_L + r_e} = \frac{r_e}{r_e + r_e} = \frac{1}{2}$$

$$A_{v2} = \alpha \frac{R_C \parallel R_L}{r_e} = \alpha_2 \frac{R_L}{r_e}$$



Ignoring r_o , R_{in} for a CC amplifier with load resistor R_L is:

$$R_{in} = (\beta + 1)(r_e + R_L)$$

$$\begin{aligned} R_{in} &= (\beta + 1)(r_{e1} + r_{e2}) \\ &= 2(\beta + 1)r_e = 2r_\pi \end{aligned}$$

$$\Rightarrow A_v = \frac{v_o}{v_i} = A_{v1} \times A_{v2} = \frac{\alpha_2 R_L}{2r_e}$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{sig} + R_{in}} \frac{\alpha_2 R_L}{2r_e}$$



Homework #2

Chapter 8 Problems:

1. 8.26
2. 8.49*
3. 8.66
4. 8.71*
5. 8.79*
6. 8.81*

* Answers in Appendix L



Ch. 8 Summary

- Integrated-circuit fabrication technology offers the circuit designer many exciting opportunities, the most important of which is the large number of inexpensive small-area MOS transistors. An overriding concern for IC designers, however, is the minimization of chip area or “silicon real estate.” As a result, large-valued resistors and capacitors are virtually absent.
- The basic gain cell of IC amplifiers is the CS (CE) amplifier with a current-source load. For an ideal current-source load (i.e., one with infinite output resistance), the transistor operates in an open-circuit fashion and thus provides the maximum gain possible, $A_{vo} = -g_m r_o = -A_0$
- The intrinsic gain A_0 is given by $A_0 = V_A/V_T$ for a BJT and $A_0 = V_A/(V_{OV}/2)$ for a MOSFET. For a BJT, A_0 is constant independent of bias current and device dimensions. For a MOSFET, A_0 is inversely proportional to $\sqrt{I_D}$ (see Eq. 8.46).
- Simple current-source loads reduce the gain realized in the basic gain cell because of their finite output resistance (usually comparable to the value of r_o of the amplifying transistor).



Ch. 8 Summary Continued

- To raise the output resistance of the CS or CE transistor, we stack a CG or CB transistor on top. This is cascoding. The CG or CB transistor in the cascode passes the current $g_m v_i$ provided by the CS or CE transistor to the output but increases the resistance at the output from r_o to $(g_m r_o) r_o$ in the MOS case [$g_m (r_o \parallel r_{\pi}) r_o$ in the bipolar case]. The maximum output resistance achieved in the bipolar case is $\beta_2 r_o$.
- A MOS cascode amplifier operating with an ideal current source load achieves a gain of $(g_m r_o)^2 = A_0^2$.
- To realize the full advantage of cascoding, the load current source must also be cascaded, in which case a gain as high as $\frac{1}{2} A_0^2$ can be obtained.
- Double cascoding is possible in the MOS case only. However, the large number of transistors in the stack between the power-supply rails results in the disadvantage of a severely limited output-signal swing. The folded-cascode configuration helps resolve this issue.
- A CS amplifier with a resistance R_S in its source lead has an output resistance $R_o \approx (1+g_m R_S) r_o$. The corresponding formula for the BJT case is $R_o = [1+g_m(R_e \parallel r_{\pi})] r_o$.



Ch. 8 Summary Continued

- Biasing in integrated circuits utilizes current sources. As well, current sources are used as load devices. Typically an accurate and stable reference current is generated and then replicated to provide bias currents for the various amplifier stages on the chip. The heart of the current steering circuitry utilized to perform this function is the current mirror.
- The MOS current mirror has a current transfer ratio of $(W/L)_2/(W/L)_1$. For a bipolar mirror, the ratio is I_{S2}/I_{S1} .
- Bipolar mirrors suffer from the finite β , which reduces the accuracy of the current transfer ratio.
- Both bipolar and MOS mirrors of the basic type have a finite output resistance equal to r_o of the output device. Also, for proper operation, a voltage of at least 0.3 V is required across the output transistor of a simple bipolar mirror ($|V_{ov}|$ for the MOS case).
- Cascoding can be applied to current mirrors to increase their output resistances. An alternative that also solves the β problem in the bipolar case is the Wilson circuit. The MOS Wilson mirror has an output resistance of $(g_m r_o) r_o$, and the BJT version has an output resistance of $\frac{1}{2} \beta r_o$. Both the cascode and Wilson mirrors require at least 1 V or so for proper operation.



Ch. 8 Summary Continued

- The Widlar current source provides an area-efficient way to implement a low-valued constant-current source that also has a high output resistance.
- Preceding the CE (CS) transistor with an emitter follower (a source follower) results in increased input resistance in the BJT case and wider bandwidth in both the BJT and MOS cases.
- Preceding the CB (CG) transistor with an emitter follower (a source follower) solves the low-input-resistance problem of the CB and CG configurations.
- The Darlington configuration results in an equivalent BJT with a current gain approaching β^2 .