LAB4 Inverter Tutorial: Turbo and PCELLS

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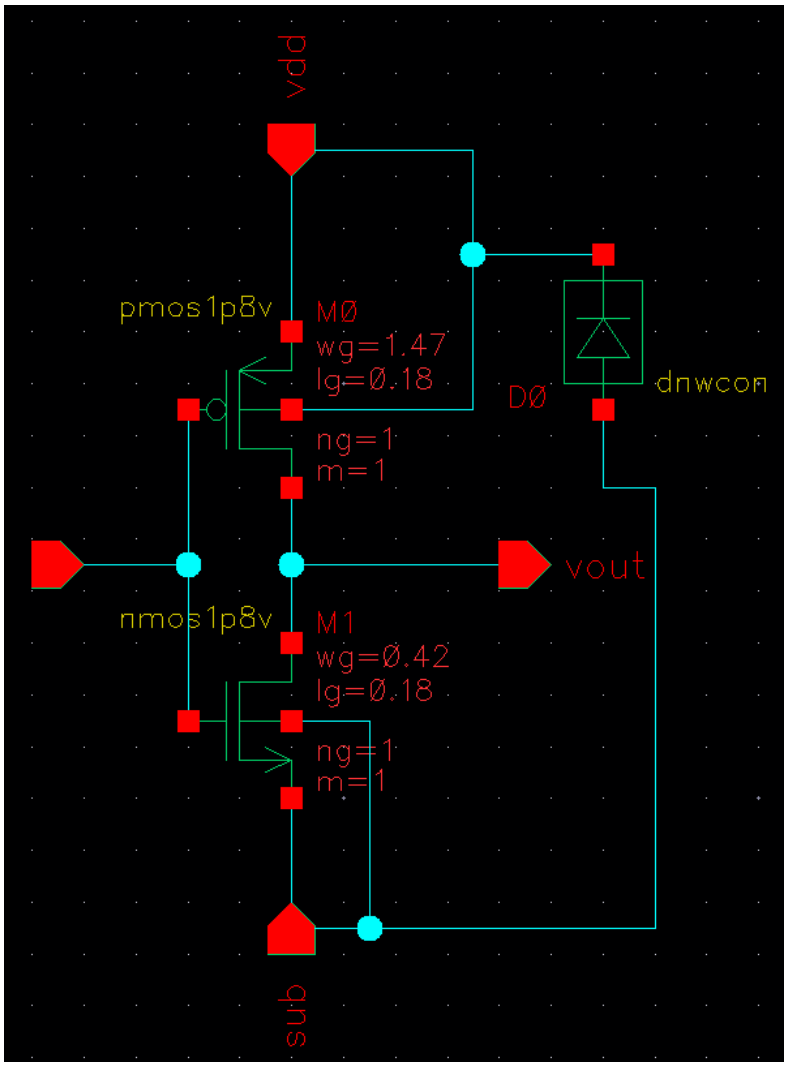
Introduction

This tutorial demonstrates my three favorite Cadence productivity tricks:

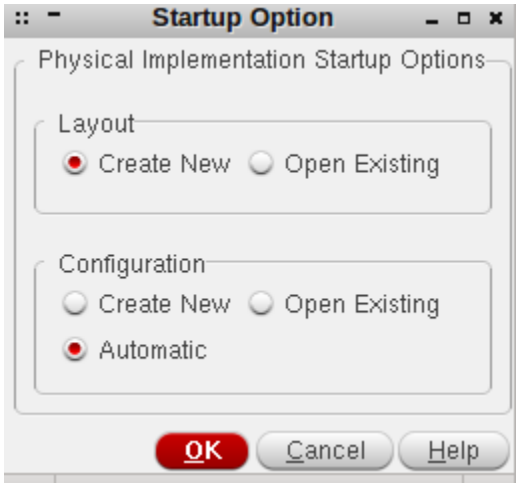
1. XL – Automatically generate layout from schematic.
2. DRC check – identifies DRC errors as you draw your layout.
3. LVS check _ compares the schematic vs. layout for any discrepancies

TURBO & PCELLS

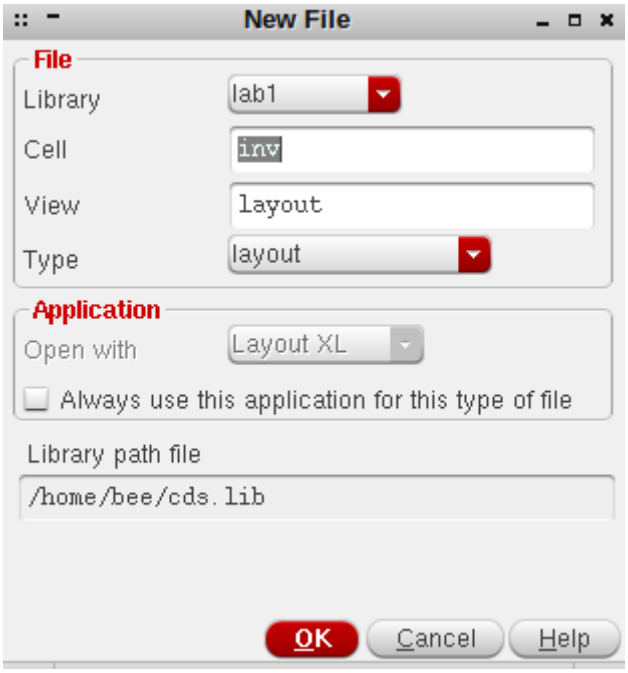
STEP 1: In library lab1, open schematic from cell **inv** .To do this, open Library Manager, select library lab1, and double click on **inv** schematic. From lab3 we determined that the value of pmos should be roughly three times bigger one used in nmos. Therefore, before we start this lab double check and make sure the right value is set for the width of pmos. To make things easier I used wg=1.47 for pmos, so if u have a slightly different value, change it to 1.47 instead.



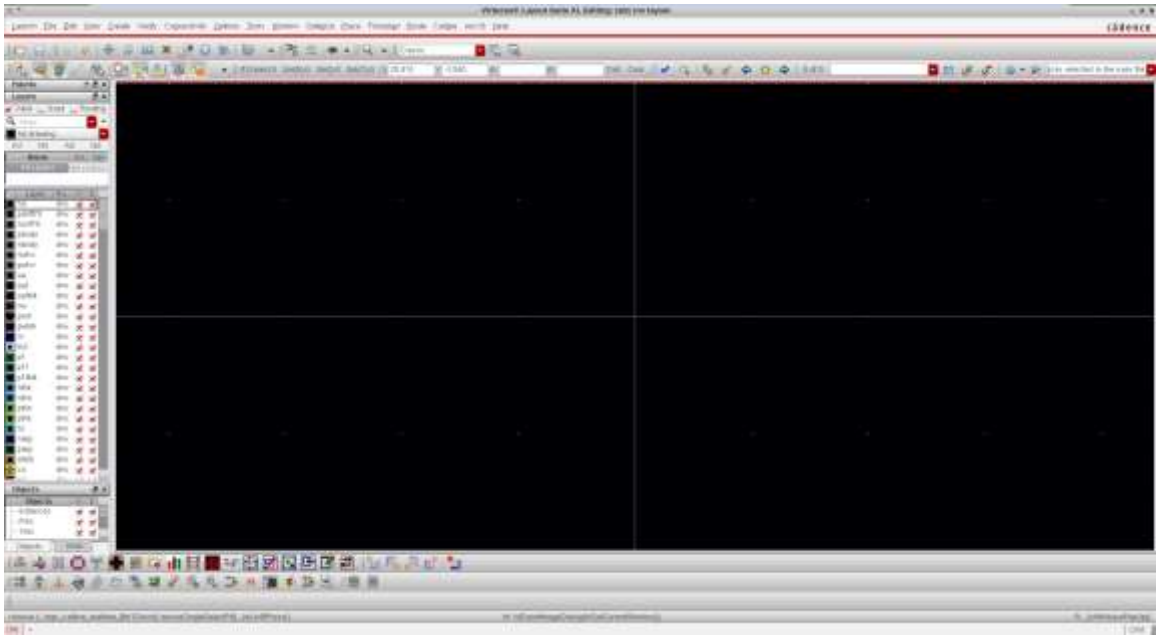
STEP 2. Create a layout view for inv2 cell. This can be achieved by selecting Launch->Layout GXL View and filling out the dialog box as shown below.



Press ok and in the new windows that pups up also press ok.



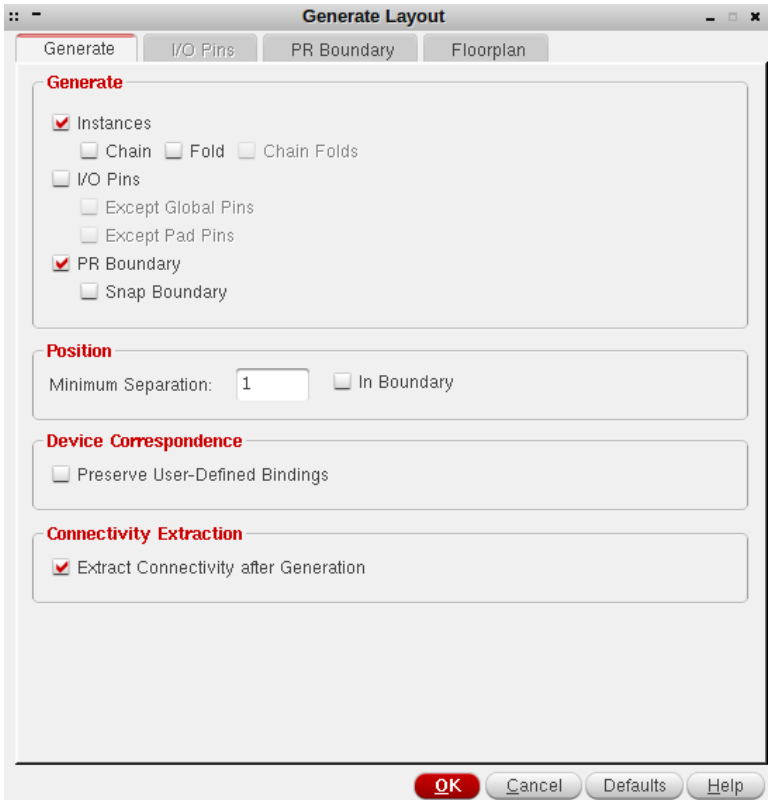
If you get a message about the License, please click on yes.
Now a blank new window should pup op as follows.



STEP 3. In layout editor, Options->Display(or press ‘E’) and change “X Snap Spacing”, “Y Snap Spacing”, and “Snap Modes” as shown below.

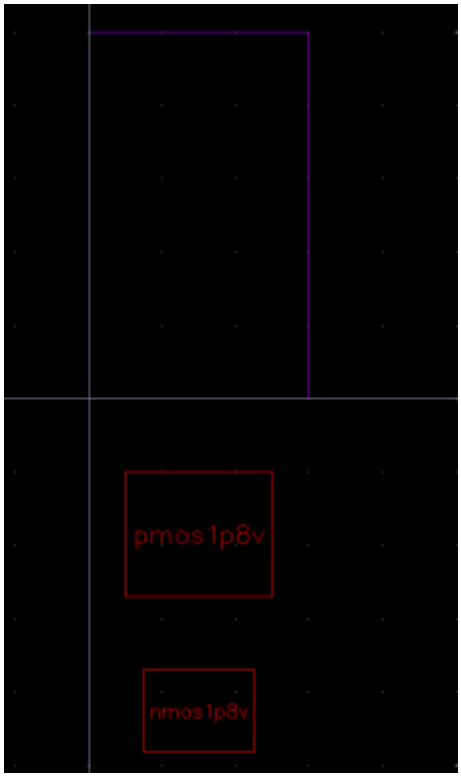
STEP 4. Generate layout components by clicking on Connectivity->Generate-> All From Source

- In the Generate Tab be sure to uncheck I/o pins

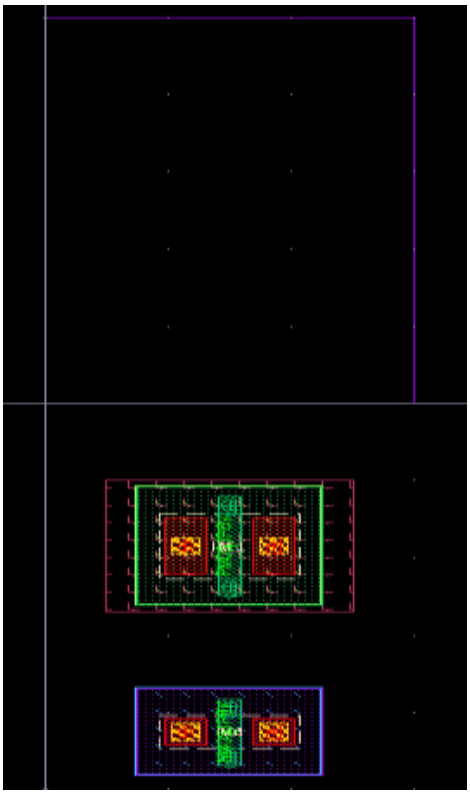


- In the PR Boundary tab change utilization to width and set it to 3
- Also change aspect ratio to height and set that to 7 and press ok

- Now you should see the layout for the nmos and pmos



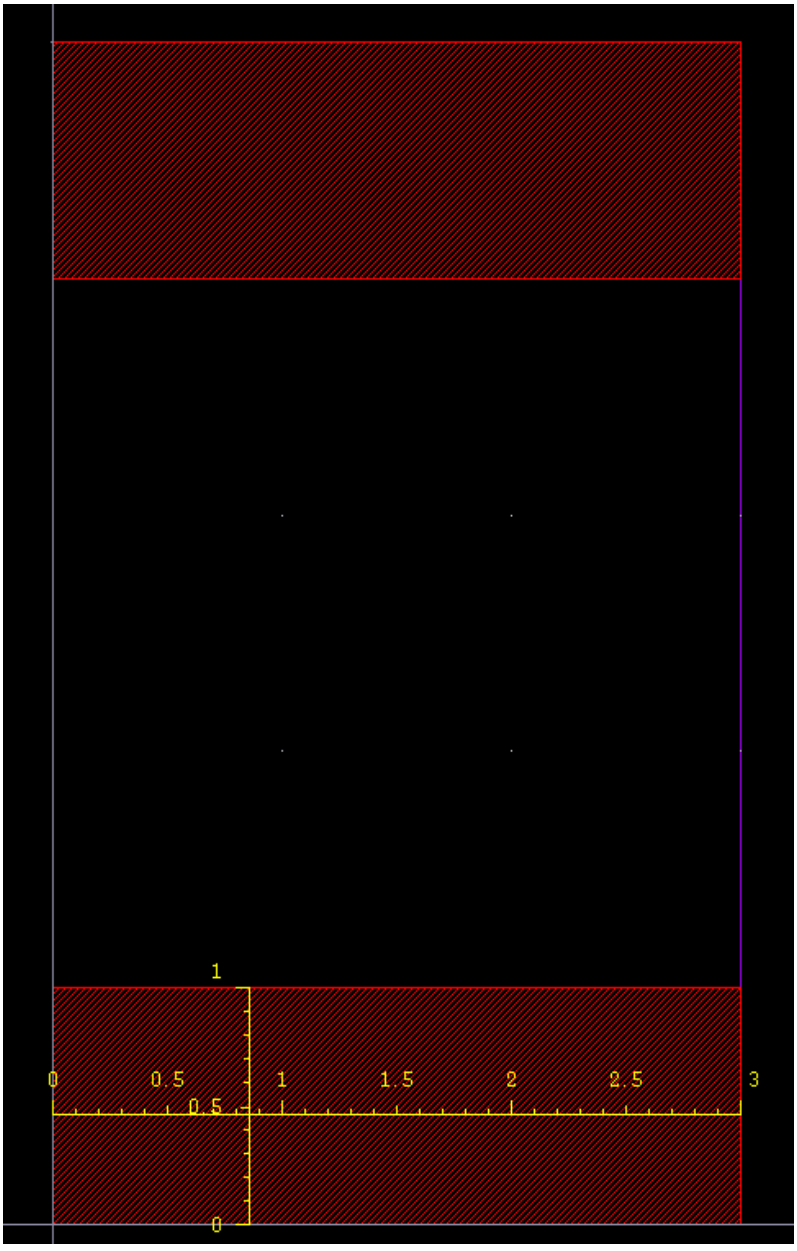
- Press Shift + F to see all layers instead of the block layout.



STEP 5. Now draw the Power Rail and the Ground Rail in Metal-1 as shown below.

- Select *M1 (Metal-1) drw* layer from the **LSW**. In the rest of the tutorial, always use the drw layers for your layouts unless otherwise specified.
- In the Layout Editing window, press the letter “r” or select Create ->Rectangle
- Move your mouse to the cell origin, where the horizontal and vertical guidelines intersect. Check the information bar at the bottom of the screen to make sure you are at the right location (0,0). **Click** on this point.
- Move the mouse up and right to create a rectangle. Use the data in the information bar to move your mouse to the point that is 3um horizontal and 1um vertical from the origin (7.2 x 5 um is always in the X direction by the Y direction, respectively). Click on this point to create the Metal-1 rectangle, which will be your ground rail.

Repeat these steps to draw the VDD rail 21um, top to bottom, above the GND rail. Read the ***Useful Editing Tools*** section below.



Useful Editing Tools

Ruler: The ruler is very useful to place objects and measure the distance between the objects.

- To start the ruler, press the letter “k” or from the menu choose: Tools->Create Ruler.
- Click the start and end in the window; a ruler is created showing the distance between the two points.
- Hit the ‘ESC’ key to exit the ruler command.
- To clear ruler marks, press <shift> k

Move: If you place the objects on the wrong place, you can use move function to adjust the location of the object.

- To begin the move process, press the letter “m” or from the menu choose: Edit -> Move
- The move dialog box will pop-up (**press F3 if it doesn’t pop automatically**)
- Click on the shape you wish to move then move the mouse to the target location and click again. The Snap Mode is an interesting option. When this is in orthogonal setting, objects will move only along one axis. This is a good feature to help you avoid alignment problems.
- When you have finished the move operation, hit the ‘ESC’ key to exit the move command.

Stretch: If you make an object too big or too small and you wish to resize it, you can use the stretch function to adjust its perimeter.

- To begin the stretch process, press the letter “s” or from the menu choose: Edit -> Stretch
- The stretch dialog box will pop-up (**press F3 if it doesn’t pop automatically**)
- Place your mouse over (DO NOT CLICK) the edge of the object you wish to stretch. You will notice that only the edge of the object will begin to highlight.
- Once the proper edge is highlighted, click on it, and then move the mouse to the place you would like the edge to be. Click again and the edge will be set.
- Hit the ‘ESC’ key to exit the stretch command.

Copy: If you want to create the same object repeatedly, you can use the copy function.

- To begin the copy process, press the letter “c” or from the menu choose: Edit -> Copy
- The copy dialog box will pop-up (**press F3 if it doesn’t pop automatically**)
- Click in an object. Notice that an outline of the object will attach to your mouse cursor.
- Move our mouse and click when you are satisfied with the location to place a copy of the object.
- Press the ‘ESC’ key to exit the copy command.

Delete: If you want to delete an object you have drawn:

- Place your mouse over the object and left-click to select it.
- Press the Delete key on the keyboard.
- Press the ‘ESC’ key to exit the delete mode

Undo: When you make a mistake (accidentally delete a component, etc.), you can undo the action by pressing the “**u**” key or clicking on the Undo icon in the toolbar. To “REDO” something you have just ‘undone’ you may press the uppercase “**U**” key.

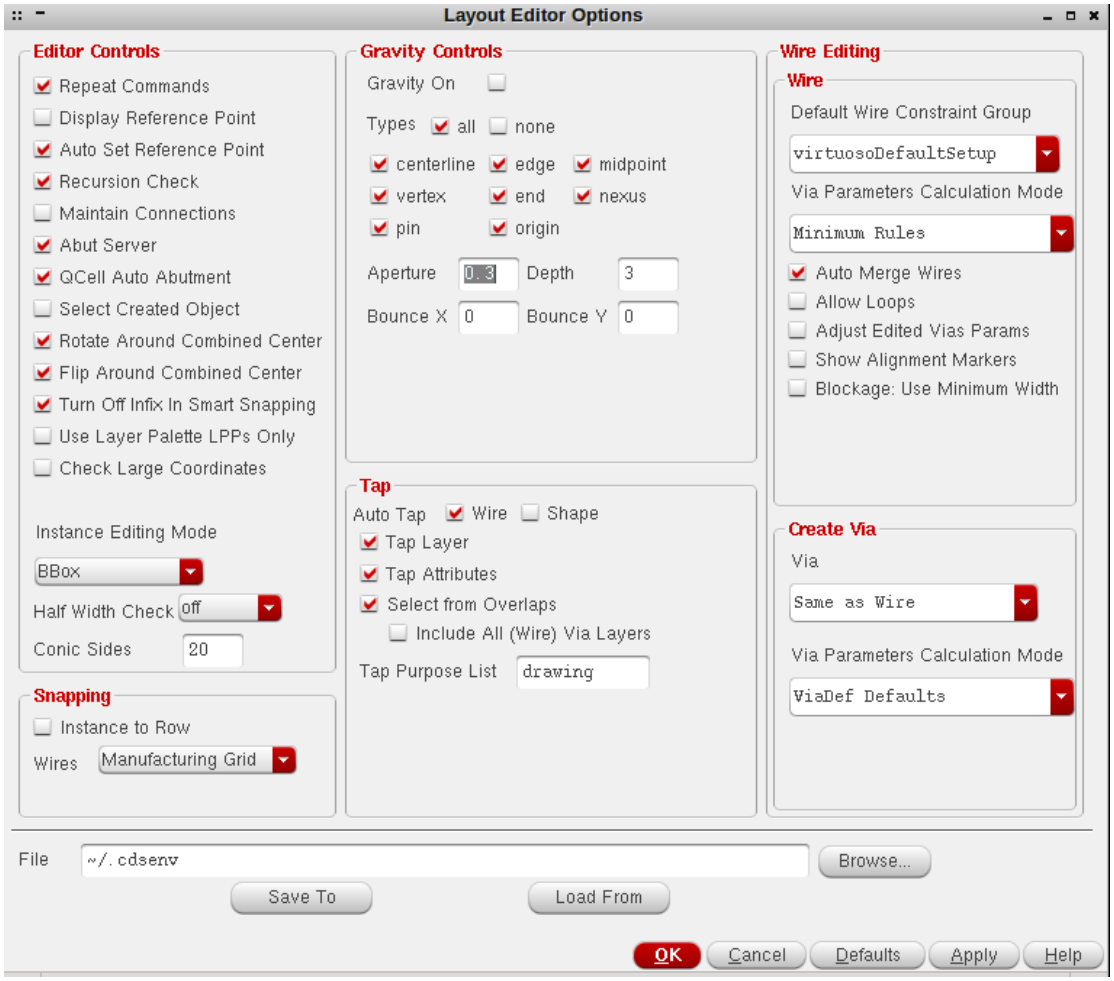
Zoom in Window: If you wish to enlarge a small area of your drawing, press the letter “**z**” then click in the left most area you wish to enlarge and release, then click on the right most bottom of the area you wish to enlarge (you will notice a square is drawn around the area you’d like enlarged.

Zoom Full: If you wish to see the entire drawing area, press the key: “f” for full view.

To see helpful window during command: press F3 key on keyboard. This is helpful when doing things like moving geometry or drawing geometry.

STEP 6. Turn off gravity.

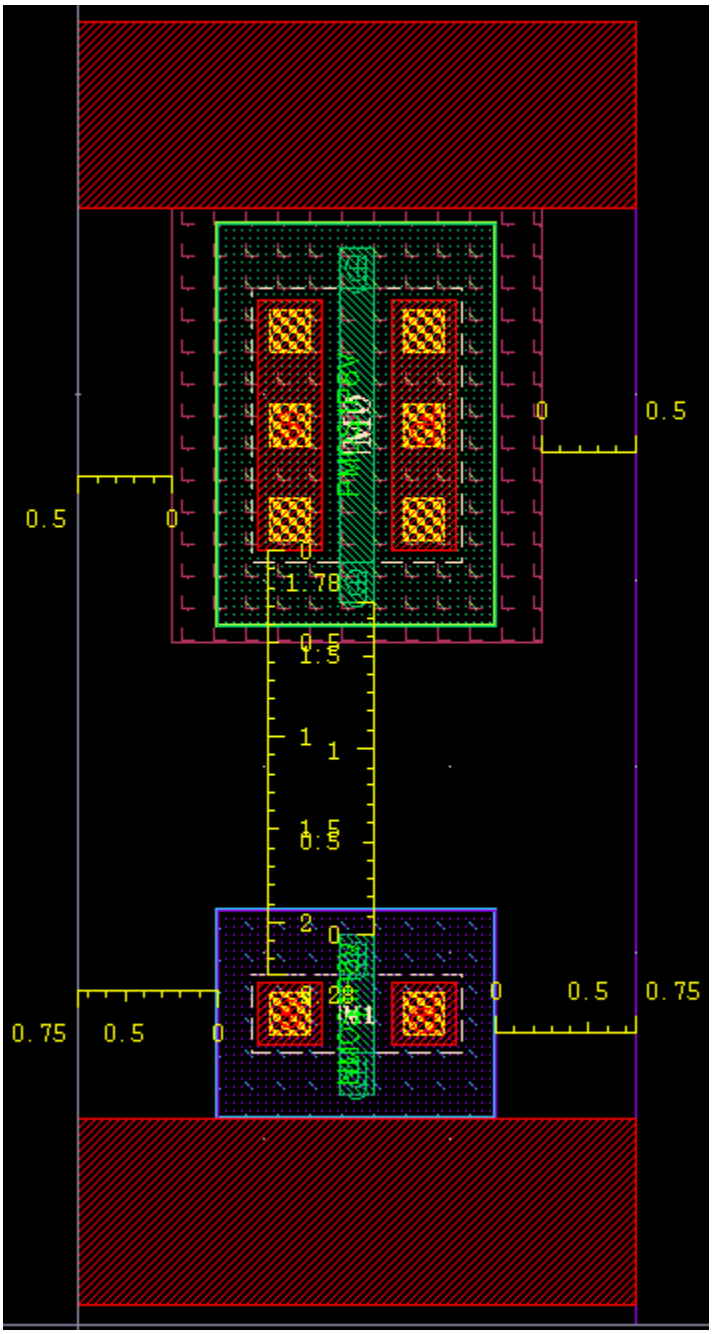
- Gravity restricts the positioning of your transistors, by turning it off; you can put transistors in any location.
- Click on Options-> Editor, and uncheck Gravity On.



STEP 7: position the Pmos and Nmos as follow.

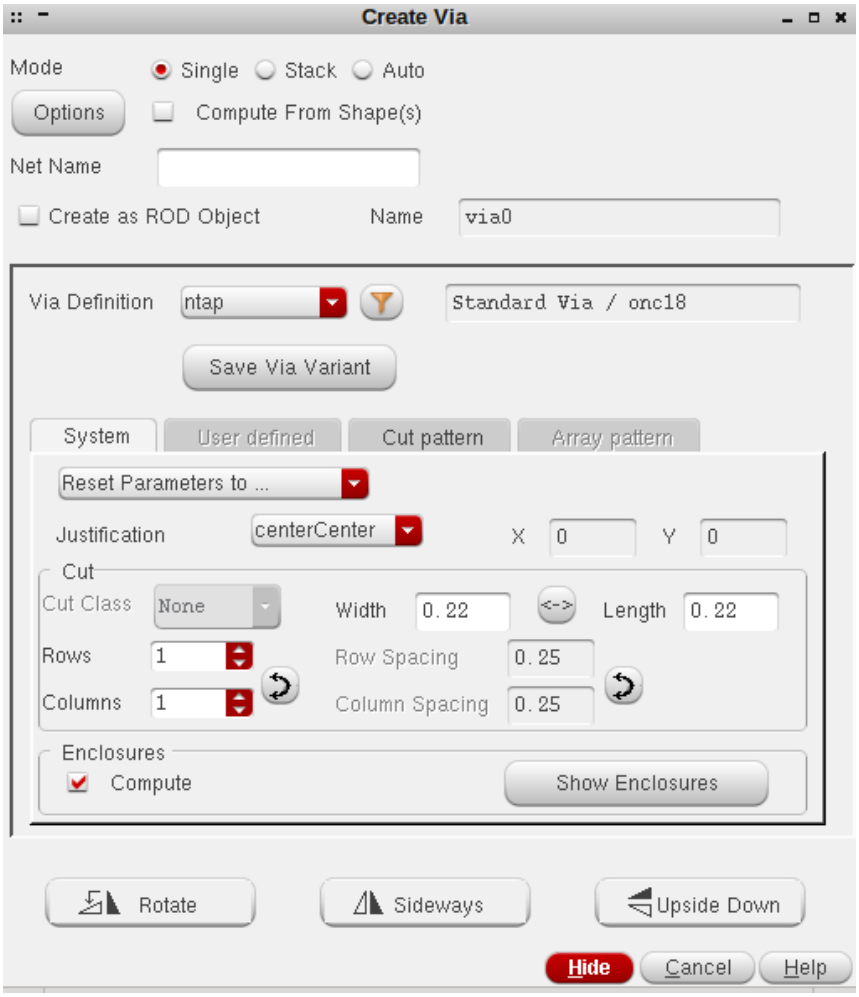
- The Nwell layer of pmos should be touching the top metal1 bar but not overlapping.
- The pmos transistor should be placed in the middle by leaving 0.5 micron on each side.
- The bottom of the nmos should be touching the bottom metal1 layer but not overlapping
- The nmos transistor should be place right in the middle, leaving 0.75 micron on each side

This positioning is important as it leaves enough space between different layers and will make it easier to pass LVS and DRC.
It also makes it easier to connect the gates and drains together as the transistors are lined up perfectly

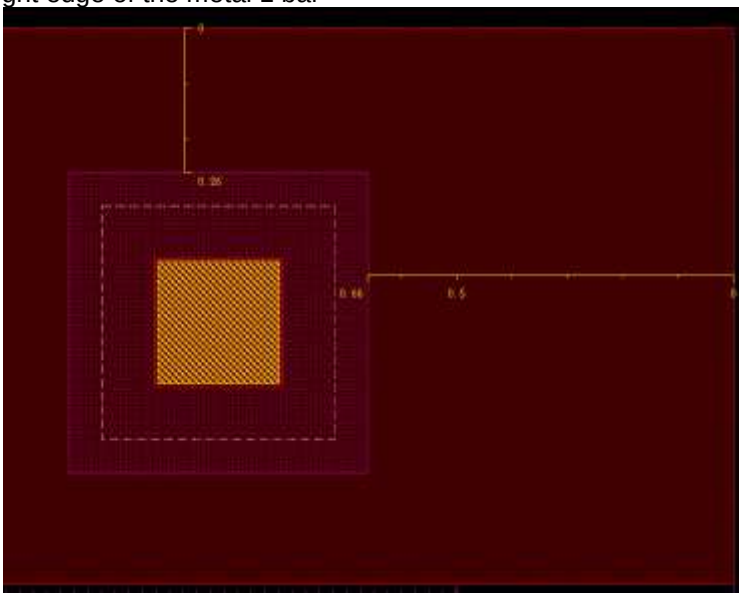


STEP 8: placing the ntap and ptap vias for connecting the bodies of nmos and pmos.

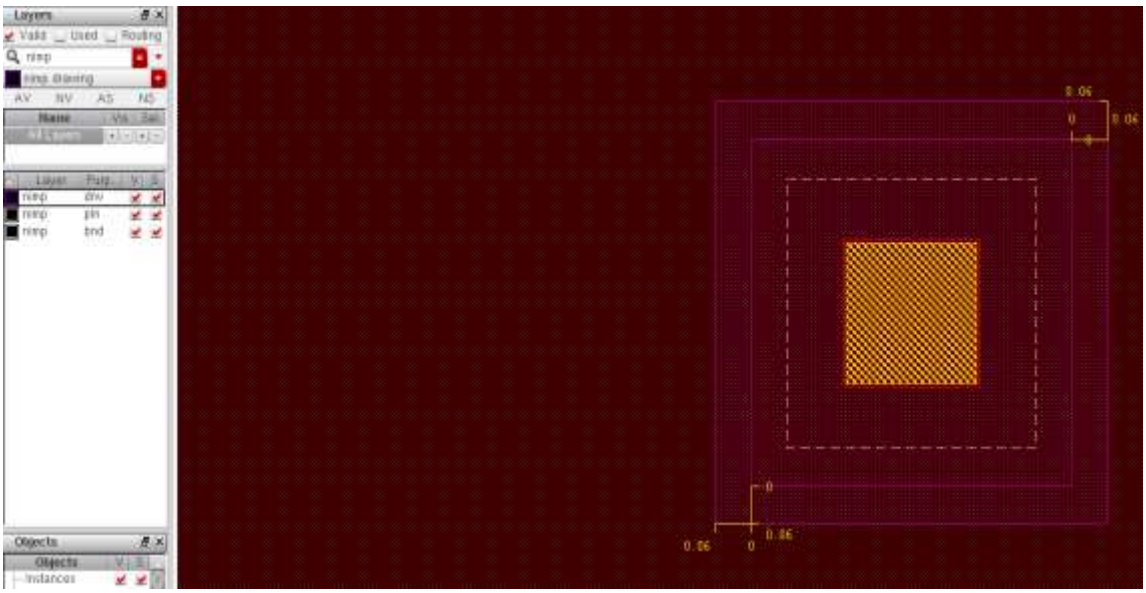
- Click on Create_via(or press O)
- Select ntap under Via Definition



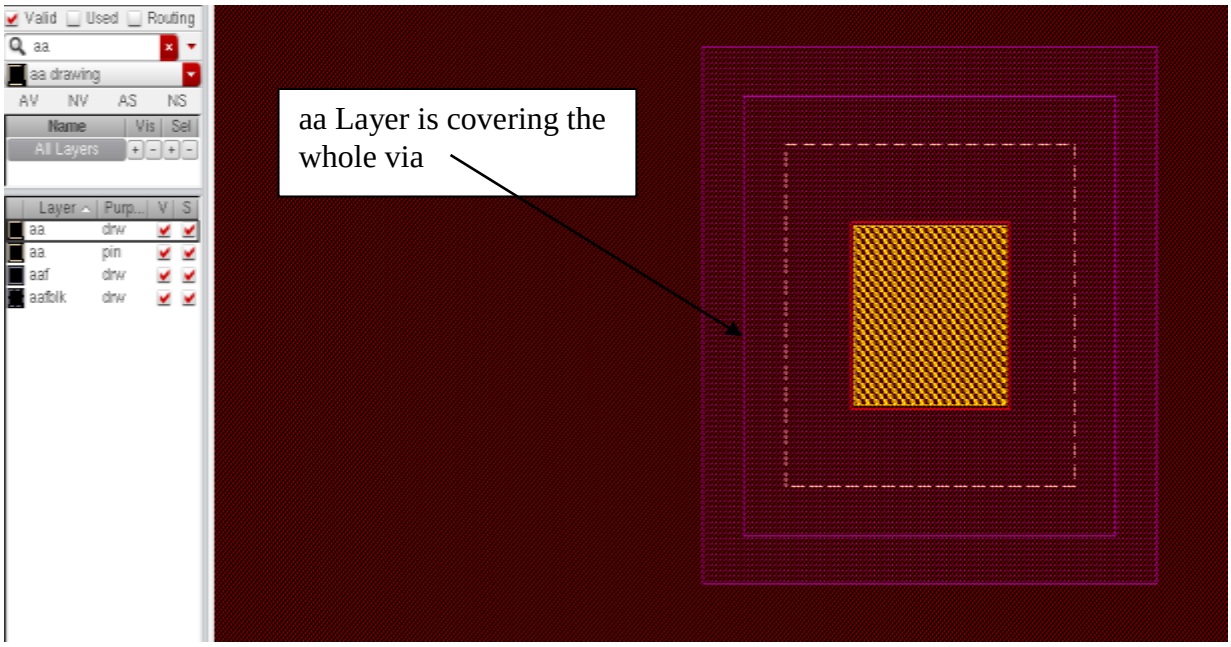
- Place the via in the in the top metal rail
  - Via should be 0.26 micron away from the top and 0.66 micron away from the right edge of the metal 1 bar



- Note as is the via wont pass the DRC because the aa layer and the nimp layer are not large enough to satisfy the DRC check.
- In order to correct that we should add the two layer as follows.
    - Choose the nimp layer, then create a rectangle which is 0.06 micron bigger than the via from each side. (you can search for nimp in the layers and find it quicker)

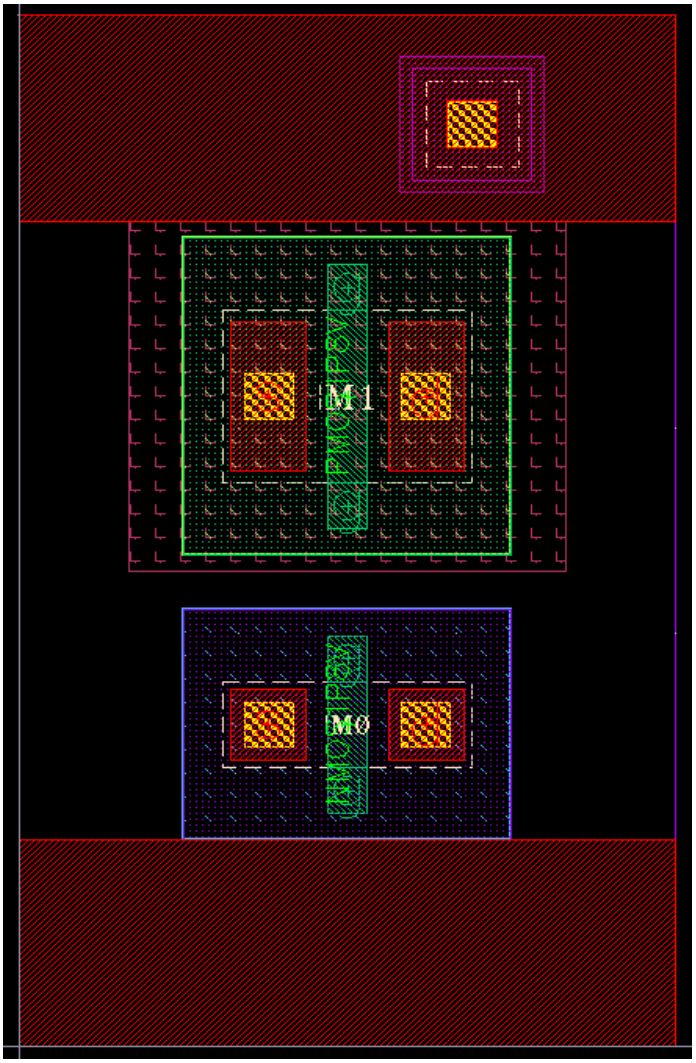


- The aa layer will have to cover the entire via and therefore will be 0.06 micron smaller than the nimp layer that was just placed.
- Select aa layer and cover the via.

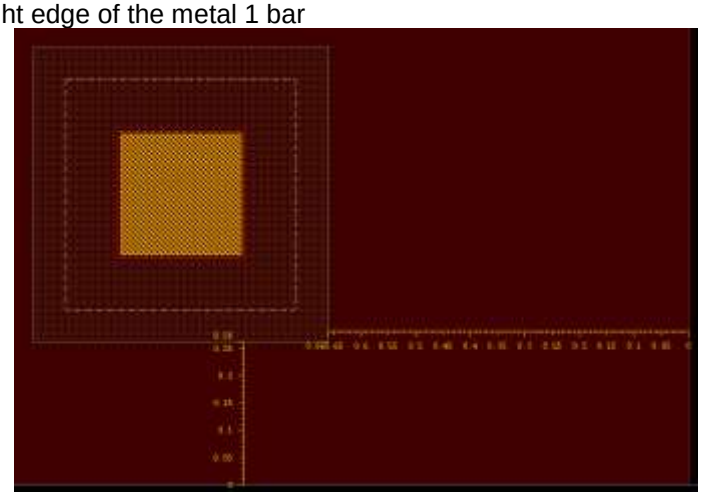


- aa layer starts at the top left of 2nd purple square and ends where the 2nd purple square ends.

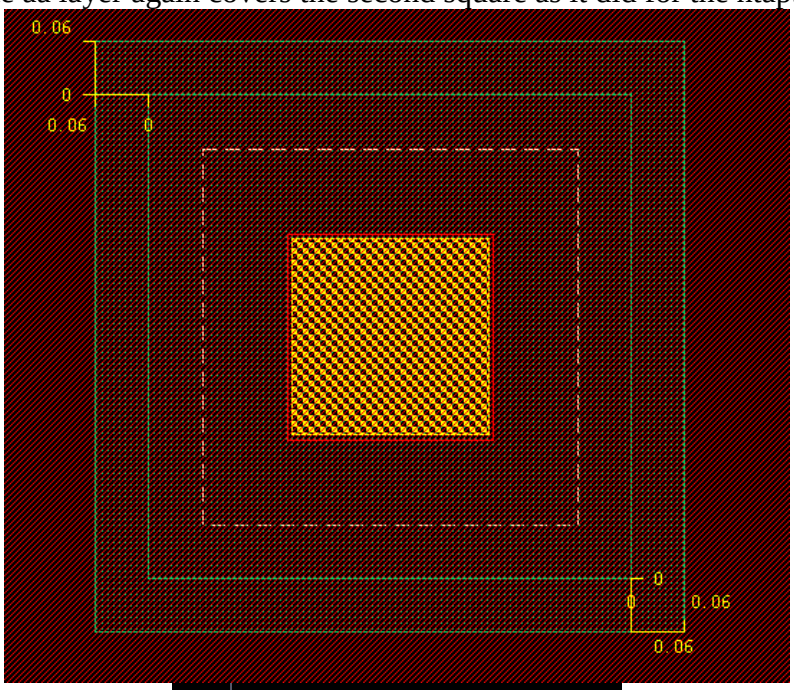
The inverter layout now should look like this.

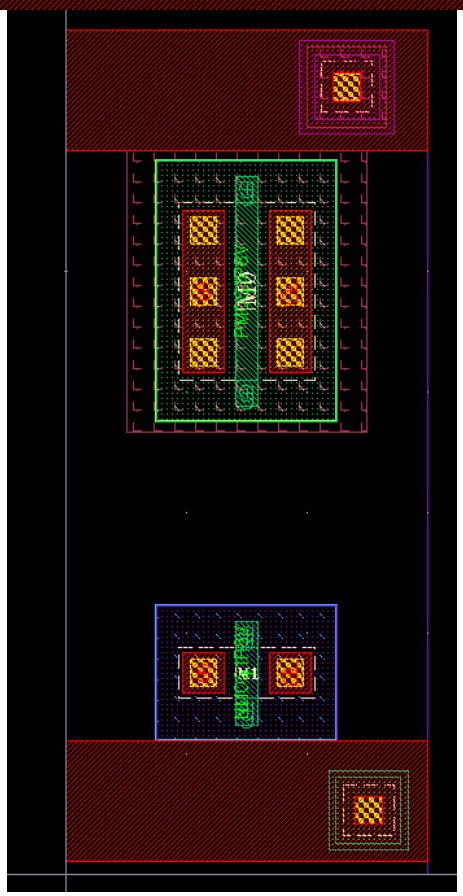


- now we will repeat the same process for the ptap via
- Press O on your keyboard and this time select ptap, and place it in the bottom metal 1 rail.
    - Via should be 0.26 micron away from the bottom and 0.66 micron away from the right edge of the metal 1 bar



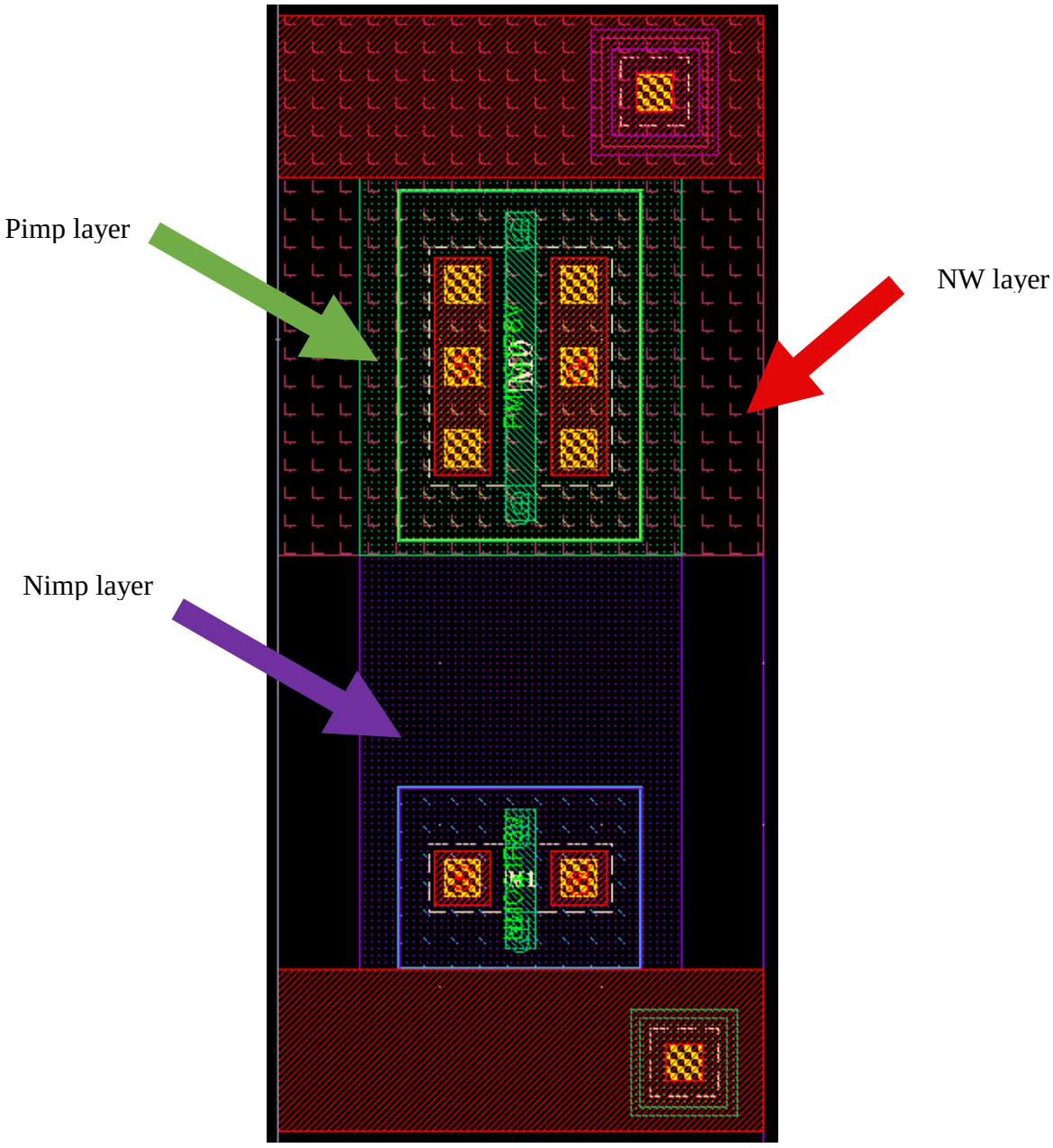
- Again we have to expand the top 2 layers in this via in order to pass drc.
- So we repeat the same process as we did for ntap, except we use pimp layer instead of nimp
- The aa layer again covers the second square as it did for the ntap.





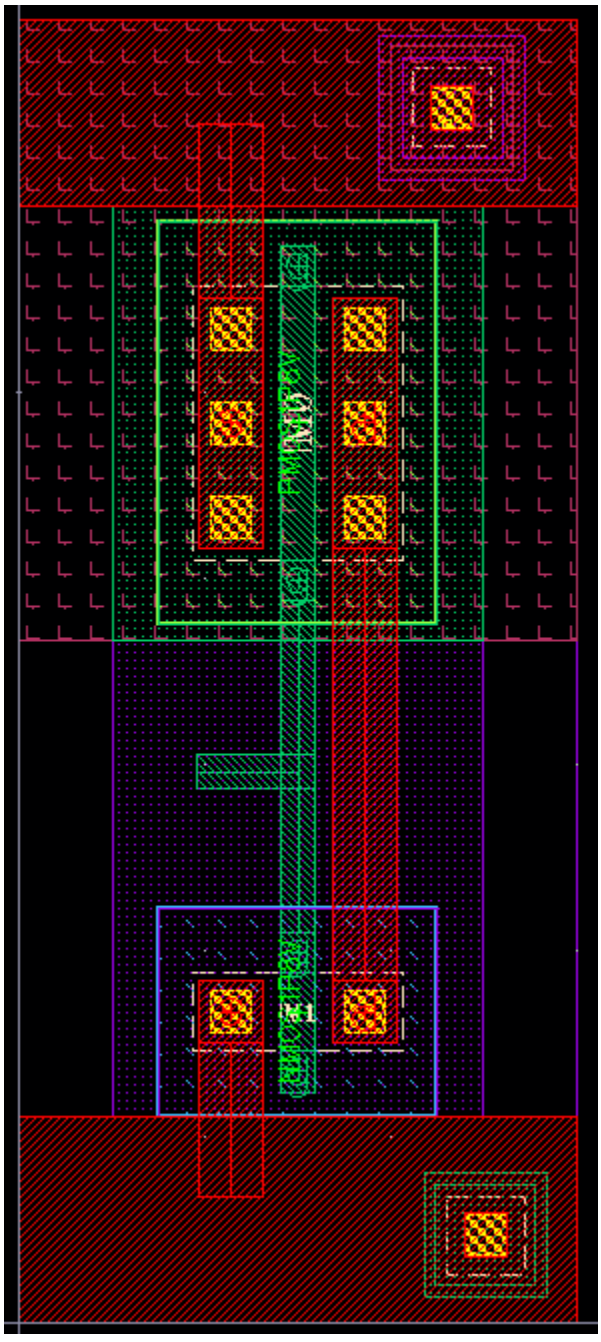
STEP 9: expand the pimp and pthn layer in pmos to cover the entire pmos.

- In order to connect the gates together we need to connect the two poly1 layers together, and we have to make sure no poly1 layer is undoped.
- In order to do that we have to make sure the pimp and the nimp layers are touching.
- Select pimp(drw) layer and create a rectangle that exactly covers the entire pmos and the nwel layer(green layer in the image)
- Then choose nimp(drw) and create a rectangle that starts at the top left corner of the nmos and goes all the way down to the bottom right corner of nmos where the top of the metal 1 bar touches the bottom of nmos and covers the entire nmos(purple layer in the image)
- We also need to connect the body of pmos to the nwel layer. In order to do that we need to create a nw(drw) layer that covers the top part of the layout and ends exactly where the pmos ends.



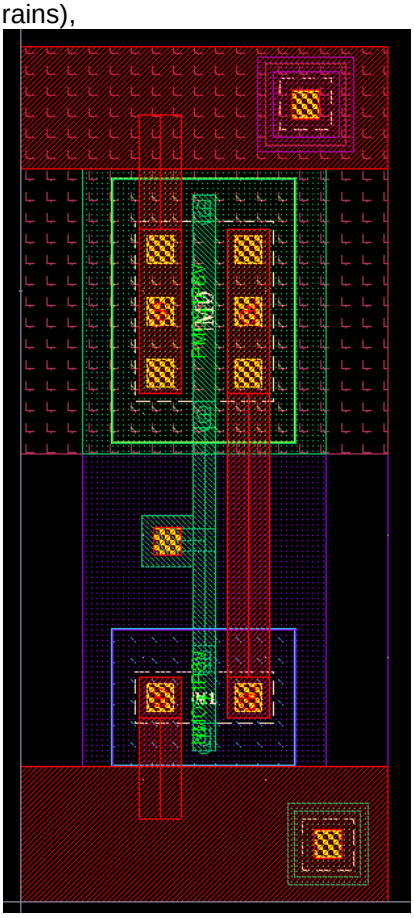
STEP 10: Create wires using path command. Select M1 layer in LSW, click on Create->Wiring->Wire(or simply press P) and connect the source of pmos to the top metal1 bar. When you are done with drawing a wire, press the enter key.

- Do the same thing for connecting the drain of pmos to the drain of nmos
- Next we need to connect the source of nmos to the bottom metal1 rail
- Lastly, we need to connect the two poly gates together. This layer is p1(drw)
- Add a small poly1 layer in the middle so we can connect the poly1 to m1 contact

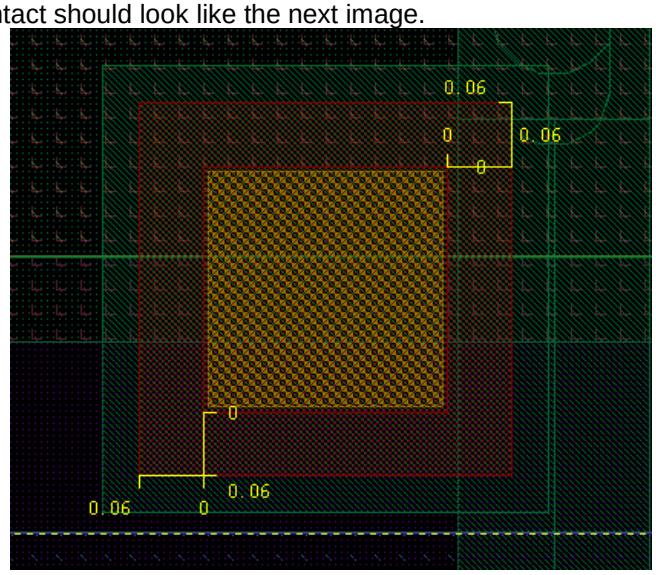


STEP 11: create a poly1 to metal1 contact so we can route the input all the way to the edge so we can easily connect the input and output to other gates.

- Press O to create a contact. Choose p1_m1 as Via definition, and place the via in the center of the p1 wire between the two gates.(be careful not to get too close to the m1 wire the connects the two drains),

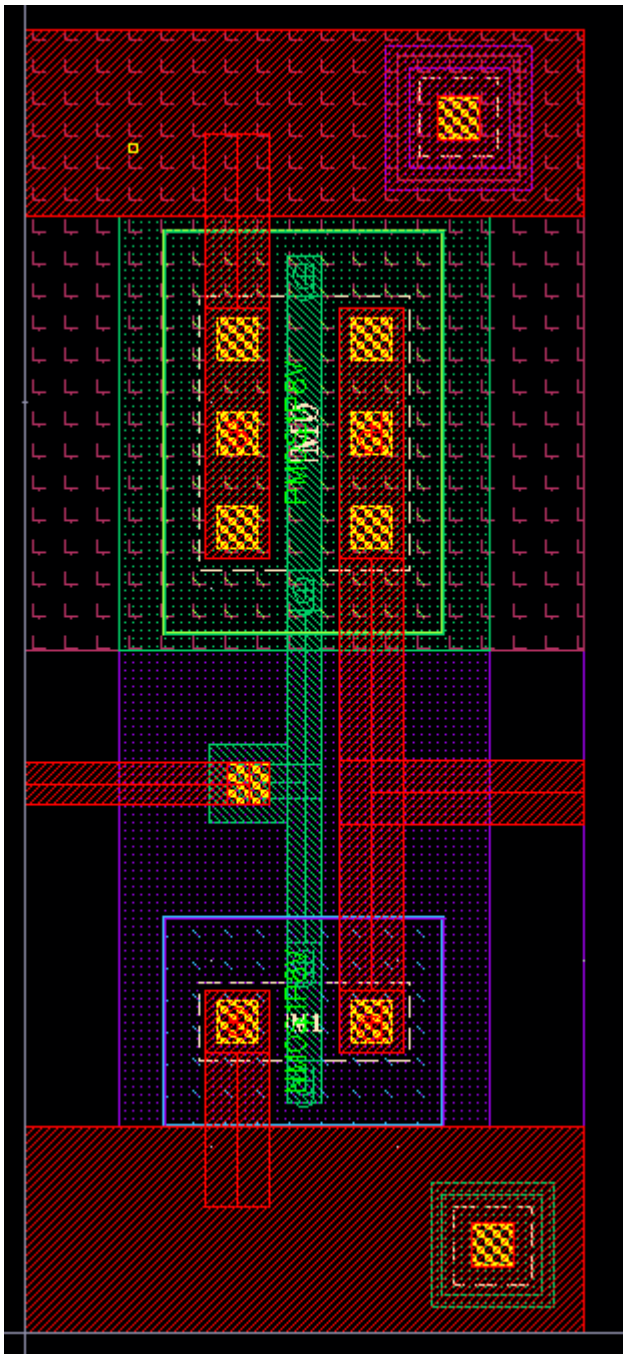


- We need to add layer of metal1 around the metal1 layer of the via to make sure the right amount of metal1 is covering the contact. Choose m1(drw) and create a square which is 0.06 micron bigger that the m1 layer in the via on each side.
- The final contact should look like the next image.



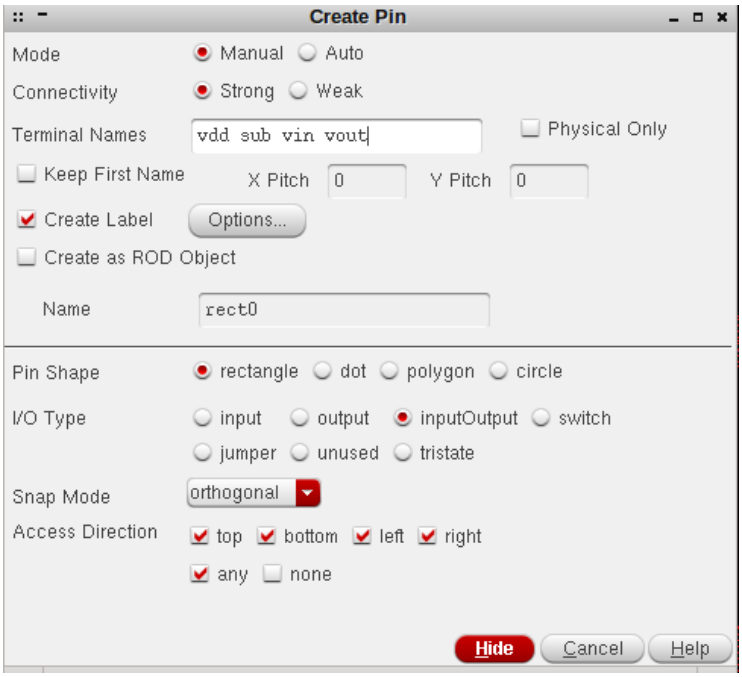
STEP 12. Route the input and output wires to the edge.

- Use m1(drw) and connect the newly created contact to m1 wire and route it all the way to the left edge
- Do the same with the m1 wire between the drains and route that wire all the way to the right edge.

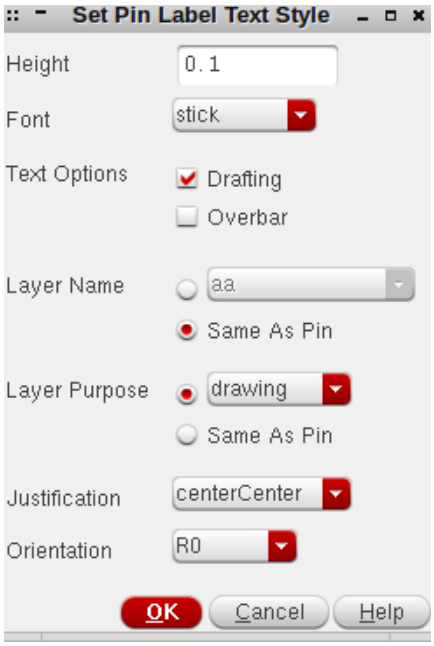


STEP 13. Create your pins.

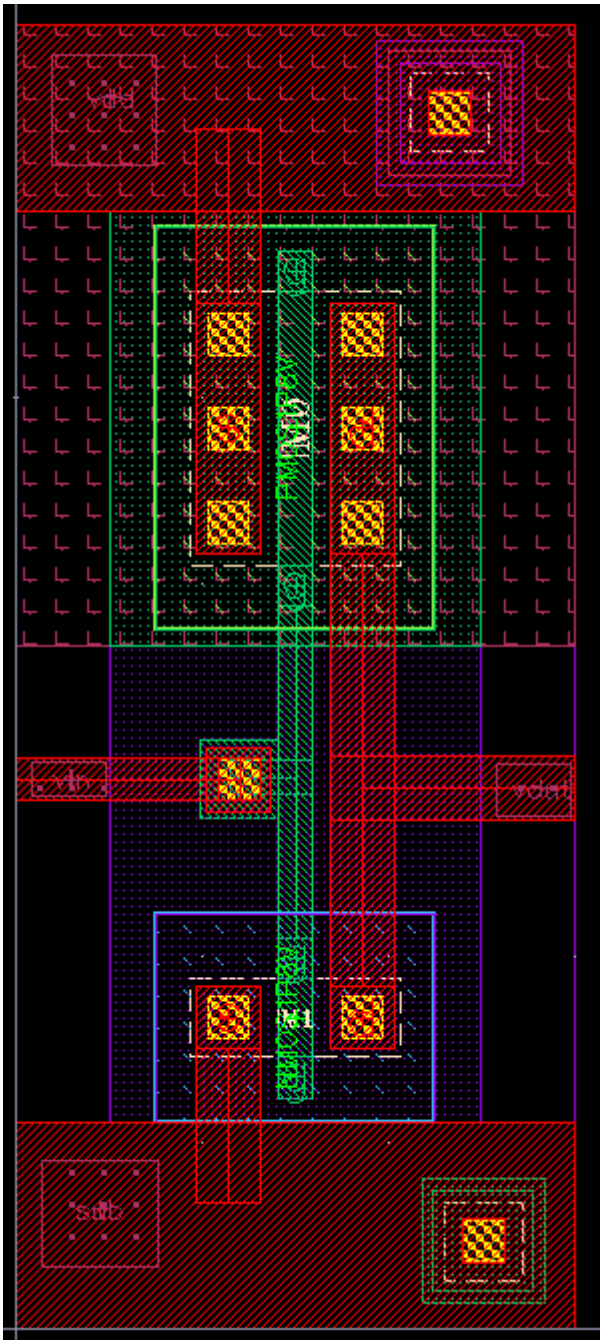
- Choose m1(port) and click on Create -> Pin
- Type the 4 terminal names: vdd sub vin vout. (these names should match schematic pin names)
- Make sure I/O type is set to inputOutput, and check create Label



- Click on options for create Label
  - Set height to 0.1
  - Set layer name to same as pin and press ok

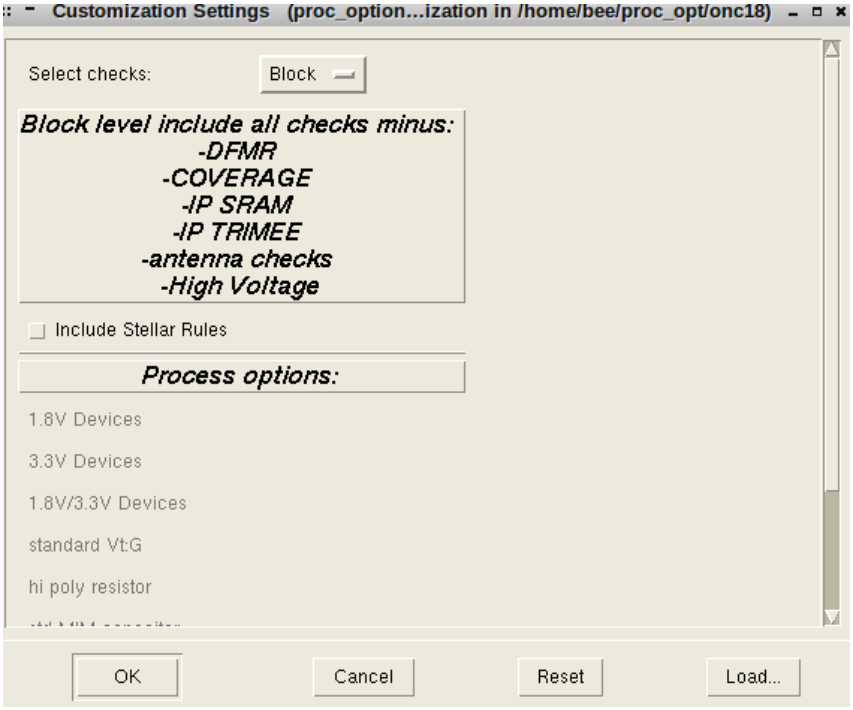


- Click on hide
- Create a rectangle and put the vdd pin in the top m1 bar
- Put sub pin in the bottom m1 bar
- Put the vin in the m1 layer connected to the gates
- Lastly put the vout pin where the m1 one connects to the two drains.

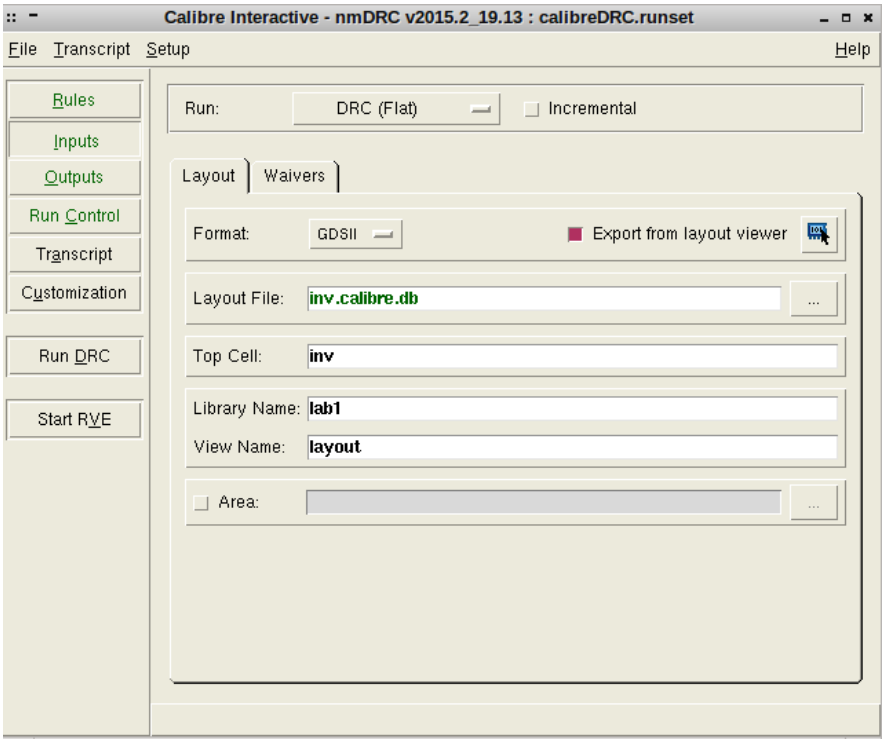


STEP 14: Run DRC

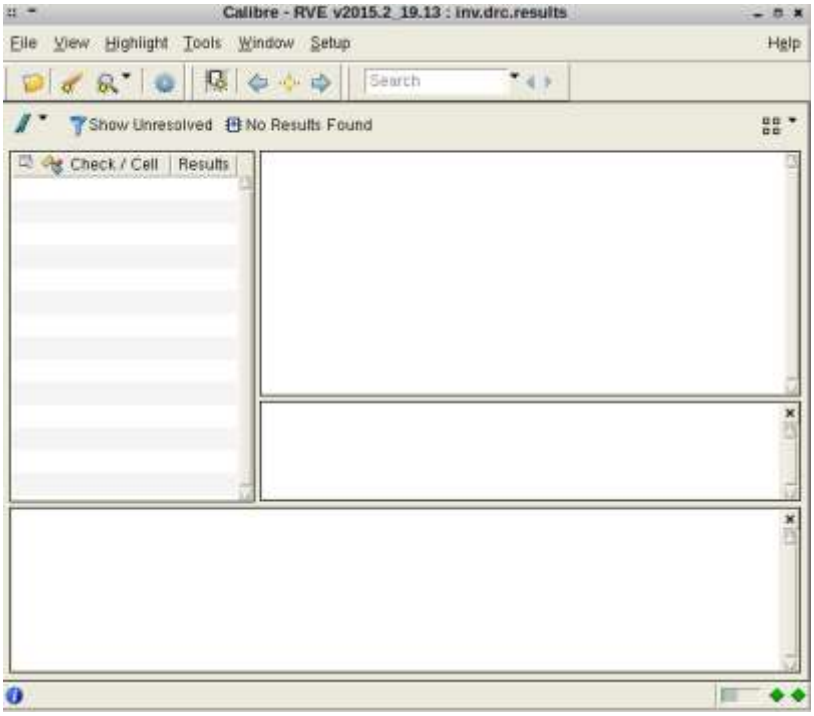
- Save your layout
- Click on Caliber->Run nmDRC
- Choose Block for select checks and press ok



- In the next window click on Run DRC and wait for the result to show up



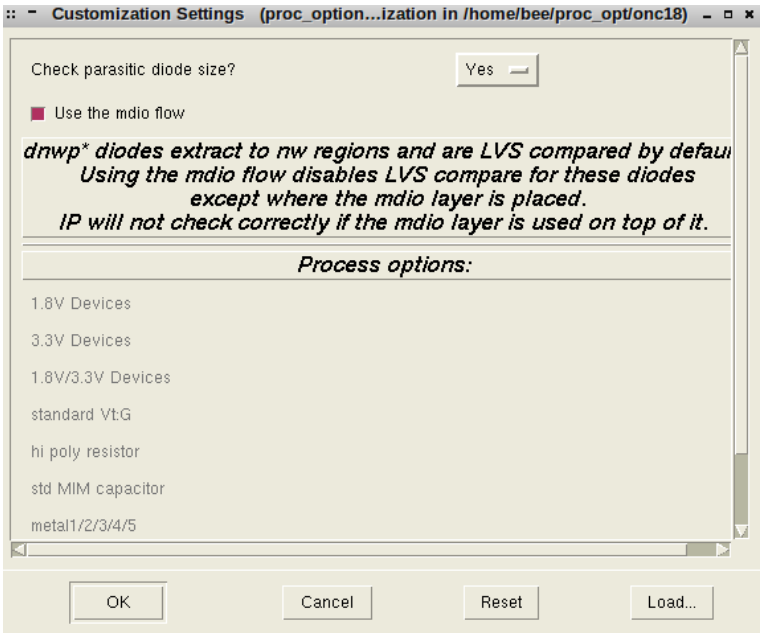
- In the next windows click on show ALL and choose show Unresolved



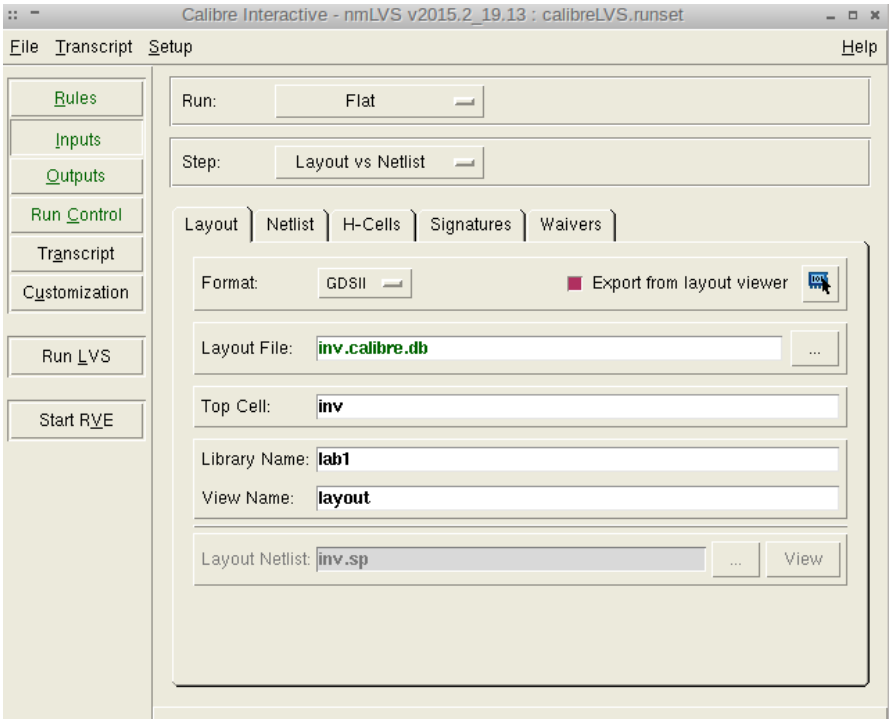
- If there is nothing to show that means the DRC has passed and you can take a screen shot of this window as you will need to turn this in

STEP 15: Run LVS

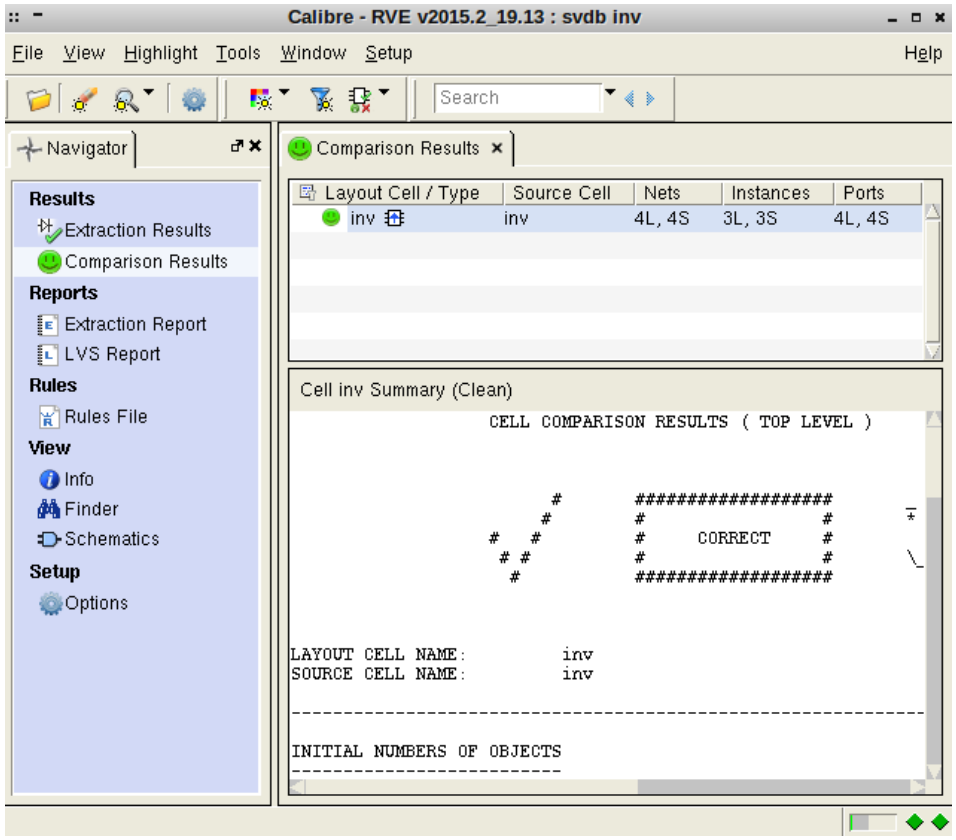
- Click on Caliber->Run nmLVS
- Check use the mido flow(if you forget to do this you will get errors about the diode not being connected to the pmos nwel) and press ok



- In the next window click on Run LVS and wait for the result to show up



- If everything passes you will get a green smiley face



- If all steps were followed carefully, both DRC and LVS should pass with no errors.

Congratulations! You have created a CMOS inverter using TURBO and PCELLS.

What to turn in? Snapshot of your layout and screenshot of successful DRC and LVS window.