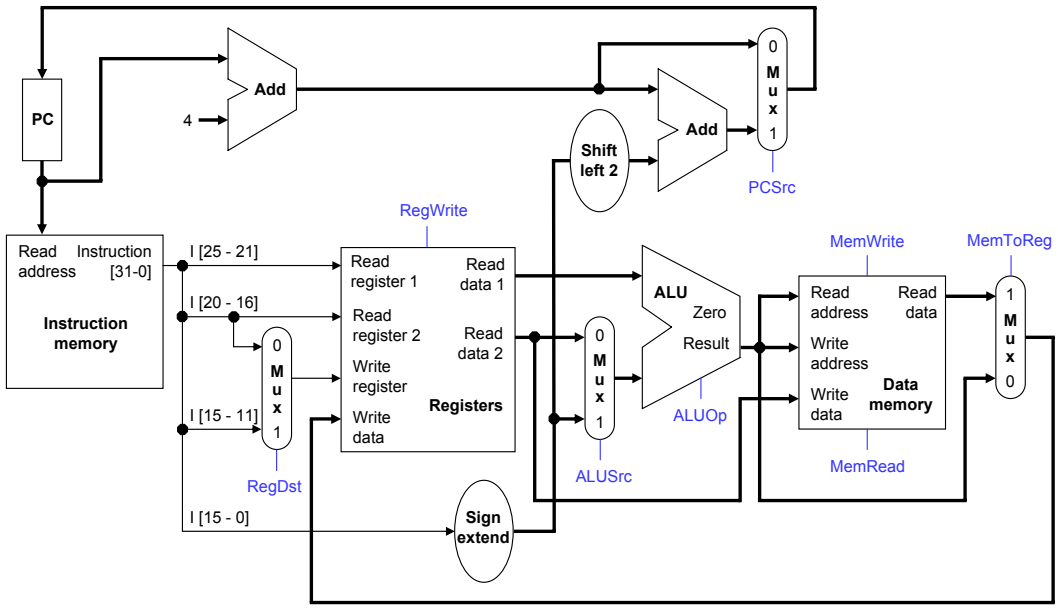
CPEG 323 Practice Final Exam

Question 1: Single-cycle Datapath and Performance



Part 1)

Consider the above single-cycle datapath. We want to implement a new I-type MIPS instruction ***push $rt*** which grows the stack by 4 bytes and stores $rt onto the stack.

Example: The instruction `push $a0` is equivalent to the MIPS instruction sequence: `addi $sp, $sp, -4; sw $a0, 0($sp)`

Question: Make the fewest possible changes to the given datapath to implement the push instruction. Be sure to indicate the value of all control signals, including any new control signals.

Part (2)

The latencies of the component of the single-cycle datapath from Problem 1 are as follows: Memory read/write: 200ps, Register read: 150 ps, Register write: 100ps, ALU: 250ps (all other components have negligible latency, 1 ps = 10^{-12} seconds).

(a) If the clock-cycle time is made as small as possible, what is the clock frequency?

(b) We have to choose between two performance optimizations: either a new ALU (latency 200 ps) or a new memory (latency 100 ps). Which would be a better choice? Justify your answer.

2. Cache :

1.

a) Consider a 2-way set-associative cache that uses 10-bit cache index and has 32-byte cache blocks. If a machine uses 32 bit physical addresses, compute:

- the number of blocks in the cache
- the size of the block offset
- the size of the tag

b) Consider a 2-way set-associative cache with a total of 4 blocks of 4 bytes each (with LRU policy) . What is the hit rate for the following memory accesses?

- 110001
- 100111
- 001111
- 001100
- 010001
- 110010
- 100101
- 001110
- 100001
- 110001

2. (a) **Cache 1:** Given a *direct-mapped* cache with 2 blocks of 2 bytes each, where the address is broken as follows: If the cache was initially empty and the addresses below

Tag	Index	Offset

were accessed in that order, which of the following would be cache misses?
0110 0010 0110 1100 0111 1001 0110 1100 1101

(b) **Cache 2:** Given a fully associative cache (using a least-recently-used replacement policy) with 3 blocks of 2 bytes each, where the address is broken as follows:

Tag	Offset

If the cache was initially empty and the addresses below were accessed in that order, which of the following would be cache misses?
0110 1101 0111 1001 1110 1100 0110 1111 1101

3. Pipelining Datapath

Fill in the datapath values (thick lined boxes) and control signal values (thin lined boxes) for each of the signals on the attached sheet (Figure 2). Use the same conventions that we used in lectures:

- Each register contains its number plus 100. For instance, register $8 contains 108, register $29 contains 129, and so forth.
- Every data memory location contains 99.

Feel free to place an X in any box whose value isn't important, like the constant field of an R-type instruction, but we will give 10 bonus points to anyone who computes those correctly.

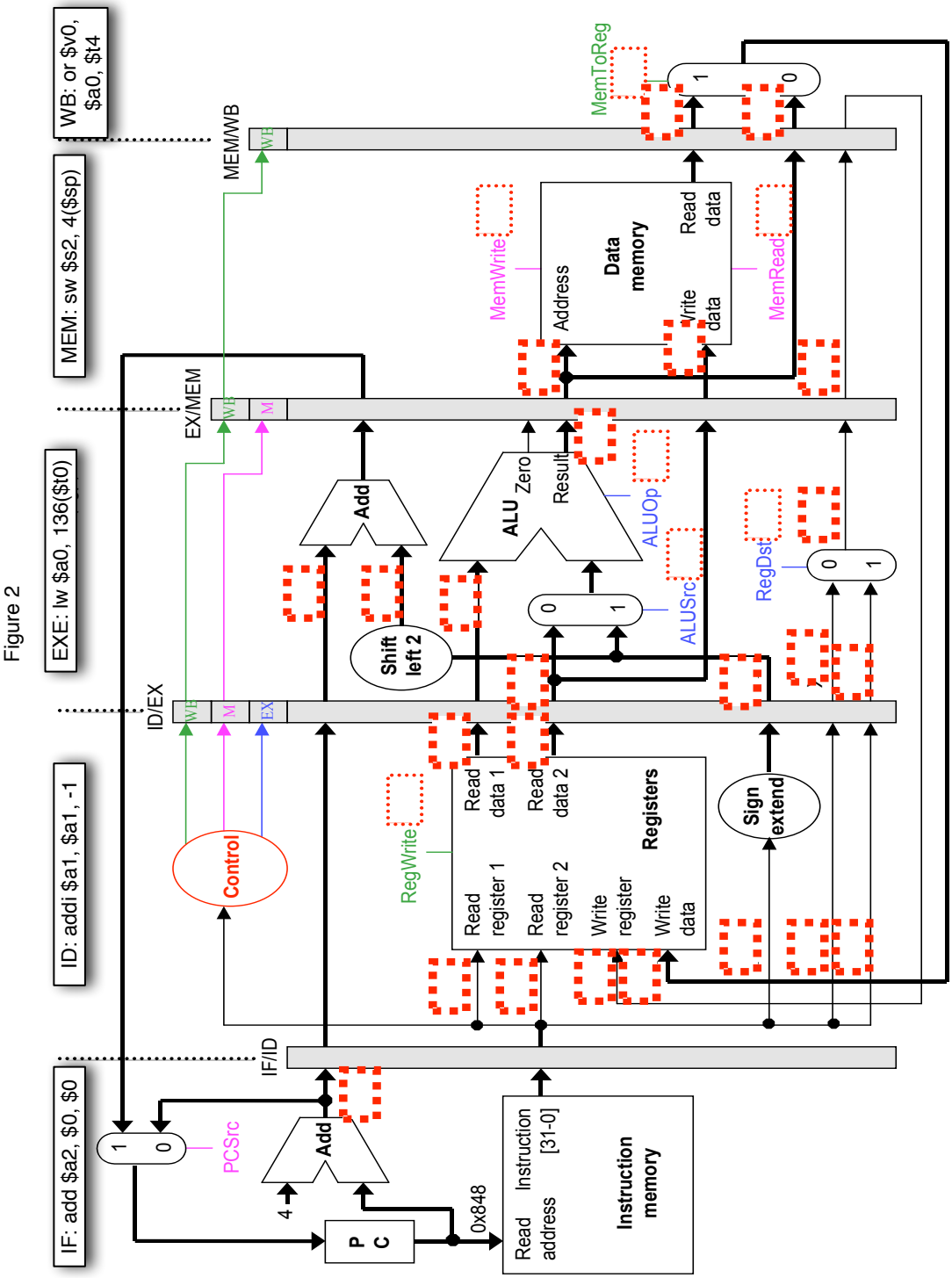

IF: add $a2, $0, $0
ID: addi $a1, $a1, -1
EXE: lw $a0, 136($t0)
MEM: sw $s2, 4($sp)
WB: or $v0, $a0, $t4
IF/ID
ID/EX
EX/MEM
MEM/WB
WB
M
EX
PCSrc
Add
4
P C
0x848
Instruction memory
Read address
Instruction [31-0]
Control
RegWrite
Registers
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Sign extend
Shift left 2
ALU
Zero
Result
ALUOp
ALUSrc
RegDst
MemWrite
MemRead
Data memory
Address
Write data
Read data
MemToReg

Figure 2