LAB3 – Inverter Tutorial: Transistor sizing using DC simulation and parametric analysis

Objectives:
- perform a DC simulation to plot a VTC curve (voltage transfer characteristic) for inverter
- perform a DC simulation and combine it with a parametric analysis to optimize transistor sizes for an inverter

Assumptions:
- Student has successfully completed Lab 1 and 2

1. Login to workstation and open up a terminal, then type:

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Virtuoso &
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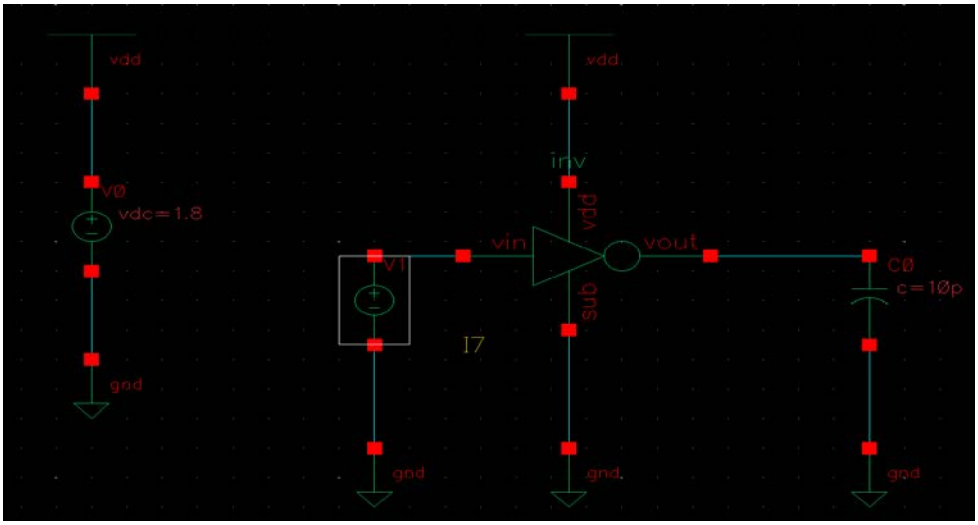
Note: Cadence should start.

2. Open your inverter testbench that you made in the previous lab

From the library manager, double-Click on **lab1->inv_tb->schematic**



3. Change your voltage pulse source into a DC source

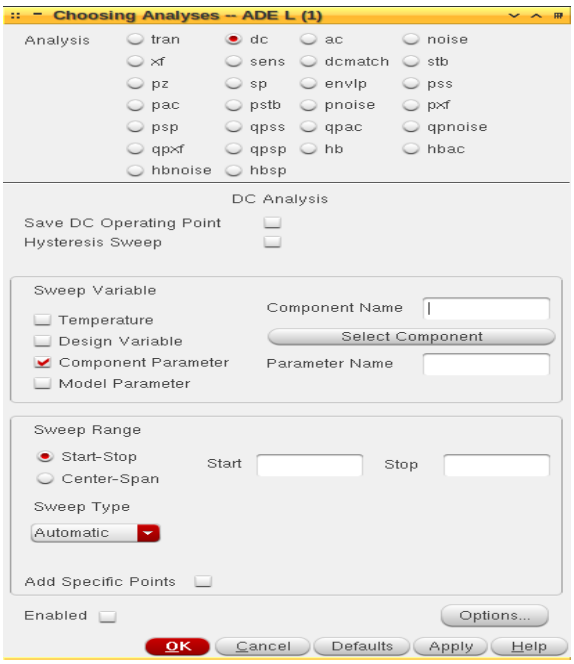
-Select the vpulse source, press **q** to bring up its properties
-In the cell name field, *delete* "*vpulse*" and type: **vdc**
-Press **OK** and your PULSED DC source will change to a DC source

4. Open the analog design environment (ADE)

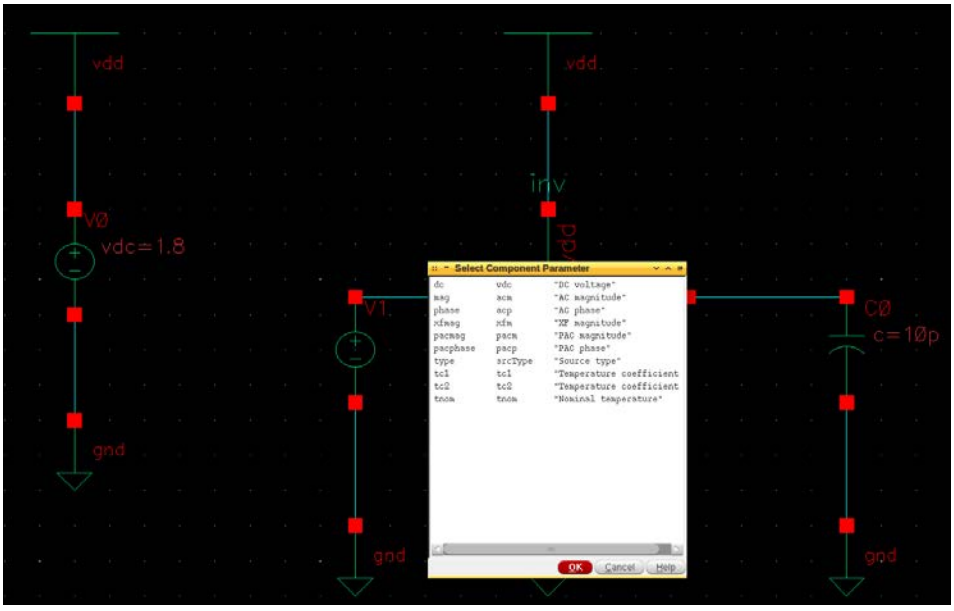
From the schematic editor menu choose: Launch - > **ADE L**

5. *Setup DC analysis*

- Analyses->choose…
- Set the **analyses** type to: **DC** and the form will change.
- Select x **Component Parameter** in the Sweep Variable List



- Press the “Select Component” button on the form
- The simulator is now waiting for you to select a component from the schematic
  - click on the schematic editor window
  - click on the dc voltage source connected to the input of your inverter
  - a menu will appear, asking you which “parameter” of the DC voltage source you wish to sweep
  - select the “DC Voltage” or dc parameter from the list and press OK



- the DC analysis window will return to the forefront, with your sweep variable: dc, filled in
- set the sweep range for the “dc” variable to:
    - Start: 0, Stop: 1.8 (this sets your x-axis values)
- press OK

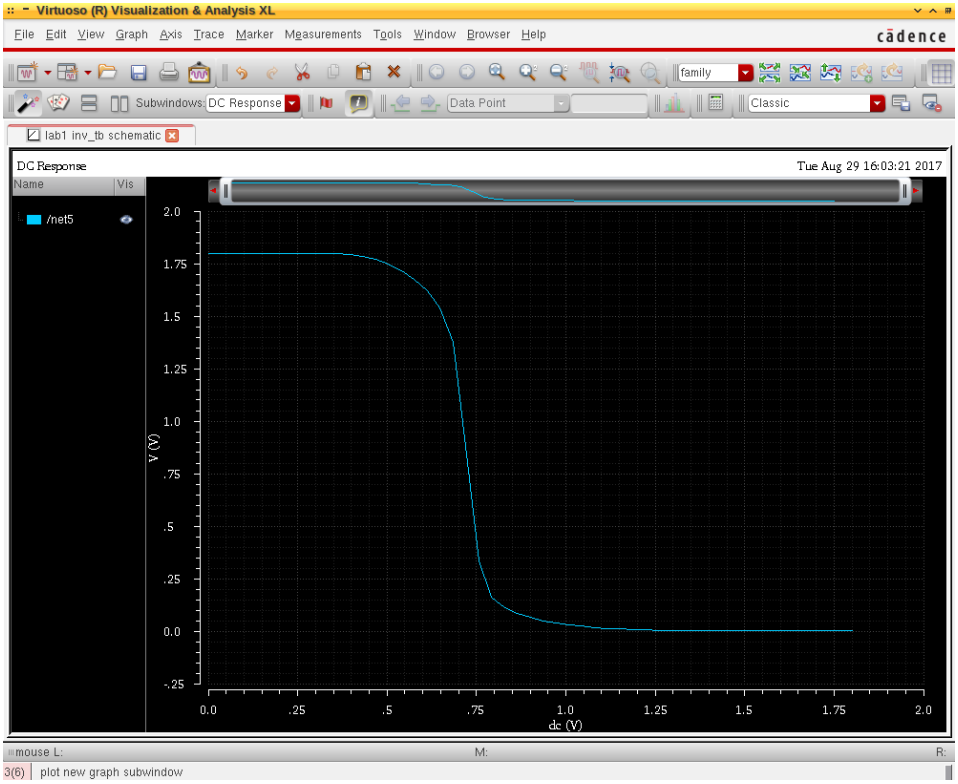
- you have now setup an analysis that will sweep the input voltage source from 0 volts to 1.8 volts

6. *Choosing which outputs to plot*

- In the simulator window, choose Outputs -> To be plotted -> Select on schematic
- In the schematic window, click on the output net (the wire) of the inverter which is connected to the capacitor.
- Run the simulation by clicking on the “Run Simulation” icon

7. Interpreting output

- The plot window will appear showing the voltage across the capacitor (the load) on the y-axis, vs. the input voltage to the inverter, swept from 0 to 1.8 volts, on the x-axis
- Press the “m” key and click anywhere on the curve
- You can move this “marker” anywhere on the curve, to determine the x-y coordinates, by dragging it with your mouse.
- Make the x-coordinate: 0.9 and determine the y-coordinate.
- This graph is known as the voltage transfer characteristic curve and it will be studied in ece 126 lecture.



Because our NMOS and PMOS have different resistance values when they are “ON” when x=0.9 volts, y is not equal to 0.9. We must change the size of our devices to make the “ON” resistance of the PMOS and NMOS equal for our inverter. We will do this by using a “parametric” analysis to help us size our devices.

Performing a parametric analysis to size W/L of NMOS and PMOS Devices

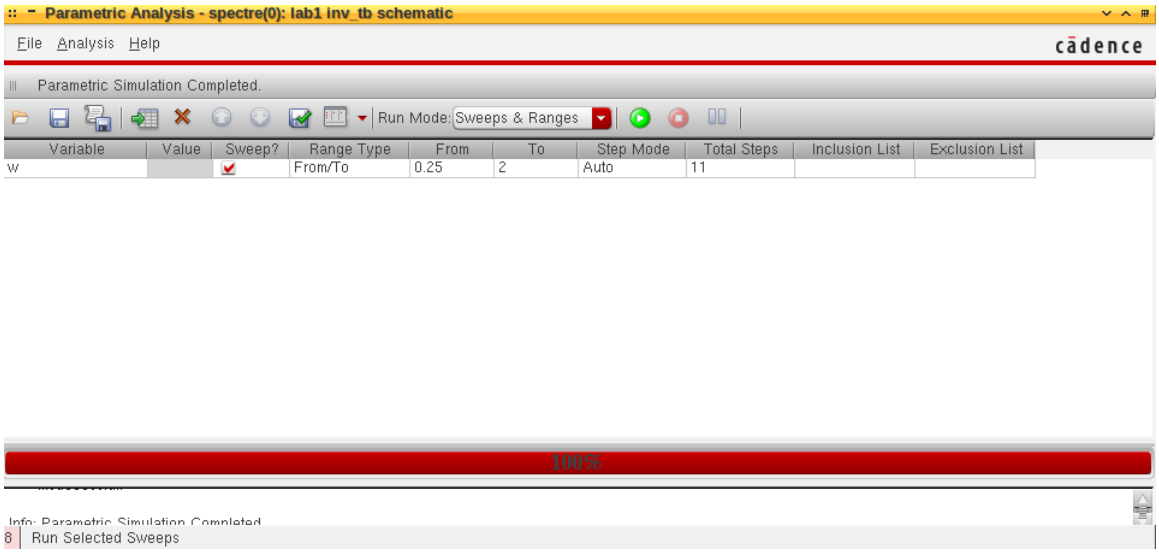
8. Setting up parameter

- Close the output graph, but leave the simulator open so we can use it later
- Return the schematic editor
- Click on your inverter symbol, descend into the transistor level by pressing **E(shift+e)**, and **OK**
  (use Capitol E not lowercase)
- Your inverter schematic will open
- Click on the PMOS transistor. Hit **q** to activate the properties form.
- Change the width to **w**. Hit Apply, then OK. Make sure to save the schematic.
- Press the **CTRL-e** key to go "back" up to the symbol level, save changes
- Press the "Check and Save" icon once your test bench re-appears

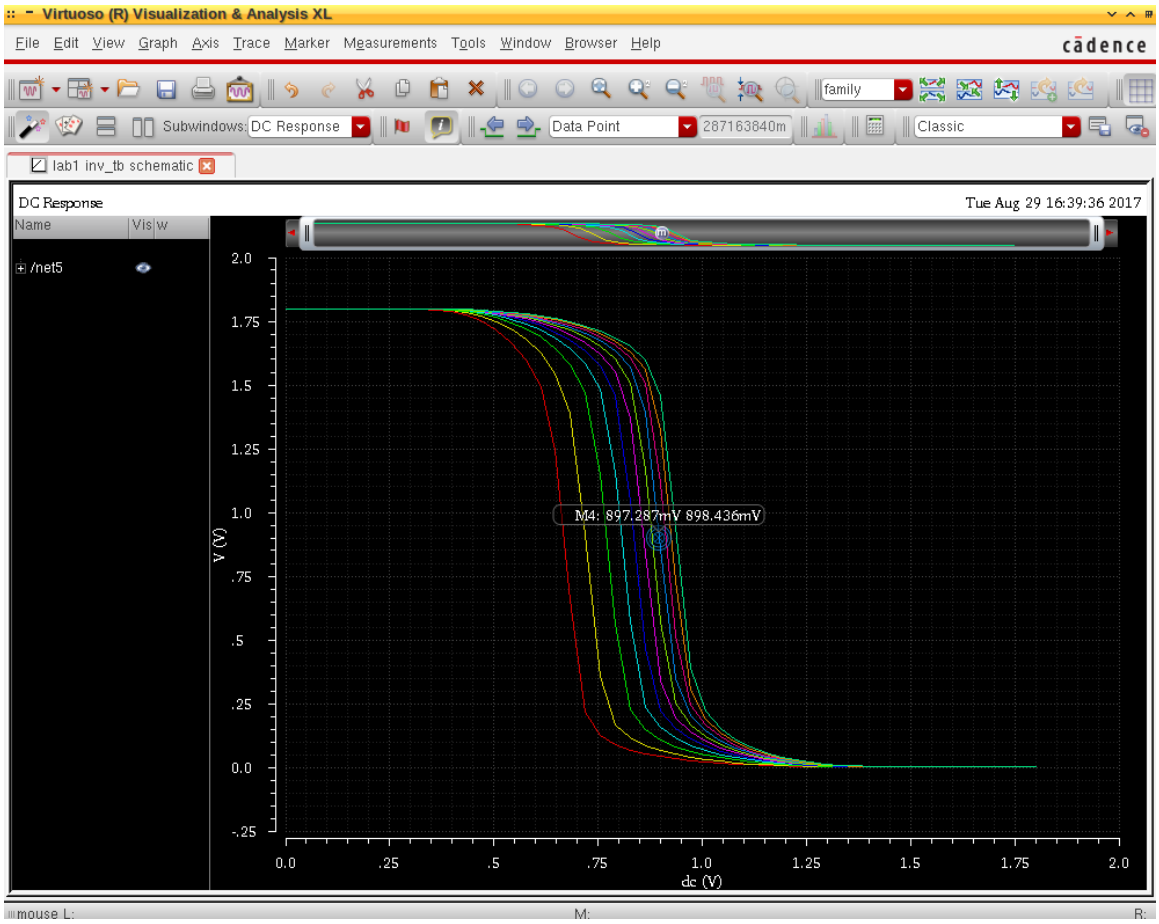
9. Setting up the simulation w/ parameter

- The simulator window is still in the background, click on the simulator window
- From the menu choose: **variables->Copy from cellview…**
  - The variable we created for the width of our pmos device appear in the design variables list
- From the simulator choose **Tools->parametric analyses**. Fill in the form as follows:
  - Double Click on Add Variable and clikc on the drop down arrow and select w

  Variable name: **w**. From 0.25 To 2. Total steps :11
- Click **run selected sweeps** button(green Button)



*Eleven DC analyses will now be performed one after the other. Each DC analysis will use a different value of the parameter: **w** (the width of the PMOS transistor) from 5microns to 15 microns.*



10.Interpreting the output

- Eleven different VTC curves will be plotted (*Vin vs. Vout* of the inverter)
- Each curve represents a DC analysis, using a different value of the **w** parameter
- The value of **w** for each graph is listed along the top of the graph, and it is color coordinated
- From the menu, choose **Trace->Trace Cursor**
- As you place your cursor at any point on any of the curves, the x-y coordinates appear in the left hand corner of the graph
- Find which curve has x=y at around 0.9V, and record the value of **w** for that curve
- You may need to re-simulate changing the range of w in step 10, to get closer to x=0.9, y=0.9

Once you have found the value for **w** that makes the output wave pass through the midpoint, 0.9, 0.9, you have properly sized the PMOS transistor to match the NMOS transistor. Essentially, they now have the same value for "**ron**" or their resistance is equal when operating.

- Save your simulation state
- Edit your inverter schematic, and change the PMOS's width to be equal to the value you have found for w.

Future Work:

Once we create a "NAND" gate (in future labs), you may repeat the procedures above tying both of its inputs together to size the transistors in a NAND gate.

Turn in: Screen shot of your final inverter curve (like one above marking the optimum inverter).