

UNIVERSITY *of* DELAWARE

Chapter 7

Transistor Amplifiers





IN THIS CHAPTER YOU WILL LEARN

1. How the transistor (a MOSFET or a BJT) can be used to make an amplifier.
2. How to obtain linear amplification from the fundamentally nonlinear MOS and bipolar transistor.
3. How to model the linear operation of a transistor around a bias point by an equivalent circuit that can be used in the analysis and design of transistor amplifiers.
4. The three basic ways to connect a MOSFET or a BJT to construct amplifiers with different properties.
5. Practical circuits for MOS and bipolar transistor amplifiers that can be constructed using discrete components.



7.1 BASIC PRINCIPLES

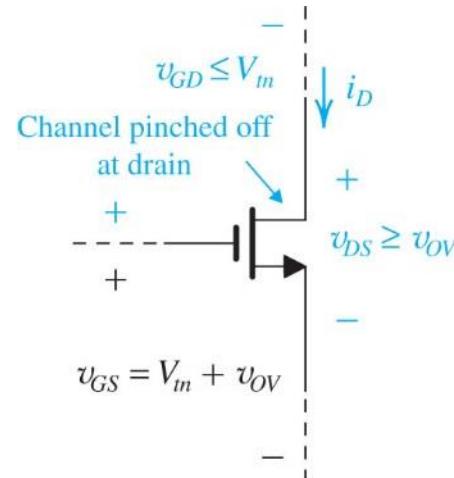


The Basis for Amplifier Operation

Saturation (active) mode:

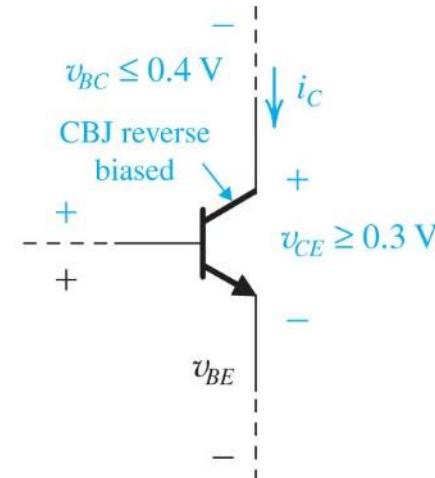
$$v_{DS} \geq v_{OV}$$

$$i_D = \frac{1}{2} k_n (v_{GS} - V_{tn})^2$$



(a)

$$i_D = \frac{1}{2} k_n (v_{GS} - V_{tn})^2$$



(b)

$$i_C = I_S e^{v_{BE}/V_T}$$

Active mode:
 $v_{CE} \geq 0.3 \text{ V}$
results in
 $v_{BC} \leq 0.4 \text{ V}$

$$i_C = I_S e^{v_{BE}/V_T}$$

Figure 7.1 Operating (a) an NMOS transistor and (b) an *n*p*n* transistor in the active mode. Note that $v_{GS} = V_{tn} + v_{OV}$ and $v_{DS} \geq v_{OV}$; thus $v_{GD} \leq V_m$, which ensures channel pinch-off at the drain end. Similarly, $v_{BE} \approx 0.7 \text{ V}$, and $v_{CE} \geq 0.3 \text{ V}$ results in $v_{BC} \leq 0.4 \text{ V}$, which is sufficient to keep the CBJ from conducting.



Obtaining a Voltage Amplifier

the MOSFET operates as a **voltage-controlled current source (VCCS)** with the control relationship described by:

$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2 (1 + \lambda_{DS}) \approx \frac{1}{2} k_n (v_{GS} - V_t)^2$$

This is a transconductance amplifier. A simple way to convert a transconductance amplifier to a voltage amplifier is to pass the output current through a resistor and take the voltage across the resistor as the output.

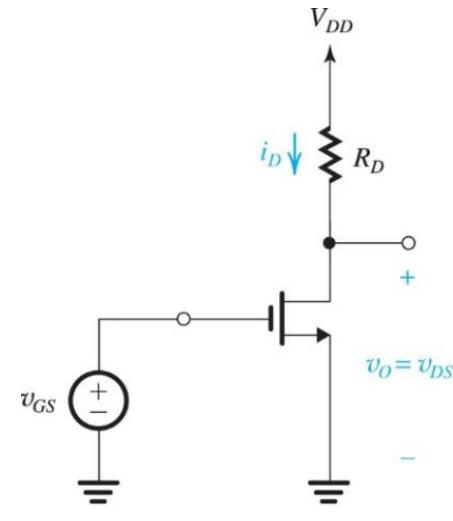
The output voltage is taken between the drain and ground, rather than simply across R_D . This is done because of the need to maintain a ground reference throughout the circuit.

The output voltage is given by:

$$v_O = v_{DS} = V_{DD} - i_D R_D$$

In the active region

$$v_O = v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_{tn})^2$$



(a)

Figure 7.2 (a) An NMOS amplifier.



The Voltage Transfer Characteristic

The **Voltage Transfer Characteristic (VTC)** is a plot of the output voltage versus the input voltage.

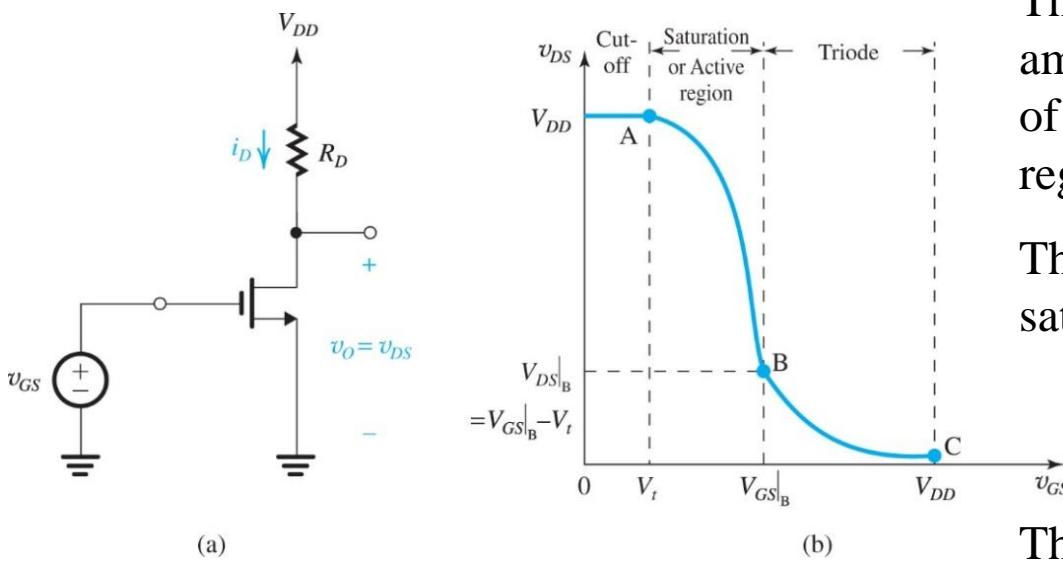


Figure 7.2 (a) An NMOS amplifier and (b) its VTC.

Point B can be found to be:

$$V_{GS}|_B = V_t + \frac{\sqrt{2k_n R_D V_{DD} + 1} - 1}{k_n R_D} \Rightarrow V_{OV}|_B = V_{GS}|_B - V_t = \frac{\sqrt{2k_n R_D V_{DD} + 1} - 1}{k_n R_D} \Rightarrow V_{DS}|_B = V_{OV}|_B$$



Voltage Transfer Curves

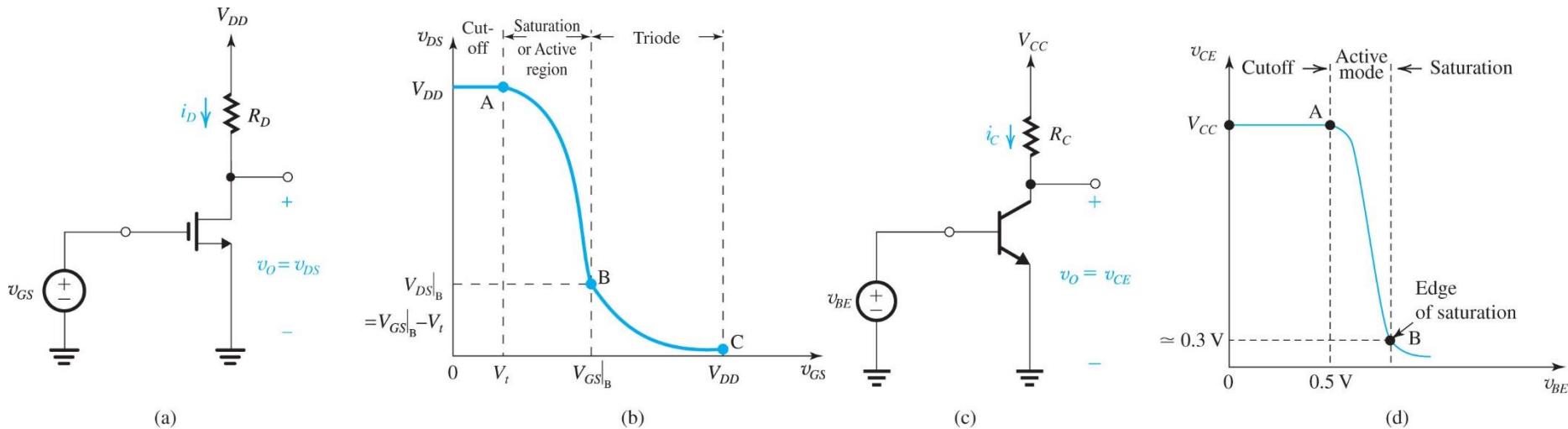


Figure 7.2 (a) An NMOS amplifier and (b) its VTC; and (c) an *npn* amplifier and (d) its VTC.

$$v_O = v_{DS} = V_{DD} - i_D R_D$$

In the saturation/active region

$$v_O = v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_{tn})^2$$

$$v_O = v_{CE} = V_{CC} - i_C R_C$$

In the active region

$$v_O = v_{CE} = V_{CC} - R_C I_S e^{v_{BE}/V_T}$$



Biasing for Linear Amplification

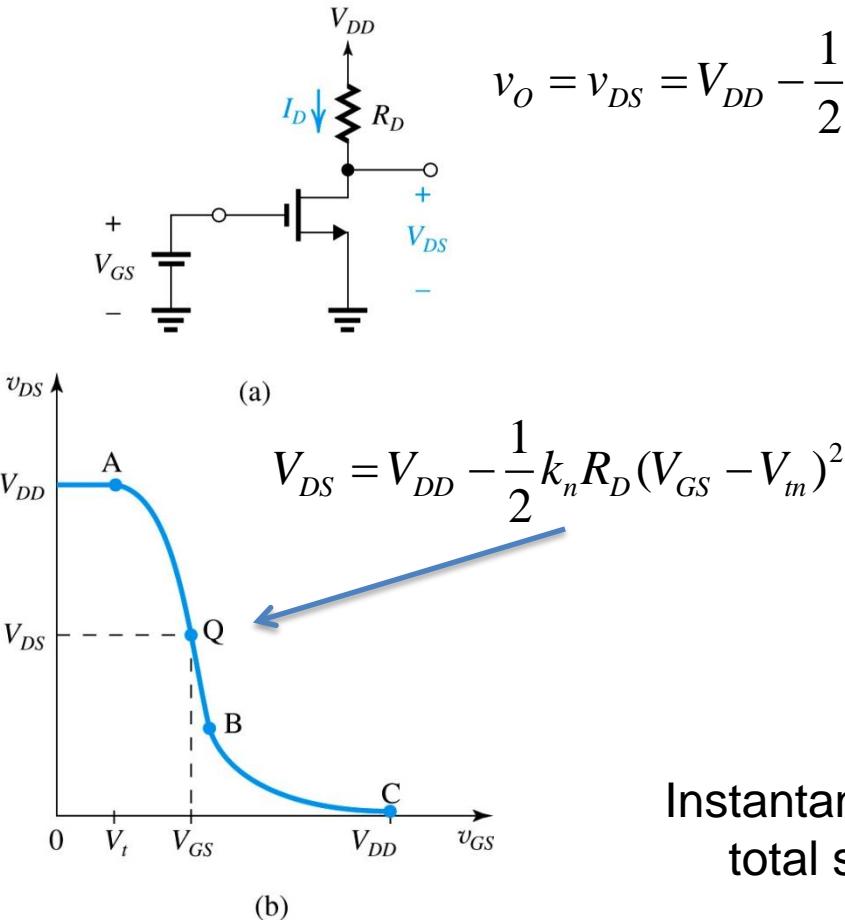


Figure 7.3 Biasing the MOSFET amplifier at a point Q located on the segment AB of the VTC.

$$v_O = v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_{tn})^2$$

The response is obviously nonlinear

Biassing enables us to obtain almost-linear amplification from the MOSFET. The technique is illustrated in Fig. 7.3. A dc voltage V_{GS} is selected to obtain operation at a point Q (the quiescent, or bias point) on the segment AB of the VTC. Next, the signal to be amplified, v_{gs} , is superimposed on the bias voltage:

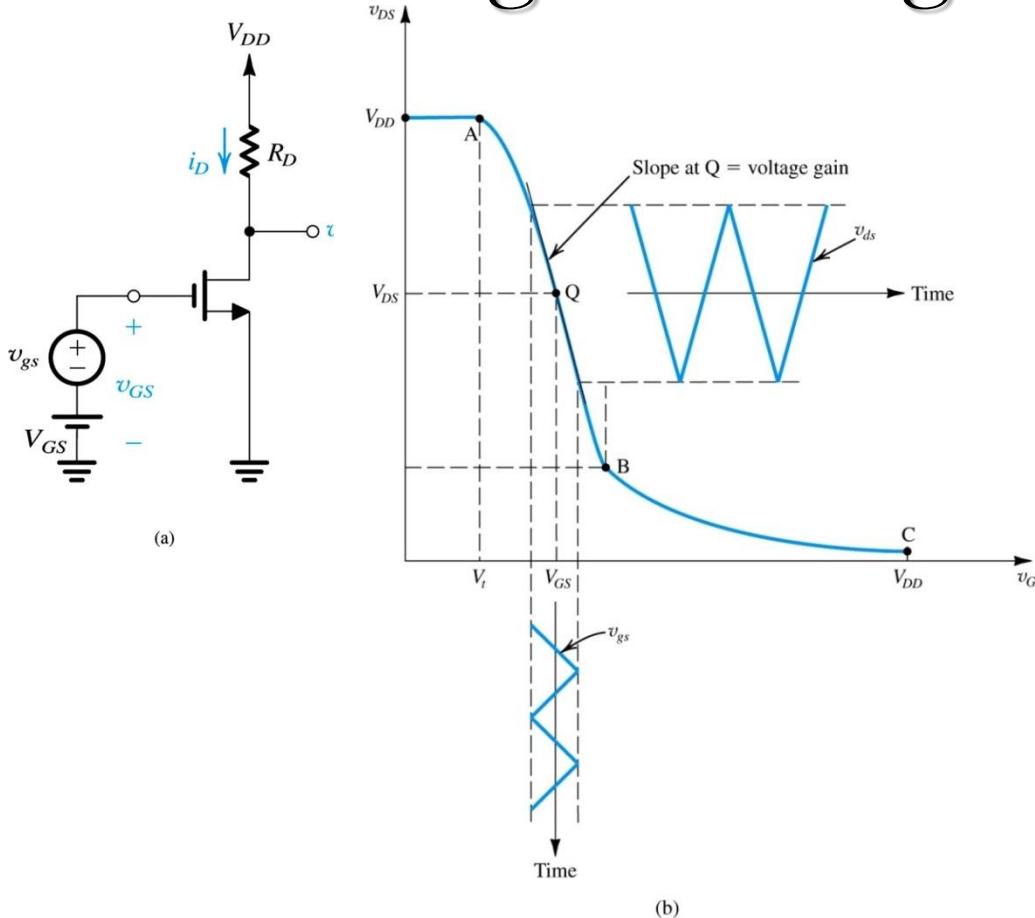
Instantaneous or total signal

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

DC or bias voltage (Q – point) AC or signal voltage (small)



Small Signal Voltage Gain - MOSFET



Next, the signal to be amplified, v_{gs} , is superimposed on the bias voltage:

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

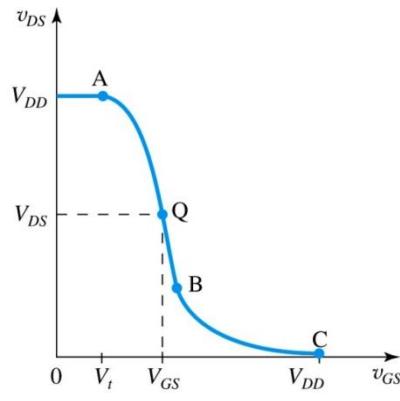
The amplitude of v_{gs} is small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q. The shorter the segment, the greater the linearity achieved. This is the essence of obtaining linear amplification from the nonlinear MOSFET.

Figure 7.4 The MOSFET amplifier with a small time-varying signal $v_{gs}(t)$ superimposed on the dc bias voltage V_{GS} . The MOSFET operates on a short almost-linear segment of the VTC around the bias point Q and provides an output voltage $v_{ds} = A_v v_{gs}$.



The Small-Signal Voltage Gain

If the input signal v_{gs} is kept small, the corresponding signal at the output v_{ds} will be nearly proportional to v_{gs} with the constant of proportionality being the slope of the almost-linear segment of the VTC around Q. This is the voltage gain of the amplifier, and its value can be determined by evaluating the slope of the tangent to the VTC at the bias point Q .



(b)

$$A_v = \frac{dv_{DS}}{dv_{GS}} \Big|_{v_{GS} = V_{GS}} = \frac{d \left[V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_t)^2 \right]}{dv_{GS}}$$

$$A_v = -k_n R_D (v_{GS} - V_t) = -k_n R_D V_{OV}$$

Two important observations:

- 1) The amplifier is inverting (180° phase shift).
- 2) The gain is related to the load resistance, the MOSFET transconductance parameter, and the overdrive voltage (gate to source voltage above the threshold voltage).



The Small-Signal Voltage Gain

$$A_v = -k_n R_D (v_{GS} - V_t) = -k_n R_D V_{OV}$$

Another way to look at the small signal voltage gain is:

$$I_D = \frac{1}{2} k_n V_{OV}^2 \quad \Rightarrow A_v = -\frac{V_{DD} - V_{DS}}{V_{OV}/2} = -\frac{I_D R_D}{V_{OV}/2} = -\frac{2I_D R_D}{V_{OV}}$$

That is, the gain is simply the ratio of the dc voltage drop across the load resistance R_D to $V_{OV}/2$. This relationship allows one to find an absolute upper limit on the magnitude of voltage gain achievable from this amplifier circuit. Simply note that $I_D R_D$ can approach but never exceed the power-supply voltage V_{DD} ; thus,

$$|A_{v\max}| = -\frac{V_{DD}}{V_{OV}/2} = -\frac{2V_{DD}}{V_{OV}}$$



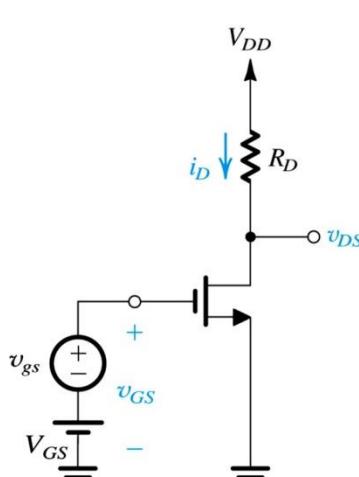
Example 7.1a

Consider the amplifier circuit shown in Fig. 7.4(a). The transistor is specified to have $V_t = 0.4 \text{ V}$, $k'_n = 0.4 \text{ mA/V}^2$, $W/L = 10$, and $\lambda = 0$.

Also, let $V_{DD} = 1.8 \text{ V}$, $R_D = 17.5 \text{ k}\Omega$, and $V_{GS} = 0.6 \text{ V}$.

(a) For $v_{gs} = 0$ (and hence $v_{ds} = 0$), find V_{OV} , I_D , V_{DS} , and A_v .

(b) What is the maximum symmetrical signal swing allowed at the drain? Hence, find the maximum allowable amplitude of a sinusoidal v_{gs} .



$$V_{OV} = V_{GS} - V_{tn} = 0.6\text{V} - 0.4\text{V} = 0.2\text{V}$$

$$I_D = \frac{1}{2}k'_n \left(\frac{W}{L} \right) V_{OV}^2 = \frac{1}{2} \left(0.4 \frac{\text{mA}}{\text{V}^2} \right) (10) (0.2\text{V})^2 = 0.08\text{mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 1.8\text{V} - 0.08\text{mA} (17.5\text{k}\Omega) = 0.4\text{V}$$

$$A_v = -k_n V_{OV} R_D = -k'_n \left(\frac{W}{L} \right) V_{OV} R_D$$

$$= - \left(0.4 \frac{\text{mA}}{\text{V}^2} \right) (10) (0.2\text{V}) (17.5\text{k}\Omega) = -14 \frac{\text{V}}{\text{V}}$$



Example 7.1b

Consider the amplifier circuit shown in Fig. 7.4(a). The transistor is specified to have $V_t = 0.4 \text{ V}$, $k'_n = 0.4 \text{ mA/V}^2$, $W/L = 10$, and $\lambda = 0$.

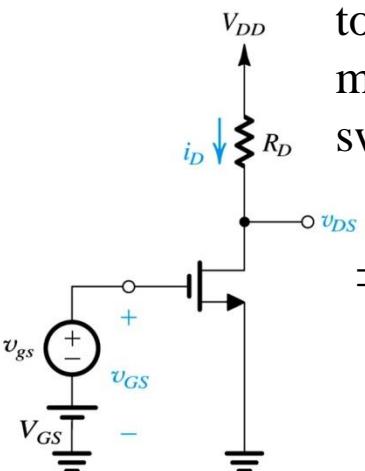
Also, let $V_{DD} = 1.8 \text{ V}$, $R_D = 17.5 \text{ k}\Omega$, and $V_{GS} = 0.6 \text{ V}$.

(b) What is the maximum symmetrical signal swing allowed at the drain? Hence, find the maximum allowable amplitude of a sinusoidal v_{gs} .

$$V_{OV} = 0.2 \text{ V}$$

$$V_{DS} = 0.4 \text{ V}$$

To stay in saturation the maximum allowable negative signal swing at the drain is 0.2 V. It can swing up to V_{DD} on the positive side so the maximum symmetrical output swing about V_{DS} is $\pm 0.2 \text{ V}$.



(a)

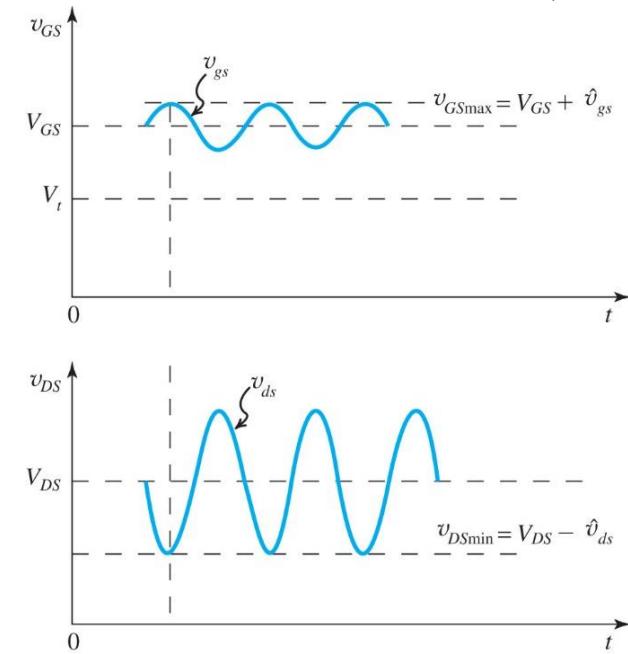


Figure 7.5 Signal waveforms at gate and drain for the amplifier in Example 7.1. Note that to ensure operation in the saturation region at all times, $v_{DS\min} \geq v_{GS\max} - V_t$.



Small-Signal Voltage Gain - BJT

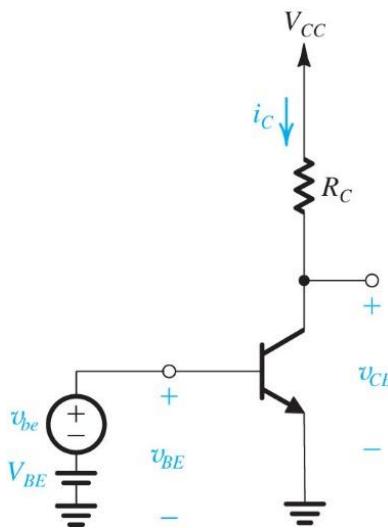


Figure 7.6 BJT amplifier biased at a point Q, with a small voltage signal v_{be} superimposed on the dc bias voltage V_{BE} .

The resulting output signal v_{ce} appears superimposed on the dc collector voltage V_{CE} . The amplitude of v_{ce} is larger than that of v_{be} by the voltage gain A_v .

$$A_v = \left. \frac{dv_{CE}}{dv_{BE}} \right|_{v_{BE} = V_{BE}} = \frac{d[V_{CC} - I_s R_c e^{v_{BE}/V_T}]}{dv_{BE}}$$

$$A_v = -\left(\frac{I_c}{V_T} \right) R_c$$

Two important observations:

- 1) The amplifier is inverting (180° phase shift).
- 2) The gain is proportional to the bias current I_c and to the load resistance R_c .

Another way to look at the small signal voltage gain is:

$$A_v = -\frac{I_c R_c}{V_T} = -\frac{V_{CC} - V_{CE}}{V_T}$$

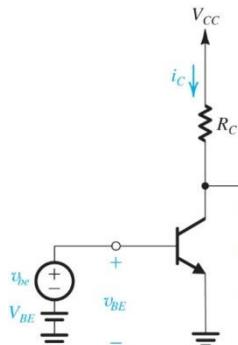
That is, the gain is simply the ratio of the dc voltage drop across the load resistance R_c to V_T .



Example 7.2a

Consider an amplifier circuit using a BJT having $I_S = 10^{-15} \text{ A}$, a collector resistance $R_C = 6.8 \text{ k}\Omega$, and a power supply $V_{CC} = 10 \text{ V}$.

- Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE} = 3.2 \text{ V}$. What is the corresponding value of I_C ?
- Find the voltage gain A_v at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE} , find the amplitude of the output sine-wave signal (assume linear operation).
- Find the positive increment in v_{BE} (above V_{BE}) that drives the transistor to the edge of saturation, where $v_{CE} = 0.3 \text{ V}$.
- Find the negative increment in v_{BE} that drives the transistor to within 1% of cutoff (i.e., to $v_{CE} = 0.99V_{CC}$).



$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{10\text{V} - 3.2\text{V}}{6.8\text{k}\Omega} = 1\text{mA}$$

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) = 25\text{mV} \times \ln\left(\frac{0.001\text{A}}{1 \times 10^{-15} \text{ A}}\right) = 690.8\text{mV}$$



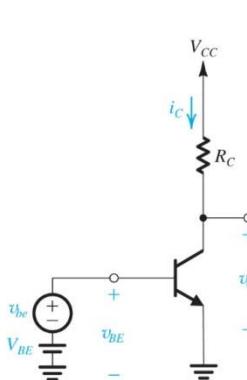
Example 7.2b,c

Consider an amplifier circuit using a BJT having $I_S = 10^{-15} \text{ A}$, a collector resistance $R_C = 6.8 \text{ k}\Omega$, and a power supply $V_{CC} = 10 \text{ V}$.

(b) Find the voltage gain A_v at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE} , find the amplitude of the output sine-wave signal (assume linear operation).

$$A_v = -\frac{V_{CC} - V_{CE}}{V_T} = -\frac{10\text{V} - 3.2\text{V}}{25\text{mV}} = -272 \frac{\text{V}}{\text{V}} \quad \hat{v}_o = |A_v| \hat{v}_i = \left(272 \frac{\text{V}}{\text{V}} \right) (5\text{mV}) = 1.36\text{V}$$

(c) Find the positive increment in v_{BE} (above V_{BE}) that drives the transistor to the edge of saturation, where $v_{CE} = 0.3 \text{ V}$.



$$I_C|_{sat} = \frac{V_{CC} - V_{CEsat}}{R_C} = \frac{10\text{V} - 0.3\text{V}}{6.8\text{k}\Omega} = 1.617\text{mA}$$

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln \left(\frac{I_2}{I_1} \right) = 25\text{mV} \times \ln \left(\frac{1.617\text{mA}}{1.0\text{mA}} \right) = 12\text{mV}$$



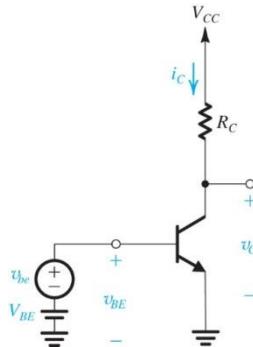
Example 7.2d

Consider an amplifier circuit using a BJT having $I_S = 10^{-15} \text{ A}$, a collector resistance $R_C = 6.8 \text{ k}\Omega$, and a power supply $V_{CC} = 10 \text{ V}$.

(d) Find the negative increment in v_{BE} that drives the transistor to within 1% of cutoff (i.e., to $v_{CE} = 0.99V_{CC}$).

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{10\text{V} - 9.9\text{V}}{6.8\text{k}\Omega} = 0.0147\text{mA}$$

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln\left(\frac{I_2}{I_1}\right) = 25\text{mV} \times \ln\left(\frac{0.0147\text{mA}}{1.0\text{mA}}\right) = -105.5\text{mV}$$





Determining VTC by Graphical Analysis

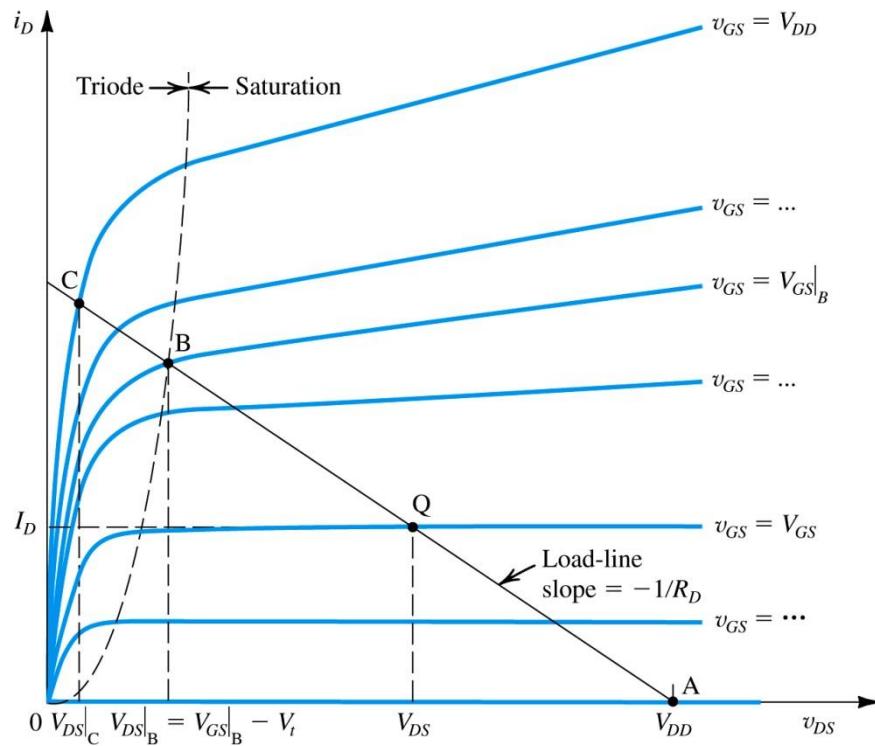


Figure 7.7 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 7.4(a).

The graphical analysis is based on the observation that for each value of v_{GS} the circuit will be operating at the point of intersection of the i_D - v_{DS} graph corresponding to the particular value of v_{GS} and the straight line representing

$$v_{DS} = V_{DD} - i_D R_D$$

which can be rewritten in the form

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS}$$

This line shows the effect of the load resistance and is hence called the **load line**.



Operation of the MOSFET as a SWITCH

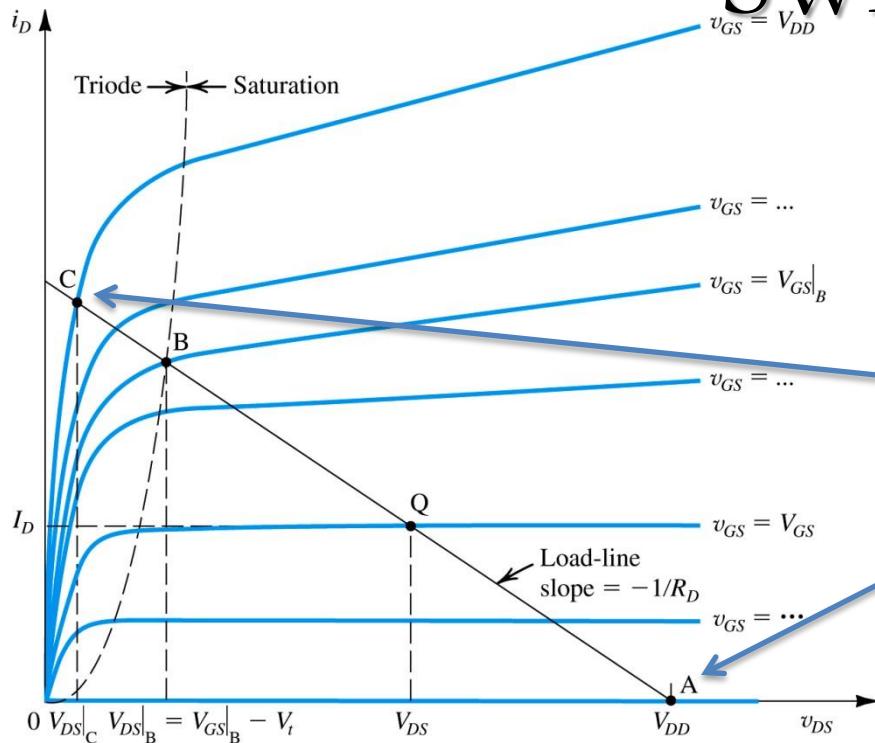


Figure 7.7 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 7.4(a).

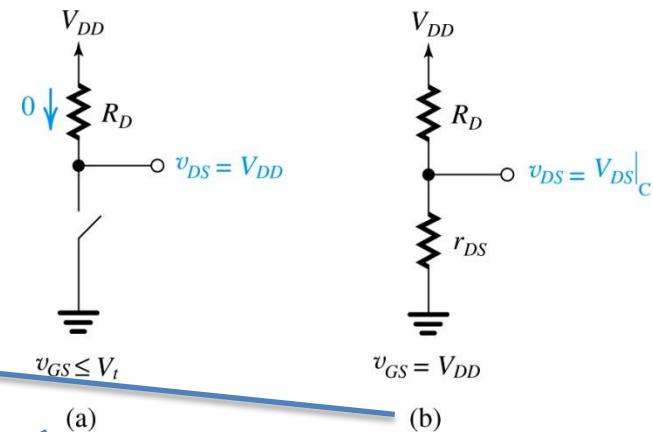


Figure 7.8 Operation of the MOSFET in Figure 7.4(a) as a switch: (a) Open, corresponding to point A in Figure 7.7; (b) Closed, corresponding to point C in Figure 7.7. The closure resistance is approximately equal to r_{DS} because V_{DS} is usually very small.



Locating the Bias Point Q

The bias point Q is determined by the value of V_{GS} and that of the load resistance R_D . Two important considerations in deciding on the location of Q are the required gain and the allowable signal swing at the output.

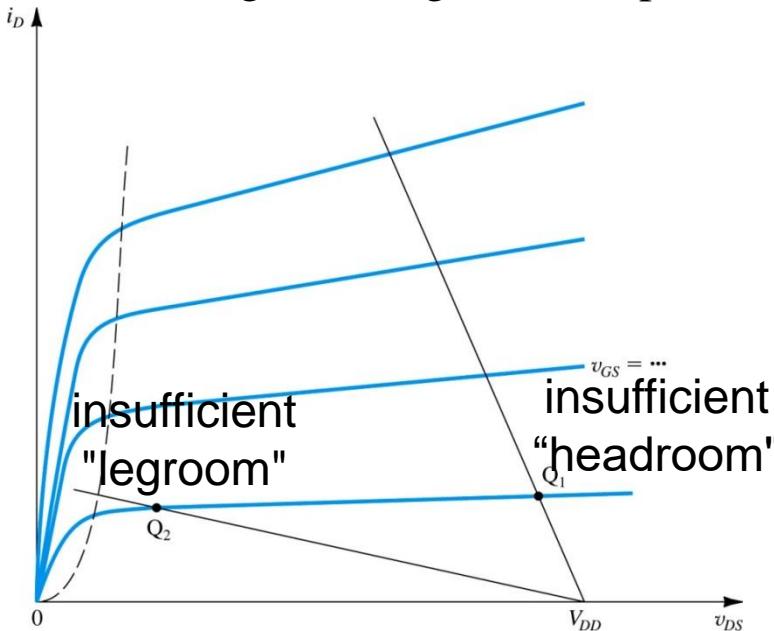


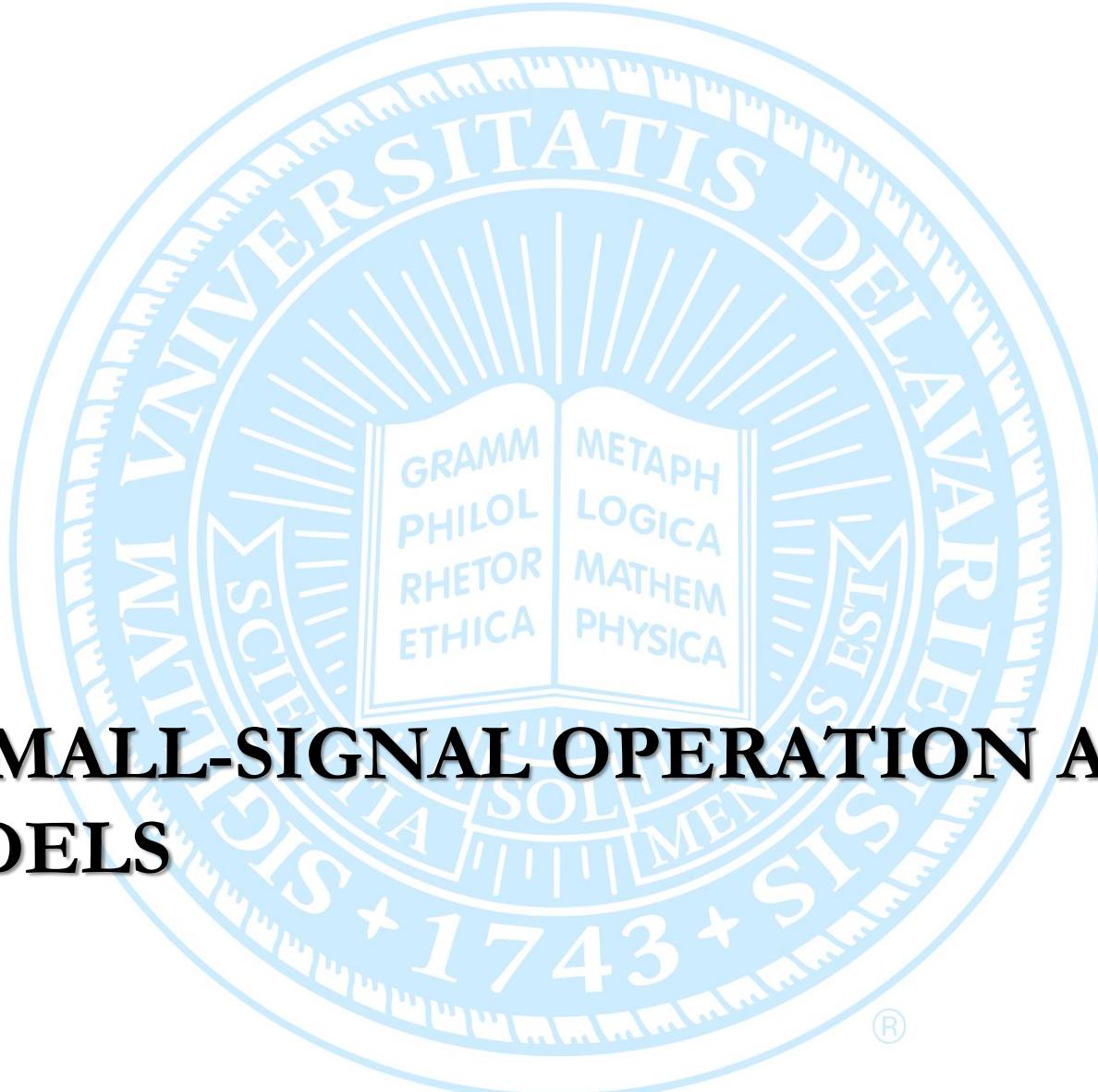
Figure 7.9 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.



Homework #13

- Read Chapter 7
- Chapter 7 Problems:
 - 7.1
 - 7.5
 - 7.6
 - 7.10*
 - 7.18*

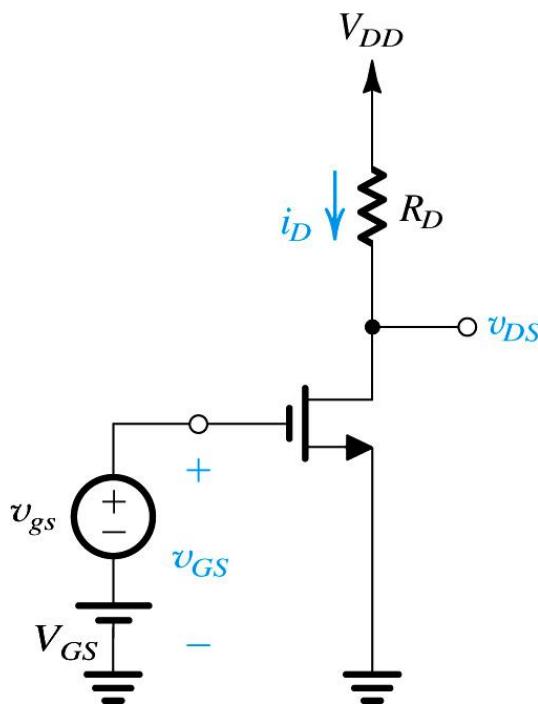
* Answers in Appendix L



7.2 SMALL-SIGNAL OPERATION AND MODELS



MOSFET Small Signal Operation



Here the MOS transistor is biased by applying a dc voltage V_{GS} , and the input signal to be amplified, v_{gs} , is superimposed on the dc bias voltage V_{GS} . The output voltage is taken at the drain. The dc bias current is given by:

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{t_n})^2 = \frac{1}{2} k_n V_{OV}^2$$

The dc bias voltage at the drain is given by:

$$V_{DS} = V_{DD} - I_D R_D$$

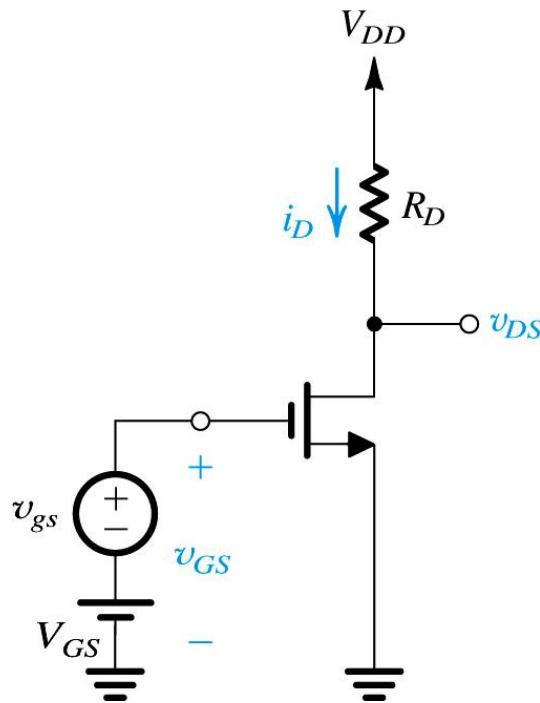
To ensure operation in the saturation region:

$$V_{DS} > V_{OV} = V_{GS} - V_t$$

Figure 7.10 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.



Small Signal Operation



Add the input signal to the dc bias voltage:

$$v_{GS} = V_{GS} + v_{gs}$$

resulting in a total instantaneous drain current:

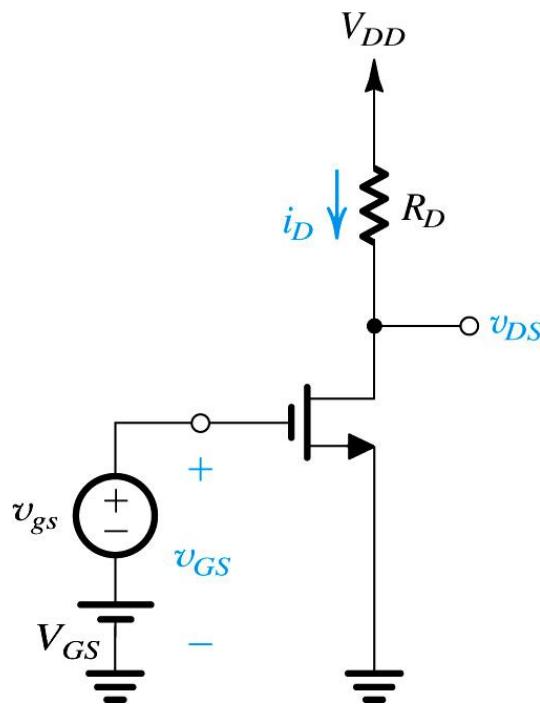
$$i_D = \frac{1}{2} k_n (V_{GS} + v_{gs} - V_{tn})^2$$

$$i_D = \underbrace{\frac{1}{2} k_n (V_{GS} - V_{tn})^2}_{\text{DC component}} + \underbrace{k_n (V_{GS} - V_{tn}) v_{gs}}_{\text{Proportional to input signal}} + \underbrace{\frac{1}{2} k_n v_{gs}^2}_{\text{Distortion}}$$

Figure 7.10 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.



Small Signal Operation



$$i_D = \underbrace{\frac{1}{2}k_n(V_{GS} - V_{tn})^2}_{\text{DC component}} + \underbrace{k_n(V_{GS} - V_{tn})v_{gs}}_{\text{Proportional to input signal}} + \underbrace{\frac{1}{2}k_nv_{gs}^2}_{\text{Distortion}}$$

We want

$$\begin{aligned} \frac{1}{2}k_nv_{gs}^2 &= k_n(V_{GS} - V_{tn})v_{gs} \\ v_{gs} &= 2(V_{GS} - V_{tn}) = 2V_{OV} \end{aligned}$$

If this **small-signal condition** is satisfied, we can neglect the last term leaving us with:

$$i_D \approx I_D + i_d$$

$$i_d = k_n(V_{GS} - V_{tn})v_{gs} = k_nV_{OV}v_{gs}$$

Figure 7.10 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.



Small Signal Operation

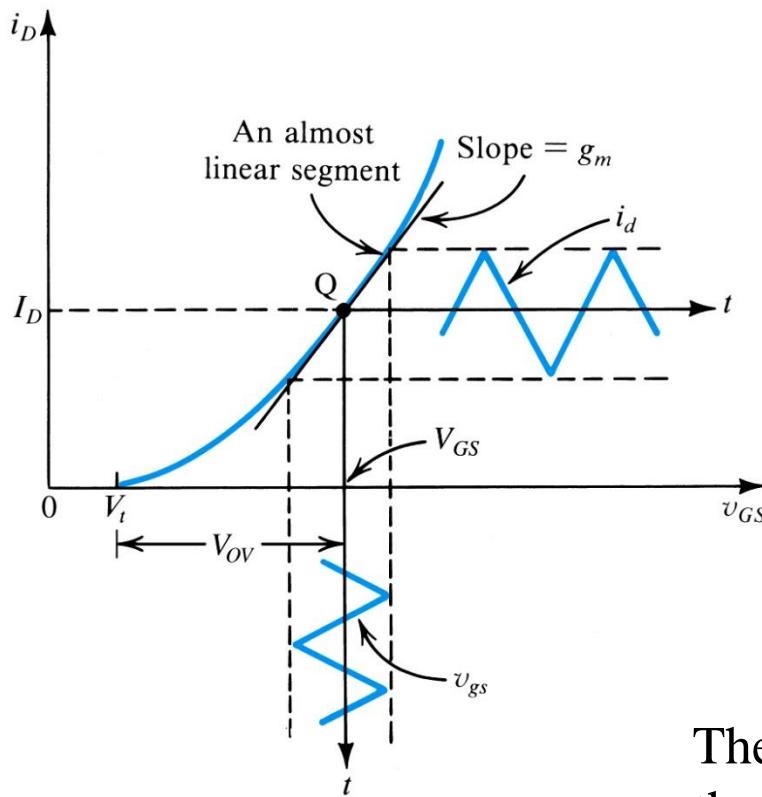


Figure 7.11 Small-signal operation of the MOSFET amplifier.

$$i_d = k_n(V_{GS} - V_{tn})v_{gs} = k_nV_{OV}v_{gs}$$

If we define the MOSFET transconductance, g_m , as

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n(V_{GS} - V_{tn}) = k_nV_{OV}$$

We have the small signal instantaneous current is

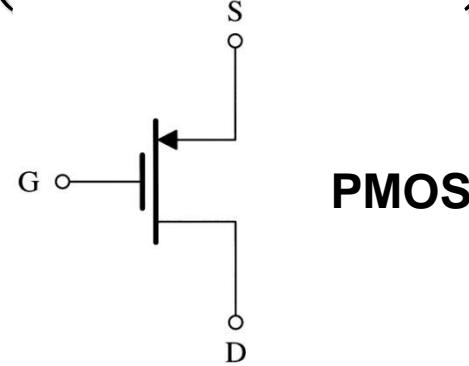
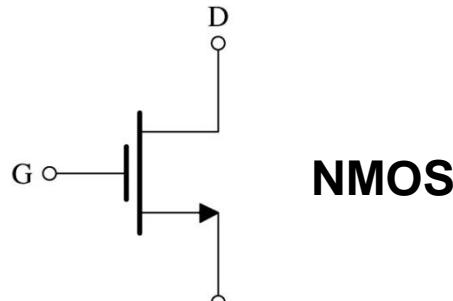
$$i_D \approx I_D + i_d = I_D + g_m v_{gs}$$

The MOSFET transconductance, g_m , is the slope of the tangent of the $i_D - v_{GS}$ curve at the bias, or Q, point.

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GS}}$$



Transconductance (Parameters)



Process transconductance parameter [mA/V²]

$$k'_n = \mu_n C_{ox}$$

$$k'_p = \mu_p C_{ox}$$

MOSFET transconductance parameter [mA/V²]

$$k_n = k'_n \left(\frac{W}{L} \right) = \mu_n C_{ox} \left(\frac{W}{L} \right)$$

$$k_p = k'_p \left(\frac{W}{L} \right) = \mu_p C_{ox} \left(\frac{W}{L} \right)$$

MOSFET transconductance [mA/V]

$$g_m = k_n V_{OV} = k'_n \left(\frac{W}{L} \right) V_{OV} = \mu_n C_{ox} \left(\frac{W}{L} \right) V_{OV}; g_m = k_p V_{OV} = k'_p \left(\frac{W}{L} \right) V_{OV} = \mu_p C_{ox} \left(\frac{W}{L} \right) V_{OV}$$



Small Signal Voltage Gain

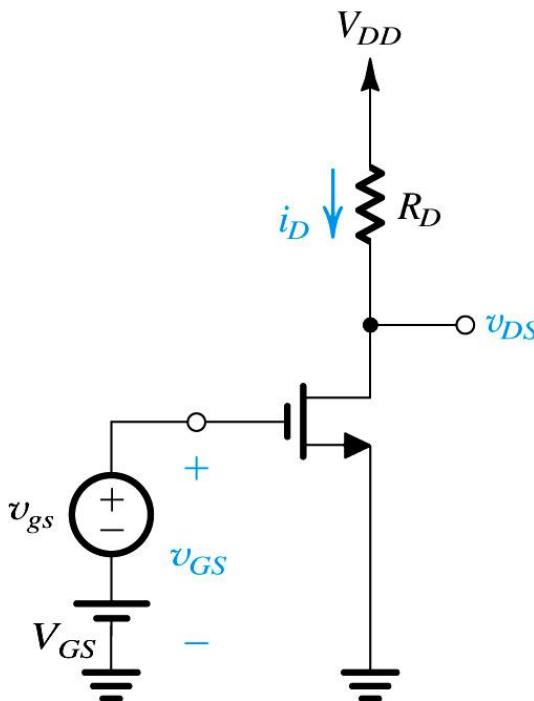


Figure 7.10 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

The total instantaneous voltage at the drain is given by:

$$v_{DS} = V_{DD} - i_D R_D$$

Under the small-signal approximation:

$$\begin{aligned} v_{DS} &= V_{DD} - (I_D + i_d) R_D \\ &= V_{DD} - I_D R_D - i_d R_D \\ &= V_{DS} - i_d R_D \end{aligned}$$

The signal component of the drain voltage is:

$$v_{ds} = -i_d R_D = -g_m v_{gs} R_D$$

The voltage gain is therefore:

$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m R_D$$



Separating the DC Analysis and the Signal Analysis

$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m R_D$$

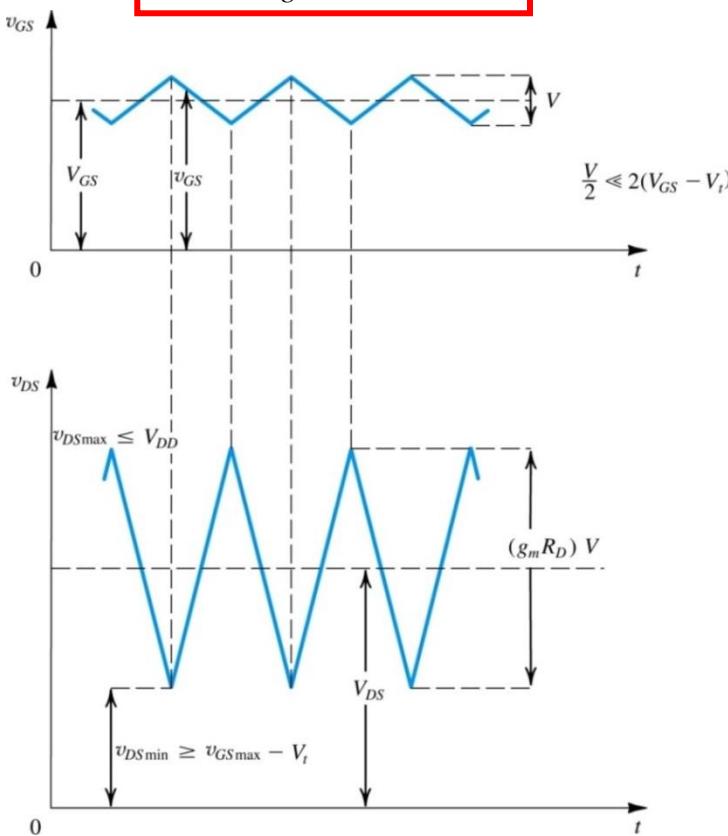


Figure 7.12 Total instantaneous voltages v_{GS} and v_{DS} for the circuit in Fig. 7.10.

From the preceding analysis, we see that under the small-signal approximation, signal quantities are superimposed on dc quantities. For instance, the total drain current i_D equals the dc current I_D plus the signal current i_d , the total drain voltage $v_{DS} = V_{DS} + v_{ds}$, and so on. **It follows that the analysis and design can be greatly simplified by separating dc or bias calculations from small-signal calculations.** That is, once a stable dc operating point has been established and all dc quantities calculated, we may then perform signal analysis ignoring dc quantities.



Small Signal Models for the MOSFET

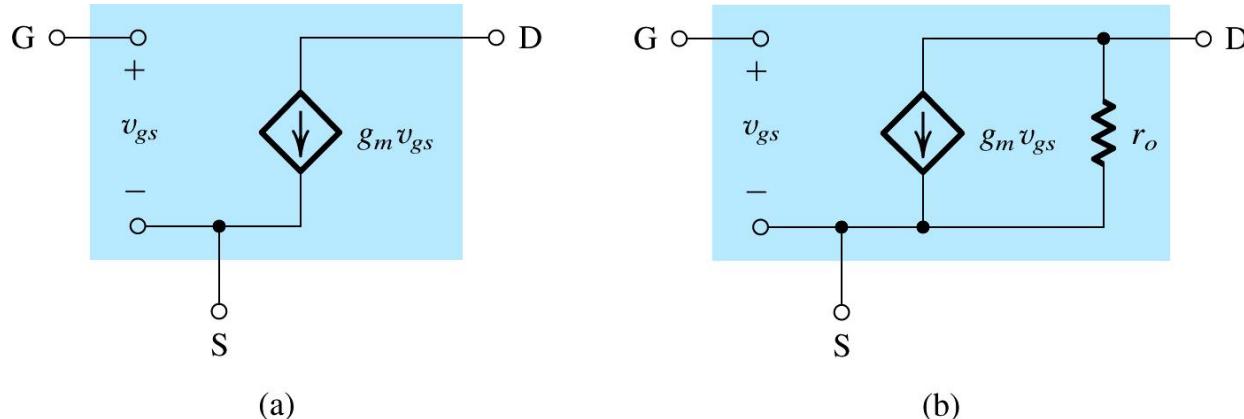


Figure 7.13 Small-signal models for the MOSFET: (a) neglecting the dependence of i_D on v_{DS} in the active region (the channel-length modulation effect) and (b) including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A|/I_D$. These models apply equally well for both NMOS and PMOS transistors.

Typically, r_o is in the range of 10 k Ω to 1000 k Ω . It follows that the accuracy of the small-signal model can be improved by including r_o in parallel with the controlled source, as shown in Fig. 5.37(b). It is important to note that the small-signal model parameters g_m and r_o depend on the dc bias point of the MOSFET. The small signal voltage gain of the previous circuit then becomes:

$$r_o = \frac{|V_A|}{I_D}$$

$$g_m = k_n V_{OV} = \frac{2I_D}{V_{OV}}$$

$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m (R_D \parallel r_o)$$



The Transconductance g_m

$$g_m = k_n V_{OV} = k'_n \left(\frac{W}{L} \right) V_{OV} = \mu_n C_{ox} \left(\frac{W}{L} \right) V_{OV}$$

or

$$g_m = k'_n \left(\frac{W}{L} \right) \sqrt{\frac{2I_D}{k'_n \left(\frac{W}{L} \right)}} = \sqrt{2k'_n} \sqrt{(W/L)} \sqrt{I_D}$$

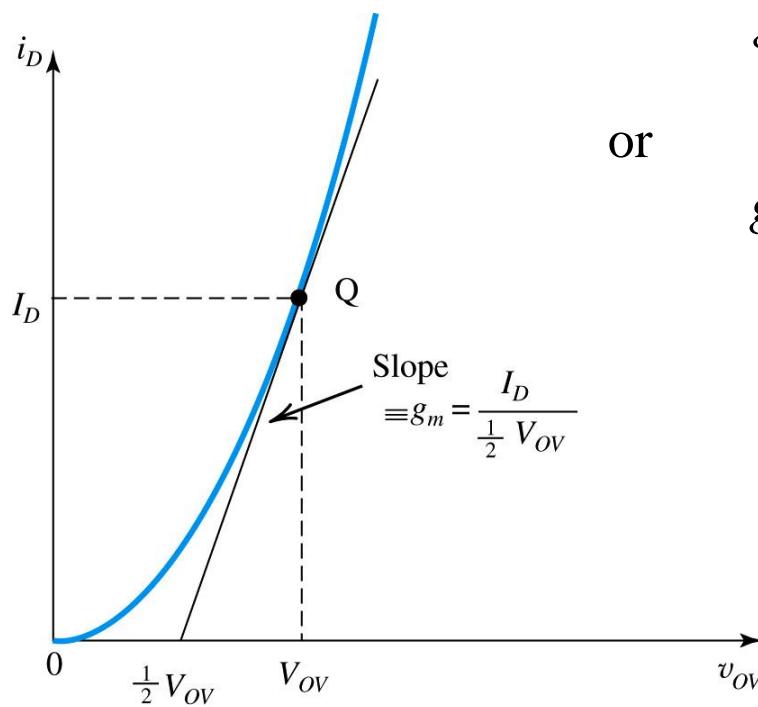


Figure 7.14 The slope of the tangent at the bias point

Q intersects the v_{OV} axis at $1/2V_{OV}$. Thus, $g_m = I_D/(1/2V_{OV})$.

This expression shows two things:

1. For a given MOSFET, g_m , is proportional to the square root of the dc bias current.
2. At a given bias current, g_m , is proportional to $\sqrt{W/L}$.

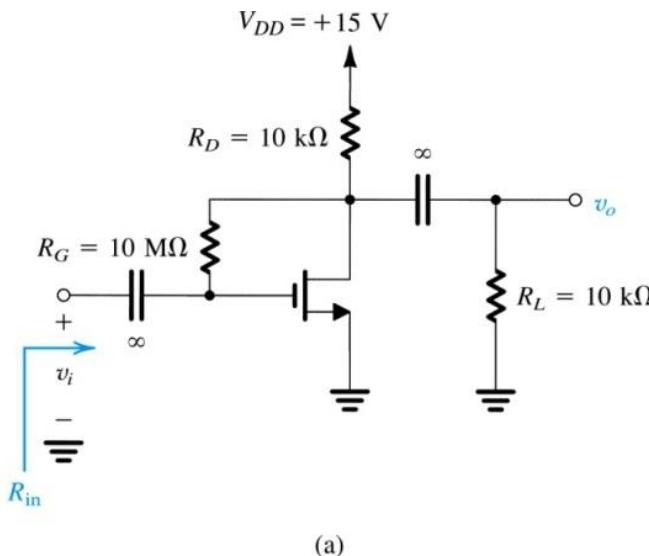
or

$$g_m = \frac{2I_D}{V_{OV}}$$



Example 7.3a

Figure 7.15(a) shows a discrete common-source MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k'_n(W/L) = 0.25$ mA/V², and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.



To find the dc operating point we open circuit the capacitors (they block dc) resulting in

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D$$

Note: no current flows into the gate and the device is in saturation.

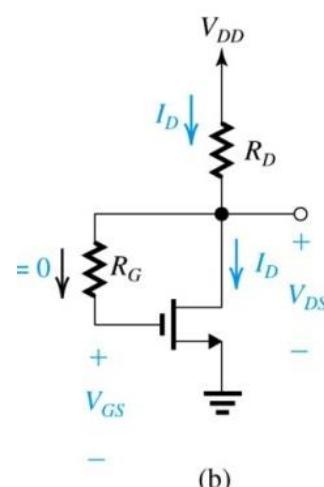


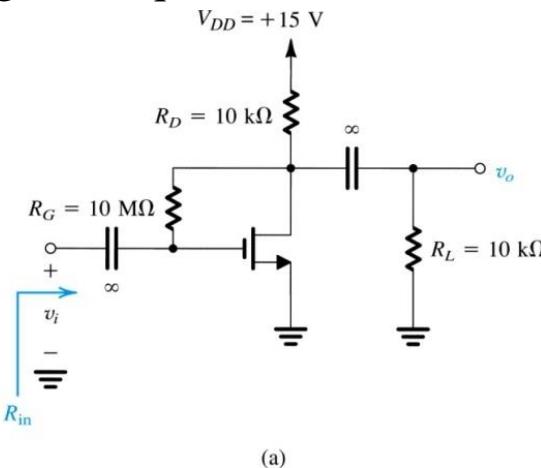
Figure 7.15 Example 7.3: (a) amplifier circuit;
Ch 7. Transistor Amplifiers

R. Martin

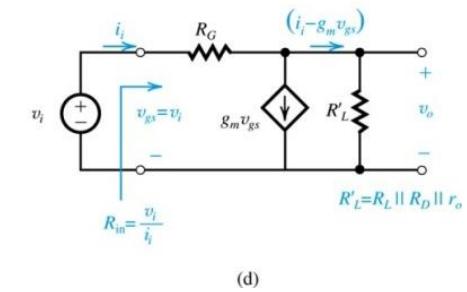
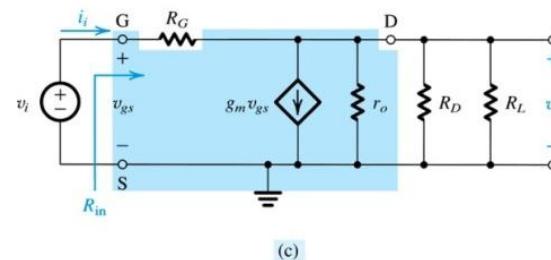


Example 7.3b

Figure 7.15(a) shows a discrete common-source MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V², and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.



Next perform a small-signal analysis



$$g_m = k_n V_{OV} = 0.725 \text{ mA/V}$$

$$r_o = \frac{V_A}{I_D} = \frac{50\text{V}}{1.06\text{mA}} = 47\text{k}\Omega$$

Figure 7.15 Example 7.3: (a) amplifier circuit; (b) circuit for determining the dc operating point; (c) the amplifier small-signal equivalent circuit; (d) a simplified version of the circuit in (c).



Example 7.3c

Figure 7.15(a) shows a discrete common-source MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 7.4. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k_n'(W/L) = 0.25$ mA/V², and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

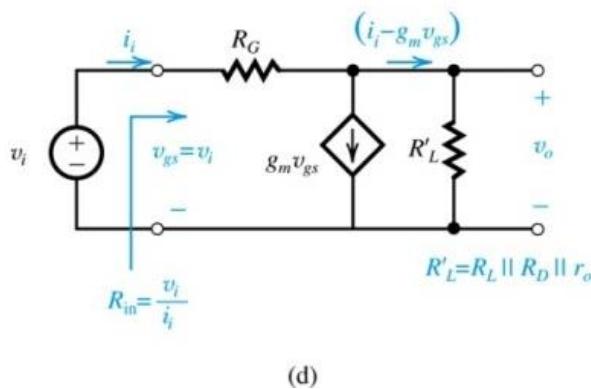


Figure 7.15 Example 7.3: (d) a simplified version of the circuit in (c).

Continue the small-signal analysis with the simplified hybrid pi circuit model

$$R_o = R'_L = 10k \parallel 10k\Omega \parallel 47k\Omega = 4.52k\Omega$$

$$v_o = (i_i - g_m v_{gs}) R'_L$$

$$i_i = \frac{v_{gs} - v_o}{R_G}$$

Combining these two relationships yields:

$$A_v = -g_m R'_L \frac{1 - (1/g_m R_G)}{1 + (R'_L/R_G)} \approx -3.3V/V$$



The T Equivalent-Circuit Model

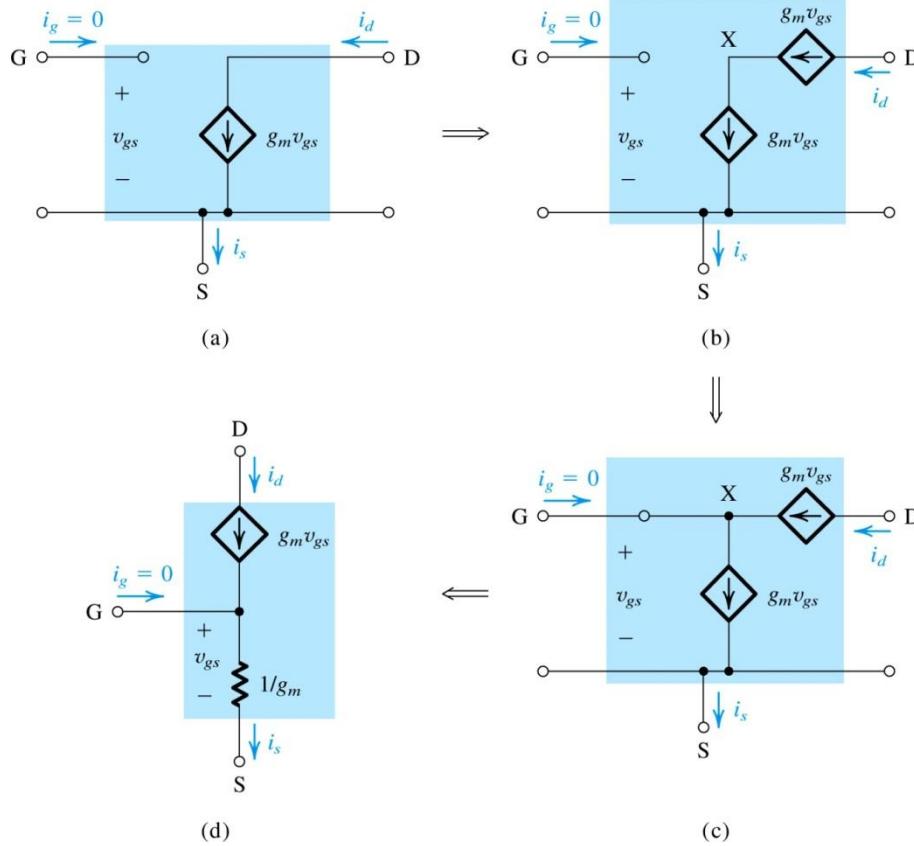


Figure 7.16 Development of the T equivalent-circuit model for the MOSFET. For simplicity, r_o has been omitted; however, it may be added between D and S in the T model of (d).

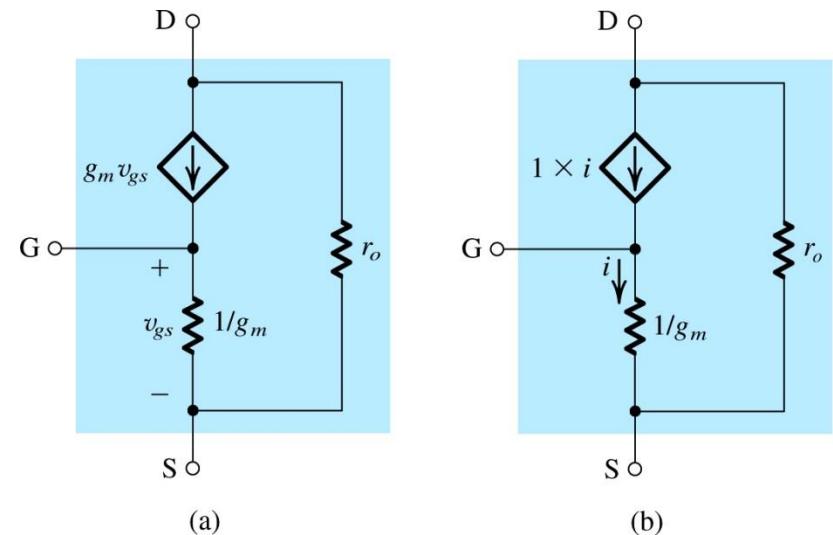
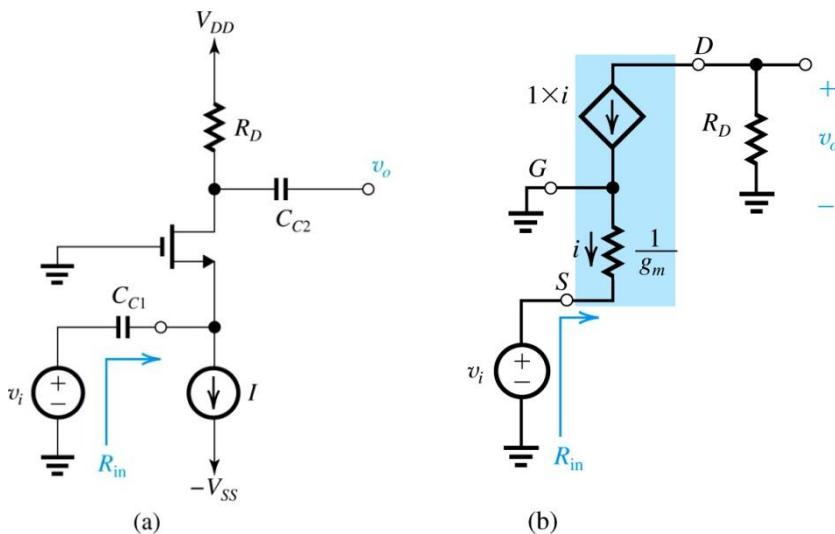


Figure 7.17 (a) The T model of the MOSFET augmented with the drain-to-source resistance r_o . (b) An alternative representation of the T model.



Example 7.4

Figure 7.18(a) shows a MOSFET amplifier biased by a constant-current source I . Assume that the values of I and R_D are such that the MOSFET operates in the saturation region. The input signal v_i is coupled to the source terminal by utilizing a large capacitor C_{C1} . Similarly, the output signal at the drain is taken through a large coupling capacitor C_{C2} . Find the input resistance R_{in} and the voltage gain v_o/v_i . Neglect channel-length modulation.



Use the T equiv circuit model

$$R_{in} = \frac{v_i}{i_i} = \frac{1}{g_m}$$

$$v_o = -i R_D = \left(\frac{v_i}{1/g_m} \right) R_D = g_m v_i R_D$$

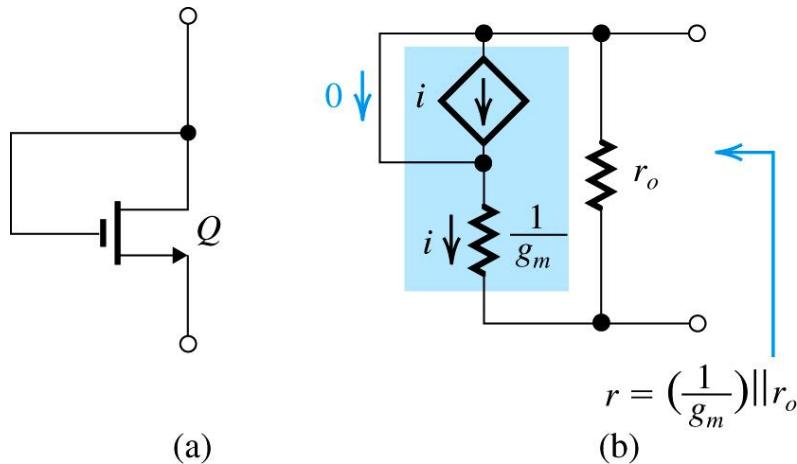
$$A_v \equiv \frac{v_o}{v_i} = g_m R_D$$

Figure 7.18 (a) Amplifier circuit for Example 7.4; (b) Small-signal equivalent circuit of the amplifier in (a).



Exercise 7.5

Use the T model of Fig. 7.17(b) to show that a MOSFET whose drain is connected to its gate exhibits an incremental resistance equal to $[(1/g_m) \parallel r_o]$.

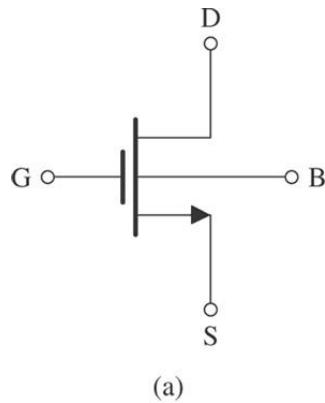


Transconductance is shorted so the drain to source is r_o in parallel with $1/g_m$.

Figure E7.5 Circuits for Exercise 7.5. Note that the bias arrangement of Q is not shown.



Modeling the Body Effect



In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the *pn* junction between the substrate and the induced channel having a constant zero (cutoff) bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether.

In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to maintain the cutoff condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit). The resulting reverse-bias voltage between source and body (V_{SB} in an *n*-channel device) will have an effect on device operation. The effect of V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage, V_t .

$$V_t = V_{t0} + \gamma \left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right]$$

Where ϕ_f is a physical parameter and $\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{c_{ox}}$



Modeling the Body Effect

As mentioned the body effect occurs in a MOSFET when the source is not tied to the substrate (which is always connected to the most negative power supply in the integrated circuit for *n*-channel devices and to the most positive for *p*-channel devices). Thus the substrate (body) will be at signal ground, but since the source is not a signal voltage v_{bs} develops between the body (B) and the source (S). The substrate then acts as a "second gate" or a backgate for the MOSFET. Thus the signal v_{bs} gives rise to a drain-current component. We can model this by adding a second transconductance (**body transconductance**) term to the FET model.

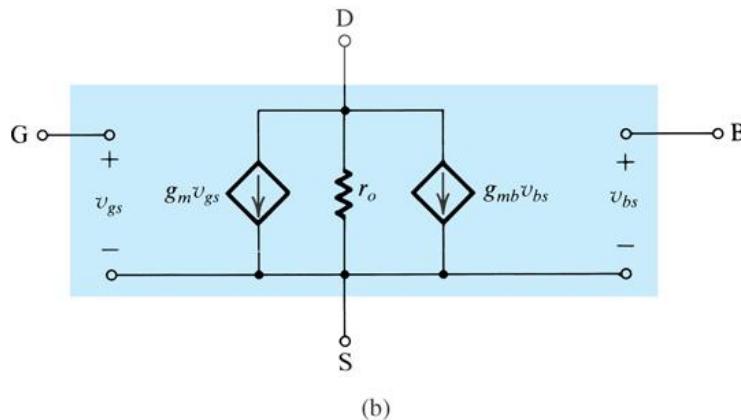


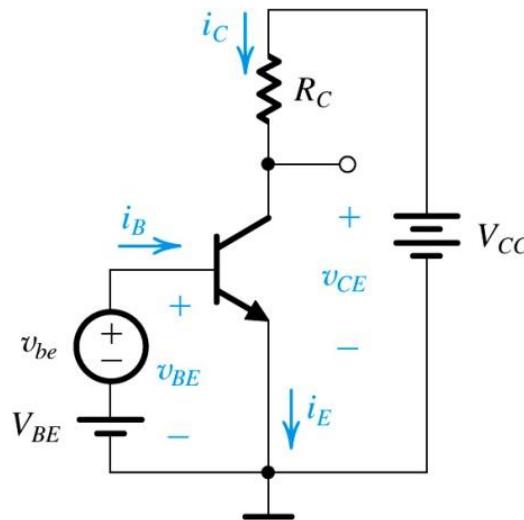
Figure 7.19 Small-signal, equivalent-circuit model of a MOSFET in which the source is not connected to the body.

$$g_{mb} = \chi g_m$$

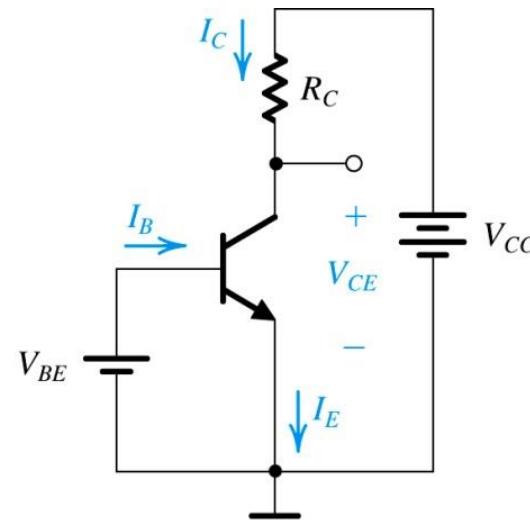
$$\chi \equiv \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$$



Small Signal Analysis with the BJT



(a)



(b)

Figure 7.20 (a) Conceptual circuit to illustrate the operation of the transistor as an amplifier. (b) The circuit of (a) with the signal source v_{be} eliminated for dc (bias) analysis.

$$I_C = I_S e^{V_{BE}/V_T}$$

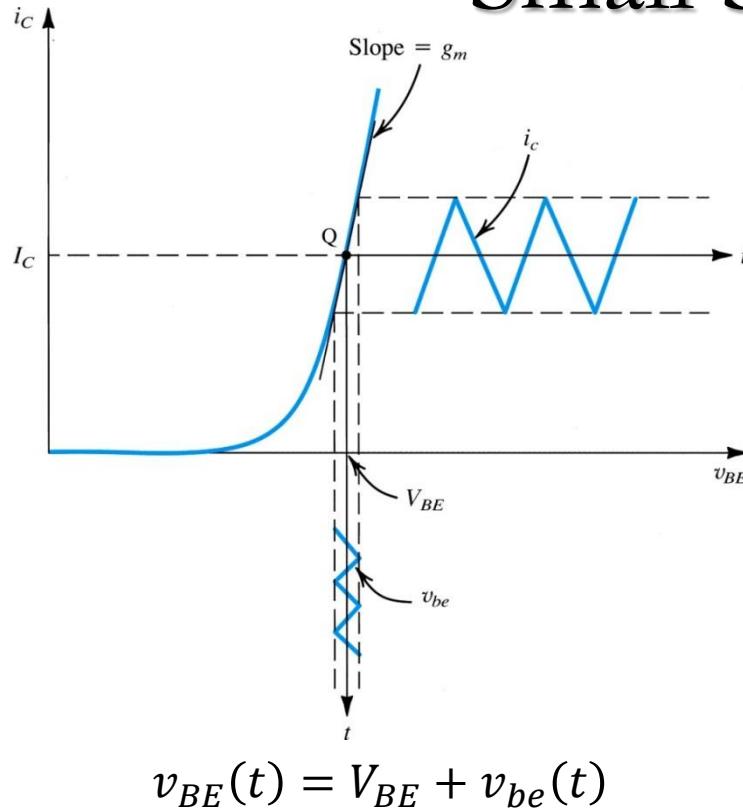
$$I_E = I_C/\alpha$$

$$I_B = I_C/\beta$$

$$V_{CE} = V_{CC} - I_C R_C$$



Small Signal Operation

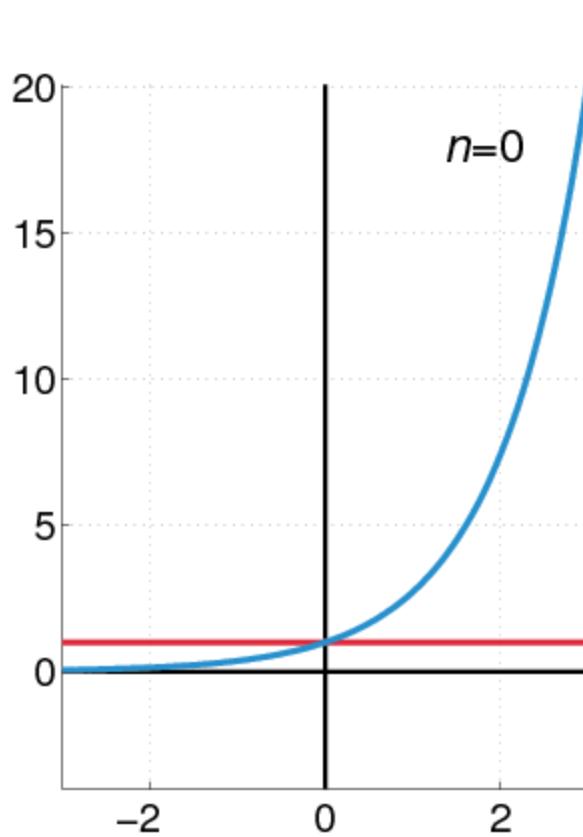


$$v_{BE}(t) = V_{BE} + v_{be}(t)$$

Figure 7.21 Linear operation of the transistor under the small-signal condition: A small-signal v_{be} with a triangular waveform is superimposed on the dc voltage V_{BE} . It gives rise to a collector-signal current i_c , also of triangular waveform, superimposed on the dc current I_C . Here, $i_c = g_m v_{be}$, where g_m is the slope of the $i_C - v_{BE}$ curve at the bias point Q .



e^x Power Series Expansion



$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!} = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \dots$$

$$e^x = \lim_{n \rightarrow \infty} \left(1 + \frac{x}{n}\right)^n$$

$$x = \frac{v_{be}}{V_T} \ll 1$$

For $v_{be} = 5$ mV, $v_{be}/V_T = 0.2$.

Thus the next term in the series expansion of the exponential will be $(0.2)^2/2 = 0.02$, a factor of 10 lower than the linear term we kept.

http://en.wikipedia.org/wiki/Exponential_function



Base and Emitter Resistance

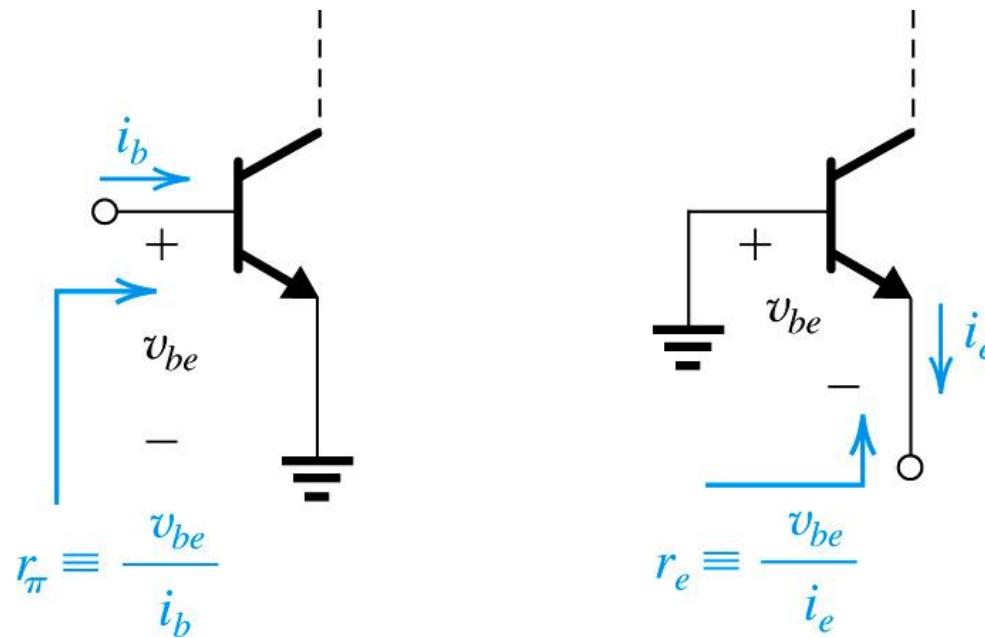


Figure 7.22 Illustrating the definition of r_π and r_e .

$$r_\pi \equiv \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

$$r_e \equiv \frac{v_{be}}{i_e} = \frac{V_T}{I_E} = \frac{\alpha}{g_m} \approx \frac{1}{g_m}$$

$$r_\pi = (\beta + 1)r_e$$



Small Signal Analysis

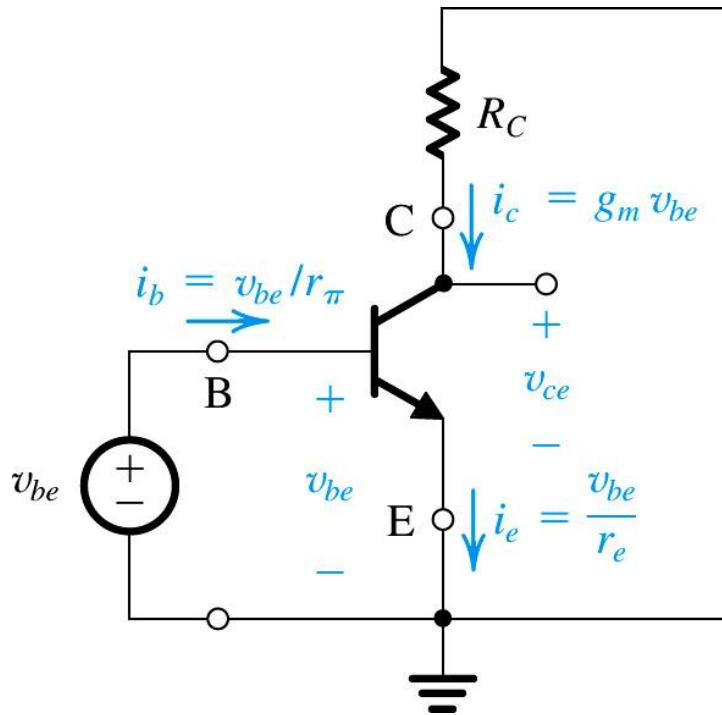


Figure 7.23 The amplifier circuit of Fig. 7.20(a) with the dc sources (V_{BE} and V_{CC}) eliminated (short-circuited). Thus only the signal components are present. Note that this is a representation of the signal operation of the BJT and not an actual amplifier circuit.

$$v_{CE} = V_{CC} - i_C R_C$$

$$v_{CE} = V_{CC} - (I_C + i_c) R_C$$

$$v_{CE} = (V_{CC} - I_C R_C) - i_c R_C$$

$$v_{CE} = V_{CE} - i_c R_C$$

$$v_{CE} = V_{CE} + v_{ce}$$

$$v_{ce} = -i_c R_C = -g_m v_{be} R_C$$

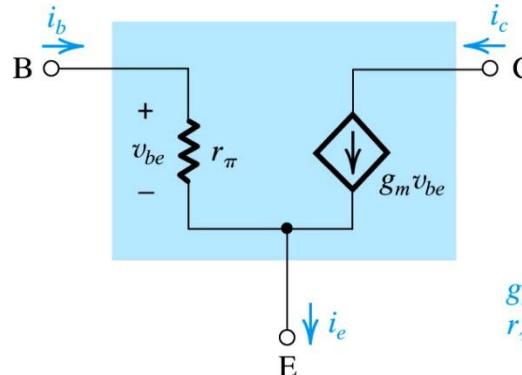
$$v_{ce} = (-g_m R_C) v_{be}$$

$$A_v \equiv \frac{v_{ce}}{v_{be}} = -g_m R_C$$

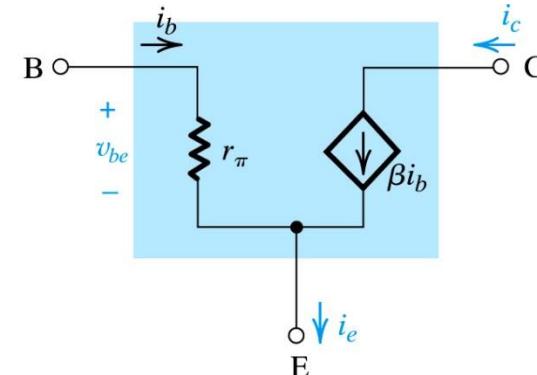
$$A_v = \frac{I_C R_C}{V_{CT}}$$



Small Signal Hybrid π Model

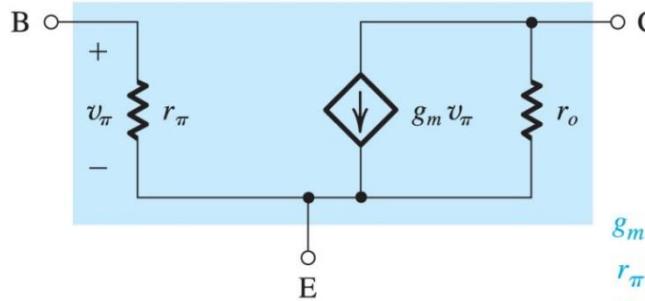


(a)

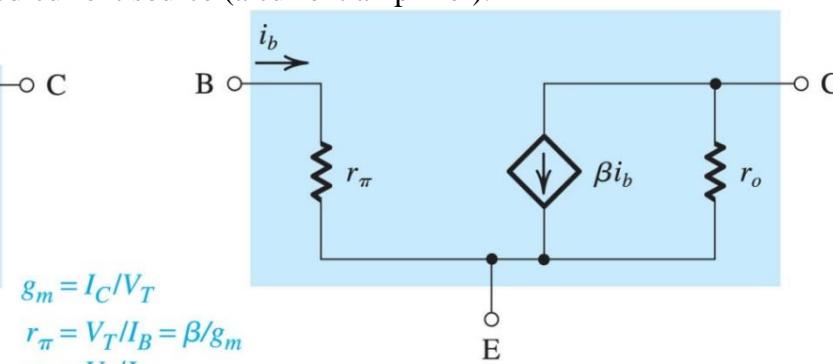


(b)

Figure 7.24 Two slightly different versions of the hybrid- π model for the small-signal operation of the BJT. The equivalent circuit in (a) represents the BJT as a voltage-controlled current source (a transconductance amplifier), and that in (b) represents the BJT as a current-controlled current source (a current amplifier).



(a)

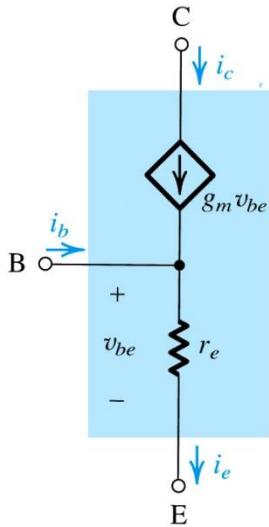


(b)

Figure 7.25 The hybrid- π small-signal model, in its two versions, with the resistance r_o included.

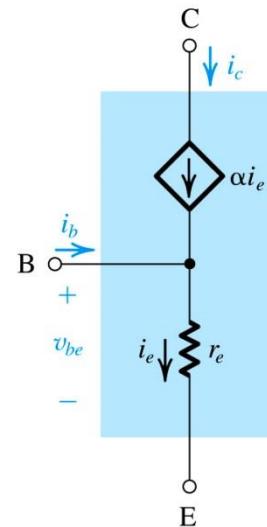


Small Signal T Model

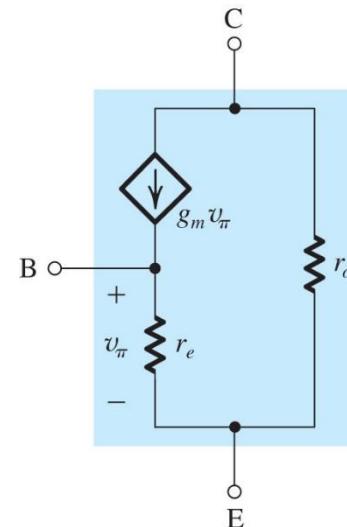


(a)

$$g_m = I_C/V_T$$
$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

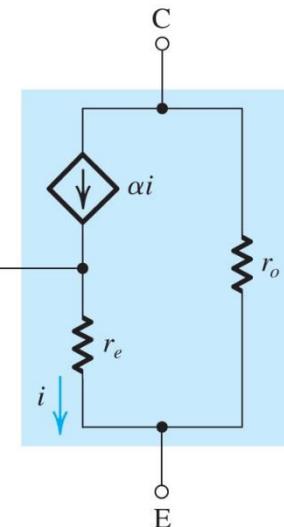


(b)



(a)

$$g_m = I_C/V_T$$
$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$
$$r_o = V_A/I_C$$



(b)

Figure 7.26 Two slightly different versions of what is known as the *T model* of the BJT. The circuit in (a) is a voltage-controlled current source representation and that in (b) is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid- π model.

Figure 7.27 The T models of the BJT.



Application of the Small-Signal Models

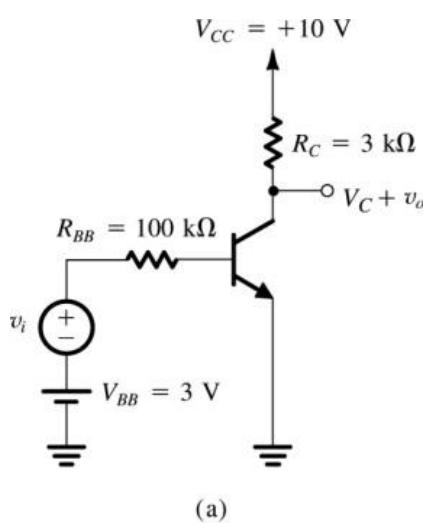
The availability of the small-signal BJT circuit models makes the analysis of transistor amplifier circuits a systematic process. The process consists of the following steps:

1. Eliminate the signal source and determine the dc operating point of the BJT and in particular the dc collector current I_C .
2. Calculate the values of the small-signal model parameters: $g_m = I_C/V_T$, $r_\pi = \beta/g_m$, and $r_e = V_T/I_E = \alpha/g_m$.
3. Eliminate the dc sources by replacing each dc voltage source with a short circuit and each dc current source with an open circuit.
4. Replace the BJT with one of its small-signal equivalent circuit models. Although any one of the models can be used, one might be more convenient than the others for the particular circuit being analyzed.
5. Analyze the resulting circuit to determine the required quantities (e.g. voltage gain, input resistance).

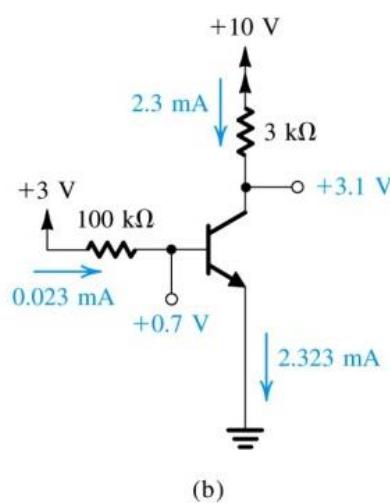


Example 7.5

We wish to analyze the transistor amplifier shown in Fig. 7.28(a) to determine its voltage gain v_o/v_{in} . Assume $\beta = 100$.



Step 1:



$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}}$$

$$I_B = \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$

$$I_C = \beta I_B = 2.3 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C$$

$$V_C = 10 - 2.3 \times 3 = 3.1 \text{ V}$$

Step 2:

$$r_e = \frac{V_T}{I_E} = 10.8 \Omega$$

$$g_m = \frac{I_C}{V_T} = 92 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = 1.09 \Omega$$

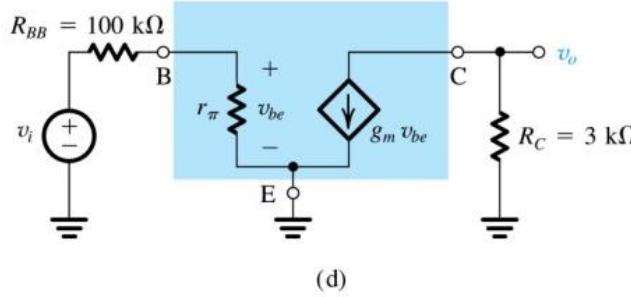
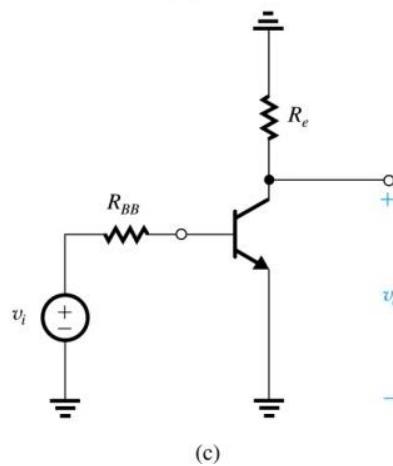
Figure 7.28 Example 7.5: (a) amplifier circuit; (b) circuit for dc analysis; (c) amplifier circuit with dc sources replaced by short circuits; (d) amplifier circuit with transistor replaced by its hybrid- π , small-signal model.



Example 7.5

We wish to analyze the transistor amplifier shown in Fig. 7.28(a) to determine its voltage gain v_o/v_{in} . Assume $\beta = 100$.

Step 3:



Step 4:

Step 5:

$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}}$$

$$v_{be} = v_i \frac{1.09}{101.09} = 0.011v_i$$

$$v_o = -g_m v_{be} R_C$$

$$v_o = -92 \times 0.011v_i \times 3 = -3.04v_i$$

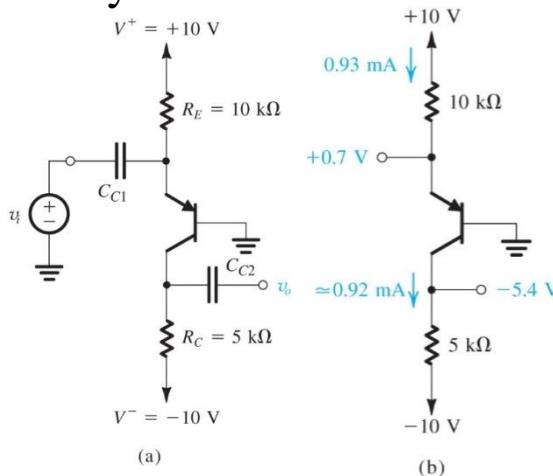
$$A_v = \frac{v_o}{v_i} = -3.04 \text{ V/V}$$

Figure 7.28 Example 7.5: (c) amplifier circuit with dc sources replaced by short circuits; (d) amplifier circuit with transistor replaced by its hybrid- π , small-signal model.



Example 7.7

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system. You may neglect the Early effect.



$$I_E = \frac{10V - V_E}{R_E} = \frac{9.3V}{10k\Omega} = 0.93mA$$

$$I_C = \frac{\beta}{\beta+1} I_E = \frac{100}{101} 0.93mA = 0.92mA$$

$$V_C = V_{EE} + I_C R_C = -10V + (0.92mA) 5k\Omega = -5.4V$$

Figure 7.30 Example 7.7: (a) circuit; (b) dc analysis;



Example 7.7

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system. You may neglect the Early effect.

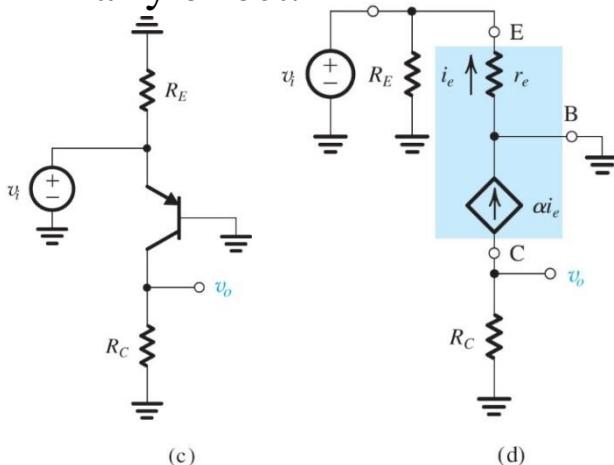


Figure 7.30 Example 7.7: (c) circuit with the dc sources eliminated; (d) small-signal analysis using the T model for the BJT.

$$g_m = \frac{I_C}{V_T} = \frac{0.92\text{mA}}{25\text{mV}} = 36.8 \frac{\text{mA}}{\text{V}}$$

$$r_e = \frac{V_T}{I_E} = \frac{25\text{mV}}{0.93\text{mA}} = 27.2\Omega$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{36.8 \frac{\text{mA}}{\text{V}}} = 2.72\text{k}\Omega$$

$$A_v \equiv \frac{v_o}{v_i} = \frac{\alpha R_C}{r_e} = \frac{0.99(5\text{k}\Omega)}{27.2\Omega} = 182 \frac{\text{V}}{\text{V}}$$



Example 7.7

We need to analyze the circuit of Fig. 7.30(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C_{C1} is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C_{C1} will be assumed to be very large so as to act as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor C_{C2} is used to couple the output signal v_o to other parts of the system. You may neglect the Early effect.

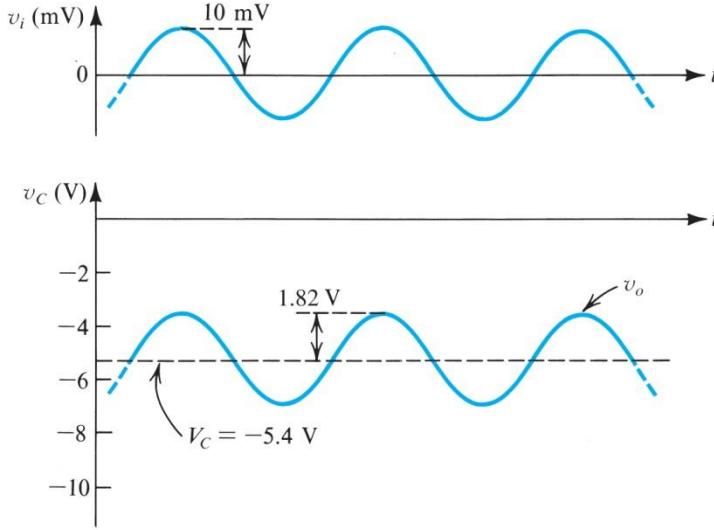
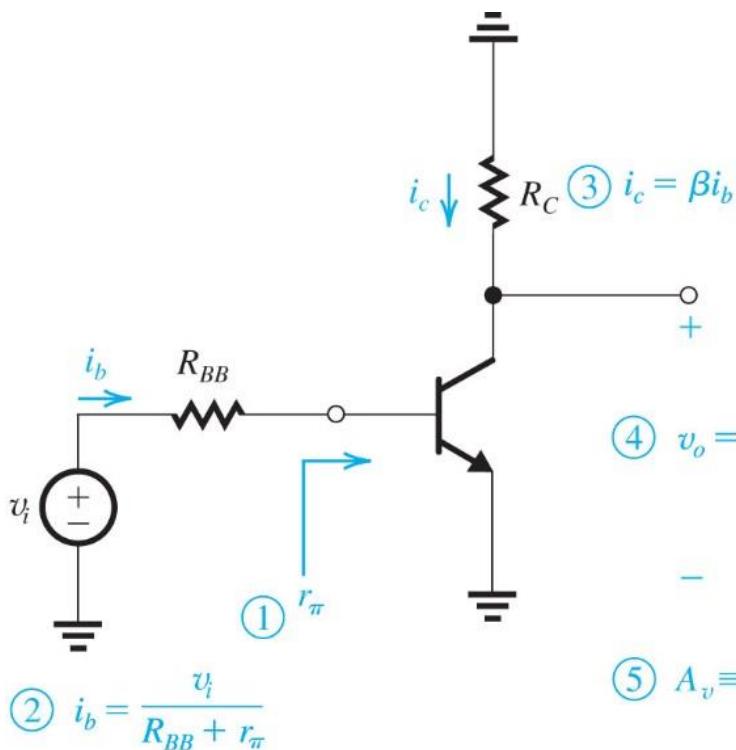


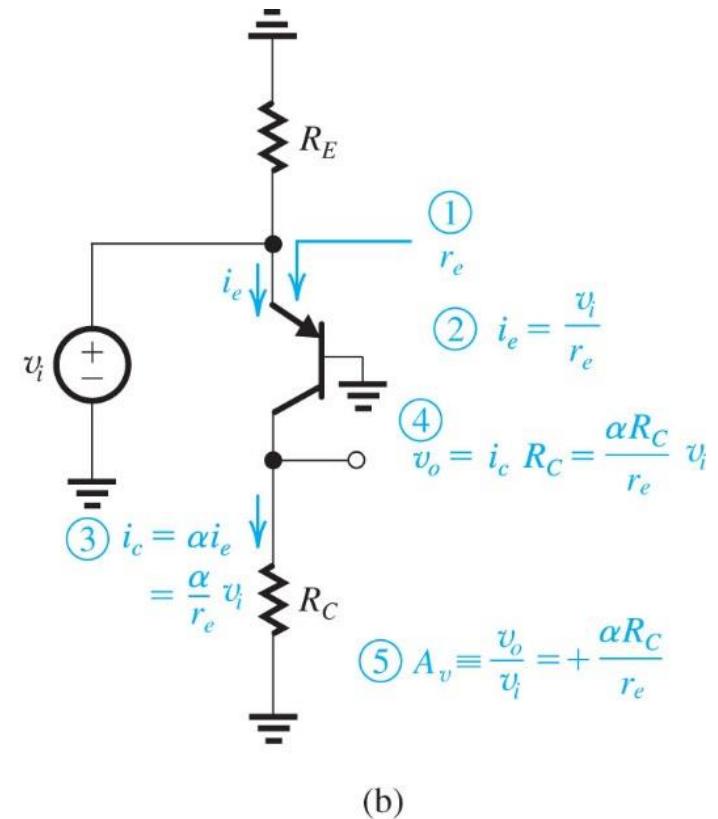
Figure 7.31 Input and output waveforms for the circuit of Fig. 7.30. Observe that this amplifier is noninverting, a property of the grounded-base configuration.



Direct Circuit Analysis



(a)



(b)

Figure 7.32 Performing signal analysis directly on the circuit diagram with the BJT small-signal model implicitly employed: (a) circuit for Example 7.5; (b) circuit for Example 7.7.

Table 7.2 Small Signal Models of the MOSFET

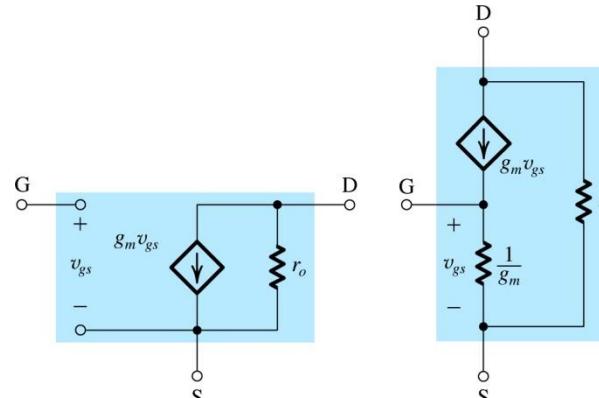
NMOS transistors

Transconductance

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L}} I_D = \frac{2I_D}{V_{OV}}$$

Output resistance

$$r_o = \frac{V_A}{I_D} = \frac{1}{\lambda I_D}$$



PMOS transistors

Transconductance

$$g_m = \mu_p C_{ox} \frac{W}{L} |V_{OV}| = \sqrt{2\mu_p C_{ox} \frac{W}{L}} I_D = \frac{2I_D}{|V_{OV}|}$$

Output resistance

$$r_o = \frac{|V_A|}{I_D} = \frac{1}{\lambda I_D}$$

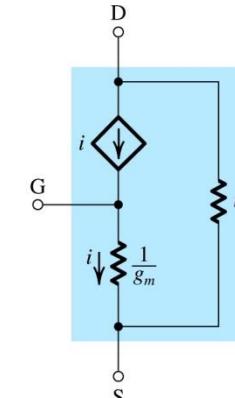


Table 7.2 Small-Signal Equivalent-Circuit Models for the MOSFET



Table 7.3 - Small Signal Models of the BJT

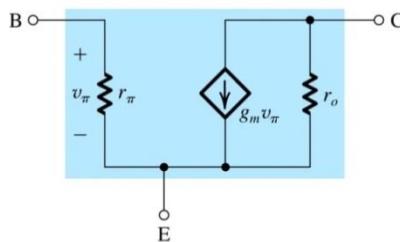
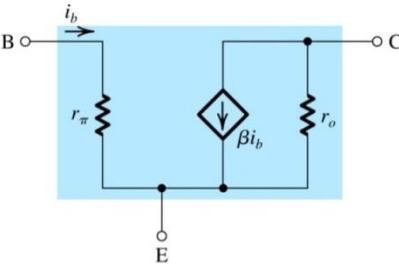
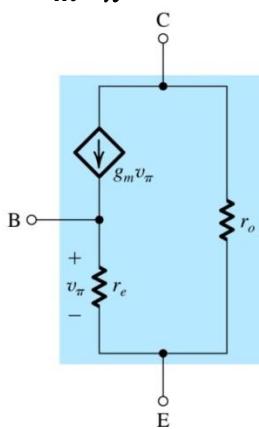
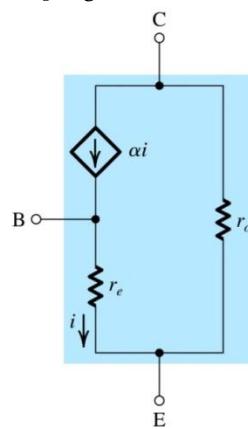
 $(g_m v_\pi)$ Version **(βi_b) Version** **$(g_m v_\pi)$ Version** **(βi_b) Version**

Table 7.3 Small-Signal Models of the BJT

Model Parameters in Terms of DC Bias currents

$$g_m = \frac{I_C}{V_T}$$

$$r_e = \frac{V_T}{I_E} = \alpha \frac{V_T}{I_C}$$

$$r_o = \frac{|V_A|}{I_C}$$

$$r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C}$$

Model Parameters in Terms of g_m

$$r_e = \frac{\alpha}{g_m}$$

$$r_\pi = \frac{\beta}{g_m}$$

Model Parameters in Terms of r_e

$$g_m = \frac{\alpha}{r_e} \quad r_\pi = (\beta + 1)r_e \quad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationship between α and β

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta + 1 = \frac{1}{1 - \alpha}$$



Homework #14

- Read Chapter 7
- Chapter 7 Problems:
 - 7.25*
 - 7.30
 - 7.35*
 - 7.36
 - 7.54

* Answers in Appendix L



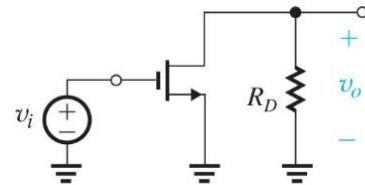
7.3 BASIC CONFIGURATIONS



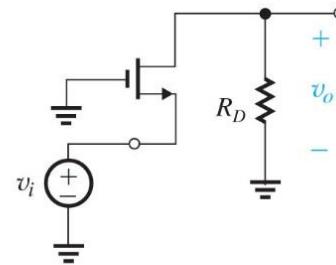
Three Basic Amplifier Configurations

The three basic amplifier configurations are shown without biasing considerations.

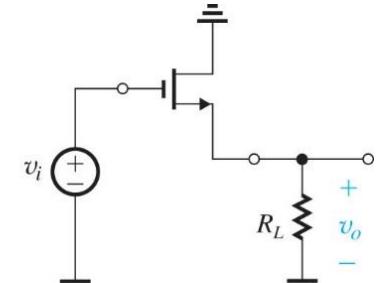
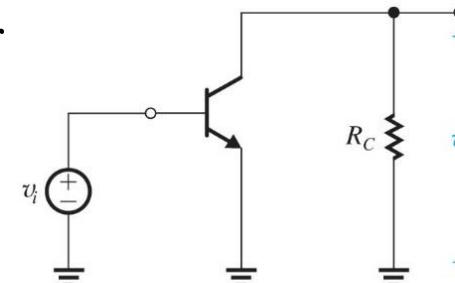
The common-source (CS) amplifier is by far the most popular amplifier configuration.



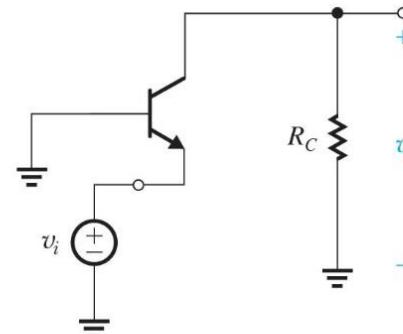
(a) Common Source (CS)



(b) Common Gate (CG)

(c) Common Drain (CD)
or Source Follower

(d) Common-Emitter (CE)



(e) Common-Base (CB)

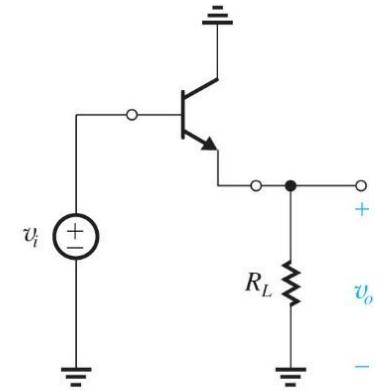
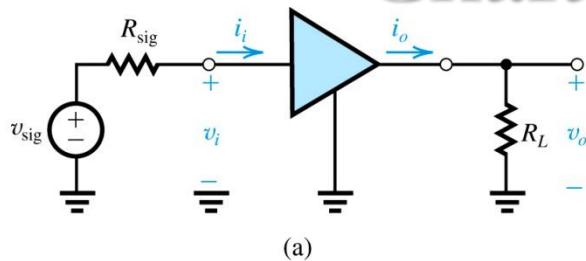
(f) Common-Collector (CC)
or Emitter Follower

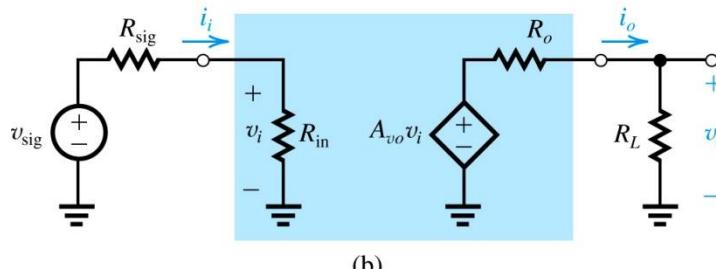
Figure 7.33 The basic configurations of transistor amplifiers. (a)–(c) For the MOSFET; (d)–(f) for the BJT.



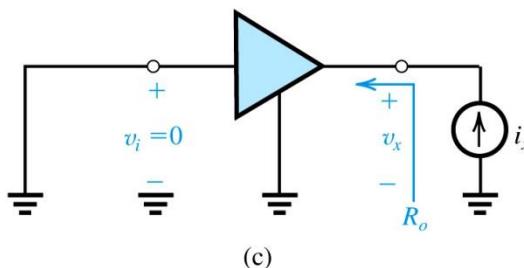
Characterizing Amplifiers



(a)



(b)



(c)

All the amplifier circuits studied in this section are **unilateral**. That is, they do not contain internal feedback, and thus R_{in} will be independent of R_L . However, as will be seen in subsequent chapters, this is not always the case. The **input resistance** is:

$$R_{in} \equiv \frac{v_i}{i_i} \quad v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig}$$

The **open-circuit voltage gain** is:

$$A_{vo} \equiv \left. \frac{v_o}{v_i} \right|_{R_L=\infty}$$

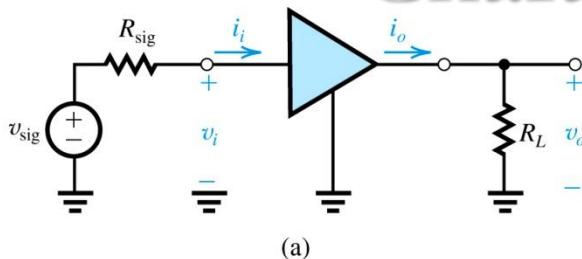
The **output resistance** is:

$$R_o \equiv \frac{v_x}{i_x} \quad v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i$$

Figure 7.34 Characterization of the amplifier as a functional block:
(a) An amplifier fed with a voltage signal v_{sig} having a source resistance R_{sig} , and feeding a load resistance R_L ; (b) equivalent-circuit representation of the circuit in (a); (c) determining the amplifier output resistance R_o .



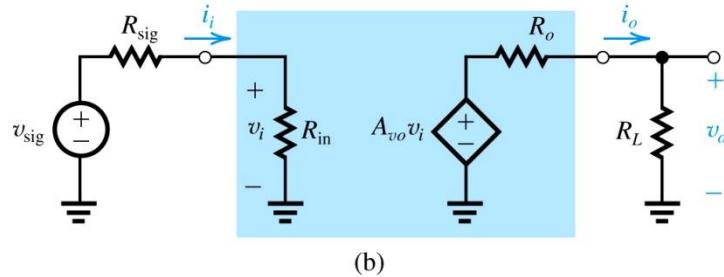
Characterizing Amplifiers



(a)

The **voltage gain** of the amplifier is:

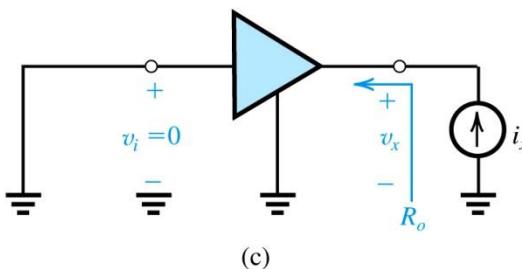
$$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o}$$



(b)

The overall **voltage gain** is:

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} A_{vo} \frac{R_L}{R_L + R_o}$$



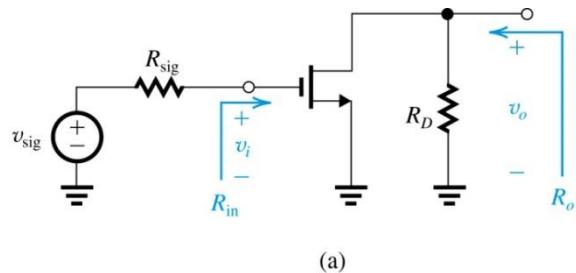
(c)

Figure 7.34 Characterization of the amplifier as a functional block:

- (a) An amplifier fed with a voltage signal v_{sig} having a source resistance R_{sig} , and feeding a load resistance R_L ; (b) equivalent-circuit representation of the circuit in (a); (c) determining the amplifier output resistance R_o .

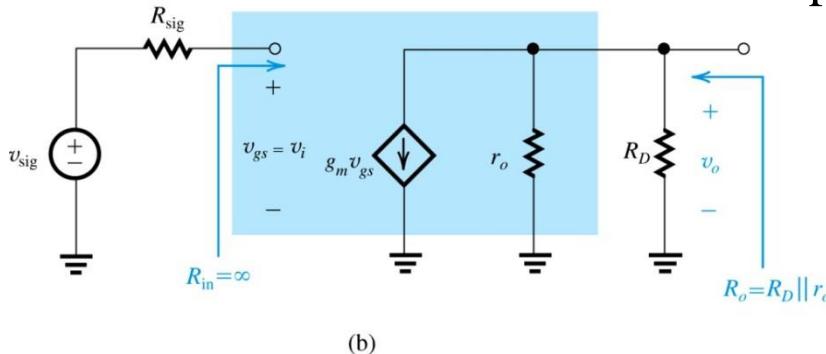


The Common-Source (CS) Amplifier



(a)

Figure 7.35(a) shows a common-source amplifier (with the biasing arrangement omitted) fed with a signal source v_{sig} having a source resistance R_{sig} . We wish to analyze this circuit to determine R_{in} , A_{vo} , R_o , and G_v . For this purpose we shall assume that R_D is part of the amplifier; thus If a load resistance R_L is connected to the amplifier output, it appears in parallel with R_D .



(b)

Figure 7.35 (a) Common-source amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} . The bias circuit is omitted. (b) The common-source amplifier with the MOSFET replaced with its hybrid- π model.

The **input resistance** is: $R_{in} \equiv \frac{v_i}{i_i} = \infty$

$$v_o = -(g_m v_{gs})(R_D \parallel r_o)$$

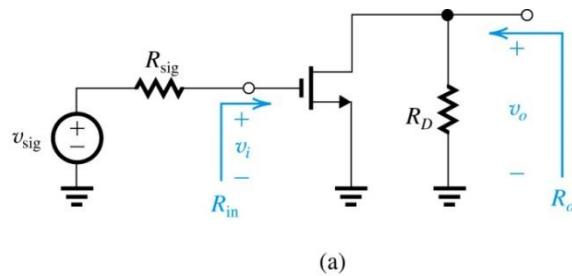
The **open-circuit voltage gain** is:

$$A_{vo} \equiv \frac{v_o}{v_i} = -g_m(R_D \parallel r_o)$$

Sometimes
neglect r_o

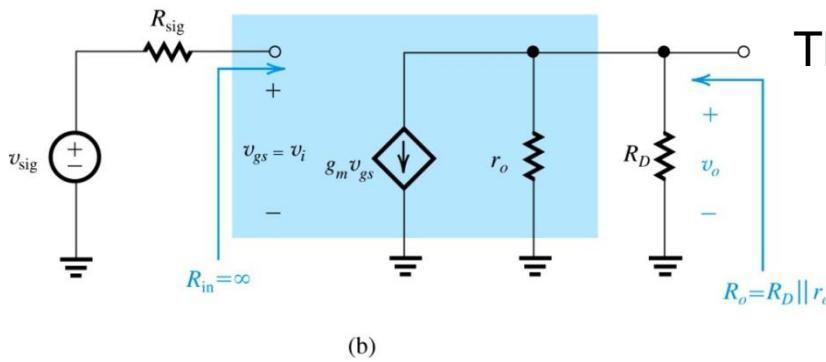


The Common-Source (CS) Amplifier



(a)

Figure 7.35(a) shows a common-source amplifier (with the biasing arrangement omitted) fed with a signal source v_{sig} having a source resistance R_{sig} . We wish to analyze this circuit to determine R_{in} , A_{vo} , R_o , and G_v . For this purpose we shall assume that R_D is part of the amplifier; thus If a load resistance R_L is connected to the amplifier output, it appears in parallel with R_D .



(b)

Figure 7.35 (a) Common-source amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} . The bias circuit is omitted. (b) The common-source amplifier with the MOSFET replaced with its hybrid- π model.

The output resistance is: $R_o \equiv \frac{v_x}{i_x} = R_D \parallel r_o$

Sometimes neglect r_o $R_o \approx R_D$

The amplifier voltage gain is:

$$A_v \equiv \frac{v_o}{v_i} = -g_m(R_D \parallel R_L \parallel r_o)$$

The overall voltage gain is:

$$G_v = A_v = -g_m(R_D \parallel R_L \parallel r_o)$$



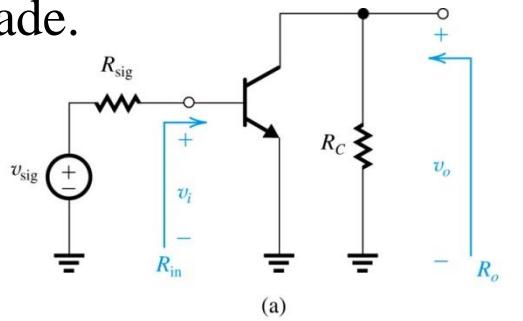
The Common-Source (CS) Amplifier

1. The input resistance is ideally infinite.
2. The output resistance is moderate to high (in the kilohms to tens of kilohms range). Reducing R_D to lower R_o is not a viable proposition, since the voltage gain is also reduced. Alternatively, if a low output resistance (in the ohms to tens of ohms range) is needed, a source follower stage is called for, as will be discussed in Section 7.3.6.
3. The open-circuit voltage gain A_{vo} can be high, making the CS configuration the workhorse in MOS amplifier design. Unfortunately, however, the bandwidth of the CS amplifier is severely limited. We shall study amplifier frequency response in Chapter 10 (ELEG 312).



Common Emitter (CE) Amplifier

Of the three basic BJT amplifier configurations, the common emitter is the most widely used. Typically, in an amplifier formed by cascading a number of stages, the bulk of the voltage gain is obtained by using one or more common-emitter stages in the cascade.



The **input resistance** is: $R_{in} \equiv \frac{v_i}{i_i} = r_\pi$

$$v_o = -(g_m v_\pi)(R_C \parallel r_o)$$

The **open-circuit voltage gain** is:

$$A_{vo} \equiv \frac{v_o}{v_i} = \frac{v_o}{v_\pi} = -g_m(R_C \parallel r_o)$$

Sometimes neglect r_o

$$A_{vo} \cong -g_m R_C$$

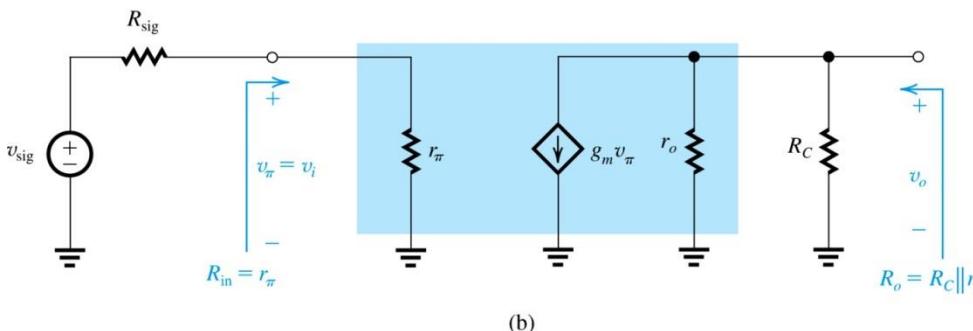
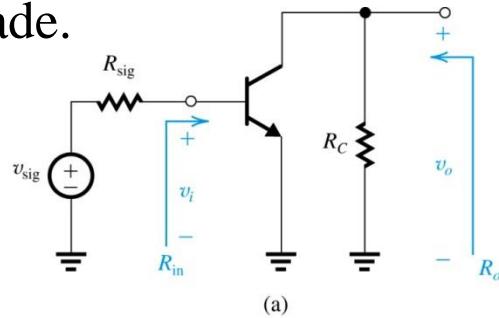


Figure 7.36 (a) Common-emitter amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} . The bias circuit is omitted. (b) The common-emitter amplifier circuit with the BJT replaced by its hybrid- π model.



Common Emitter (CE) Amplifier

Of the three basic BJT amplifier configurations, the common emitter is the most widely used. Typically, in an amplifier formed by cascading a number of stages, the bulk of the voltage gain is obtained by using one or more common-emitter stages in the cascade.



The **output resistance** is: $R_o \equiv \frac{v_x}{i_x} = R_C \parallel r_o$

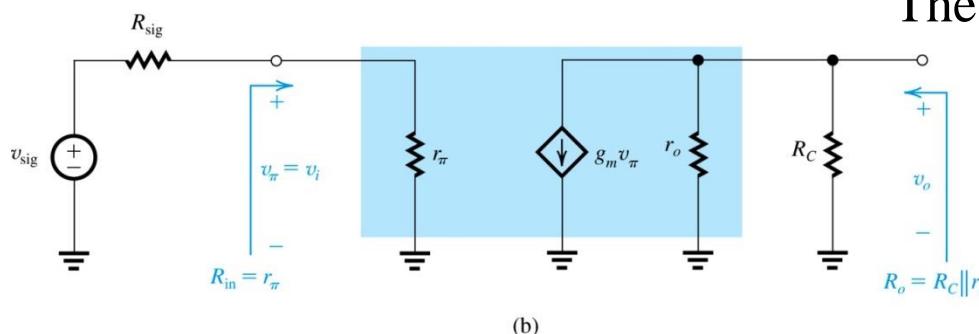
Sometimes neglect r_o $R_o \simeq R_C$

The **amplifier voltage gain** is:

$$A_v \equiv \frac{v_o}{v_i} = -g_m(R_C \parallel R_L \parallel r_o)$$

The **overall voltage gain** is:

$$G_v \equiv \frac{v_o}{v_{sig}} = -\frac{r_\pi}{r_\pi + R_{sig}} g_m(R_C \parallel R_L \parallel r_o)$$



(b)

Figure 7.36 (a) Common-emitter amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} . The bias circuit is omitted. (b) The common-emitter amplifier circuit with the BJT replaced by its hybrid- π model.



Common Emitter (CE) Amplifier

The amplifier voltage gain is:

$$A_v = -g_m(R_C \parallel R_L \parallel r_o)$$

$$A_v = -\alpha \frac{(R_C \parallel R_L \parallel r_o)}{r_e}$$

$$A_v = -\alpha \frac{\text{Total resistance in collector}}{\text{Total resistance in emitter}}$$

The overall voltage gain is:

$$G_v = -\frac{r_\pi}{r_\pi + R_{sig}} g_m (R_C \parallel R_L \parallel r_o)$$

$$G_v = -\beta \frac{(R_C \parallel R_L \parallel r_o)}{r_\pi + R_{sig}} g_m$$

$$G_v = -\beta \frac{\text{Total resistance in collector}}{\text{Total resistance in base}}$$

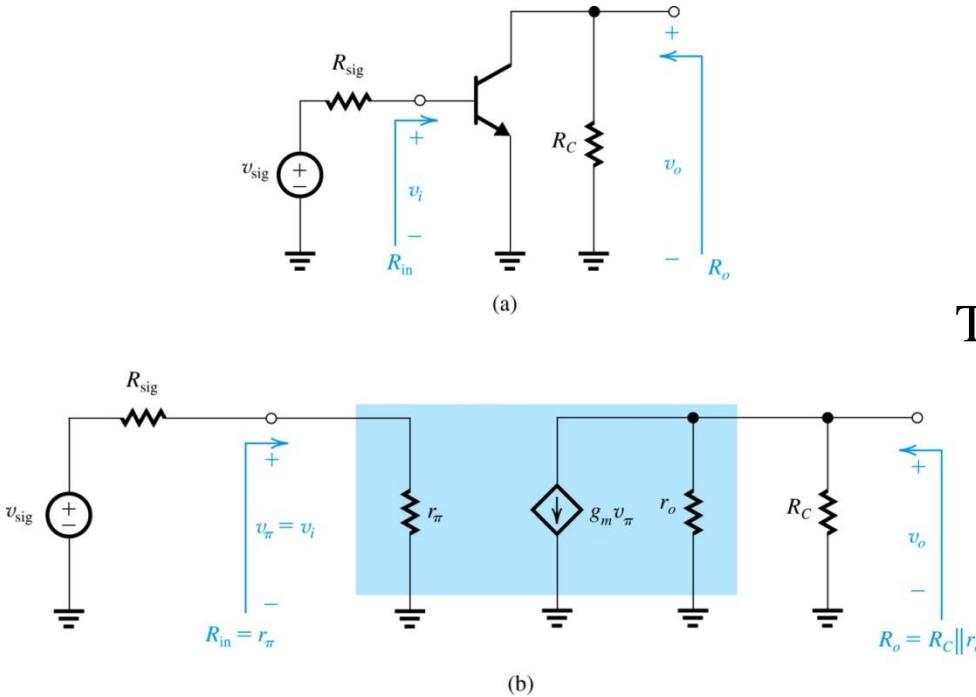


Figure 7.36 (a) Common-emitter amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} . The bias circuit is omitted. (b) The common-emitter amplifier circuit with the BJT replaced by its hybrid- π model.



Example 7.8

A CE amplifier utilizes a BJT with $\beta = 100$ is biased at $I_C = 1 \text{ mA}$ and has a collector resistance $R_C = 5 \text{ k}\Omega$. Find R_{in} , R_o , and A_{vo} . If the amplifier is fed with a signal source having a resistance of $5 \text{ k}\Omega$, and a load resistance $R_L=5 \text{ k}\Omega$ is connected to the output terminal, find the resulting A_v and G_v . If \hat{v}_π is to be limited to 5 mV , what are the corresponding \hat{v}_{sig} and \hat{v}_o with the load connected?

$$R_{in} = r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C} = 100 \frac{25 \text{ mV}}{1 \text{ mA}} = 2.5 \text{ k}\Omega \quad R_o = R_C = 5 \text{ k}\Omega$$

$$A_{vo} = -g_m R_C = -\left(\frac{I_C}{V_T}\right) 5 \text{ k}\Omega = -\left(\frac{1 \text{ mA}}{25 \text{ mV}}\right) 5 \text{ k}\Omega = -200 \frac{\text{V}}{\text{V}}$$

$$A_v = A_{vo} \left(\frac{R_L}{R_L + R_o} \right) = \left(-200 \frac{\text{V}}{\text{V}} \right) \left(\frac{5 \text{ k}\Omega}{5 \text{ k}\Omega + 5 \text{ k}\Omega} \right) = -100 \frac{\text{V}}{\text{V}}$$

$$A_v = -g_m (R_C \parallel R_L) = -\left(\frac{1 \text{ mA}}{25 \text{ mV}}\right) \left(\frac{5 \text{ k}\Omega \times 5 \text{ k}\Omega}{5 \text{ k}\Omega + 5 \text{ k}\Omega} \right) = -100 \frac{\text{V}}{\text{V}}$$



Example 7.8

A CE amplifier utilizes a BJT with $\beta = 100$ is biased at $I_C = 1$ mA and has a collector resistance $R_C = 5$ k Ω . Find R_{in} , R_o , and A_{vo} . If the amplifier is fed with a signal source having a resistance of 5 k Ω , and a load resistance $R_L=5$ k Ω is connected to the output terminal, find the resulting A_v and G_v . If \hat{v}_π is to be limited to 5 mV, what are the corresponding \hat{v}_{sig} and \hat{v}_o with the load connected?

$$G_v = \left(\frac{R_{in}}{R_{in} + R_{sig}} \right) A_v = \left(\frac{2.5\text{k}\Omega}{2.5\text{k}\Omega + 5\text{k}\Omega} \right) = -33.3 \frac{\text{V}}{\text{V}}$$

$$\hat{v}_{sig} = \left(\frac{R_{in} + R_{sig}}{R_{in}} \right) \hat{v}_\pi = \left(\frac{2.5\text{k}\Omega + 5\text{k}\Omega}{2.5\text{k}\Omega} \right) 5\text{mV} = 15\text{mV}$$

$$\hat{v}_o = |A_v| \hat{v}_\pi = 100 \frac{\text{V}}{\text{V}} 5\text{mV} = 500\text{mV}$$

$$\hat{v}_o = |G_v| \hat{v}_{sig} = 33.3 \frac{\text{V}}{\text{V}} 15\text{mV} = 500\text{mV}$$

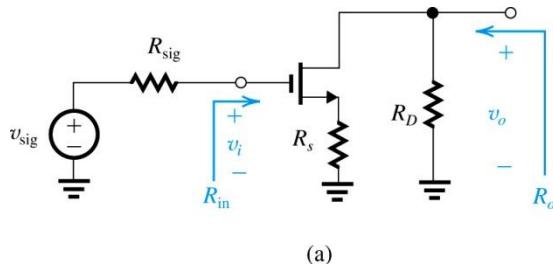


CE Summary

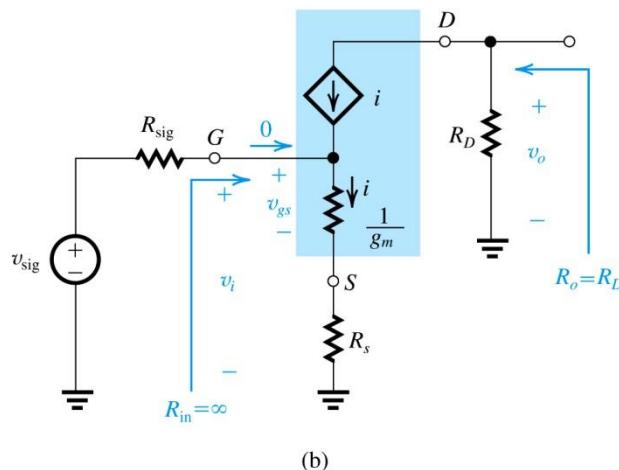
1. The input resistance $R_{in} = R_p = \beta/g_m$ is moderate to low in value (typically, in the kilohm range). Obviously R_{in} is directly dependent on β and is inversely proportional to the collector bias current I_C . To obtain a higher input resistance, the bias current can be lowered, but this also lowers the gain. This is a significant design trade-off. If a much higher input resistance is desired, then a modification of the CE configuration or an emitter-follower stage can be employed.
2. The output resistance $R_o \approx R_C$ is moderate to high in value (typically, in the kilohm range). Reducing R_C to lower R_o is usually not a viable proposition because the voltage gain is also reduced. Alternatively, if a very low output resistance (in the ohms to tens of ohms range) is needed, an emitter-follower stage is called for, as will be discussed in Section 7.3.6.
3. The open-circuit voltage gain A_{vo} can be high, making the CE configuration the workhorse in BJT amplifier design. Unfortunately, however, the bandwidth of the CE amplifier is severely limited. We shall study amplifier frequency response in Chapter 10 (ELEG 312).



The CS Amplifier with a Source Resistor



(a)



(b)

Figure 7.37 The CS amplifier with a source resistance R_s : (a) Circuit without bias details; (b) Equivalent circuit with the MOSFET represented by its T model.

Use the T model and neglect r_o

The **input resistance** is: $R_{in} \equiv \frac{v_i}{i_i} = \infty$

$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_S} = \frac{v_i}{1 + g_m R_S}$$

R_S controls/reduces the magnitude of the input signal.

$$v_o = -i R_D$$

$$i = \frac{v_i}{1/g_m + R_S} = \left(\frac{g_m}{1 + g_m R_S} \right) v_i$$

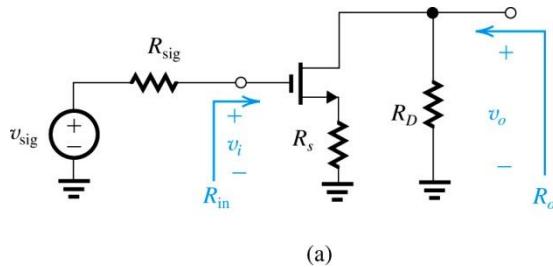
The **open-circuit voltage gain** is:

$$A_{vo} \equiv \frac{v_o}{v_i} = -\frac{R_D}{1/g_m + R_S} = -\frac{g_m R_D}{1 + g_m R_S}$$

R_S reduces the open-circuit voltage gain.



The CS Amplifier with a Source Resistor

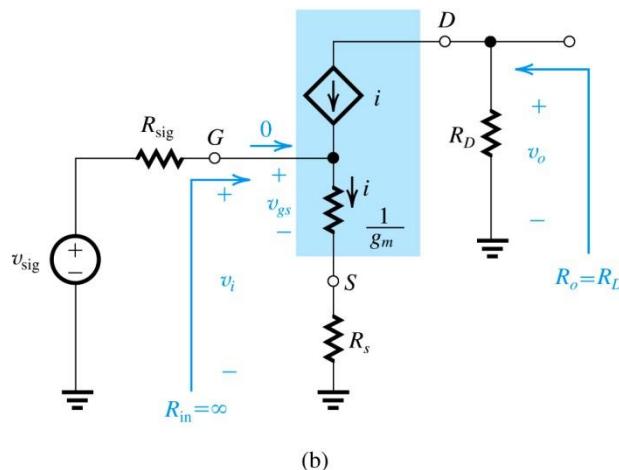


Use the T model and neglect r_o

The **output resistance** is: $R_o \equiv \frac{v_x}{i_x} = R_D$

The **amplifier voltage gain** is:

$$A_v \equiv \frac{v_o}{v_i} = -\frac{R_D \parallel R_L}{1/g_m + R_S} = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$$

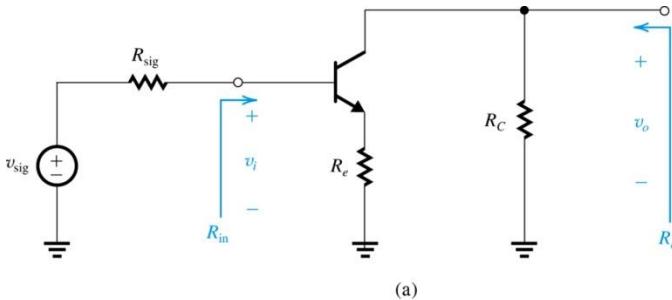


R_S reduces the amplifier voltage gain.
 R_S is known as a **source-degeneration resistance** and provides negative feedback in the circuit.

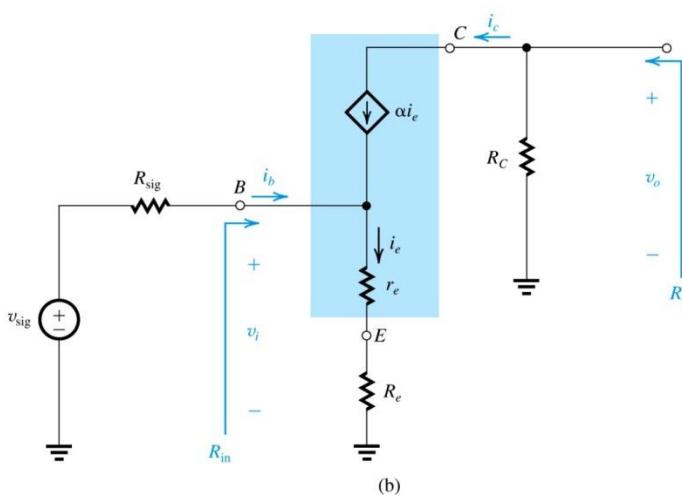
Figure 7.37 The CS amplifier with a source resistance R_s : (a) Circuit without bias details; (b) Equivalent circuit with the MOSFET represented by its T model.



CE Amplifier with an Emitter Resistance



(a)



(b)

Figure 7.38 The CE amplifier with an emitter resistance R_e ; (a) Circuit without bias details; (b) Equivalent circuit with the BJT replaced with its T model.



CE Amplifier with an Emitter Resistance

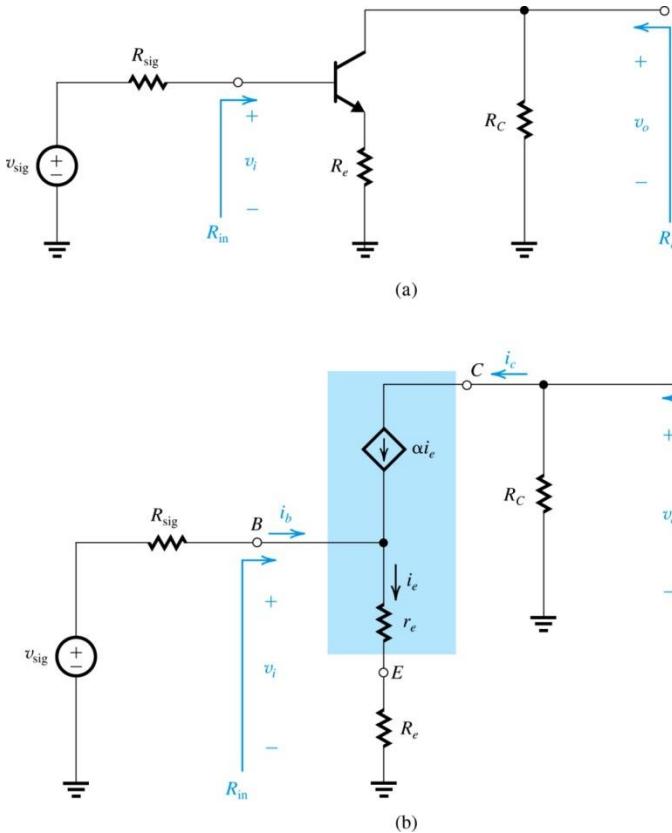


Figure 7.38 The CE amplifier with an emitter resistance R_e ; (a) Circuit without bias details; (b) Equivalent circuit with the BJT replaced with its T model.

$$v_o = -i_c R_C = -\alpha i_e R_C \quad i_e = \frac{v_i}{r_e + R_e}$$

The open-circuit voltage gain is:

$$A_{vo} \equiv \frac{v_o}{v_i} = -\alpha \frac{R_C}{r_e + R_e}$$

$$A_{vo} = -\frac{\alpha}{r_e} \frac{R_C}{1 + R_e/r_e}$$

$$A_{vo} = -\frac{g_m R_C}{1 + R_e/r_e} = -\frac{g_m R_C}{1 + g_m R_e}$$

R_e reduces the voltage gain by the factor $(1+g_m R_e)$ which is the same factor by which R_{in} is increased. This points out an interesting trade-off between gain and input resistance.

The output resistance is: $R_o \equiv \frac{v_x}{i_x} = R_C$



CE Amplifier with an Emitter Resistance

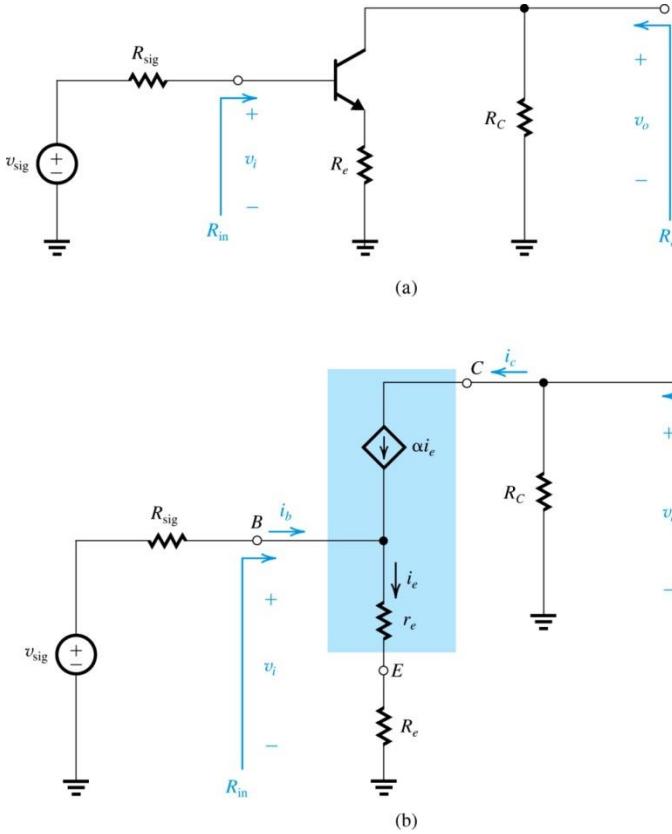


Figure 7.38 The CE amplifier with an emitter resistance R_e ; (a) Circuit without bias details; (b) Equivalent circuit with the BJT replaced with its T model.



CE with Emitter Resistor Summary

1. The input resistance R_{in} is increased by a factor of $(1+g_m R_e)$.
2. The voltage gain from base to collector, A_v , is reduced by the factor $(1+g_m R_e)$.
3. For the same nonlinear distortion, the input signal v_i can be increased by the factor $(1+g_m R_e)$.
4. The overall voltage gain is less dependent on the value of β .
5. The high-frequency response is significantly improved (as we shall see in Chapter 10 ELEG 312).



Example 7.9

For the CE amplifier specified in Example 7.8, what value of R_e is needed to raise R_{in} to a value four times that of R_{sig} ? With R_e included, find A_{vo} , R_o , A_v , and G_v . Also, if \hat{v}_π is limited to 5 mV, what are the corresponding values of \hat{v}_{sig} and \hat{v}_o ?

$$r_\pi = (\beta + 1)r_e \quad \Rightarrow r_e = \frac{r_\pi}{(\beta + 1)} = \frac{2.5\text{k}\Omega}{101} = 24.75\Omega$$

$$R_{in} = (\beta + 1)(r_e + R_e) = 4R_{sig} = 4(5\text{k}\Omega) = 20\text{k}\Omega$$

$$\Rightarrow R_e = \frac{20\text{k}\Omega}{(\beta + 1)} - r_e = \frac{20\text{k}\Omega}{(100 + 1)} - 24.75\Omega = 173.25\Omega$$

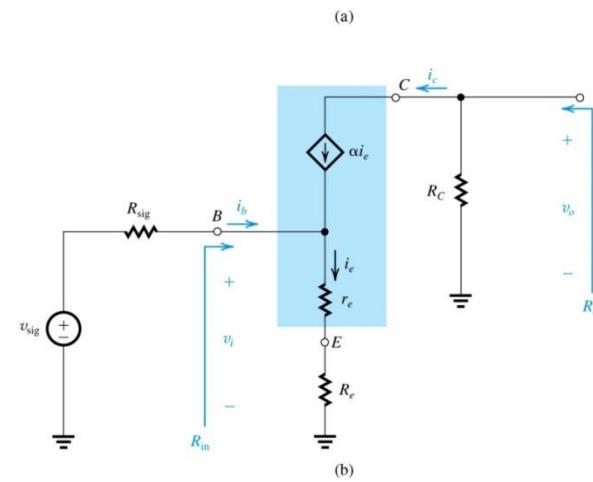
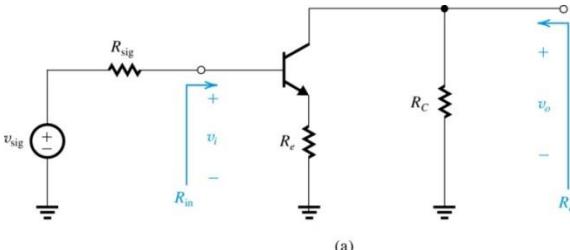
$$A_{vo} = -\alpha \frac{R_C}{r_e + R_e} = -\left(\frac{\beta}{\beta + 1}\right) \frac{5000\Omega}{(24.75\Omega + 173.25\Omega)} = -25.0 \frac{\text{V}}{\text{V}}$$

$$A_v = A_{vo} \frac{R_L}{R_L + R_o} = \left(-25.0 \frac{\text{V}}{\text{V}}\right) \frac{5\text{k}\Omega}{(5\text{k}\Omega + 5\text{k}\Omega)} = -12.5 \frac{\text{V}}{\text{V}}$$



Example 7.9

For the CE amplifier specified in Example 7.8, what value of R_e is needed to raise R_{in} to a value four times that of R_{sig} ? With R_e included, find A_{vo} , R_o , A_v , and G_v . Also, if \hat{v}_π is limited to 5 mV, what are the corresponding values of \hat{v}_{sig} and \hat{v}_o ?



$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v = \frac{20\text{k}\Omega}{(20\text{k}\Omega + 5\text{k}\Omega)} \left(-12.5 \frac{\text{V}}{\text{V}} \right) = -10.0 \frac{\text{V}}{\text{V}}$$

$$\hat{v}_i = \hat{v}_\pi \left(\frac{r_e + R_e}{r_e} \right) = 5\text{mV} \left(\frac{24.75\Omega + 173.25\Omega}{24.75\Omega} \right) = 40\text{mV}$$

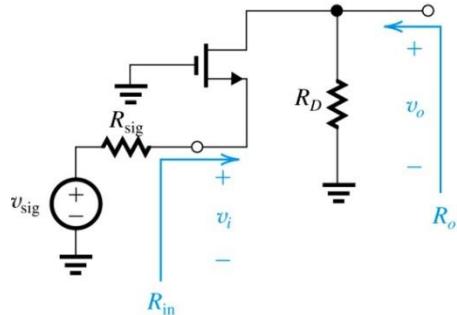
$$\hat{v}_{sig} = \hat{v}_i \left(\frac{R_{in} + R_{sig}}{R_{in}} \right) = 40\text{mV} \left(\frac{20\text{k}\Omega + 5\text{k}\Omega}{20\text{k}\Omega} \right) = 50\text{mV}$$

$$\hat{v}_o = |A_v| \hat{v}_i = 12.5 \frac{\text{V}}{\text{V}} 40\text{mV} = 500\text{mV}$$

$$\hat{v}_o = |G_v| \hat{v}_{sig} = 10.0 \frac{\text{V}}{\text{V}} 50\text{mV} = 500\text{mV}$$



The Common-Gate (CG) Amplifier



Use the T model and neglect r_o

The **input resistance** is:

$$R_{in} \equiv \frac{v_i}{i_i} = \frac{1}{g_m}$$

typically $1/g_m$ is a few hundred ohms so the common gate amplifier has a low input resistance.

$$v_o = -iR_D \quad i = -\frac{v_i}{1/g_m}$$

The **open-circuit voltage gain** is: $A_{vo} \equiv \frac{v_o}{v_i} = g_m R_D$

this is the same open-circuit voltage gain as the CS amplifier only non-inverting.

The **output resistance** is:

$$R_o \equiv \frac{v_x}{i_x} = R_D$$

The **overall voltage gain** is: $G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$

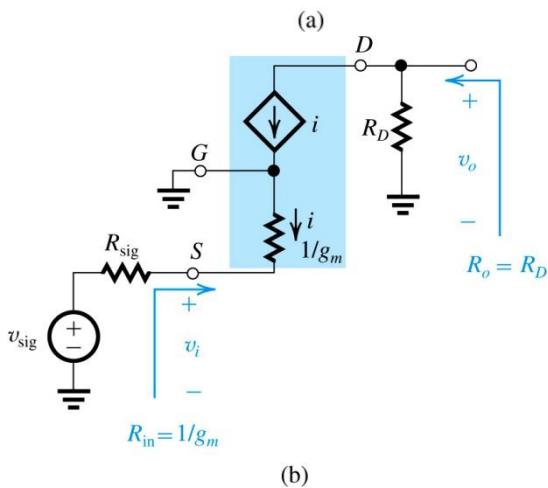


Figure 7.39 (a) Common-gate (CG) amplifier with bias arrangement omitted. (b) Equivalent circuit of the CG amplifier with the MOSFET replaced with its T model.



The Common-Gate (CG) Amplifier

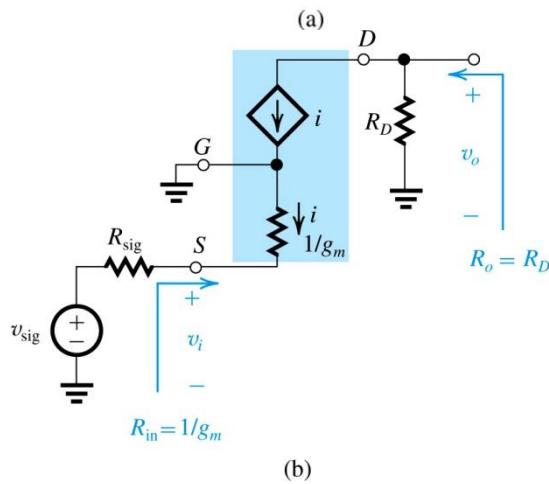
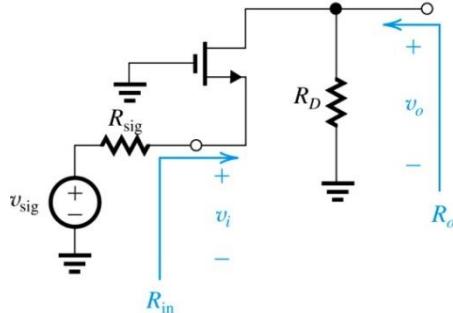


Figure 7.39 (a) Common-gate (CG) amplifier with bias arrangement omitted. (b) Equivalent circuit of the CG amplifier with the MOSFET replaced with its T model.

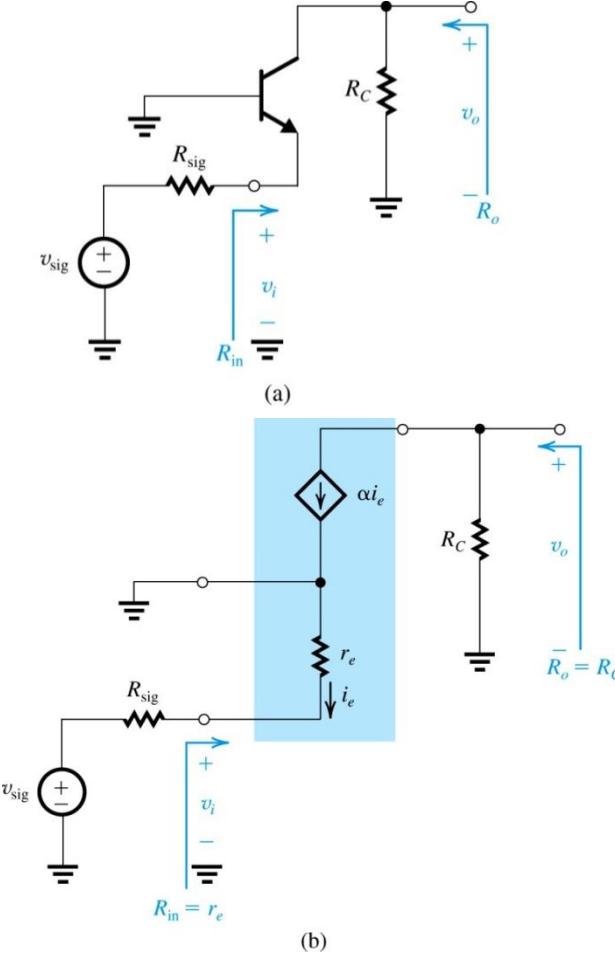
The **overall voltage gain** is: $G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$

Observe that the overall voltage gain is simply the ratio of the total resistance in the drain circuit to the total resistance in the source circuit. If R_{sig} is of the same order as R_D and R_L , G_v will be very small.

Because of its low input resistance, the CG amplifier alone has very limited application. One such application is to amplify high-frequency signals that come from sources with relatively low resistances. These include cables, where it is usually necessary for the input resistance of the amplifier to match the characteristic resistance of the cable. As will be shown in Chapter 10, the CG amplifier has excellent high-frequency response. Thus it can be combined with the CS amplifier in a very beneficial way that takes advantage of the best features of each of the two configurations. A very significant circuit of this kind will be studied In Chapter 10 (ELEG312!!).



Common Base (CB) Amplifier



The **input resistance** is: $R_{in} \equiv \frac{v_i}{i_i} = r_e$

$$v_o = -\alpha i_e R_C \quad i_e = -\frac{v_i}{r_e}$$

The **open-circuit voltage gain** is:

$$A_{vo} \equiv \frac{v_o}{v_i} = \frac{\alpha R_C}{r_e} = g_m R_C$$

The **output resistance** is: $R_o \equiv \frac{v_x}{i_x} = R_C$

The **amplifier voltage gain** is:

$$A_v \equiv \frac{v_o}{v_i} = g_m (R_C \parallel R_L)$$

The **overall voltage gain** is:

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{r_e}{r_e + R_{sig}} g_m (R_C \parallel R_L)$$

$$G_v = \alpha \frac{R_C \parallel R_L}{r_e + R_{sig}}$$

Figure 7.40 (a) CB amplifier with bias details omitted; (b) Amplifier equivalent circuit with the BJT represented by its T Model.



The Need for Voltage Buffers

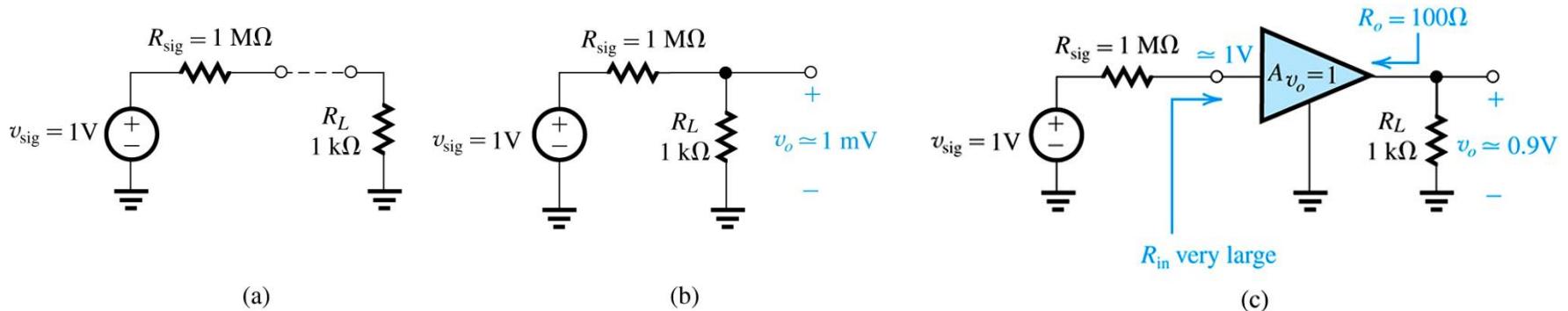
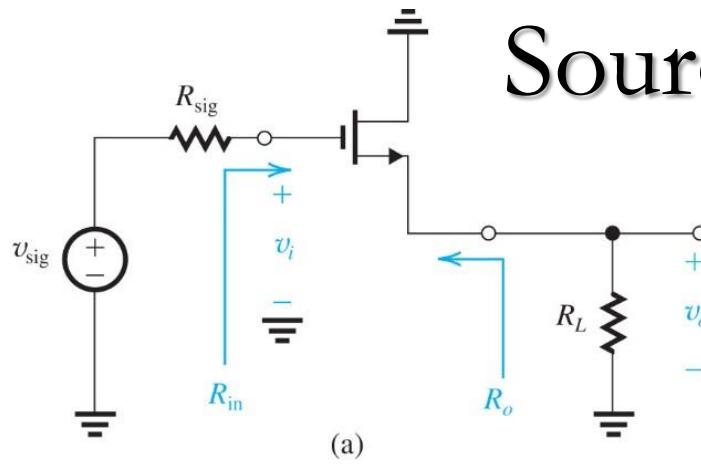


Figure 7.41 Illustrating the need for a unity-gain buffer amplifier.

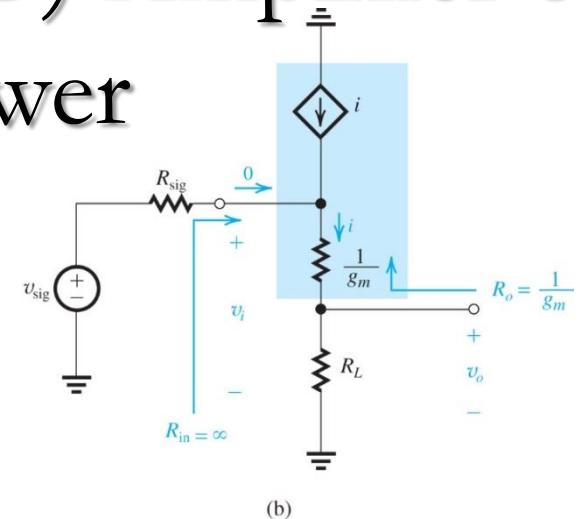
Consider the situation depicted in Fig. 7.41(a). A signal source delivering a signal of reasonable strength (1 V) with an internal resistance of $1\text{ M}\Omega$ is to be connected to a $1\text{-k}\Omega$ load resistance. Connecting the source to the load directly as in Fig. 7.41(b) would result in severe attenuation of the signal. An alternative course of action is suggested in Fig. 7.41(c). Here we have interposed an amplifier between the source and the load. Note that our amplifier has a very large input resistance, thus almost all of v_{sig} , (i.e., 1 V) will appear at the input of the amplifier proper. Since the amplifier has a low output resistance (100Ω), 90% of this signal (0.9 V) will appear at the output, obviously a very significant improvement over the situation without the amplifier.



The Common-Drain (CD) Amplifier or Source Follower



(a)



(b)

Figure 7.42 (a) Common-drain amplifier or source follower with the bias circuit omitted. (b) Equivalent circuit of the source follower obtained by replacing the MOSFET with its T model.

The **input resistance** is: $R_{in} \equiv \frac{v_i}{i_i} = \infty$

Use the T model and neglect r_o

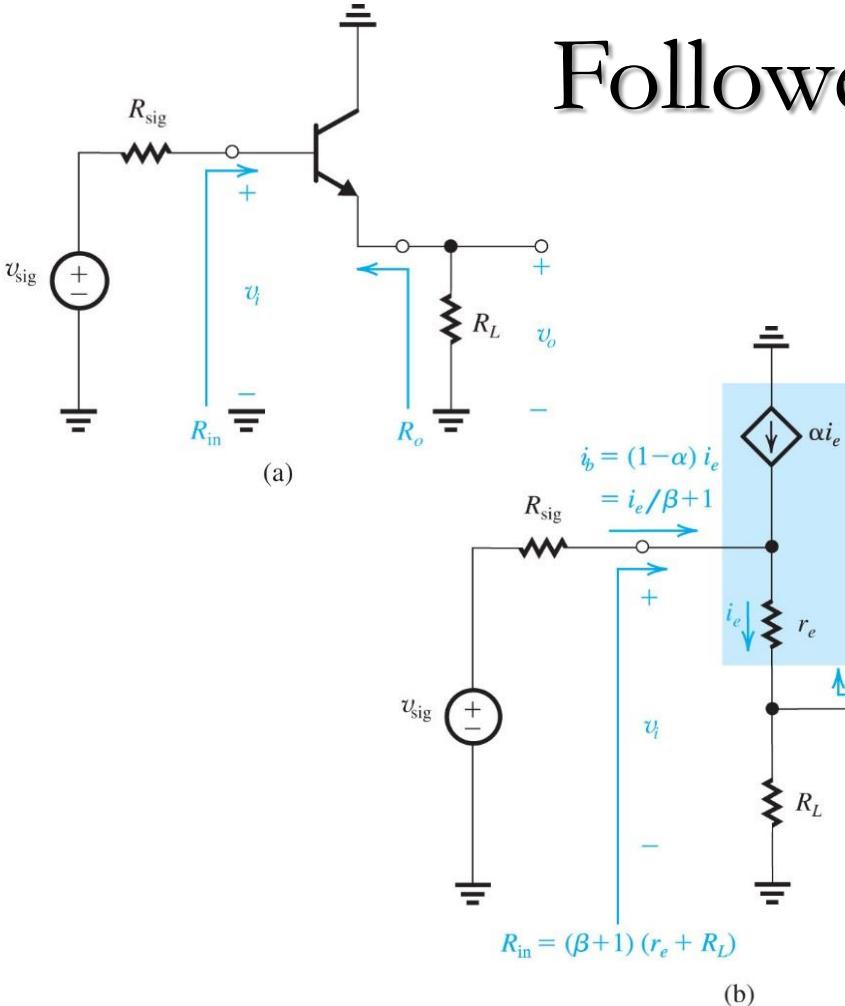
The **open-circuit voltage gain** is: $A_{vo} \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m} = 1$ Since $R_L = \infty$

The **output resistance** is: $R_o \equiv \frac{v_x}{i_x} = 1/g_m$

The **overall voltage gain** is: $G_v = A_v = \frac{R_L}{R_L + 1/g_m}$



Common-Collector (CC) or Emitter Follower Amplifier



The **input resistance** is: $R_{\text{in}} \equiv \frac{v_i}{i_b}$

$$i_e = \frac{v_i}{r_e + R_L}$$

$$R_{\text{in}} = (\beta + 1)(r_e + R_L)$$

The **amplifier voltage gain** is:

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + r_e}$$

The **open-circuit voltage gain** is:

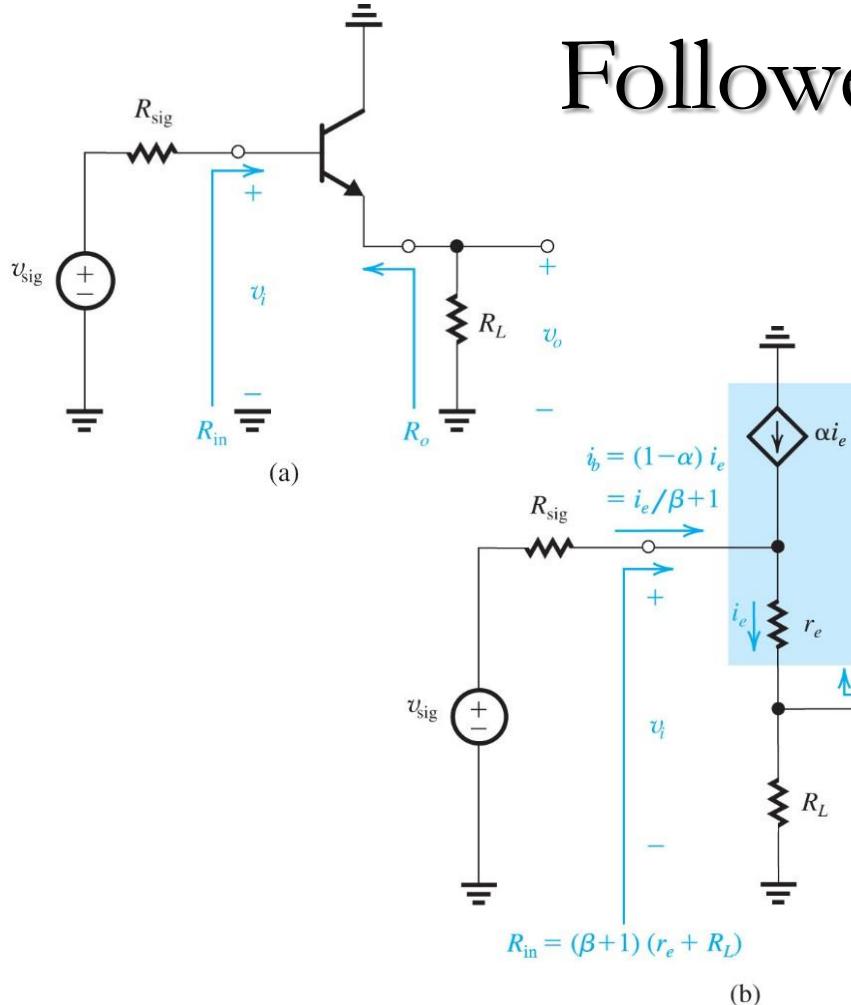
$$A_{vo} \equiv \frac{v_o}{v_i} = 1$$

The **output resistance** is: $R_o \equiv \frac{v_x}{i_x} = r_e$

Figure 7.43 (a) Common-collector amplifier or emitter follower with the bias circuit omitted.(b) Equivalent circuit obtained by replacing the BJT with its T model.



Common-Collector (CC) or Emitter Follower Amplifier



The overall voltage gain is: $G_v \equiv \frac{v_o}{v_{sig}}$

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}}$$

$$\frac{v_i}{v_{sig}} = \frac{(\beta + 1)(r_e + R_L)}{(\beta + 1)(r_e + R_L) + R_{sig}}$$

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{v_i}{v_{sig}} \times A_v$$

$$G_v = \frac{(\beta + 1)(r_e + R_L)}{(\beta + 1)(r_e + R_L) + R_{sig}} \frac{R_L}{R_L + r_e}$$

$$G_v = \frac{(\beta + 1)R_L}{(\beta + 1)r_e + (\beta + 1)R_L + R_{sig}}$$

Figure 7.43 (a) Common-collector amplifier or emitter follower with the bias circuit omitted.(b) Equivalent circuit obtained by replacing the BJT with its T model.



The Emitter Follower Amplifier

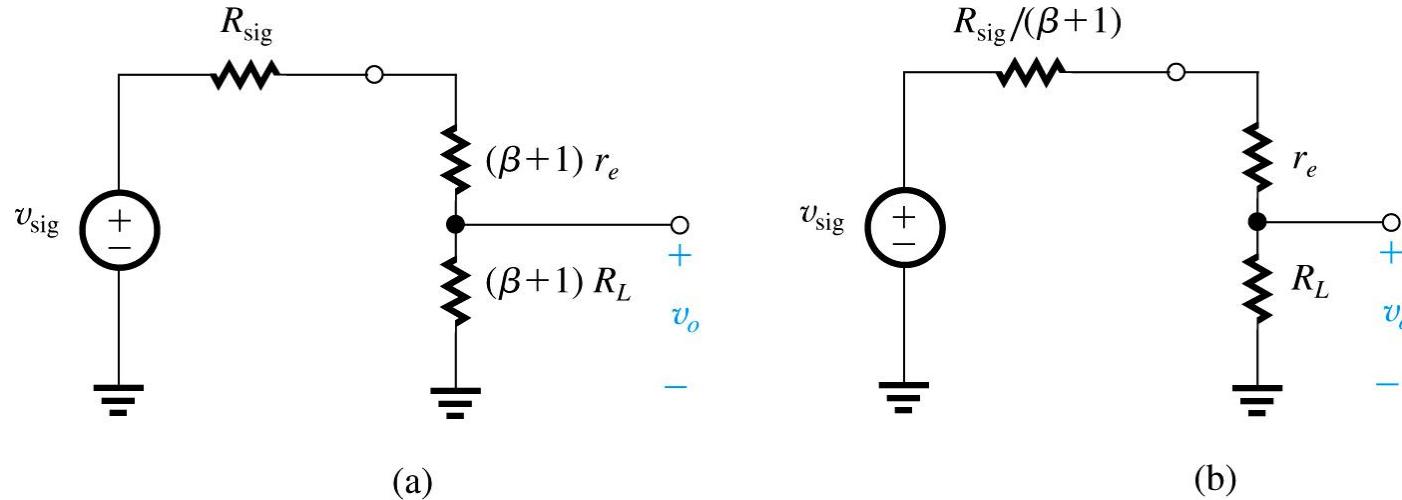


Figure 7.44 Simple equivalent circuits for the emitter follower obtained by (a) reflecting r_e and R_L to the base side, and (b) reflecting v_{sig} and R_{sig} to the emitter side. Note that the circuit in (b) can be obtained from that in (a) by simply dividing all resistances by $(\beta+1)$.

$$G_v = \frac{(\beta + 1)R_L}{(\beta + 1)r_e + (\beta + 1)R_L + R_{sig}}$$

$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{r_e + R_L + R_{sig}/(\beta + 1)}$$



Thevenin Representation of the Emitter-Follower Output

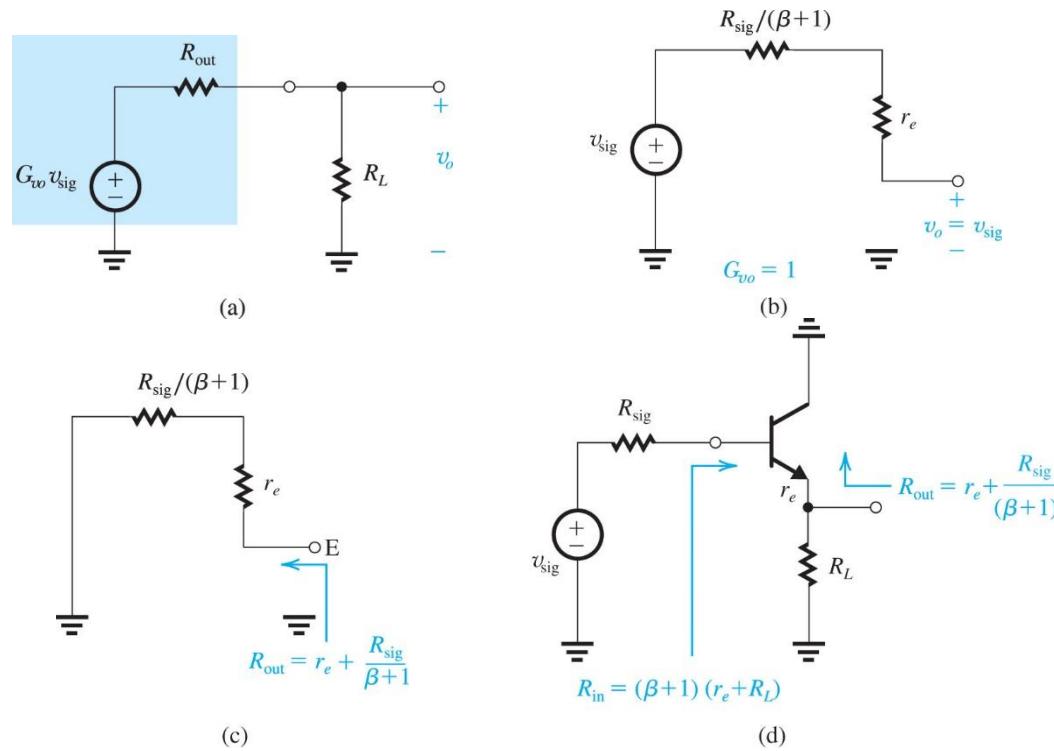
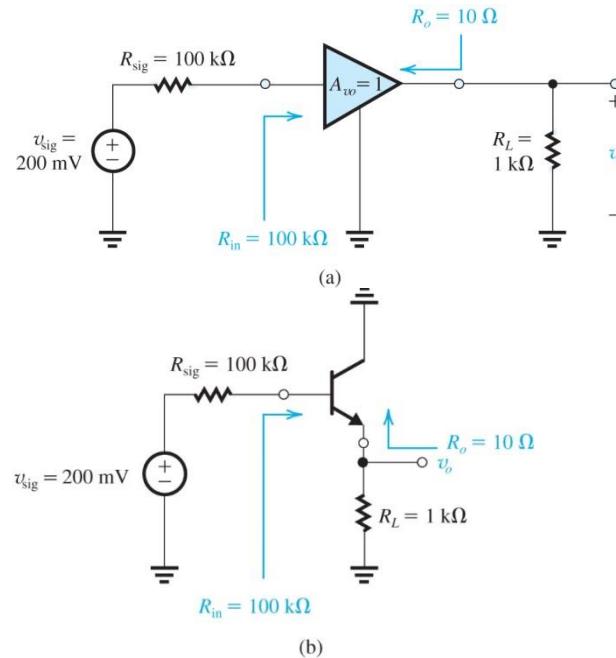


Figure 7.45 (a) Thevenin representation of the output of the emitter follower. (b) Obtaining G_{vo} from the equivalent circuit in Fig. 7.44(b). (c) Obtaining R_{out} from the equivalent circuit in Fig. 7.44(b) with v_{sig} set to zero. (d) The emitter follower with R_{in} and R_{out} determined simply by looking into the input and output terminals, respectively.



Example 7.10

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{\text{sig}} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 k Ω , and to 0.5 k Ω .



$$R_o = r_e = \frac{V_T}{I_E} = 10\Omega$$
$$\Rightarrow I_E = \frac{V_T}{r_e} = \frac{25\text{mV}}{10\Omega} = 2.5\text{mA}$$

$$R_{\text{in}} = (\beta + 1)(r_e + R_L) = 100\text{k}\Omega$$

$$\Rightarrow \beta_{\min} = \frac{100\text{k}\Omega}{(0.01\text{k}\Omega + 1\text{k}\Omega)} - 1 = 98$$

Figure 7.46 Circuit for Example 7.10.



Example 7.10

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{\text{sig}} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 k Ω , and to 0.5 k Ω .

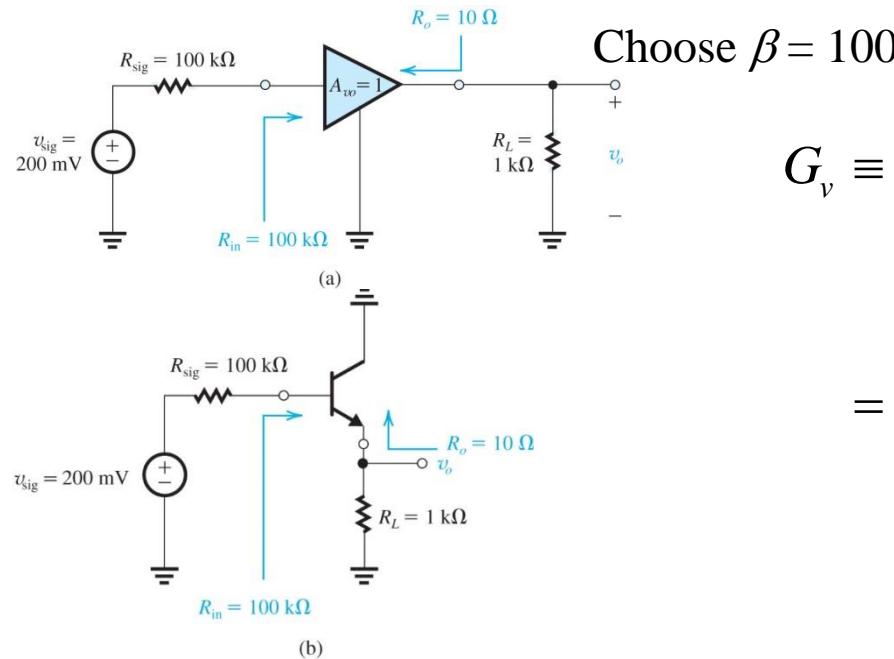


Figure 7.46 Circuit for Example 7.10.



Example 7.10

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{\text{sig}} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 k Ω , and to 0.5 k Ω .

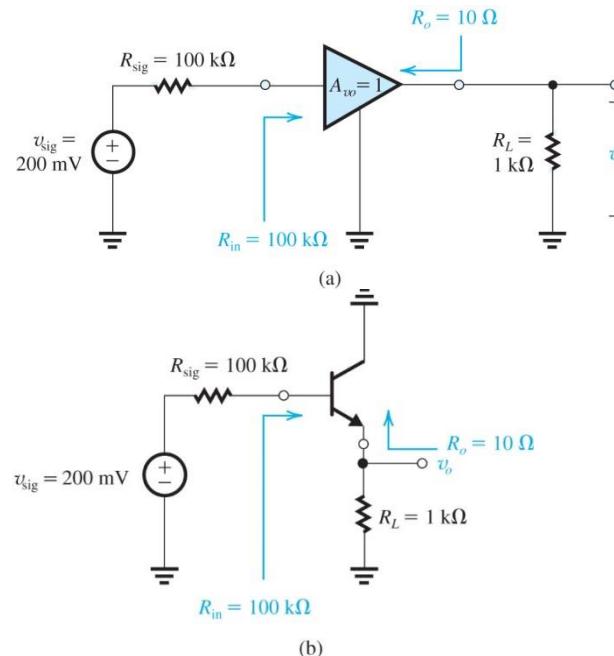
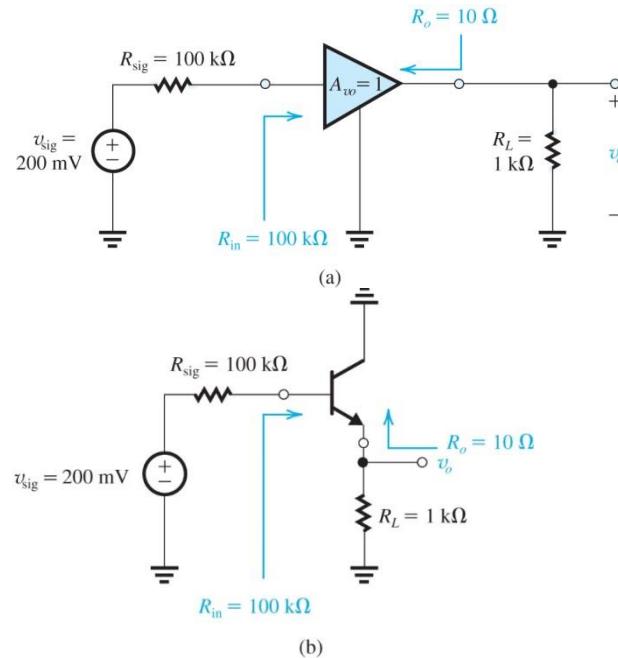


Figure 7.46 Circuit for Example 7.10.



Example 7.10

It is required to design an emitter follower to implement the buffer amplifier of Fig. 7.46(a). Specify the required bias current I_E and the minimum value the transistor β must have. Determine the maximum allowed value of v_{sig} if v_π is to be limited to 5 mV in order to obtain reasonably linear operation. With $v_{sig} = 200$ mV, determine the signal voltage at the output if R_L is changed to 2 k Ω , and to 0.5 k Ω .



$$G_v \equiv \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + R_{out}}$$

If $R_L = 2\text{k}\Omega$

$$v_o = v_{sig} \frac{R_L}{R_L + R_{out}} = 200\text{mV} \frac{2\text{k}\Omega}{2\text{k}\Omega + 1\text{k}\Omega} = 133.33\text{mV}$$

If $R_L = 0.5\text{k}\Omega$

$$v_o = v_{sig} \frac{R_L}{R_L + R_{out}} = 200\text{mV} \frac{0.5\text{k}\Omega}{0.5\text{k}\Omega + 1\text{k}\Omega} = 66.67\text{mV}$$

Figure 7.46 Circuit for Example 7.10.



Table 7.4 Characteristics of MOSFET Amplifiers

Amplifier type	R_{in}	A_{vo}	R_o	A_v	G_v
Common source	∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_S	∞	$\frac{g_m R_D}{1 + g_m R_S}$	R_D	$-\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$	$-\frac{g_m(R_D \parallel R_L)}{1 + g_m R_S}$
Common gate	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Common drain or source follower	∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$



Table 7.5 BJT Amplifier Summary

	R_{in}	A_{vo}	R_o	A_v	G_v
common emitter	$(\beta + 1)r_e$	$g_m R_C$	R_C	$-g_m(R_C \parallel R_L)$ $-\alpha \frac{R_C \parallel R_L}{r_e}$	$-\beta \frac{(R_C \parallel R_L)}{R_{sig} + (\beta + 1)r_e}$
common emitter with R_e	$(\beta + 1)(r_e + R_e)$	$-\frac{g_m R_C}{1 + g_m R_e}$	R_C	$-\frac{g_m(R_C \parallel R_L)}{1 + g_m R_e}$ $-\alpha \frac{R_C \parallel R_L}{r_e + R_L}$	$-\beta \frac{(R_C \parallel R_L)}{R_{sig} + (\beta + 1)(r_e + R_e)}$
common base	r_e	$g_m R_C$	R_C	$g_m(R_C \parallel R_L)$ $\alpha \frac{R_C \parallel R_L}{r_e}$	$\alpha \frac{R_C \parallel R_L}{R_{sig} + r_e}$
emitter follower	$(\beta + 1)(r_e + R_L)$	1	r_e	$\frac{R_L}{R_L + r_e}$	$\frac{R_L}{R_L + r_e + R_{sig}/(\beta + 1)}$ $G_{vo} = 1$ $R_{out} = r_e + \frac{R_{sig}}{\beta + 1}$



Summary of MOSFET and BJT Amplifiers

1. MOS amplifiers provide much higher, ideally infinite input resistances (except, of course, for the CG configuration). This is a definite advantage over BJT amplifiers.
2. BJTs exhibit higher g_m values than MOSFETs, resulting in higher gains.
3. For discrete-circuit amplifiers the BJT remains the device of choice. This is because discrete BJTs are much easier to handle physically than discrete MOSFETs and, more important, a very wide variety of discrete BJTs is available commercially. The remainder of this chapter is concerned with discrete-circuit amplifiers.
4. Integrated-circuit (IC) amplifiers predominantly use MOSFETs, although BJTs are utilized in certain niche areas. Chapters 8 to 13 are mainly concerned with IC amplifiers.
5. The CS and CE configurations are the best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.



Summary of MOSFET and BJT Amplifiers

6. Including a resistance R_s in the source of the CS amplifier (a resistance R_e in the emitter of the CE amplifier) provides a number of performance improvements at the expense of gain reduction.
7. The low input resistance of the CG and CB amplifiers makes them useful only in specific applications. As we shall see in Chapter 10, these two configurations exhibit a much better high-frequency response than that available from the CS and CE amplifiers. This makes them useful as high-frequency amplifiers, especially when combined with the CS or CE circuit. We shall study one such combination in Chapter 8.
8. The source follower (emitter follower) finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load, and as the output stage in a multistage amplifier, where its purpose is to equip the amplifier with a low output resistance.



When and How to Include the Output Resistance r_o

So far we have been neglecting the output resistance r_o of the MOSFET and the BJT. We have done this to keep things simple and because our main interest in this chapter is discrete-circuit design, where the circuit resistances (e.g., R_C , R_D , and R_L) are usually much smaller than r_o . Nevertheless, in some instances it is relatively easy to include r_o in the analysis. Specifically:

1. In the CS and CE amplifiers, it can be seen that r_o of the transistor appears in parallel with R_D and R_C , respectively, and can be simply included in the corresponding formulas in Tables 7.4 and 7.5 by replacing R_D with $(R_D \parallel r_o)$ and R_C with $(R_C \parallel r_o)$. The effect will be a reduction in the magnitude of gain, of perhaps 5% to 10%.
2. In the source and emitter followers, it can be seen that the transistor r_o appears in parallel with R_L and can be taken into account by replacing R_L in the corresponding formulas with $(R_L \parallel r_o)$. Thus, here too, the effect of taking r_o into account is a small reduction in gain. More significant, however, taking r_o into account reduces the open-circuit voltage gain A_{vo} from unity to

$$A_{vo} = \frac{r_o}{r_o + (1/g_m)}$$



Homework #15

- Read Chapter 7
- Chapter 7 Problems:
 - 7.59*
 - 7.60
 - 7.64*
 - 7.68
 - 7.71
 - 7.75

* Answers in Appendix L



7.4 BIASING



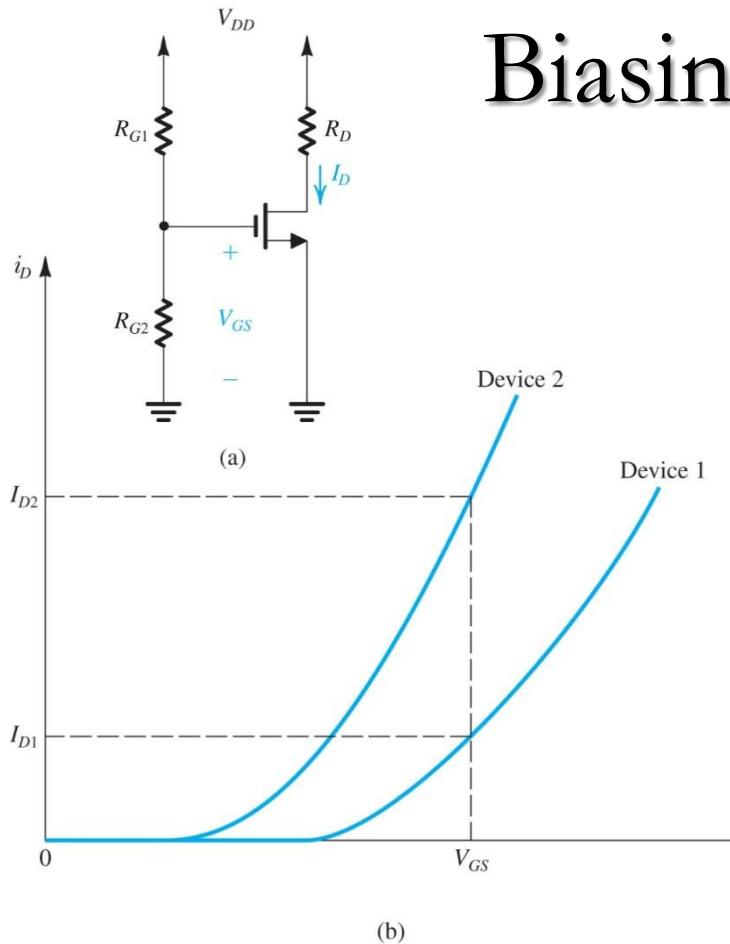


Figure 7.47 (a) Biasing the MOSFET with a constant V_{GS} generated from V_{DD} using a voltage divider (R_{G1}, R_{G2}); (b) the use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D . Devices 1 and 2 represent extremes among units of the same type.

Biasing by Fixing V_{GS}

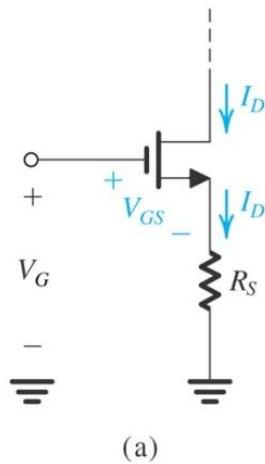
The most straight forward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide the desired I_D .

$$I_D = \frac{1}{2} k'_n \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2$$

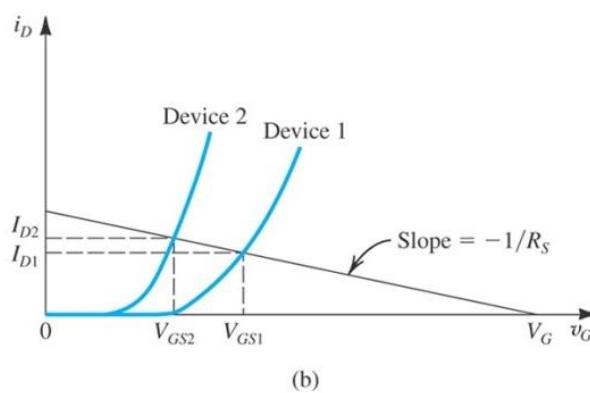
NOT a good idea as parameters can vary widely from device to device. Fig. 7.47 shows two i_D - v_{GS} characteristic curves representing extreme values in a batch of MOSFETs of the same type.



Biasing by Fixing V_{GS} and Adding a Source Resistance



(a)



(b)

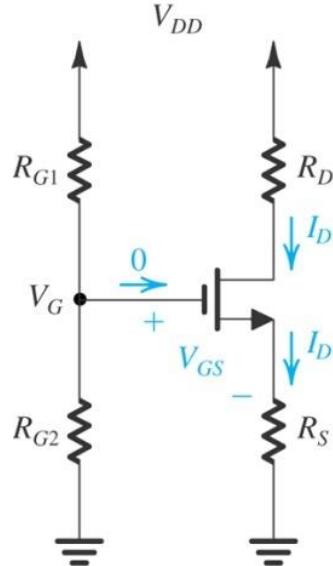
An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G , and connecting a resistance in the source lead, as shown in Fig. 7.48(a).
$$V_G = V_{GS} + R_S I_D$$

since V_G is constant, V_{GS} will have to decrease if I_D increases. This in turn results in a decrease in I_D , a change that is opposite to that initially assumed. Thus the action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name **degeneration resistance**.

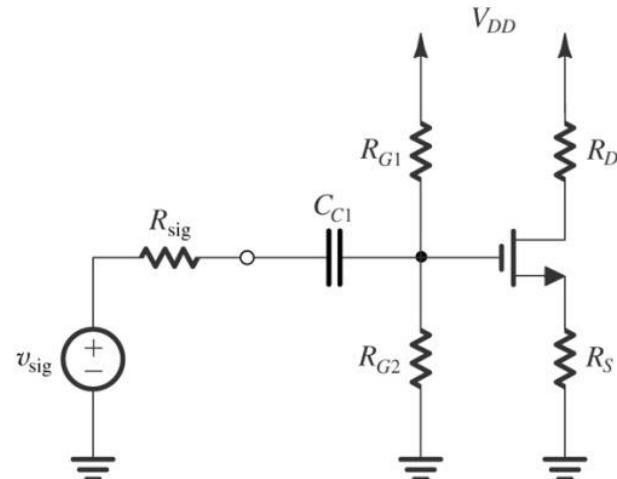
7.48 Biasing using a fixed voltage at the gate, V_G , and a resistance in the source lead, R_S : (a) basic arrangement; (b) reduced variability in I_D ;



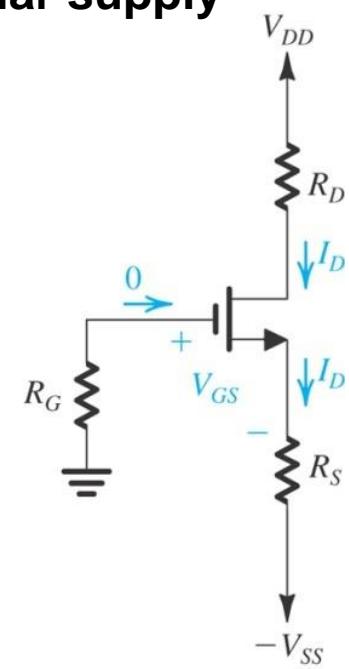
Biasing by Fixing V_{GS} and Adding a Source Resistance

Single supply

(c)

Single supply with AC coupled source

(d)

Bipolar supply

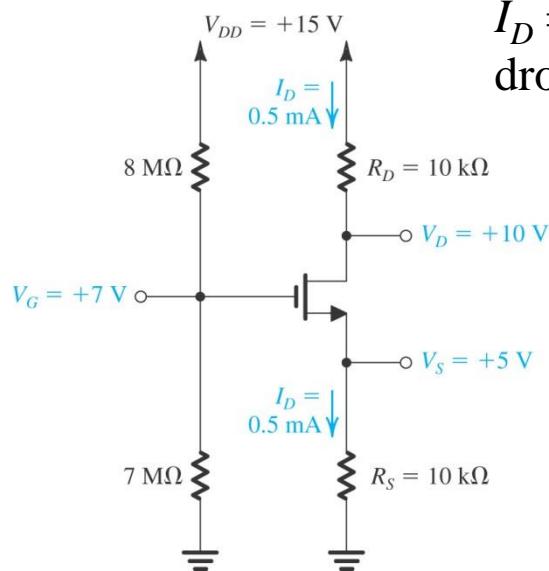
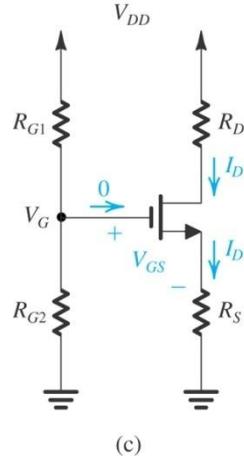
(e)

Figure 7.48 Biasing using a fixed voltage at the gate, V_G , and a resistance in the source lead, R_S : (c) practical implementation using a single supply; (d) coupling of a signal source to the gate using a capacitor C_{C1} ; (e) practical implementation using two supplies.



Example 7.11a

It is required to design the circuit of Fig. 7.48(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n'W/L = 1$ mA/V². For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'W/L$ but $V_t = 1.5$ V.



$I_D = 0.5$ mA so $R_D = R_S = 10$ k Ω so that 5 V is dropped across each resistor

$$V_{OV} = \sqrt{\frac{I_D}{\frac{1}{2}k'_n\left(\frac{W}{L}\right)}} = 1V = V_{GS} - V_t$$

$$V_{GS} = 2V \quad V_G = 7V$$

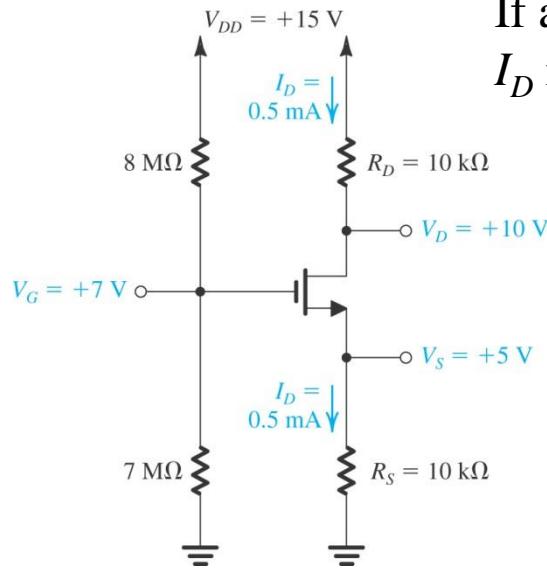
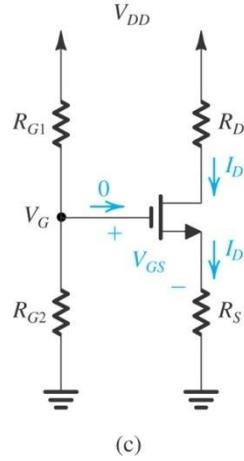
$$R_{G1} = 8M\Omega \quad R_{G2} = 7M\Omega$$

Figure 7.49 Circuit for Example 7.11.



Example 7.11b

It is required to design the circuit of Fig. 7.48(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n'W/L = 1$ mA/V². For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'W/L$ but $V_t = 1.5$ V.



If a new NMOS transistor with $V_t = 1.5$ V the new I_D is:

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{tn})^2$$

$$V_{GS} = V_G - V_S = 7V - I_D R_S$$

From MATHCAD $I_D = 455$ μ A or
 674 μ A

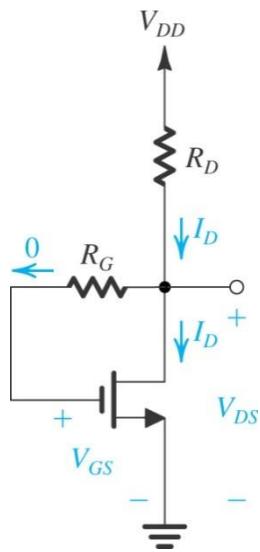
$$\frac{0.455 - 0.5}{0.5} = -9\%$$

Figure 7.49 Circuit for Example 7.11.



Biasing with a Drain-to-Gate Feedback Resistance

A simple and effective discrete-circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in Fig. 7.50. Here the large feedback resistance R_G (usually in the megohm range) forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$). Thus we can write



$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \quad \text{or} \quad V_{DD} = V_{GS} + R_D I_D$$

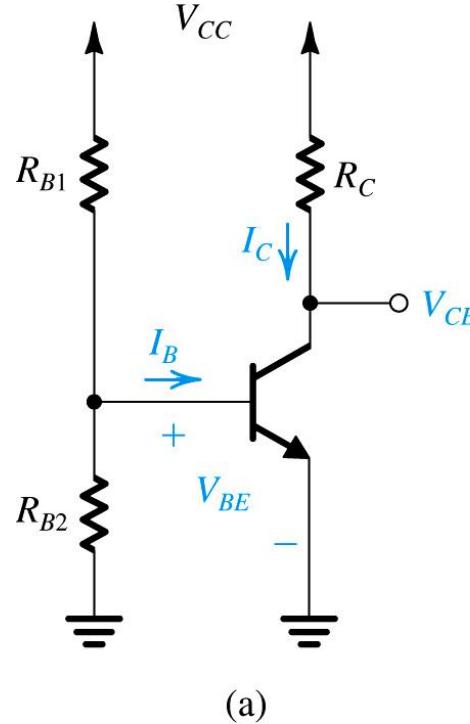
Which is identical in form to the CS with the source resistance case. Since V_{DD} is constant, V_{GS} will have to decrease if I_D increases. This in turn results in a decrease in I_D , a change that is opposite to that initially assumed. Thus the **negative feedback** or **degeneration** provided by R_G works to keep the value of I_D as constant as possible.

Figure 7.50 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G .



“Bad” BJT Biasing Schemes

Susceptible
to V_{BE}
variations



Susceptible
to β
variations

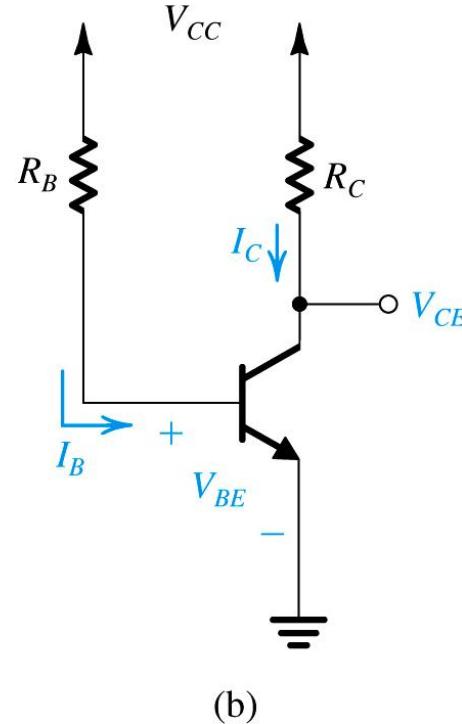


Figure 7.51 Two obvious schemes for biasing the BJT: (a) by fixing V_{BE} ; (b) by fixing I_B . Both result in wide variations in I_C and hence in V_{CE} and therefore are considered to be “bad.” Neither scheme is recommended.



Single Supply Biasing Technique

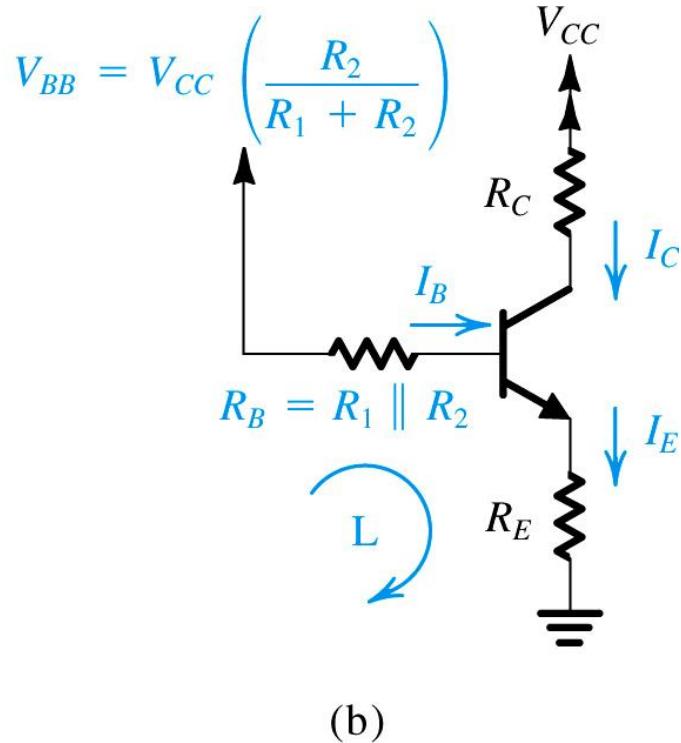
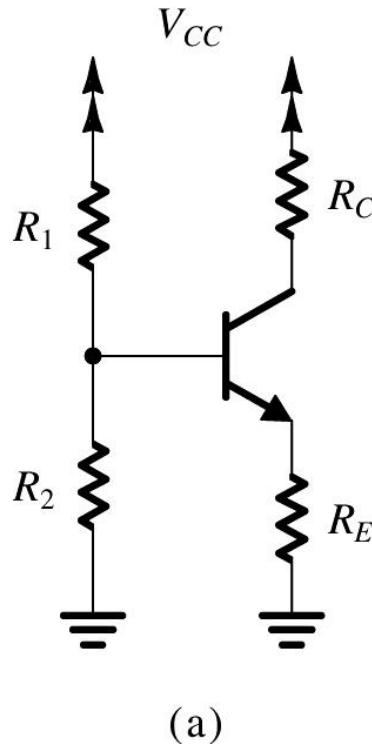


Figure 7.52 Classical biasing for BJTs using a single power supply: (a) circuit; (b) circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta + 1)}$$

We place constraints

$$V_{BB} \gg V_{BE}$$

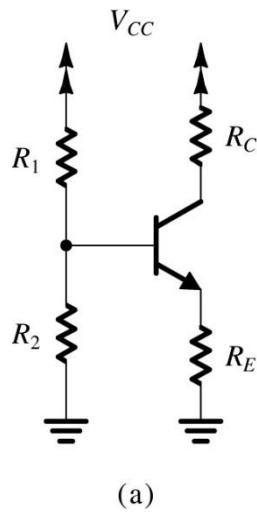
$$R_E \gg \frac{R_B}{\beta + 1}$$

Resistor R_E provides a **negative feedback** action that stabilizes the bias current.



Example 7.12

We wish to design the bias network of the amplifier in Fig. 7.52 to establish a current $I_E = 1 \text{ mA}$ using a power supply $V_{CC} = +12 \text{ V}$. The transistor is specified to have a nominal β value of 100.



$$V_B = 4\text{V}$$

$$V_E = V_B - V_{BE} = 4\text{V} - 0.7\text{V} = 3.3\text{V}$$

$$R_E = \frac{V_E}{I_E} = \frac{3.3\text{V}}{1\text{mA}} = 3.3\text{k}\Omega$$

Choose a bias voltage divider current of 0.1 $I_E = 0.1\text{mA}$

$$R_1 + R_2 = \frac{V_{CC}}{0.1I_E} = \frac{12\text{V}}{0.1\text{mA}} = 120\text{k}\Omega$$

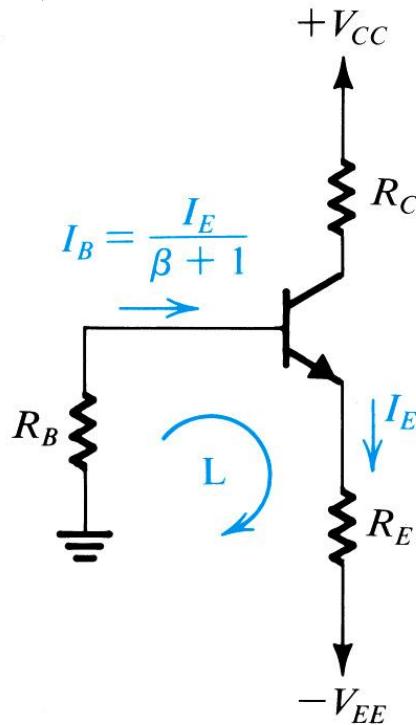
$$12\text{V} \left(\frac{R_2}{R_1 + R_2} \right) = 12\text{V} \left(\frac{R_2}{120\text{k}\Omega} \right) = 4\text{V} \Rightarrow R_2 = 40\text{k}\Omega; R_1 = 80\text{k}\Omega$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12\text{V} - 8\text{V}}{\alpha I_E} = \frac{4\text{V}}{\left(\frac{100}{101}\right)\text{1mA}} = 4.04\text{k}\Omega$$

R. Martin



Dual Power Supply Bias Scheme



$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)}$$

This equation is identical to the previous single ended supply configuration except for V_{EE} replacing V_{BB} . Thus the two previous constraints apply here as well.

$$V_{BB} \gg V_{BE}$$

$$R_E \gg \frac{R_B}{\beta + 1}$$

Figure 7.53 Biasing the BJT using two power supplies. Resistor R_B is needed only if the signal is to be capacitively coupled to the base. Otherwise, the base can be connected directly to ground, or to a grounded signal source, resulting in almost total β -independence of the bias current.



Biasing with a Collector to Base Feedback Resistor

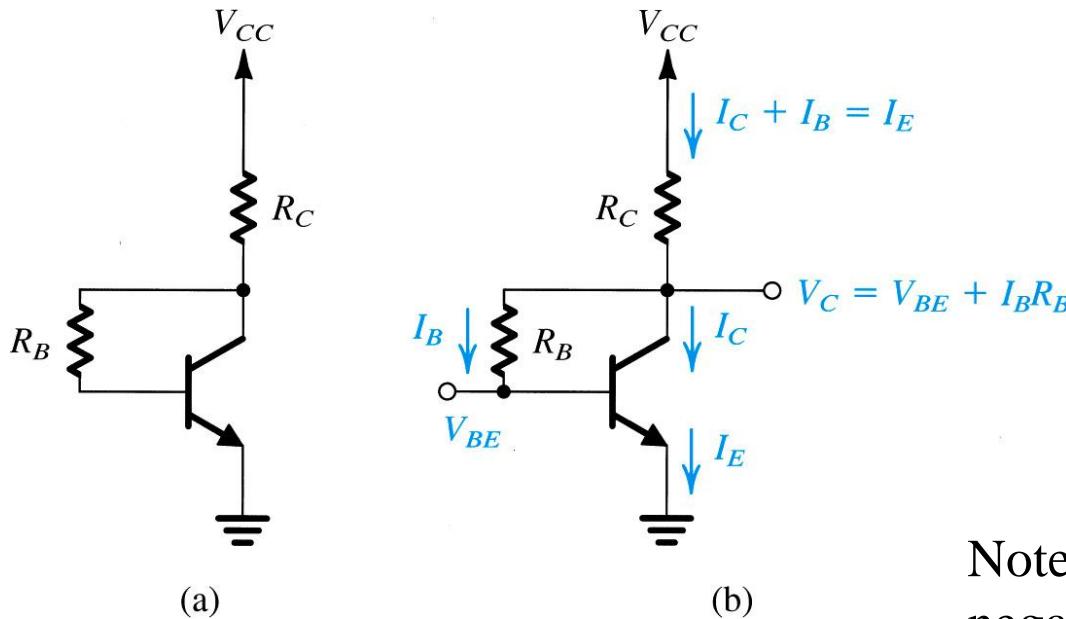


Figure 7.54 (a) A common-emitter transistor amplifier biased by a feedback resistor R_B . (b) Analysis of the circuit in (a).

$$V_{CC} = I_E R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE}$$

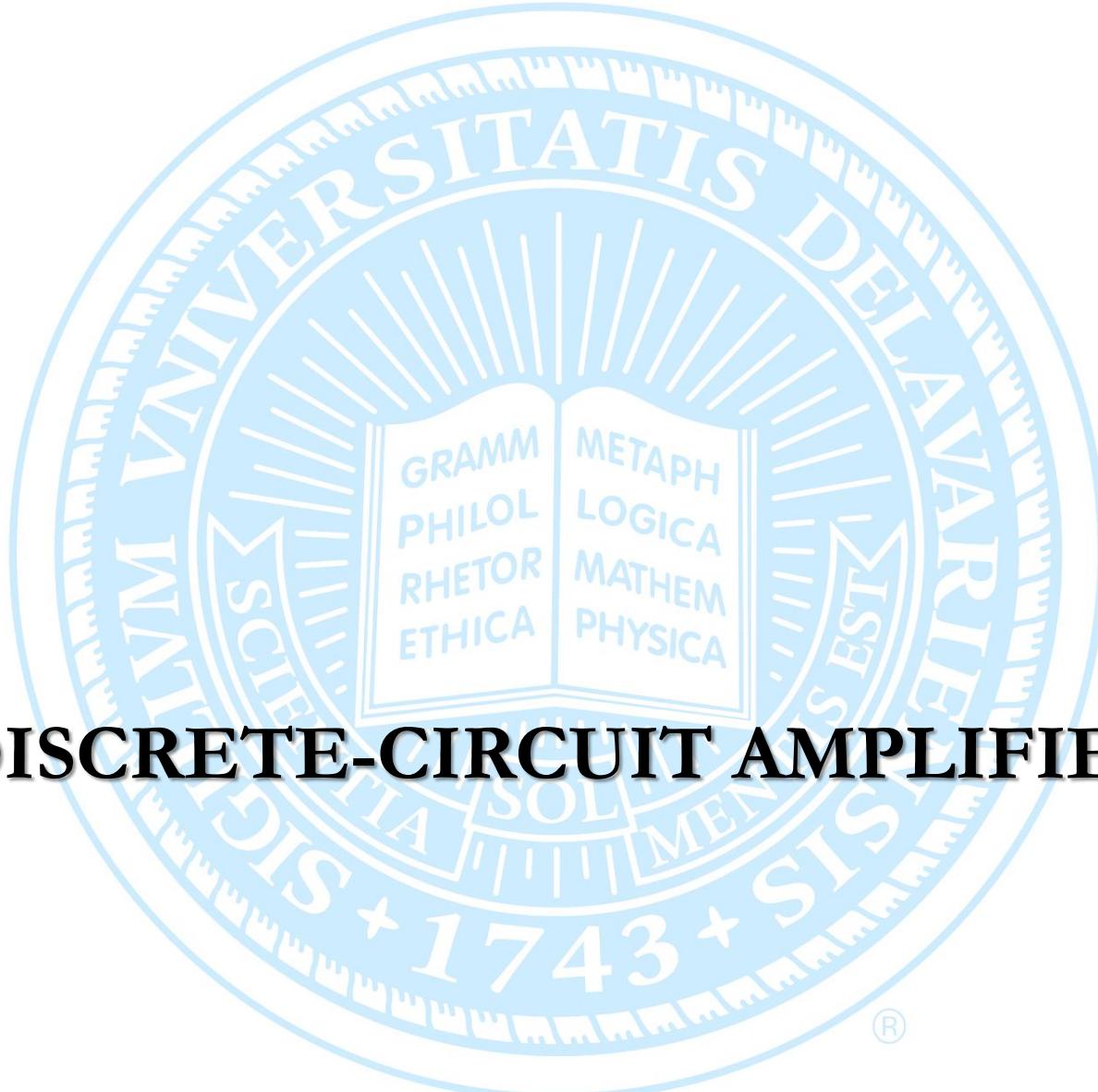
$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B / (\beta + 1)}$$

We place constraint

$$R_B / (\beta + 1) \ll R_C$$

Note R_B determines the allowable negative signal swing at the collector since

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta + 1}$$



7.5 DISCRETE-CIRCUIT AMPLIFIERS



The Common-Source (CS) Amplifier

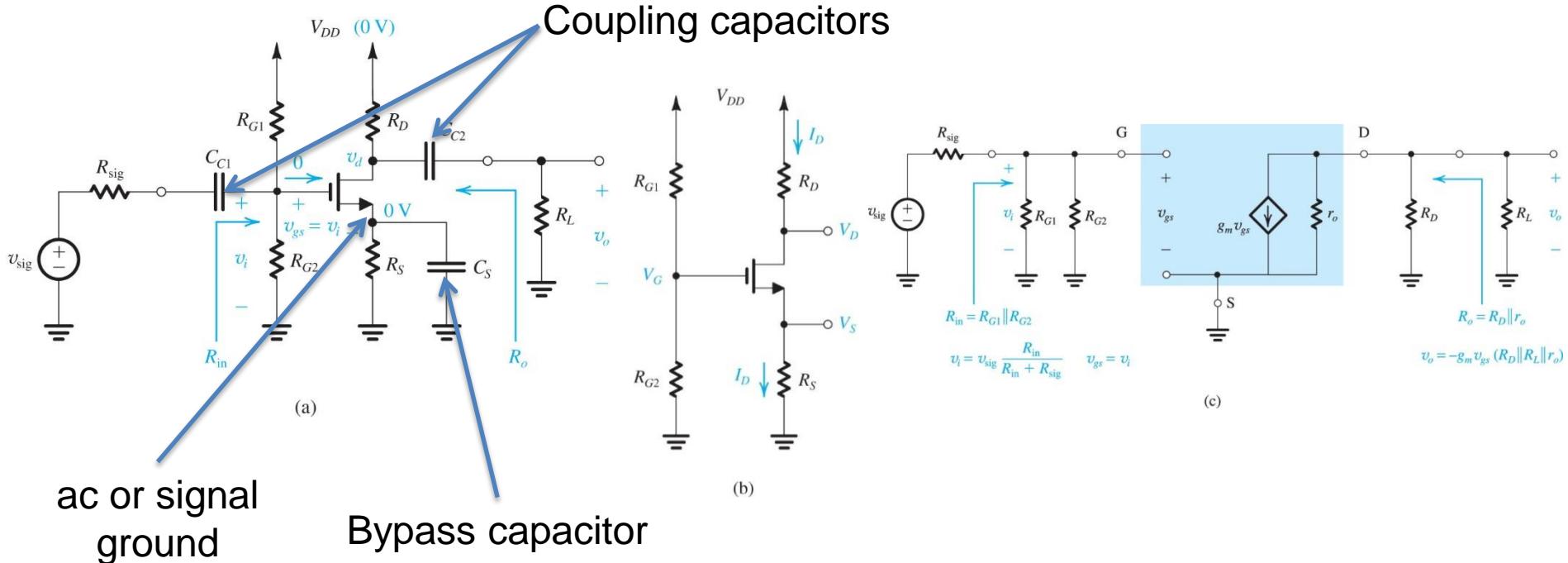


Figure 7.55 (a) A common-source amplifier using the classical biasing arrangement of Fig. 7.48(c). (b) Circuit for determining the bias point. (c) Equivalent circuit and analysis.

$$R_{in} = R_G = R_{G1} \parallel R_{G2}$$

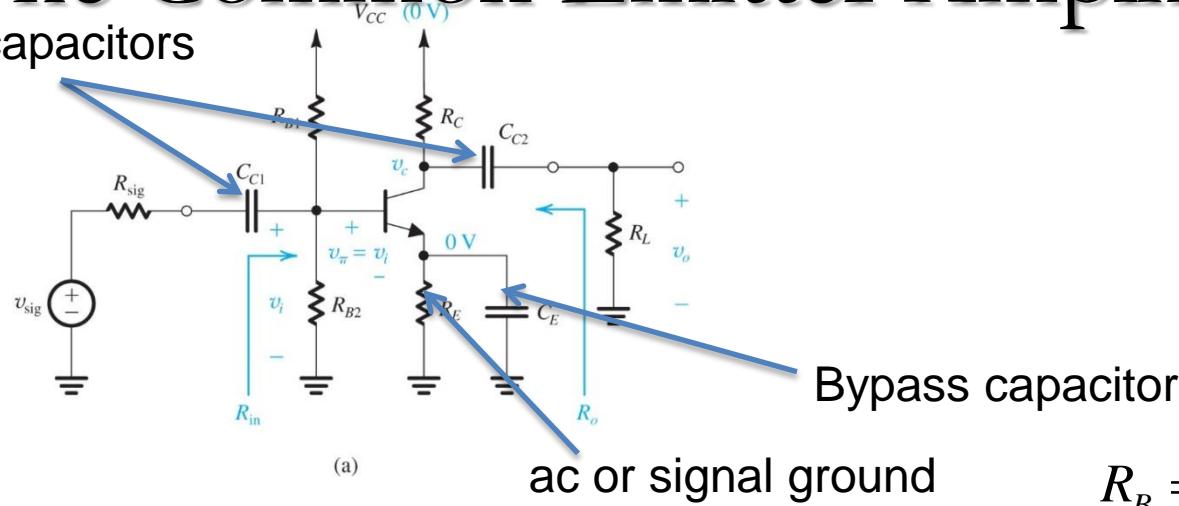
$$R_o = R_D \parallel r_o$$

$$G_v = -\frac{R_{in}}{R_{in} + R_{sig}} g_m (R_D \parallel R_L \parallel r_o)$$

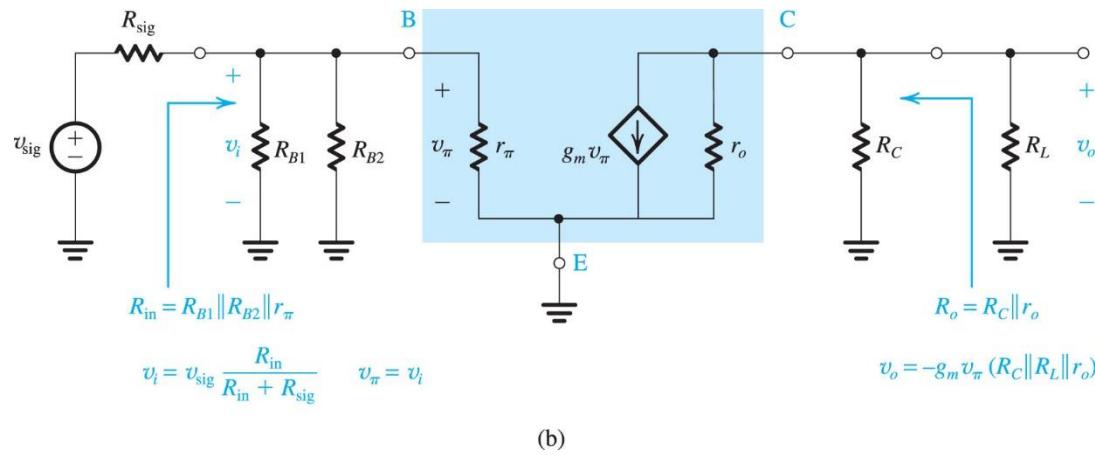


The Common Emitter Amplifier

Coupling capacitors



$$R_B = R_{B1} \parallel R_{B2}$$



$$R_{in} = R_B \parallel r_\pi = R_{B1} \parallel R_{B2} \parallel r_\pi$$

Figure 7.56 (a) A common-emitter amplifier using the classical biasing arrangement of Fig. 7.52(a). (b) Equivalent circuit and analysis.



The Common Emitter Amplifier with an Emitter Resistor

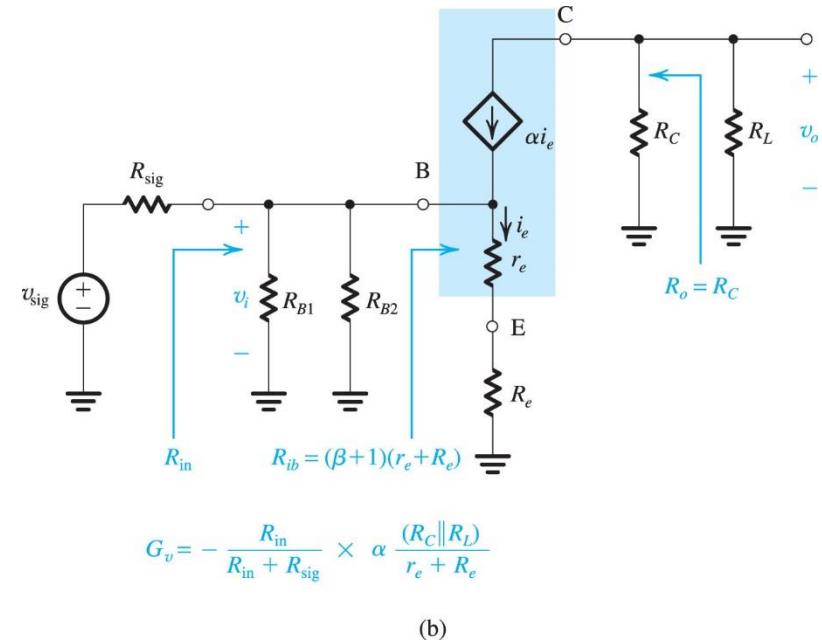
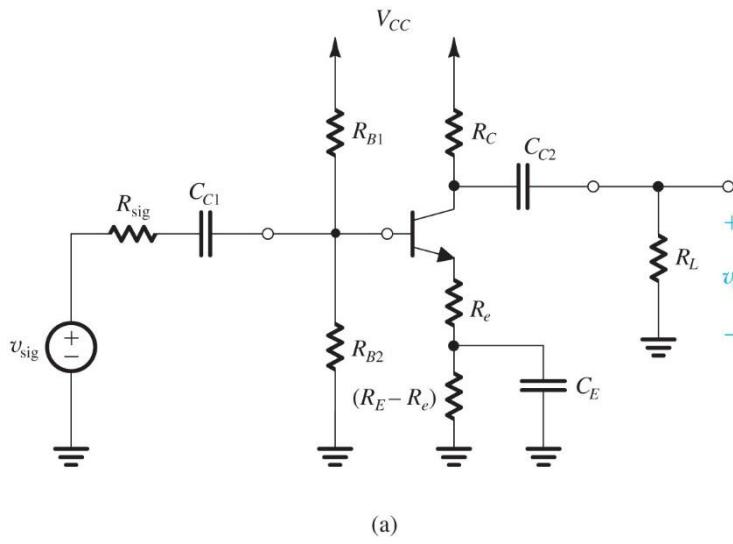


Figure 7.57 (a) A common-emitter amplifier with an unbiased emitter resistance R_e . (b) The amplifier small-signal model and analysis.

$$R_{in} = R_B \parallel [(\beta + 1)(r_e + R_e)]$$



The Common Base Amplifier

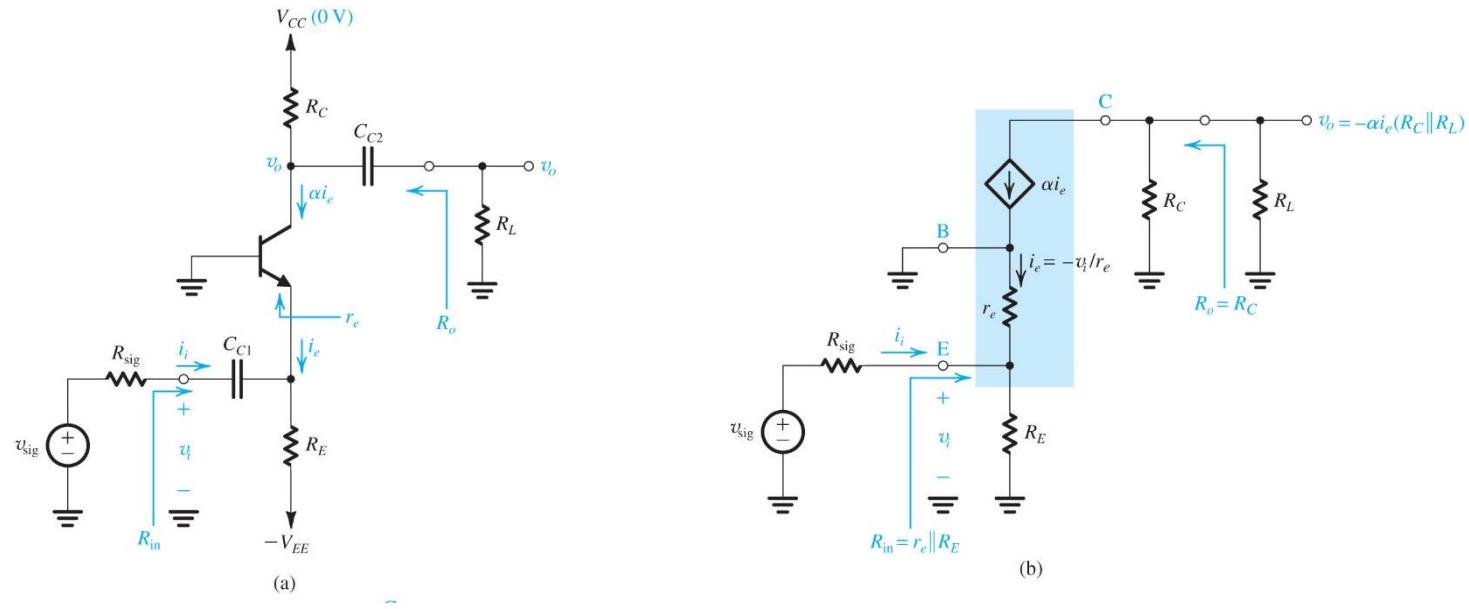


Figure 7.58 (a) A common-base amplifier using the structure of Fig. 7.53 with R_B omitted (since the base is grounded). (b) Equivalent circuit obtained by replacing the transistor with its T model.



The Emitter-Follower Circuit

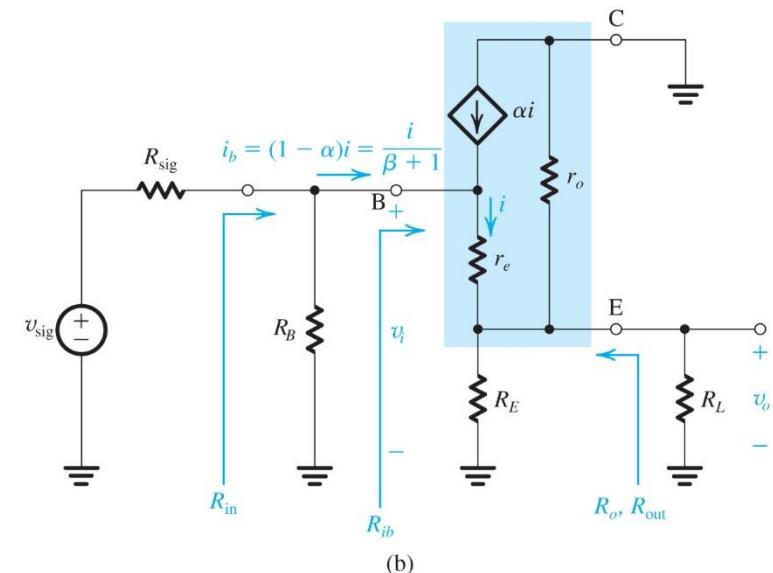
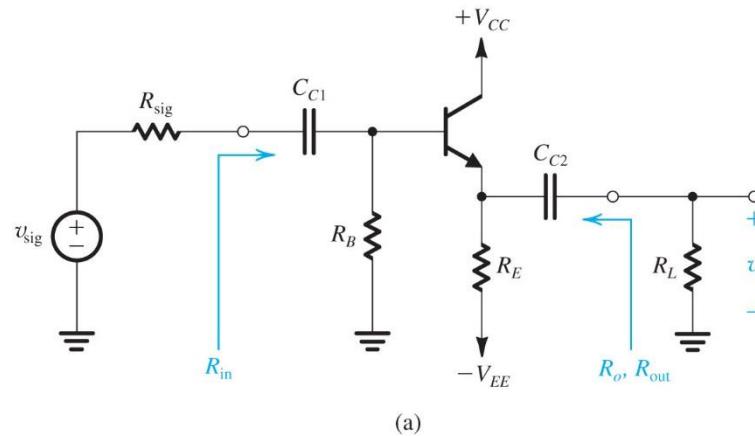


Figure 7.59 (a) An emitter-follower circuit. (b) Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model. Note that r_o is included because it is easy to do so. Normally, its effect on performance is small.

$$R_{in} = R_B \parallel [(\beta + 1)(r_e + R_L)]$$



The Amplifier Frequency Response

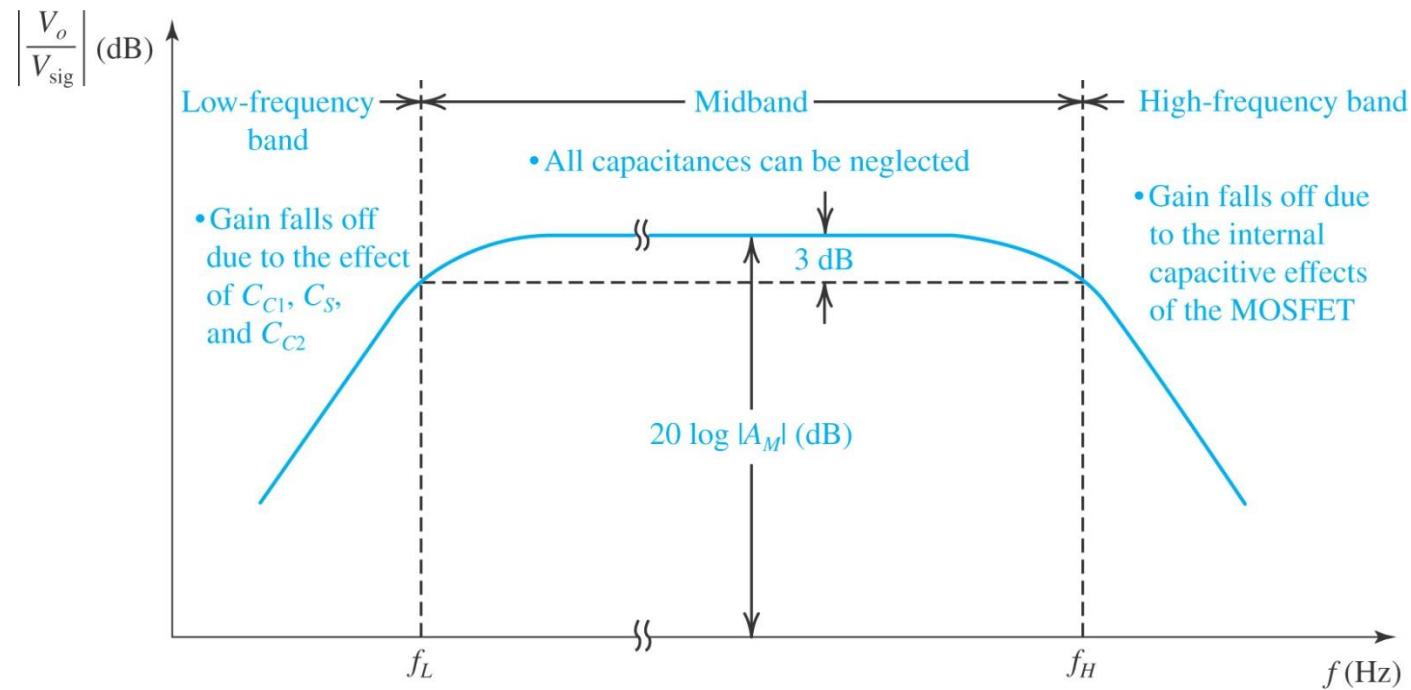


Figure 7.60 Sketch of the magnitude of the gain of a CE (Fig. 7.56) or CS (Fig. 7.55) amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency-response determination.

A figure of merit for the amplifier is its gain-bandwidth product, defined as

$$GB = |A_M|BW$$

where $|A_M|$ is the magnitude of the amplifier gain in the midband.



Homework #16

- Read Chapter 7
- Chapter 7 Problems:
 - 7.92*
 - 7.117
 - 7.125
 - 7.129
 - 7.135

* Answers in Appendix L



Summary

- The essence of the use of the MOSFET (the BJT) as an amplifier is that when the transistor is operated in the active region, v_{GS} controls i_D (v_{BE} controls i_C) in the manner of a voltage-controlled current source. When the device is dc biased in the active region, and the signal v_{gs} (v_{be}) is kept small, the operation becomes almost linear, with $i_d = g_m v_{gs}$ ($i_c = g_m v_{be}$).
- The most fundamental parameter in characterizing the small-signal linear operation of a transistor is the transconductance g_m . For a MOSFET, $g_m = \mu_n C_{ox} (W/L) V_{OV} = (2\mu_n C_{ox} (W/L) I_D)^{1/2} = 2I_D/V_{OV}$; and for the BJT, $g_m = I_C/V_T$.
- A systematic procedure for the analysis of a transistor amplifier circuit is presented in Table 7.1. Tables 7.2 and 7.3 present the small-signal models for the MOSFET and the BJT, respectively.
- When a resistance is connected in series with the source (or emitter), the T model is the most convenient to use.



Summary

- The three basic configurations of MOS and BJT amplifiers are presented in Fig. 7.33. Their characteristic parameter values are provided in Table 7.4 (for the MOS case) and in Table 7.5 (for the BJT case).
- The CS amplifier, which has (ideally) infinite input resistance and a reasonably high gain but a rather high output resistance and a limited high-frequency response (more on the latter point in Chapter 10), is used to obtain most of the gain in a cascade amplifier. Similar remarks apply to the CE amplifier, except that it has a relatively low input resistance ($r_\pi = \beta/g_m$) arising from the finite base current of the BJT (finite β). Its voltage gain, however, can be larger than that of the CS amplifier because of the higher values of g_m obtained with BJTs.
- Adding a resistance R_s in the source of a CS amplifier (a resistance R_e in the emitter of a CE amplifier) can lead to beneficial effects including the following: raising the input resistance of the CE amplifier, increasing linearity, and extending the useful amplifier bandwidth, at the expense of reducing the gain, all by a factor equal to $(1 + g_m R_s)$ [$(1 + g_m R_e)$ for the BJT case].



Summary

- The CG (CB) amplifier has a low input resistance and thus, used alone has limited and specialized applications. However, its excellent high-frequency response makes it attractive in combination with the CS (CE) amplifier.
- The source follower has (ideally) infinite input resistance, a voltage gain lower than but close to unity, and a low output resistance. It is employed as a voltage buffer and as the output stage of a multistage amplifier. Similar remarks apply to the emitter follower except that its input resistance, though large, is finite. Specifically, the emitter follower multiplies the total resistance in the emitter by $(\beta + 1)$ before presenting it to the signal source.
- The resistance-reflection rule is a powerful tool in the analysis of BJT amplifier circuits: All resistances in the emitter circuit including the emitter resistance r_e can be reflected to the base side by multiplying them by $(\beta + 1)$. Conversely, we can reflect all resistances in the base circuit to the emitter side by dividing them by $(\beta + 1)$.



Summary

- In the analysis and design of discrete-circuit amplifiers, it is rarely necessary to take the transistor output resistance r_o into account. In some situations, however, r_o can be easily taken into account; specifically in the CS (CE) amplifier and in the source (emitter) follower. In IC amplifiers, r_o must always be taken into account.
- A key step in the design of transistor amplifiers is to bias the transistor to operate at an appropriate point in the active region. A good bias design ensures that the parameters of the operating point (I_D , V_{OV} , and V_{DS} for the MOSFET; I_C and V_{CE} for the BJT) are predictable and stable and do not vary by large amounts when the transistor is replaced by another of the same type. The bias methods studied in this chapter are suited for discrete-circuit amplifiers only because they utilize large coupling and bypass capacitors.
- Discrete-circuit amplifiers predominantly employ BJTs. The opposite is true for IC amplifiers, where the device of choice is the MOSFET.