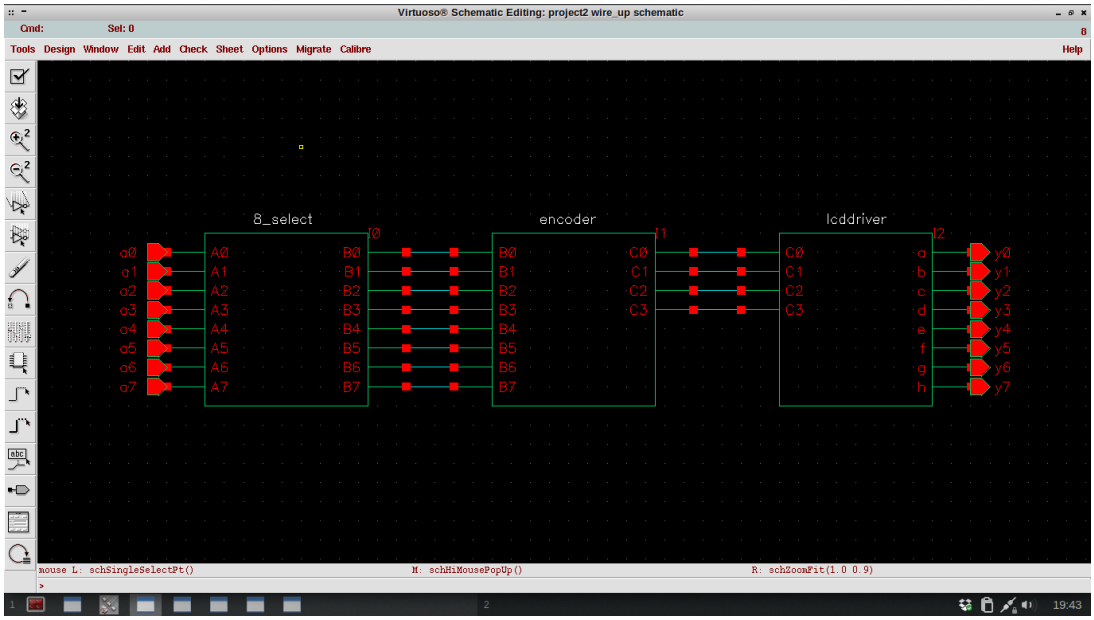
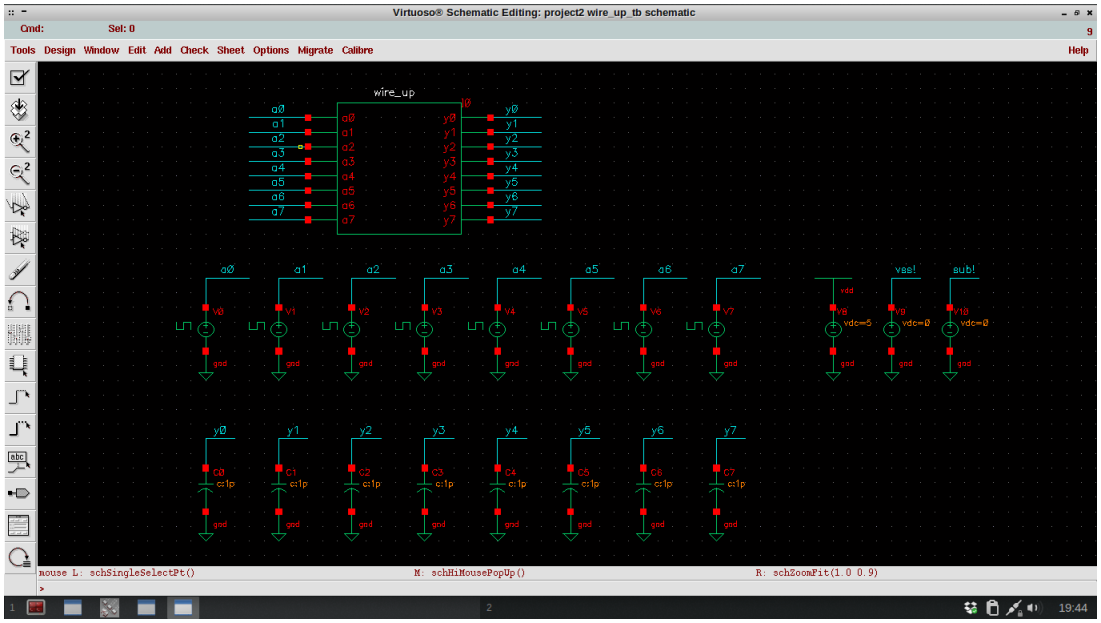
Project 2 part 2-Schematic and Simulation

Wangqing Shen
Qianzi Yan
Xiwei Zhang
11/16/2015

1. Total schematic of 8-inupts-reponser:



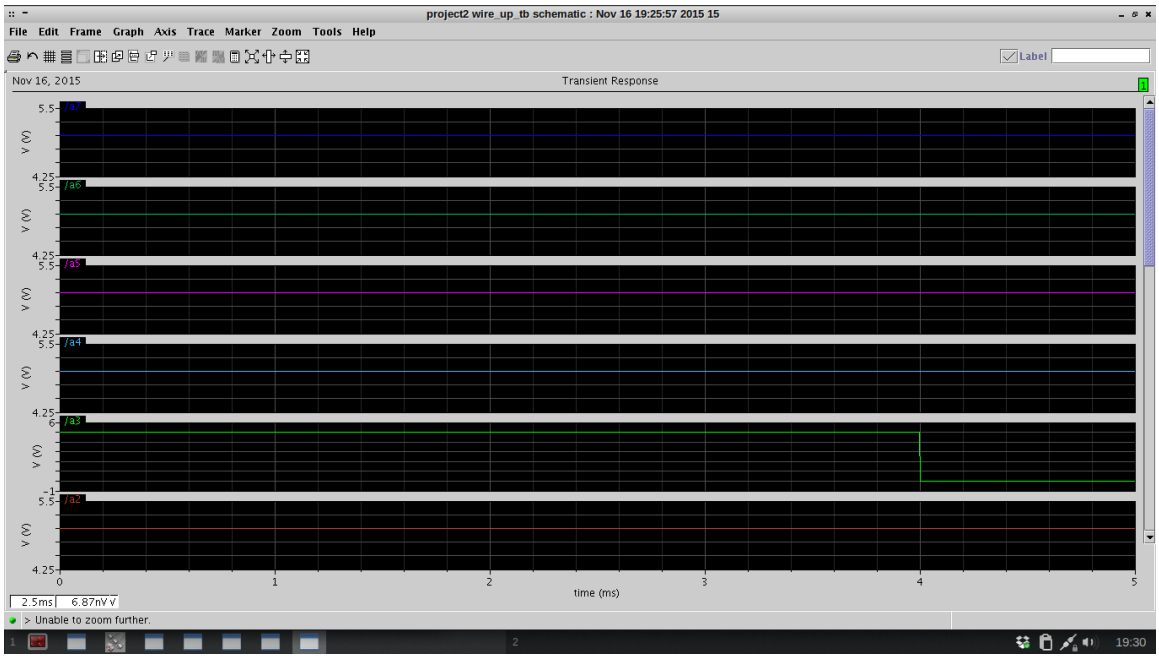
2. Total test schematic for 8-inupts-reponser:

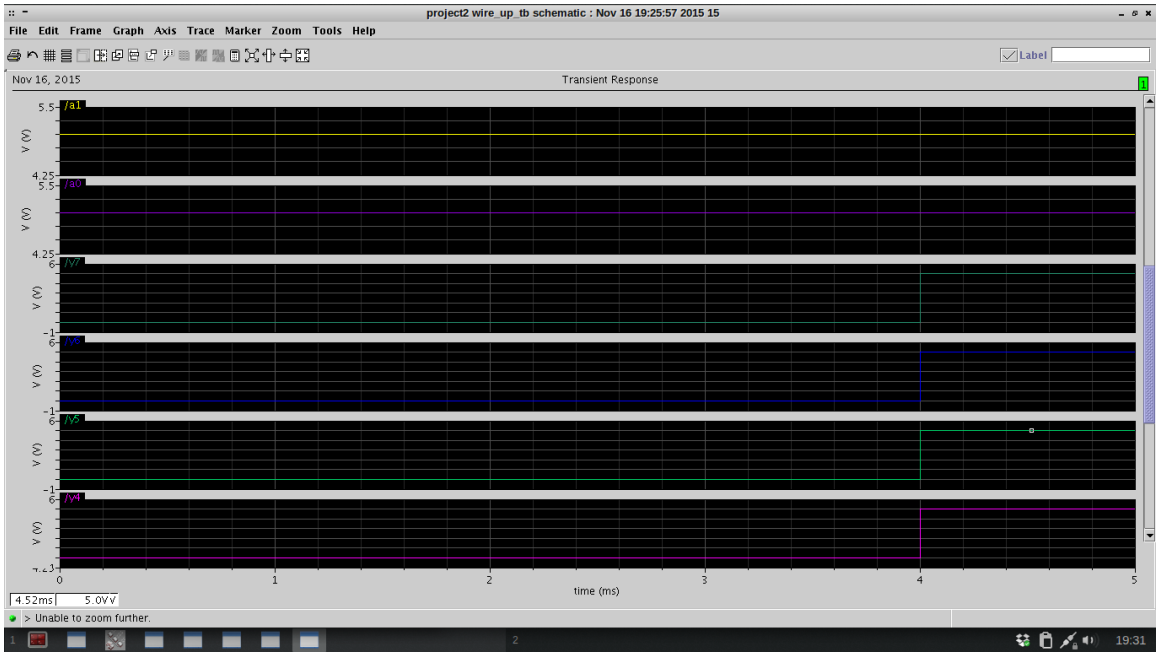


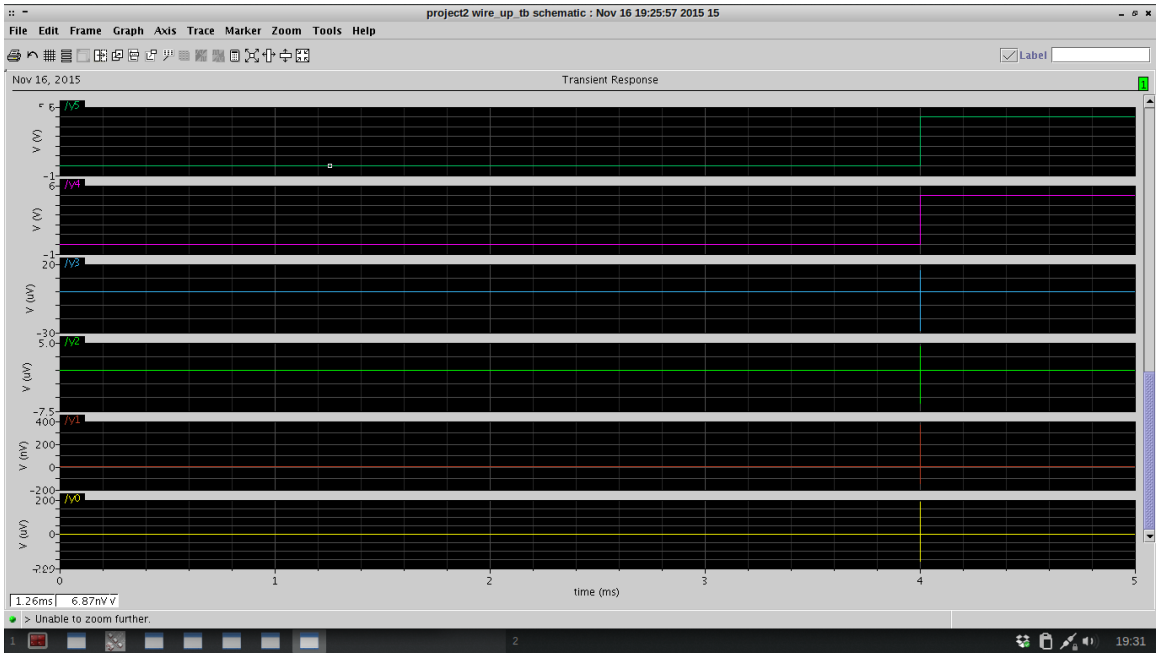
3. The simulation of schematic:

For example:

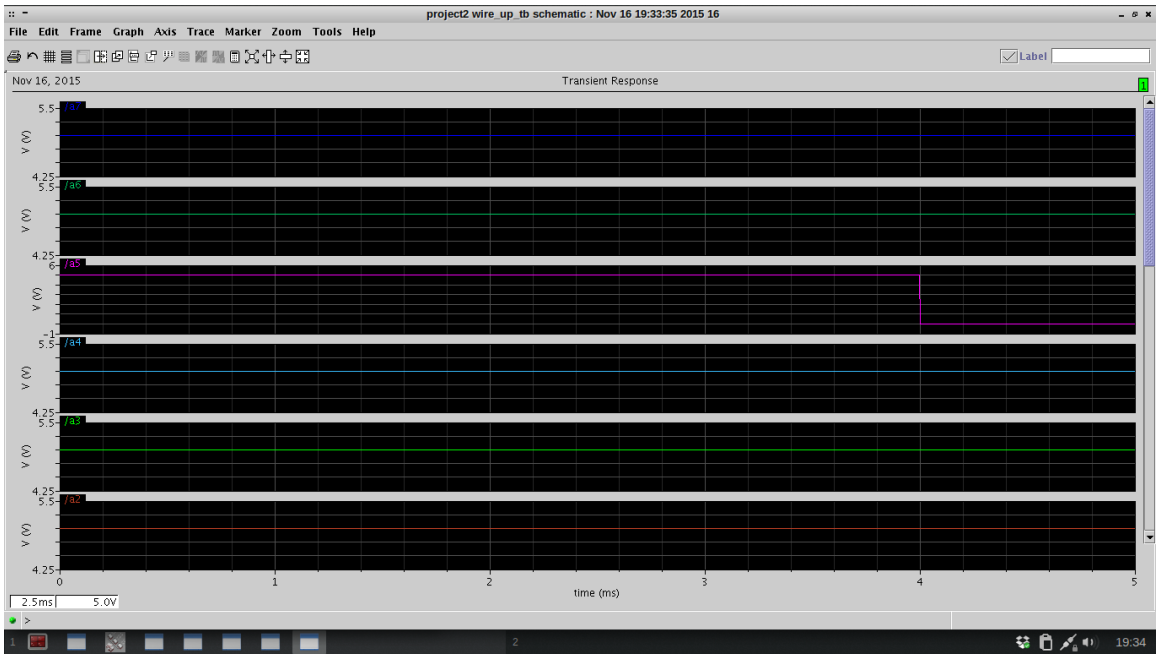
(1) If a3=0, then four bulks will be lighted.

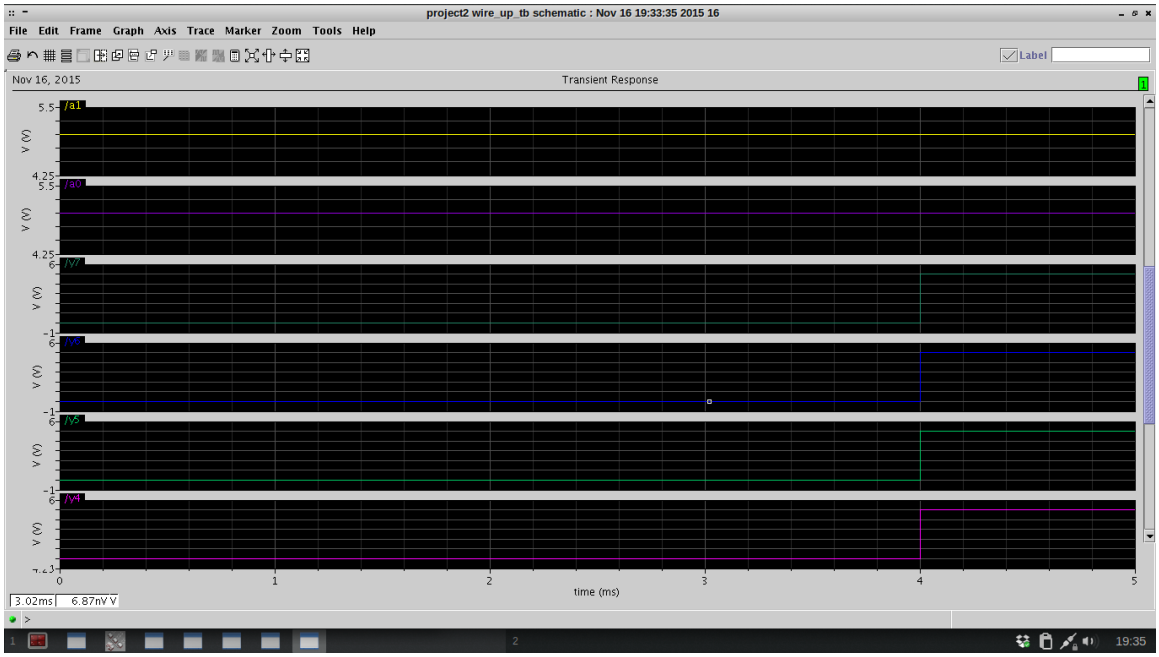


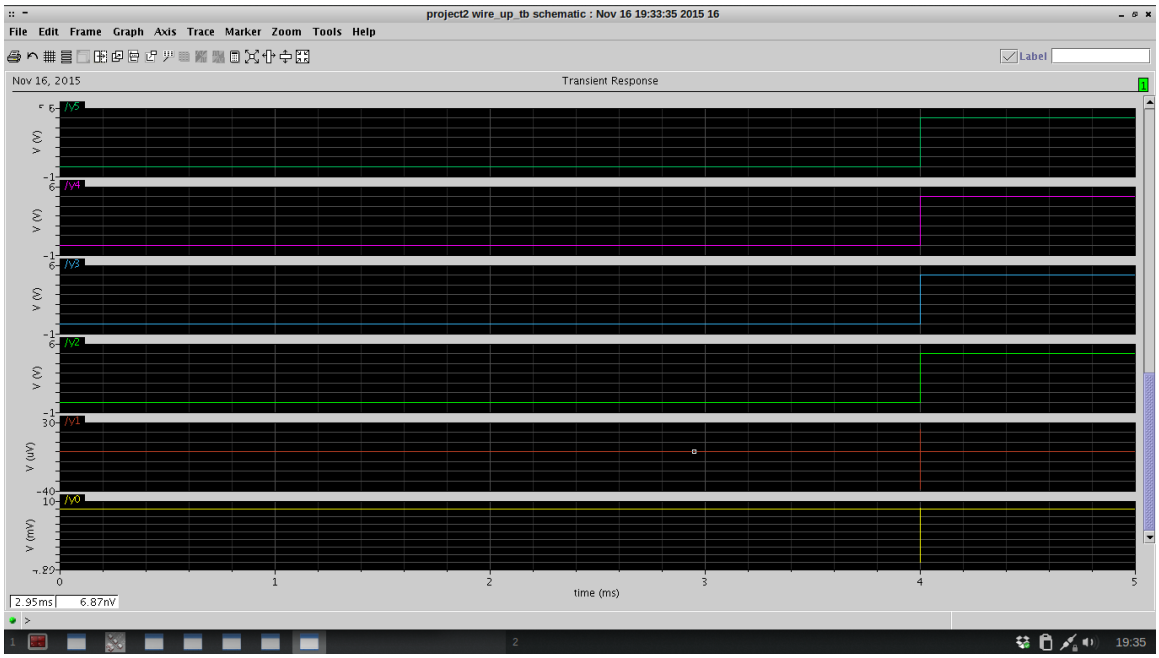




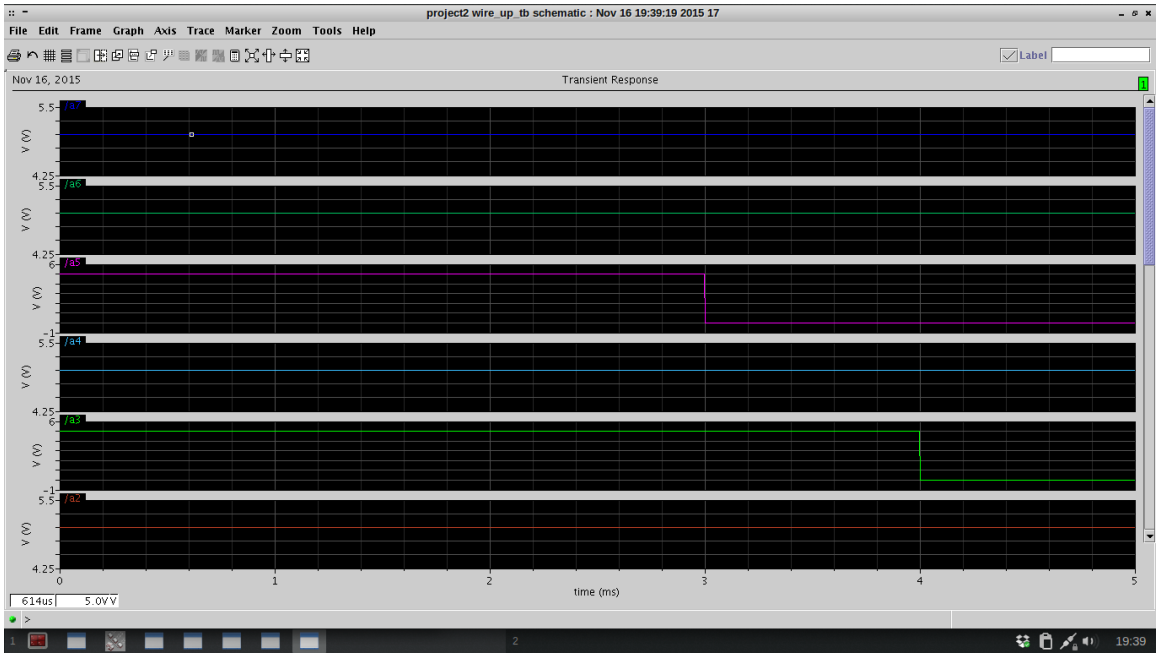
(2) If a5=0, then six bulks will be lighted.

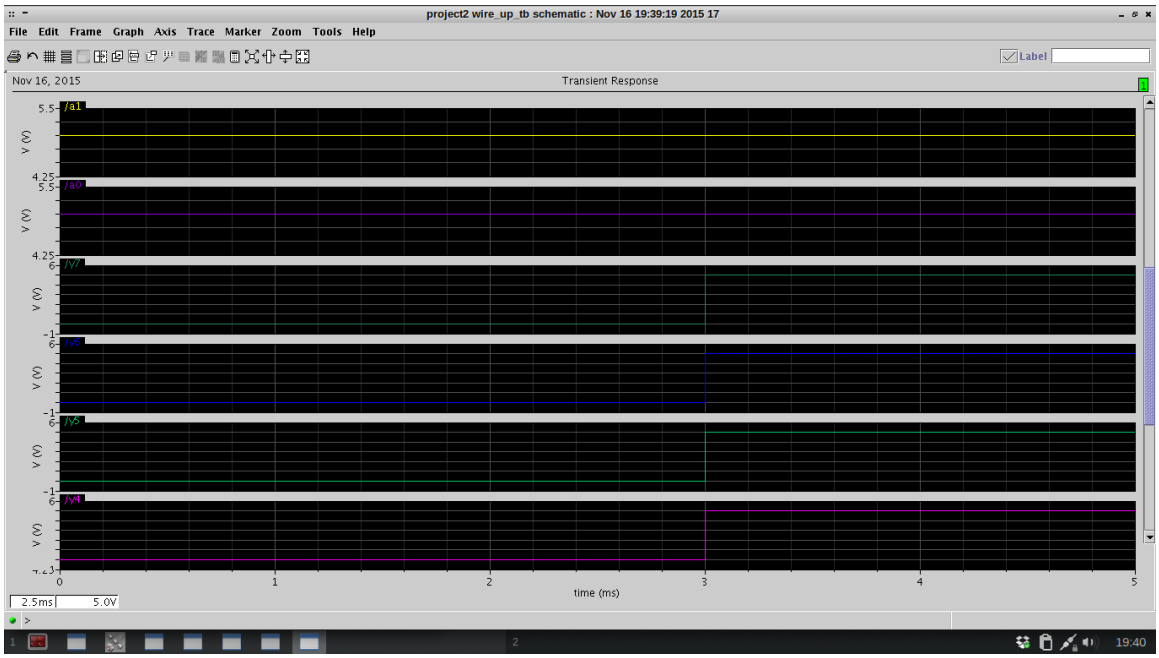


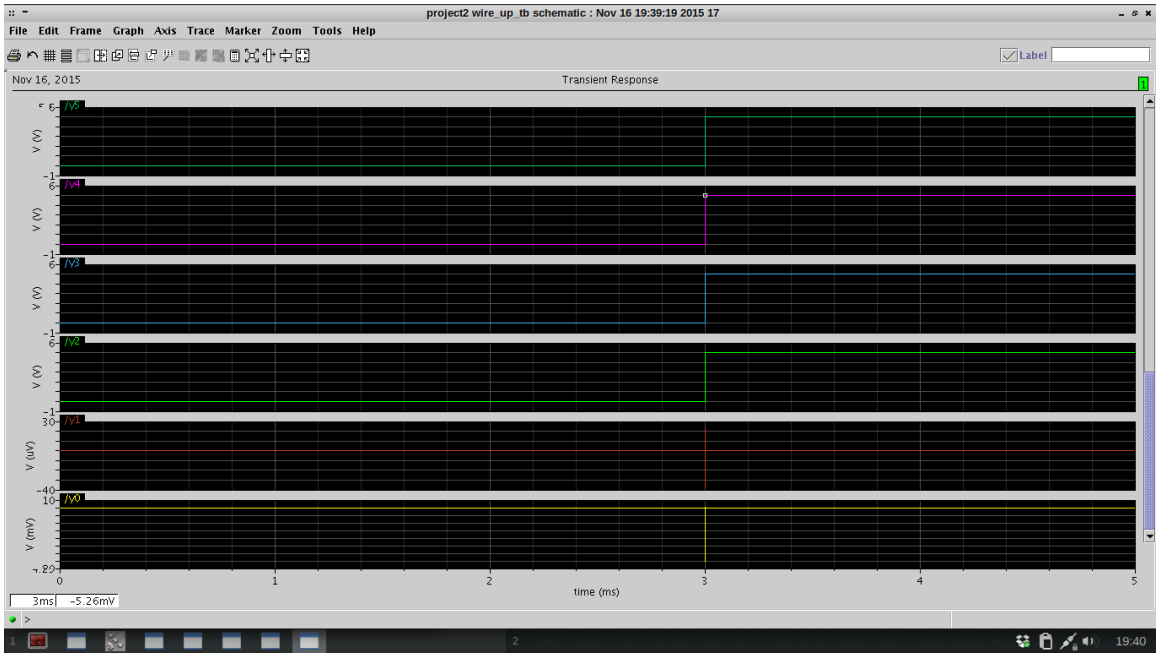




(3)We also simulated the situation that there were two voters and recognized the faster one.


project2 wire_up_tb schematic : Nov 16 19:39:19 2015 17
File Edit Frame Graph Axis Trace Marker Zoom Tools Help
Label
Nov 16, 2015
Transient Response
/a7
/a6
/a5
/a4
/a3
/a2
5.5
4.25
6
-1
0
1
2
3
4
5
time (ms)
614us
5.0V V
19:39

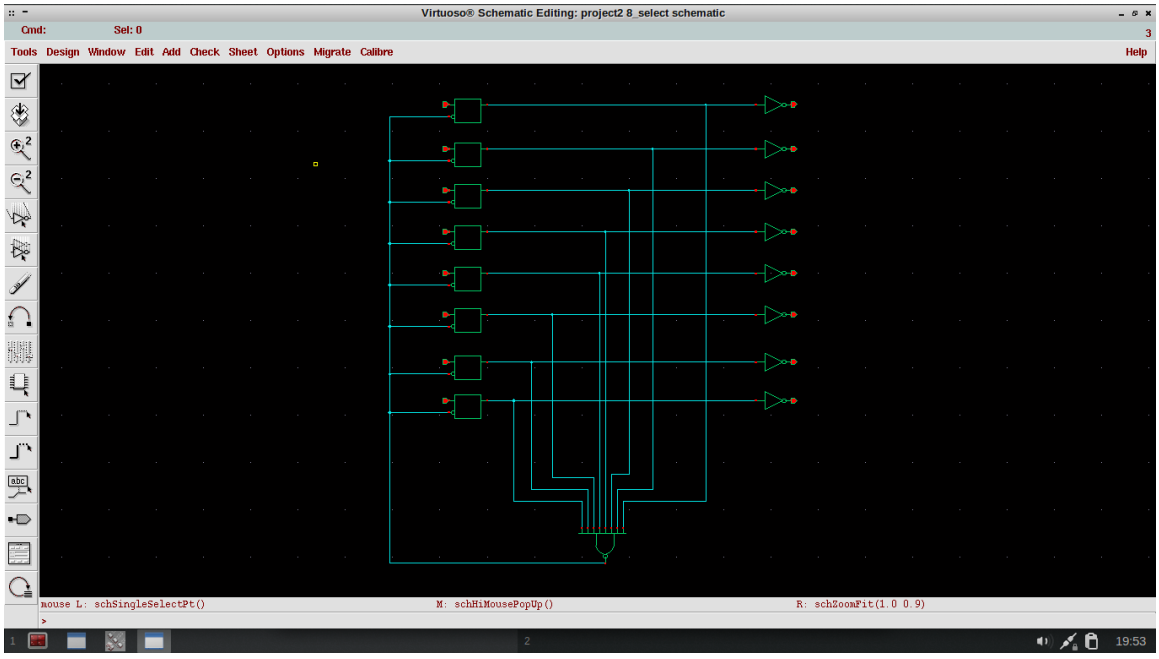

project2 wire_up_tb schematic : Nov 16 19:39:19 2015 17
File Edit Frame Graph Axis Trace Marker Zoom Tools Help
Label
Nov 16, 2015
Transient Response
/a1
/a0
/y7
/y6
/y5
/y4
5.5
4.25
6
-1
0
1
2
3
4
5
time (ms)
2.5ms
5.0V
19:40

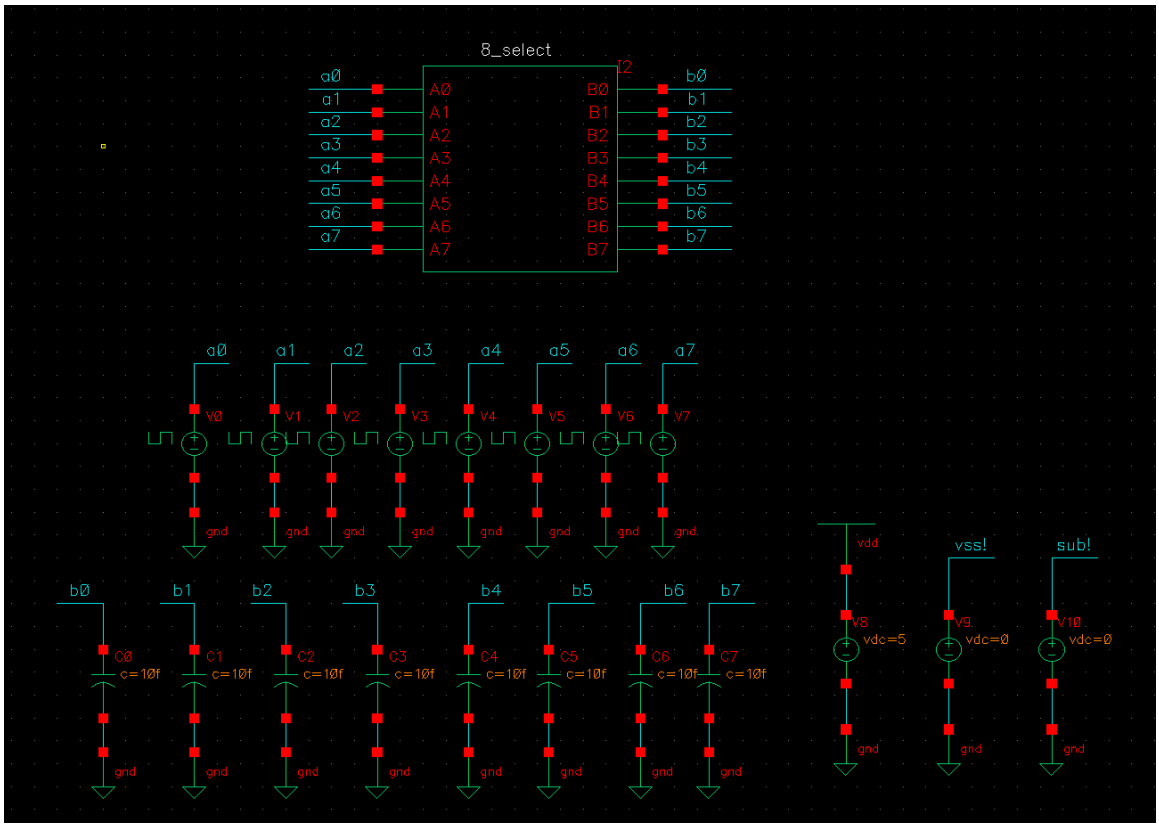


4. The following are schematics and simulations of each part:

(i) The 1st part:

Schematic:



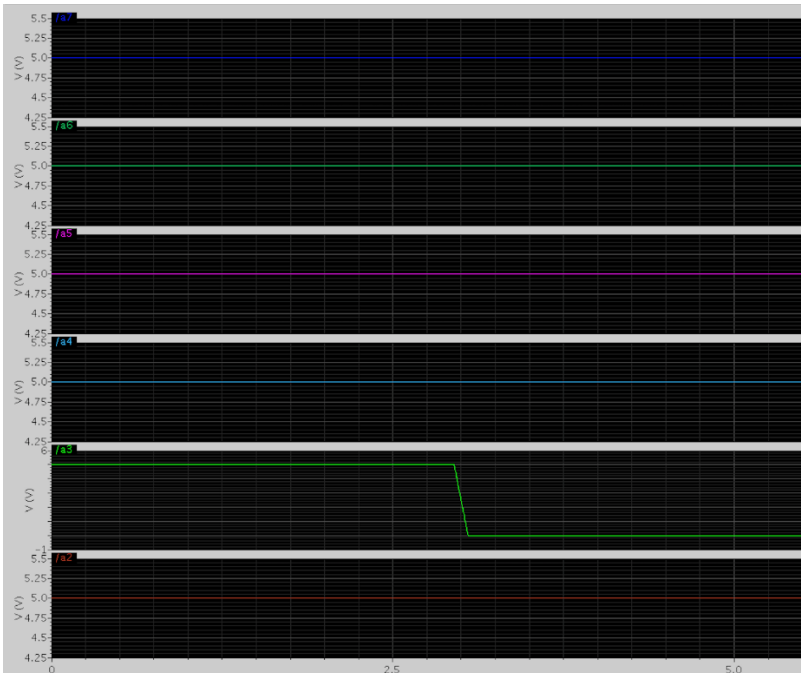


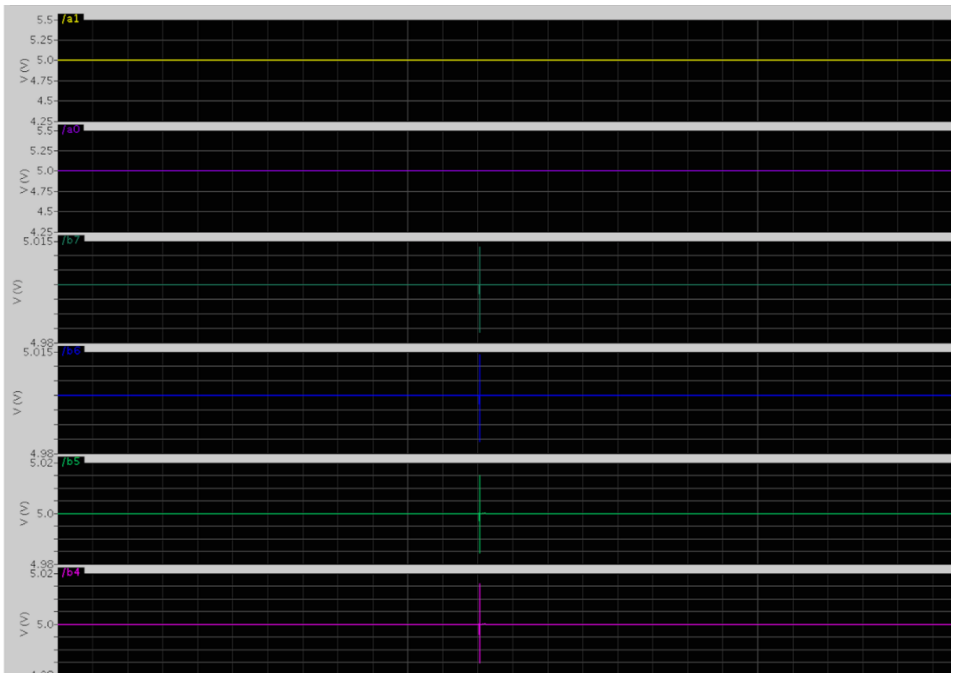
Simulation:

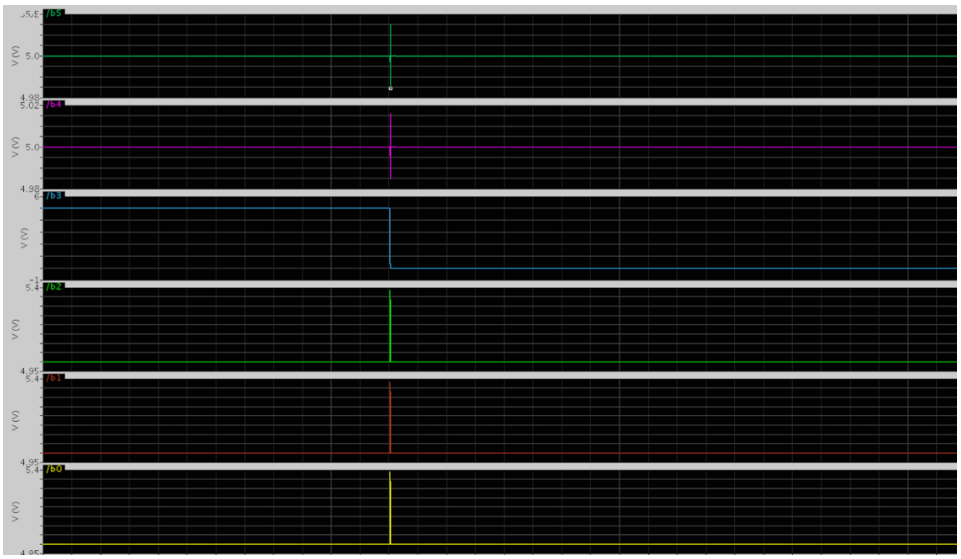
(1) We've simulated some possible situations:

For example:

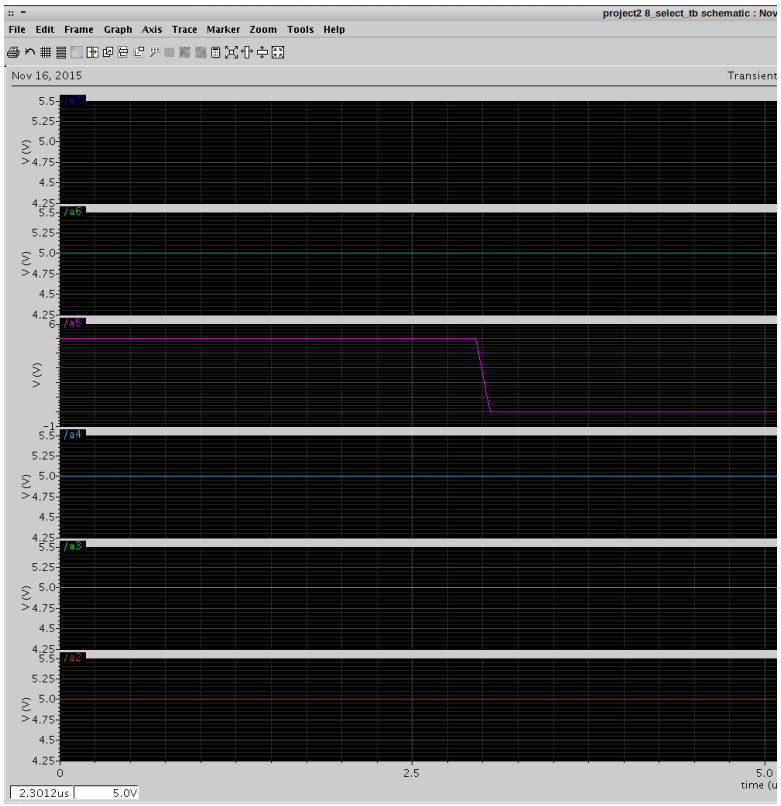
① No.4 is the fastest.

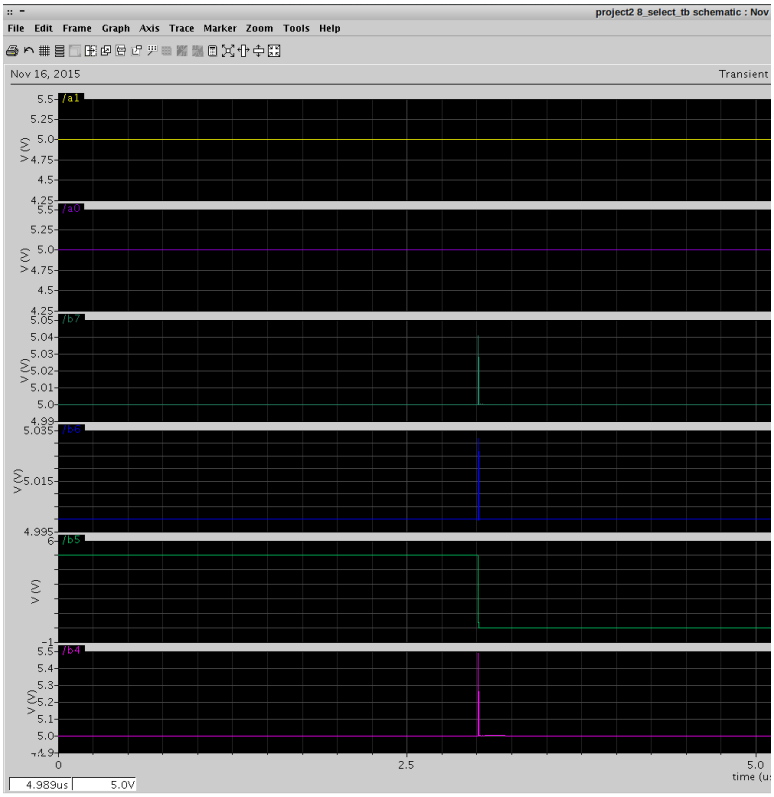


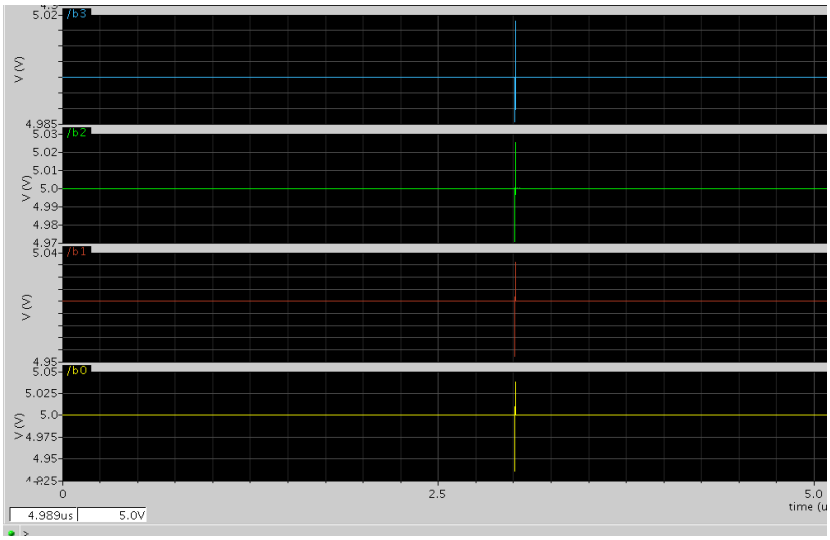

/a1
/a0
/b7
/b6
/b5
/b4
V (V)


/b3
/b4
/b3
/b2
/b1
/b0
V (V)

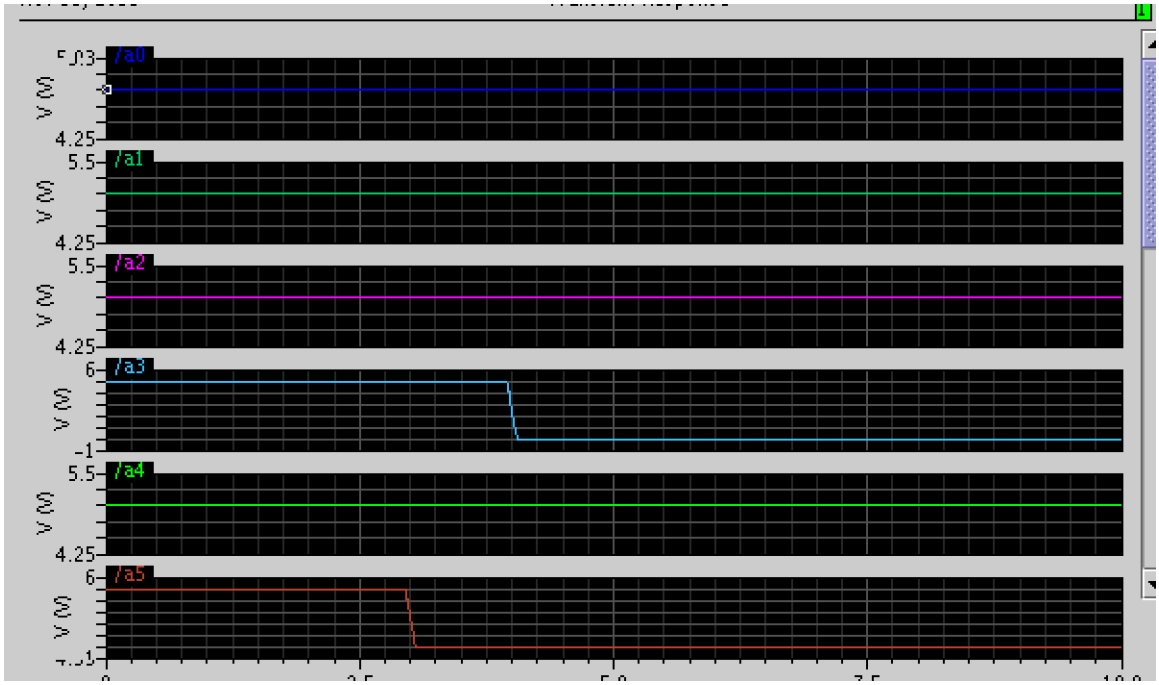
② No.6 is the fastest.

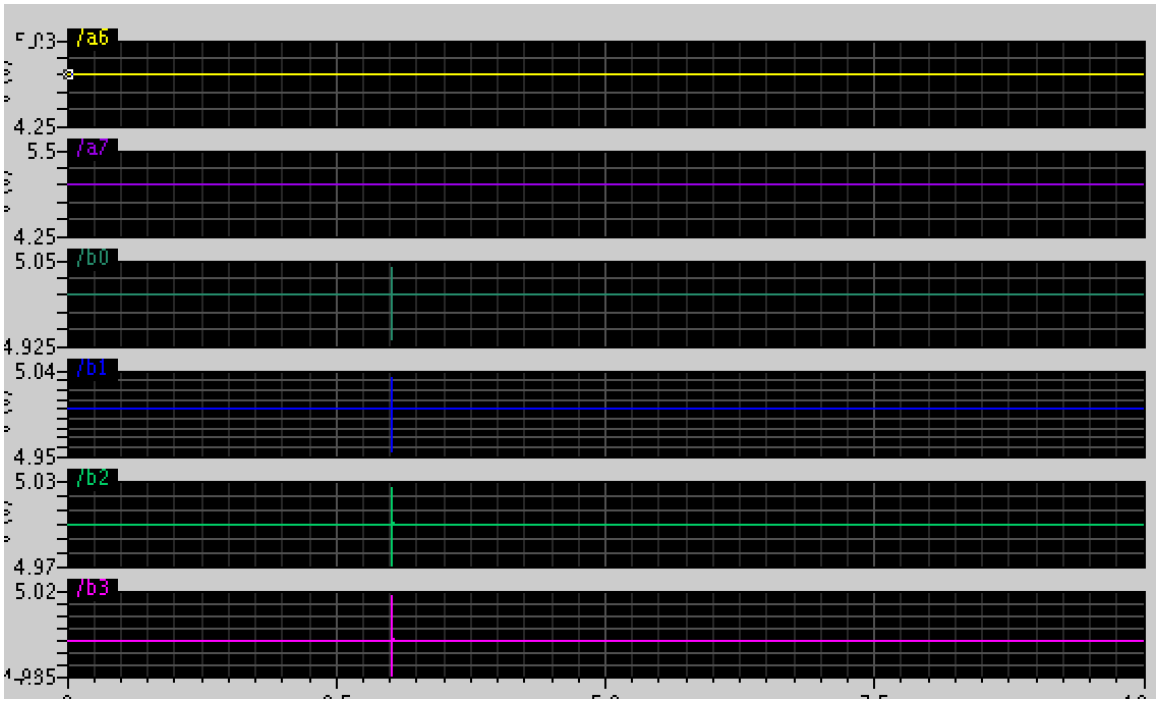


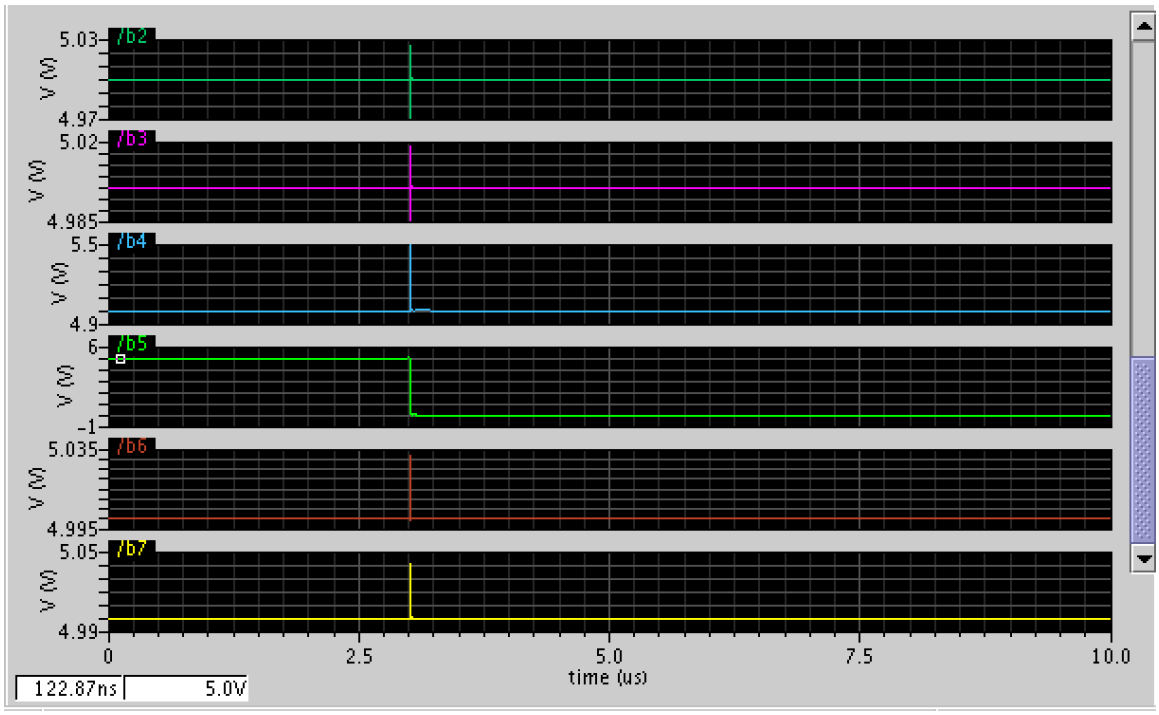




(2) Simulated with two inputs and the fastest signal can lock the D-latch, thus the following signal won't have an effect on the output:

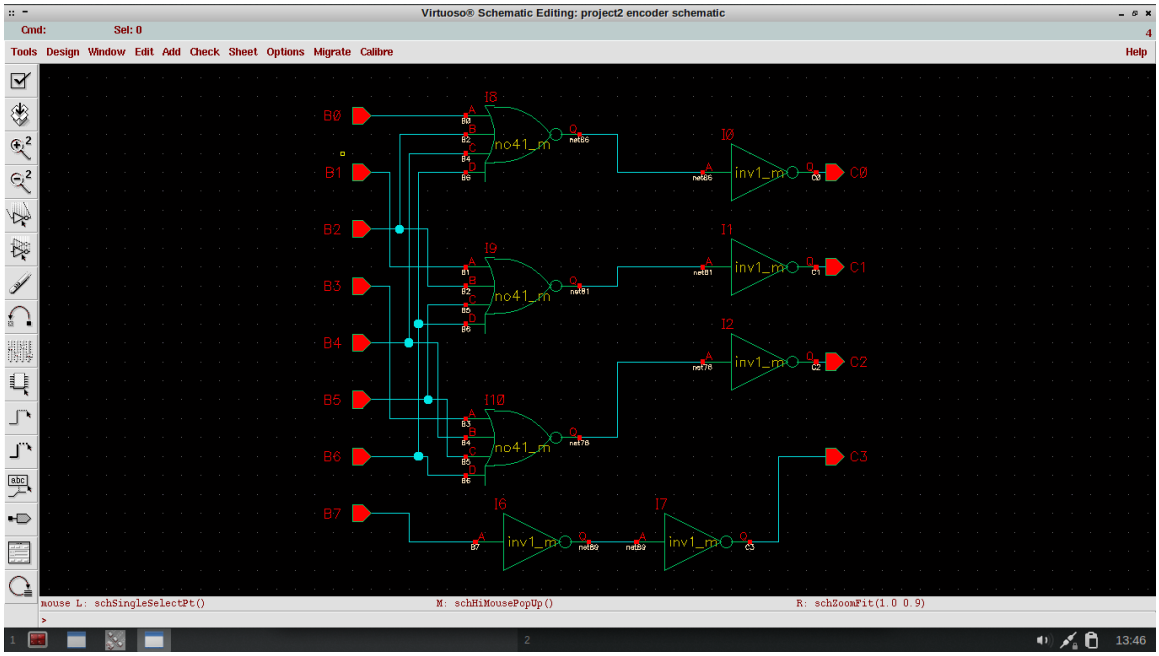


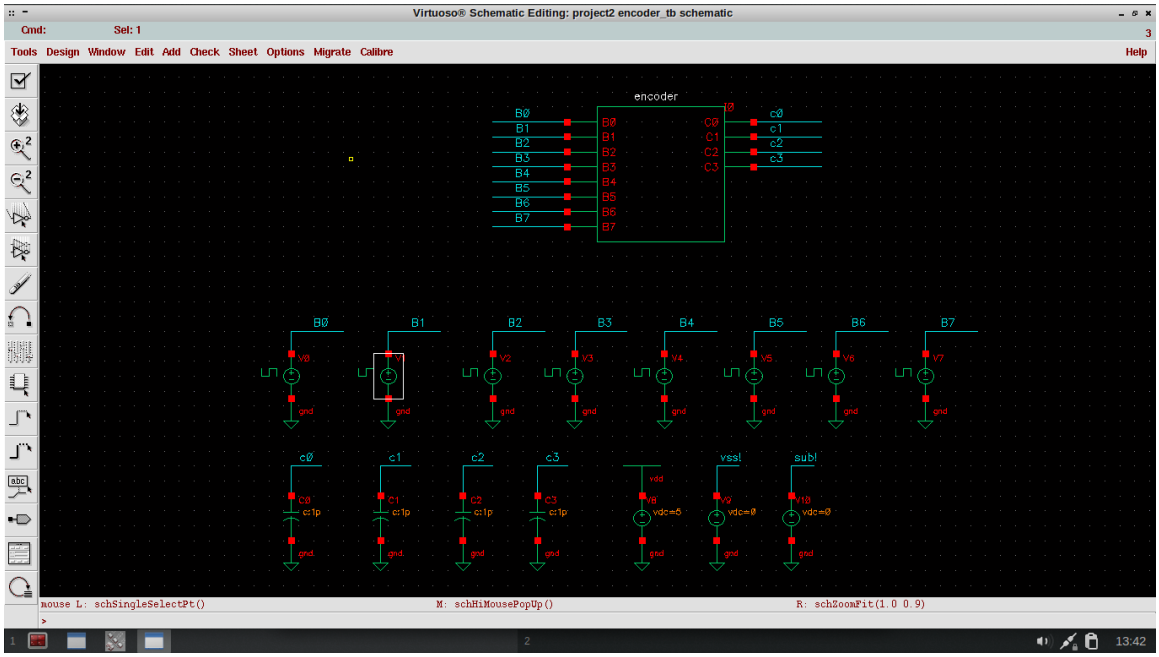

/a6
/a7
/b0
/b1
/b2
/b3


/b2
/b3
/b4
/b5
/b6
/b7
V (V)
0
2.5
5.0
7.5
10.0
time (us)
122.87ns
5.0V

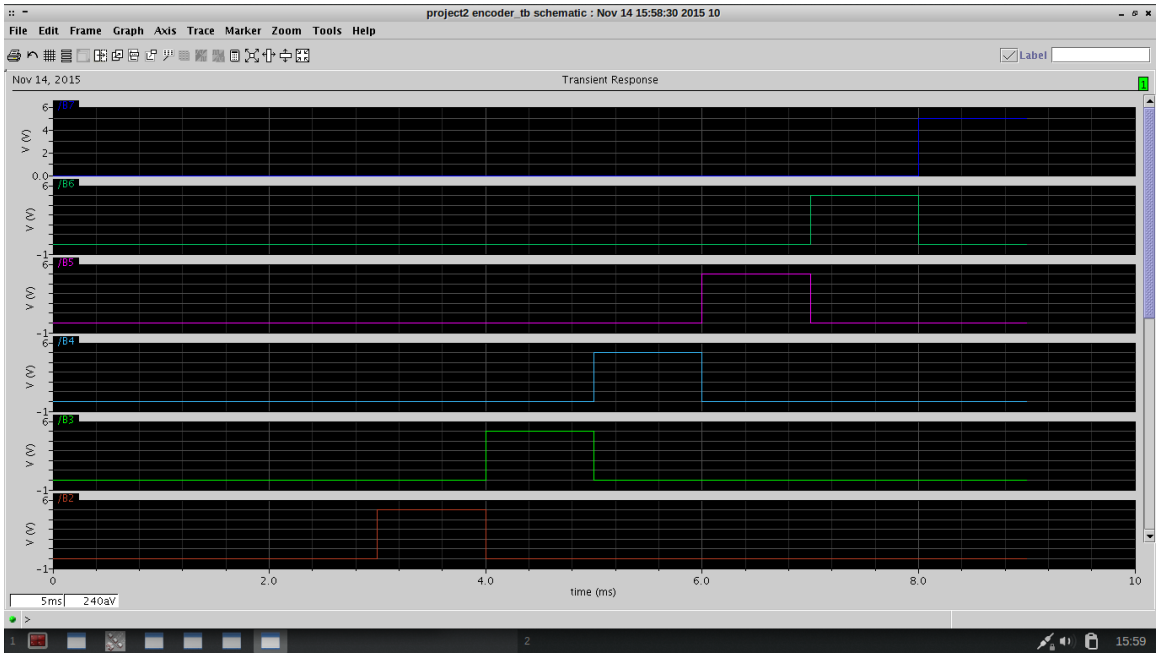
(ii)The 2nd part:

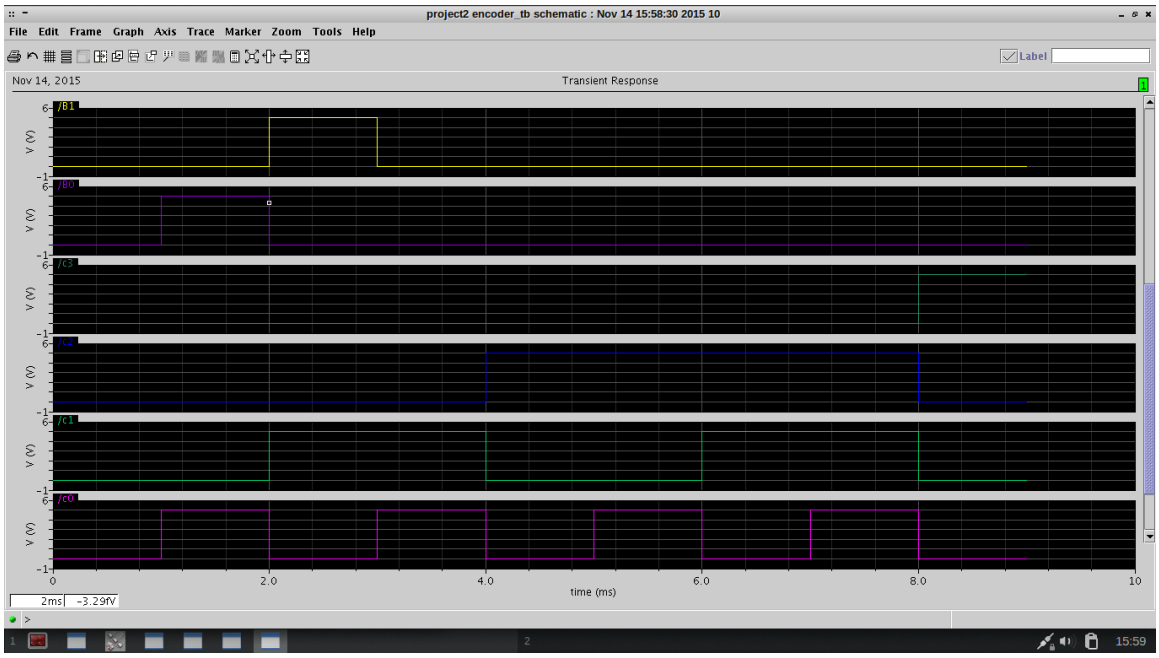
Schematic:





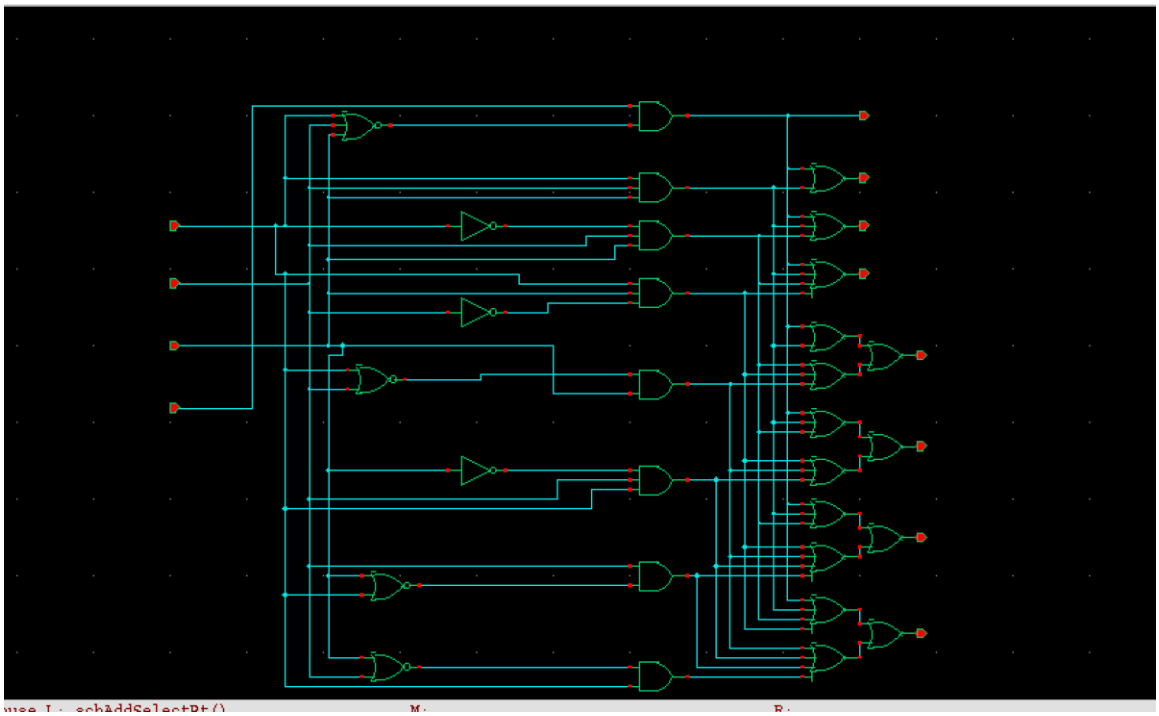
Simulation:

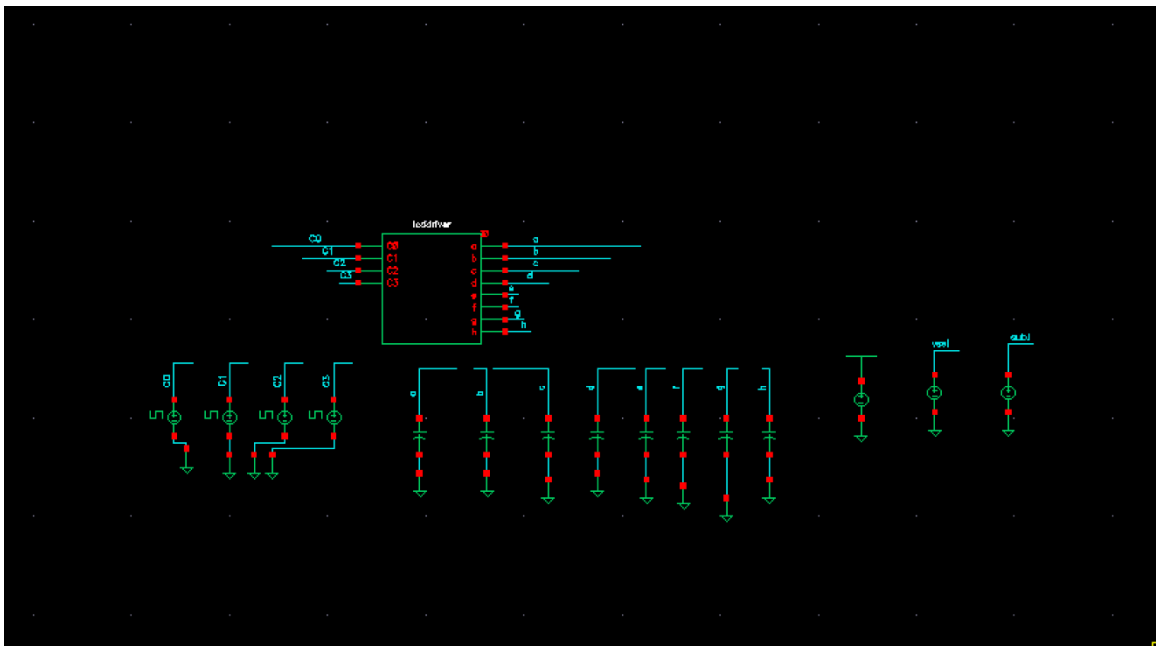

project2 encoder_tb schematic : Nov 14 15:58:30 2015 10
File Edit Frame Graph Axis Trace Marker Zoom Tools Help
Label
Nov 14, 2015
Transient Response
/B7
/B6
/B5
/B4
/B3
/B2
V (V)
0
2.0
4.0
6.0
8.0
10
time (ms)
5ms 240aV
15:59


project2 encoder_tb schematic : Nov 14 15:58:30 2015 10
File Edit Frame Graph Axis Trace Marker Zoom Tools Help
Label
Nov 14, 2015
Transient Response
/B1
/B0
/C3
/C2
/C1
/C0
V (V)
0
2.0
4.0
6.0
8.0
10
time (ms)
2ms -3.29fV
15:59

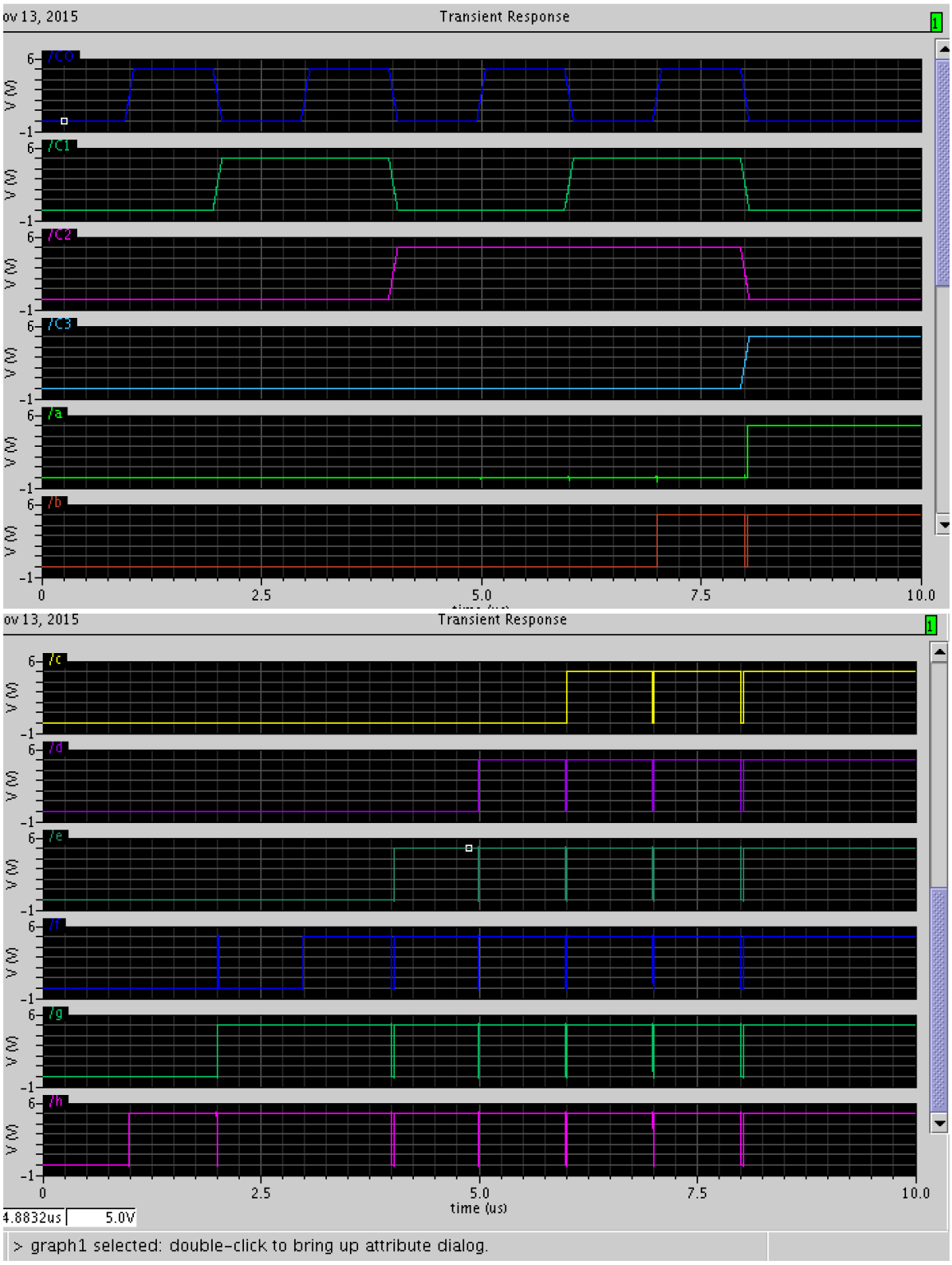
(iii)The 3rd part:

Schematic:





Simulation:



The simulation of the 2nd part and the 3rd part fit the truth table, thus these two parts are logically correct.