

Saleae Logic 4 USB Logic Analyzer

FEATURES

- Powerful, Easy-to-use Software
- Deep Sample Buffers
- Highly Portable, USB Attached
- 24 Included Protocol Analyzers
- Automation API
- Custom Protocol Decoder Plugin API
- Edge and Pulse Width Triggering
- Protocol Result Filter and Search
- Measurements, Bookmarks and Timing Markers
- Four Data Export Formats: CSV, Binary, VCD and MATLAB
- Cross Platform Windows, Linux, and OSX

APPLICATIONS

- Firmware Debugging
- FPGA Debugging
- Functional Verification
- Performance Profiling
- Reverse Engineering
- Protocol Decoding
- Data Logging

KEY SPECIFICATIONS

- Four Digital Channels
- 12 MSPS Digital Sampling
- 3 MHz Max Digital Bandwidth
- One Analog Channel
- 6 MSPS Analog Sampling
- 1 MHz Analog Bandwidth
- Recording Length Limited by Available RAM and Density of Recorded Data
- RGB LED, Customizable 24 bit Color

DESCRIPTION

The Saleae Logic 4 USB Logic Analyzer is a 4 channel logic analyzer with one input dual purposed as a single channel analog data recorder. The device connects to a PC over USB and uses the Saleae Logic Software to record and view digital and analog signals.

A logic analyzer is a debugging tool used to record and view digital signals. It operates by sampling a digital input connected to a device under test (DUT) at a high sample rate. These samples are recorded to a sample buffer, and at the end of the capture, the buffer is displayed in the software for review.

Logic analyzers are great for debugging embedded applications. In the most common case, a developer working on firmware for a microcontroller will write code to communicate with another component, possibly using protocols like serial, I2C, or SPI. To verify the functionality or to diagnose errors in the firmware, a logic analyzer is connected to the digital IO used for communication and records the activity during testing. The recording is then shown on the display so the user can view the actual behavior of the firmware, and compare that with the expected behavior to narrow down and identify the source of the issue – or verify that the operation is correct.

INCLUDED COMPONENTS

Saleae Logic 4 USB Logic Analyzer, 4 Channel Wire Harness, 8 Micro-Gripper Hooks, Saleae Carrying Case, USB 2.0 cable, and a Getting Started Guide



www.saleae.com

PIN CONFIGURATION

Channel 0 [Digital + Analog]	Channel 1 [Digital Only]	Channel 2 [Digital Only]	Channel 3 [Digital Only]
Ground	Ground	Ground	Ground

ABSOLUTE MAXIMUM RATINGS

Input Voltage-25.00V to +25.00V

Operating Temperature0°C to +70°C

OPERATING RATINGS

Input Voltage+0.00V to +5.00V

Temperature0°C to +70°C

ELECTRICAL CHARACTERISTICS

Input Impedance	1 MΩ 10 pF
Digital Sampling Rates	12 MSPS, 6* MSPS, 3* MSPS, 1* MSPS
Analog Sample Rates	6 MSPS, 125* KSPS, 5* KSPS, 1* KSPS, 100* SPS, 10* SPS
Digital Logic Threshold	V _{IL} +0.8V, V _{IH} +2.0V
Common Supported Logic Standards	+5.0V, +3.3V, +2.5V, RS-232, RS-485/RS-422, +12V
Digital Bandwidth	3 MHz
Analog Bandwidth (-3db)	600 kHz**
ADC Number of Bits	8
Analog Input Voltage Range	+0.0V to +5.0V
Analog Volts per LSB	19.5mV
PC Connection	USB 2.0 High Speed
Internal Sampling Clock Error (Digital)	±0.005%***

Notes:

*Planned sample rates. Only 12 MSPS digital + 6 MSPS analog currently supported.

**Bandwidth when sampling at 6 MSPS.

*** For the total pulse-width error, refer to our Time Measurement Error support article here:

<https://support.saleae.com/faq/technical-faq/time-measurement-error>



www.saleae.com

APPLICATION INFORMATION

The Saleae Logic Software user guide can be located on the Saleae support site:

<https://support.saleae.com/user-guide>

System Requirements

Supported Operating Systems: Windows XP (x32), Windows Vista (x32/x64), Windows 7 (x32/x64), Windows 8 (x32/x64), Windows 8.1 (x32/x64), OSX 10.7+, Ubuntu Linux 12.04.2+ (x32/x64)

USB 2.0 high speed ports are required.

The Saleae Logic Software can be downloaded from the Saleae website:

<https://www.saleae.com/downloads>

Sample Buffer Limit

The maximum recording length is determined by the density of activity in the recorded signal, the amount of free memory available to the Logic software, and the exact settings of the capture. More information, as well as recommendations, can be found on the Saleae support site:

<https://support.saleae.com/faq/technical-faq/how-long-can-i-record-data>

Bandwidth vs Sample Rate

In order to accurately record a signal, the sample rate must be sufficiently higher in order to preserve the information in the signal, as detailed in the Nyquist–Shannon sampling theorem. Digital signals must be sampled at least four times faster than the highest frequency component in the signal. Analog signals need to be sampled ten times faster than the fastest frequency component in the signal.



www.saleae.com

CONSIDERATIONS

Many additional considerations and suggestions can be found in the Saleae support material on the website:

<http://support.saleae.com>

Ground Loops

Ground loops introduce risk of damage to the equipment. To mitigate the risk of damage, follow the precautions outlined on the Saleae website:

<https://support.saleae.com/user-guide/safety-and-warranty>

Over Voltage Protection

The input pins on the new Saleae Logic devices (Logic 4, Logic 8, Logic Pro 8 and Logic Pro 16) have protection for signals within -25.00V to +25.00V for continuous operation. The device can be safely used for normal operation with signals in this range. The analog input on Logic 4 and Logic 8 is limited to +0V to +5V, and will saturate (take on minimum or maximum value) outside of this range. Logic Pro 8 and Logic Pro 16 have an analog input limited to -10V to +10V, and will saturate outside of that range.

Differential Signals

Each digital input is single ended only. It is recommended to use a differential to single ended receiver to first convert a differential signal to single ended before attempting to record. This is not always necessary. Details can be found on the Saleae support site:

<https://support.saleae.com/protocol-analyzers/analyzer-user-guides/decode-differential-and-high-voltage-data>