6872 Foundations of Electronics

Lecture 9: Field Effect Transistor (FET)

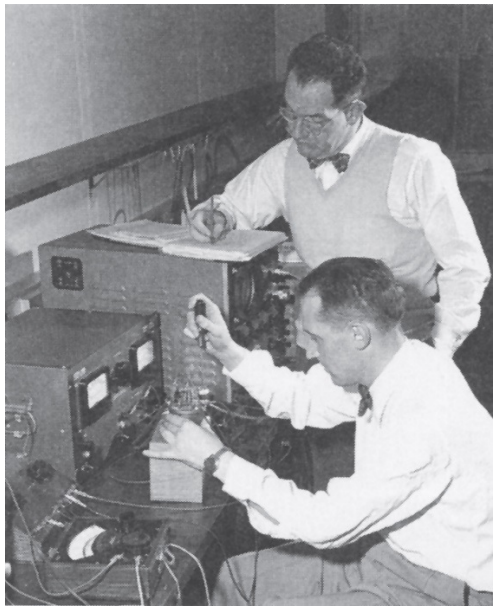
Elvio J. Leonardo

Bachelor Degree in Computer Science
Department of Informatics
State University of Maringa

v. 2020

Abstract

- JFET: Basic Construction and Operation
- MOSFET: Basic Construction and Operation
- Biasing Circuits
  - Fixed-Bias
  - Self-Bias
  - Voltage-Divider Bias



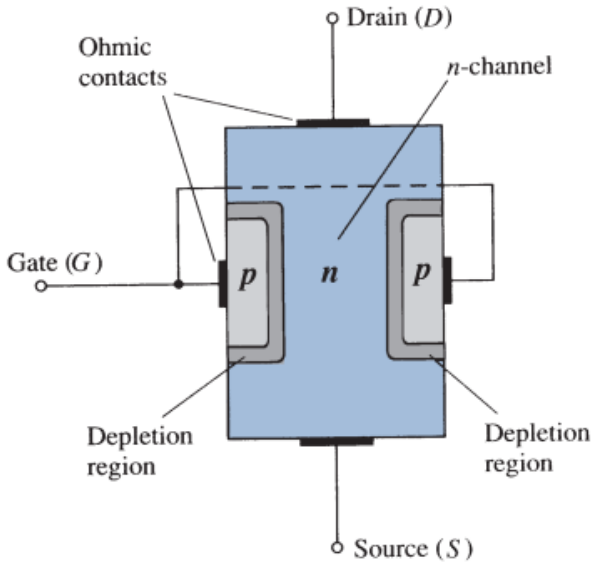
Ian M. Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a field-effect transistor in 1955.

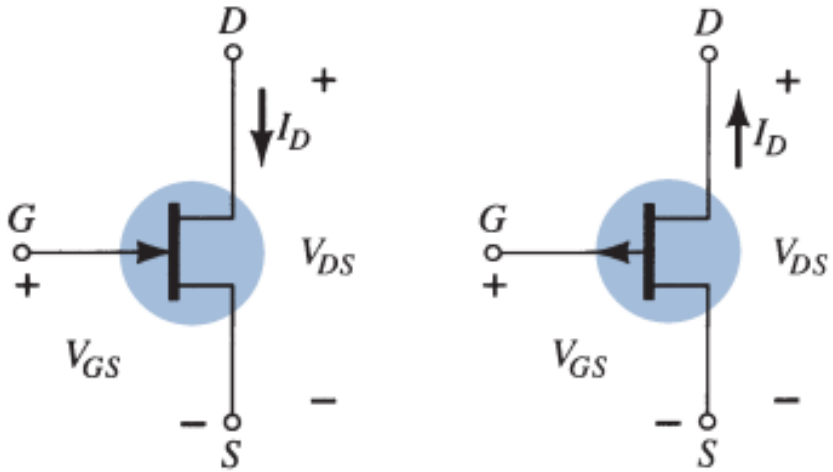
FET and BJT

- Field-Effect Transistor (FET) is a three-terminal device with use similar to the BJT
- Primary differences between FET and BJT
  - BJT is a current-controlled device (controlled by I_B)
    FET is a voltage-controlled device (controlled by V_{GS})
  - BJT is a bipolar device: conduction done by electrons and holes)
    FET is a unipolar device: conduction done by either electrons (N-channel device) or holes (P-channel device)
- FET has a very high input impedance ($I_G \approx 0$)
- FETs are more temperature stable than BJTs
- FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chip
- Voltage gain for BJT amplifier is typically greater than for FET amplifiers
- FET types: Junction FET (JFET), and Metal-Oxide-Semiconductor FET (MOSFET) depletion and enhancement types

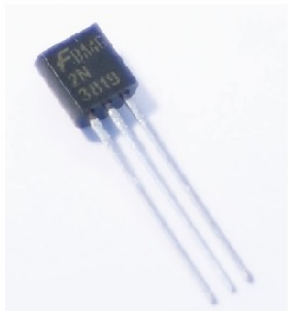
Junction FET Construction

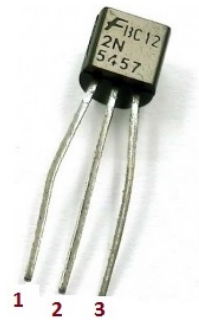
- N-channel JFET (depicted) and P-channel JFET
  - Channel (N-type) connected at each end to drain (D) and source (S) terminals
  - Channel between embedded layers of P-type material
  - P-type layers form gate (G) terminal
- Symbols

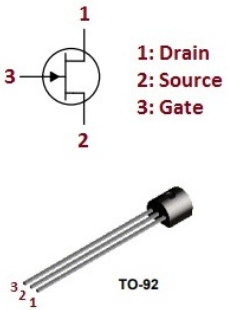




N-channel (left) and P-channel (right) FETs

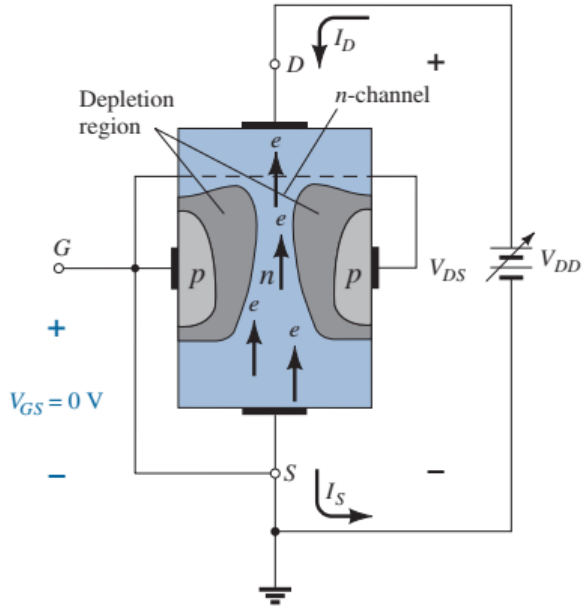


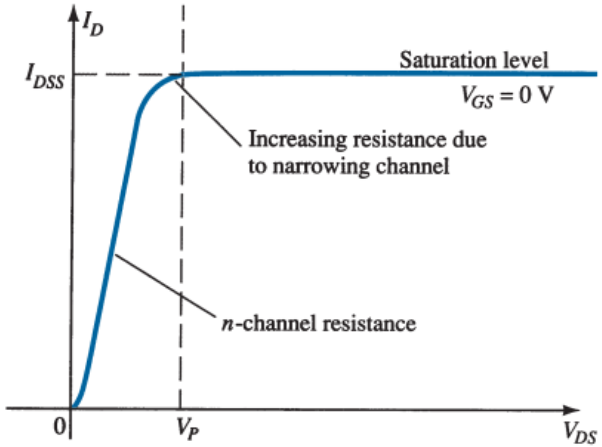


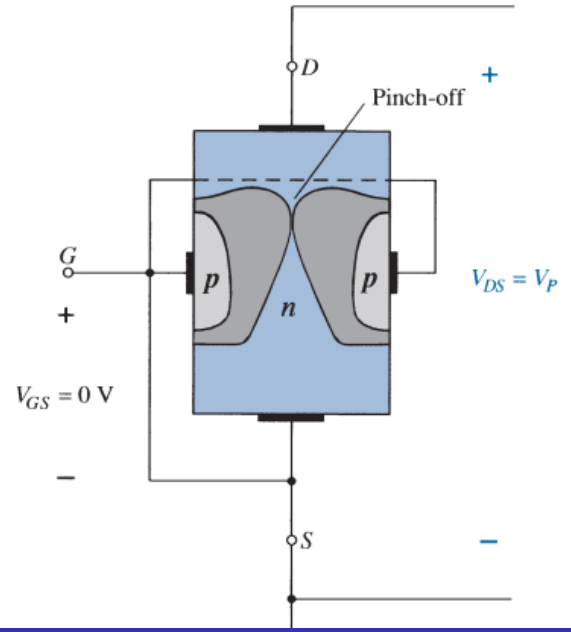


Junction FET Operation

- $V_{GS} = 0$, $V_{DS} > 0$
  - Junction PN is reverse biased and $I_G = 0$
  - Current $I_D = I_S$ flows between drain and source
  - Current is limited solely by the resistance of the N-channel
  - Depletion region is wider closer to drain terminal because of higher positive voltage
  - For $V_{DS} = V_P$, the two depletion zones would touch, a condition known as **pinch-off**
  - With pinch-off, the channel current saturates at $I_D = I_{DSS}$ (for $V_{GS} = 0$)

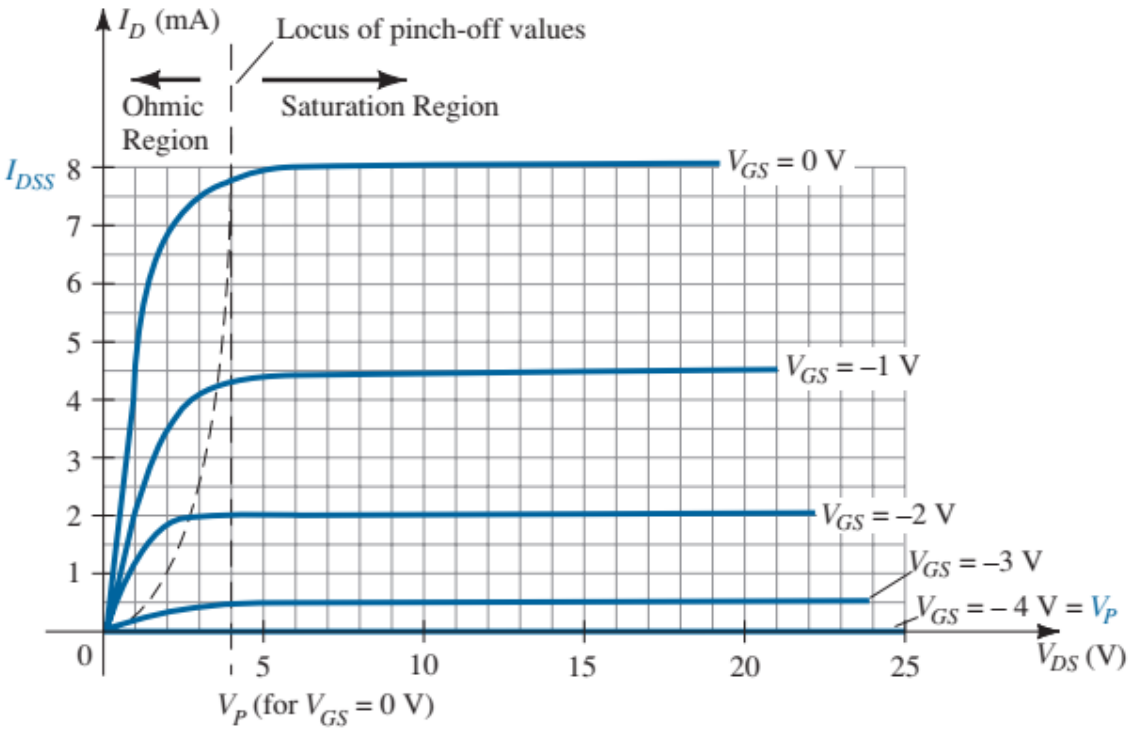


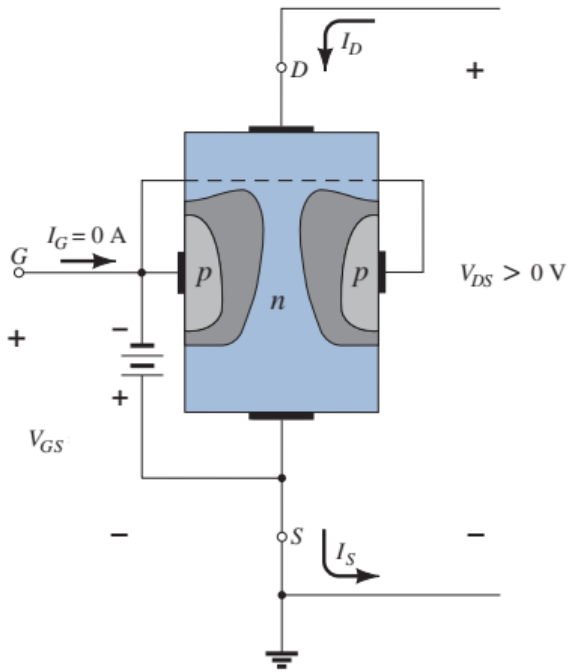




Junction FET Operation

- $V_{GS} < 0$, $V_{DS} > 0$
  - Negative V_{GS} widens depletion region
  - Pinch-off (and saturation current) reached earlier
  - For each value of V_{GS}, there is a curve $V_{DS} \times I_D$
  - JFET characteristics includes **ohmic region** and **saturation region**
  - Note that for $V_{GS} < V_P$, $I_D = 0$





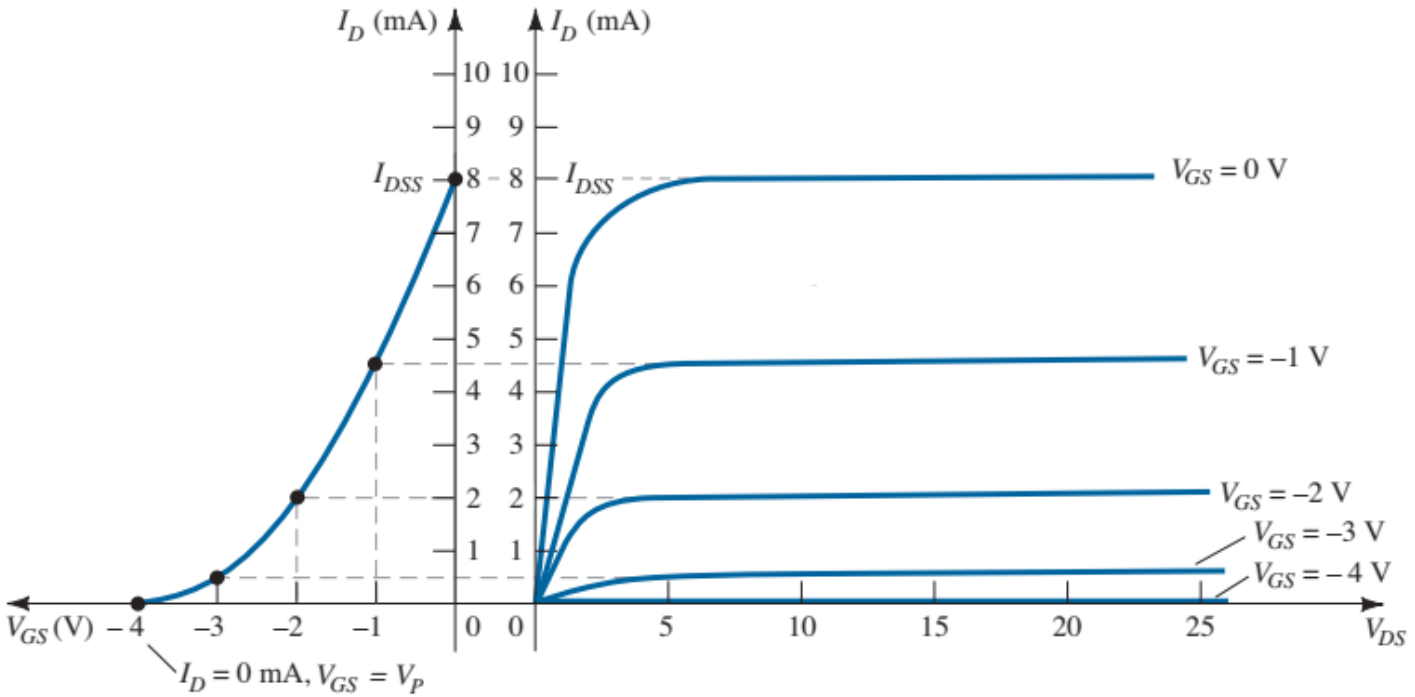
Assuming $I_{DSS} = 8$ mA and $V_P = -4$ V

Junction FET Characteristics

- BJT has a linear relationship between the controlling current (I_B) and the output current I_C: $I_C = \beta I_B$
- For JFET, this relationship is not linear:

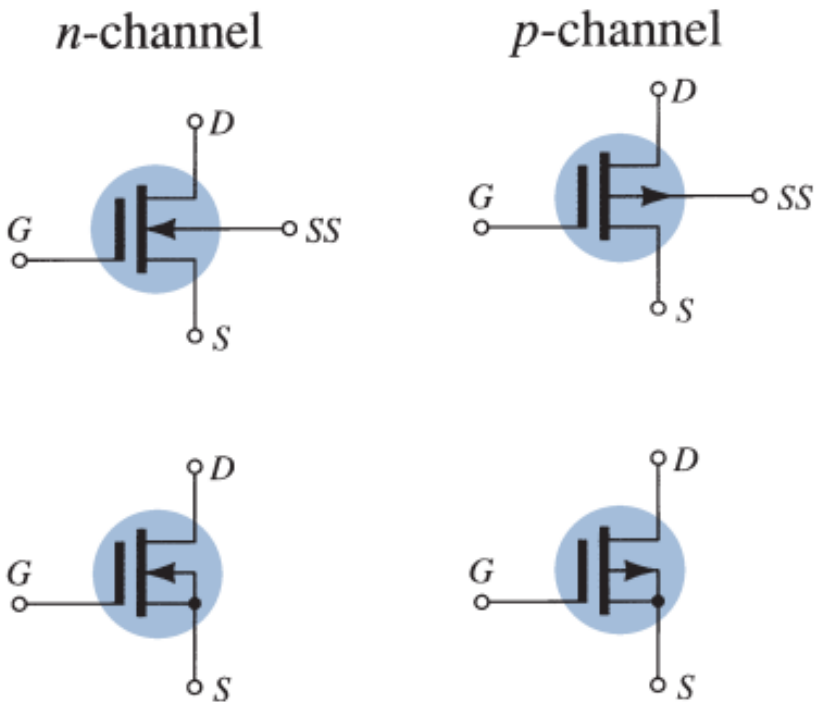
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

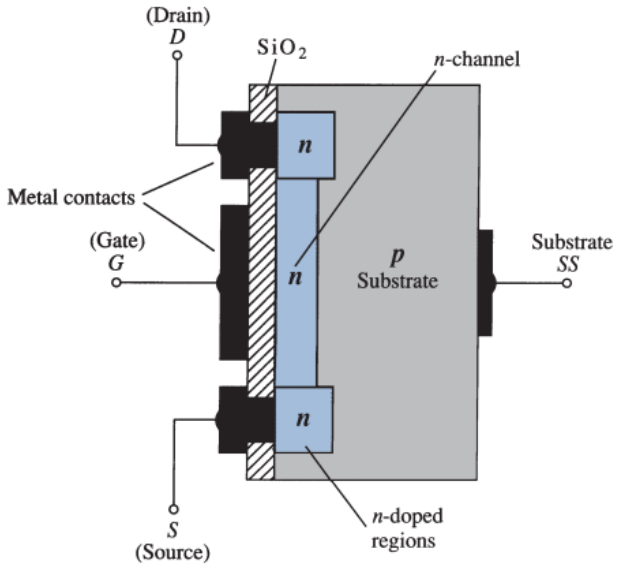
I_{DSS} and V_P are given in datasheet



Depletion MOSFET Construction

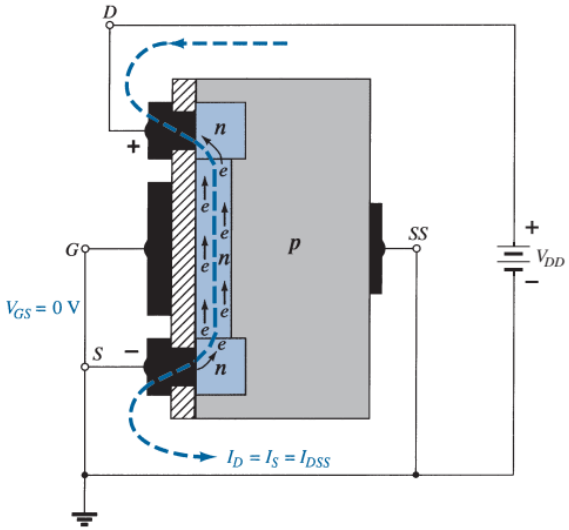
- N-channel (depicted) and P-channel Depletion MOSFET
  - Channel (N-type) connected at each end to drain (D) and source (S) terminals
  - Gate is insulated from N-channel by a very thin silicon dioxide (SiO_2)
- Symbols





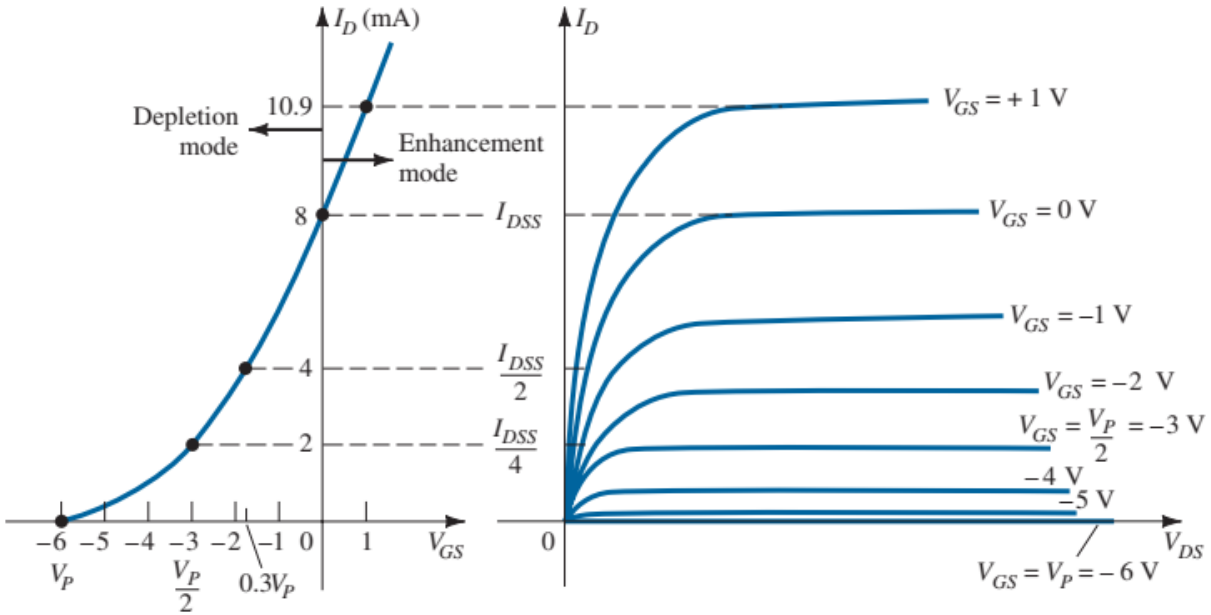
Depletion MOSFET Operation

- $V_{GS} = 0$, $V_{DS} > 0$
  - Current $I_D = I_S = I_{DSS}$ flows between drain and source
  - Current is only limited by channel resistance
- $V_{GS} < 0$, $V_{DS} > 0$
  - Channel electrons are repelled to P-type substrate, reducing the number of free electrons in the N-channel available for conduction
- $V_{GS} > 0$, $V_{DS} > 0$
  - Positive gate draws additional electrons from substrate



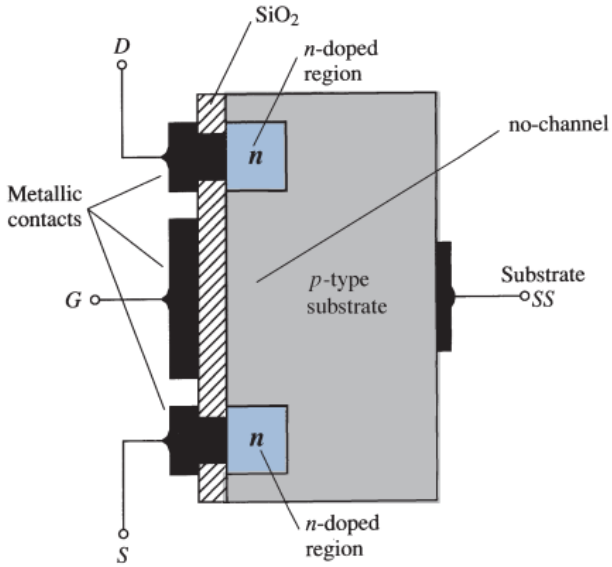
- Relationship $V_{GS} \times I_D$

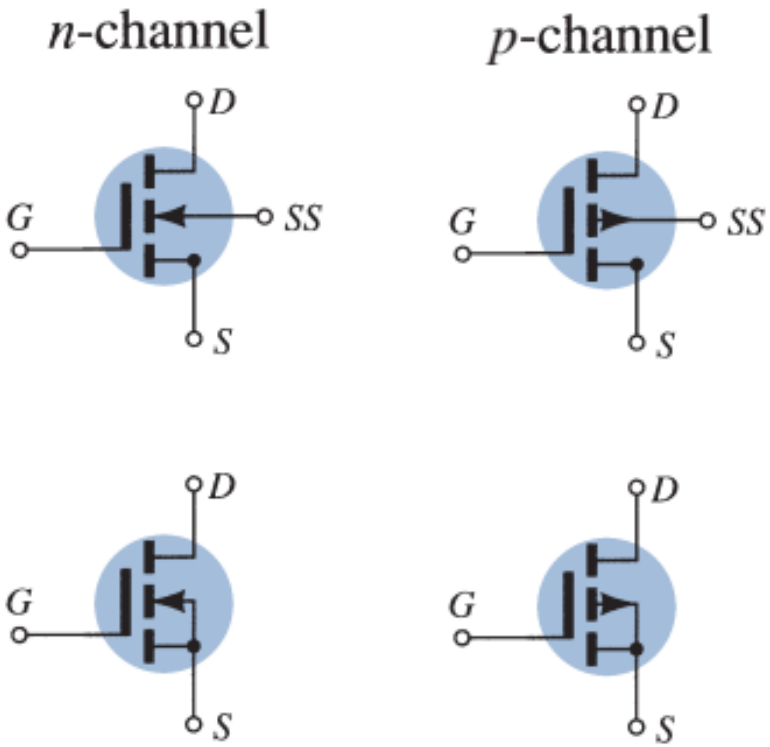
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Enhancement MOSFET Construction

- N-channel (depicted) and P-channel Enhancement MOSFET
  - Channel is absent as a constructed component
  - Gate is insulated from N-channel by a very thin silicon dioxide (SiO_2)
- Symbols

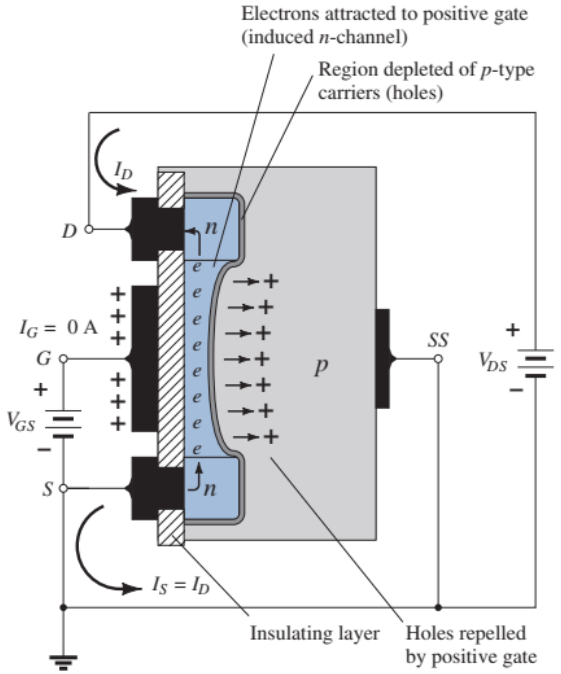


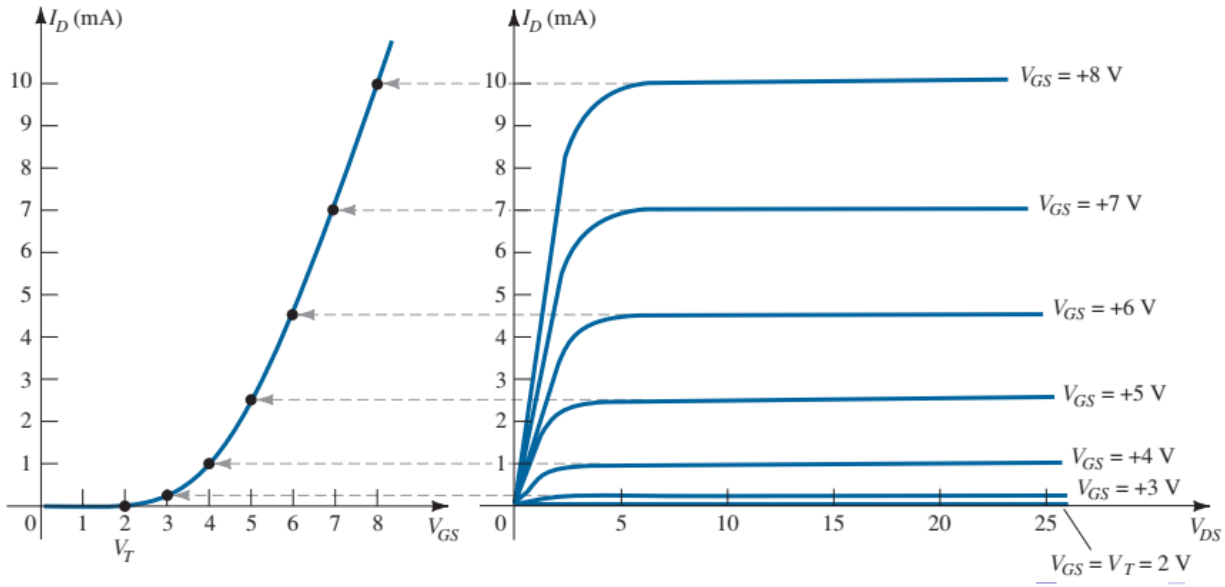


Enhancement MOSFET Operation

- $V_{GS} < V_T$, $V_{DS} > 0$
  - Channel absent and $I_D = I_S = 0$
- $V_{GS} > V_T$, $V_{DS} > 0$
  - Positive potential attracts electrons and a channel is formed
- Relationship $V_{GS} \times I_D$

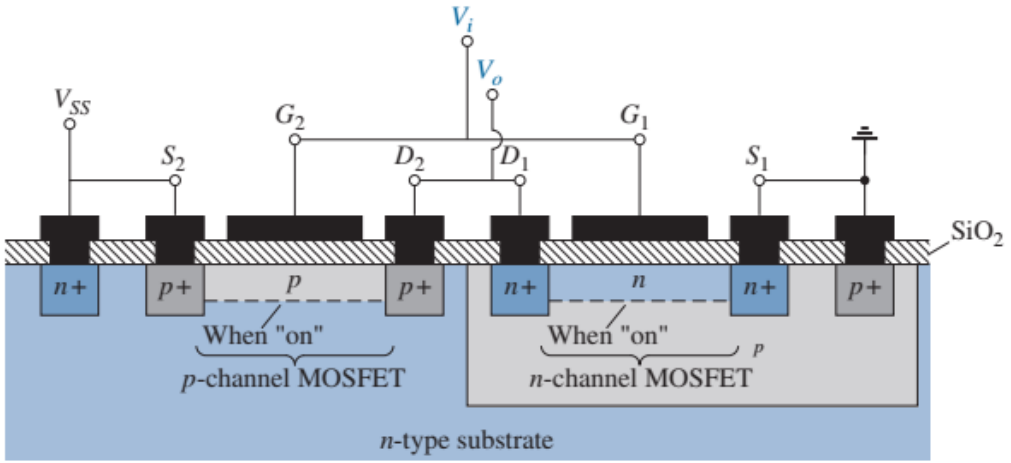
$$\boxed{I_D = k\,(V_{GS} - V_T)^2} \text{ with } k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

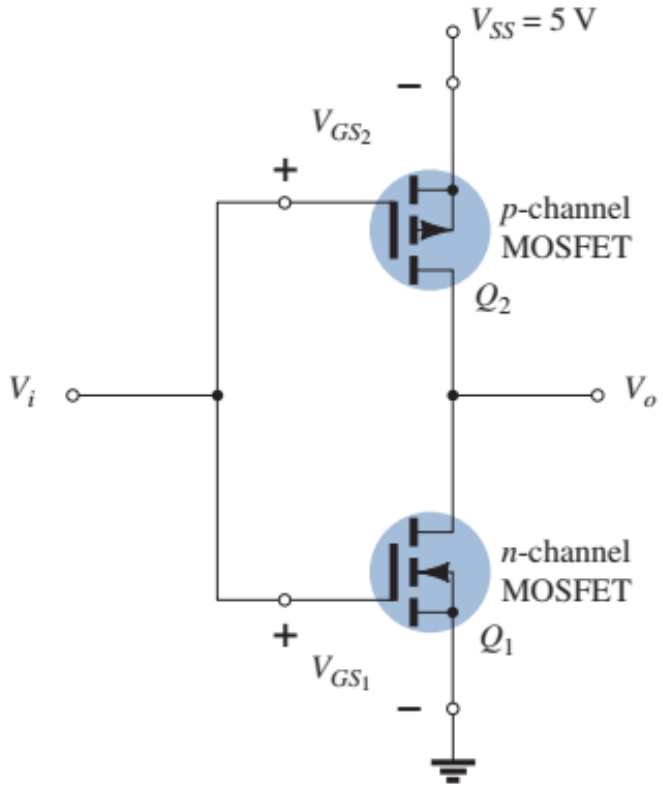




Complementary MOSFET (CMOS)

- CMOS construction: P-channel and N-channel MOSFETs built on the same substrate, with similar (but opposite) characteristics
- Extensively used in logic circuit design
- Offers high input impedance, fast switching speeds, and lower operating power levels
- Example: NOT (inverter) gate





Biasing

- Biasing places transistor in its fixed operating point (Q-point)
- Important basic relationships for a transistor:

$$\boxed{I_G \approx 0} \qquad \boxed{I_D = I_S}$$

- Relationship for JFET and depletion-type MOSFET:

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

- Relationship for enhancement-type MOSFET:

$$\boxed{I_D = k\left(V_{GS} - V_T\right)^2}$$

- Q-point can be determined using **analytical** or **graphical** approach

Biasing Circuits: Fixed-Bias

- Gate-Source loop

$$V_{GG} - I_G R_G + V_{GS} = 0$$

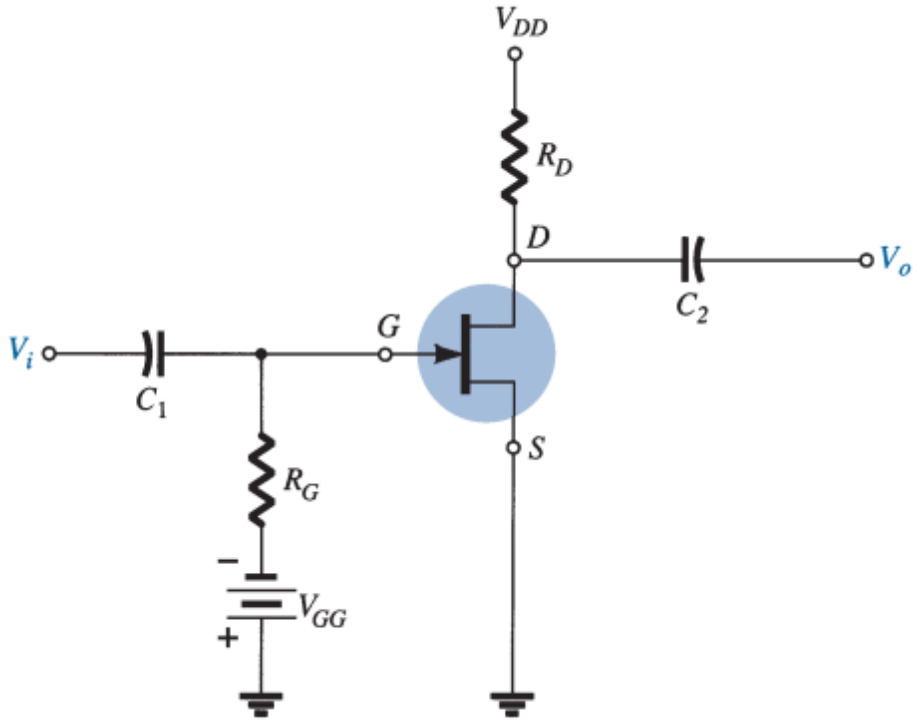
$$\boxed{V_{GS} = -V_{GG}}$$

- Drain-Source loop

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

$$V_{DD} - V_{DS} - I_D R_D$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$



Fixed-Bias Example

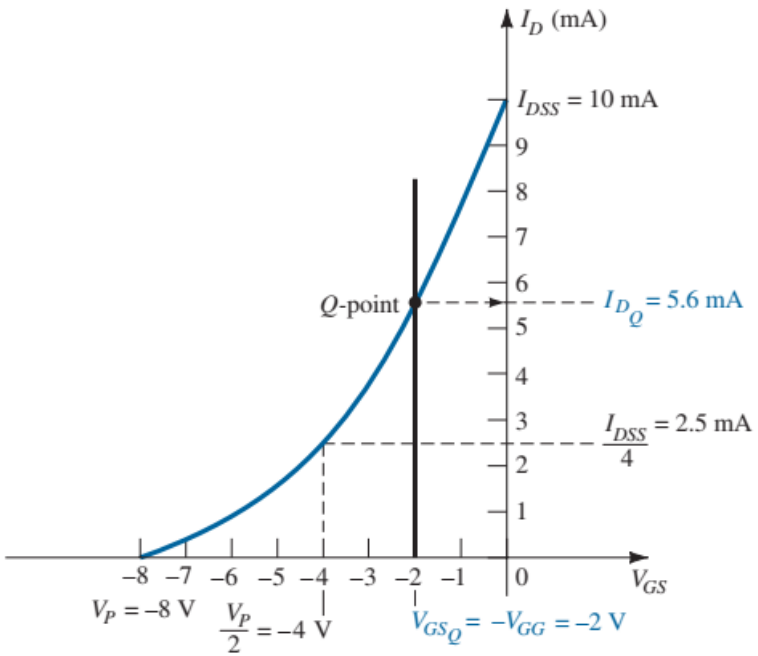
- Analytical approach:

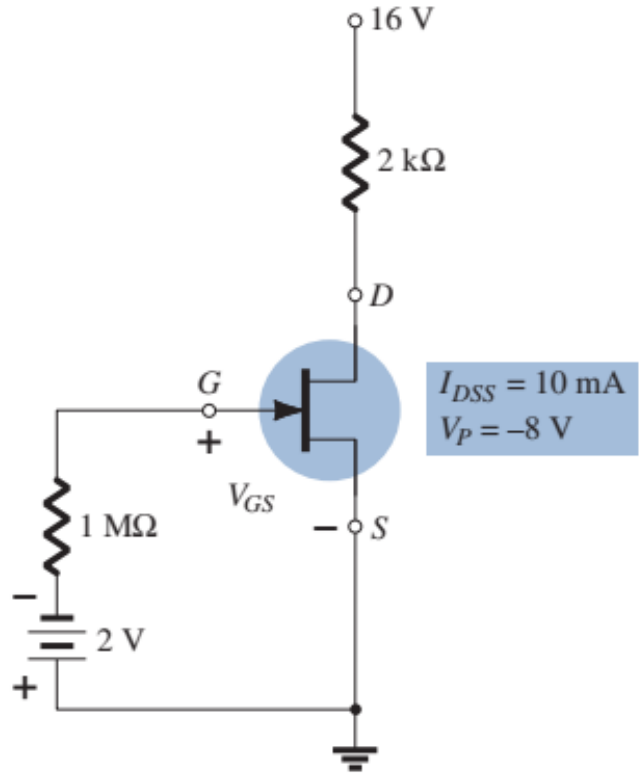
$$V_{GS} = -V_{GG} = -2 \text{ V}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{m}\left(1 - \frac{-2}{-8}\right)^2 = 5.63 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 16 - 5.63\text{m} \times 2\text{k} = 4.75 \text{ V}$$

- Graphical approach:





Biasing Circuits: Self-Bias

- Gate-Source loop

$$I_D R_S - I_G R_G + V_{GS} = 0$$

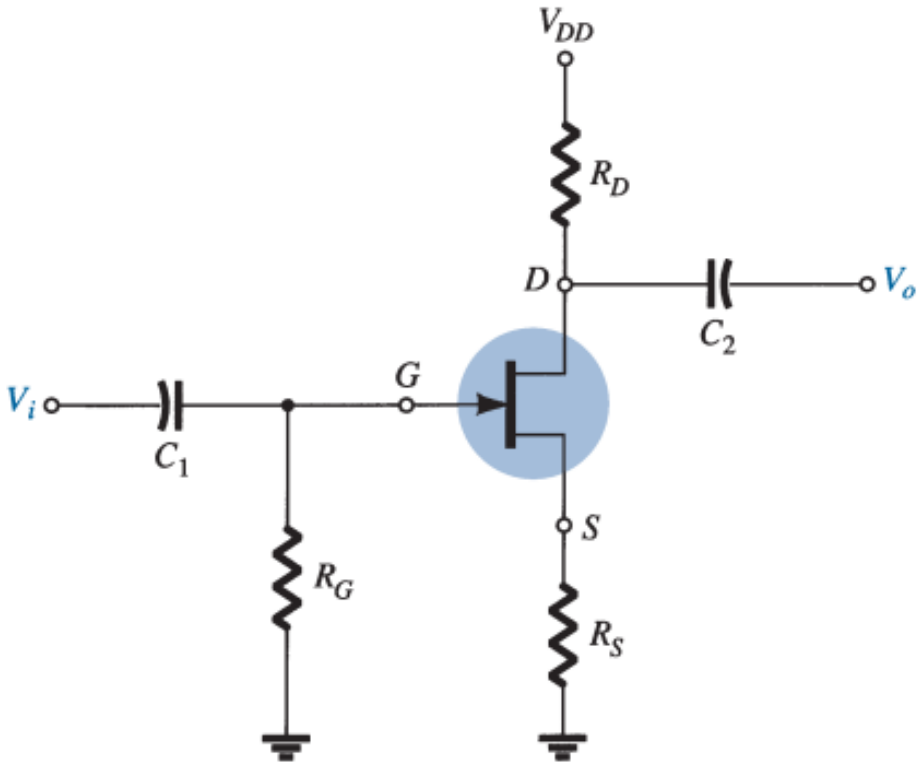
$$\boxed{V_{GS} = -I_D R_S}$$

- Drain-Source loop

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

$$V_{DD} - V_{DS} - I_D(R_D + R_S)$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$



Self-Bias Example

- Analytical approach:

$$V_{GS} = -I_D R_S = -1\text{k} I_D \leftarrow \boxed{\text{load-line}}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8\text{m}\left(1 - \frac{-1\text{k} I_D}{-6}\right)^2 \rightarrow$$

$$\frac{2\text{k}}{9} I_D^2 - \frac{11}{3} I_D + 8\text{m} = 0 \rightarrow$$

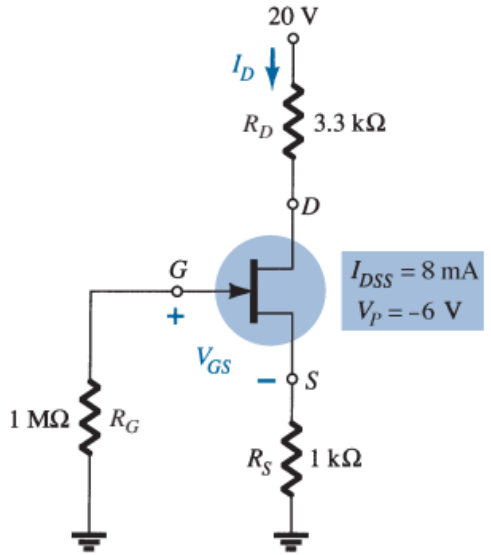
$$I_D = 13.9 \text{ mA, or } I_D = 2.59 \text{ mA}$$

$$V_{GS} = -1\text{k} \times 2.59\text{m} = -2.59 \text{ V}$$

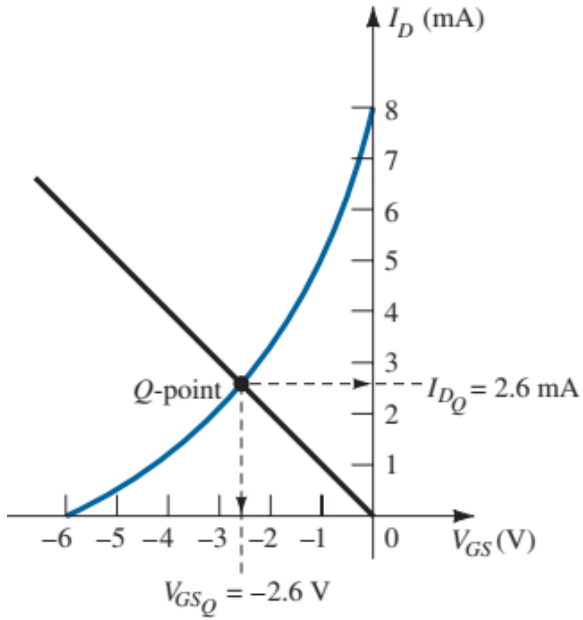
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 20 - 2.59\text{m}(3.3\text{k} + 1\text{k})$$

$$= 8.86 \text{ V}$$



- Graphical approach →



Biasing Circuits: Voltage-Divider Bias

- Gate-Source loop

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$V_G - V_{GS} - I_D R_S = 0$$

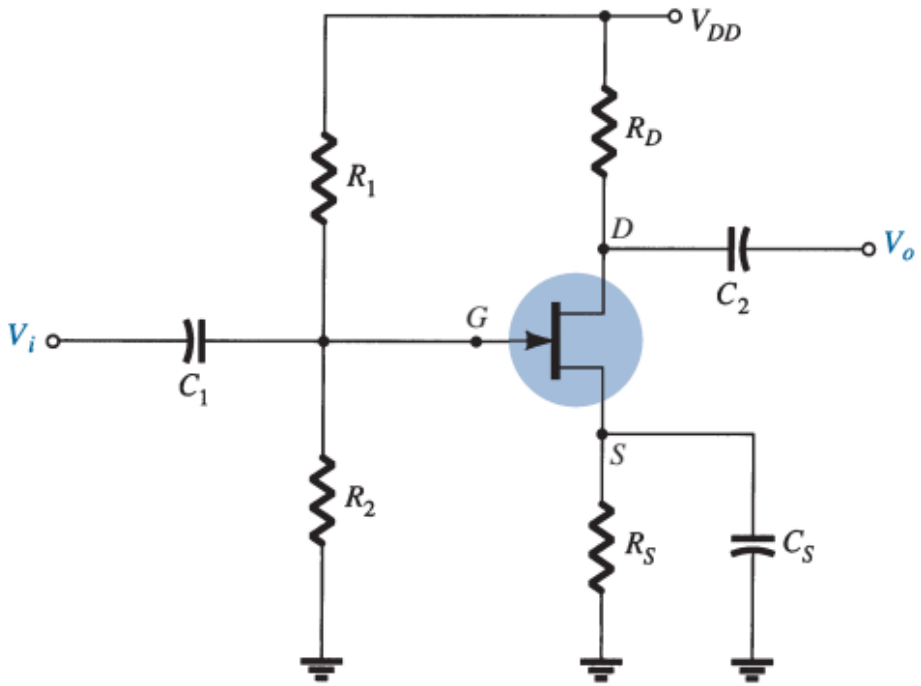
$$\boxed{V_{GS} = V_G - I_D R_S}$$

- Drain-Source loop

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

$$V_{DD} - V_{DS} - I_D(R_D + R_S)$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$



Voltage-Divider Bias Example

- Analytical approach:

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{270\text{k}}{2.1\text{M} + 270\text{k}} 16 = 1.82 \text{ V}$$

$$V_{GS} = V_G - I_D R_S = 1.82 - 1.5\text{k} I_D \leftarrow \boxed{\text{load-line}}$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8\text{m} \left(1 - \frac{1.82 - 1.5\text{k} I_D}{-4}\right)^2 \rightarrow$$

$$1.125\text{k} I_D^2 - 9.734 I_D + 16.952\text{m} = 0 \rightarrow$$

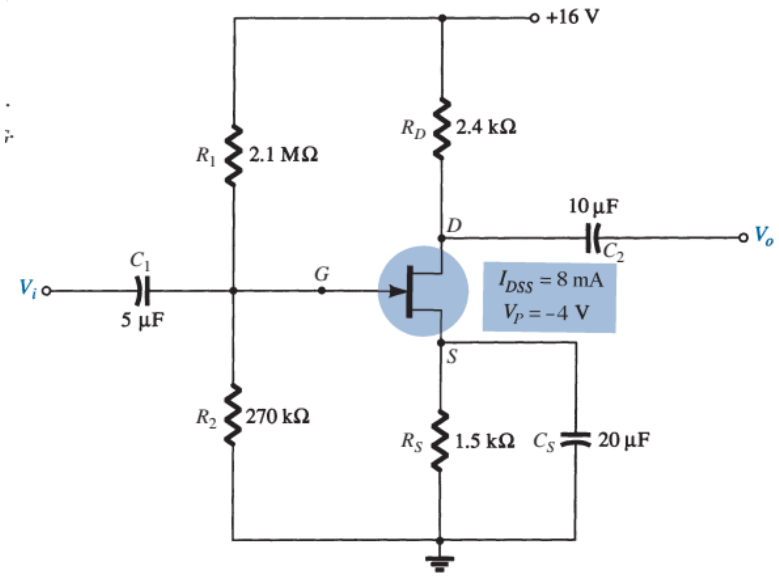
$$I_D = 6.24 \text{ mA, or } I_D = 2.42 \text{ mA}$$

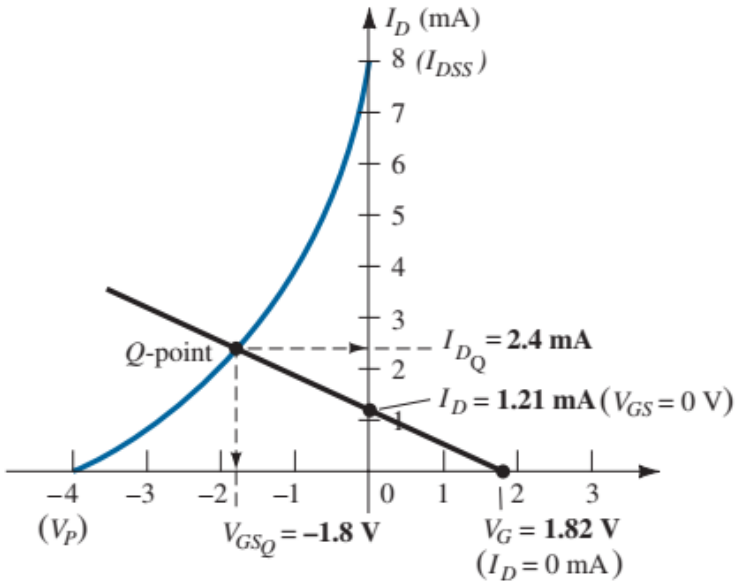
$$V_{GS} = 1.82 - 1.5\text{k} \times 2.42\text{m} = -1.81 \text{ V}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 16 - 2.42\text{m}(2.4\text{k} + 1.5\text{k})$$

$$= 6.56 \text{ V}$$





- Graphical approach →

Voltage-Divider Bias Example

- Graphical approach:

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{18\text{M}}{22\text{M} + 18\text{M}} 40 = 18 \text{ V}$$

$$V_{GS} = V_G - I_D R_S = 18 - 820 I_D \leftarrow \boxed{\text{load-line}}$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

$$= \frac{3\text{m}}{(10-5)^2} = 0.12 \text{ mA/V}^2$$

$$I_D = k\,(V_{GS} - V_T)^2 = 0.12\text{m}\,(V_{GS} - 5)^2$$

$$V_{GS} = 10 \text{ V} \rightarrow I_D = 3 \text{ mA}$$

$$V_{GS} = 15 \text{ V} \rightarrow I_D = 12 \text{ mA}$$

$$V_{GS} = 20 \text{ V} \rightarrow I_D = 27 \text{ mA}$$