Xianwei ZHANG ✉ xianeizhang@cs.pitt.edu http://iarchsys.com
+1 412-425-4362 6514 Sennott Square, Pittsburgh PA-15206

Research Interests

Memory System, Computer Architecture and Systems
My research interests lie broadly in computer architecture and system with particular emphasis on memory system design and optimization on the critical aspects of latency, energy and bandwidth. Besides memory design, I also explore memory topics in extended scenarios such as approximate computing and security.
In addition, I also have broad interests on other system areas/topics, e.g. operating system, GPGPU and compilation, which are partially covered in my tech blog and notes.

Education

Ph.D. candidate in Computer Science Aug 2011 - Apr 2017 (expected)
University of Pittsburgh, Pittsburgh, USA

- `Dissertation Topic`: *"Exploration of DRAM Scaling from Restoring Perspective"*
- `Advisor`: Prof. *Youtao Zhang*
- `Co-advisors` (working with): Prof. *Jun Yang* (ECE) and Prof. *Bruce Childers* (CS)

B.E. in Software Engineering Sep 2007 - Jun 2011
Northwestern Polytechnical University, Xi'an, China

Experiences

University of Pittsburgh Graduate Student Researcher
Pittsburgh, USA May 2013 – Present

- Dec 15- Now , Apply approximate computing to achieve energy-accuracy tradeoff.
- Jan 14-Sep 15, Mitigate performance and yield issues in further scaling DRAM.
- Oct 14-Mar 15, Improve bandwidth and performance in Hybrid Memory Cube (HMC).
- Feb 13-May 15, Construct energy efficient non-volatile memories (PCM and DWM).

University of Pittsburgh Teaching Assistant
Pittsburgh, USA Aug 2011 – Apr 2013
CS0401 (Fall'11, Spring'12), CS1502 (Fall'12), CS2520 (Spring'13), CS2210 (Spring'15)

Alipay Technology Inc., Alibaba Java Developer Intern
Hangzhou, China Aug 2010 – Dec 2010
Implemented source management system based on SOFA/Spring framework.

Publications

`Xianwei Zhang`, Youtao Zhang, Bruce R. Childers and Jun Yang HPCA'2016
Restore Truncation for Performance Improvement in Future DRAM Systems.
The 22nd IEEE Symposium on High Performance Computer Architecture(HPCA), Barcelona, Spain, 2016.

`Xianwei Zhang`, Youtao Zhang, Bruce R. Childers and Jun Yang TODAES
On the Restore Time Variations of Future DRAM Memory, (*under review*).
ACM Transactions on Design Automation of Electronic Systems (TODAES).

`Xianwei Zhang`, Youtao Zhang, Bruce R. Childers and Jun Yang DATE'2015
Exploiting DRAM Restore Time Variations in Deep Sub-micron Scaling.
The IEEE conference on Design, Automation and Test in Europe (DATE), Grenoble, France, 2015.

`Xianwei Zhang`, Youtao Zhang and Jun Yang ICCD'2015
DLB: Dynamic Lane Borrowing for Improving Bandwidth and Performance in Hybrid Memory Cube.
The 33rd IEEE International Conference on Computer Design(ICCD), NYC, NY, 2015.

`Xianwei Zhang`, Youtao Zhang and Jun Yang ICCD'2015
TriState-SET: Proactive SET for Improved Performance in MLC Phase Change

Memories.
The 33rd IEEE International Conference on Computer Design(ICCD), NYC, NY, 2015.

`Xianwei Zhang`, Youtao Zhang and Jun Yang ICCD'2015
Exploit Common Source-Line to Construct Energy Efficient Domain Wall Memory based Caches.
The 33rd IEEE International Conference on Computer Design(ICCD), NYC, NY, 2015.

`Xianwei Zhang`, Youtao Zhang and Jun Yang DAC'2015
Adaptive Lane Borrowing of Hybrid Memory Cube, (*Work-in-progress*).
The 52nd ACM/IEEE Design Automation Conference (DAC), San Francisco, CA, June 2015.

`Xianwei Zhang`, Youtao Zhang, Chuanjun Zhang and Jun Yang ISLPED'2013
WoM-SET: Lowering Write Power of Proactive-SET based PCM Write Strategy Using WoM Code.
The International Symposium on Low Power Electronics and Design (ISLPED), Beijing, China, 2013.
⋆⋆⋆ **Best Paper Award** ⋆⋆⋆

Presentations

HPCA Symposium *Mar 2016*, Barcelona, Spain
Restore Truncation for Performance Improvement in Future DRAM Systems

Thesis Proposal *Jan 2016*, Pittsburgh, USA
Exploration of DRAM Scaling from Restoring Perspective

ICCD Symposium *Oct 2015*, New York City, USA
DLB: Dynamic Lane Borrowing for Improving Bandwidth and Performance in Hybrid Memory Cube
TriState-SET: Proactive SET for Improved Performance of MLC Phase Change Memories

MemSys Symposium *Oct 2015*, Washington DC, USA
Achieving Yield, Density and Performance Effective DRAM at Extreme Technology Sizes

CompExam *Jul 2015*, Pittsburgh, USA
Shared Resources Management and Execution Replay in Chip Multiprocessor

Honors & Awards

Andrew Mellon Predoctoral Fellowship *University of Pittsburgh*'2016

Student Travel Awards *HPCA*'2016, *SPAA*'2015

Best Paper Award *ISLPED*'2013

Recipient of 2011 graduation design (Thesis) key support fund *NPU*'2011

National Scholarship *Ministry of Education of China*'2010

Tencent Technology Excellence Scholarship *Tencent Inc.*'2009

Skills

Programming: C/C++, JAVA, Shell, Python, Android
Simulation: GEM5, MARSSx86, DRAMSim2, USIMM, CACTI, SPICE
Tools: Pin, Vim, Makefile, Git, GDB, LaTeX, gcc/g++

Misc

Homepage: https://people.cs.pitt.edu/∼xianeizhang/
Github: https://github.com/cinwell
Blog: http://iarchsys.com

References

Available upon request.