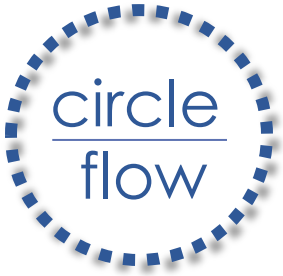
turns

Ethernet switch

into

network analyzer



overview

- working principle
- product solution
- business value
- law statements

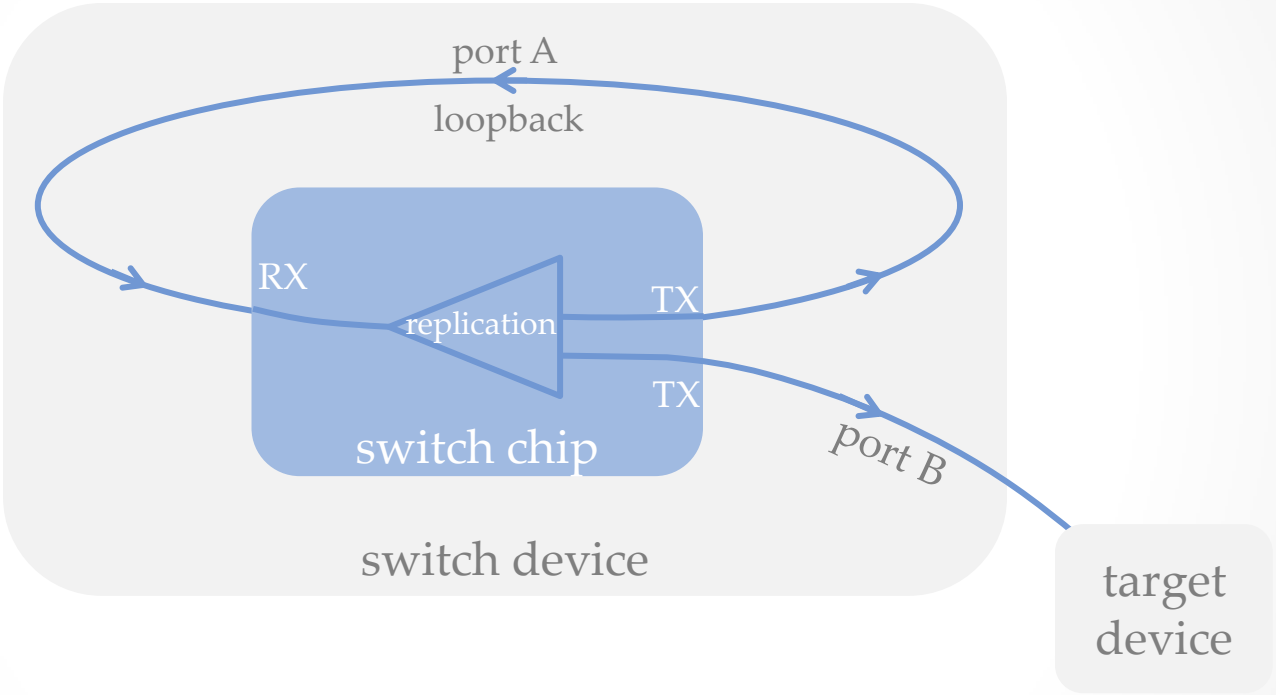
is it possible ?

- Ethernet layer 2/3 switching at wire speed
- ASIC
- about RMB 200 per port

- Ethernet traffic generating and analysis at wire speed
- FPGA
- about RMB 2K per port

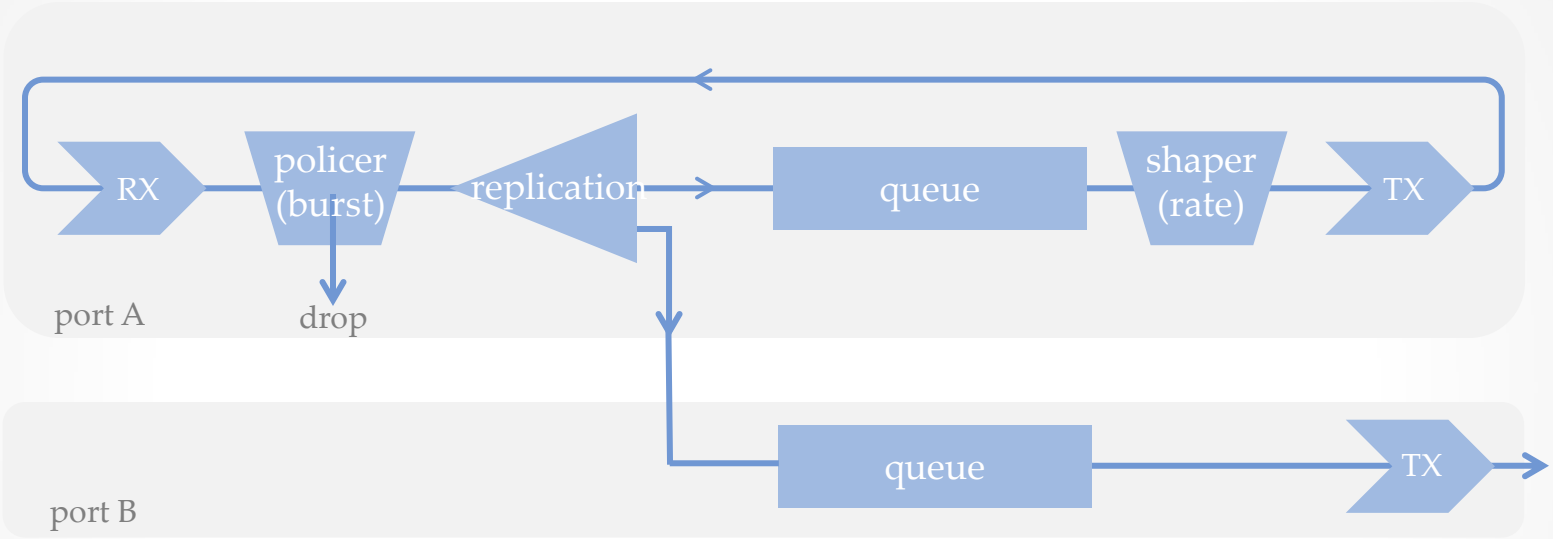
price source：http://www.smartechconsulting.com/Test/Spirent-TestCenter-Test-Center

basic idea



with two ports A and B, A is in loopback, B connects to external.
packet flows in loop of A, each loop replicates a copy of packet for B,
and B send it out to external device, i.e. continuing traffic flow.
A and B keep on the same packet rate.

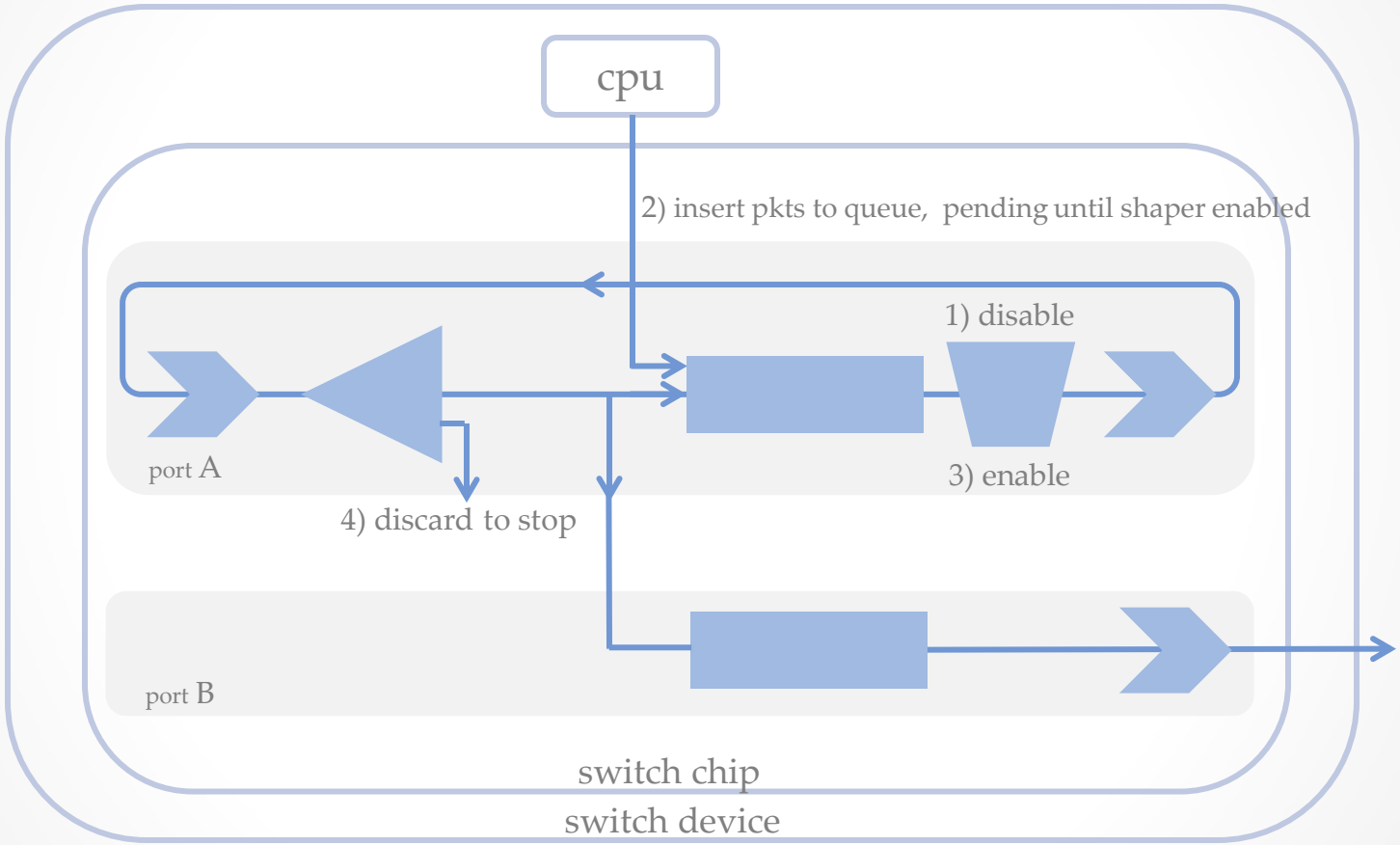
rate & burst



with the shaper on queue of port A, we are enable to control the packet rate that flowing inside A, that is the same rate of B.

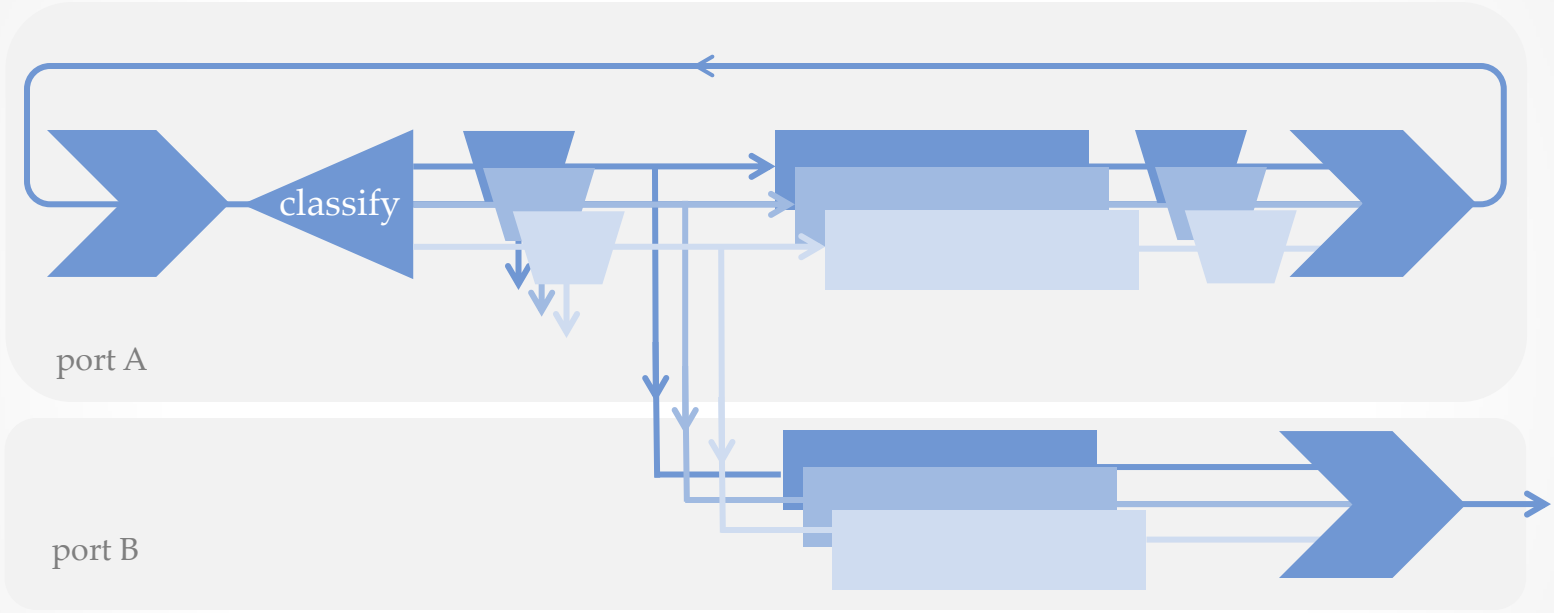
with the policer at ingress of port A, we are able to control the number of loop times, that is the burst number of packets. for a close look:
turn off token injecting, set existing token number, start loop traffic.
once token exhausted, all ingress packet will be discard, no more replication, no more loop, then B stops sending packets out.

start & stop



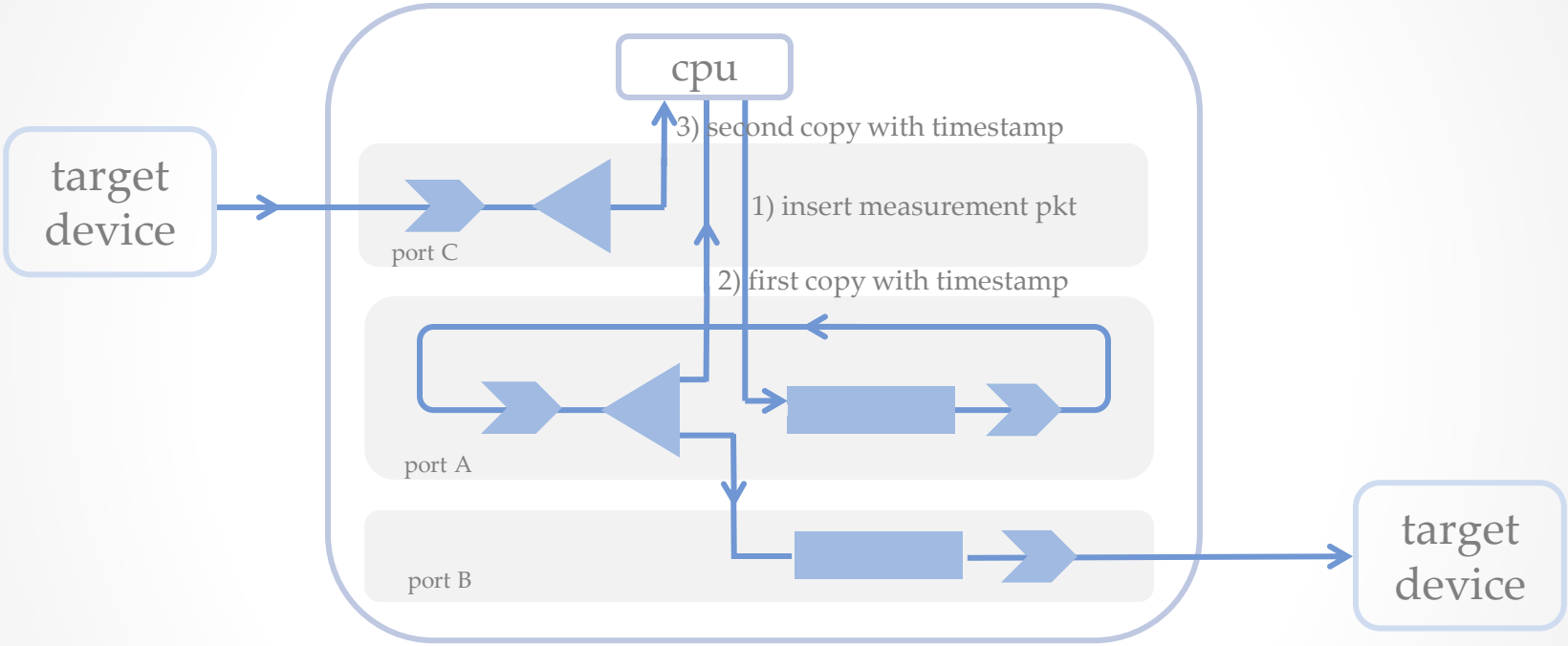
start: disable shaper, CPU insert pkt to queue, enable shaper.
with looping, just few(<10) pkts required to reach wire speed.
stop: simply discard packets at ingress to break loop flow.

multi flow per port



typically there're 8 or more queue per port, thus we have 8 or more individual flows with rate control per port.
each flow identified by pkt classification and redirect to corresponded queue.

latency measurement



1) CPU insert a marked pkt into port A, that pkt duplicates into 2 copy after loopback.
2) first copy is sent back to CPU with timestamp T1.
3) second copy is sent to target device via port B, finally comeback to port C, and sent to CPU with timestamp T2.
4) calculating T1 and T2 to have the forwarding latency of target device.

completed function

- flow with variable content of packets(increasing, decreasing, random)
  CPU inserts a number of packet with different content into queue.
  the depth of queue(buffer) decides how many packets acceptable.

- transmit statistics of flow
  according to the transmitted counter of queue on port (port B)

- analysis on received traffic
  with the ingress classification of port, to counting and capture specific flow received

limitation

- dimension of HW resource
  number of queue decides the number transmitting flow
  packet classification(TCAM) decides the number of receiving flow
  availability of buffer (queue depth) decides the variable flow

- out of sequence detection
  this detection requires a unique SN for each packet, and inspecting it on receiving. it is not possible to support this by regular ethernet switch chip.

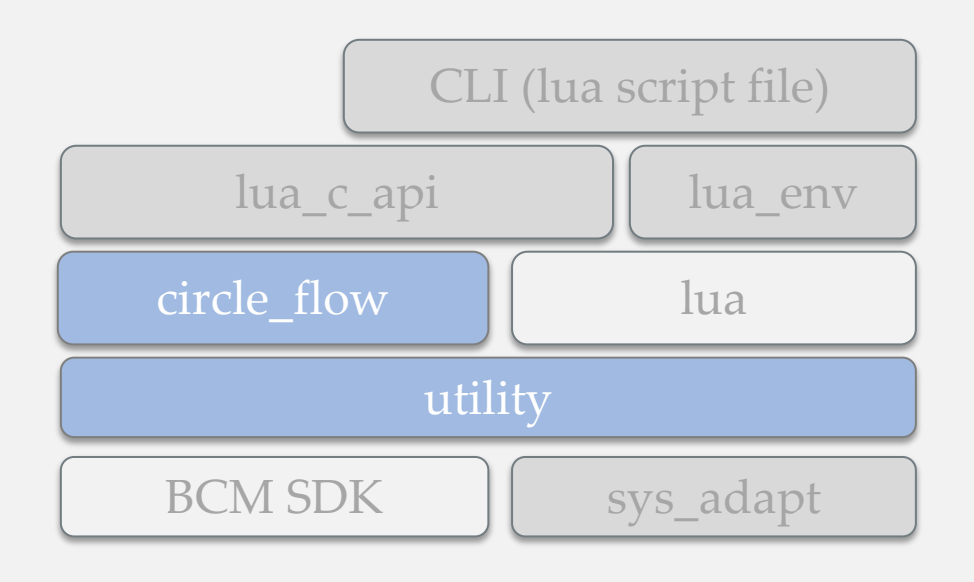
- global sharing
  buffer, TCAM and most of other resource are shared globally, they could be exhausted by configuration on particular ports, and this would lead to out of resource failure when configuring on other ports.

reborn

1) reuse existing ethernet switch box hardware
2) replace software (integrate “circle flow”, design UI)

what's circle flow

example of implementation code, based on Broadcom XGS chip
provides the core functionality of network analyzer, and CLI.



: kernel module
: system/application module (optional)
: third party module

business value

- low cost
  reuse existing ethernet switch box, no more HW R&D cost.
  low BOM, ASIC < FPGA (other solution).

- performance
  based on industrial ethernet switch chip, it is easy to provide 10/40/100G wire speed traffic.

- high port dense
  it is easy to build several switch chip on board, to provide massive ports.

- low power consumption
  ASIC < FPGA (other solution)

statements

- copyright of “circle flow” is reserved, only allows for use of experimental purpose, dose not allow for any commercial purpose.
- author of “circle flow” shall not be liable for any claim, damages or liability in connection with the software.
- the method of turning ethernet switch into network analyzer is under protection of patent (ZL 2013 1 0227029.9).

find more

at

www.circleflow.net

or

github.com/circleflow