FMEA Analysis Report
ESP32-C6 Development Board

Failure Mode and Effects Analysis
for Electronic Circuit Board

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Standard:	AIAG-VDA FMEA / IPC-A-610
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Executive Summary

This FMEA analysis evaluates the ESP32-C6 Development Board circuit design to identify potential failure modes and assess associated risks. The analysis examined 0 components across 5 subsystems.

Key Findings

Metric	Value	Status
Total Failure Modes Analyzed	15	✓ Good
Critical Risk Modes (RPN ≥ 300)	3	■ Attention
High Risk Modes (125 ≤ RPN < 300)	9	■ Attention
Average RPN Score	207.9	■ Attention

System Overview

ESP32-C6 Development Board with hierarchical design featuring: - USB-C interface with proper CC resistors and ESD protection - 5V to 3.3V power regulation using AMS1117 linear regulator - ESP32-C6-MINI-1 microcontroller module with WiFi 6 and BLE 5 - Debug header for programming and development - Status LED for user indication

Subsystems

• **USB-C Interface**: USB-C receptacle with CC resistors (5.1kΩ) for UFP mode and ESD protection

• **Power Supply**: AMS1117-3.3V linear regulator with input/output capacitors

• **ESP32-C6 MCU**: ESP32-C6-MINI-1 module with USB signal conditioning

• **Debug Interface**: 2x3 IDC header for UART, reset, and boot control

• **Status LED**: LED with 330Ω current limiting resistor

FMEA Analysis Table

ID	Component	Failure Mode	Effect	S	O	D	RPN	Risk
1	J1 - USB-C Connector	Solder joint failure	Complete loss of power and USB	9	6	7	378	Critical
2	U1 - AMS1117	Thermal shutdown	System shutdown, no 3.3V power	8	7	6	336	Critical
3	U2 - ESP32-C6	RF interference	WiFi/BLE performance degradati	6	8	7	336	Critical
4	D1/D2 - ESD Diodes	ESD protection failure	USB data lines vulnerable to E	7	5	8	280	High
5	USB Data Lines	Signal integrity issues	USB enumeration failure, data	7	6	6	252	High
6	C2 - Input Cap	Capacitance degradation	Power supply instability, incr	6	7	6	252	High
7	MCU Ground Pins	Poor ground connection	Digital noise, system instabil	7	5	7	245	High
8	J2 - Debug Header	Intermittent connection	Programming/debugging failures	5	7	5	175	High
9	C3 - Output Cap	ESR increase	3.3V rail noise, potential MCU	6	6	6	216	High
10	R1/R2 - CC Resistors	Resistance drift	Incorrect USB-C power negotiat	6	5	6	180	High
11	R4/R5 - USB Resistor	Value tolerance	USB signal integrity degradati	5	6	6	180	High
12	C4 - MCU Decoupling	High frequency noise	MCU supply noise, logic errors	5	5	7	175	High
13	D3 - Status LED	LED burn-out	Loss of status indication only	3	4	3	36	Low
14	R3 - LED Resistor	Open circuit	LED non-functional	2	3	3	18	Low
15	PCB Substrate	Delamination	Potential trace breaks, cosmet	4	3	5	60	Medium

Risk Assessment Matrix

Risk Level	RPN Range	Count	Action Required
Critical	≥ 300	3	Immediate action required
High	125-299	9	Action required before production
Medium	50-124	1	Monitor and improve if feasible
Low	< 50	2	Acceptable risk level

Recommendations

Priority Actions

• **J1 - USB-C Connector** - Solder joint failure: Add mechanical support brackets, use thicker copper pours (2oz), implement strain relief

• **U1 - AMS1117** - Thermal shutdown: Add thermal vias under regulator, implement copper pour heatsink, consider switching regulator

• **U2 - ESP32-C6** - RF interference: Implement solid ground plane, add ferrite beads, improve decoupling network

• **D1/D2 - ESD Diodes** - ESD protection failure: Upgrade to TVS diode arrays, add series resistance, implement guard rings

• **USB Data Lines** - Signal integrity issues: Control impedance to 90Ω differential, match trace lengths, add ground guards

General Recommendations

• Implement design review process with focus on high-RPN items

• Establish component derating guidelines (50-80% of maximum ratings)

• Add test points for critical signals to improve detection capability

• Implement thermal analysis and management for power components

• Establish incoming inspection procedures for critical components

• Document lessons learned and update FMEA regularly