单时钟FIFO测试代码

# 测试empty flag

## 1．写一个数，然后读空

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 23:02:59 03/13/2013

// Design Name: top\_sync\_fifo

// Module Name: E:/fpga\_svn/sync\_fifo/top\_sync\_fifo\_testbench.v

// Project Name: sync\_fifo

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: top\_sync\_fifo

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module top\_sync\_fifo\_testbench;

// Inputs

reg clk;

reg rst;

reg wena;

reg rena;

reg [7:0] wdata;

// Outputs

wire [7:0] rdata;

wire empty;

wire full;

// Instantiate the Unit Under Test (UUT)

top\_sync\_fifo uut (

.clk(clk),

.rst(rst),

.wena(wena),

.rena(rena),

.wdata(wdata),

.rdata(rdata),

.empty(empty),

.full(full)

);

initial begin

// Initialize Inputs

clk = 0;

rst = 1;

wena = 0;

rena = 0;

wdata = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

rst = 0;

#5; clk = 1; wdata = 8'b1100\_0000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

end

endmodule

## 2．未写入数直接读空

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

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// Inputs

reg clk;

reg rst;

reg wena;

reg rena;

reg [7:0] wdata;

// Outputs

wire [7:0] rdata;

wire empty;

wire full;

// Instantiate the Unit Under Test (UUT)

top\_sync\_fifo uut (

.clk(clk),

.rst(rst),

.wena(wena),

.rena(rena),

.wdata(wdata),

.rdata(rdata),

.empty(empty),

.full(full)

);

initial begin

// Initialize Inputs

clk = 0;

rst = 1;

wena = 0;

rena = 0;

wdata = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

rst = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

end

endmodule

# 测试满标志

## 一直写，写到溢出

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

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//

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// Outputs

wire [7:0] rdata;

wire empty;

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top\_sync\_fifo uut (

.clk(clk),

.rst(rst),

.wena(wena),

.rena(rena),

.wdata(wdata),

.rdata(rdata),

.empty(empty),

.full(full)

);

initial begin

// Initialize Inputs

clk = 0;

rst = 1;

wena = 0;

rena = 0;

wdata = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

rst = 0;

#5; clk = 1; wdata = 8'b0000\_0001;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b0000\_0010;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b0000\_0100;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b0000\_1000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b0001\_0000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b0010\_0000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b0100\_0000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b1000\_0000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b1100\_0000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

end

endmodule

## 先写再读空

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

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// Engineer:

//

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// Outputs

wire [7:0] rdata;

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wire full;

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top\_sync\_fifo uut (

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#5; clk = 1; rena = 0;

#5; clk = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

#5; clk = 1; wdata = 8'b1100\_0000;

#5; clk = 0;

#5; clk = 1; wena = 1;

#5; clk = 0;

#5; clk = 1; wena = 0;

#5; clk = 0;

#5; clk = 1; rena = 1;

#5; clk = 0;

#5; clk = 1; rena = 0;

#5; clk = 0;

end

endmodule