异步FIFO测试文档

//\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_full flag\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 16:45:24 03/13/2013

// Design Name: top\_asyn\_fifo

// Module Name: E:/fpga\_svn/asyn\_fifo/top\_asyn\_fifo\_testbench.v

// Project Name: asyn\_fifo

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: top\_asyn\_fifo

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module top\_asyn\_fifo\_testbench;

// Inputs

reg wclk;

reg rclk;

reg wrst;

reg rrst;

reg wena;

reg rena;

reg [7:0] w\_data;

// Outputs

wire [7:0] r\_data;

wire full;

wire empty;

// Instantiate the Unit Under Test (UUT)

top\_asyn\_fifo uut (

.wclk(wclk),

.rclk(rclk),

.wrst(wrst),

.rrst(rrst),

.wena(wena),

.rena(rena),

.w\_data(w\_data),

.r\_data(r\_data),

.full(full),

.empty(empty)

);

initial begin

// Initialize Inputs

wclk = 0;

rclk = 0;

wrst = 1;

rrst = 1;

wena = 0;

rena = 0;

w\_data = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

wrst = 0;

rrst = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_0001;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_0010;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_0100;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_1000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0001\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0010\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0100\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b1000\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b1100\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

end

always begin

#5;

rclk = ~rclk;

end

endmodule

//\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_empty flag\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

`timescale 1ns / 1ps

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// Inputs

reg wclk;

reg rclk;

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reg rrst;

reg wena;

reg rena;

reg [7:0] w\_data;

// Outputs

wire [7:0] r\_data;

wire full;

wire empty;

// Instantiate the Unit Under Test (UUT)

top\_asyn\_fifo uut (

.wclk(wclk),

.rclk(rclk),

.wrst(wrst),

.rrst(rrst),

.wena(wena),

.rena(rena),

.w\_data(w\_data),

.r\_data(r\_data),

.full(full),

.empty(empty)

);

initial begin

// Initialize Inputs

wclk = 0;

rclk = 0;

wrst = 1;

rrst = 1;

wena = 0;

rena = 0;

w\_data = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

wrst = 0;

rrst = 0;

#5; rclk = 1;

#5; rclk = 0;

#5; rclk = 1; rena = 1;

#5; rclk = 0;

#5; rclk = 1; rena = 0;

#5; rclk = 0;

end

always begin

#1;

wclk = ~wclk;

end

endmodule

//\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_读写双时钟\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

`timescale 1ns / 1ps

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reg wclk;

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reg [7:0] w\_data;

// Outputs

wire [7:0] r\_data;

wire full;

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// Instantiate the Unit Under Test (UUT)

top\_asyn\_fifo uut (

.wclk(wclk),

.rclk(rclk),

.wrst(wrst),

.rrst(rrst),

.wena(wena),

.rena(rena),

.w\_data(w\_data),

.r\_data(r\_data),

.full(full),

.empty(empty)

);

initial begin

// Initialize Inputs

wclk = 0;

rclk = 0;

wrst = 1;

rrst = 1;

wena = 0;

rena = 0;

w\_data = 0;

// Wait 100 ns for global reset to finish

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rrst = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_0001;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_0010;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_0100;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0000\_1000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0001\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0010\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b0100\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b1000\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

#1; wclk = 1; w\_data = 8'b1100\_0000;

#1; wclk = 0;

#1; wclk = 1; wena = 1;

#1; wclk = 0;

#1; wclk = 1; wena = 0;

#1; wclk = 0;

// #5;

// rclk = 1; rena = 1;

// #5;

// rclk = 0;

// #5;

// rclk = 1; rena = 0;

// #5;

// rclk = 0;

end

always begin

#5;

rclk = ~rclk; rena = ~rena;

#5;

rclk = ~rclk;

end

endmodule