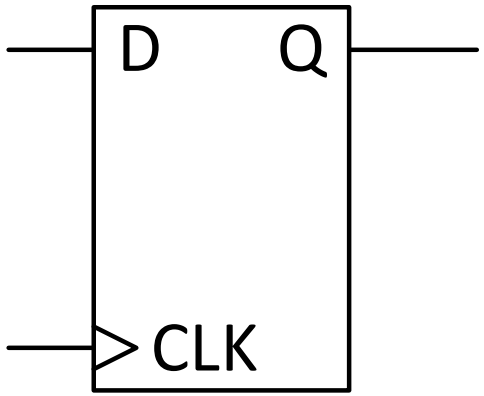
Electronics Systems (938II)

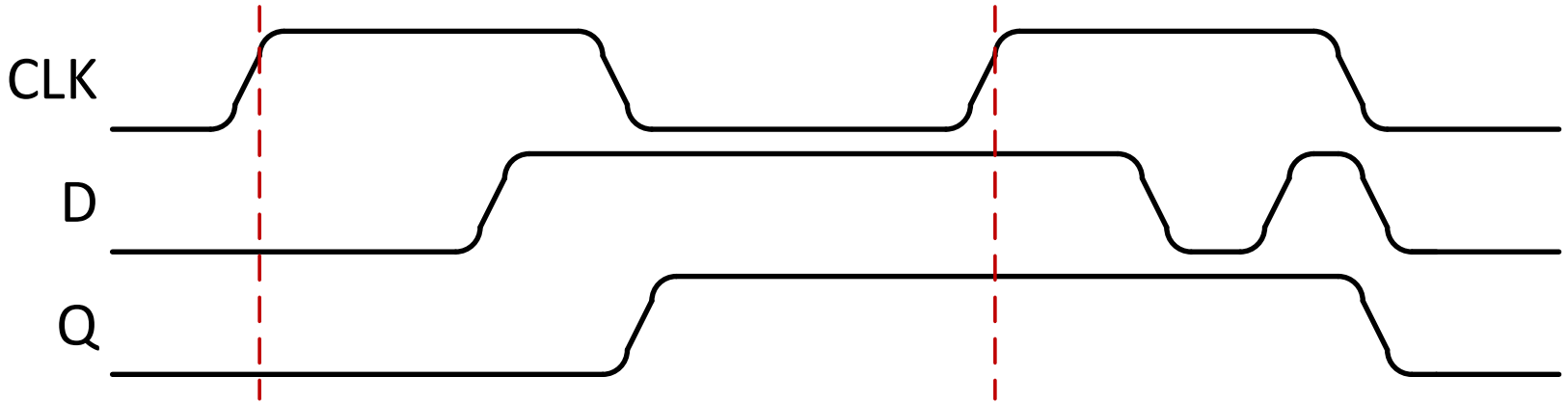
Lecture 2.6

Building Blocks of Electronic Systems – Timing constraints

Timing constraints

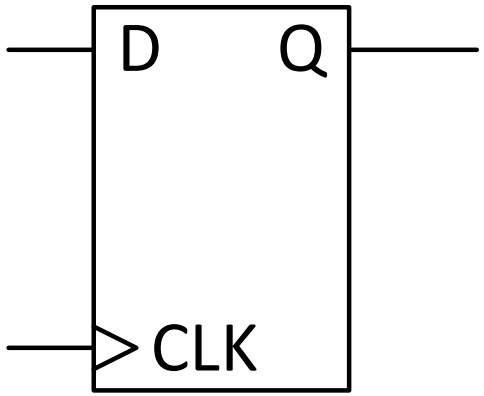
- Do you remember of registers and flip-flops?
  - They are edge-triggered, i.e. the output change only on the triggering edge of the clock signal

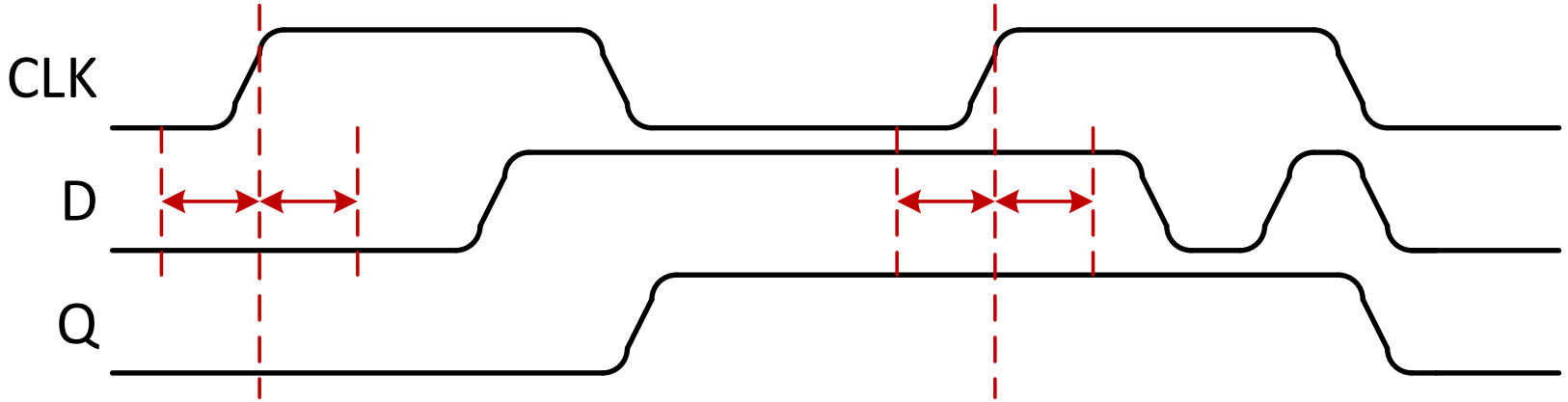




Timing constraints

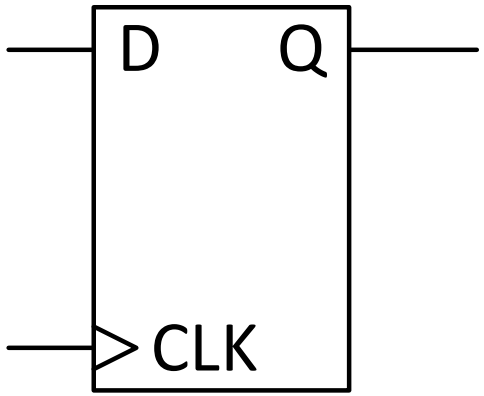
- Do you remember of registers and flip-flops?
  - To work properly, the input signal (D), must be stable
    - A certain time interval **before** the (triggering) edge of clock
    - A certain time interval **after** the (triggering) edge of clock

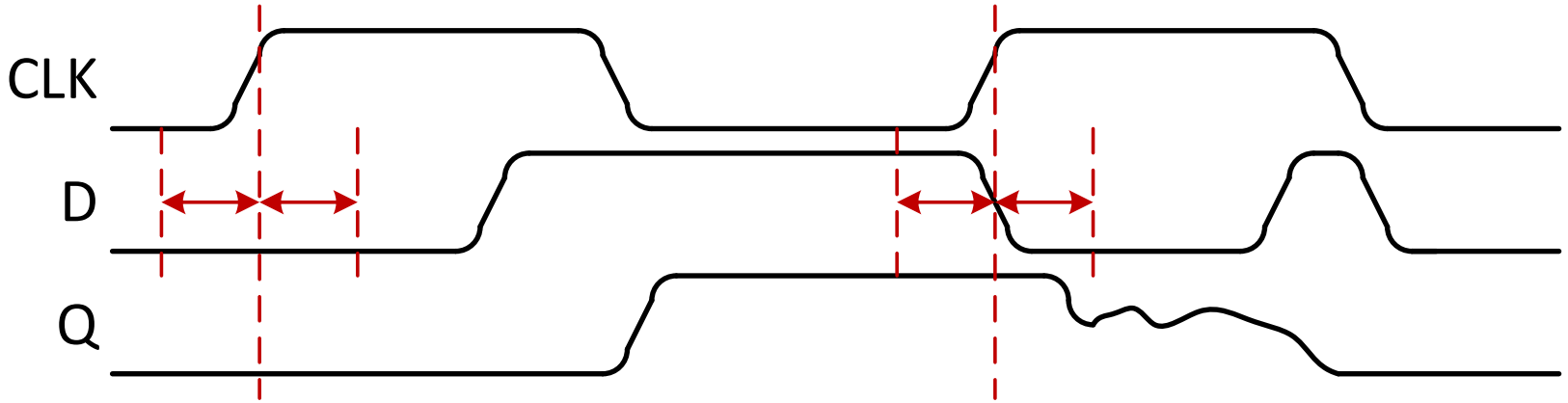




Timing constraints

- Do you remember of registers and flip-flops?
  - Otherwise, the register/flip-flop goes into a metastable state
    - I.e., the output is unpredictable
    - It oscillates for a while between 0 and 1, and then settles down to either 1 or 0





Timing constraints

- Do you remember of registers and flip-flops?
  - Otherwise, the register/flip-flop goes into a metastable state
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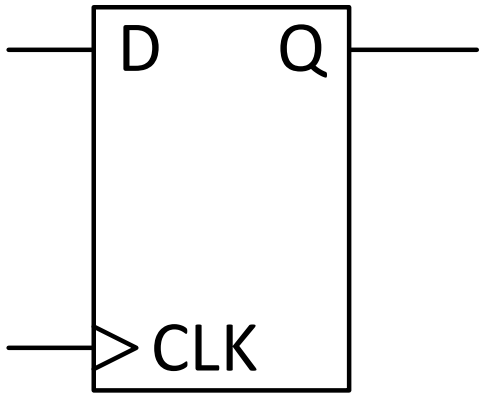
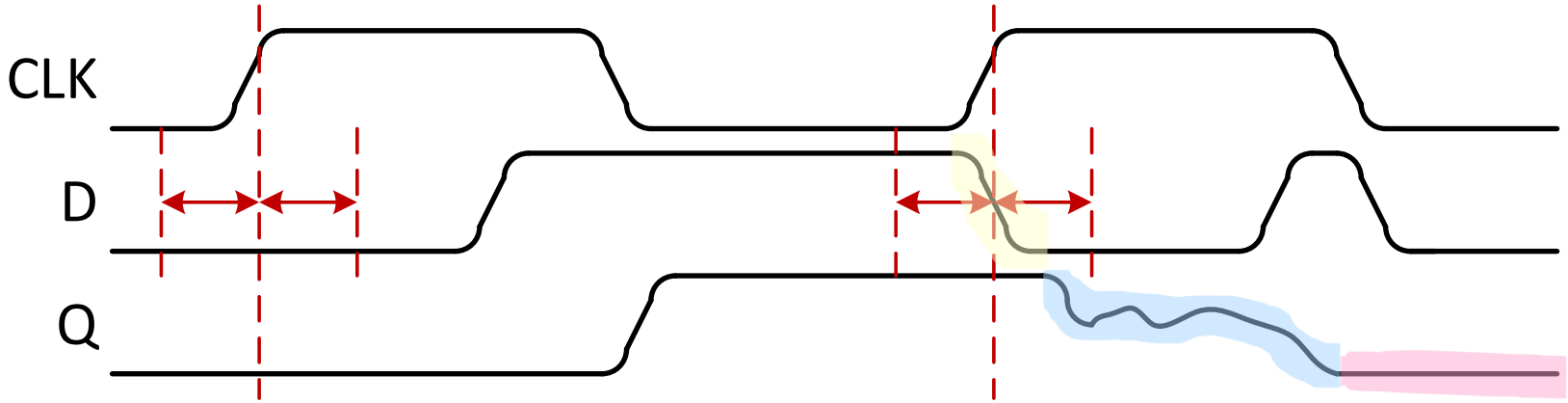
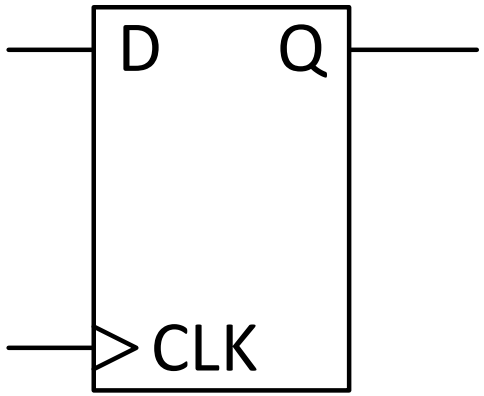
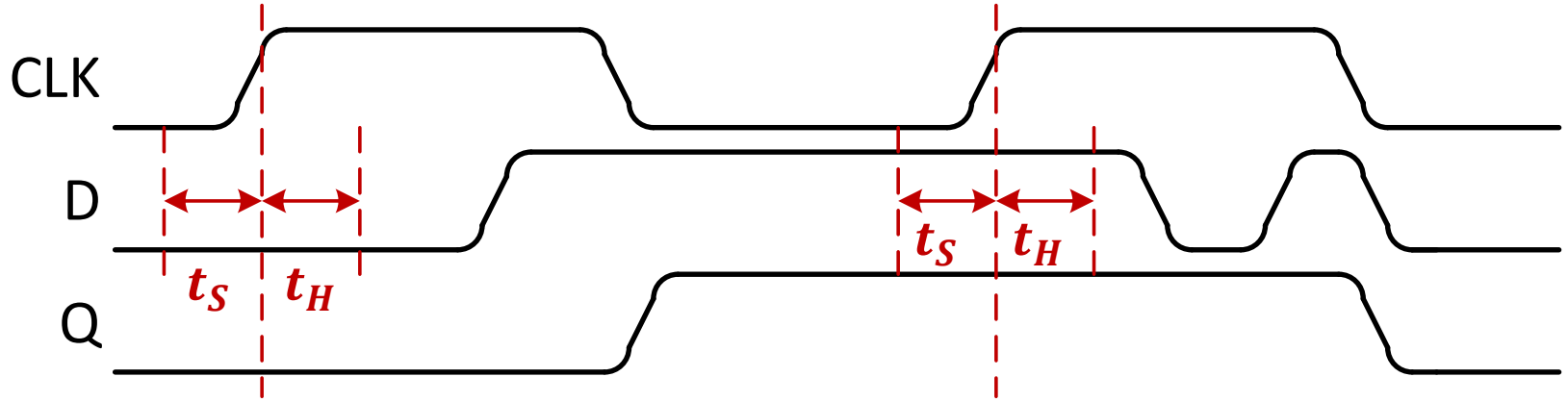




Timing constraints

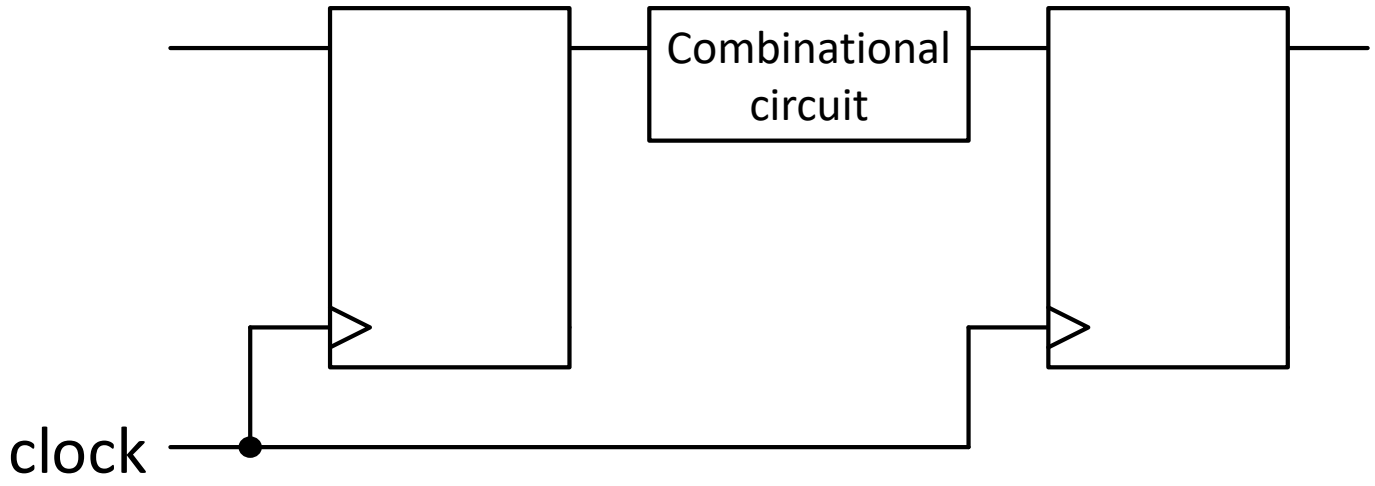
- Do you remember of registers and flip-flops?
  - The interval time in which the input must be stable
    - **Before** the triggering-edge of clock is called **setup time**: t_S
    - **After** the triggering-edge of clock is called **hold time** : t_H





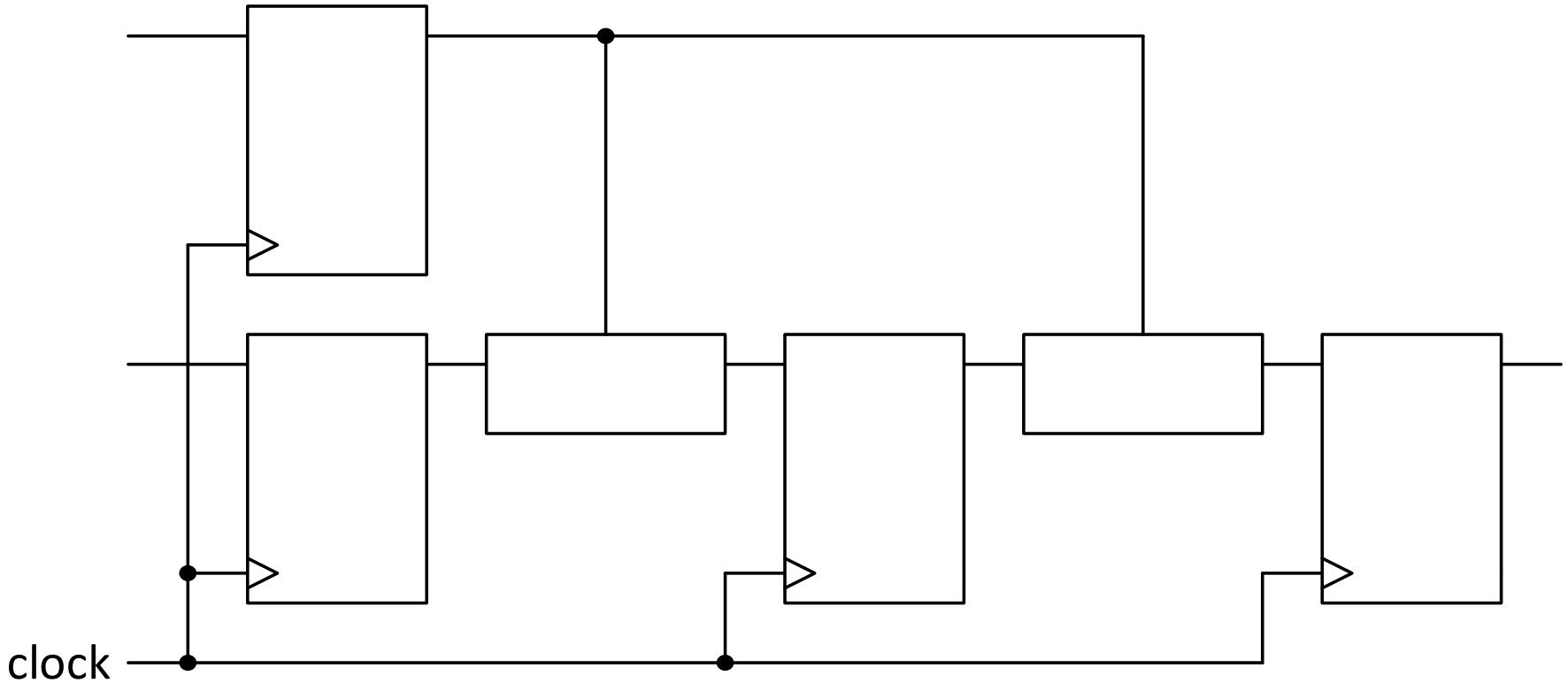
Timing constraints

- To check whether the conditions on setup and hold times are met, any digital synchronous circuit can be split in **register-to-register paths**
  - RTL representation of the circuit



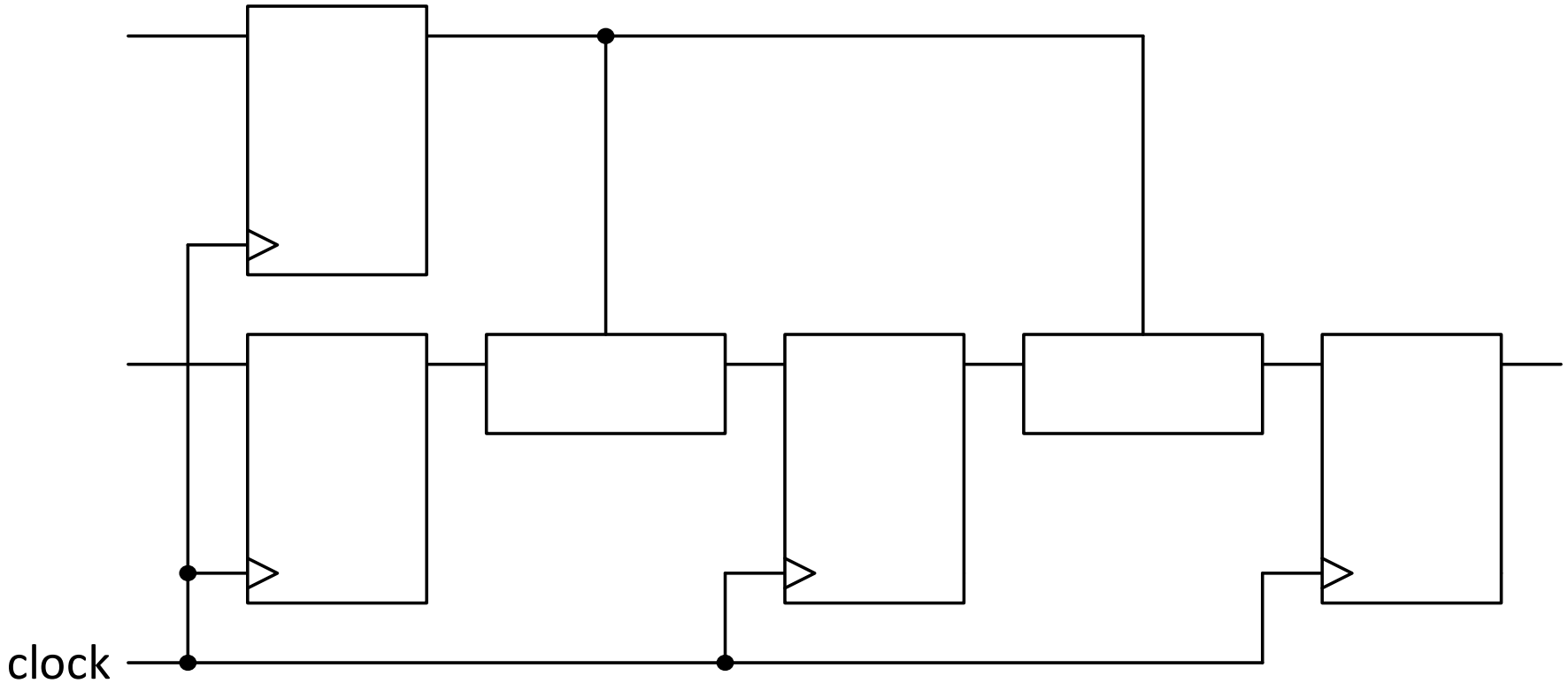
Register-to-register path

- An example
  - How many paths?



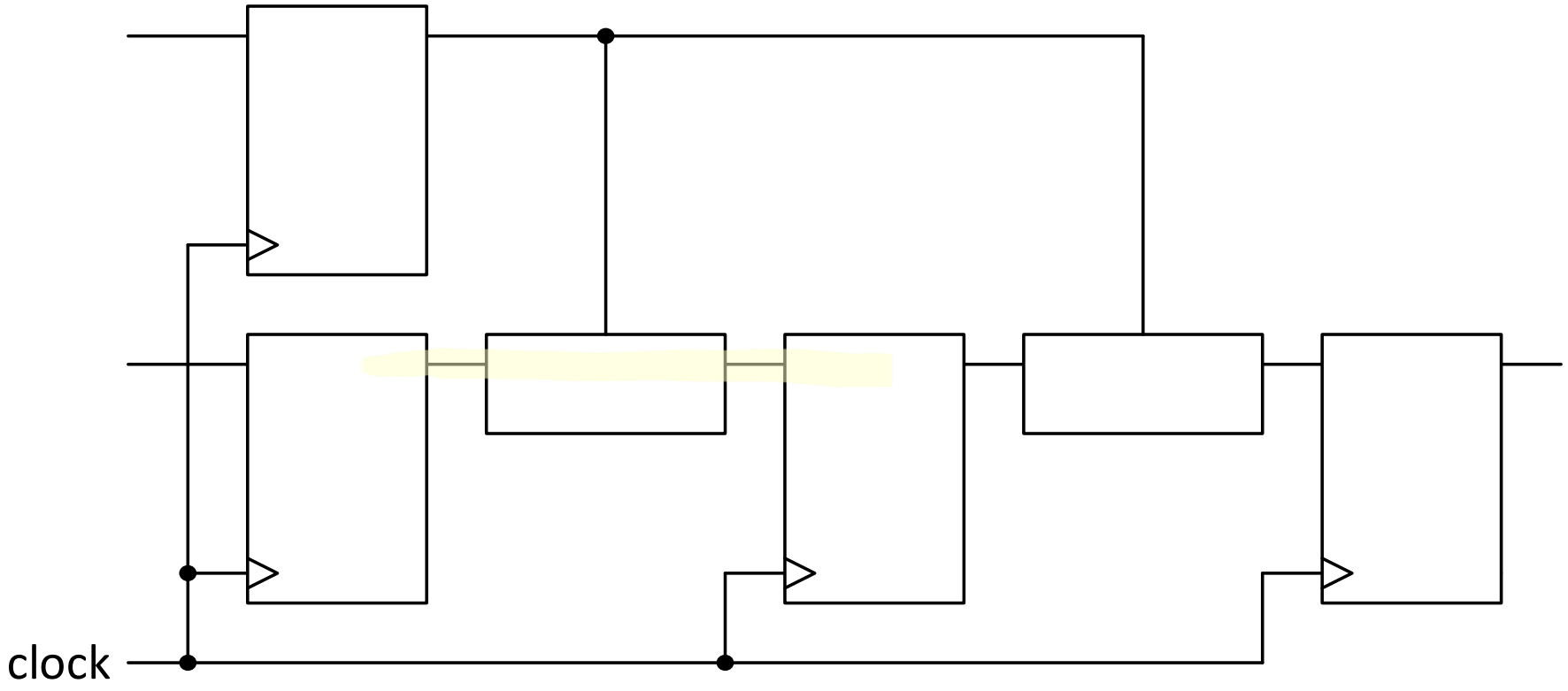
Register-to-register path

- An example
  - How many paths?
  - 4!



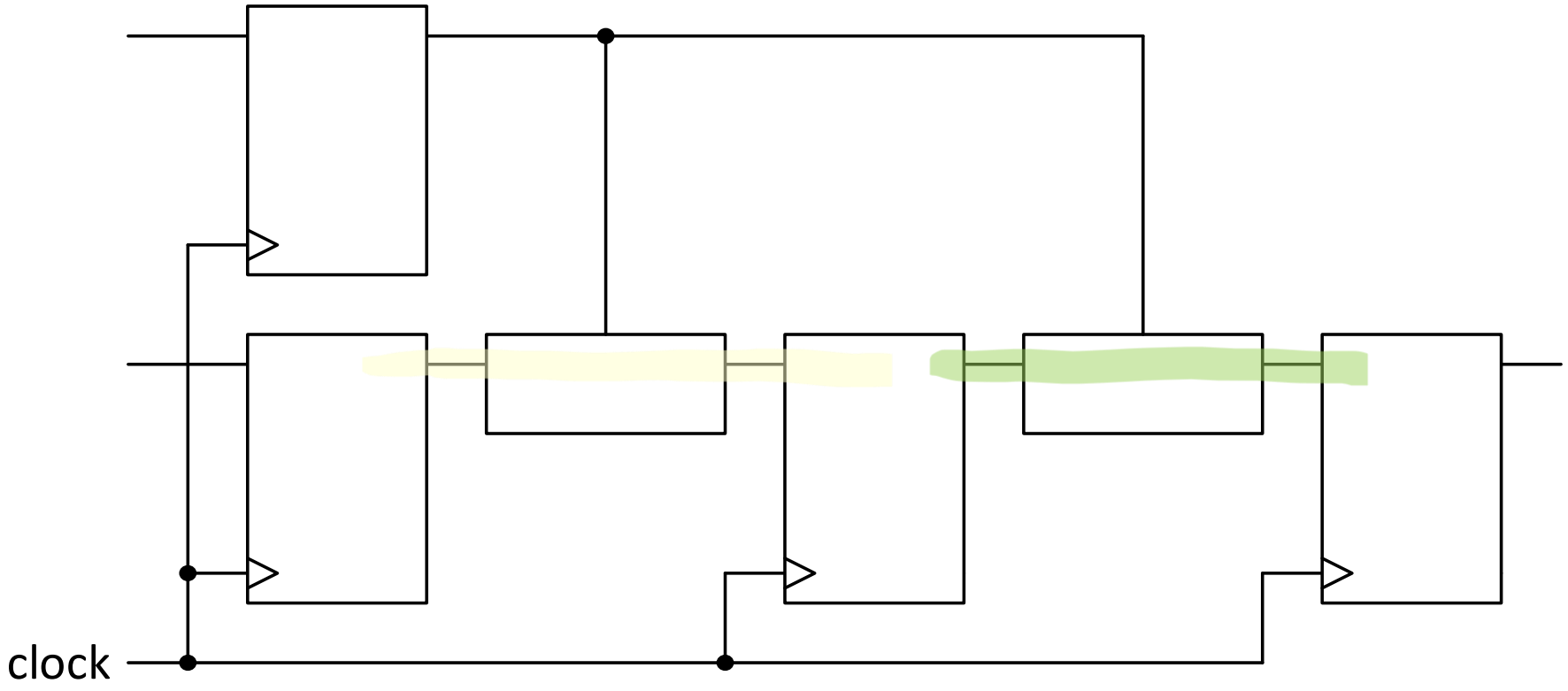
Register-to-register path

- An example
  - How many paths?
  - 4!
    - 1



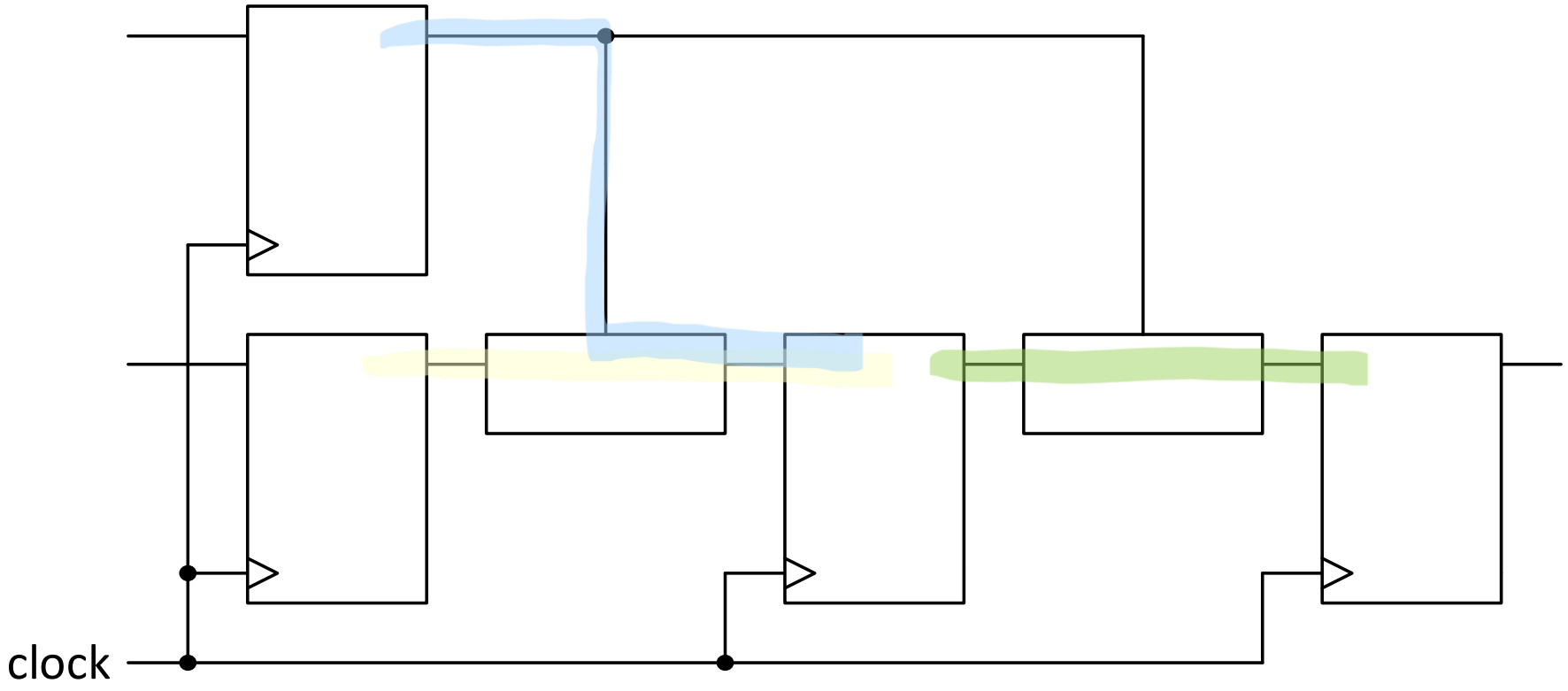
Register-to-register path

- An example
  - How many paths?
  - 4!
    - 2



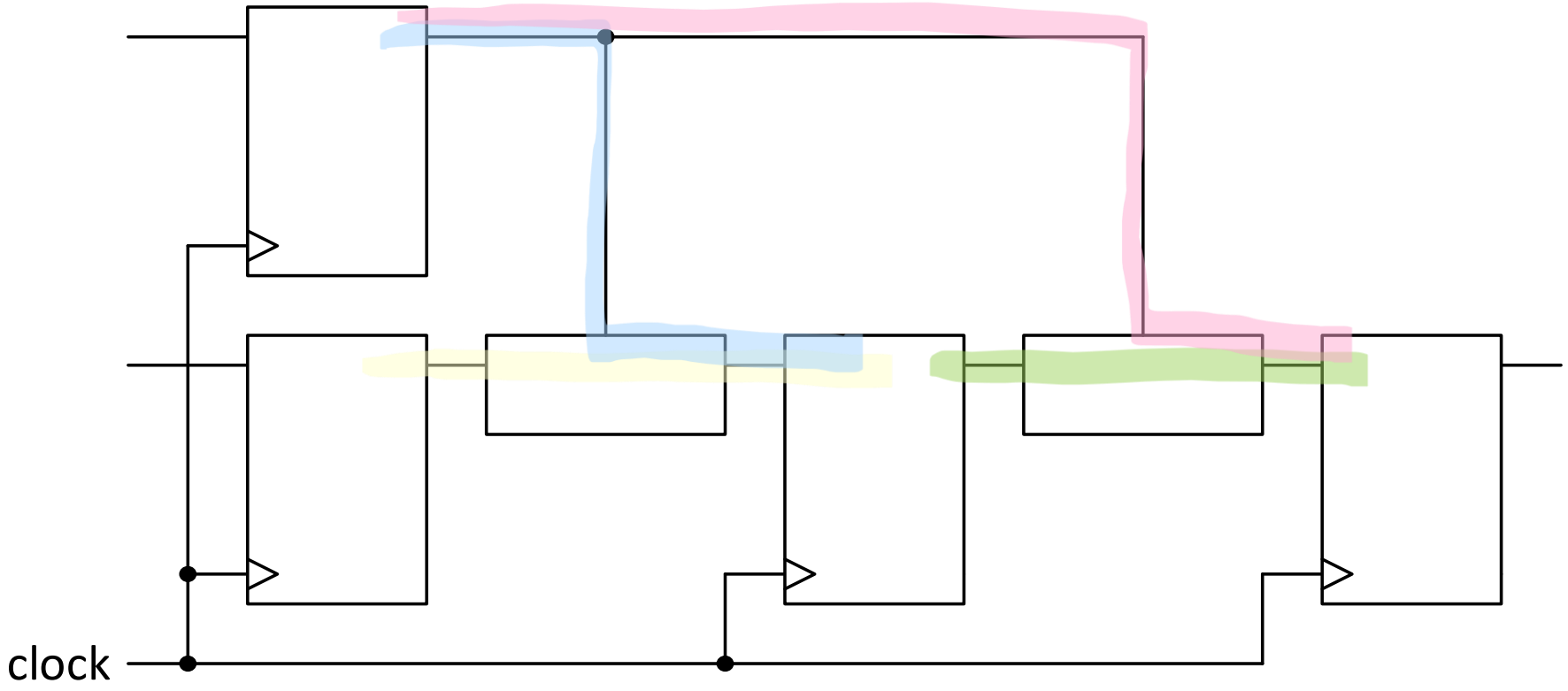
Register-to-register path

- An example
  - How many paths?
  - 4!
    - 3



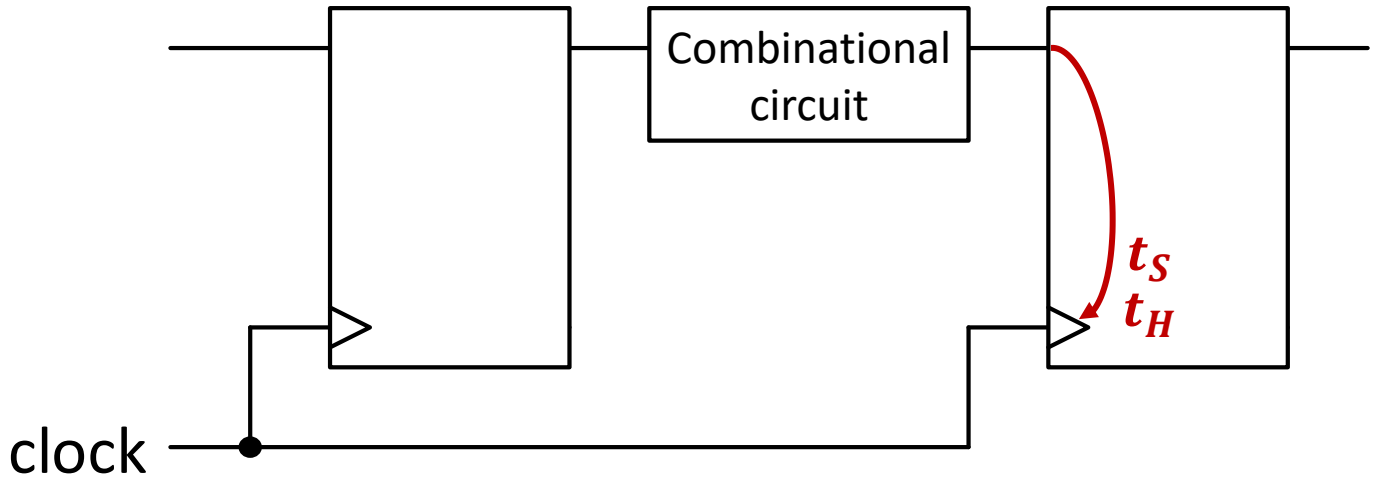
Register-to-register path

- An example
  - How many paths?
  - 4!
    - 4



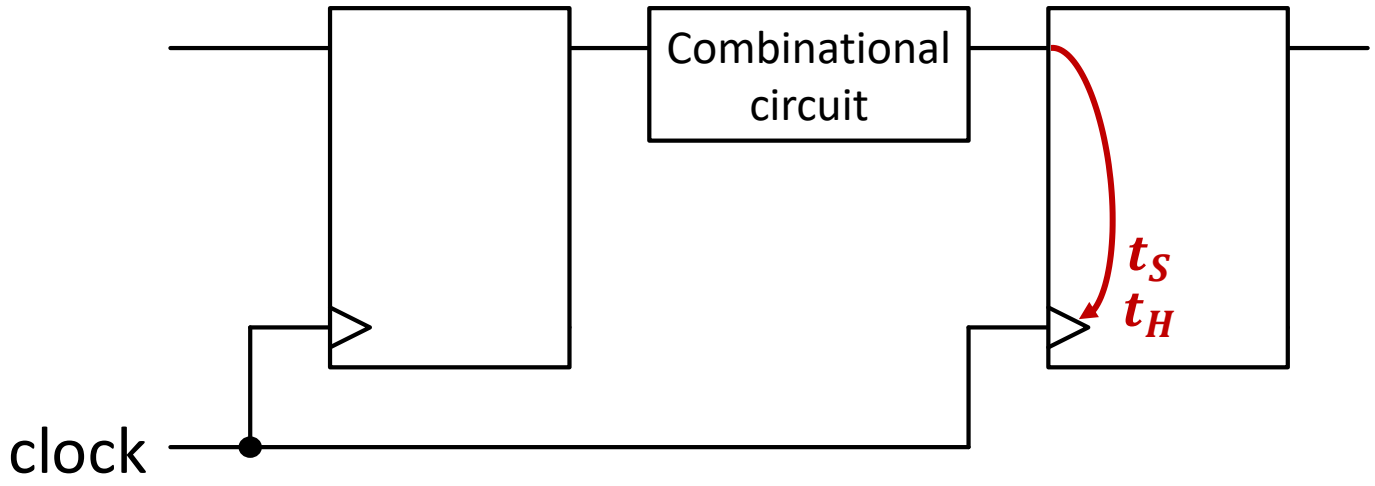
Register-to-Register path

- Setup and hold times refer to the path between input data and clock



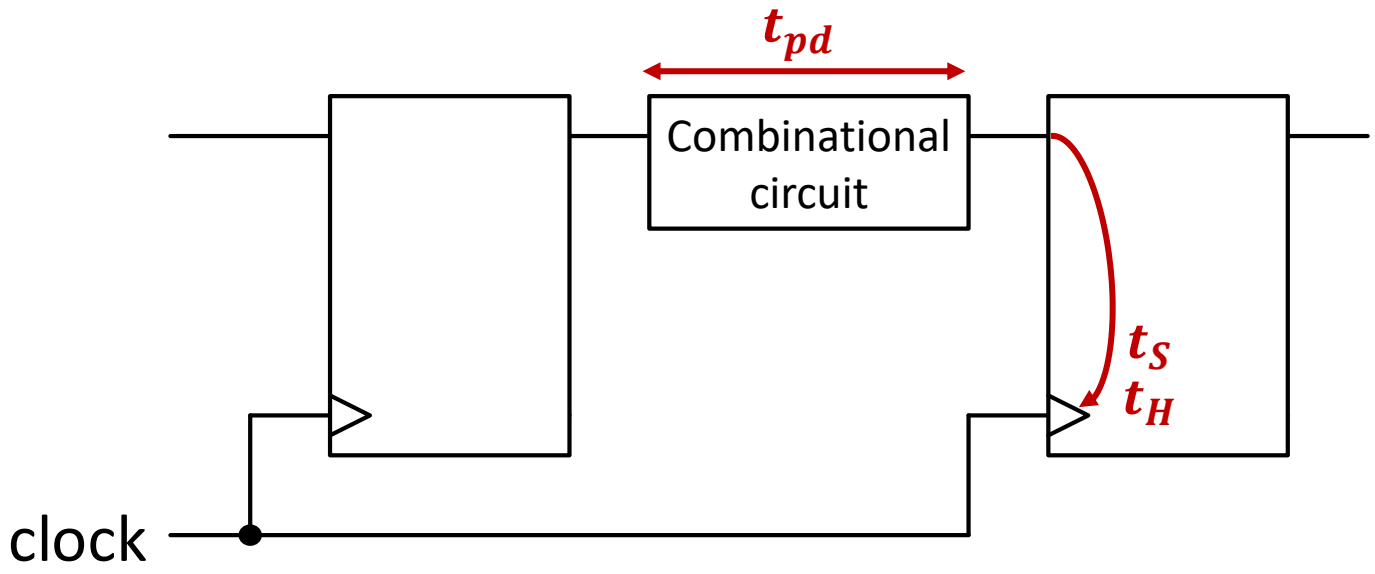
Register-to-Register path

- However, for this analysis, also other time intervals must also be considered



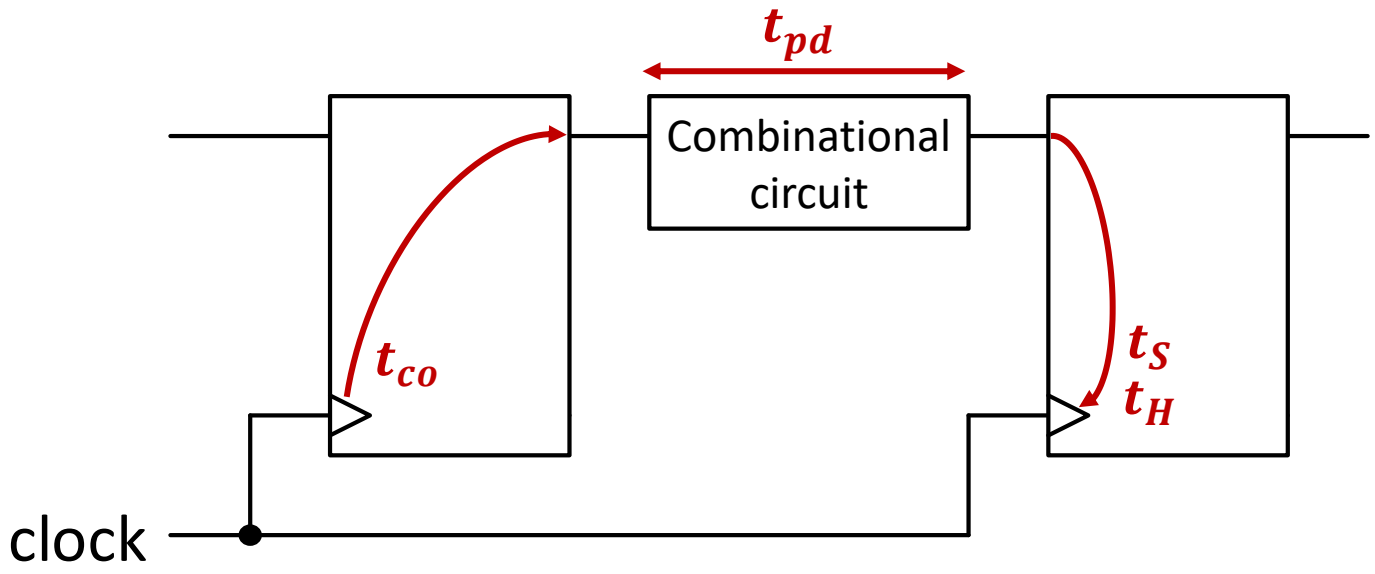
Register-to-Register path

- However, for this analysis, also other time intervals must also be considered
  - t_{pd} = **propagation delay** of **combinational** circuit between the registers



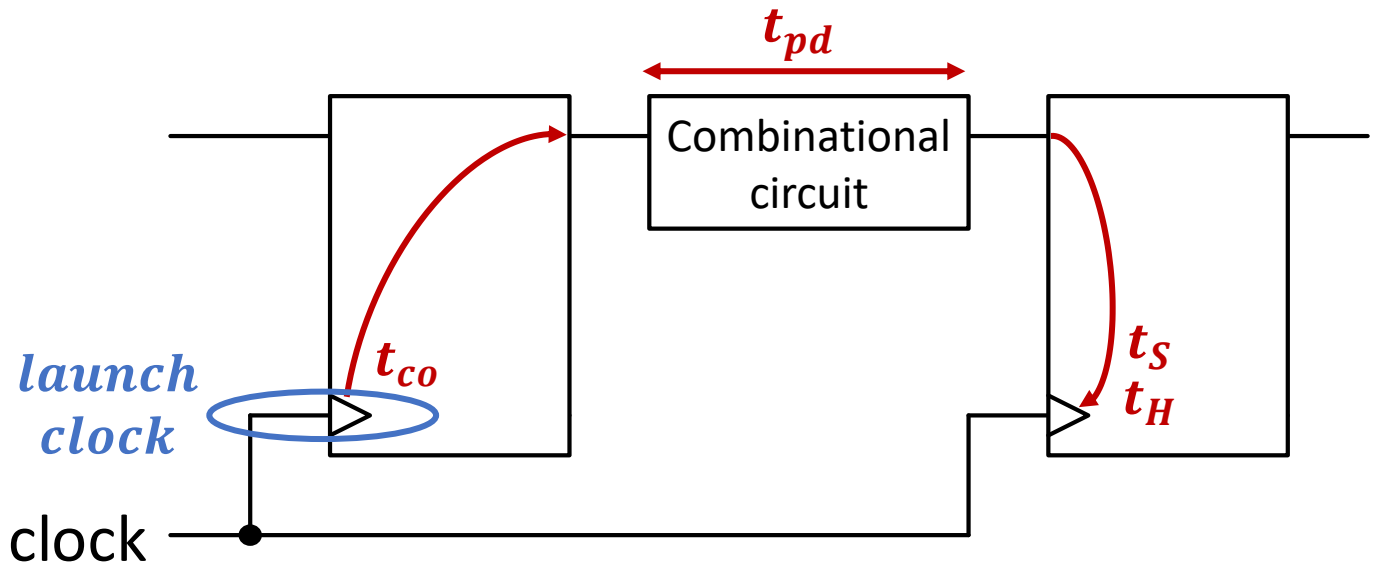
Register-to-Register path

- However, for this analysis, also other time intervals must also be considered
  - t_{co} = **clock-to-output time**, i.e. the time required to settle a valid output on an output pin after a clock transition



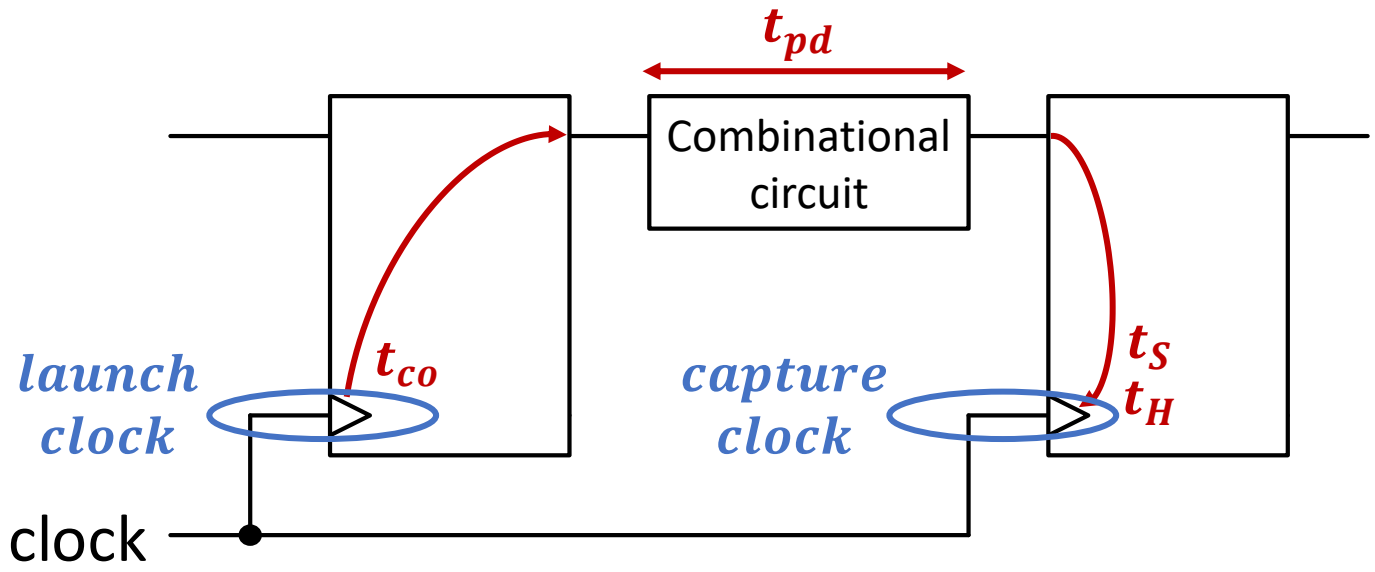
Register-to-Register path

- In addition
  - The source register is called the **launch register**, and the corresponding clock signal is called the **launch clock**



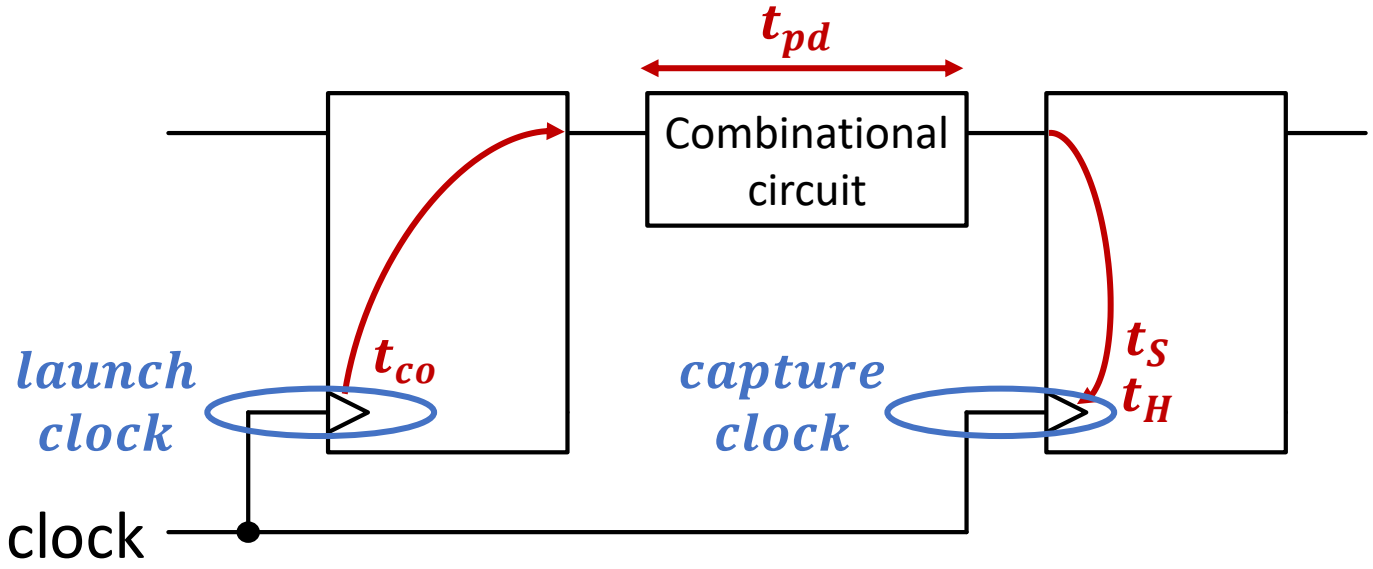
Register-to-Register path

- In addition
  - The destination register is called the **capture register**, and the corresponding clock signal is called the **capture clock**



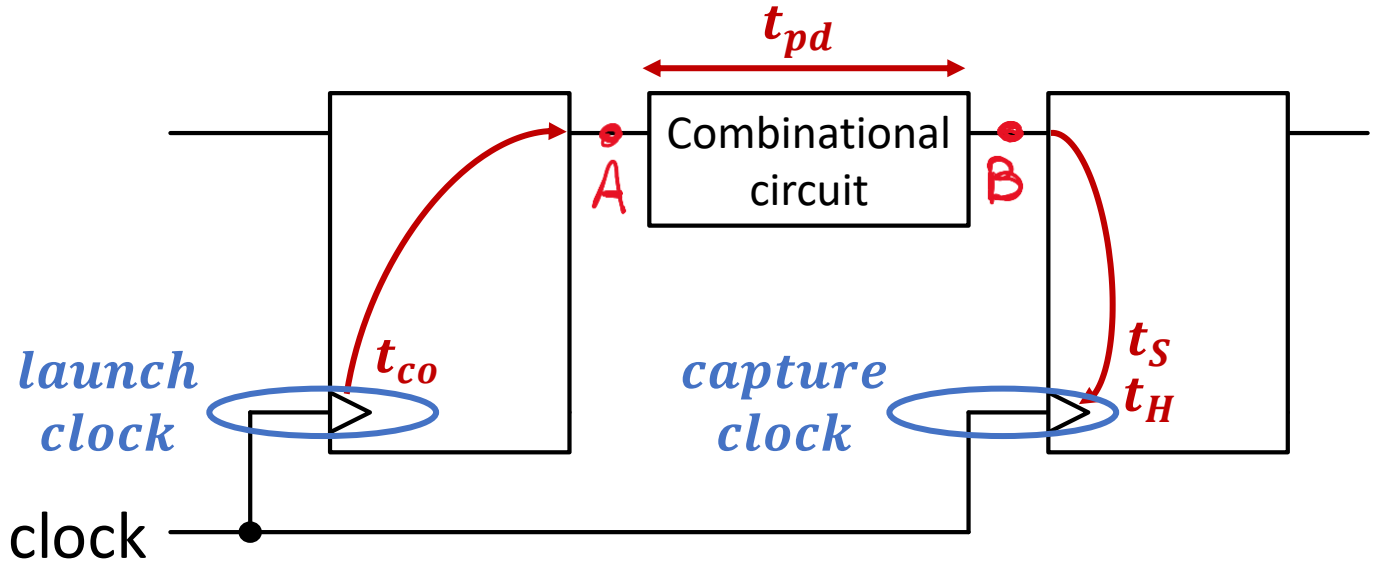
Register-to-Register path

- Ideally, the launch and capture clocks are the same signal with a **period T_{clk}**, but let's consider them as two distinct signals
  - It depends on the circuit manufacturing process
  - Trust me for a while

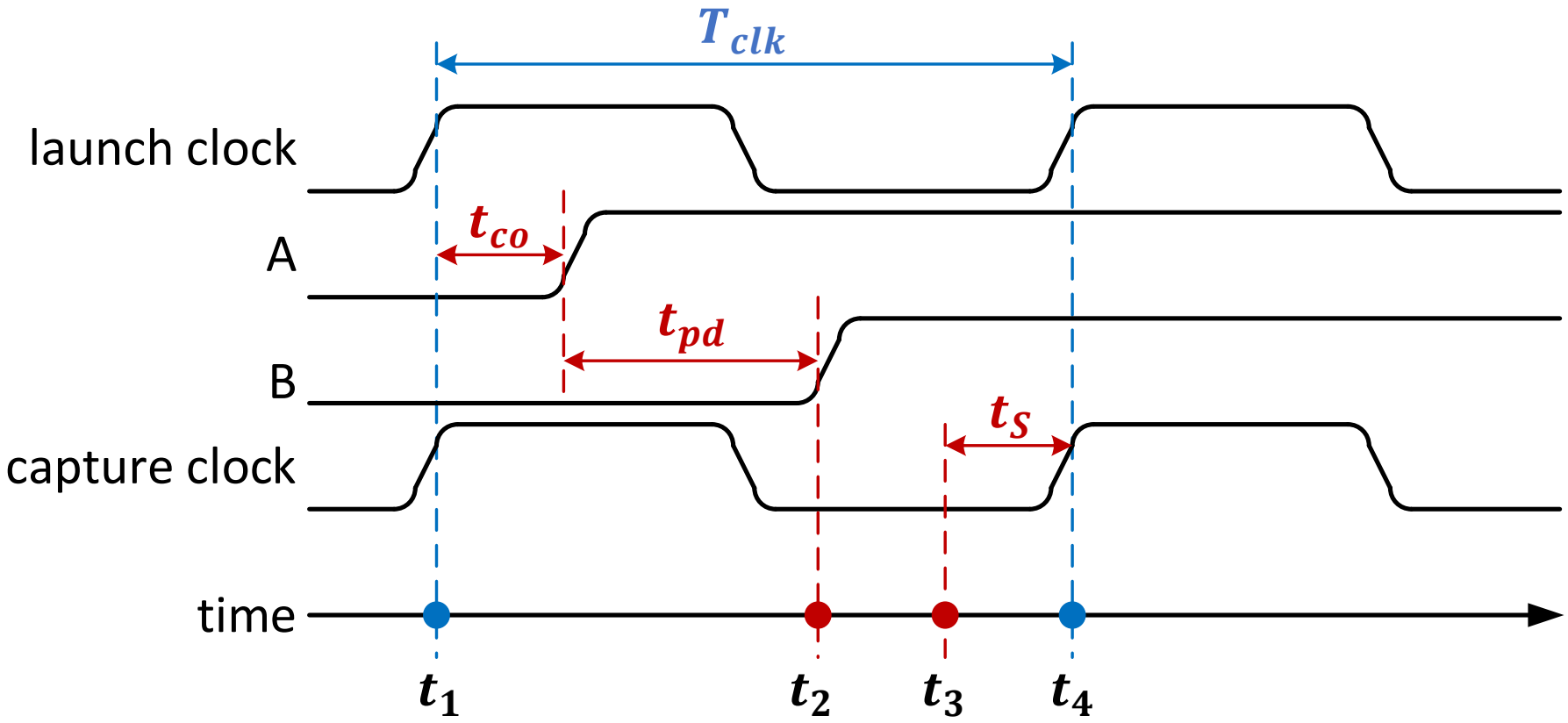


Timing constraints – Setup time

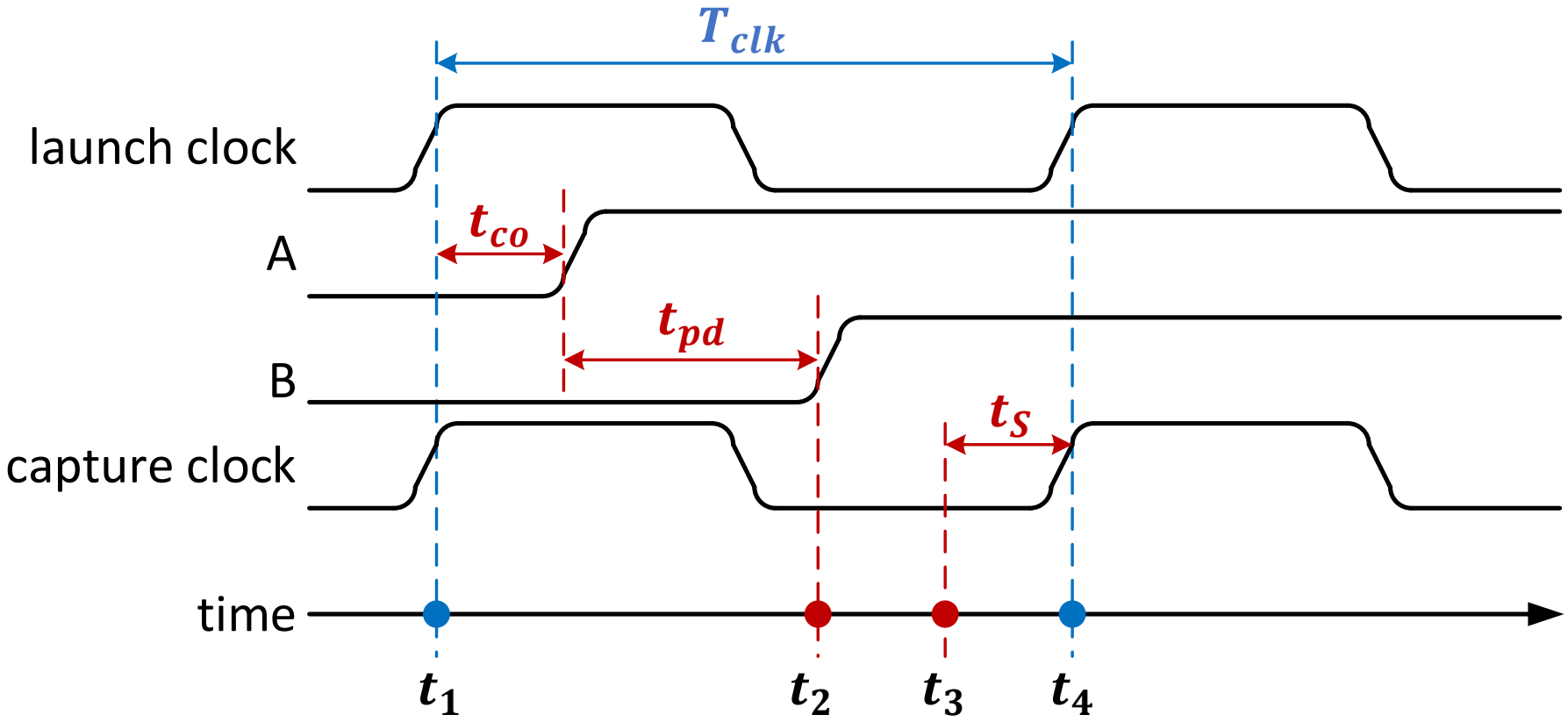
- Let's start by determining the timing constraint on the setup time
  - Let's define the points
    - **A** = the output pin of the launch register
    - **B** = the input pin of the capture register



Timing constraints – Setup time

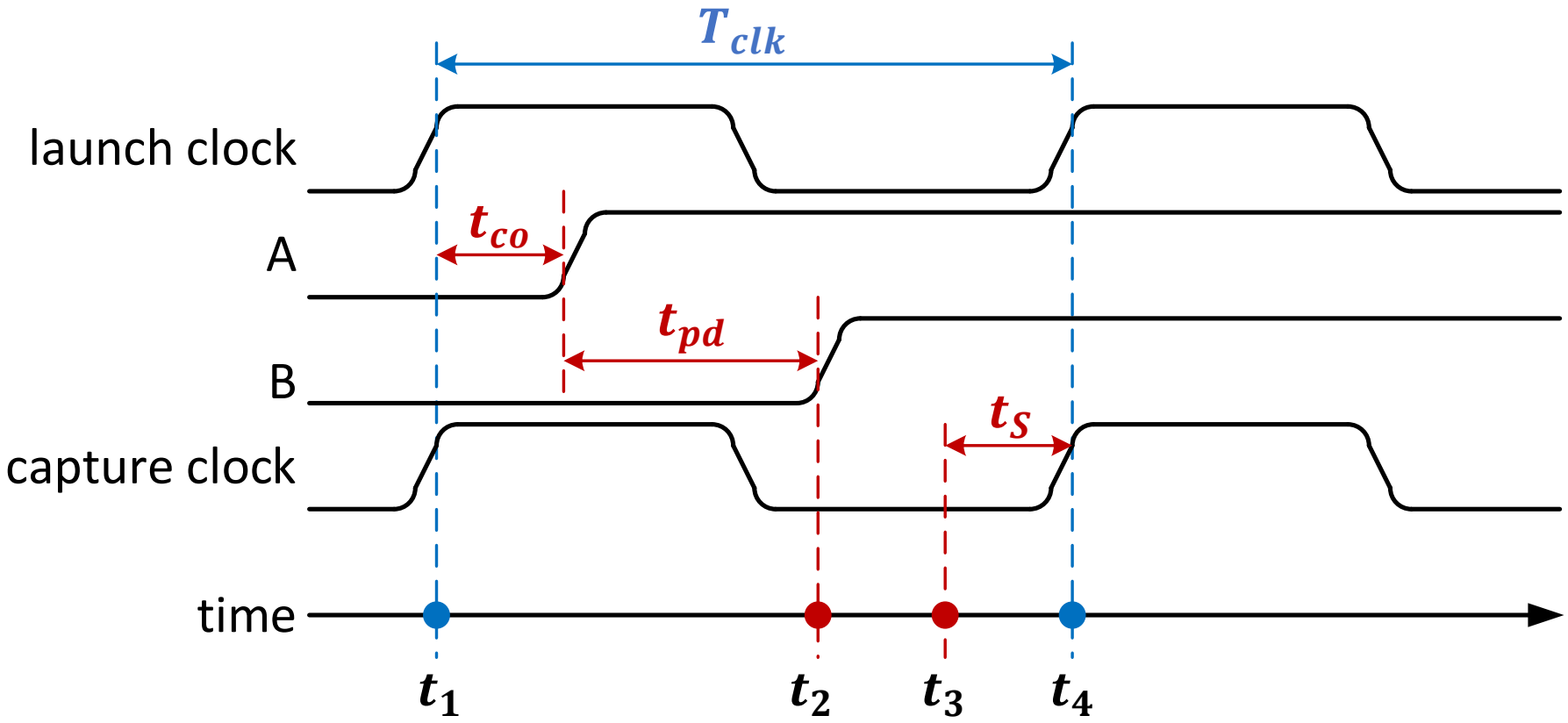


Timing constraints – Setup time



If $t_2 > t_3$, the change of input to the capture register (B) falls in the setup time, so …

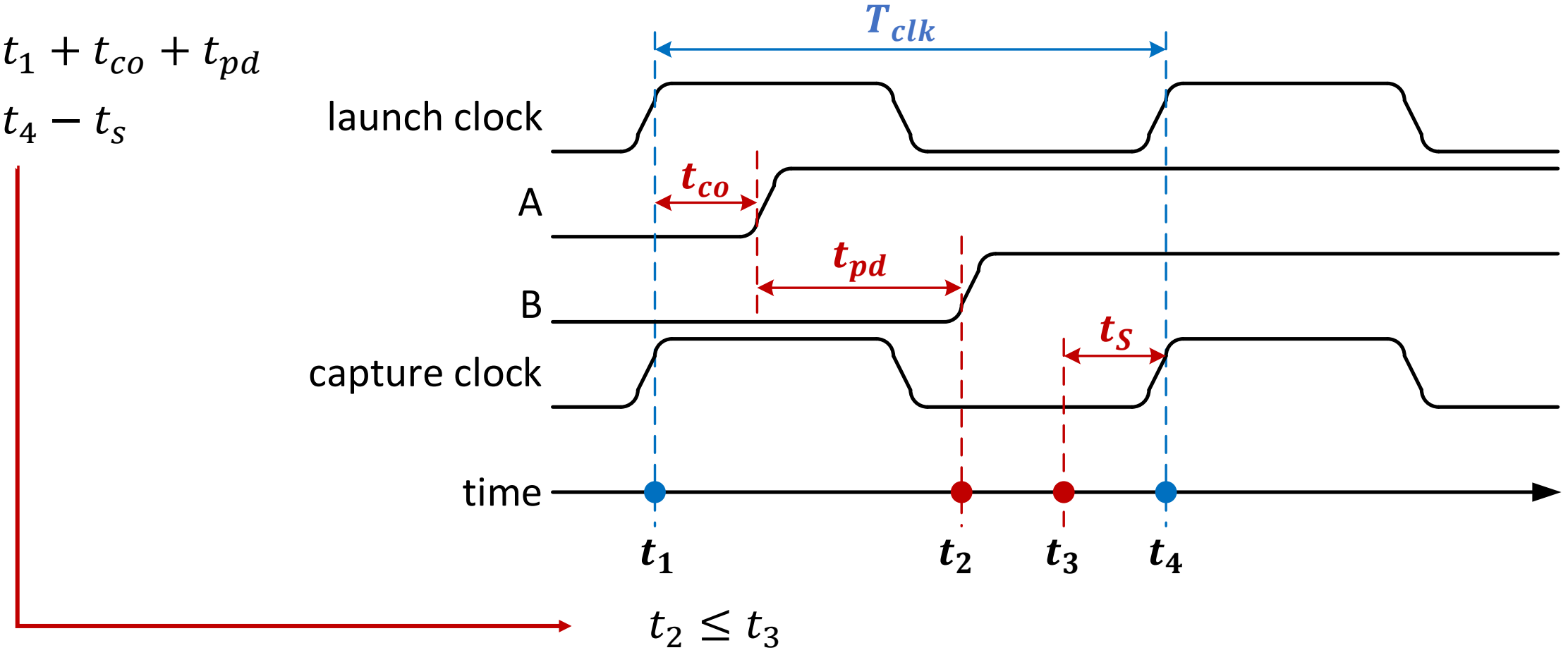
Timing constraints – Setup time



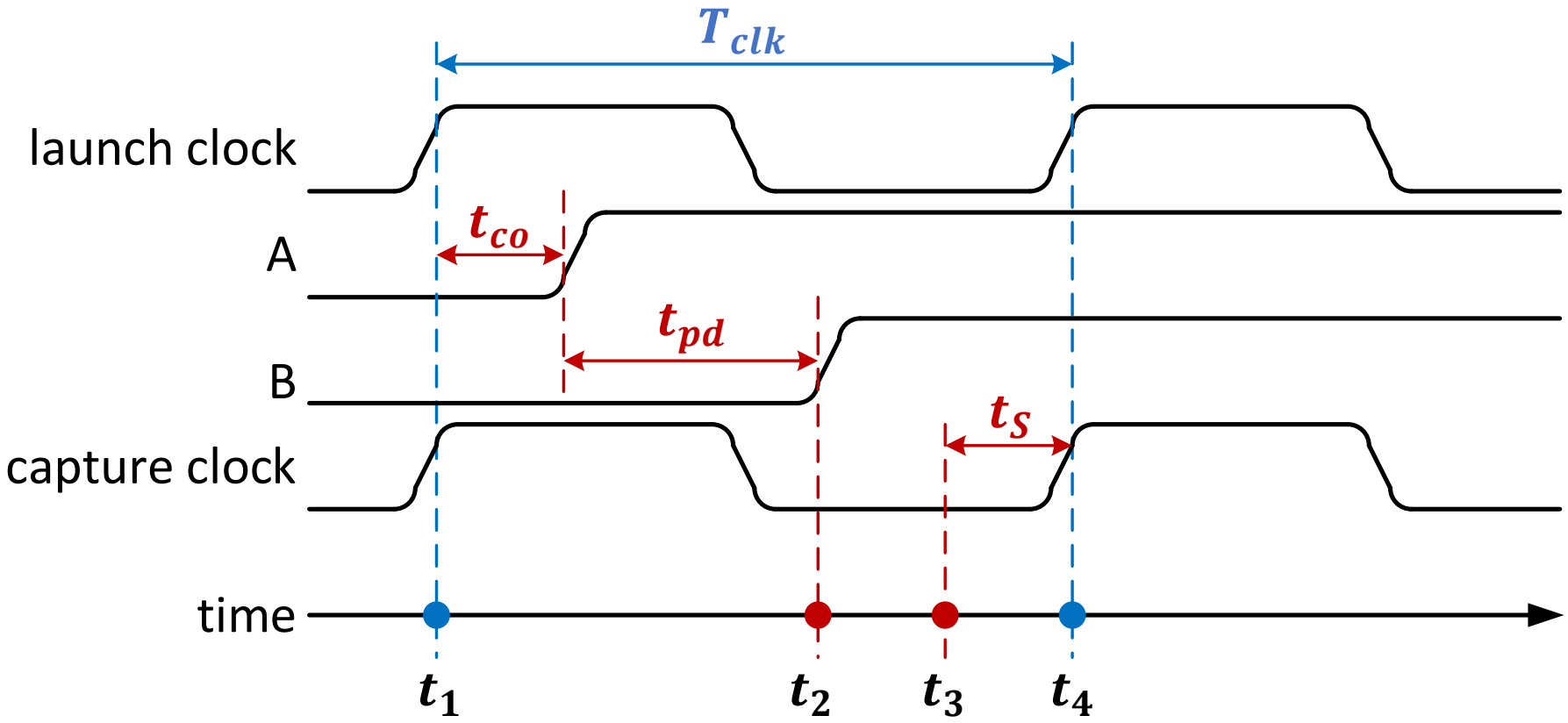
$$t_2 \leq t_3$$

Timing constraints – Setup time

- $t_2 = t_1 + t_{co} + t_{pd}$
- $t_3 = t_4 - t_s$



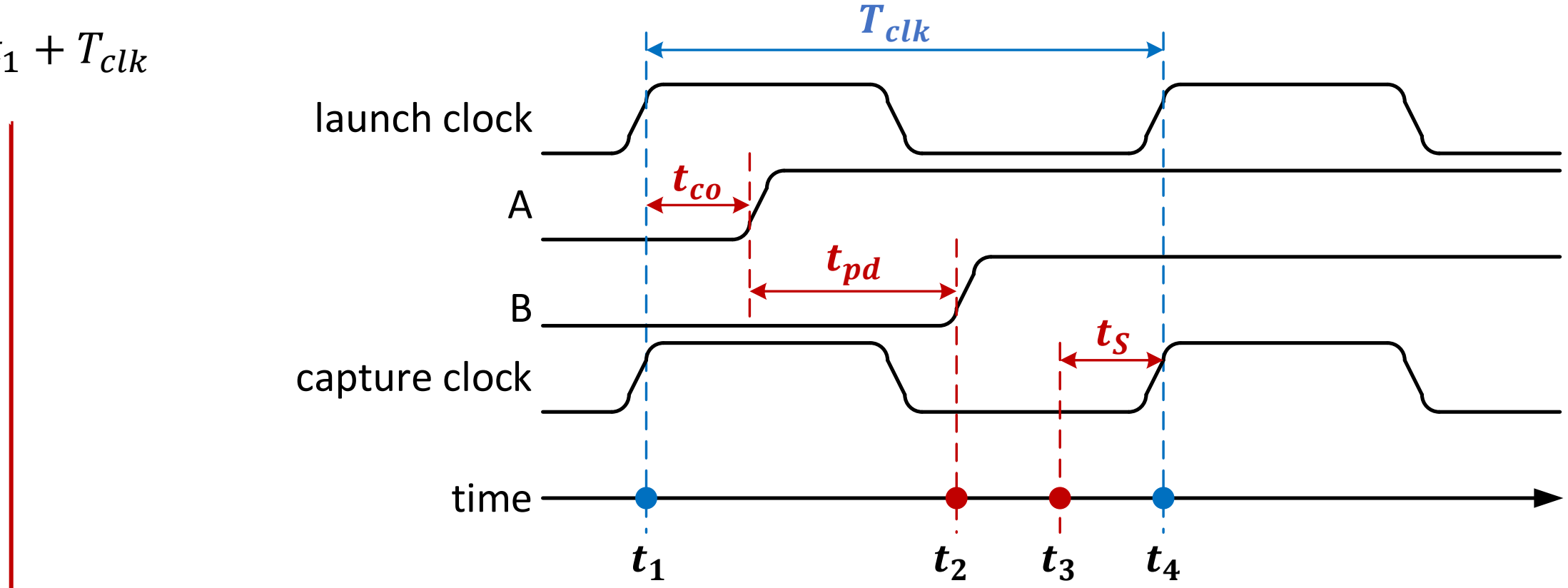
Timing constraints – Setup time



$$t_1 + t_{co} + t_{pd} \leq t_4 - t_s$$

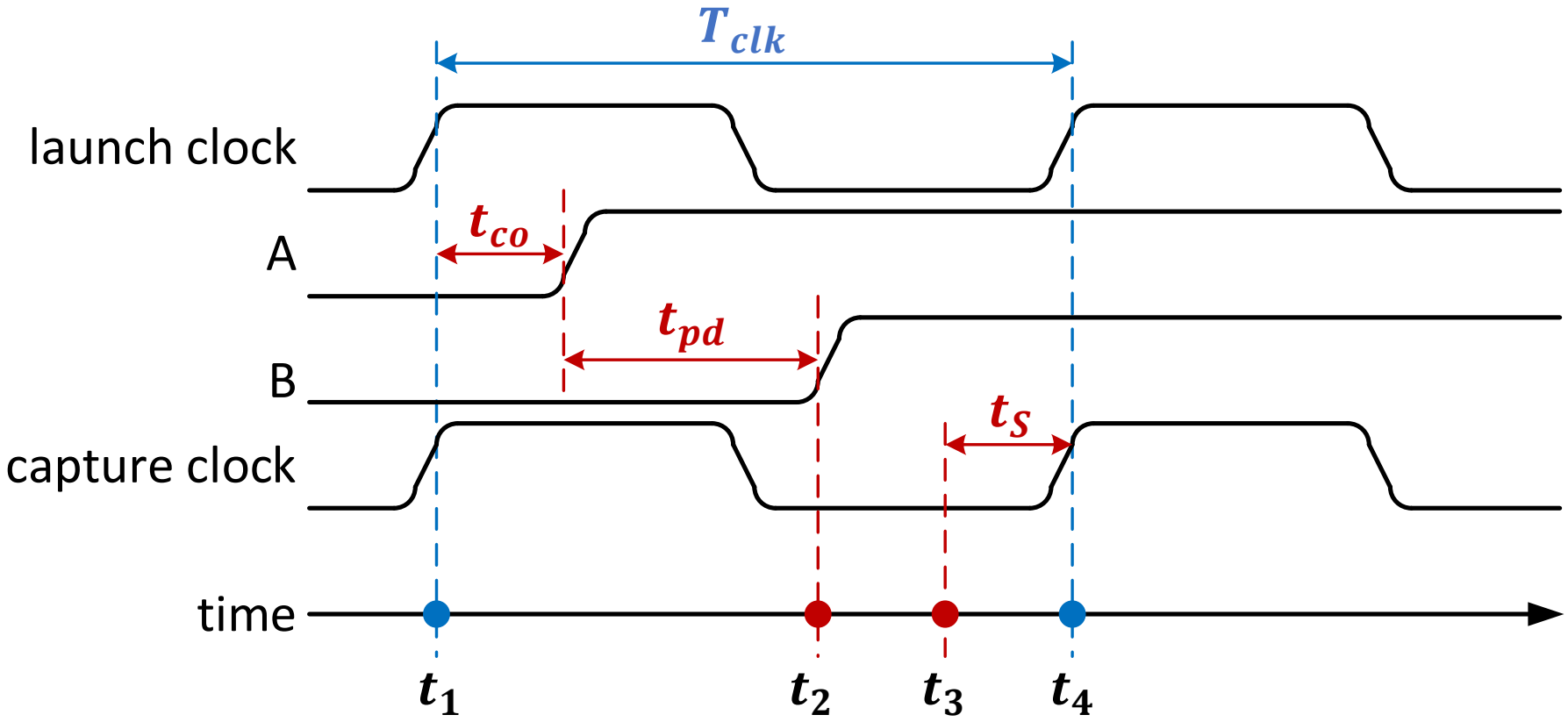
Timing constraints – Setup time

- $t_4 = t_1 + T_{clk}$



$$t_1 + t_{co} + t_{pd} \leq t_4 - t_s$$

Timing constraints – Setup time



$$t_1 + t_{co} + t_{pd} \leq t_1 + T_{clk} - t_s$$

Timing constraints – Setup time

$$t_1 + t_{co} + t_{pd} \leq t_1 + T_{clk} - t_S$$

Timing constraints – Setup time

$$t_1 + t_{co} + t_{pd} \leq t_1 + T_{clk} - t_S$$

Timing constraints – Setup time

$$t_1 + t_{co} + t_{pd} \leq t_1 + T_{clk} - t_S \quad \rightarrow \quad t_S + t_{co} + t_{pd} \leq T_{clk}$$

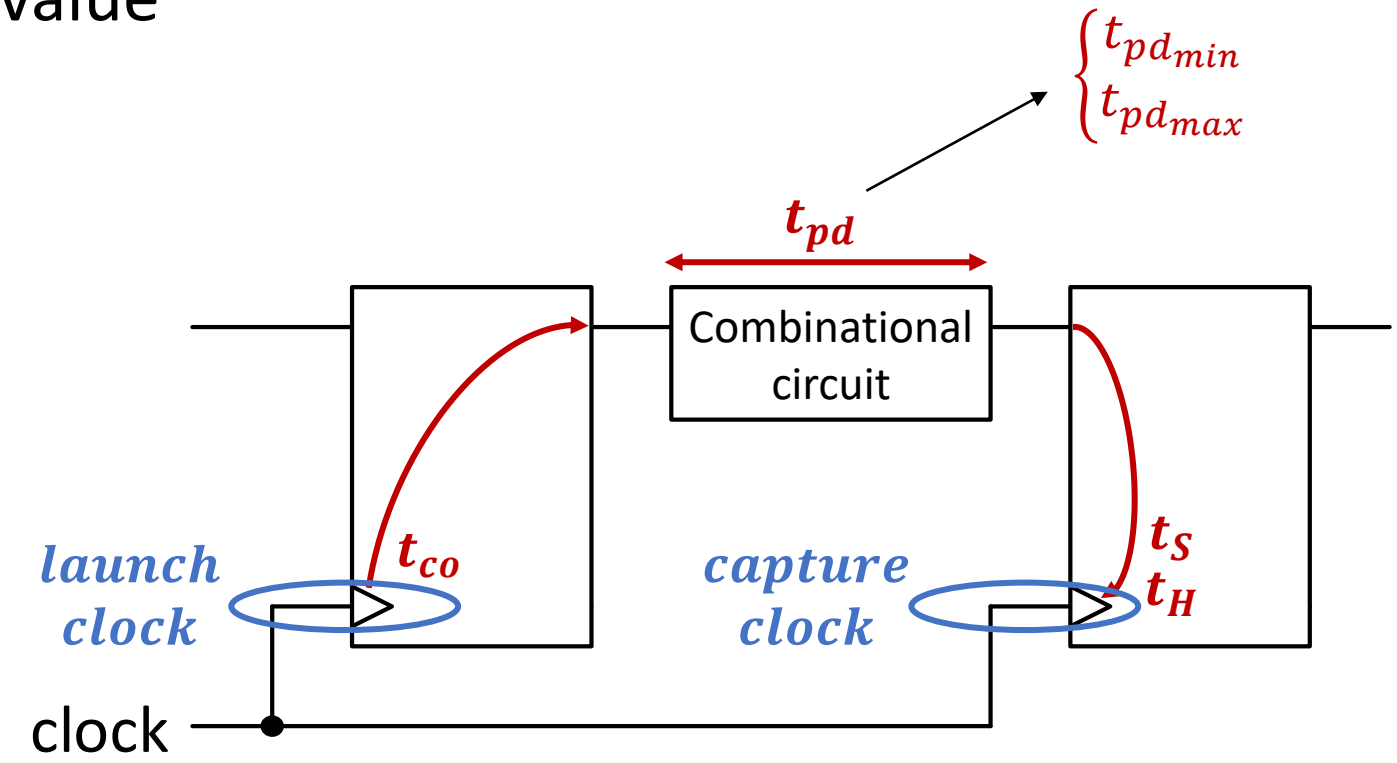
Timing constraints – Setup time

$$t_1 + t_{co} + t_{pd} \leq t_1 + T_{clk} - t_S \quad \rightarrow \quad t_S + t_{co} + t_{pd} \leq T_{clk}$$

$$T_{clk} \geq t_S + t_{co} + t_{pd}$$

Timing constraints – Setup time

- To be honest, the propagation delay can be characterized by a minimum and maximum value
  - $t_{pd_{max}}$
  - $t_{pd_{min}}$



Timing constraints – Setup time

- $T_{clk} \geq t_S + t_{co} + t_{pd}$
  - $t_{pd}\ ?=?\ \begin{cases} t_{pd_{min}} \\ t_{pd_{max}} \end{cases}$

Timing constraints – Setup time

- $T_{clk} \geq t_S + t_{co} + t_{pd}$
  - $t_{pd}\,?=?\begin{cases} t_{pd_{min}} \\ t_{pd_{max}} \end{cases}$ → Worst case!

Timing constraints – Setup time

- $T_{clk} \geq t_S + t_{co} + t_{pd}$
  - $t_{pd}\,? = ? \begin{cases} t_{pd_{min}} \\ t_{pd_{max}} \end{cases}$ → Worst case!
  - Why the worst case ($t_{pd_{\max}}$) ?

Timing constraints – Setup time

- $T_{clk} \geq t_S + t_{co} + t_{pd}$
  - $t_{pd}\ ?\ =\ ?\ \begin{cases} t_{pd_{min}} \\ t_{pd_{max}} \end{cases}$ → Worst case!
  - Why the worst case ($t_{pd_{\max}}$) ?
  - Because if the circuit works in the worst conditions, for sure it works also in the other conditions: typical, best

Timing constraints – Setup time

- Summarizing, the timing constraint on the setup time (t_S) is

$$T_{clk} \geq t_S + t_{co} + t_{pd_{max}}$$

Timing constraints – Setup time and clock frequency

- Summarizing, the timing constraint on the setup time (t_S) is

$$T_{clk} \geq t_S + t_{co} + t_{pd_{max}}$$

- The clock frequency is $f_{clk} = \frac{1}{T_{clk}}$, so the clock frequency must satisfy

$$f_{clk} \leq \frac{1}{t_S + t_{co} + t_{pd_{max}}}$$

Timing constraints – Setup time and clock frequency

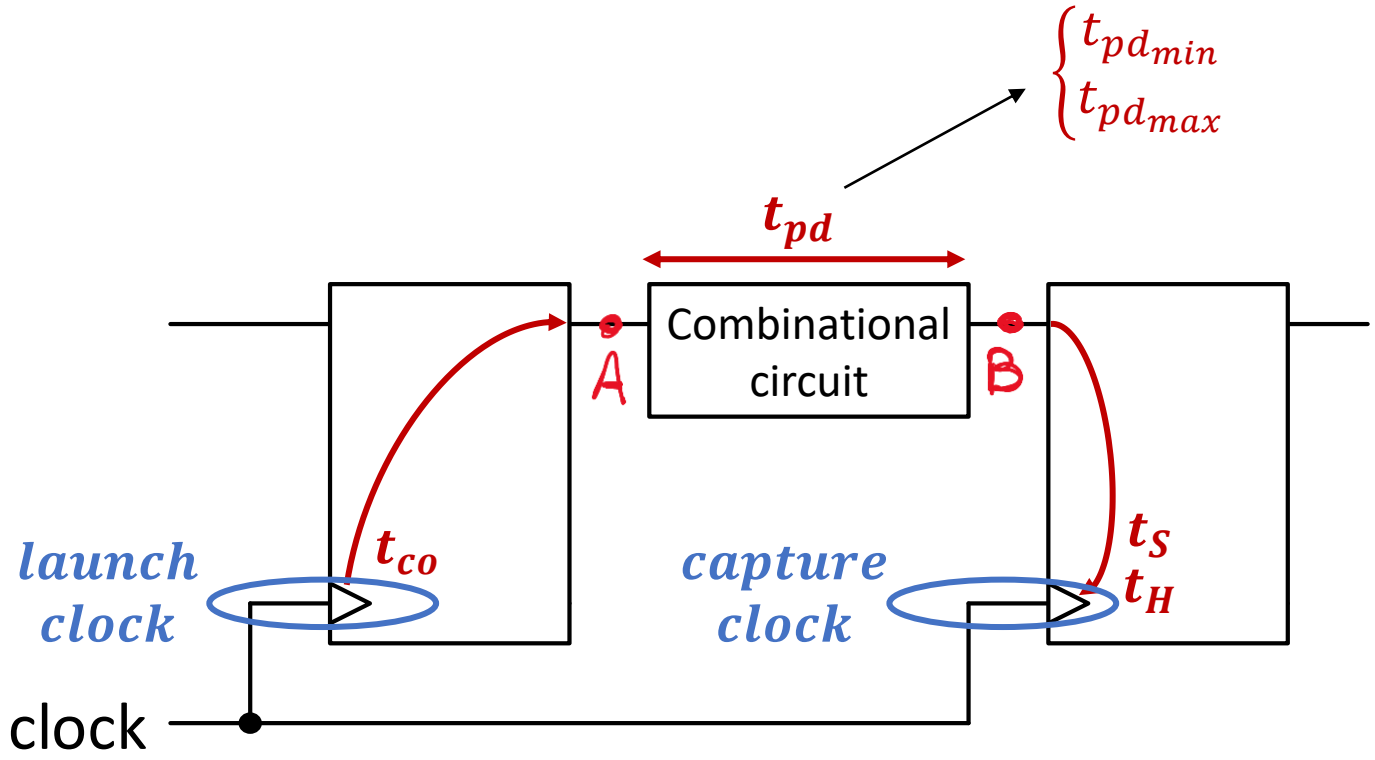
- $f_{clk} \leq \frac{1}{t_S + t_{co} + t_{pd_{max}}}$

- Therefore, the maximum frequency is:

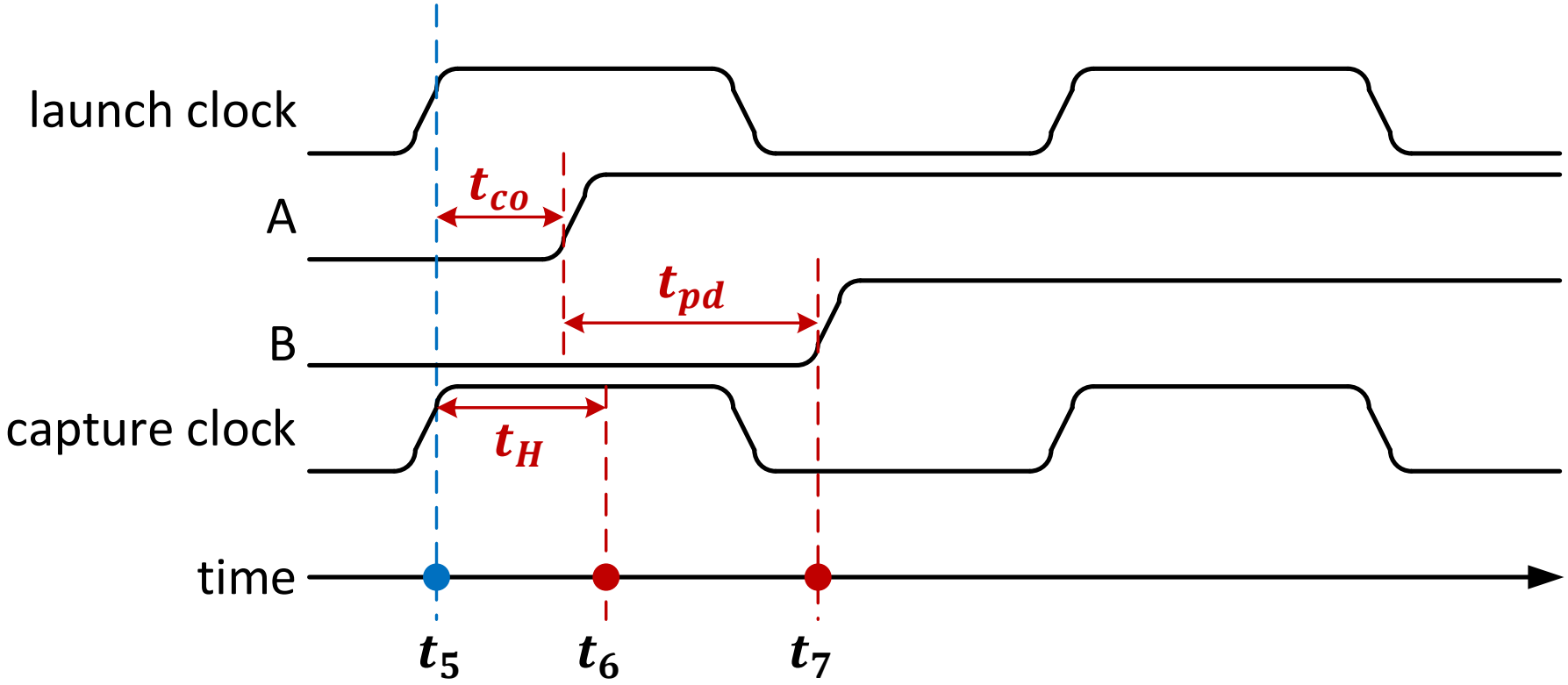
$$f_{clk_{max}} = \frac{1}{t_S + t_{co} + t_{pd_{max}}}$$

Timing constraints – Hold time

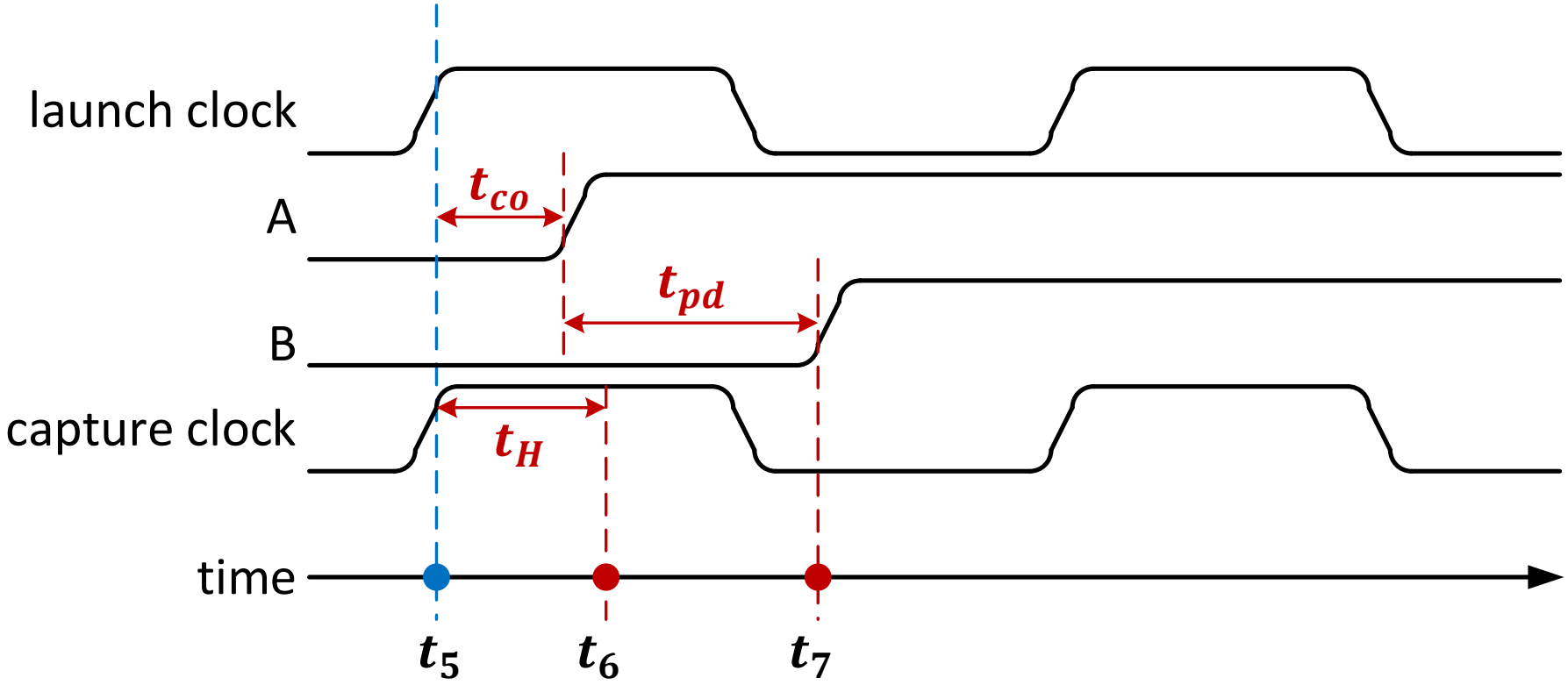
- Now let's move to the timing constraint on the hold time



Timing constraints – Hold time

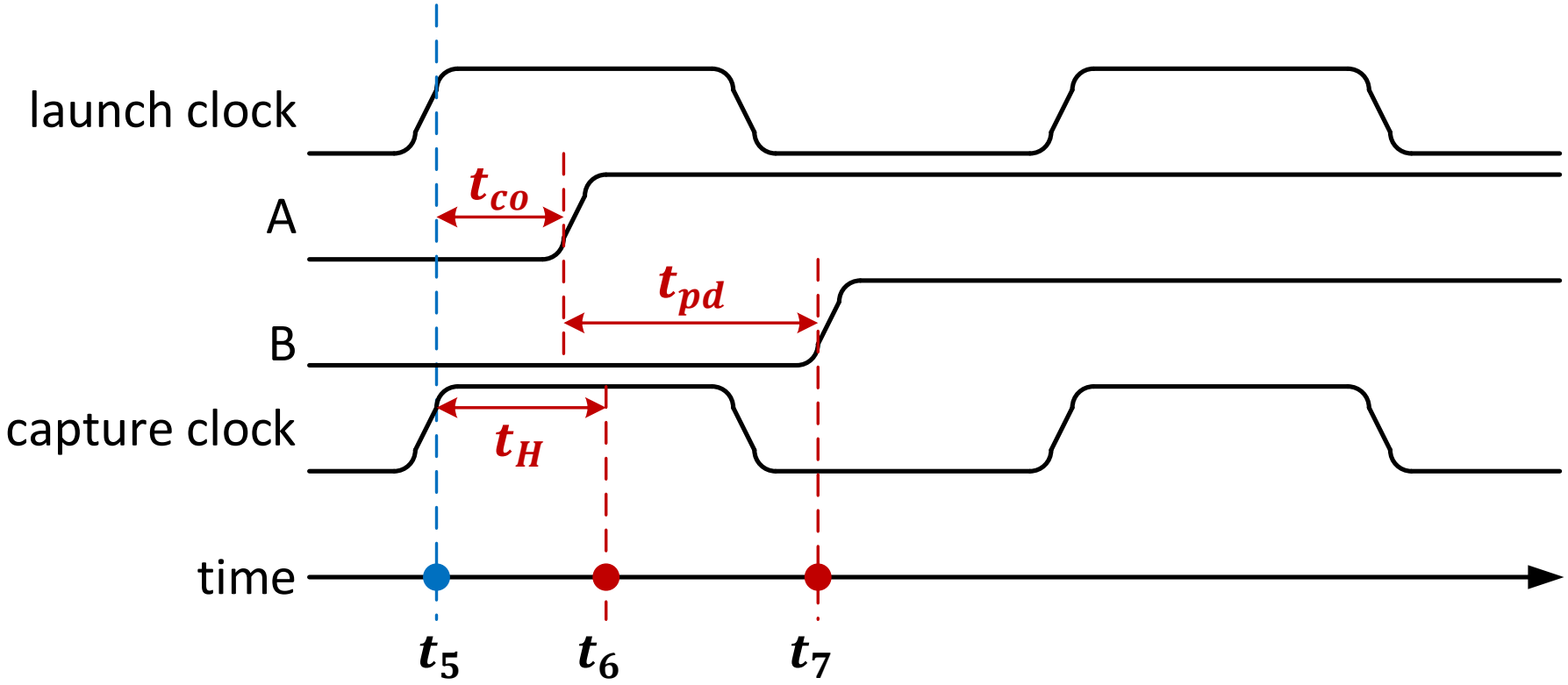


Timing constraints – Hold time



If $t_7 < t_6$, the change of input to the capture register (B) falls in the hold time, so …

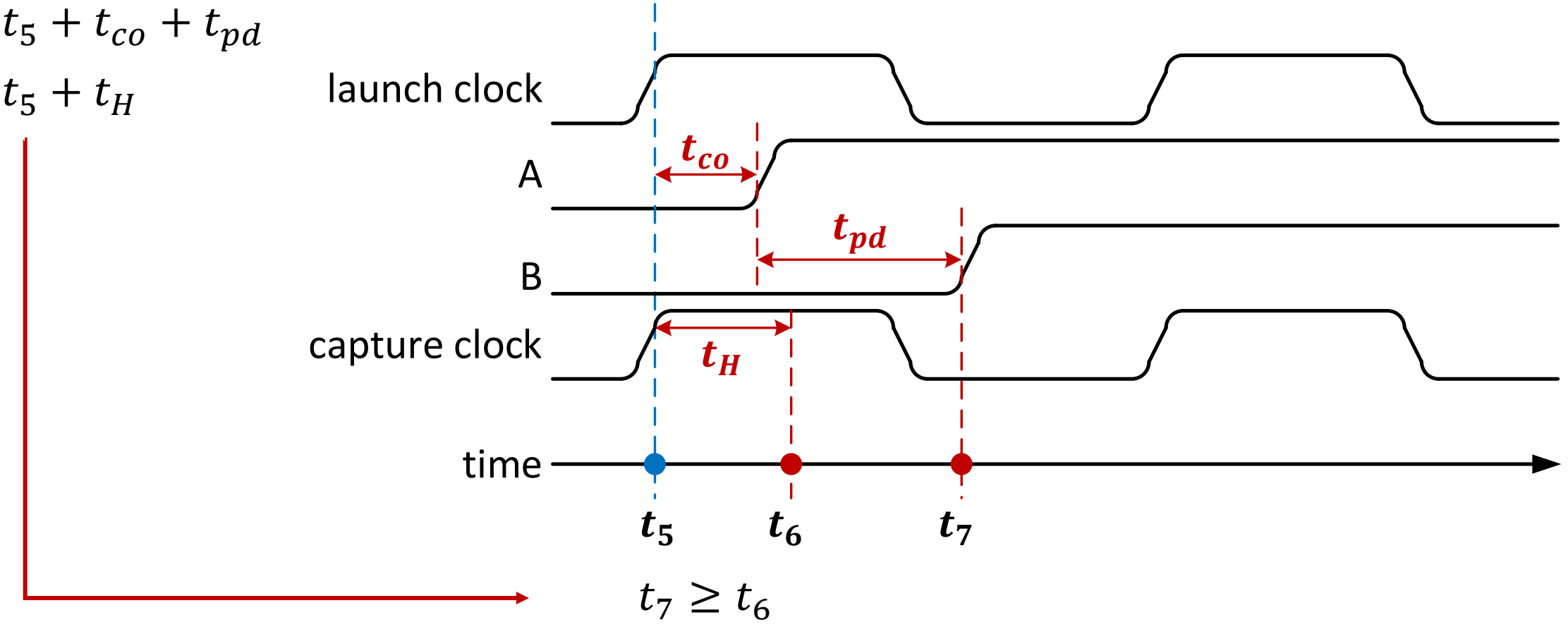
Timing constraints – Hold time



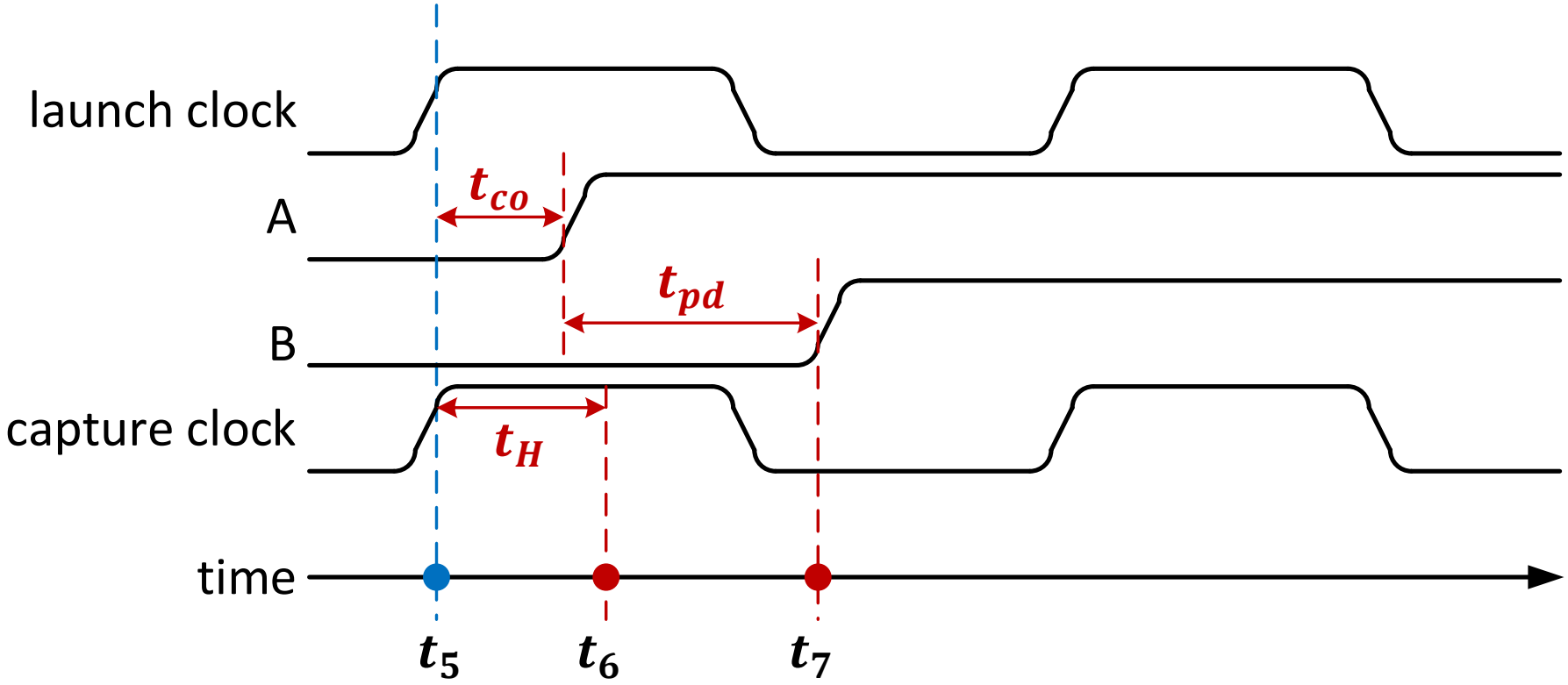
$$t_7 \geq t_6$$

Timing constraints – Hold time

- $t_7 = t_5 + t_{co} + t_{pd}$
- $t_6 = t_5 + t_H$



Timing constraints – Hold time



$$t_5 + t_{co} + t_{pd} \geq t_5 + t_H$$

Timing constraints – Hold time

$$t_5 + t_{co} + t_{pd} \geq t_5 + t_H$$

Timing constraints – Hold time

$$t_5 + t_{co} + t_{pd} \geq t_5 + t_H$$

Timing constraints – Hold time

$$t_5 + t_{co} + t_{pd} \geq t_5 + t_H \qquad \rightarrow \quad t_{co} + t_{pd} \geq t_H$$

Timing constraints – Hold time

$$t_5 + t_{co} + t_{pd} \geq t_5 + t_H \quad \rightarrow \quad t_{co} + t_{pd} \geq t_H$$

$$t_H \leq t_{co} + t_{pd}$$

Timing constraints – Hold time

- $t_H \leq t_{co} + t_{pd}$
  - $t_{pd}\ ?=?\ \begin{cases} t_{pd_{min}} \\ t_{pd_{max}} \end{cases}$

Timing constraints – Hold time

- $t_H \leq t_{co} + t_{pd}$
  - $t_{pd}\,?=?\begin{cases} t_{pd_{min}} \\ t_{pd_{max}} \end{cases}$ → Worst case!
  - Again, worst case for the same reasons

Timing constraints – Hold time

- Summarizing, the timing constraint on the hold time (t_H) is

$$t_H \leq t_{co} + t_{pd_{min}}$$

Timing constraints

- Summary
  - Setup → $T_{clk} \geq t_S + t_{co} + t_{pd_{max}}$ → $\left(f_{clk} \leq \frac{1}{t_S + t_{co} + t_{pd_{max}}}\right)$
  - Hold → $t_H \leq t_{co} + t_{pd_{min}}$

Timing constraints

- Summary
  - Setup → $T_{clk} \geq t_S + t_{co} + t_{pd_{max}}$ → $\left(f_{clk} \leq \frac{1}{t_S + t_{co} + t_{pd_{max}}}\right)$
  - Hold → $t_H \leq t_{co} + t_{pd_{min}}$
- Is it ALL the truth?

Timing constraints

- Summary
  - Setup → $T_{clk} \geq t_S + t_{co} + t_{pd_{max}}$ → $\left(f_{clk} \leq \frac{1}{t_S + t_{co} + t_{pd_{max}}}\right)$
  - Hold → $t_H \leq t_{co} + t_{pd_{min}}$

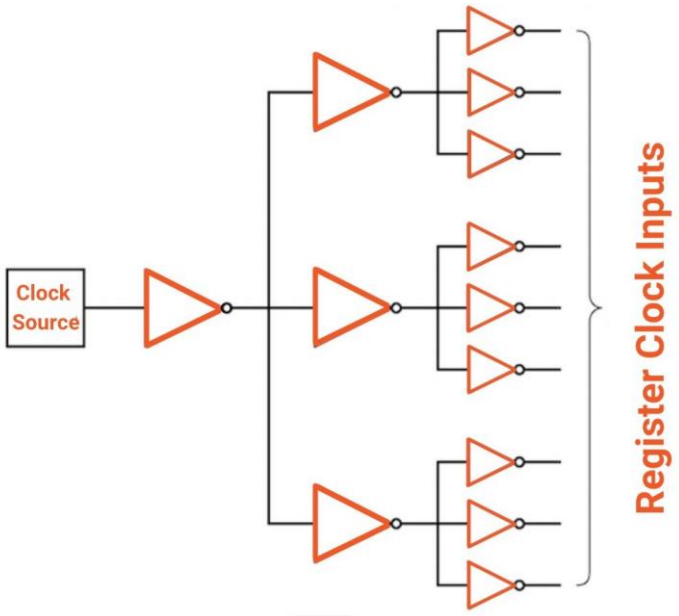
- Is it ALL the truth? No!
  - Some aspects are still missing

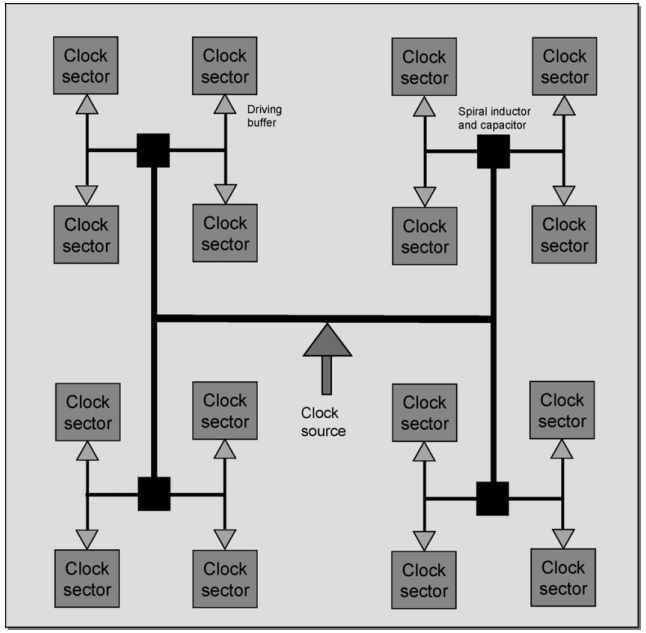
Timing constraints

- Modern digital systems count a lot of transistors
  - We saw about VLSI: transistor count $\geq 10^6$
    - In some case up to 10^{10}
  - Part of these transistors are used for registers/flip-flops
  - A single clock signal must reach (physically) many registers
    - Ideally at the same time
    - However, this is not physically possible (because of the high density of registers)

Timing constraints

- The clock distribution is a very delicate aspect of the chip manufacturing process
  - It constitutes a specific and dedicated step of the manufacturing process: CTS (Clock Tree Synthesis)
  - They exist techniques to optimize the distribution of clock and equalize it as much as possible





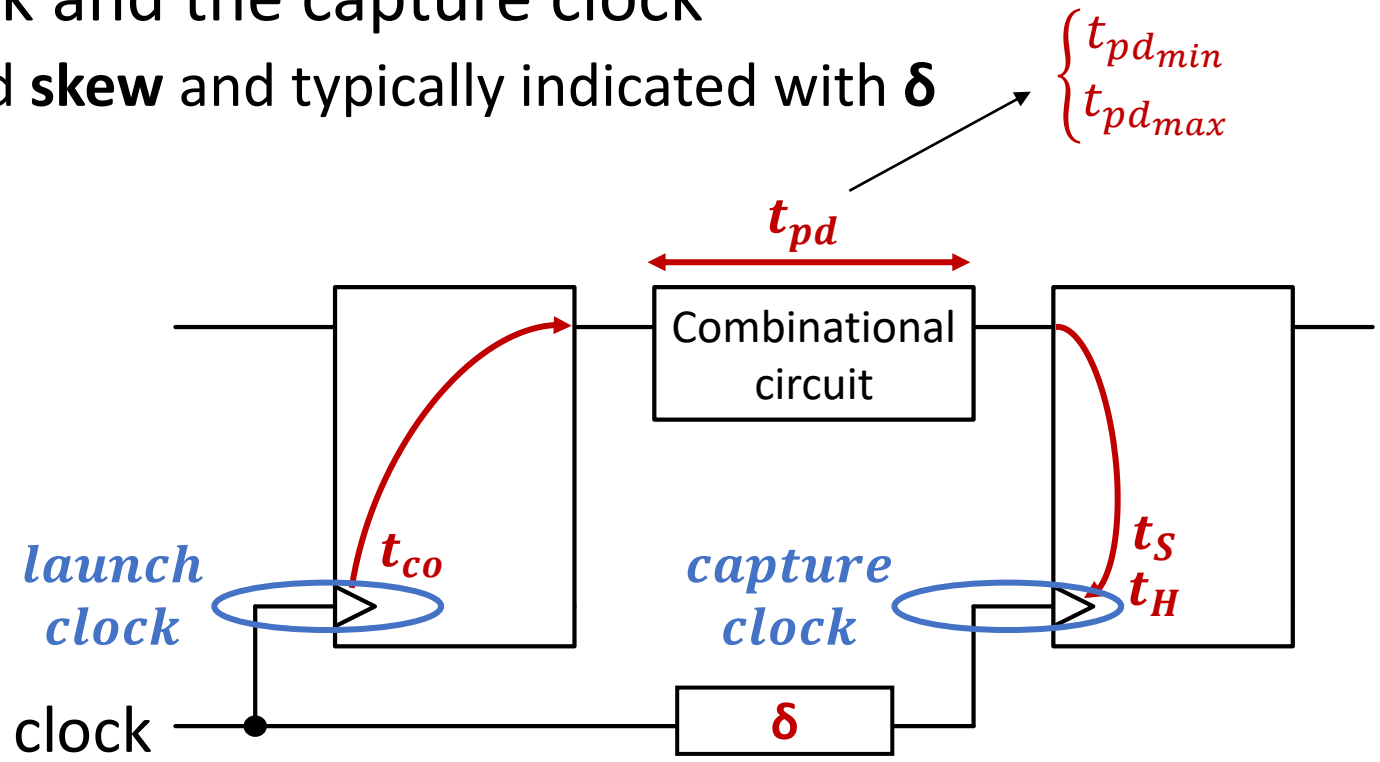
Timing constraints

- Anyway, is not physically possible to make the distance between the clock source and the clock port of registers equal for all the registers

- And even if so, other (physical, and unpredictable) factors may cause delays on the clock between different registers
  - Temperature variations
  - Material imperfections
  - …

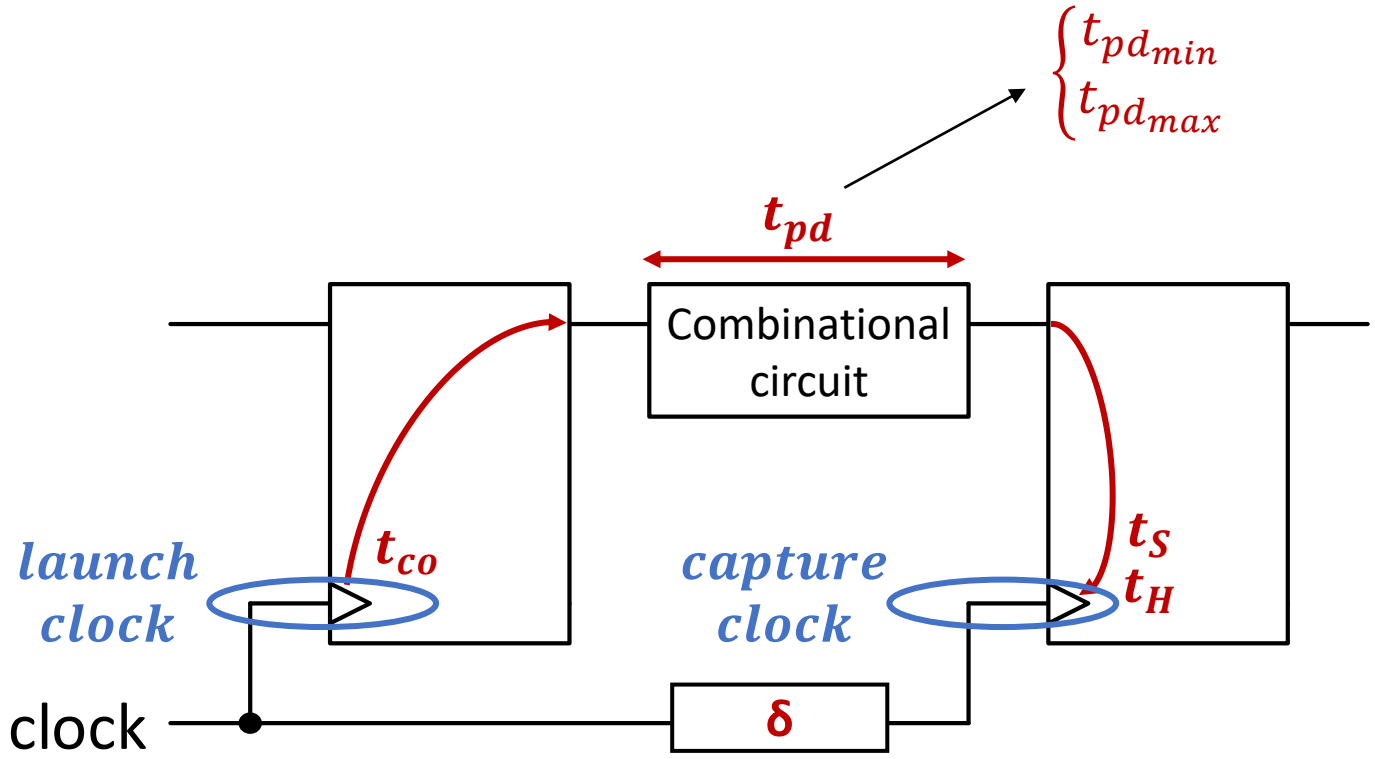
Timing constraints

- Therefore, the delay model should include also the delay between the launch clock and the capture clock
  - It is called **skew** and typically indicated with **δ**



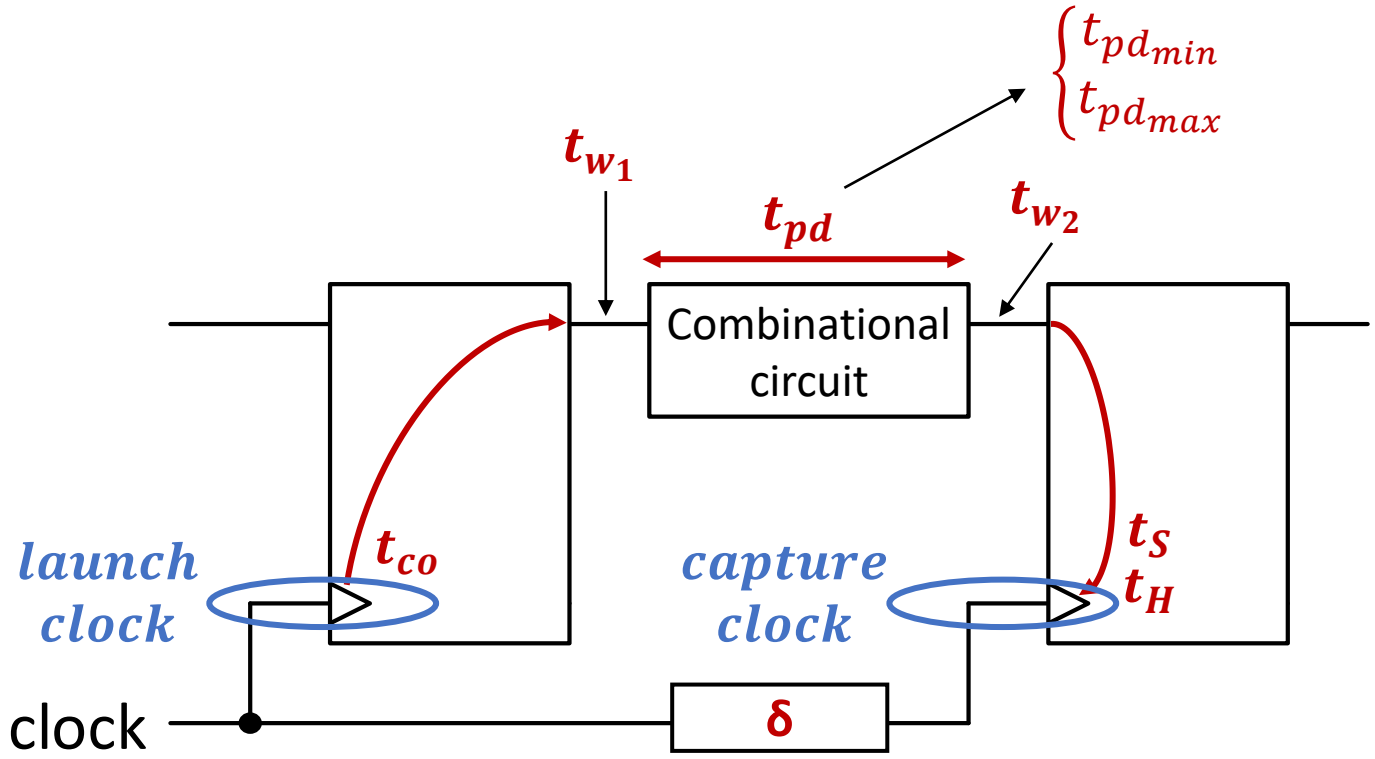
Timing constraints

- This slightly changes the previous constraints we determined



Timing constraints

- In addition, also the wires delay (t_{w_i}) should be considered

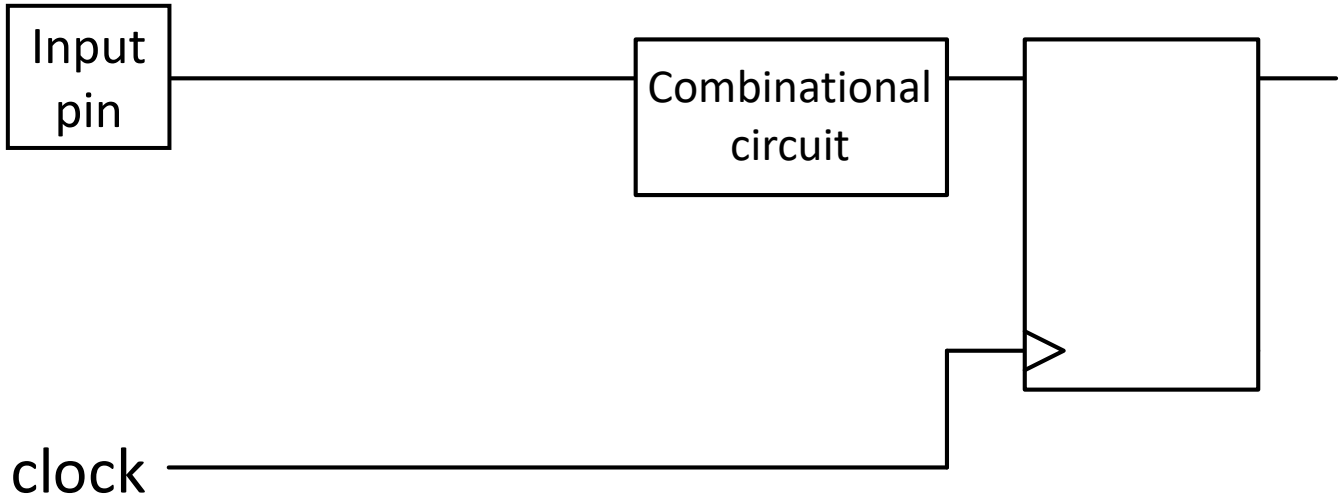


Timing constraints

- And they exist corner cases that we did not consider

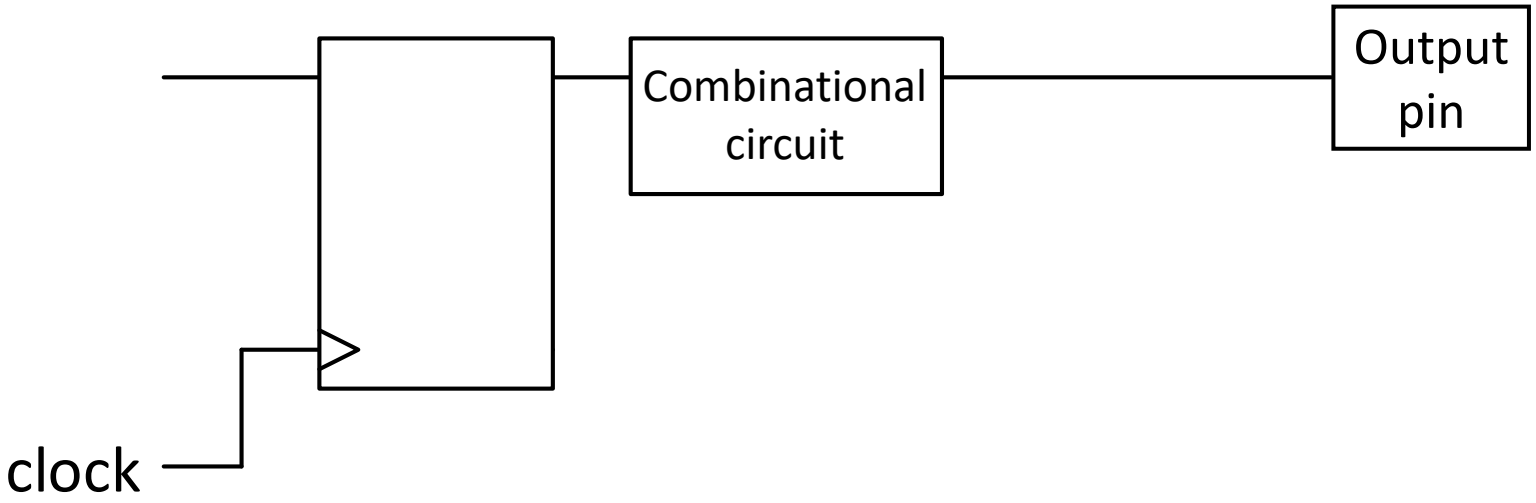
Timing constraints

- And they exist corner cases that we did not consider
  - Input paths
    - Launch register misses



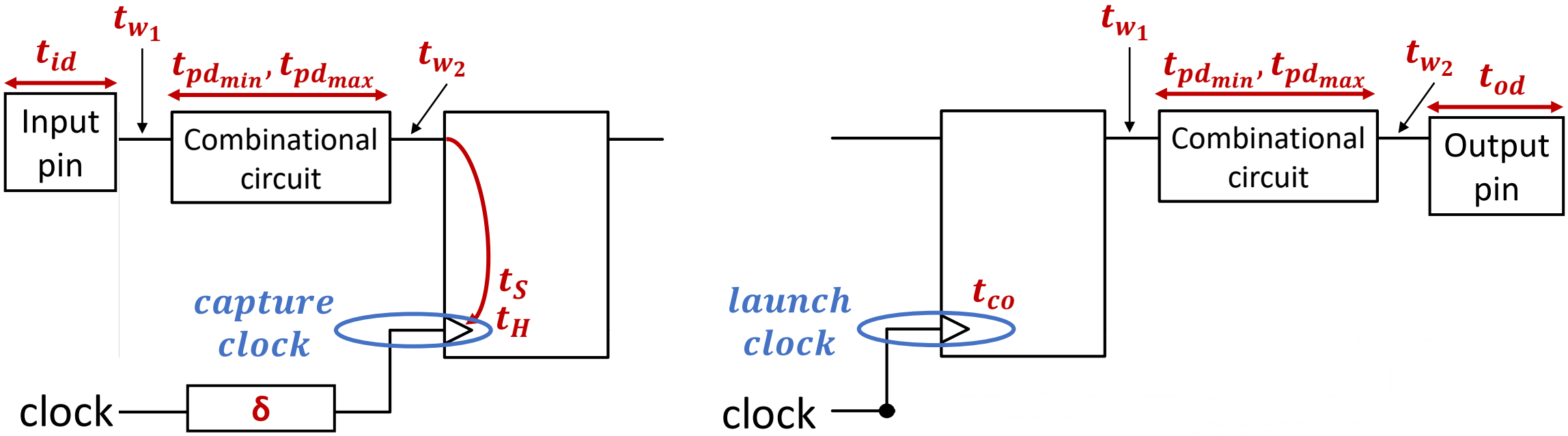
Timing constraints

- And they exist corner cases that we did not consider
  - Output paths
    - Capture register misses



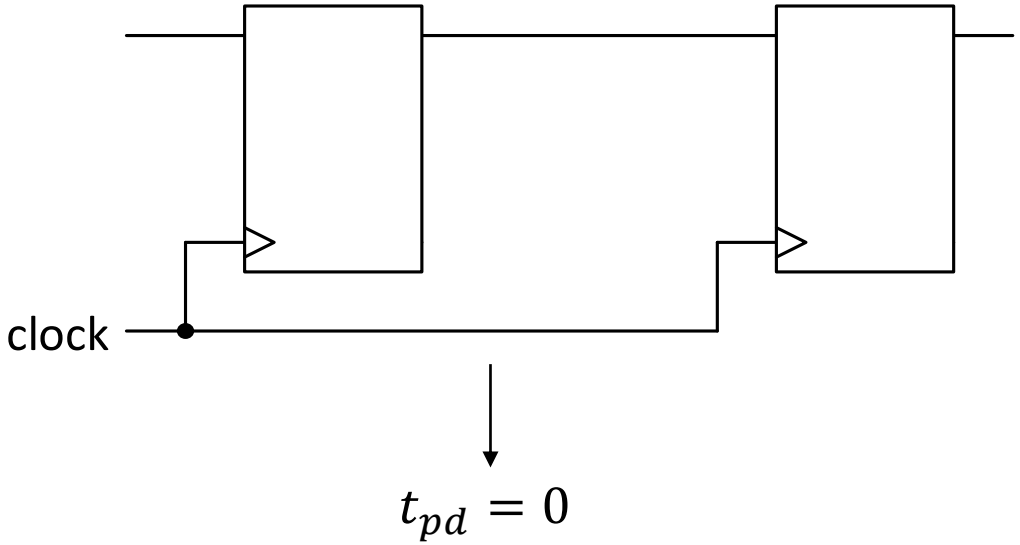
Timing constraints

- Input and output paths would require a more accurate delay model
  - t_{id} = input delay (of the input pin)
  - t_{od} = output delay (of the output pin)

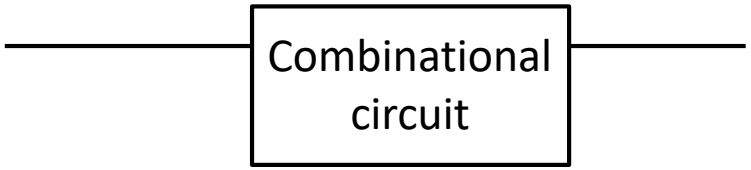


Timing constraints

- And they exist corner cases that we did not consider
  - Others
    - Combinational logic misses



Both registers miss (combinational path)



Timing constraints

- We are going to analyze the more accurate delay models

- However, remember that
  - The timing analysis to check the setup and hold constraints are met is an essential part of the design process of a circuit
    - It is automated and called **STA** = **S**tatic **T**iming **A**nalysis
    - It can be performed multiple times/at different level, since any step of the design process can add information about timing
      - Gate-level → information about gate delays
      - Transistor-level → information about delays of wires, pins, …

Timing constraints

- Also remember that
  - Setup violations
    - Can be fixed during design phase
      - Frequency lowering, insertion of pipeline(s) to reduce the path delay, …
    - Can be fixed after the fabrication of the chip
      - Frequency lowering
  - Hold violations
    - Can be fixed during design phase
      - Inserting delay chains (e.g., cascade of NOT gates or buffers)
    - Cannot be fixed after the fabrication of the chip!!!

Thank you for your attention

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