Electronics Systems (938II)

Lecture 3.5

Semiconductor Memories – SRAM

Introduction to Random Access Memory (RAM)

- With the term **RAM** (Random Access Memory), typically we indicate memories that are:
  - **RWM** (Read and Write Memory)
  - **Volatile**

- Note
  - EPROM or EEPROM (or Flash memory) could be seen as a sort of RWM, but…
    - … for those devices, 'writing' (= erasing + reprogramming) is disruptive
    - **In RAMs (or better, RWM) writing is not disruptive**

Introduction to Random Access Memory (RAM)

- RAM classification
  - **Static** RAM (**SRAM**)
    - The memory content is hold over the time, as long as the memory is powered
  - **Dynamic** RAM (**DRAM**)
    - Even if the memory is powered, the memory content needs to be refreshed over the time, otherwise it is lost

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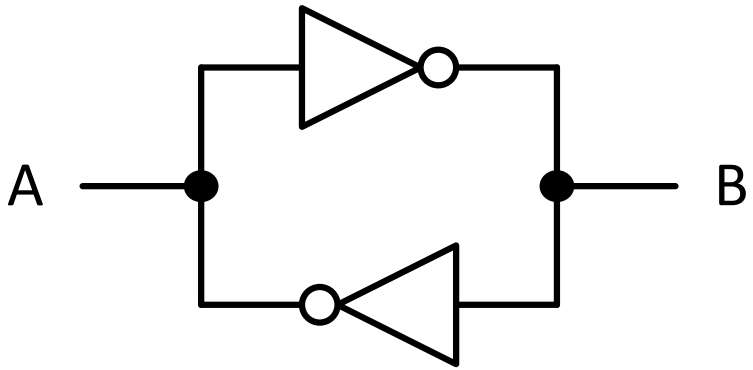
SRAM – Memory cell

- **Bistable** = two closed-loop inverters



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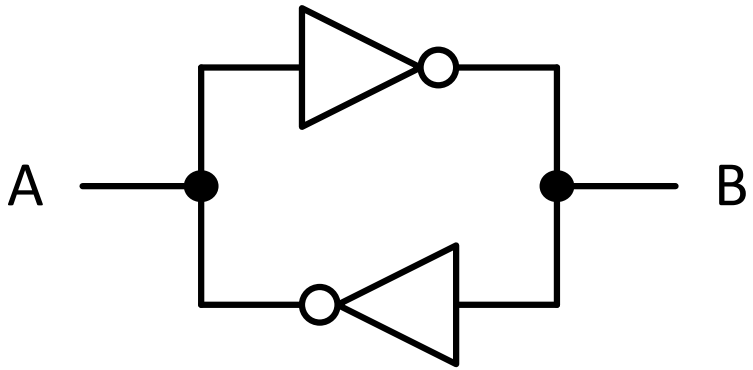

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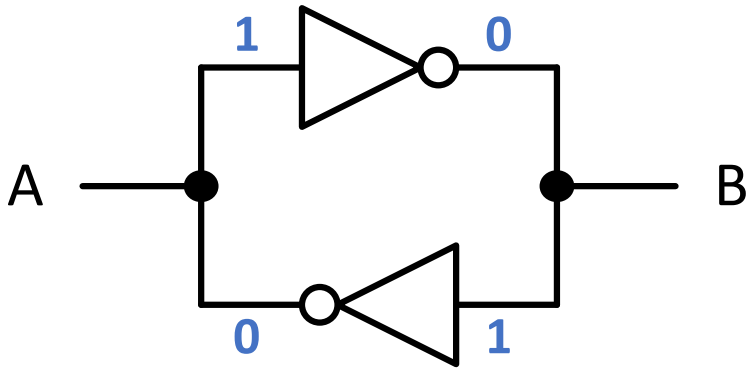

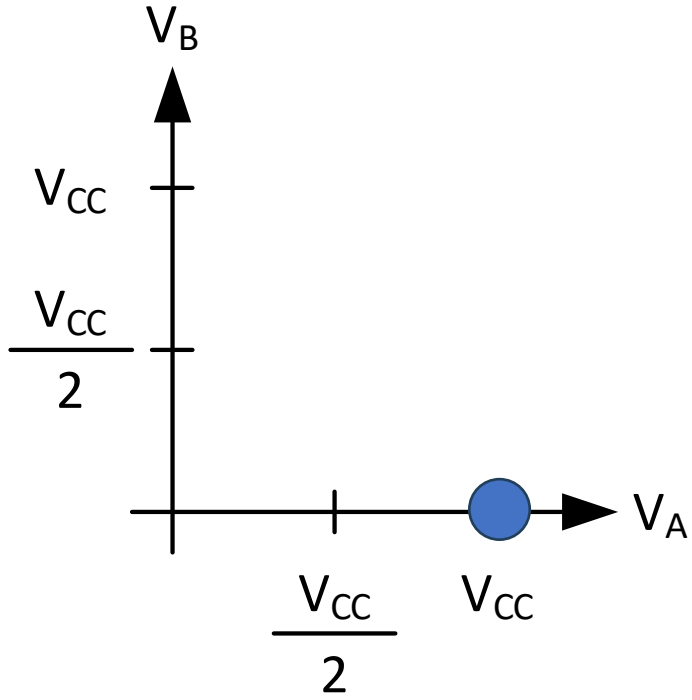

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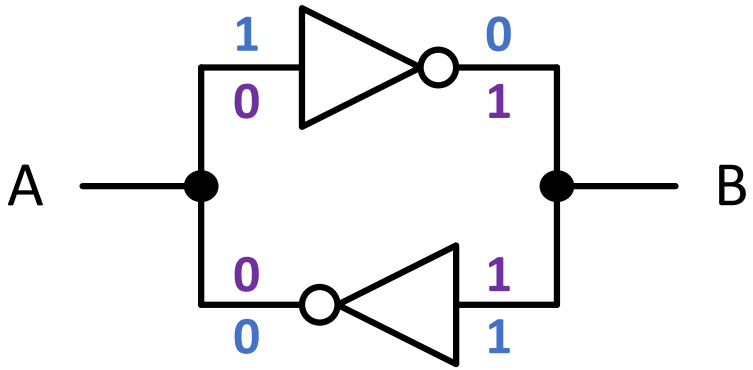

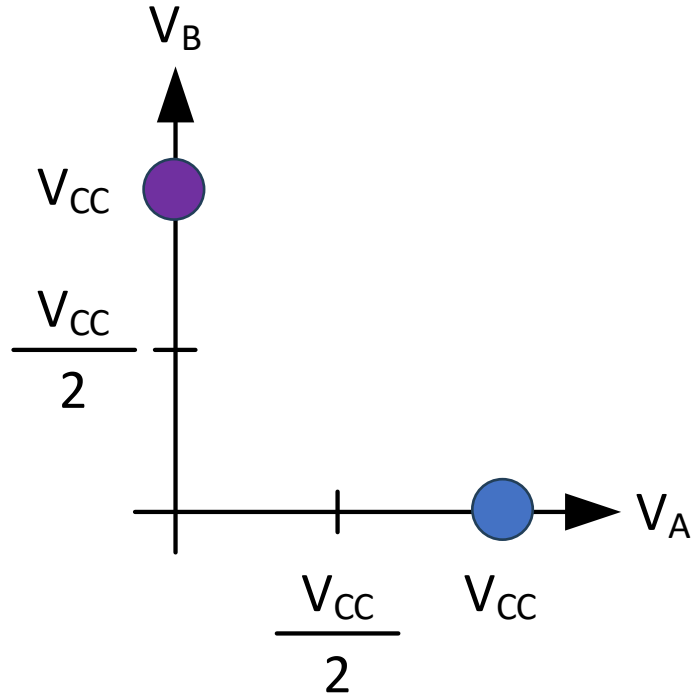

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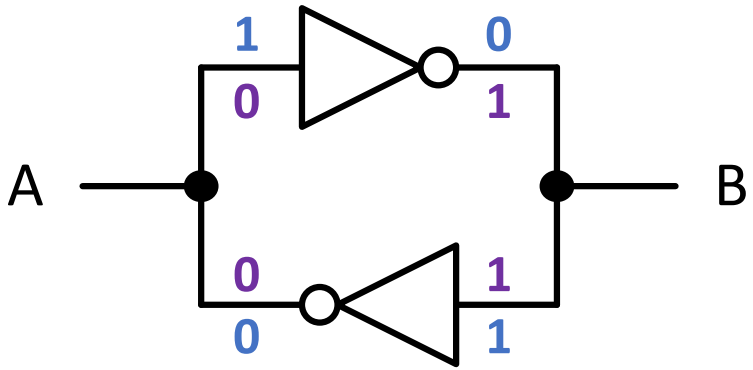

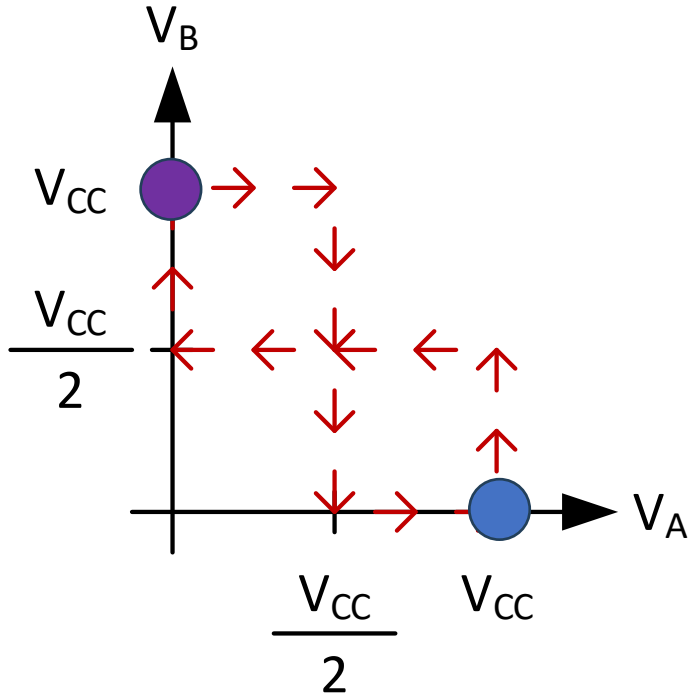

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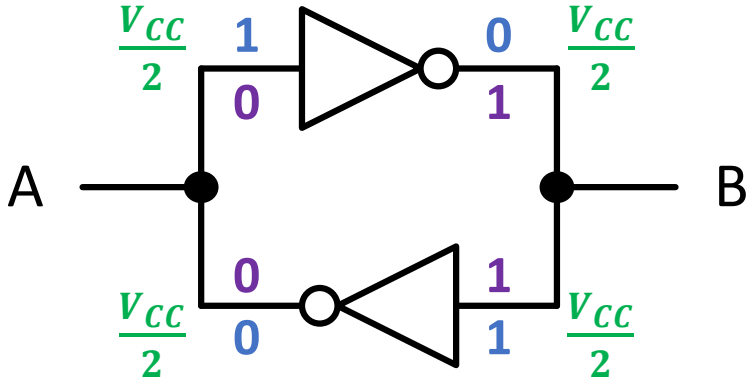
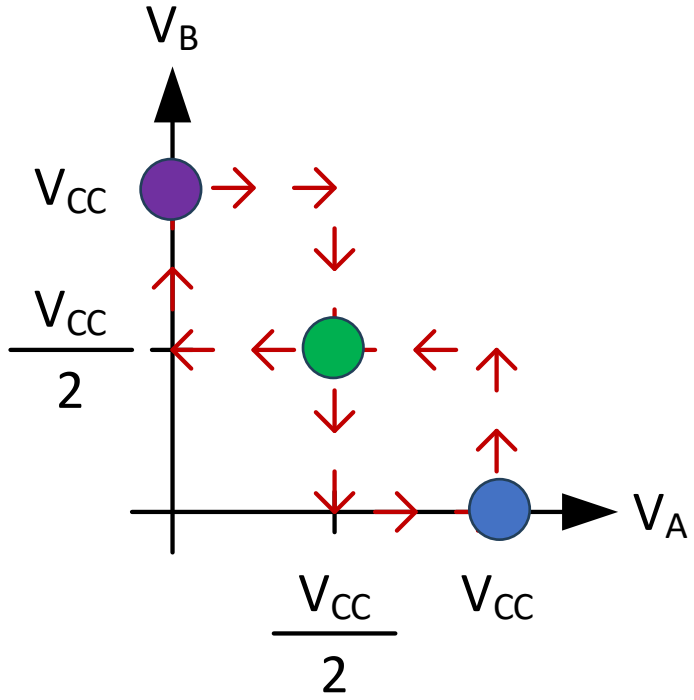
    - **State 3** ???





SRAM – Memory cell

- Bistable = two closed-loop inverters
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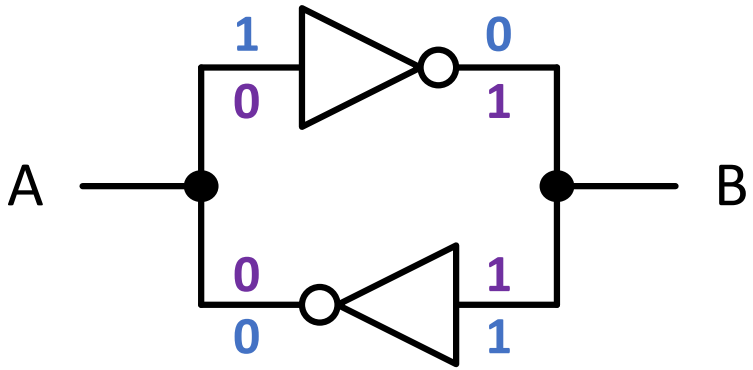
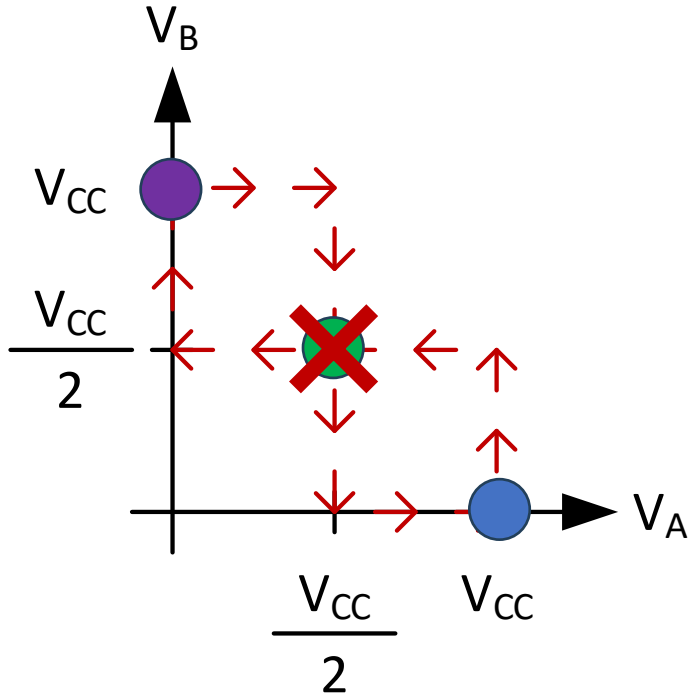
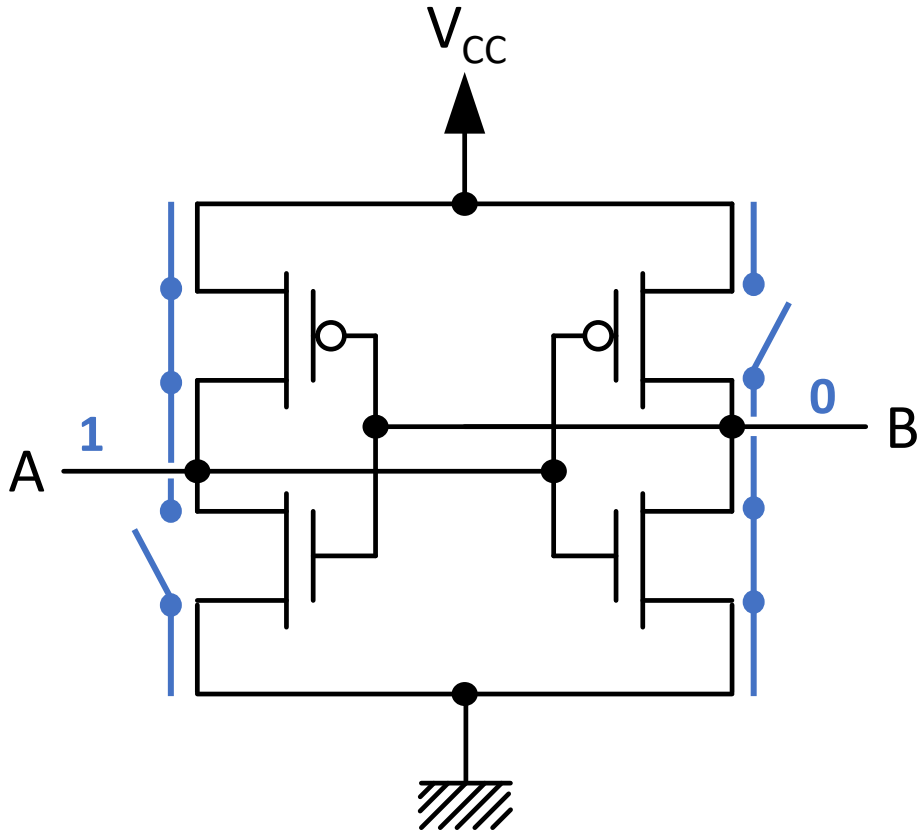
    - **State 3** ??? → No! Unstable!!!





SRAM – Memory cell

- Bistable
  - **CMOS implementation**
    - State 1
    - State 2



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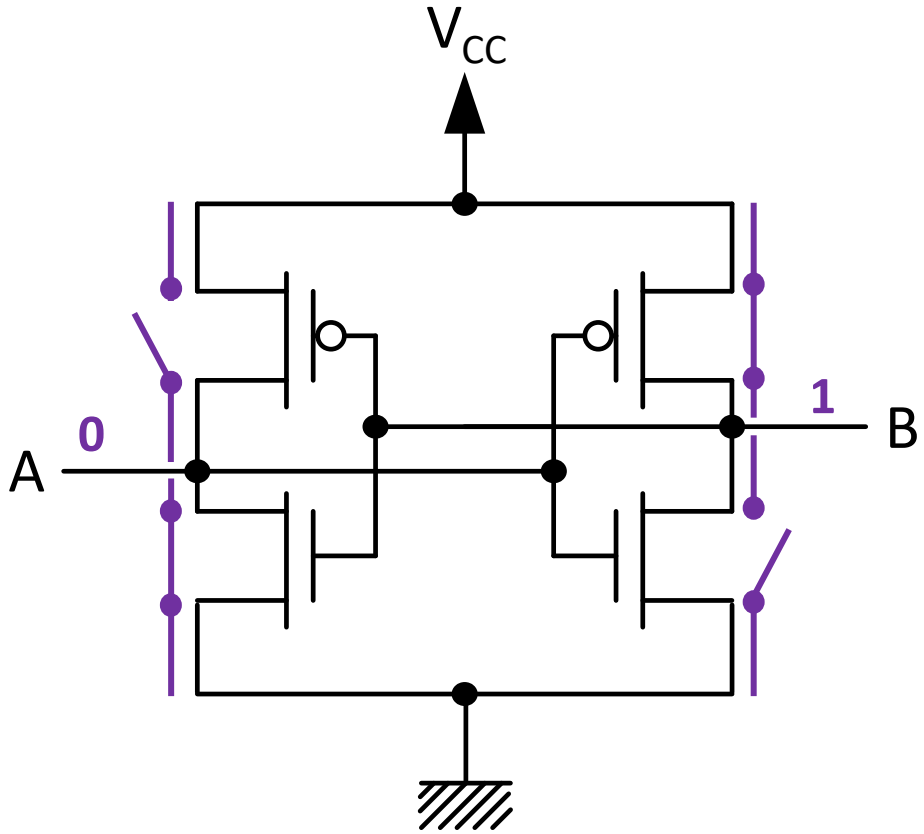
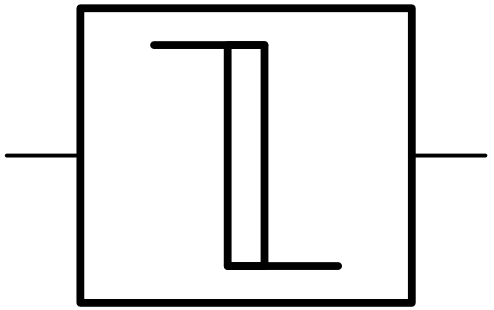


SRAM – Memory cell

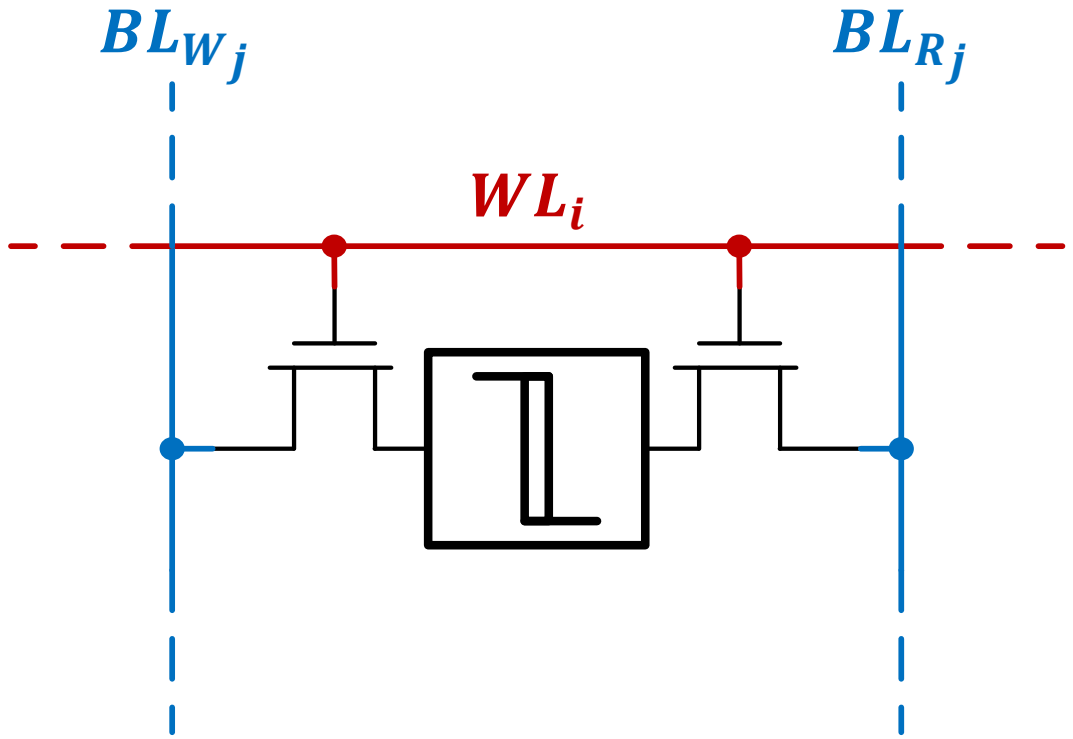
- Bistable
  - **Symbol**



SRAM – Memory cell

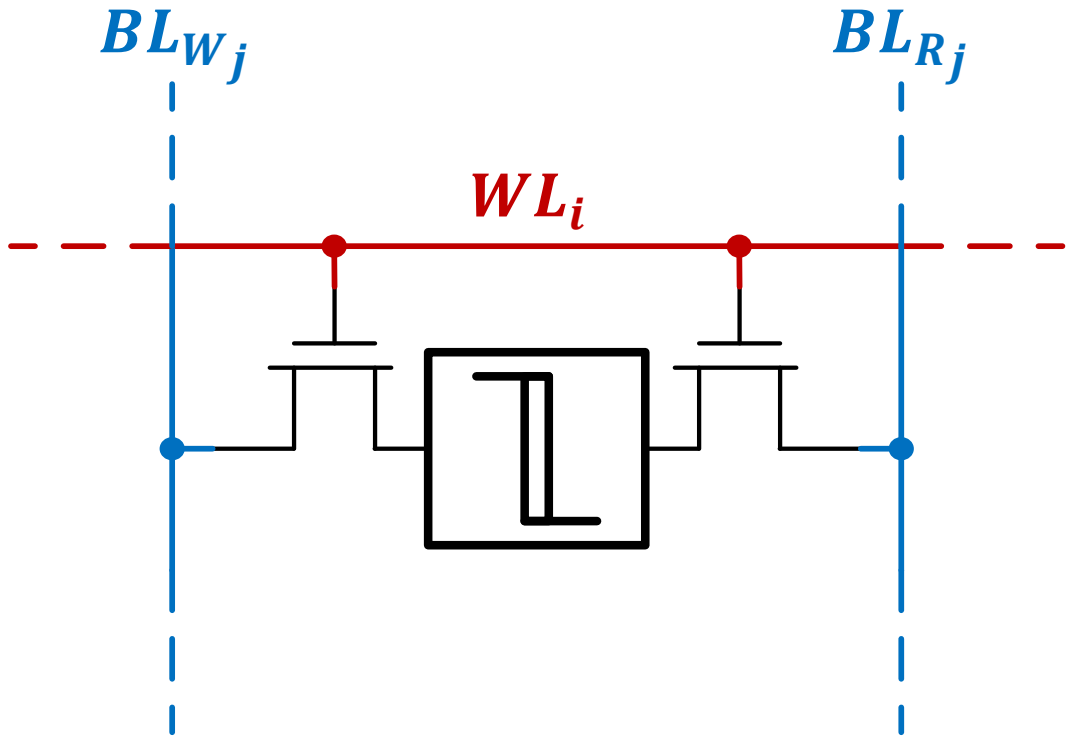
- Architecture
  - Bistable
  - 2x access transistors

  - WL_i = Word Line
  - BL_{W_j} = Bit Line for Write
  - BL_{R_j} = Bit Line for Read



SRAM – Memory cell

- Architecture
  - Bistable
  - 2x access transistors
  - Also called **6T** (6-Transistors) **SRAM cell**
    - Other architecture exist
    - Example: 4-transistors (4T)



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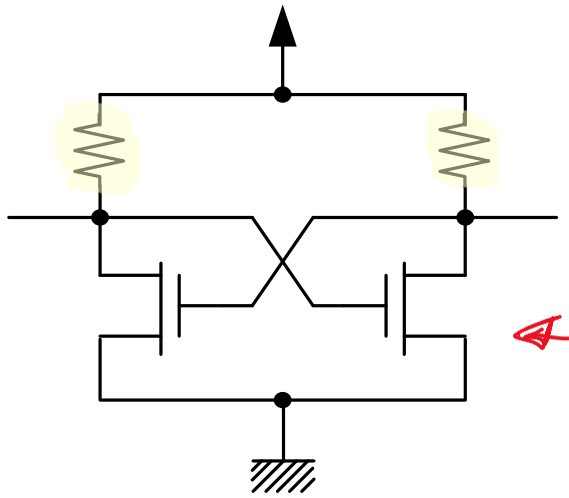
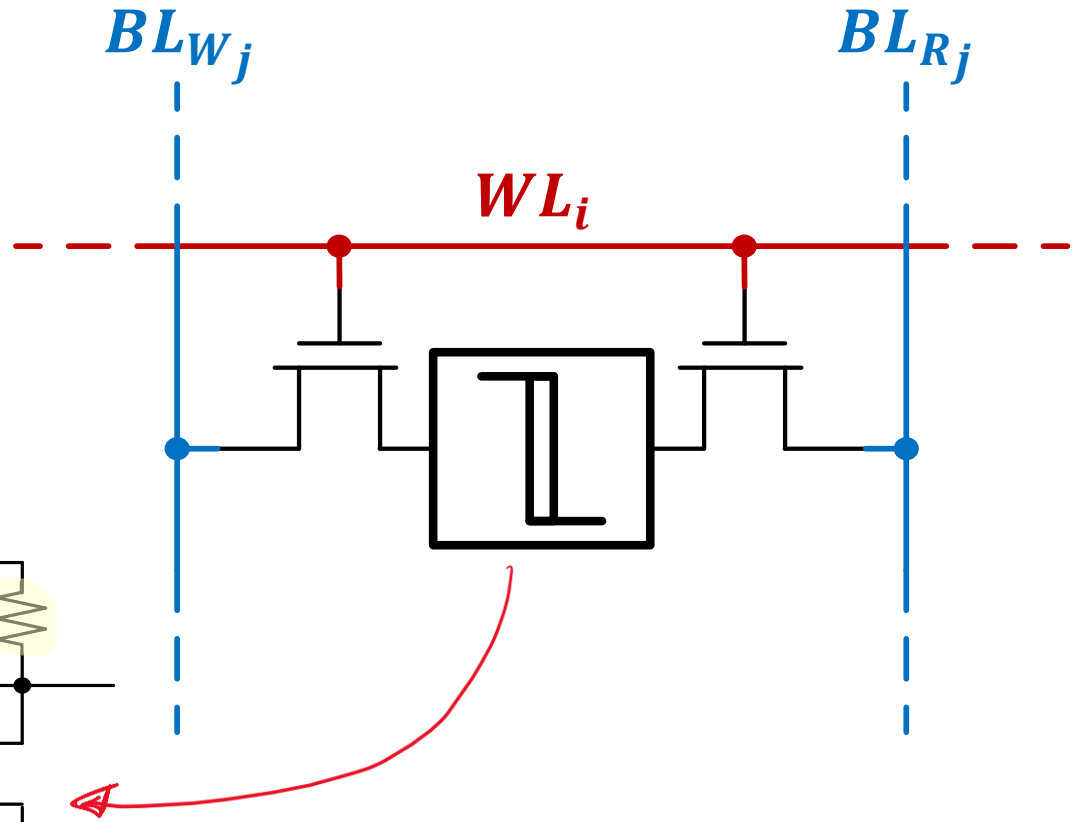
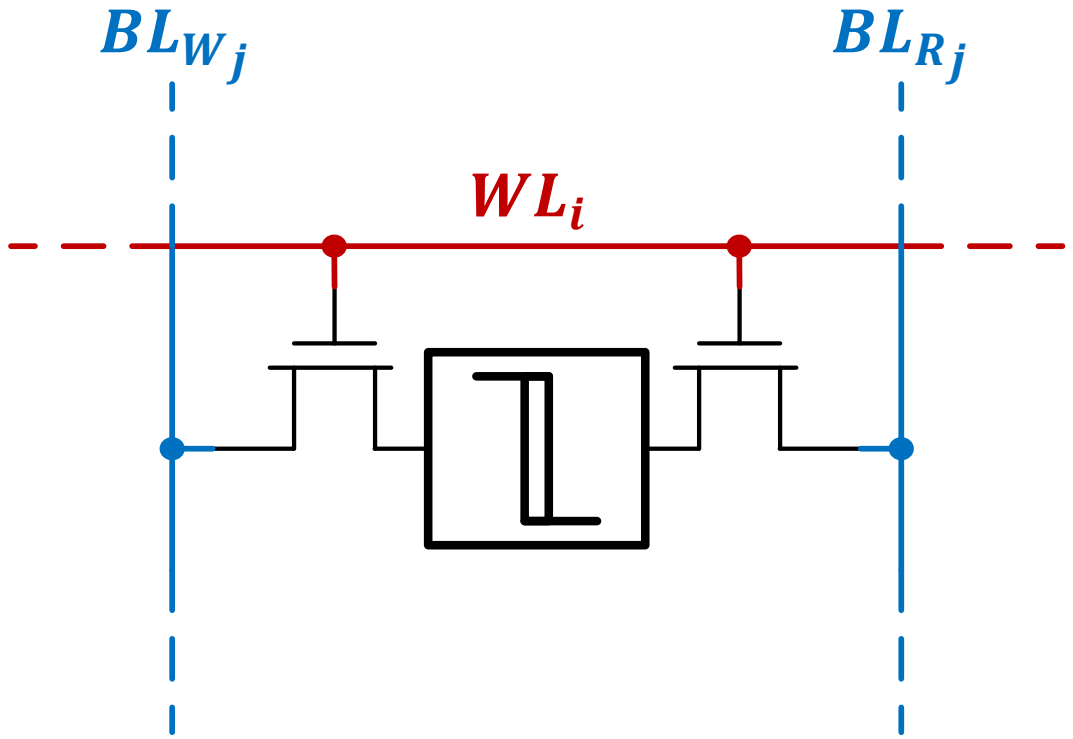
    - Other architecture exist
    - Example: 4-transistors (4T)
      - Resistors instead of pull-up p-MOS in the bistable





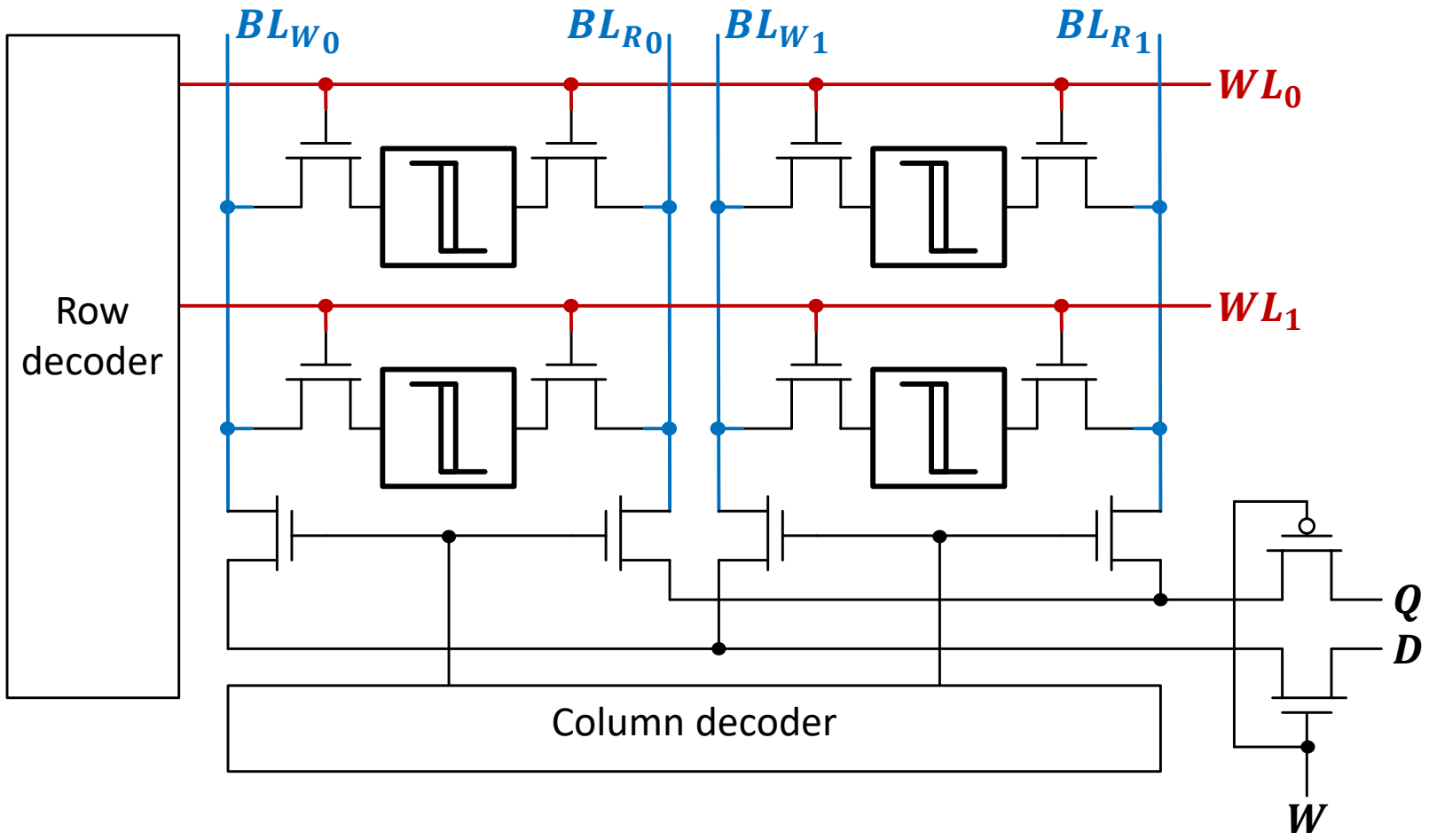
SRAM – Memory cell

- Architecture
  - Bistable
  - 2x access transistors
  - Also called **6T** (6-Transistors) **SRAM cell**
    - However, 6T is the most diffused
      - Performance vs. costs
    - If you are interested in other SRAM cell circuits:
      - https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10134887



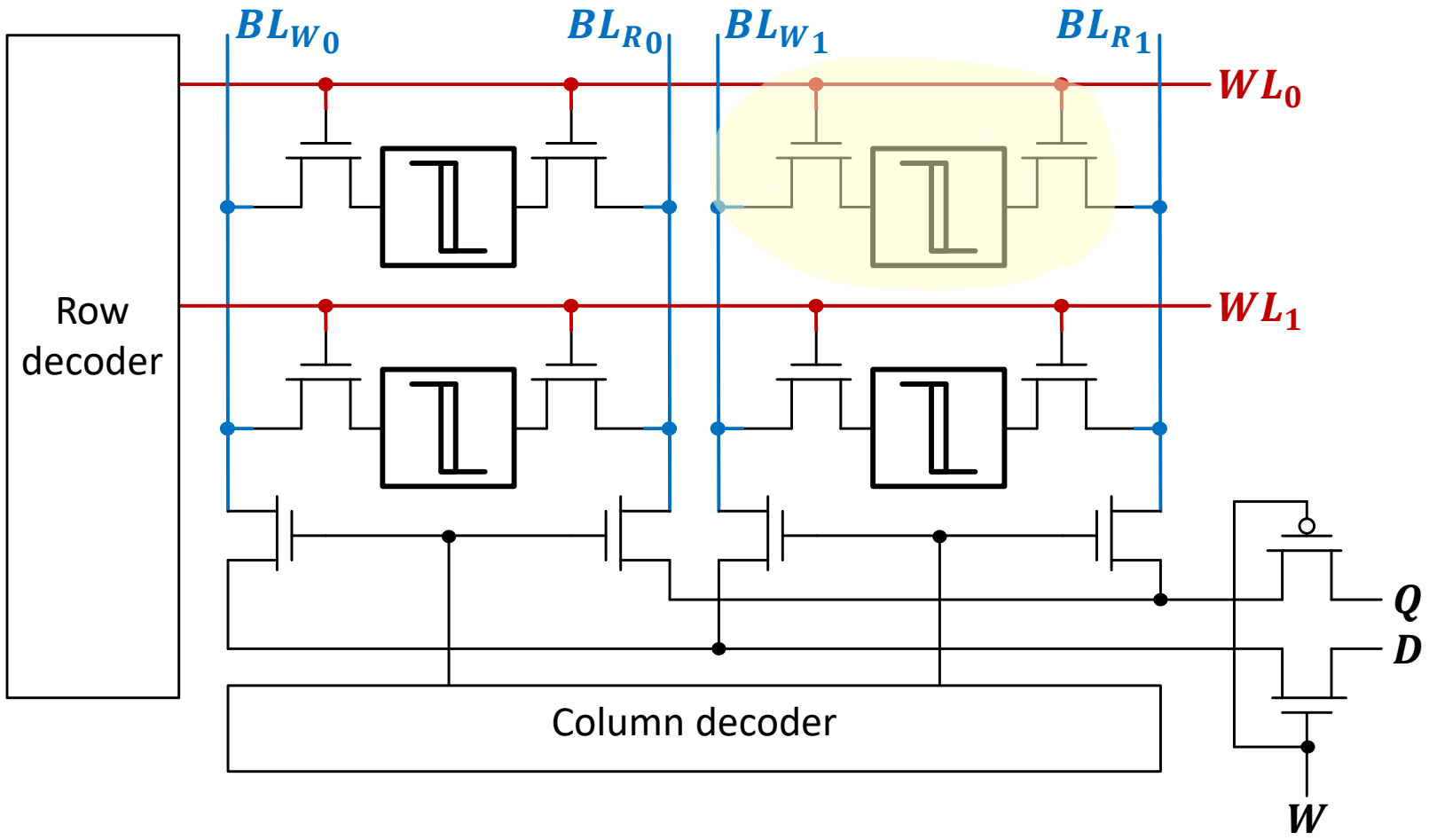
SRAM – Architecture and working principle

- Example – 4x4
  - **D** = input (write) data
  - **Q** = output (read) data
  - **W** = write command
    - 1 = write
    - 0 = read



SRAM – Architecture and working principle

- Example – 4x4
  - **Read**
    - Cell (0,1)



SRAM – Architecture and working principle

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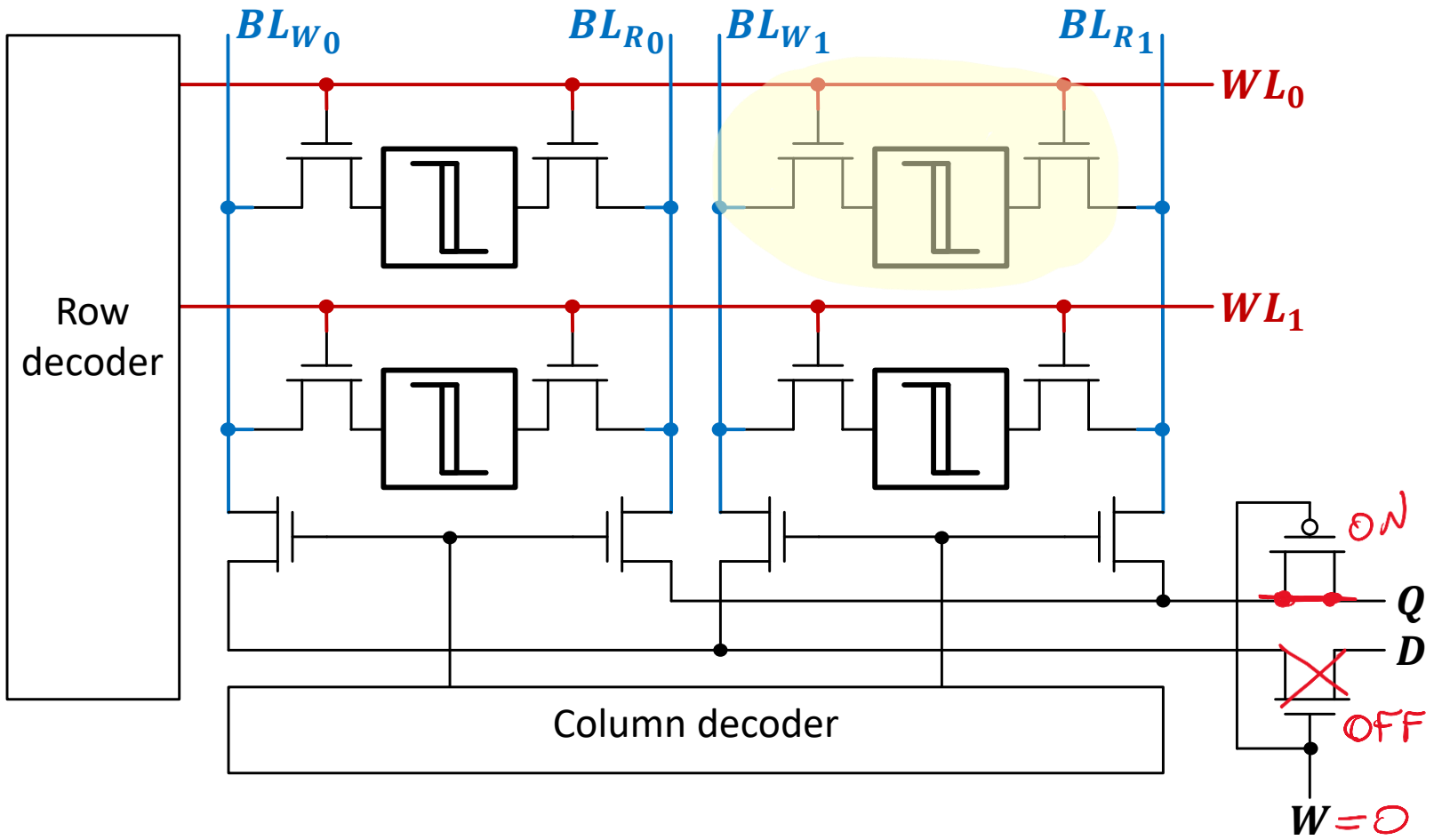

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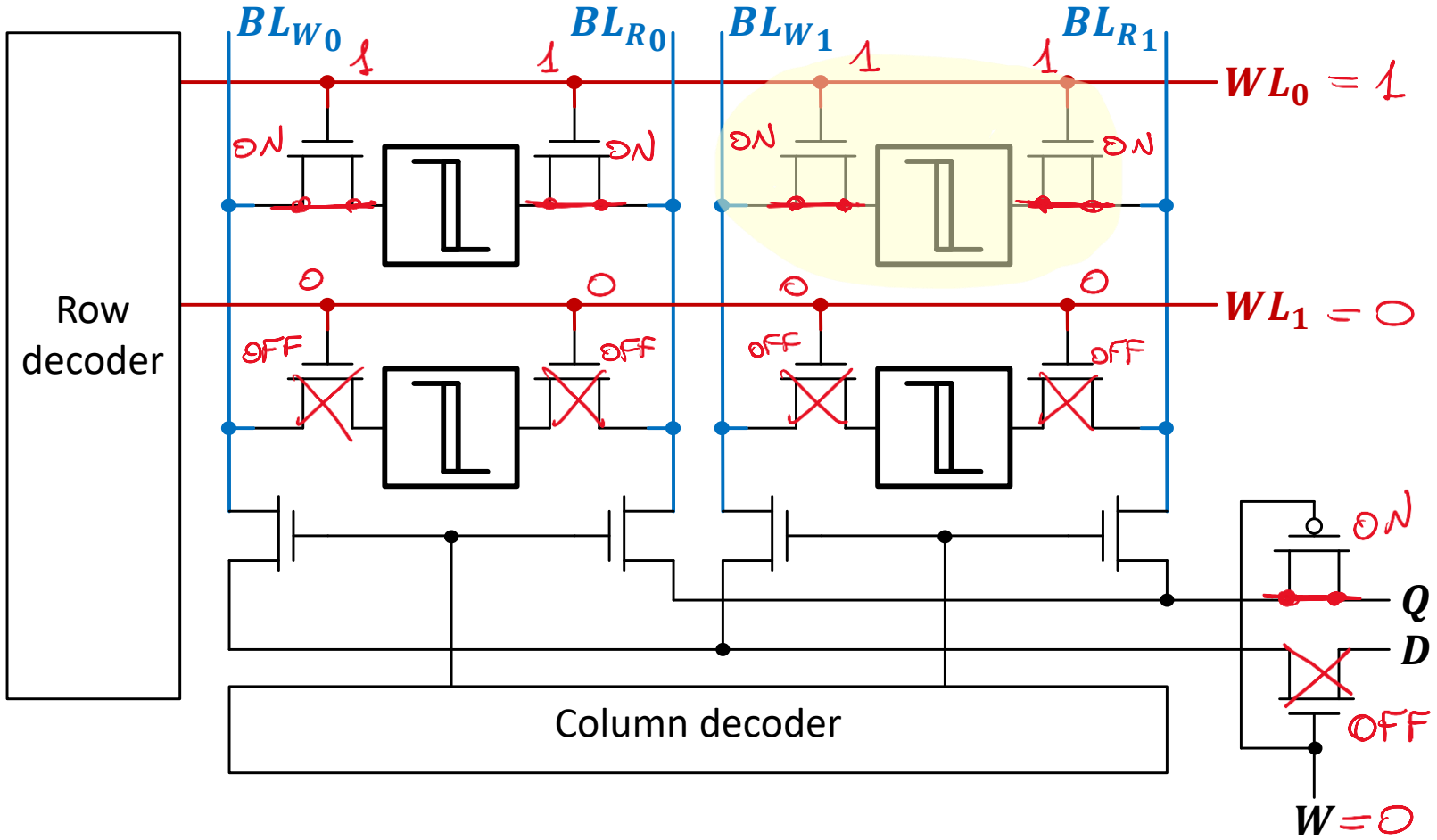

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- Example – 4x4
  - **Read**
    - Cell (0,1)
    - W = 0
    - $WL_0 = 1$
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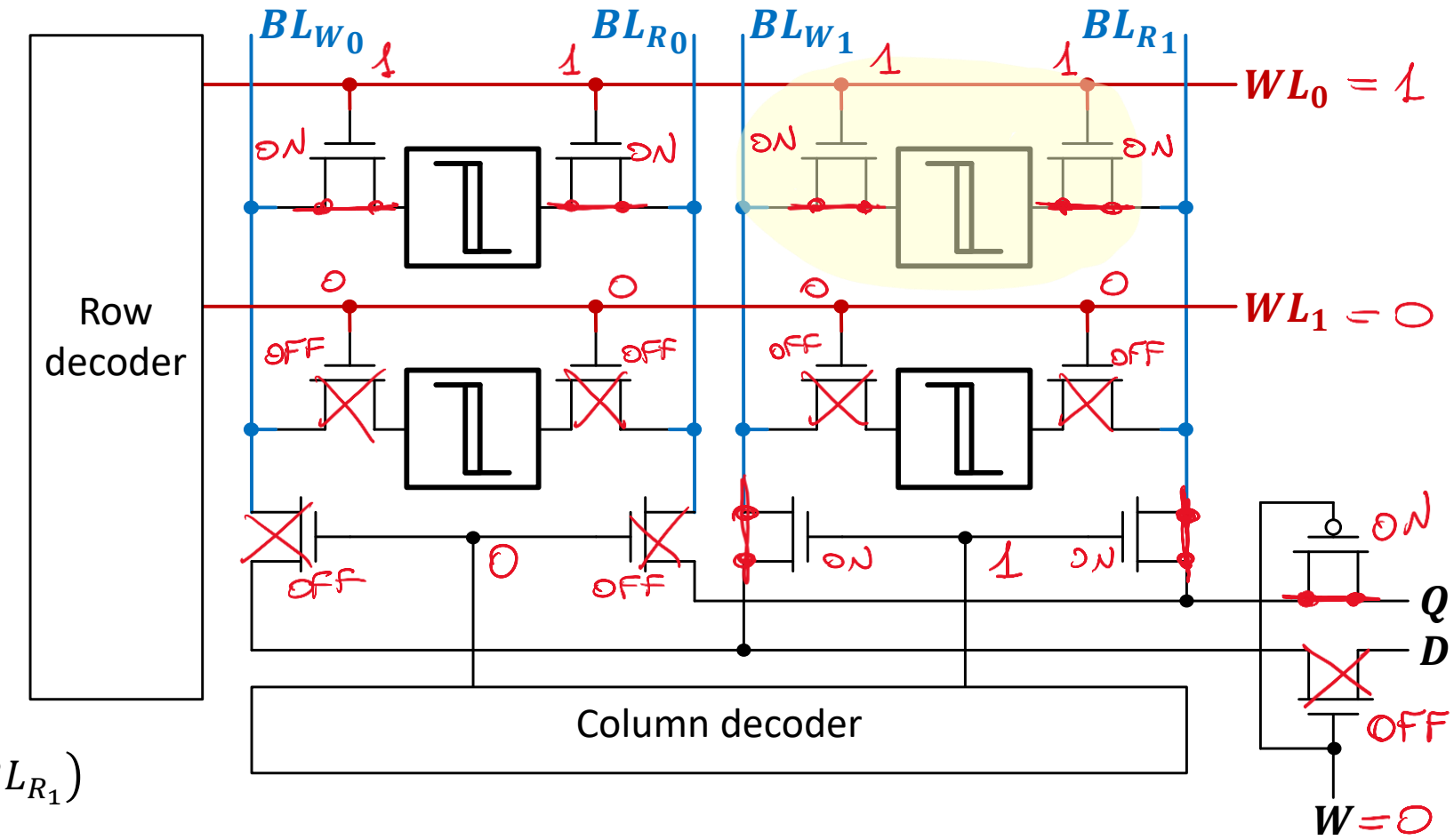
    - Column decoder
      - Activating access transistors of (BL_{W_1}, BL_{R_1})



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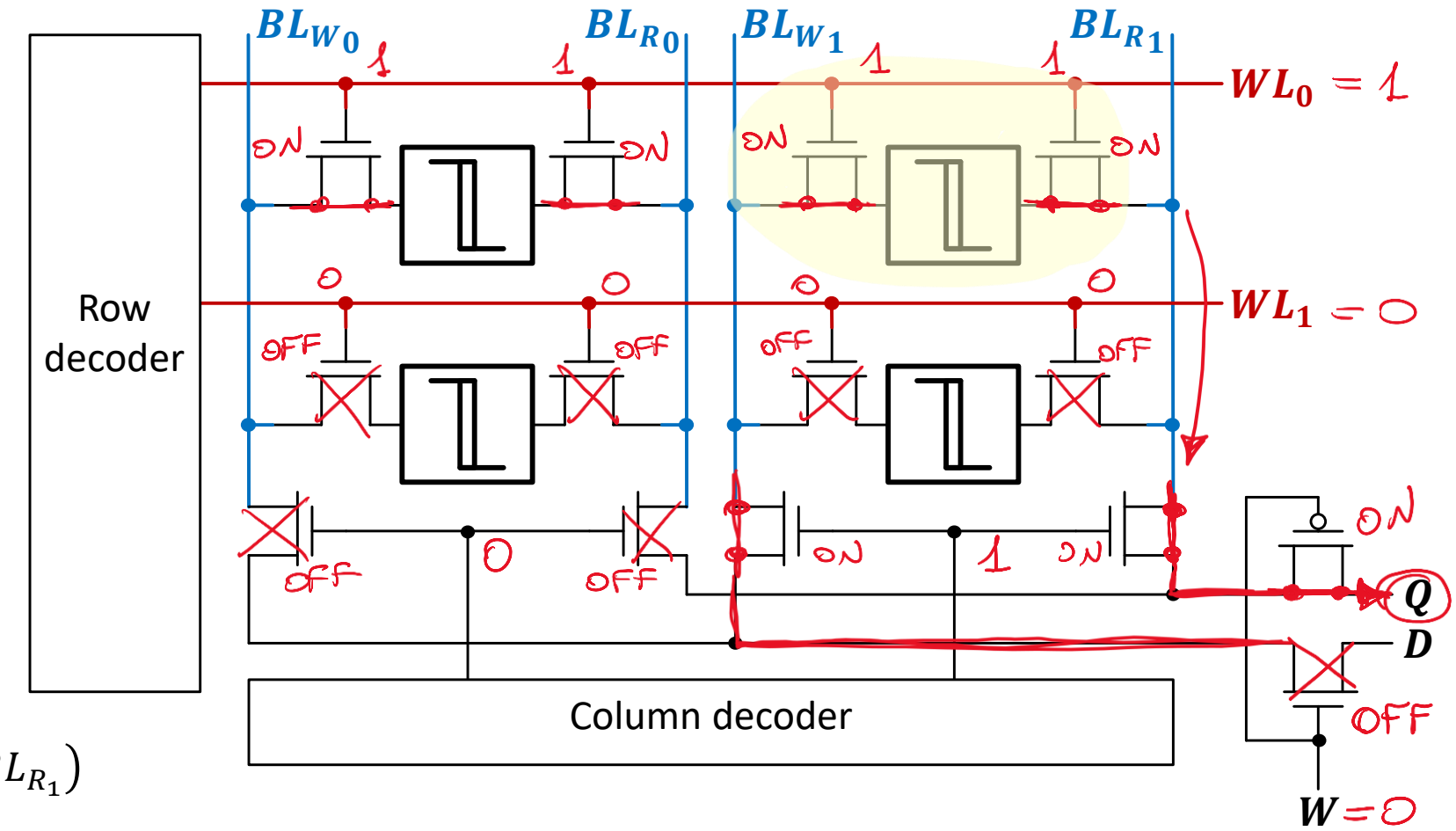

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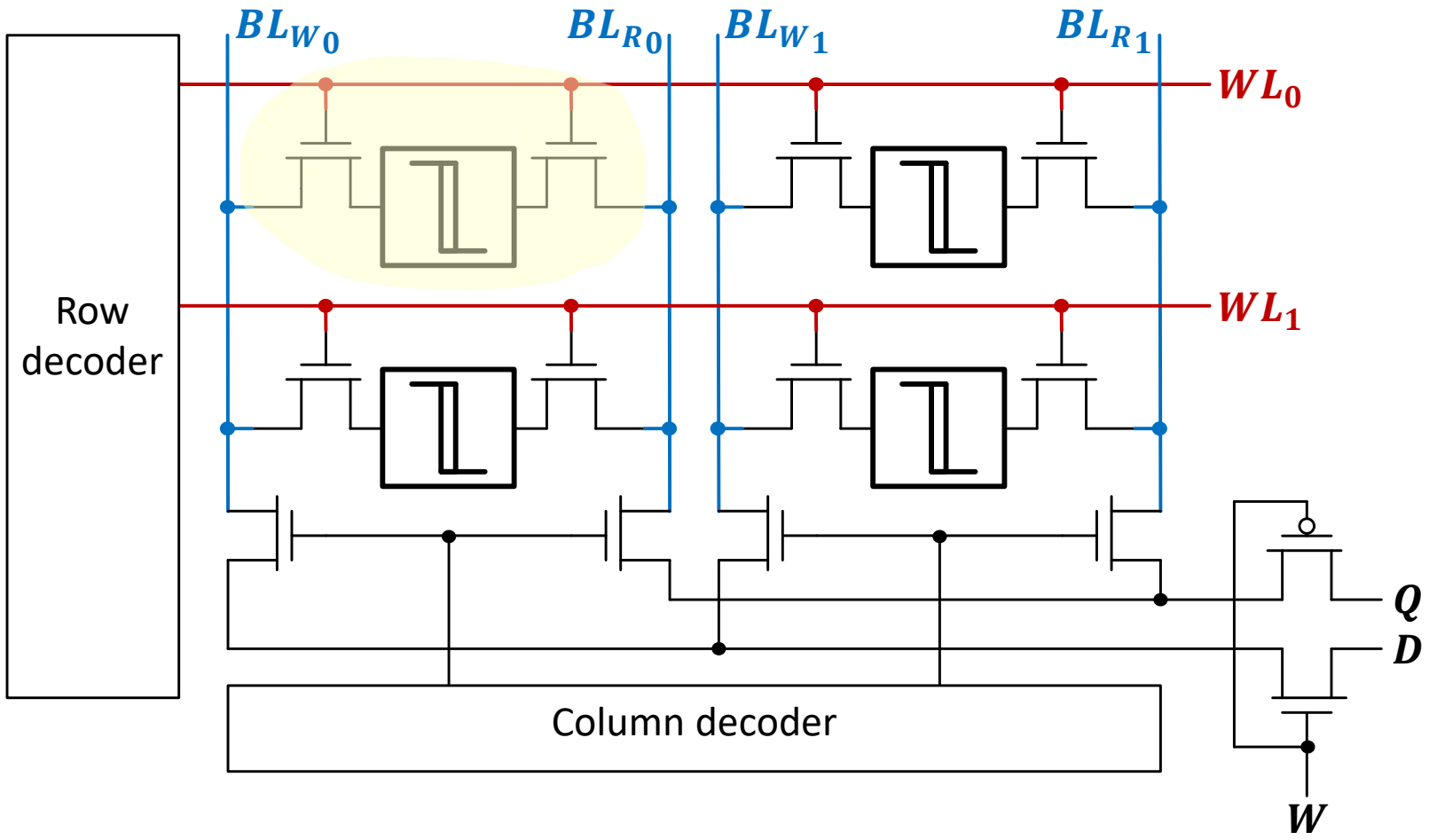

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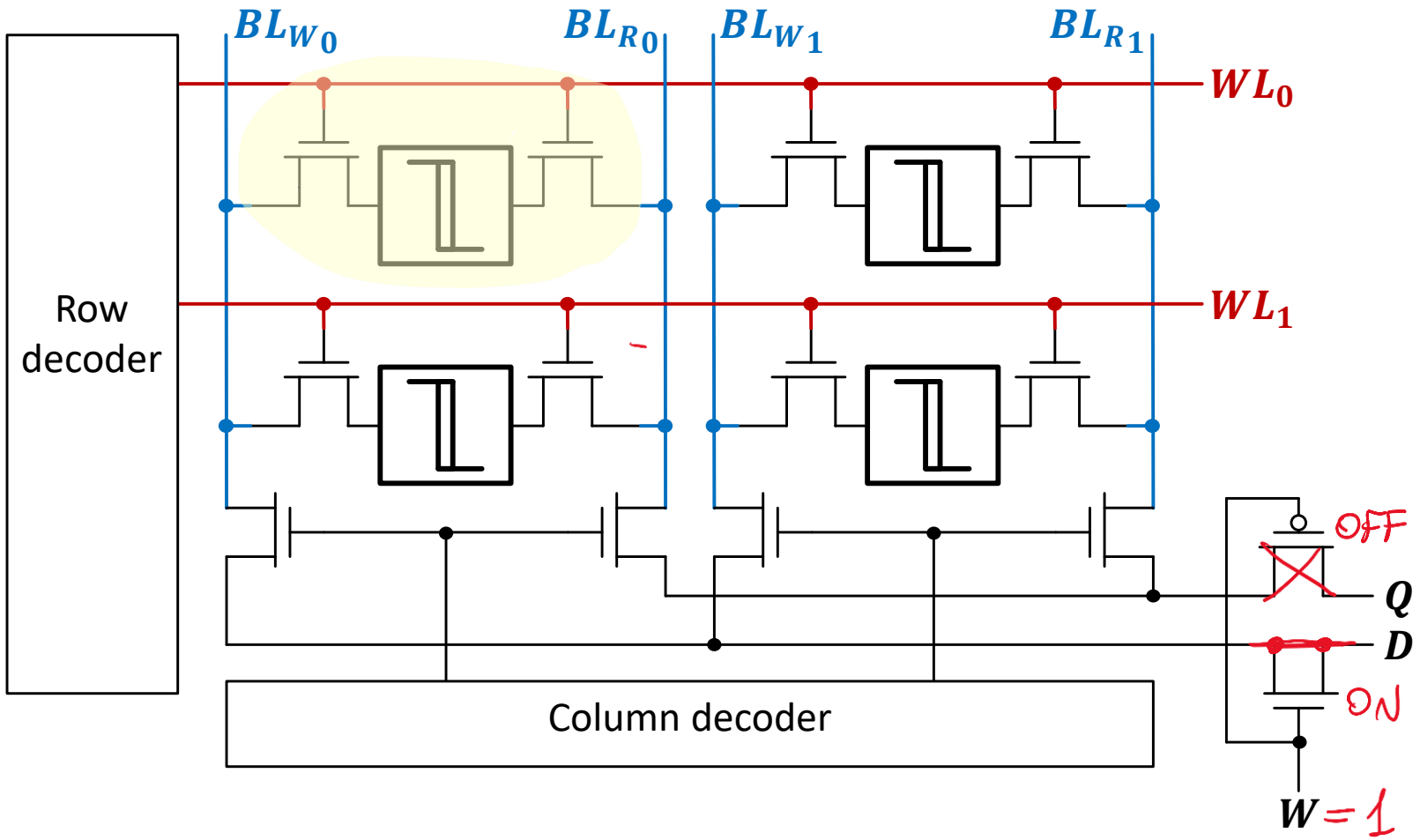

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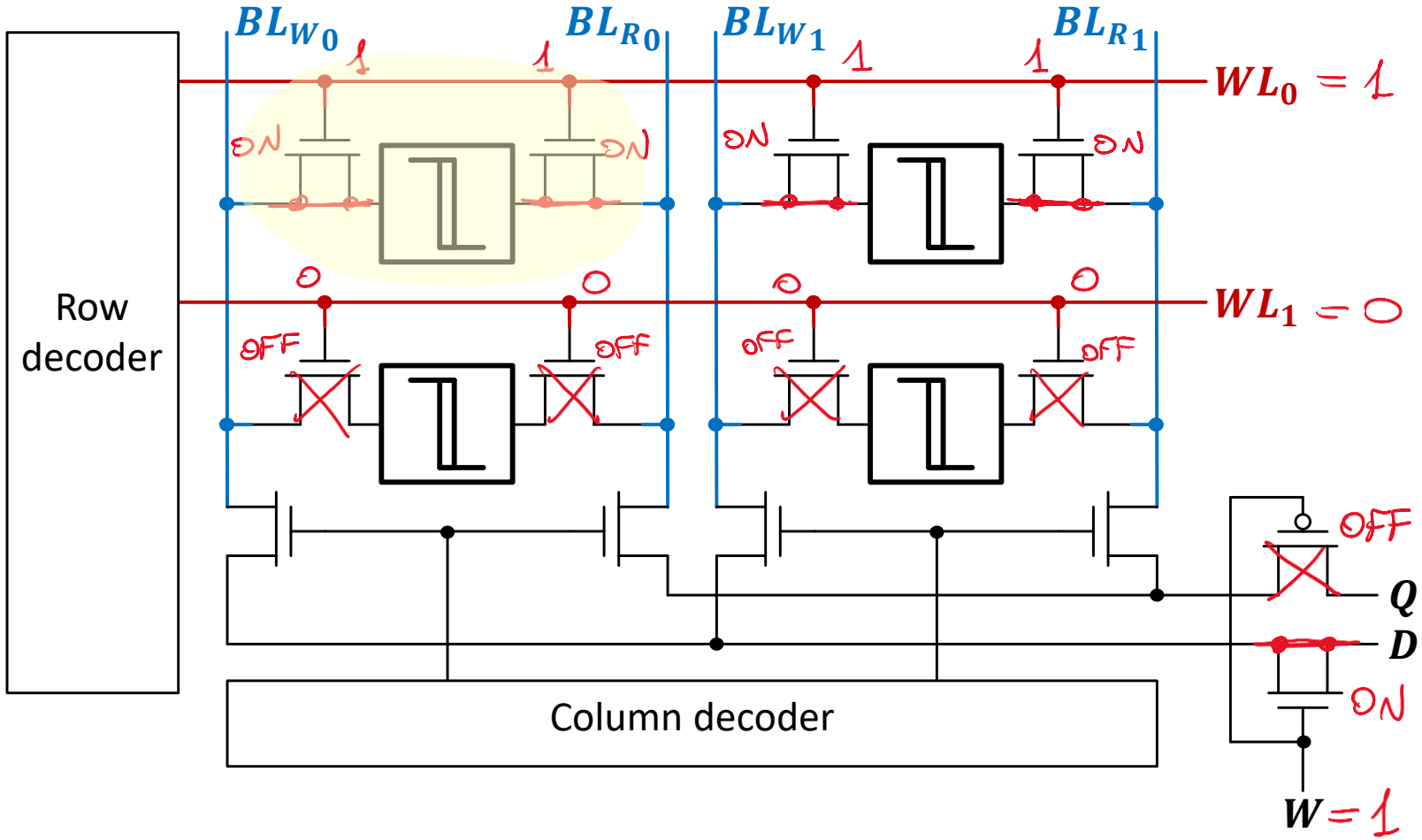

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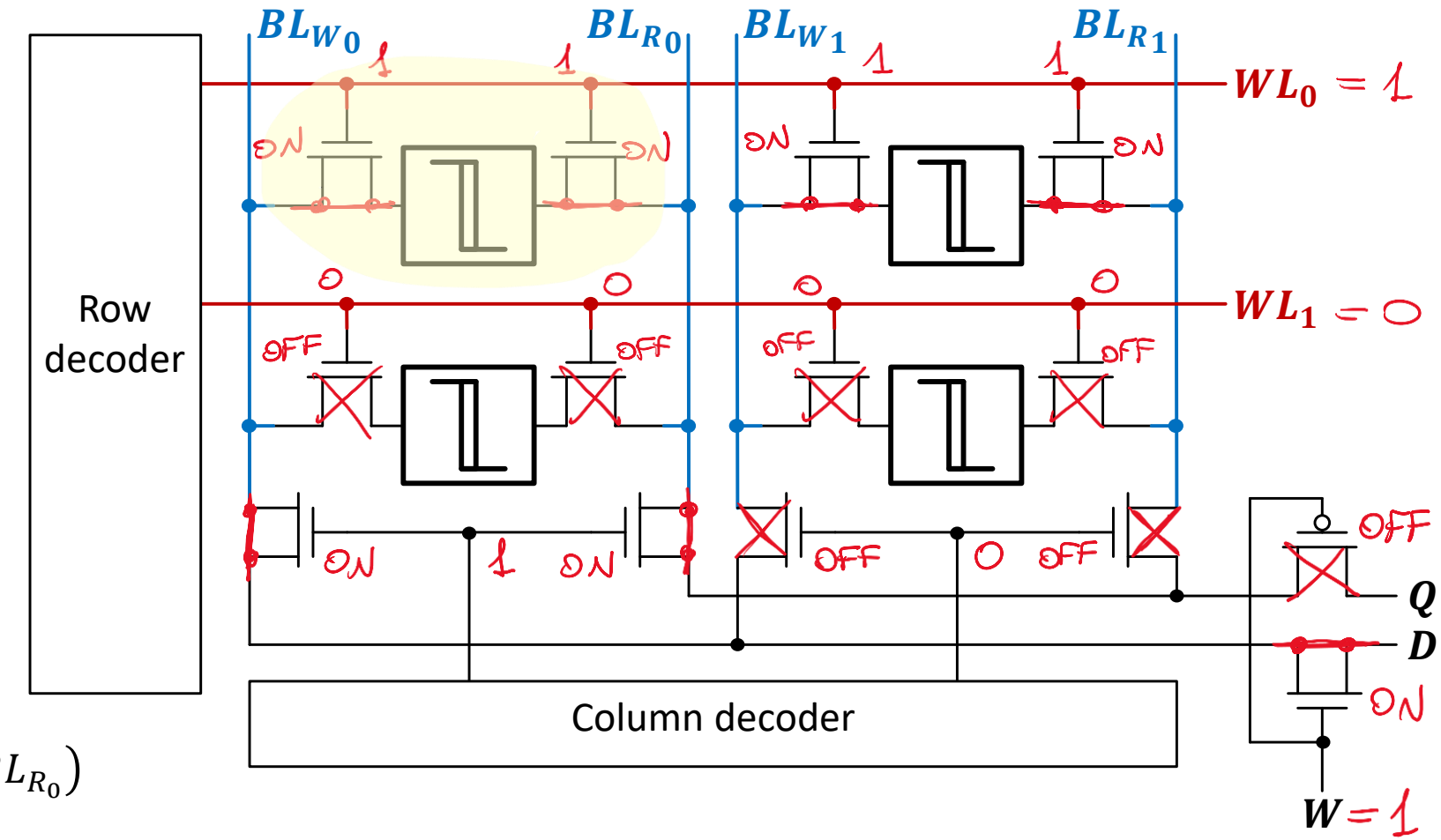

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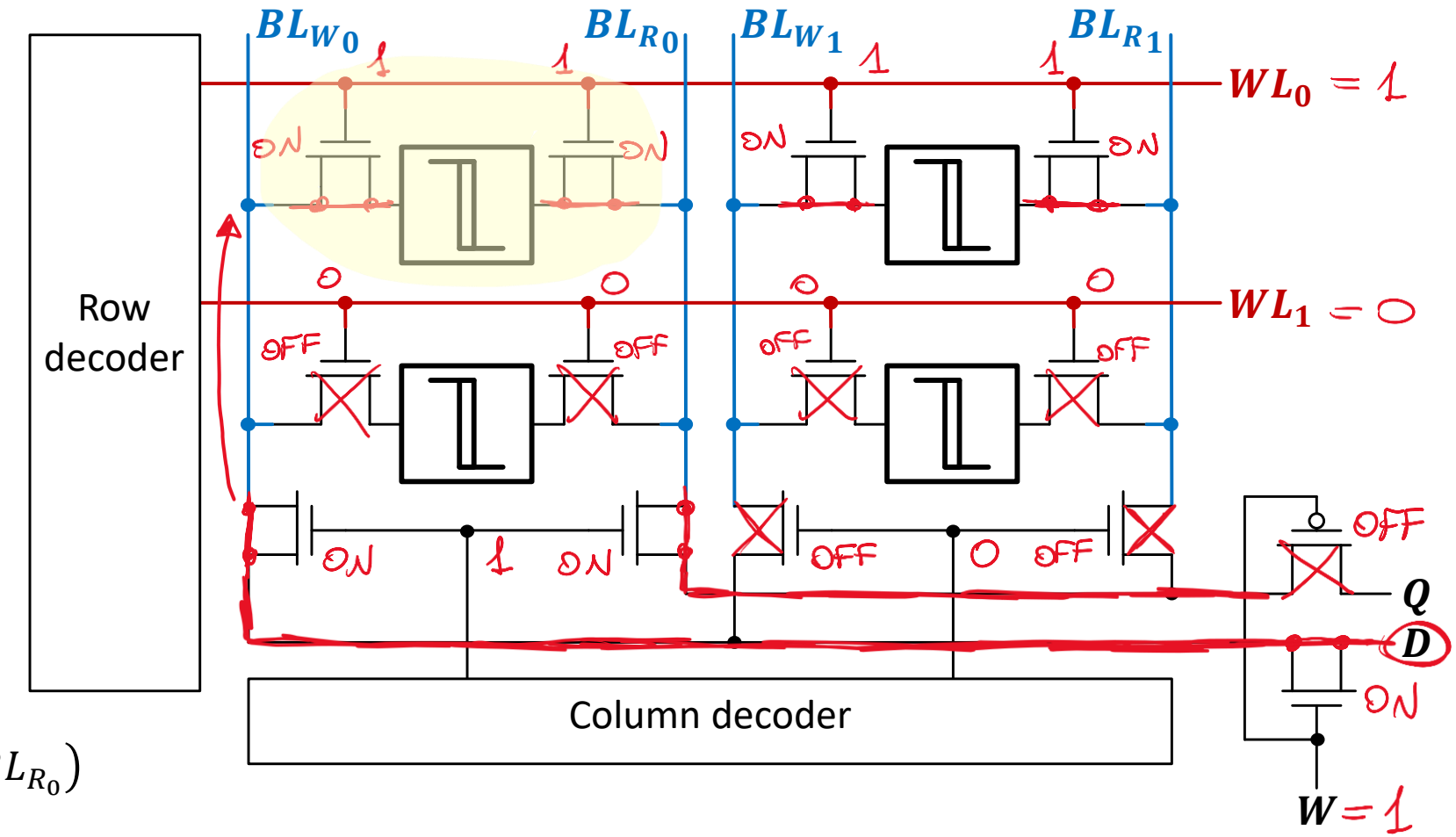

Thank you for your attention

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