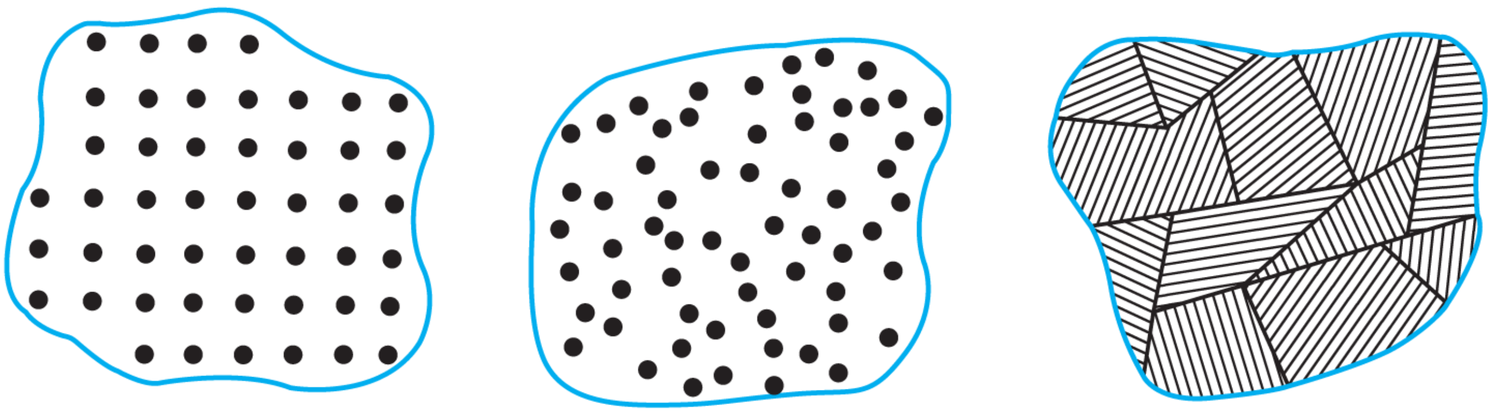
Crystal Growth and Wafer Preparation

Content

- Crystal and defects
- Si crystal growth
- GaAs crystal growth
- Gettering techniques
- Wafer specifications
- Wafer clean process

Type of Solids

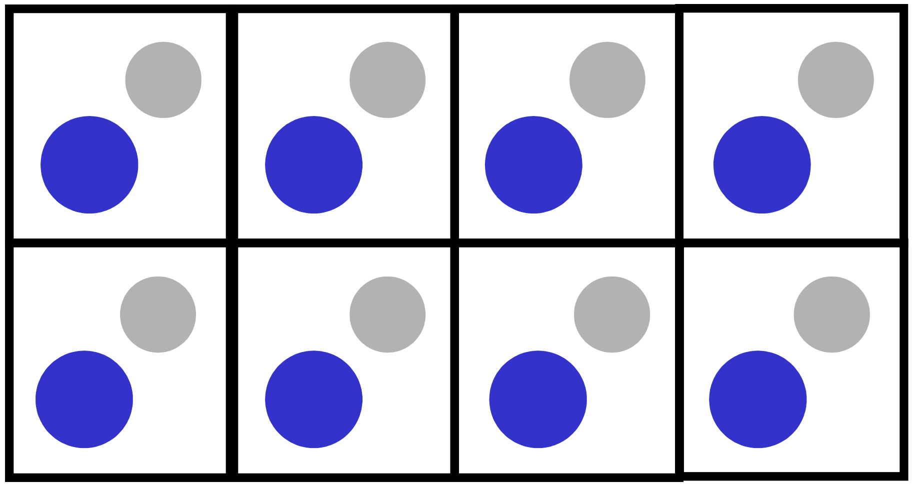
- Crystalline solid
  - The atoms making up the solid are arranged in a periodic fashion.
- Amorphous solid
  - No periodic structure at all.
- Polycrystalline solid
  - The solid composed of many small regions of single-crystal material.
- IC manufacturing needs single-crystal semiconductor in order to boost device performance and speed up circuit operation.



(a) Crystalline (b) Amorphous (c) Polycrystalline

How to Describe a Crystal ?

- Lattice
  - A regular periodic arrangement of points in space.
  - A lattice is a mathematical abstraction.
- Basis
  - A group of atoms.
- Crystal structure
  - Lattice + basis = crystal structure



- Unit cell
  - Representative of the entire lattice and is regularly repeated through the crystal.
- Primitive cell
  - The smallest unit cell that can be repeated to form the lattice.
  - There is a density of one lattice point per primitive cell.

How to Describe a Crystal ?

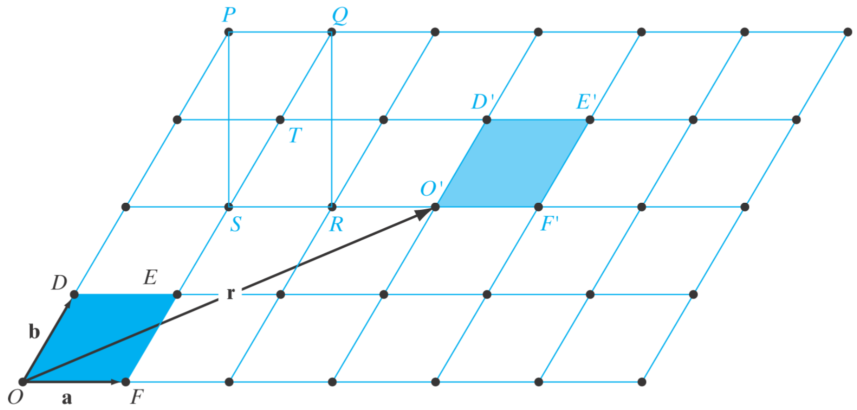
Lattice translation vector

- An ideal crystal is composed of atoms arranged on a lattice defined by three fundamental translation vector a, b, c such that the atomic arrangement looks the same in every respect when viewed from any point r.

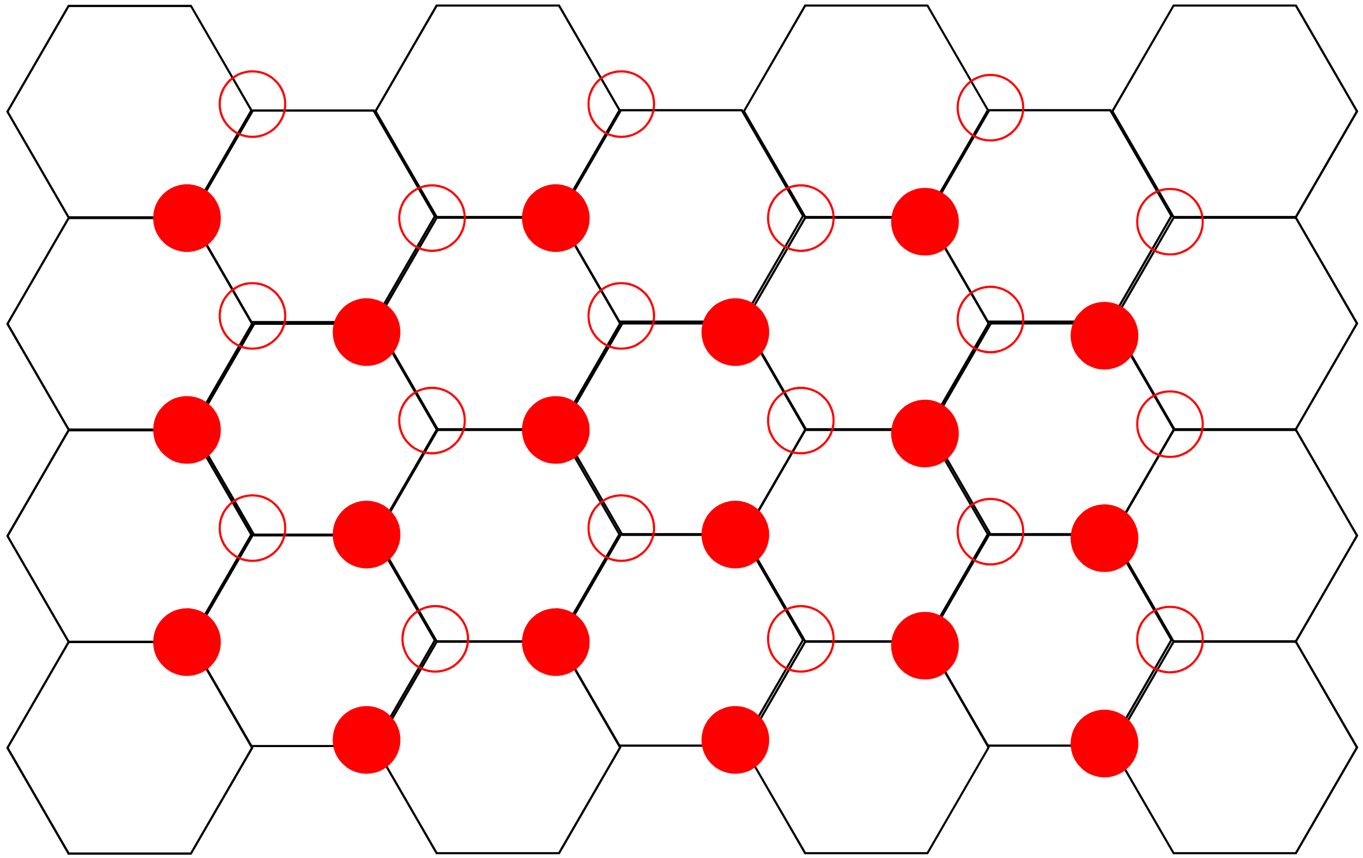
$$r = pa + qb + sc$$

Primitive vector (Basic vector)

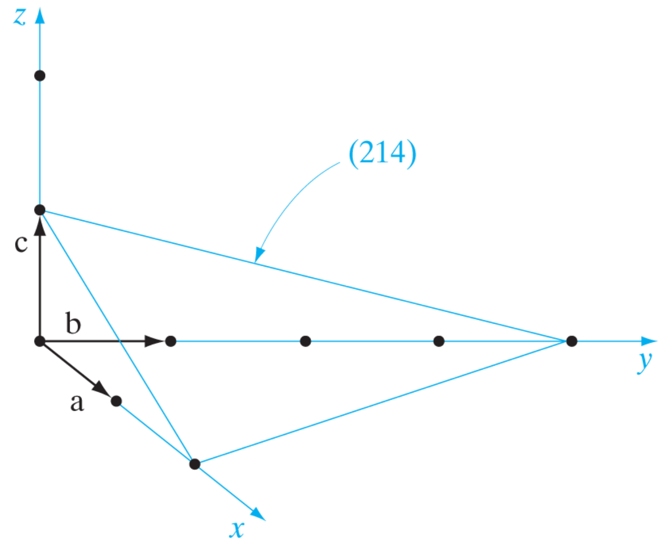
- As the unit cell is translated by integral multiples of these vectors, a new unit cell identical to the original is found.



Example of Lattice and Basis



Crystal Plane

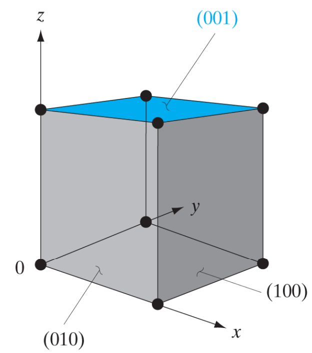


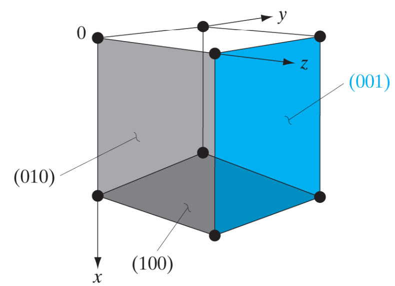
➢ Describe a particular plane *(h k l)*

- Find the intercepts of the plane with the crystal axes and express these intercepts as integral multiples of the basic vectors.
- Take the reciprocals of the three integers found in step 1 and reduce these to the smallest set of integers h, k, and l, which have the same relationship to each other as the three reciprocals.

➢ Miller indices

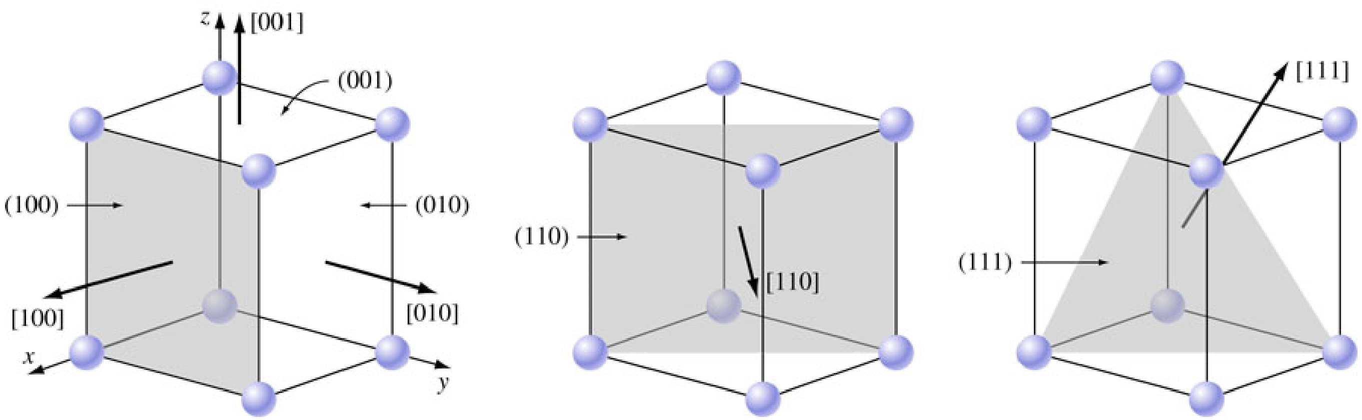
- The three integers *h*, *k*, and *l are the Miller indices*.
- A plane with given Miller indices can be shifted about in the lattice simple by choice of the position and orientation of the unit cell.
- Minus sign is placed above the Miller index for convenience, such as $(h\,\bar{k}\,l)$.
- Many planes in a lattice are equivalent. These planes are collectively designated as ***{h k l}***





Crystal Direction

- Describe a particular direction ***[h k l]***
  - A direction is expressed as a set of three integers with the same relationship as the components of a vector in that direction.
  - The three vector components are expressed as multiples of the basic vectors.
  - The three integers are reduced to their smallest values while retaining the relationship among them.
  - Many directions in a lattice are equivalent, depending only on the arbitrary choice of orientation for the axes. These directions are collectively designated as ***<h k l>***.



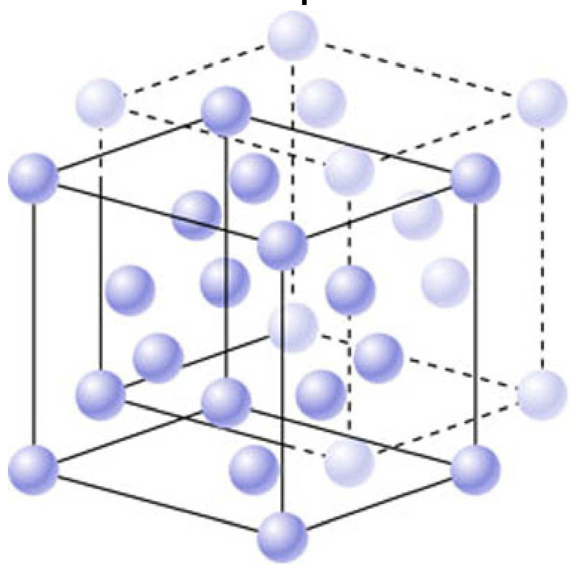
Diamond & Zinc blende Lattice -1

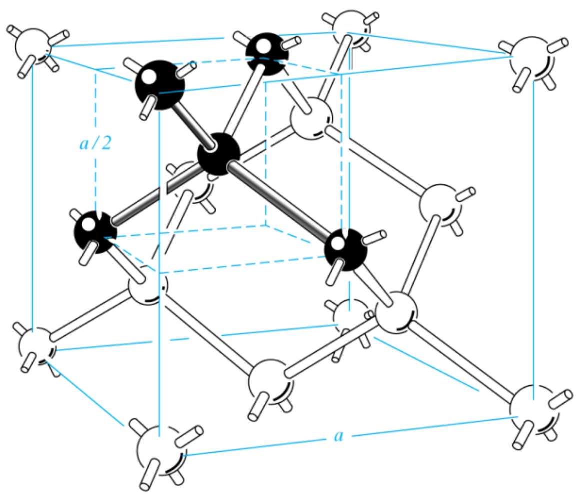
➢ Diamond lattice

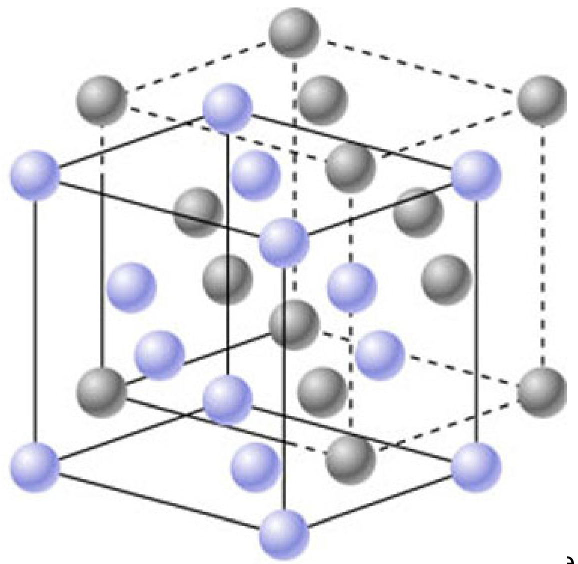
- The diamond lattice can be thought of as an fcc structure with an extra atom placed at $\frac{a}{4}+\frac{b}{4}+\frac{c}{4}$ from each of the fcc atoms.
- It can be constructed as an original fcc associates with a second interpenetrating fcc displaced by ¼, ¼, ¼.
- Example : C (a = 3.567Å), Si (a = 5.43Å), and Ge (a = 5.658Å).

➢ Zinc blende (ZnS) lattice

- The atoms of diamond structure differ on alternating sites.
- Example : GaAs.







Diamond & Zinc blende Lattice -2

➢ Ternary compound semiconductors

- It is possible to vary the composition of ternary alloy by choosing the fraction of Al or Ga atoms on the column III sub-lattice.
- $Al_xGa_{1-x}As$ refers to a ternary alloy in which the column III sub-lattice in the zincblende structure contains a fraction x of Al atoms and 1-x of Ga atoms.
- It is possible to grow four element (quarternary) compounds such as $In_xGa_{1-x}As_yP_{1-y}$.

➢ Symmetry

- Translation, mirror reflection, rotation (1-, 2-, 3-, 4-, and 6-folds rotation)
- Crystals often can be cleaved along certain atomic planes.
- The facets of a diamond reveal the triangular, hexagonal, and rectangular symmetries of intersecting planes in various crystallographic directions.

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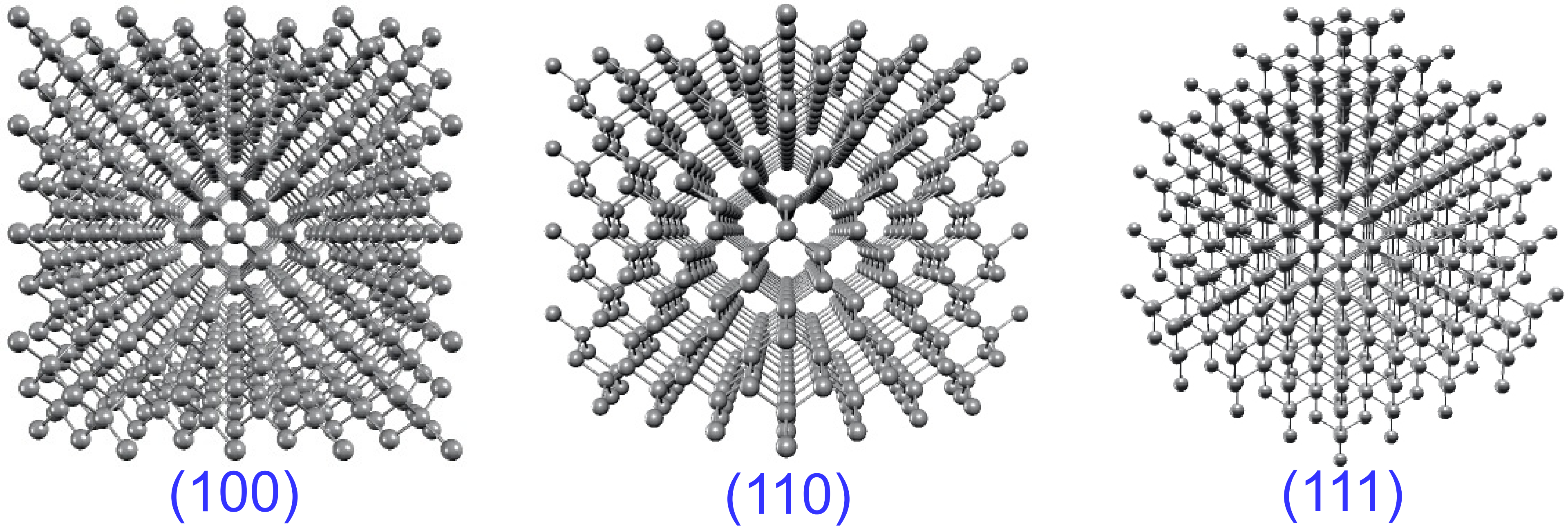
Properties of Si Crystal Planes



Orientation	Area of unit cell (cm^2)	Si atoms in area	Si bonds in area	Bonds available	Bonds 10^{14} cm^{-2}	Available bonds 10^{14} cm^{-2}	N relative to (110)
(110)	$\sqrt{2}a^2$	4	8	4	19.18	9.59	1.000
(111)	$1/2\sqrt{3}a^2$	2	4	3	15.68	11.76	1.227
(100)	a^2	2	4	2	13.55	6.77	0.707

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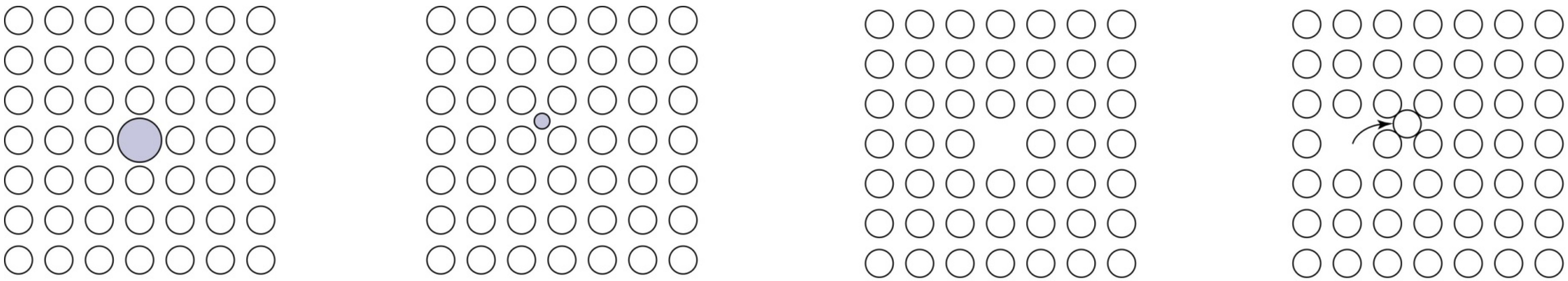
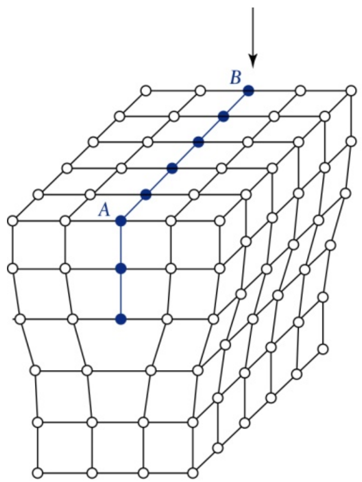
Crystal Defects

- Point defects

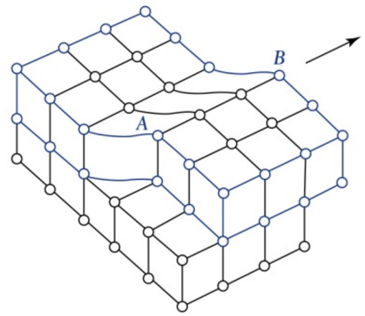


Substitutional Interstitial vacancy Frenkel-type

- Line defects (dislocation)
  - Edge :
    - Extra plane inserted.
    - Terminated at the edge of a crystal.
  - Screw :
    - Pushing part of crystal by one lattice space
    - Form a closed loop in the crystal.



Edge

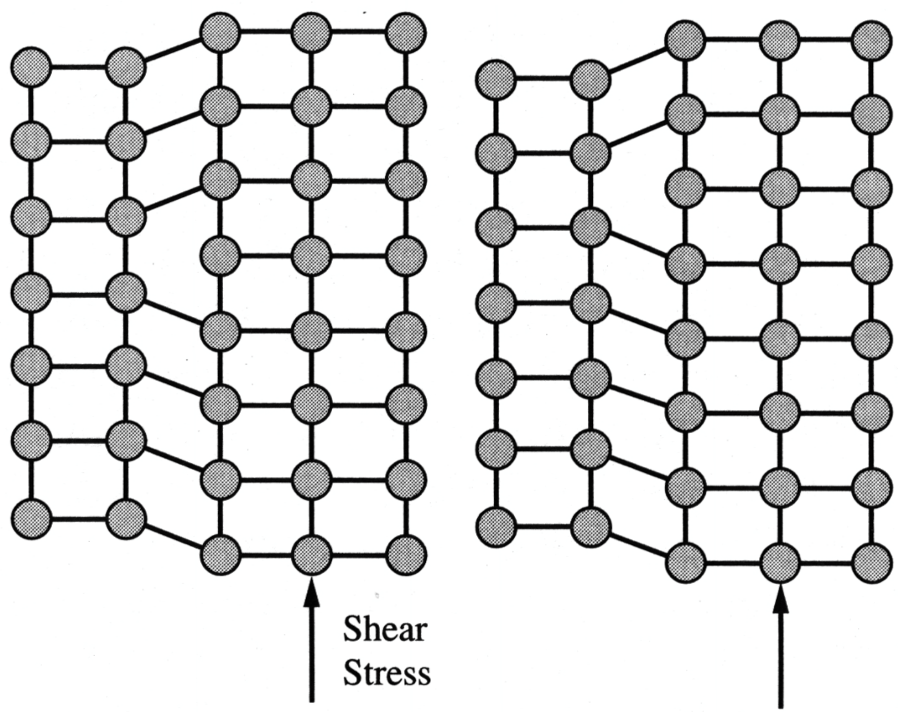


Screw

Dislocations

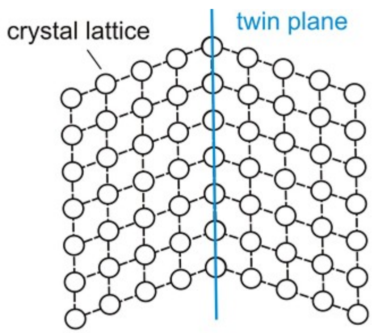
- Generated as the stress inside the wafer is sufficiently large.
  - Examples: (1) SiN capping; (2) SiGe/SiC heteroepitaxy; (3) High temperature gradient during rapid thermal processing.
- Movable when subjected to stresses or when excess points are present.

Movement of a dislocation by gliding in response to the shear stress

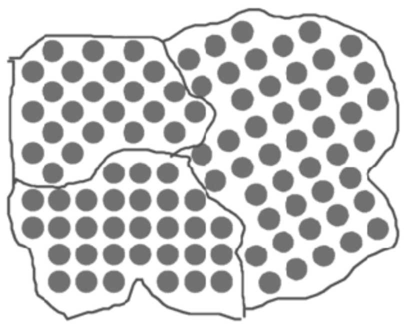


Crystal Defects

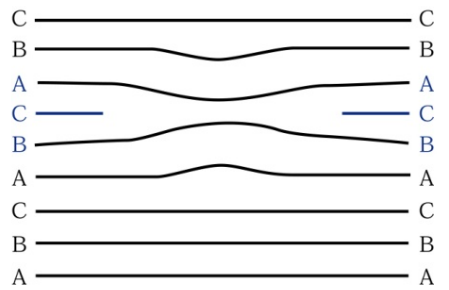
- **Area defects**
  - Twins : a change in the crystal orientation across a plane
  - Grain boundary : a transition between crystals having no particular orientation relationship
  - Stacking fault
- **Volume defects**
  - Participates of impurities or dopants.



Twins crystal

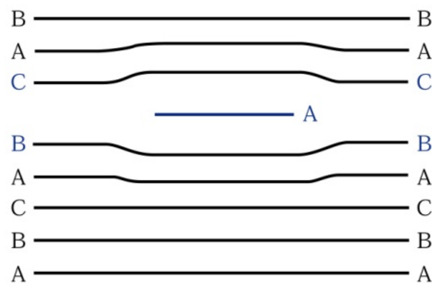


Grain Boundary



Intrinsic stacking fault

a plane is missing (ABCABABC, etc).



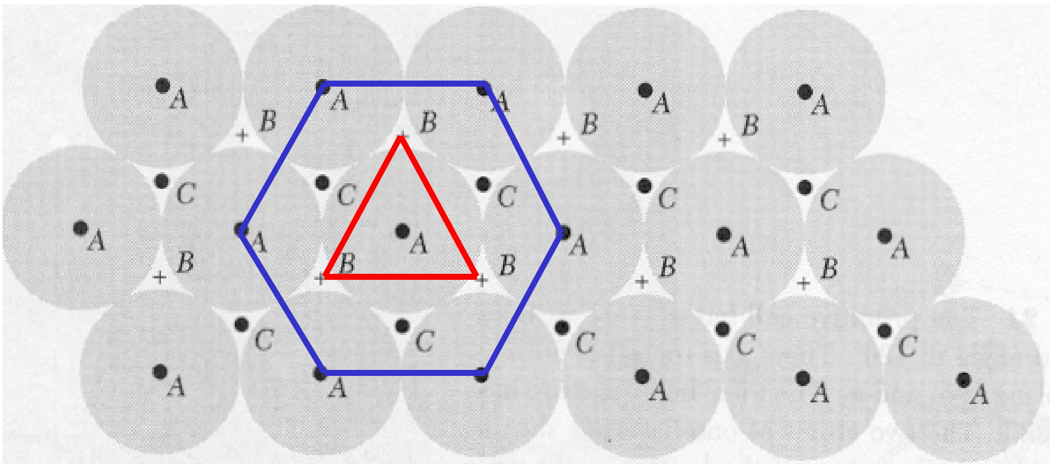
Extrinsic stacking fault

An extra plane is inserted

(ABCABACAB, etc).

Stacking Faults

- Always form along {111} planes, and are simply the insertion or removal of an extra {111} plane.
- Normally there are three parallel {111} planes, referred to as A, B, and C, in each unit cell of an fcc lattice. The stacking order is ABCABC--- in a perfect crystal.

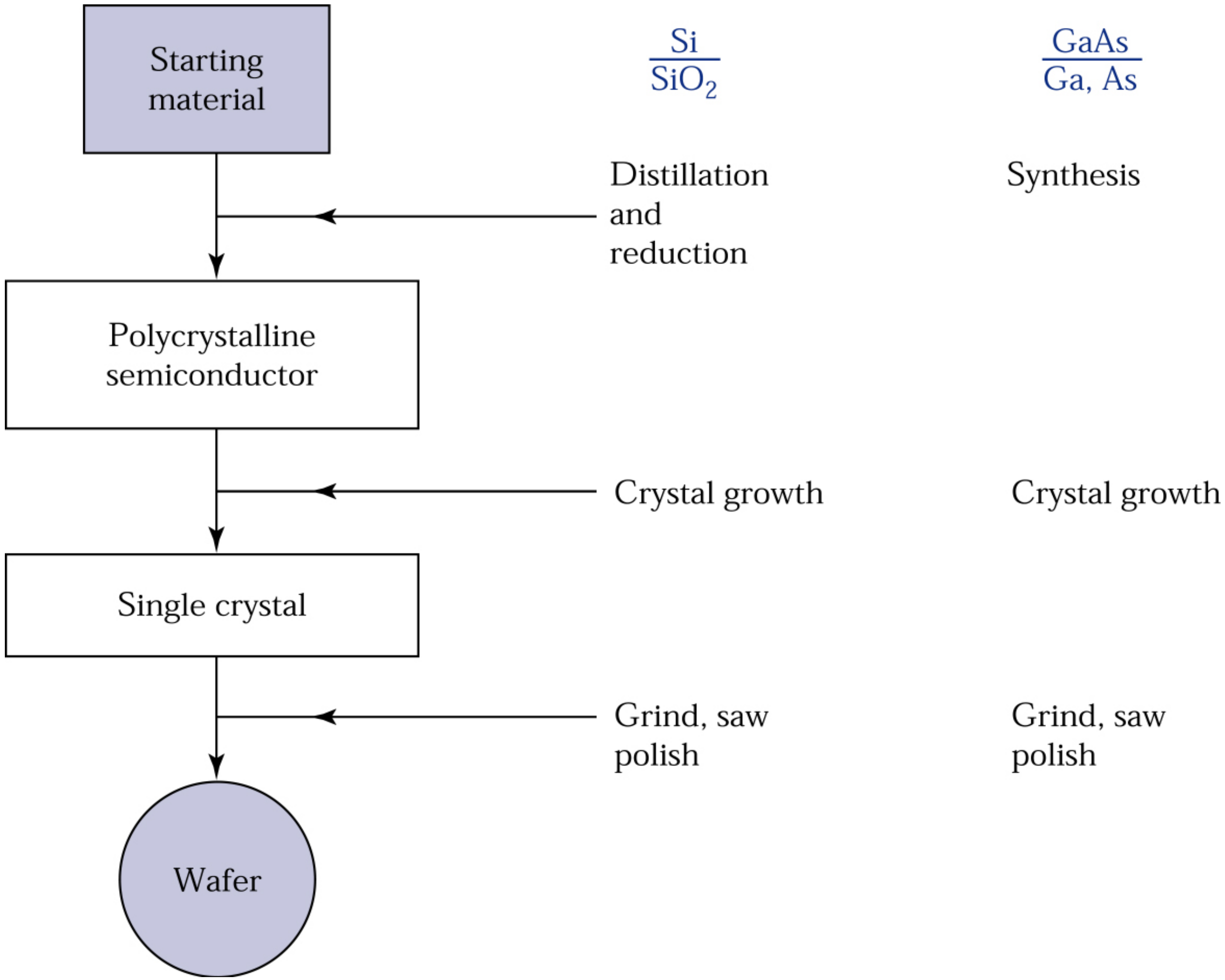


Closest-packed layers of spheres

- Centers of spheres in the first layer: A
- Centers of spheres in the second layer: B
- Centers of spheres in the third layer: C or A

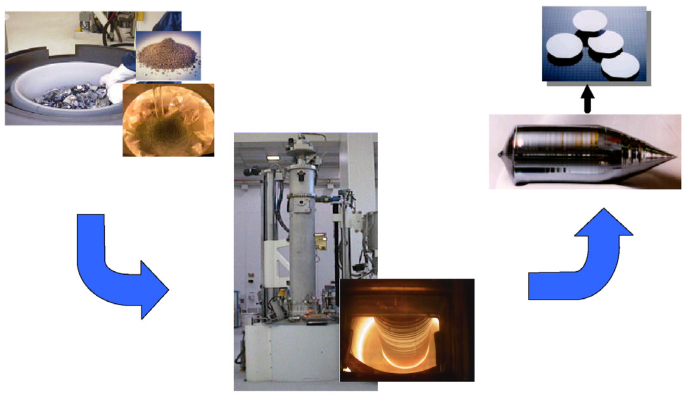
- fcc: stack sequence ABCABC
- hcp: stack sequence ABABAB ----
- Both may have closest-packed ratio of 0.74.

Process Flow From Starting Material To Polished Wafer



From Sand to Wafer

- Quartz sand (SiO_2) to metallic grade Si (MGS) or semiconductor grade Si (SGS)
- React MGS powder with HCl to form $SiHCl_3$ (TCS)
- Purify TCS by vaporization and condensation
- React TCS to H_2 to form polysilicon (electronic grade silicon or EGS)
- Formation of single crystal ingot with CZ or FZ method
- Cut end, polish side, and make notch or flat
- Saw ingot into wafers
- Edge rounding, lap, wet etch, and CMP
- Laser scribe



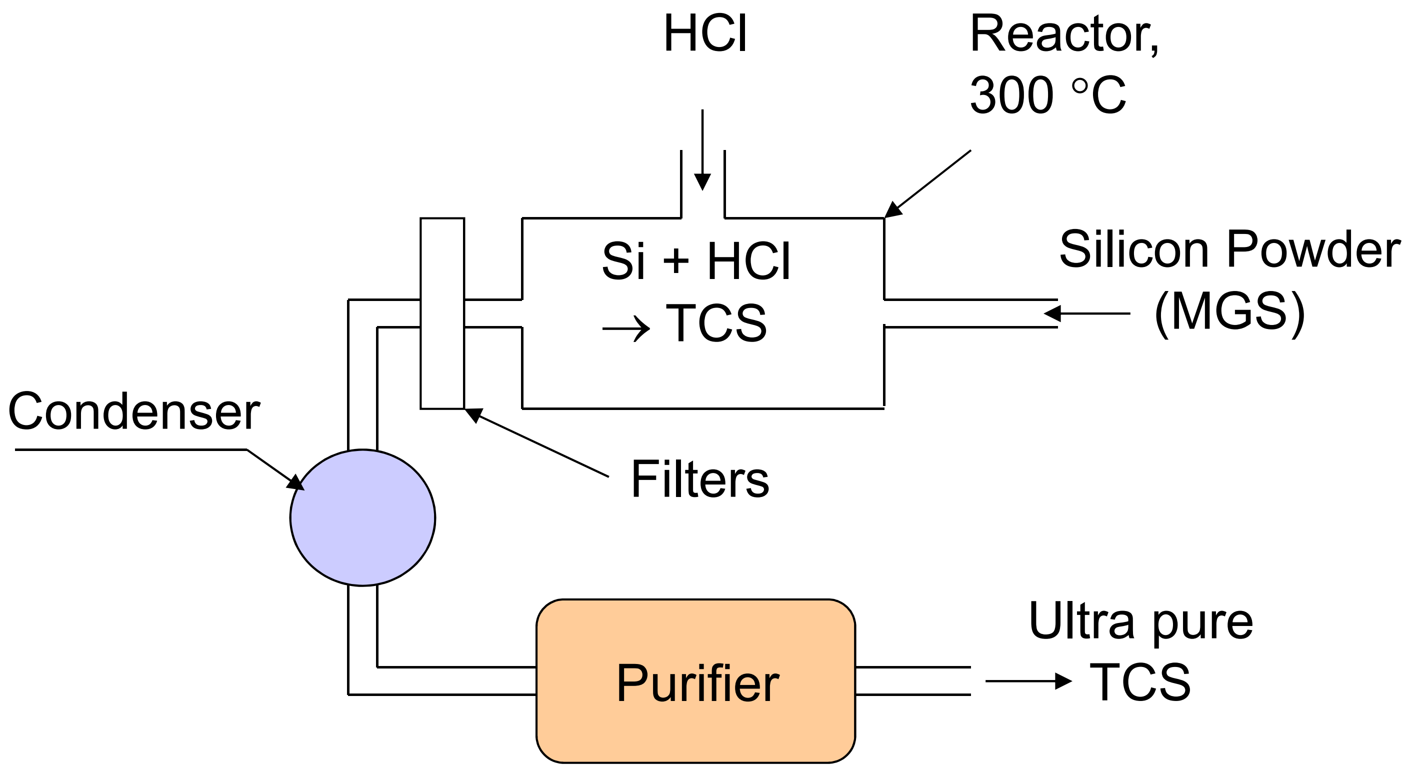
From Sands to Si Crystals

- Si contained materials ➡ Metallurgical-grade : impurity~98%

$$SiC(solid) + SiO_2(solid) \rightarrow Si(solid) + SiO(gas) + CO(gas)$$

- MGS Si ➡ Ultra pure TCS

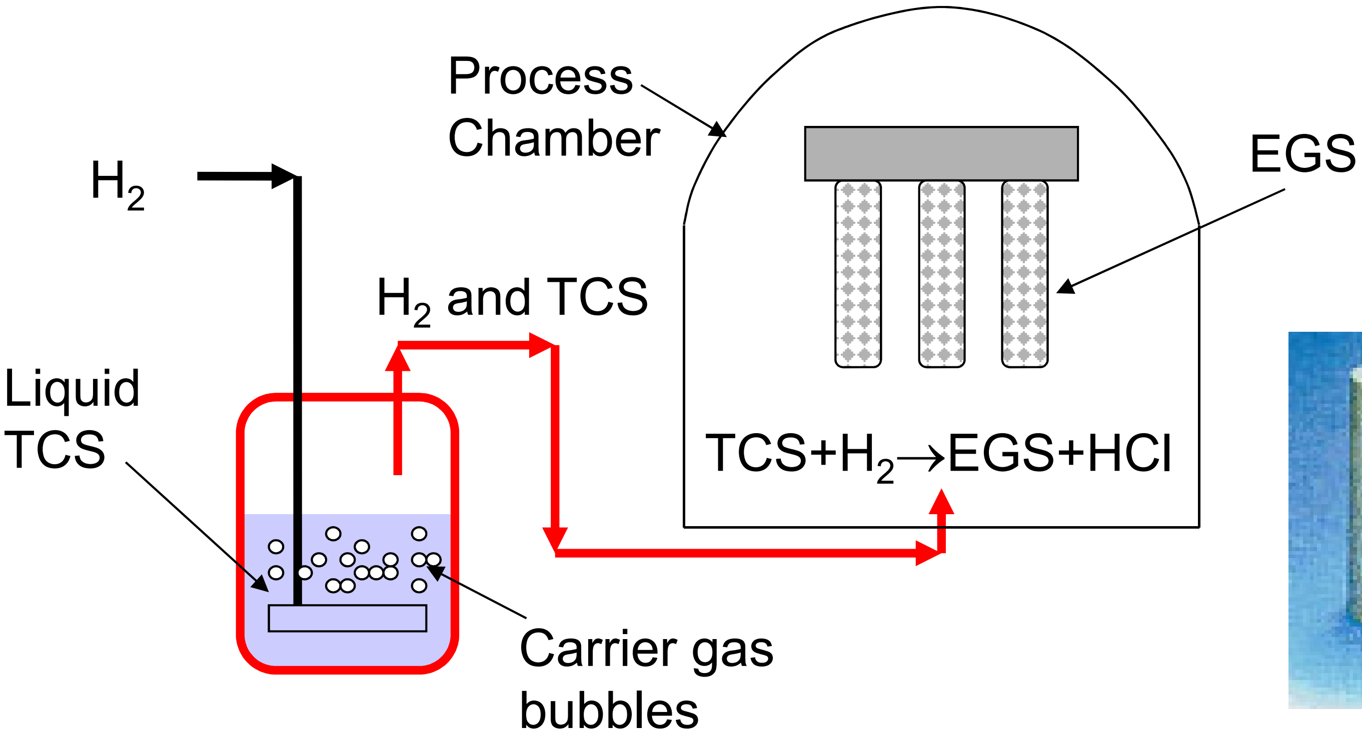
$$Si(solid) + 3HCl(gas) \xrightarrow{300°C} SiHCl_3(gas) + H_2(gas)$$

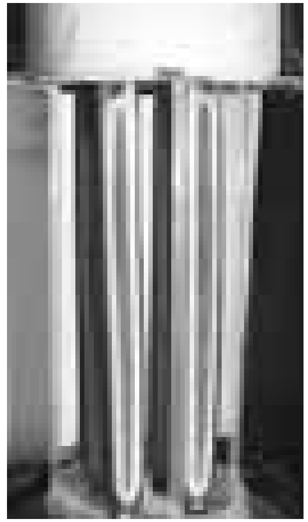


From Sands to Si Crystals

- Ultra pure TCS ➡ Electronic-grade : impurity ~ ppb

$$SiHCl_3(gas) + H_2(gas) \xrightarrow{1100°C} Si(solid) + 3HCl(gas)$$





Source: http://www.fullman.com/semiconductors/_polysilicon.html

Crystal Growth Methods

➢ Czochralski (CZ) Method:

- Dominant technique since the incept of IC industry.
- C (10^{15}~10^{16} cm^{-3}) and O (10^{17}~10^{18} cm^{-3}) contamination due to the use of crucible is a major concern, making the wafers not suitable for some specific applications (e.g., power devices).
- O doping helps increase the mechanical strength and can participate in the intrinsic gettering procedure.

➢ Float-zone (FZ) Method:

- Ultra-high purity, suitable for making power devices.
- Limited wafer size.

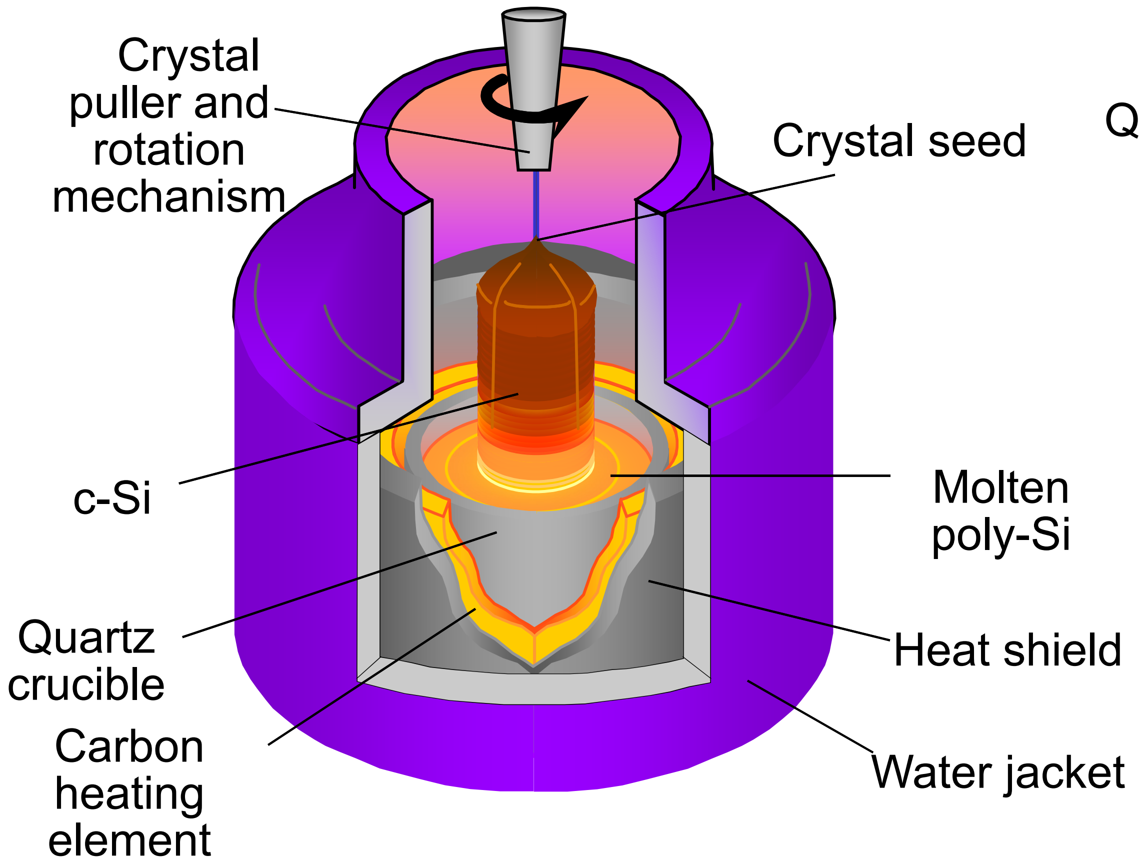
➢ Bridgman Method

- For compound semiconductor such as GaAs, etc.

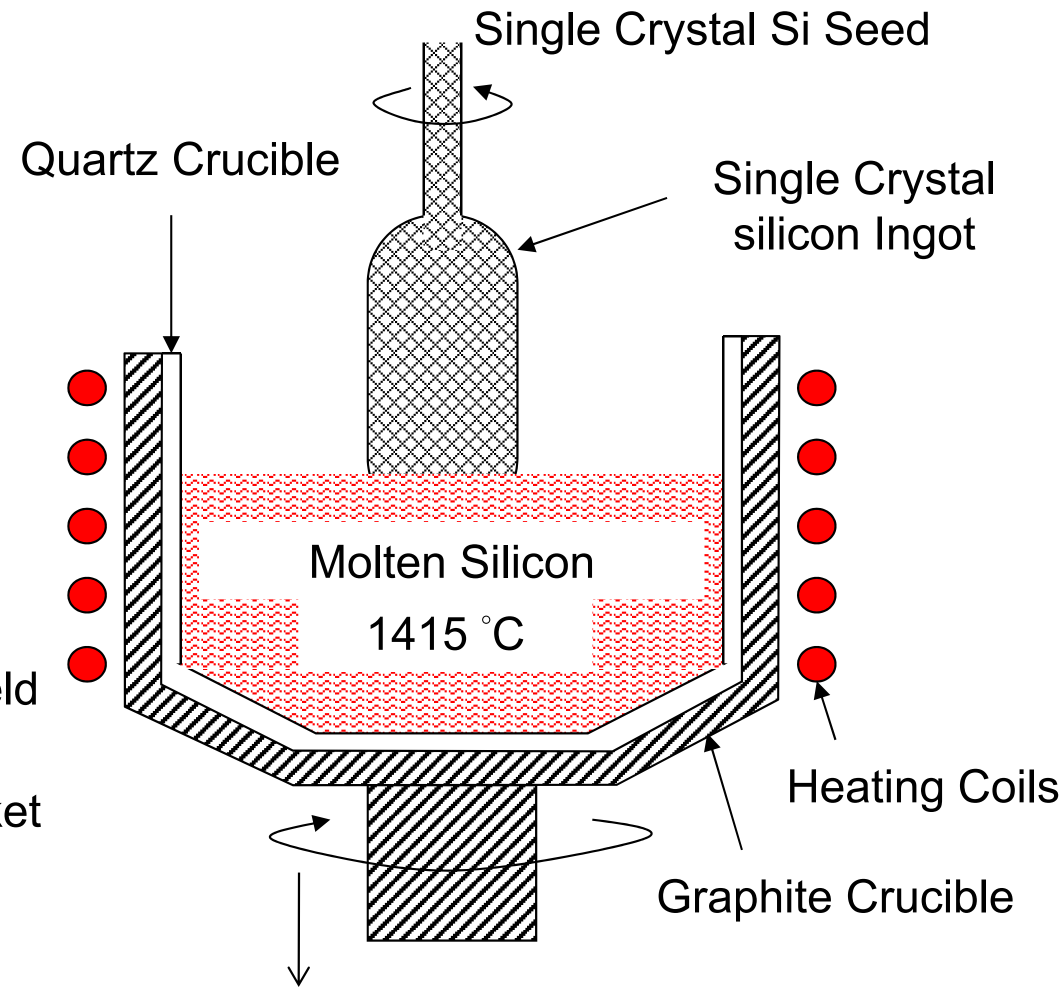
CZ Crystal Pulling

- Pieces of EGS are placed in a quartz crucible and melt.
- A small seed (a perfect Si crystal) is inserted into the molten Si, and then drawn away slowly from the surface of the melt.
- Seed determines the orientation of the pulled crystal.
- During pulling the pulled crystal rotates in a direction opposite to that of the crucible.
- Diameter of the pulled crystal mainly determined by the pulling rate.
- O contamination mainly from the quartz crucible.
- C contamination mainly from the EGS and graphite susceptor.
- Usually processed in an Ar ambient.

Crystal Pulling: CZ method



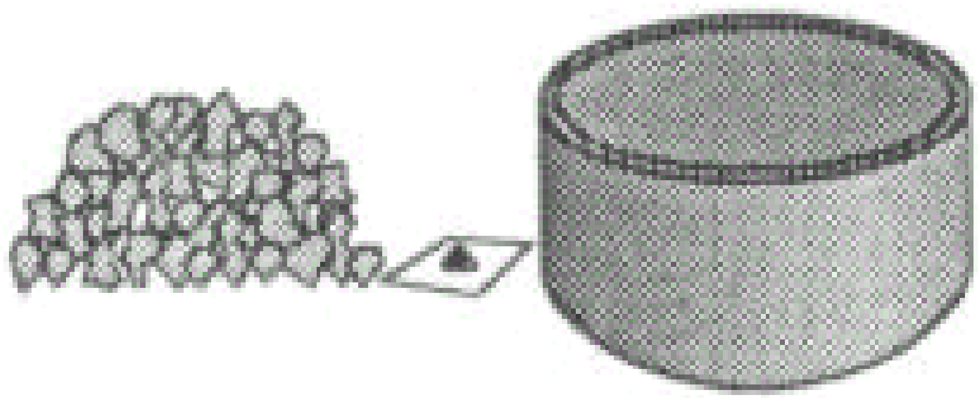
Usually performed in an Ar ambient



Rotate in a direction opposite to that of pulling seed.

Charge Preparation & Loading

- Materials gathered per specification
  - Seed
  - Dopant
  - Poly-Si
  - Quartz Crucible
  - Graphite
- Charge Placed in Puller

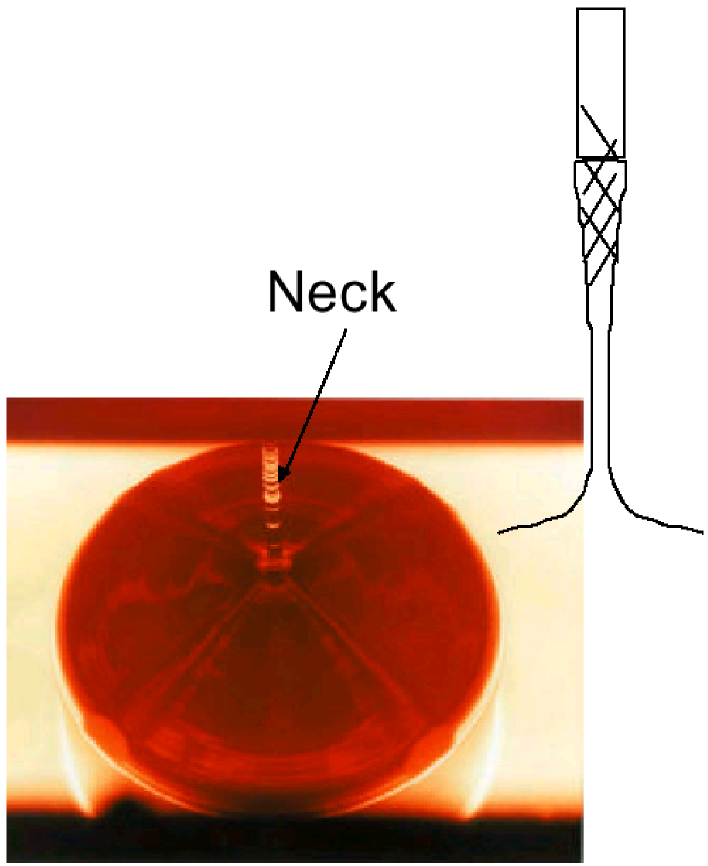


Melting/Stabilization

- Polysilicon is melted.
- Melt temperature brought to thermal equilibrium for crystal growth.
- The melting point of silicon is 1415 ºC.
- A typical 200 mm charge size can be over 100 kg and takes several hours to melt.

Seed Dip/Neck/Taper/Body Growth

- Seed placed in contact with melt.
- Neck growth to eliminate dislocations generated by thermal shock to seed crystal when it touches the melt.
- The neck is only 4-6 mm thick for a modern large diameter crystal but can still support the weight of the crystal.
- Taper grown to transition to required diameter. The diameter is typically a few millimeters more than 200 mm to allow for grinding.



Czochralski Method for Crystal Growth

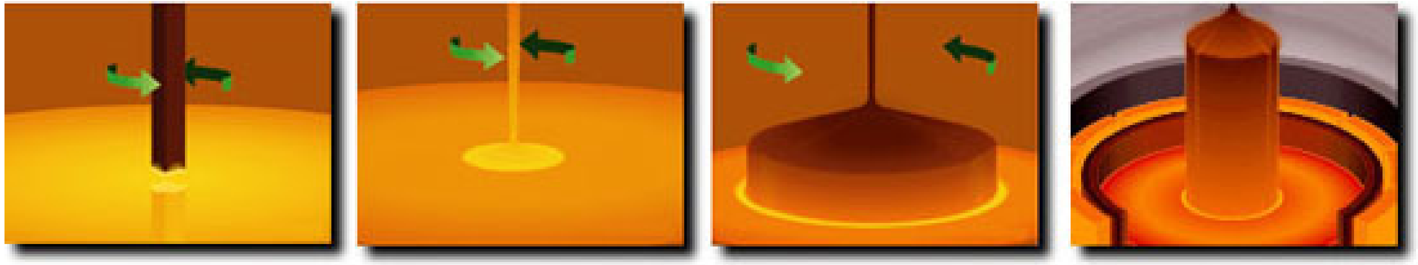
- Maximum pulling rate:

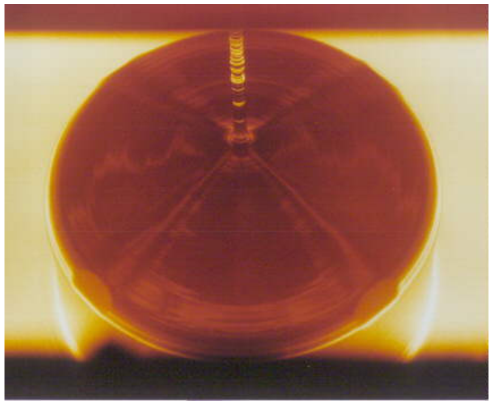
$$v_{PMAX} = \frac{1}{LN}\sqrt{\frac{cT_M^5}{3r}} \propto \sqrt{\frac{1}{r}}$$

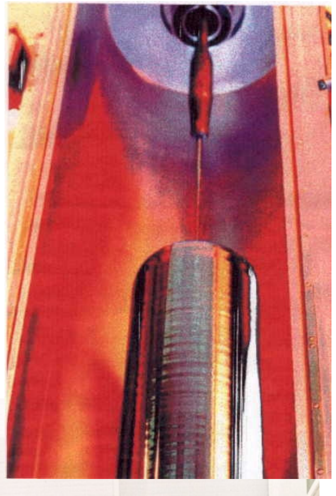
L: latent heat of fusion;
N: density of Si;
r: radius of the ingot;
T_M: melting temperature of Si;
c: a constant.

- Typical growth rates for a 200 mm crystal are 0.3 ~ 1.5 mm/min.
- Typical cooling rate during crystal growth are 0.3 - 3.0 ºC/min
- Oxygen incorporation into crystal is 8 ~17 ppma.

CZ Crystal Pulling





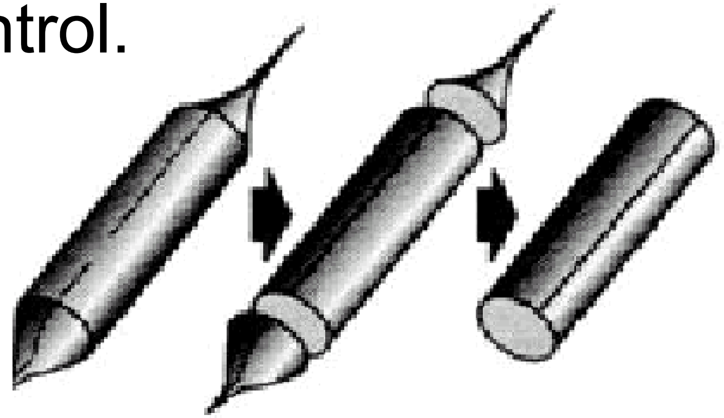


Source: www.fullman.com/semiconductors/_crystalgrowing.html

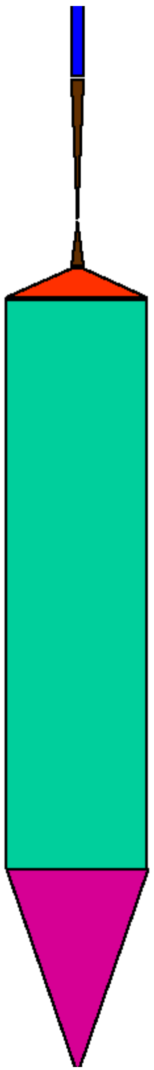
Photograph courtesy of Kayex Corp.,
300 mm Si crystal puller

Endcone/Cooling/Modification

- Endcone or bottom - Diameter reduced to a point to prevent thermal shockback when the crystal is removed from the melt.
- Crystal cooled prior to removal/handling. This takes several hours as the crystal has to cool below 300 ~ 400 ºC before it can be handled.
- Crystal taper and endcone "cropped".
- Control slugs taken to verify process control.



Crystal Parts



Seed - determines crystal orientation

Neck - removes the dislocations generated by thermal shock when seed is dipped into the melt.

Shoulder or taper - transitions to required diameter

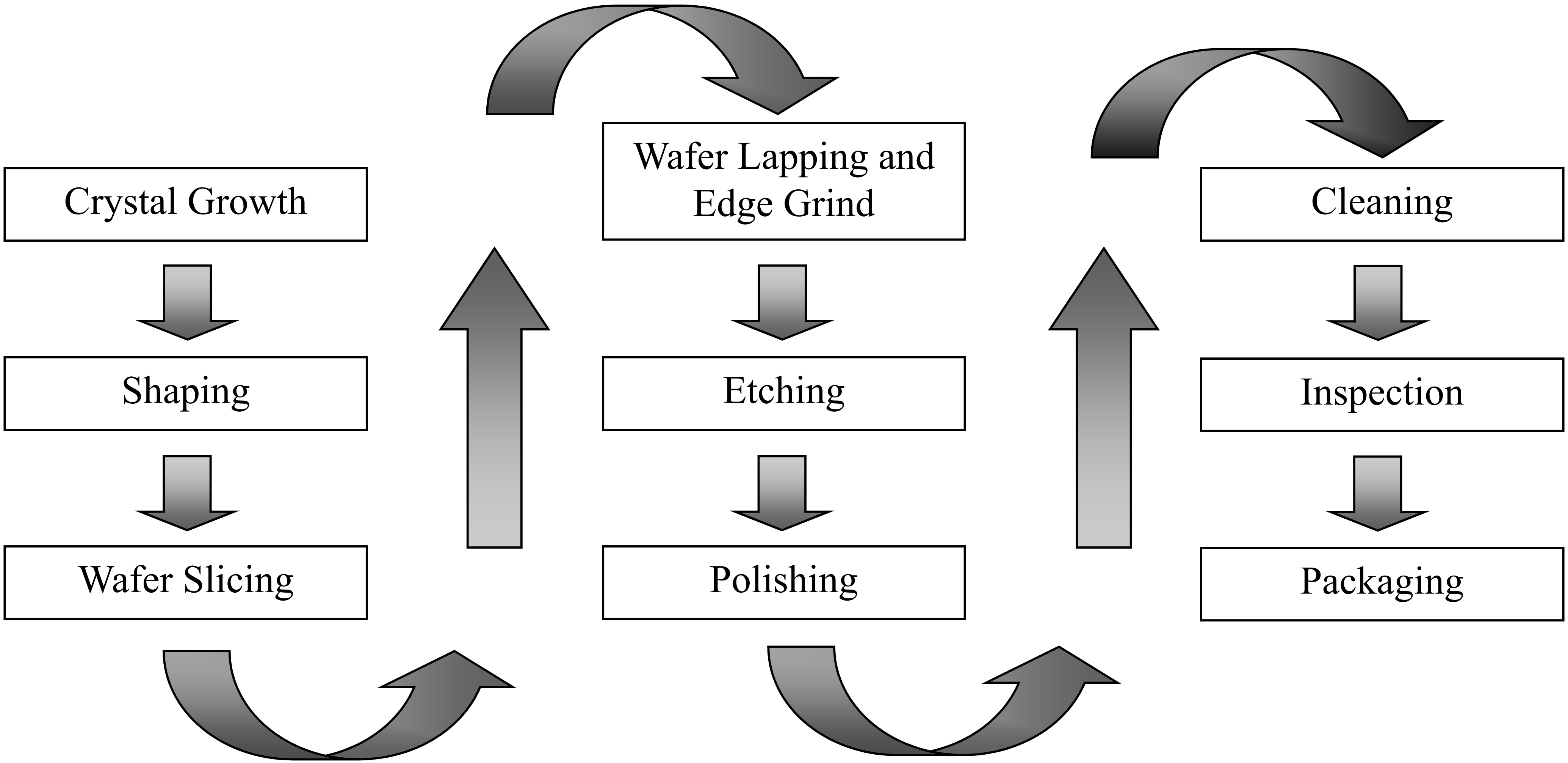
Body - Part of the crystal actually used for wafers

Endcone or bottom - prevents shockback into the body when the crystal is removed from the melt

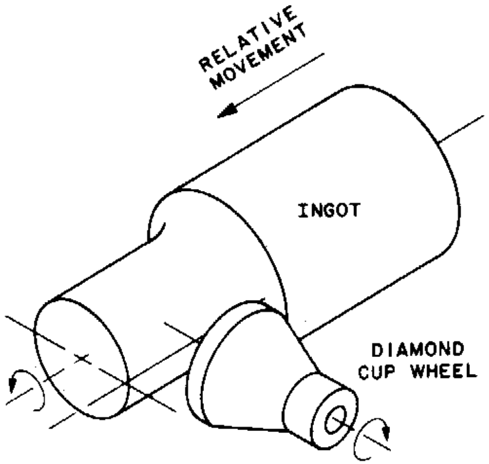
300 mm Ingot

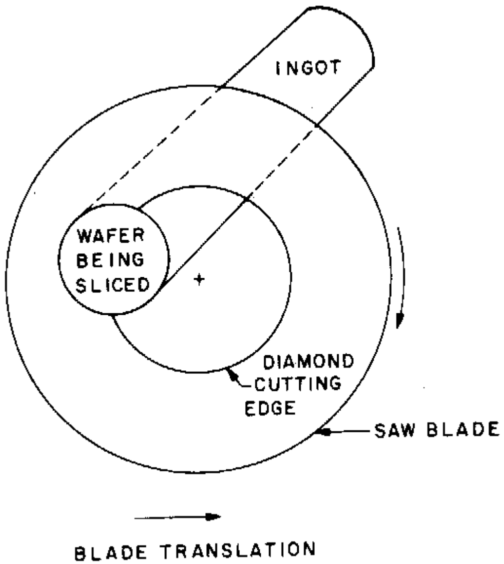
400 mm Ingot

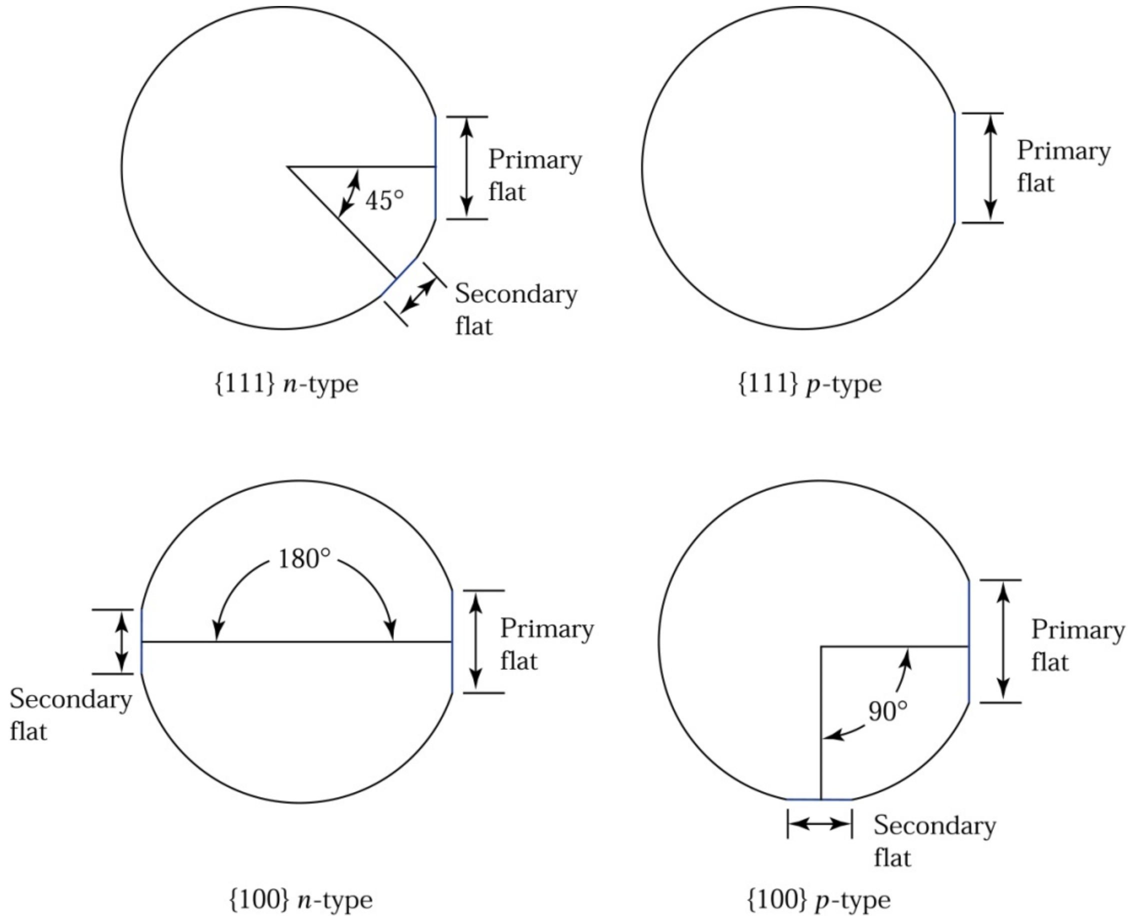
Process Steps for Wafer Preparation



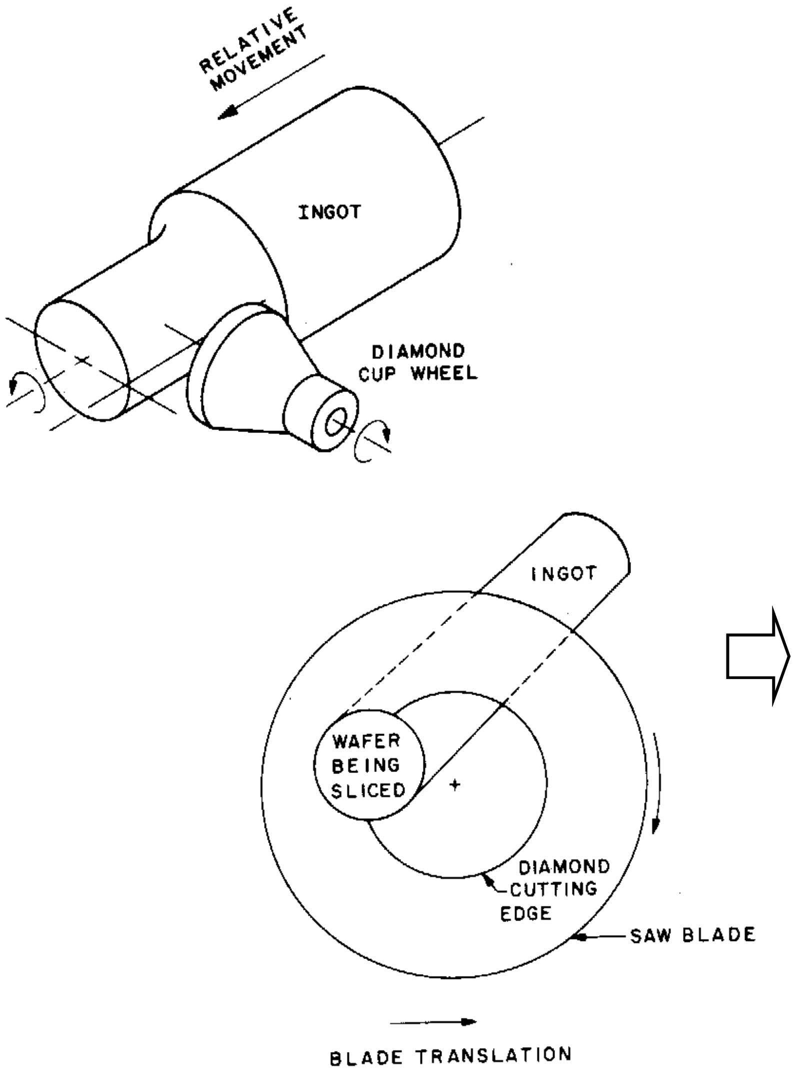
Grinding and Slicing

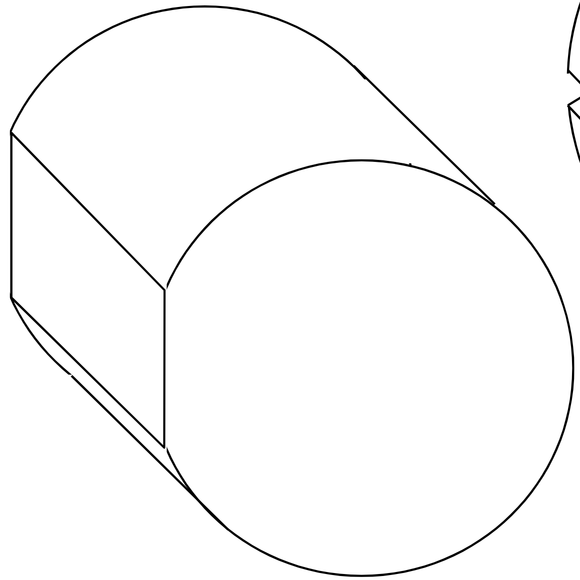




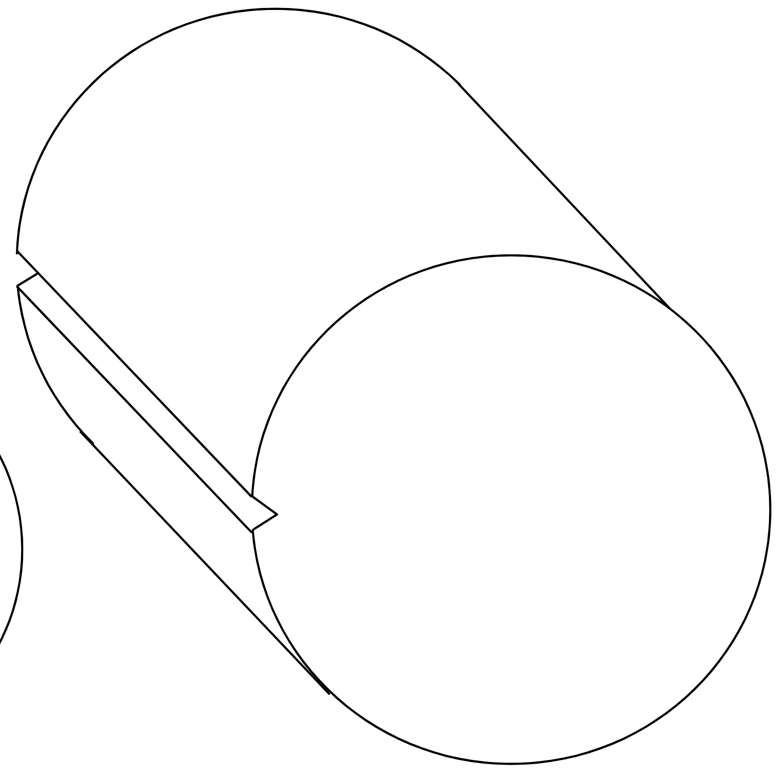


Ingot Polishing/Flat or Notch





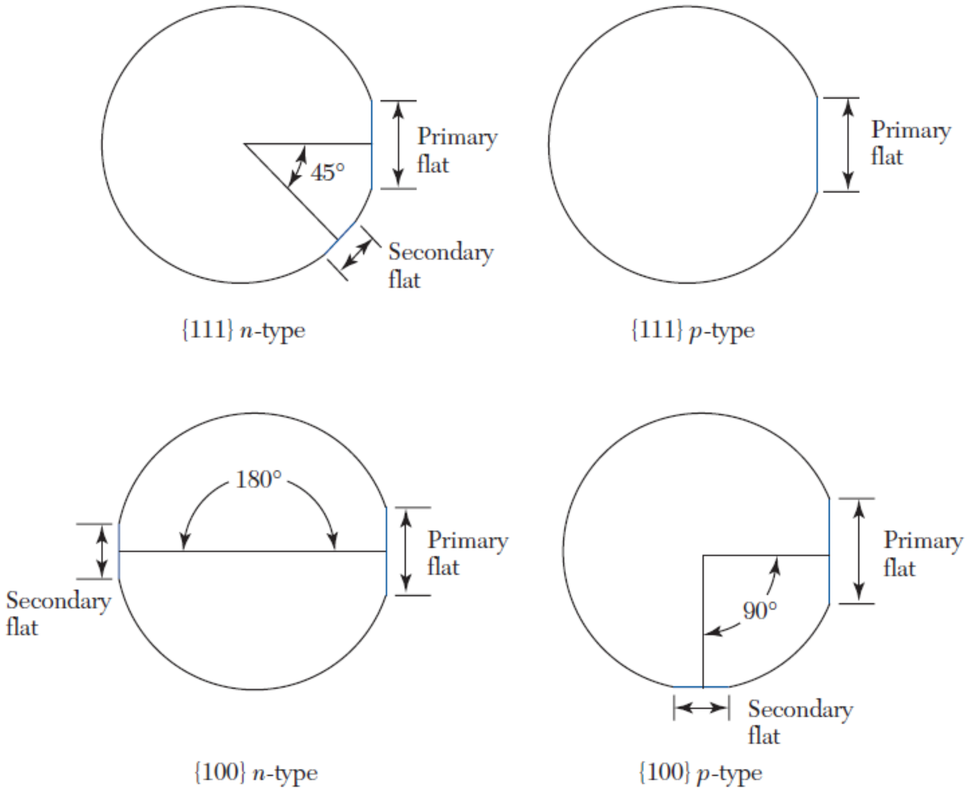
Flat,
150 mm and smaller



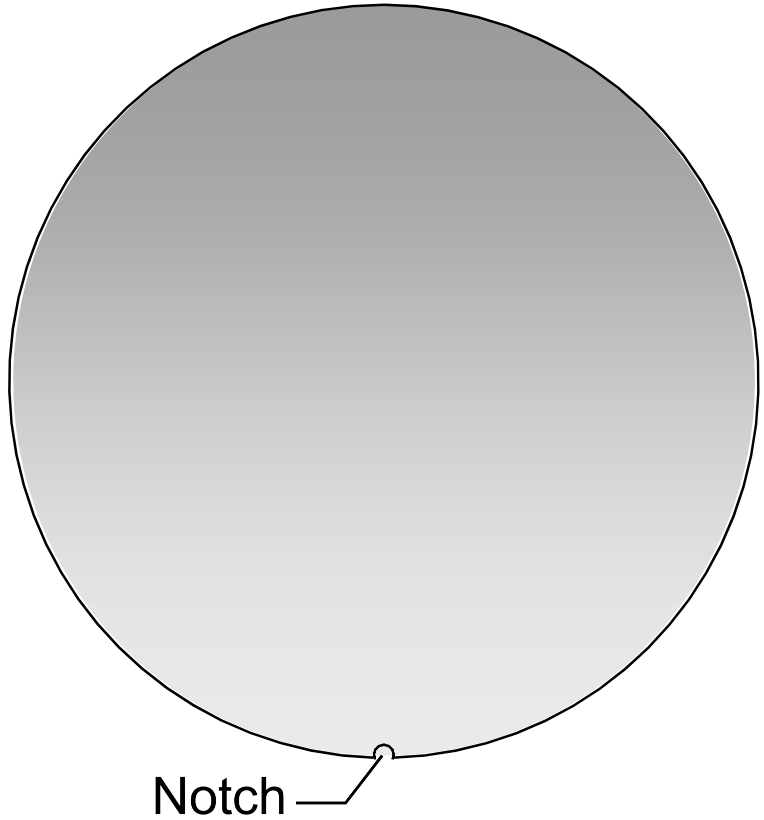
Notch,
200 mm and larger

Wafer Flat and Notch

Flat, 150 mm and smaller

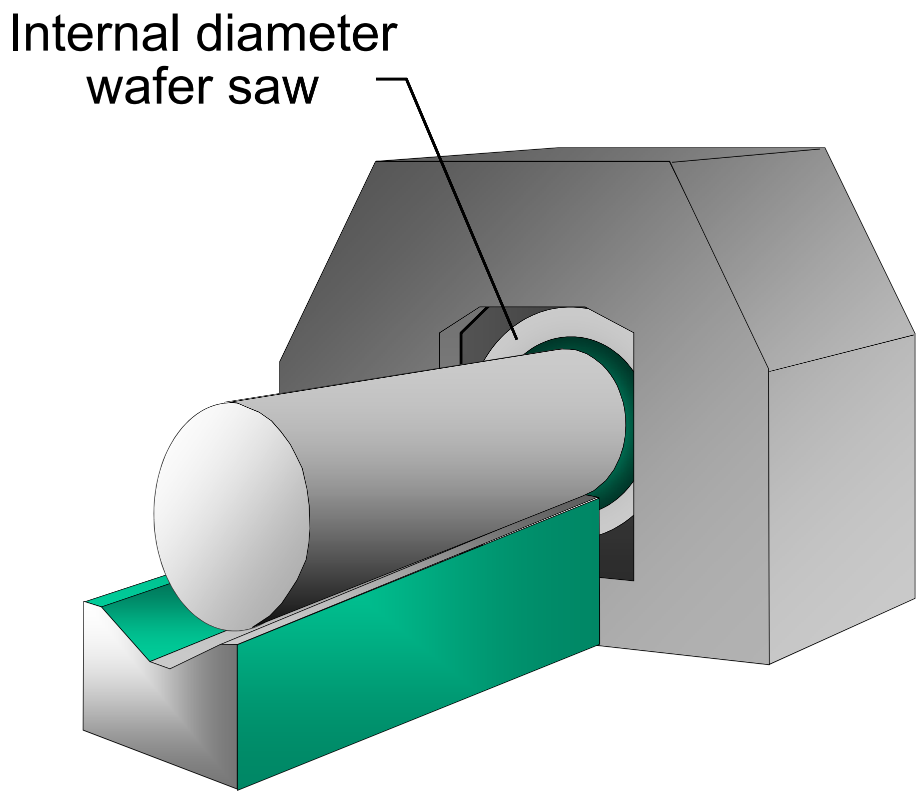


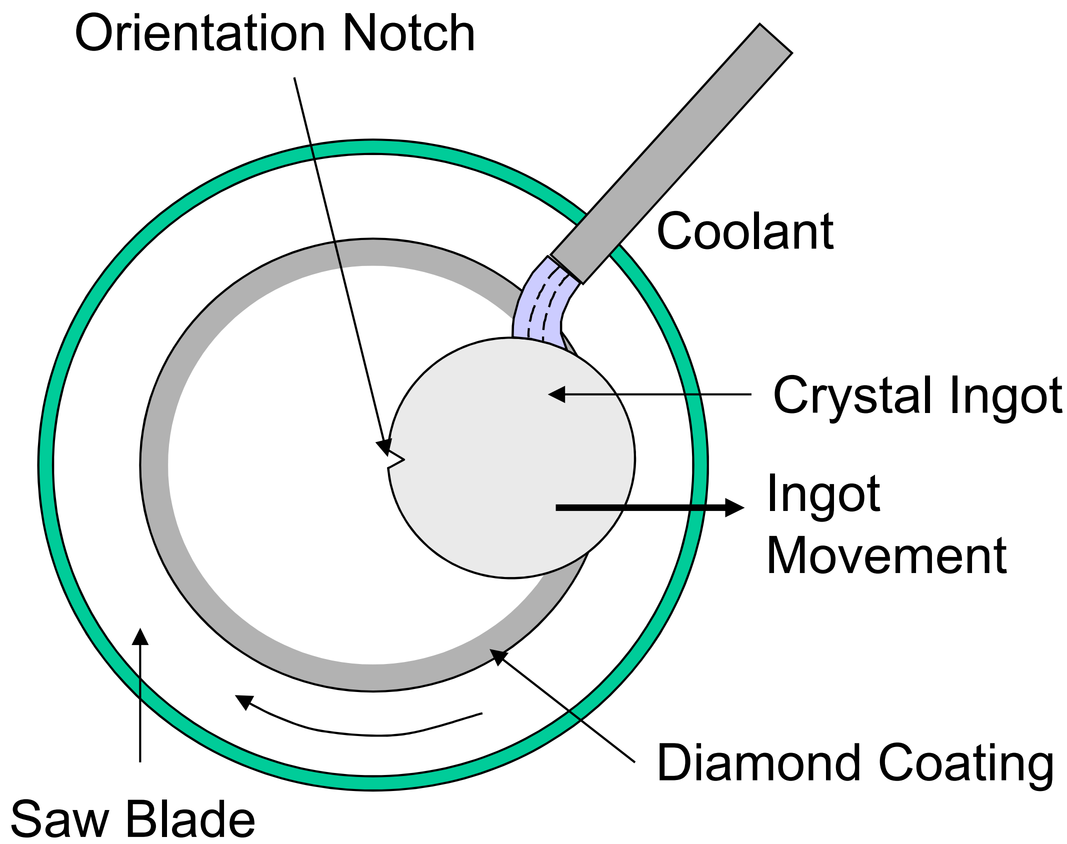
Notch, 200 mm and larger



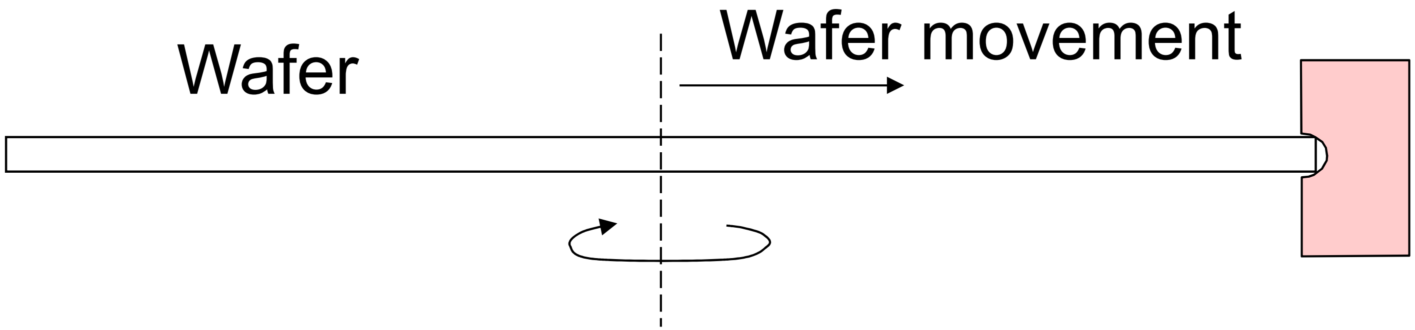
- Primary flat orients the wafer to the crystal structure.
- Secondary flat identifies the orientation and doping type of the wafer.

Wafer Sawing

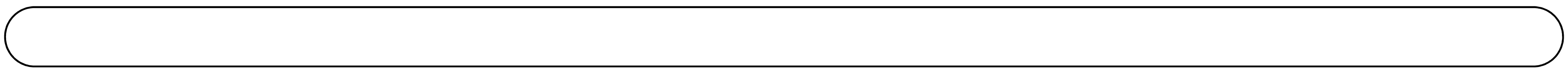




Wafer Edge Rounding



Wafer Before Edge Rounding

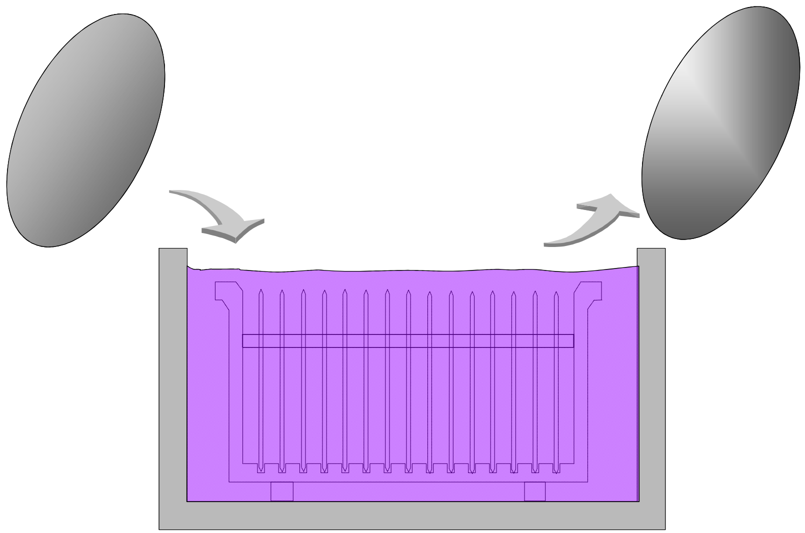


Wafer After Edge Rounding

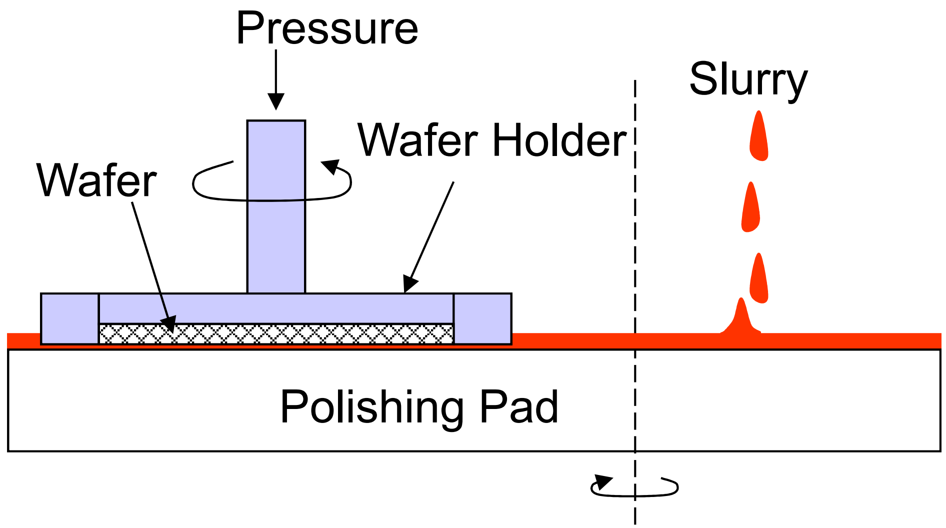
Wafer Lapping and Wet Etching

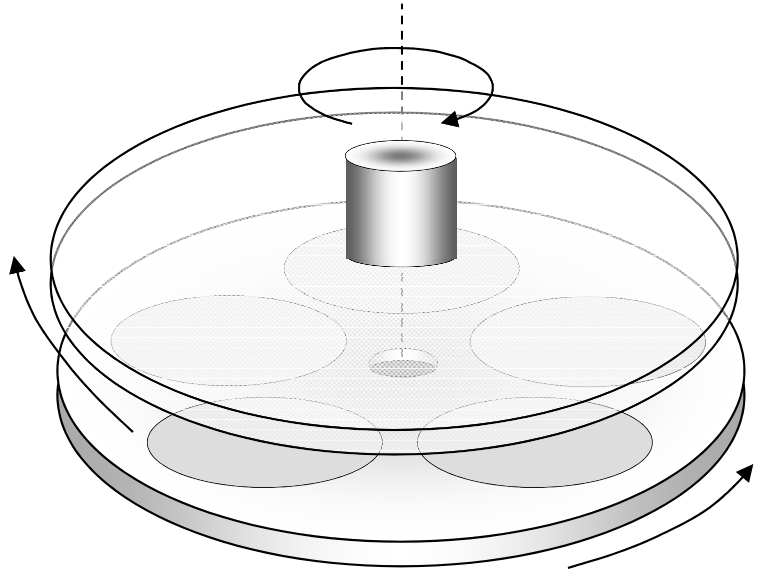
- Wafer lapping
  - Rough polished with conventional (abrasive) slurry-lapping.
  - To remove majority of surface damage and create a flat surface.

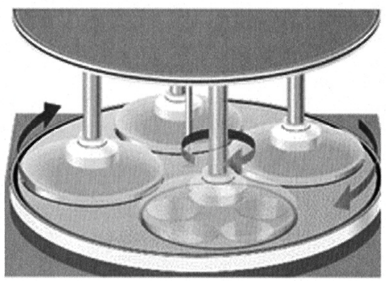
- Wet etching
  - Remove defects from wafer surface.
  - 4:1:3 mixture of HNO_3 (79 wt% in H_2O), HF (49 wt% in H_2O), and pure CH_3COOH.
  - $3\,Si + 4\,HNO_3 + 6\,HF$
    $\rightarrow 3\,H_2SiF_6 + 4\,NO + 8\,H_2O$

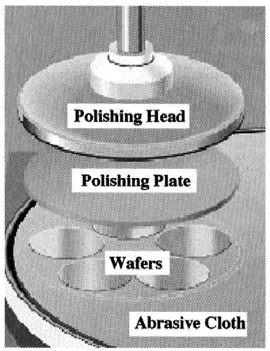


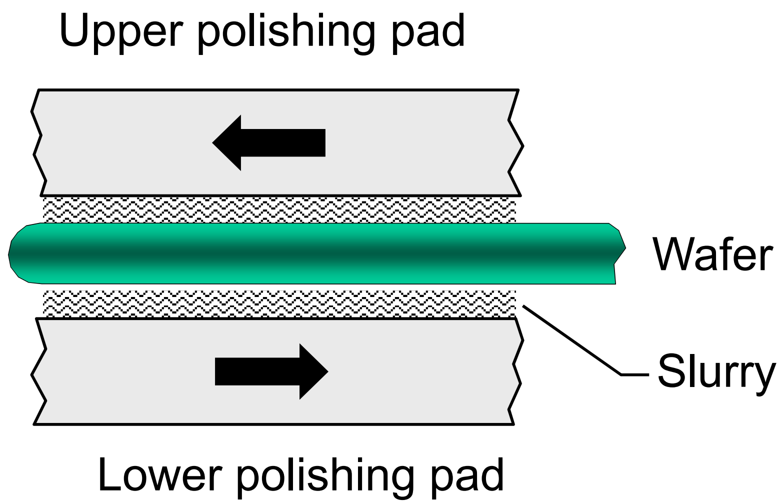
Chemical Mechanical Polishing



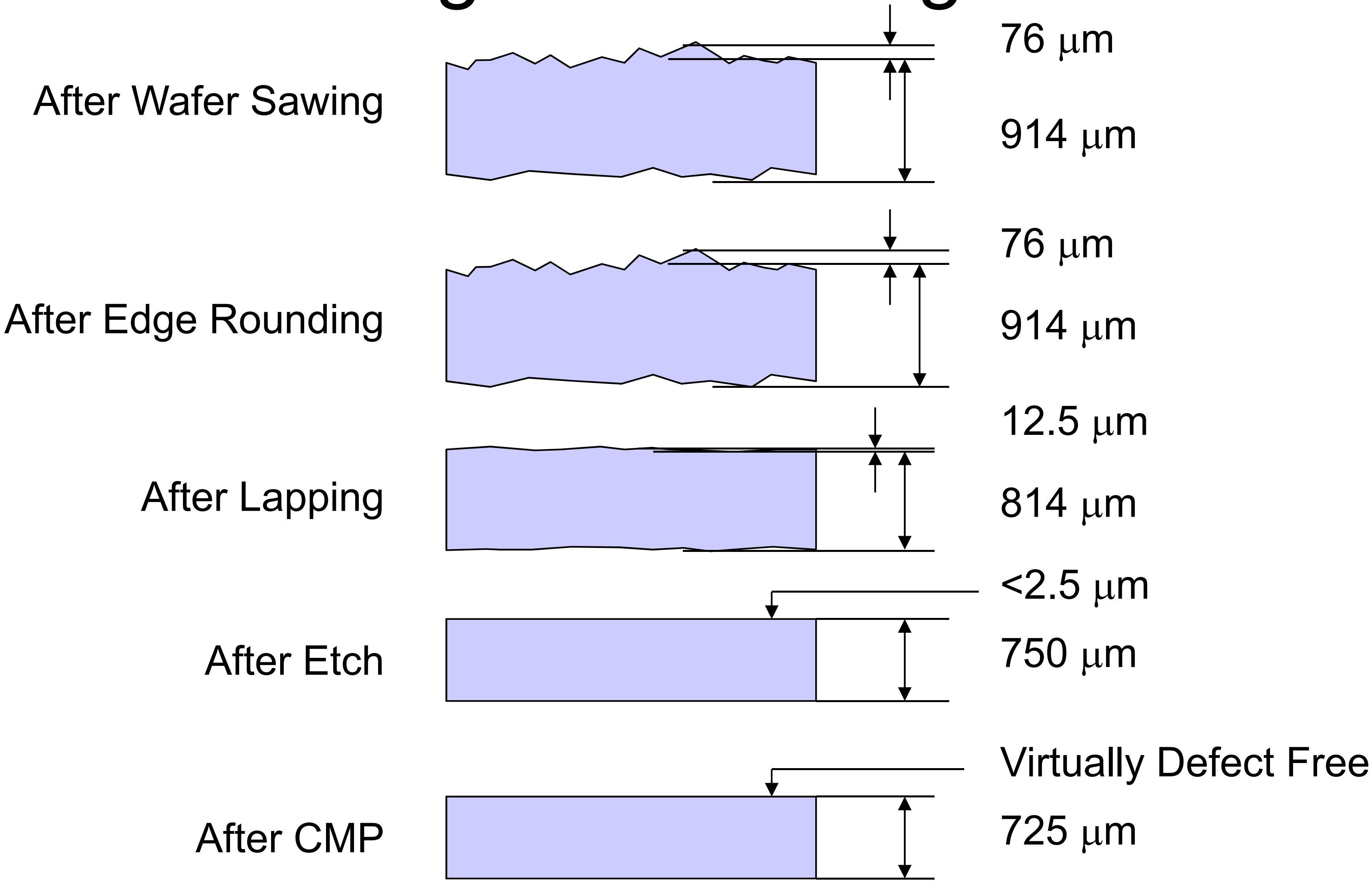






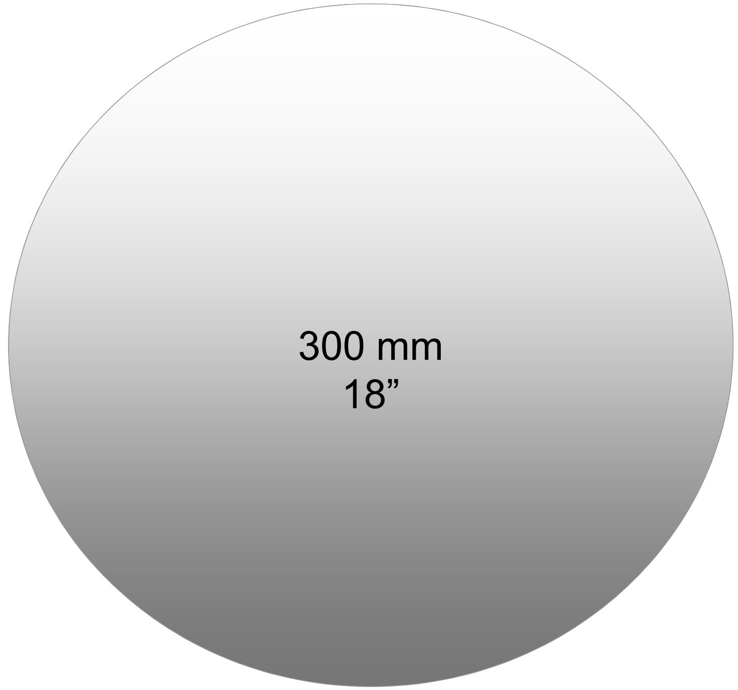


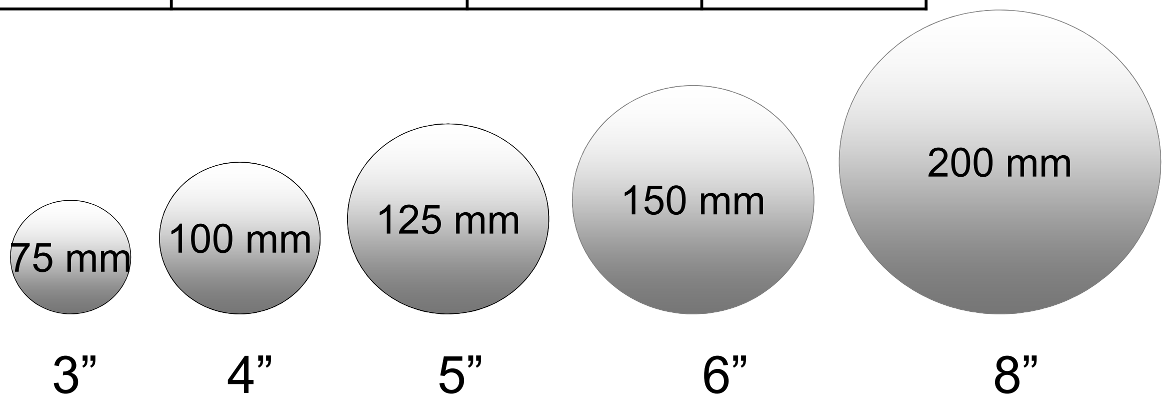
200 mm Wafer Thickness and Surface Roughness Changes

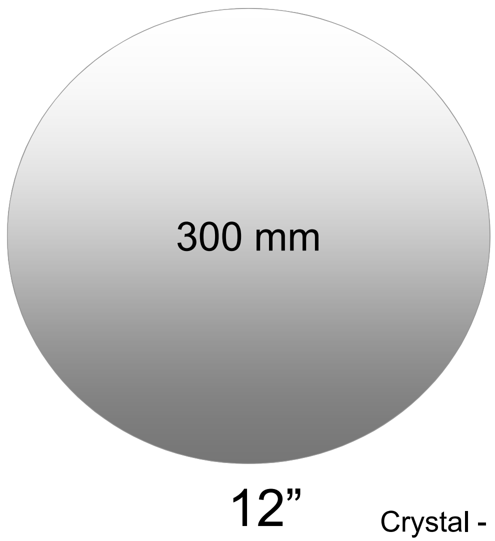


Parameters of Silicon Wafer

Wafer Size (mm)	Thickness (μm)	Area (mm^2)	Weight (g)
50.8 (2”)	279	20.26	1.32
76.2 (3”)	381	45.16	4.05
100 (4”)	525	78.65	9.67
125 (5”)	625	112.72	17.87
150 (6”)	675	176.72	27.82
200 (8”)	725	314.16	52.98
300 (12”)	775	706.21	127.62
450 (18”)	875	1588.79	324.16







Crystal Puller Evolution

100-150mm
30-40kg
'70's
14 ft.

Kayex

150 -200 mm
50-80kg
'80's
17 ft.

Leybolds

150 - 300 mm
100-150kg
'90s
21 ft.

Ferrofluidic/Kayex

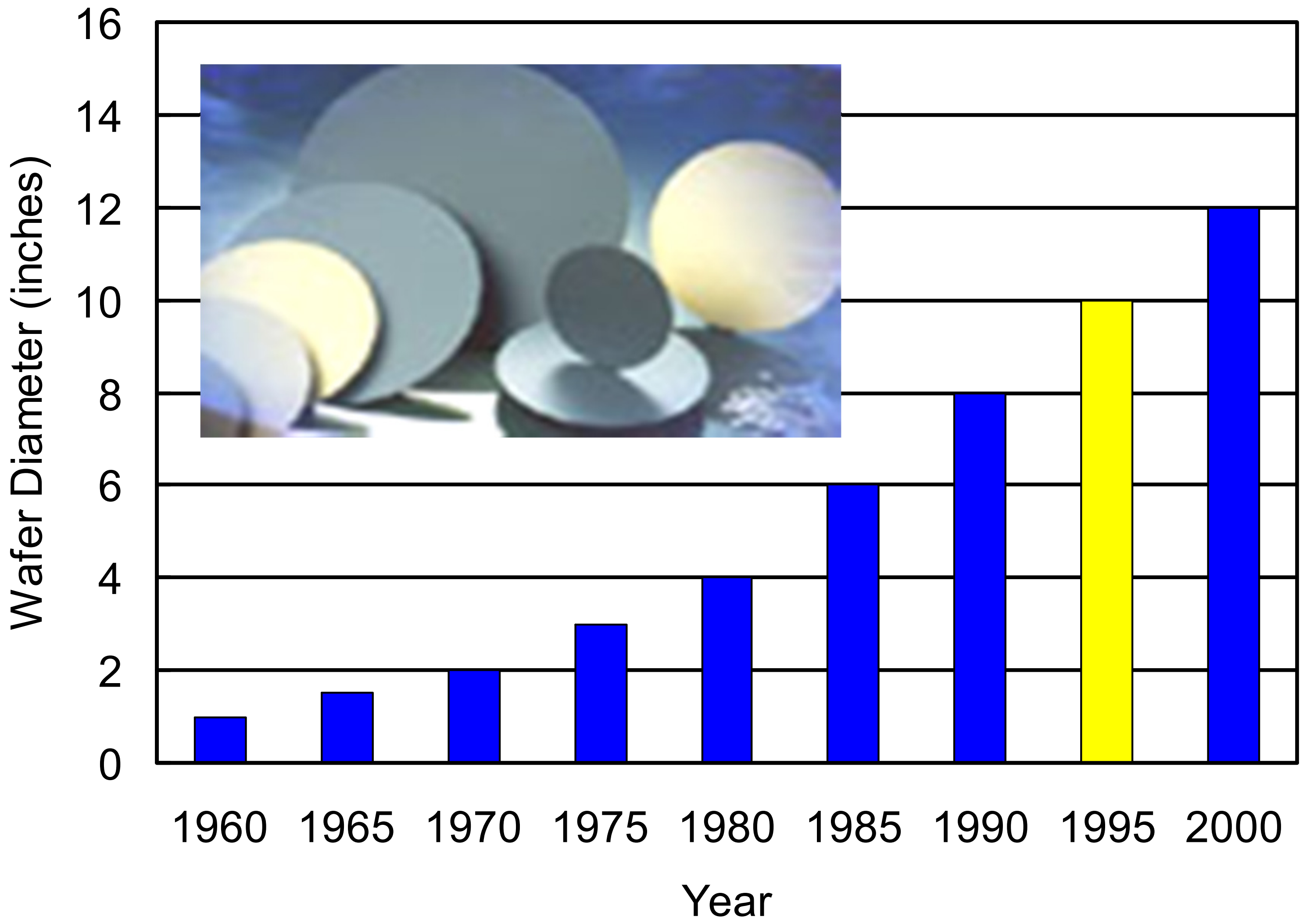
300 -400 mm
300kg
'97
25 ft.

Ferrofluidic/Kayex

300 - 450 mm
400kg
'98
30 ft.

Leybold puller : Courtesy of Super Silicon Institute (SSI)

Wafer Size Evolution



Dopant Segregation

- The doping concentration incorporated into the crystal is usually different from the doping concentration of the melt at the interface.
  - K_0 : equilibrium segregation coefficient
  - M_0 : initial weight of melt
  - M : weight of grown crystal
  - S : amount of dopant remaining in melt

$$k_0 \equiv \frac{C_s}{C_l}$$

$$-dS = C_s dM \qquad C_l = \frac{S}{M_o - M} \Rightarrow \frac{dS}{S} = -k_0\left(\frac{dM}{M_0 - M}\right)$$

$$\int_{C_0 M_0}^{S} \frac{dS}{S} = k_0 \int_0^M \frac{-dM}{M_0 - M} \Rightarrow C_s = k_0 C_0 \left(1 - \frac{M}{M_0}\right)^{K_0 - 1}$$

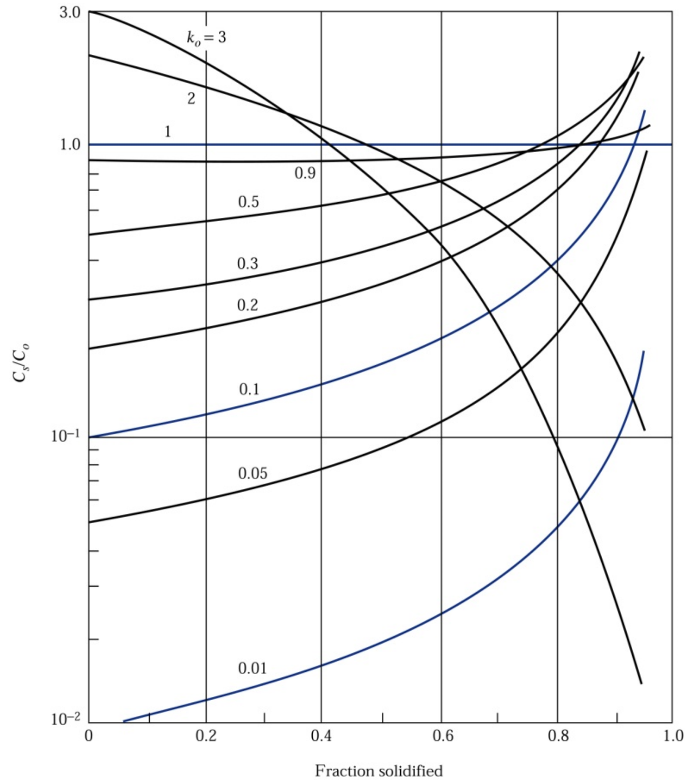


Table 3–2 Equilibrium segregation coefficients during CZ crystal growth for Si

Impurity	Segregation Coefficient
As	0.3
Bi	7×10^{-4}
C	0.07
Li	10^{-2}
O	0.5
P	0.35
Sb	0.023
Al	2.8×10^{-3}
Ga	8×10^{-3}
B	0.8
Au	2.5×10^{-5}

Effective Segregation Coefficient

- If the rejection rate is higher than the rate of which the dopant can be transported away by diffusion or stirring, then a concentration gradient will develop at the interface.

$k_0 = \frac{C_s}{C_l(0)} \Rightarrow$ Effective segregation coefficient : $k_e \equiv \frac{C_s}{C_l}$

Diffusion eq. $0 = v\frac{dC}{dx} + D\frac{d^2C}{dx^2}$ ⇨ $C = A_1 e^{-vx/D} + A_2$

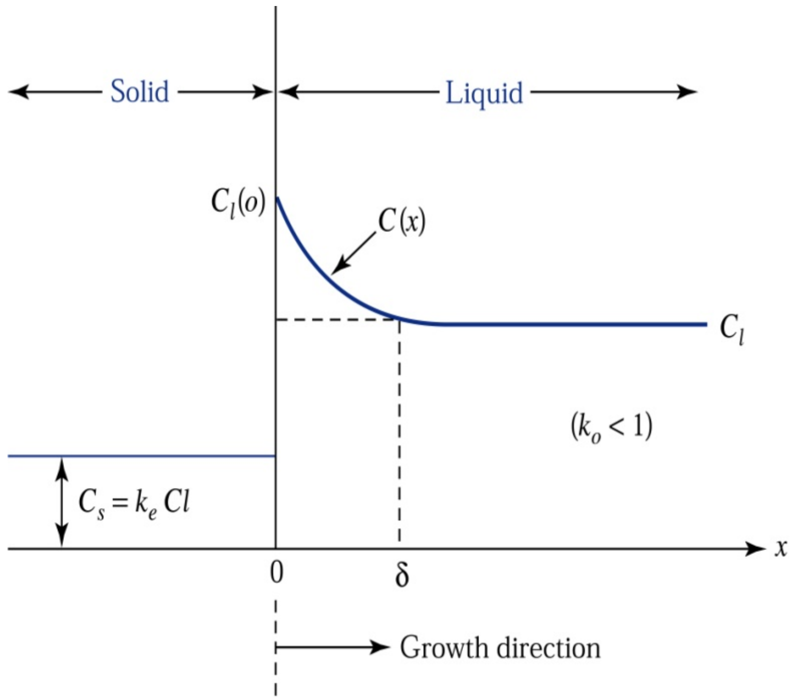
Boundary conditions :

$C = C_l(0)$ at $x = 0$ & $C = C_l$ at $x = \delta$

Dopant conservation : $D\left(\frac{dC}{dx}\right)_{x=0} + \left[C_l(0) - C_s\right]v = 0$

⇨ $e^{-v\delta/D} = \frac{C_l - C_s}{C_l(0) - C_s}$

$K_e \equiv \frac{C_s}{C_l} = \frac{K_0}{K_0 + (1 - K_0)e^{-v\delta/D}} > \mathrm{k}_0$ as $v\delta >> D \Rightarrow K_e \to 1$

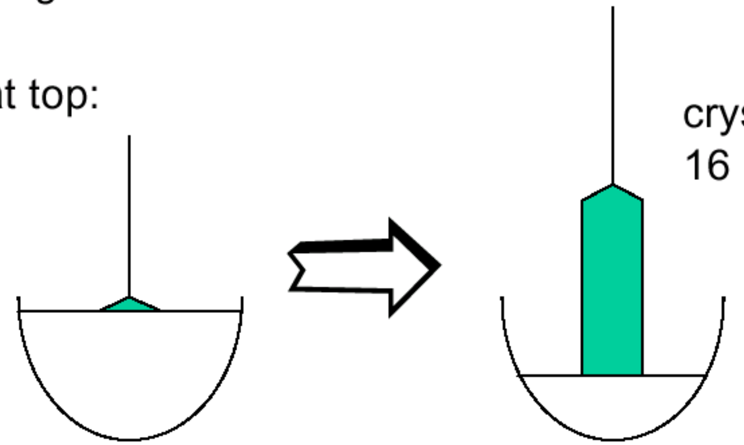


Dopant Incorporation

Example of a segregation coefficient of 0.8:

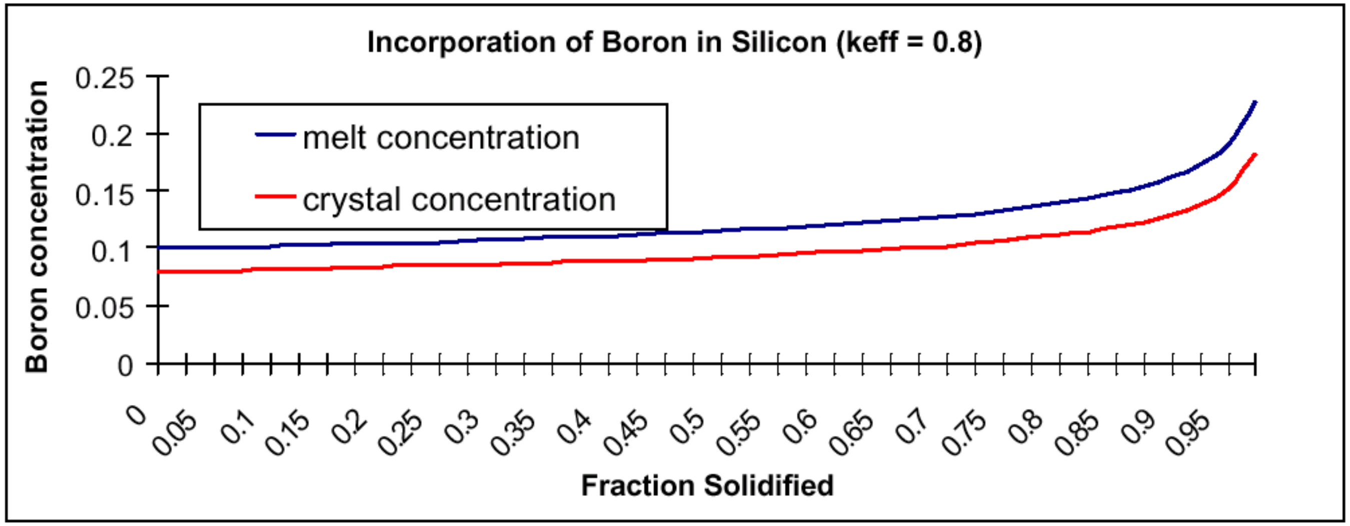
initial crystal concentration at top:
8 mg boron / kg silicon

initial melt concentration:
10 mg boron / kg silicon



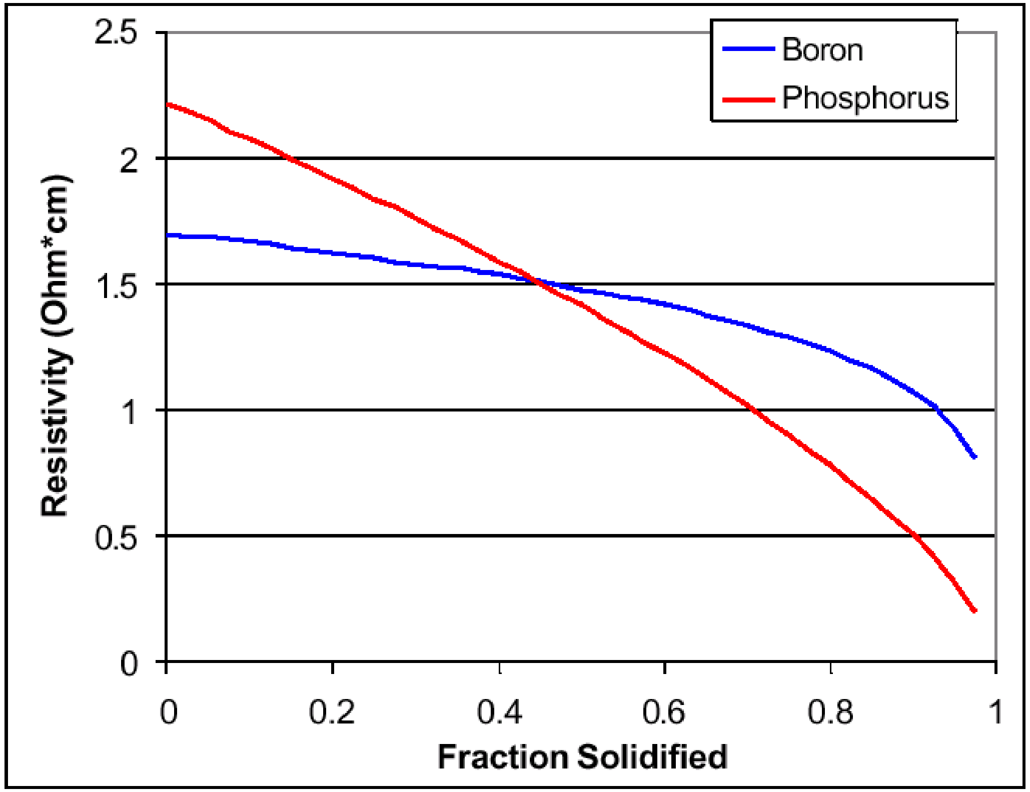
crystal concentration in body:
16 mg boron / kg silicon

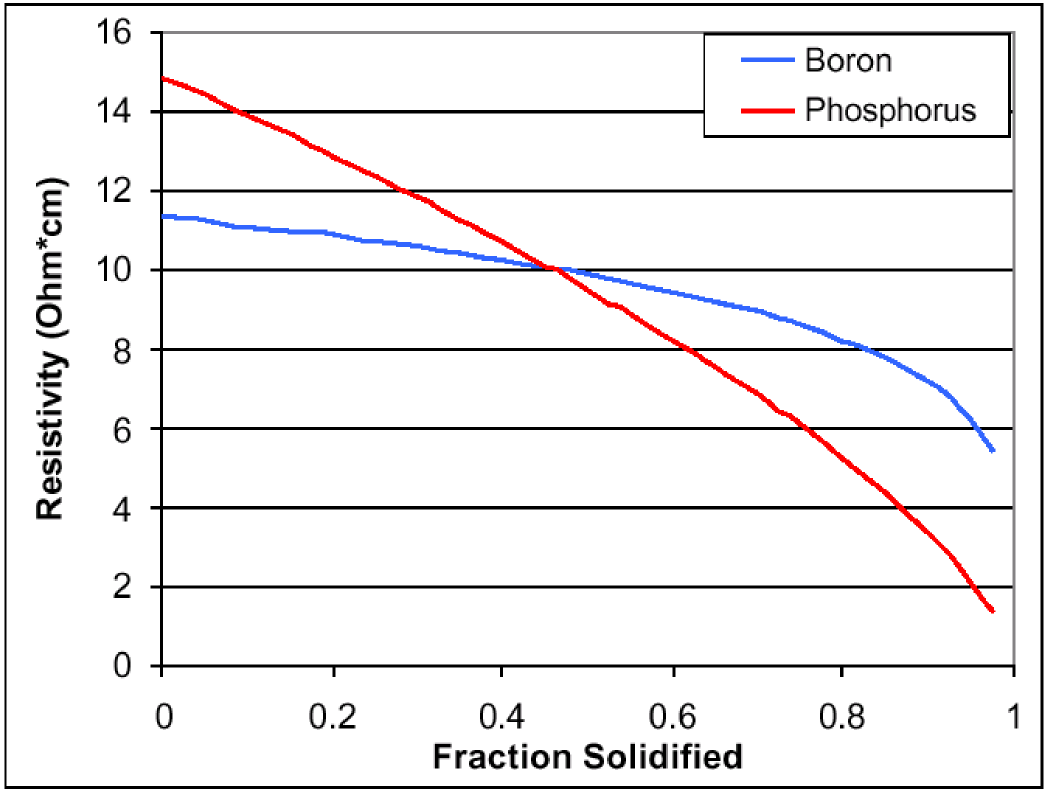
melt concentration:
20 mg boron / kg silicon



$$C_s = k_e C_0 \left(1 - \frac{M}{M_0}\right)^{K_e - 1}$$

Dopant Incorporation



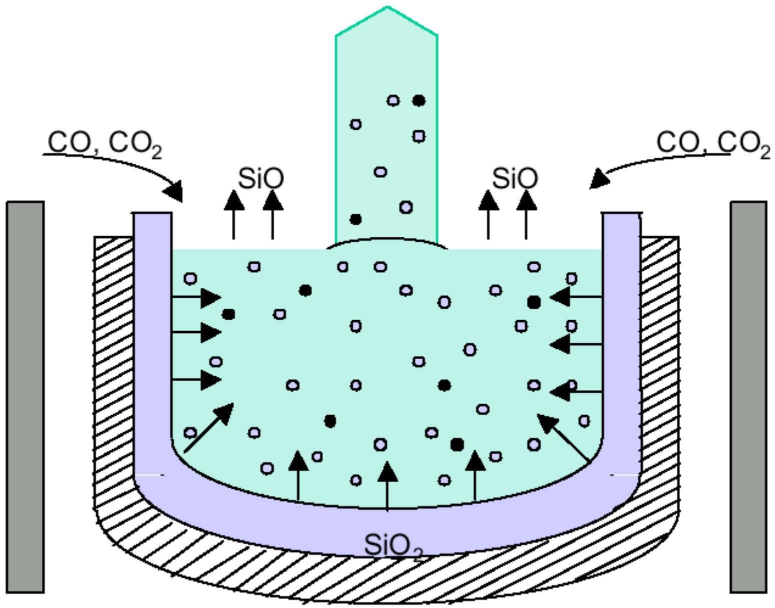


Target 1.5 Ωcm

Target 10 Ωcm

Carbon & Oxygen Sources

- Oxygen source: quartz (SiO_2) crucible dissolution.
- >98% of oxygen dissolved evaporates as SiO.
- Remainder is incorporated into the silicon crystal.
- Carbon source: graphite parts.
- Carbon concentrations normally ~ FTIR detection limit.
- Abnormal concentration is indicative of heater arcing or puller leak.

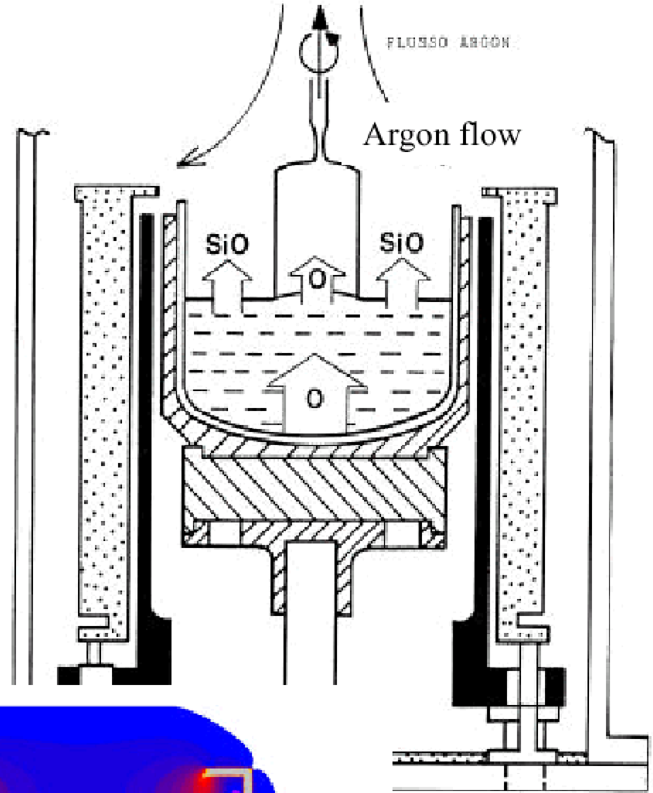


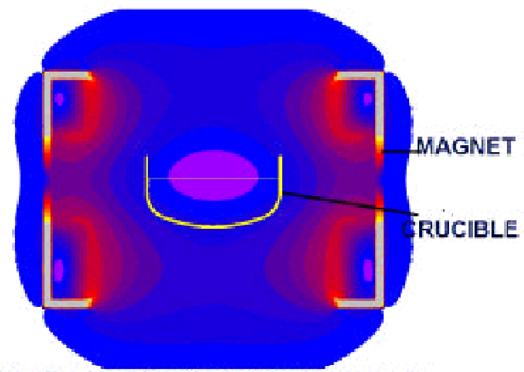
Oxygen Control

- Oxygen control is obtained by varying the following parameters:

	High Oi	Low Oi
Charge mass	Larger	Smaller
Crucible rotation	Faster	Slower
Magnetic field	Lower	Higher

- The magnetic field can be applied vertically or horizontally. It lowers oxygen level, dampening the melt flow.
- In modern MCZ crystal pullers, the applied magnetic field can be several thousand Gauss.



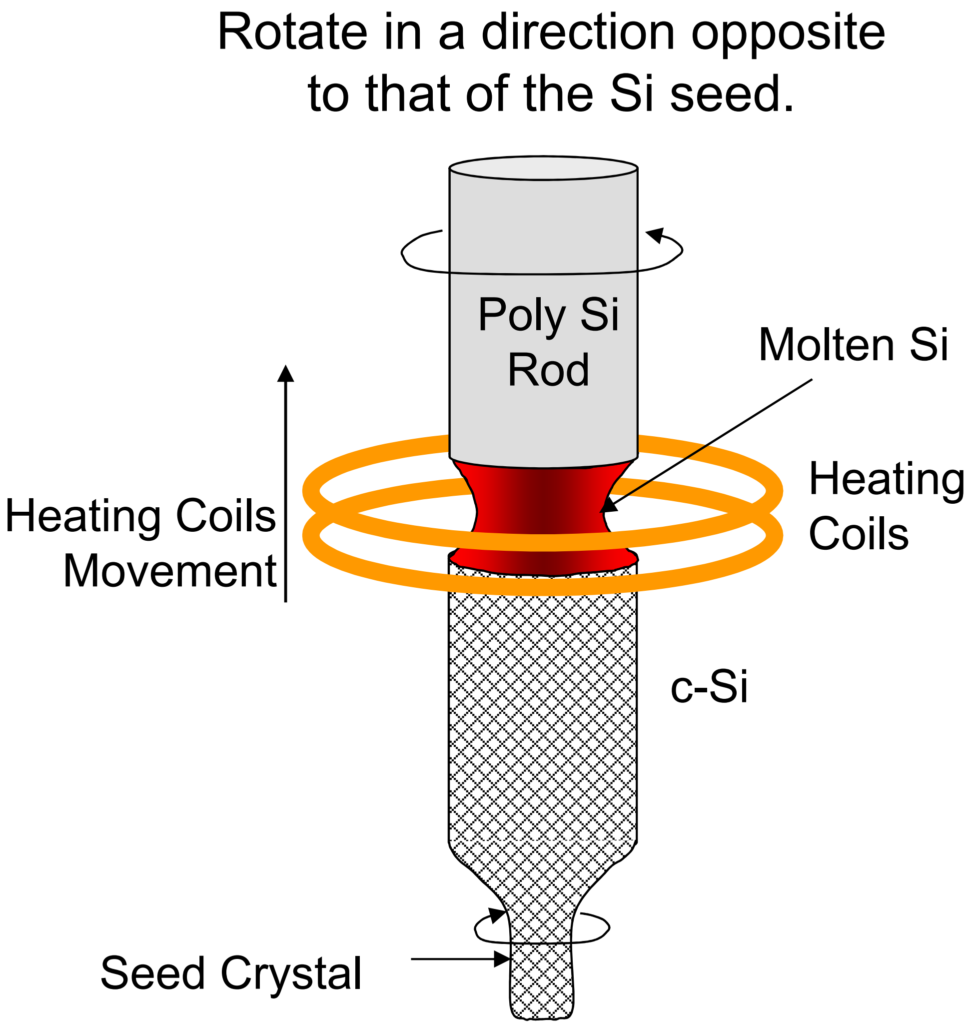


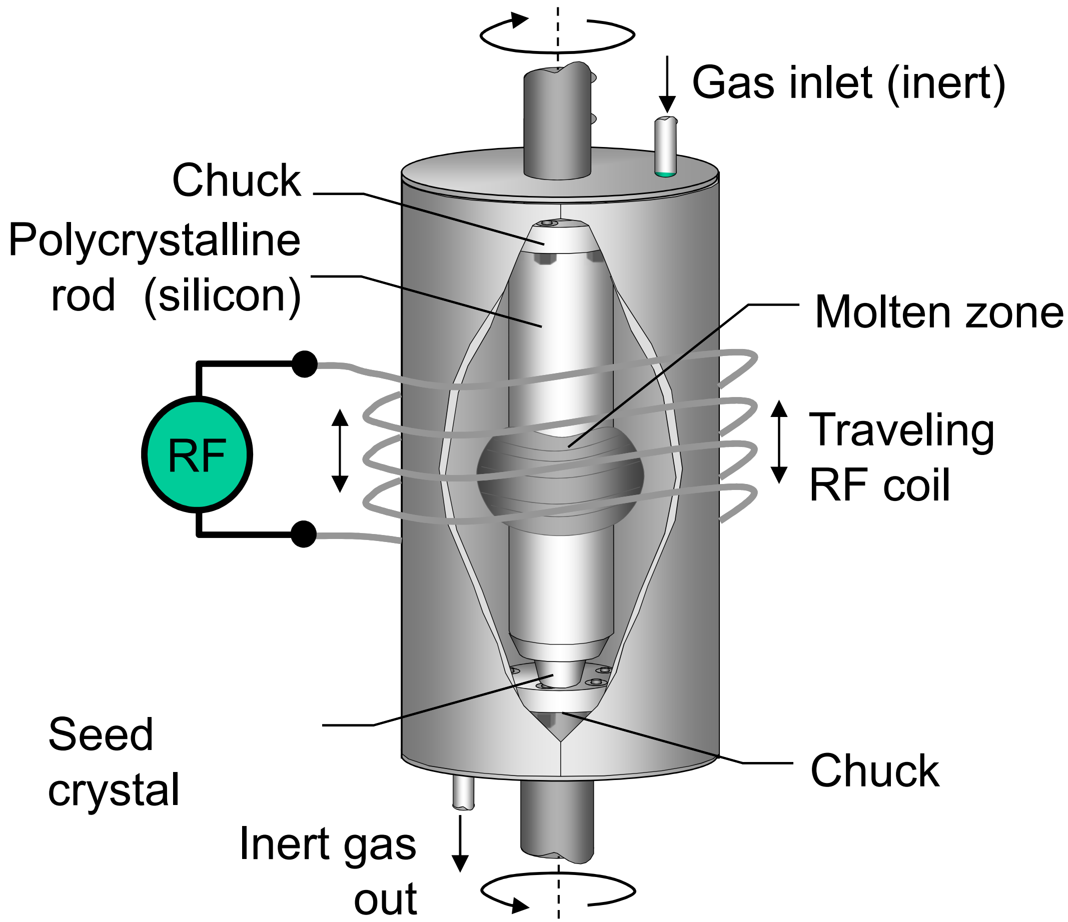
CONTOUR PLOT OF MAGNETIC FIELD

Floating Zone (FZ) Crystal Pulling

- A rod of EGS polycrystalline Si is clamped at both ends, with the bottom in contact with a single-crystal seed.
- An RF coil heats and melts the EGS rod. The melting starts at the seed end and then the coil (or the rod) is slowly moving to grow single crystal rod.
- No crucible is used. Impurity contamination is significantly suppressed.
- Seed determines the orientation of the grown crystal.
- Because of stability problems associated with the liquid zone on a gravity environment, it is not easy to grow crystal with a large diameter.

Floating Zone Method





Dopant Incorporation in FZ Crystal

- Since usually k_o <1, impurity doping in the crystal much less than that in ESG, the reason why also called zone refining.
- High purity, high resistivity crystal silicon can be achieved.
- Several intentional doping methods have been developed, following are two of them:
  - Carry out FZ process in a gas ambient that contains the dopant species (e.g, diluted B_2H_6 or PH_3)
  - Neutral transmutation doping (NTD): place the FZ ingot inside a nuclear reactor and expose it with thermal neutrons to transform the ^{30}Si isotope (~3% in the crystal) into ^{31}P.

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Dopant Incorporation in FZ Crystal

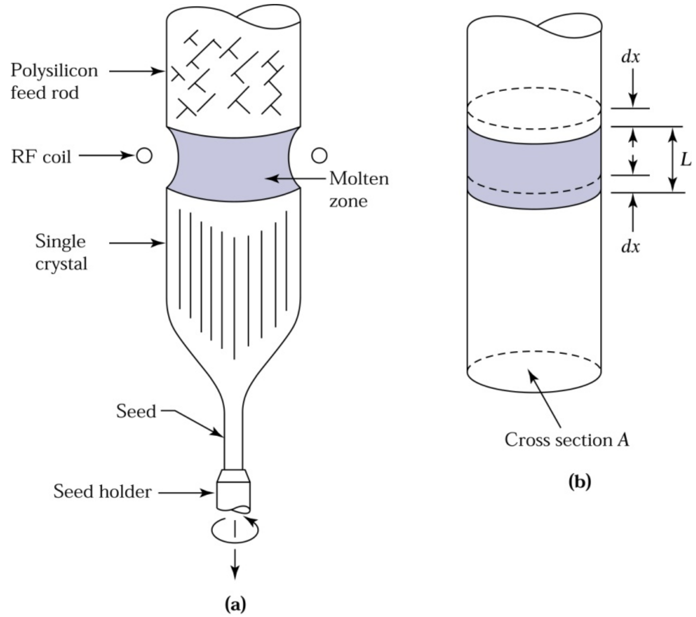
S is the amount of dopant in the molten zone (in weight)

ρ_d is the specific density of Si (in weight/volume)

C_o is the uniform doping concentration in the rod (in weight)

S_o is the amount of dopant in the zone at the front end of the rod

C_s is the doping concentration in the crystal at the retreating end



$$dS = C_0\rho_d A dx - \frac{k_e S}{L}dx = \left(C_0\rho_d A - \frac{k_e S}{L}\right)dx$$

$$\int_0^x dx = \int_{S_0}^{S} \frac{dS}{C_0\rho_d A - (k_e S/L)} \text{ where } S_0 = C_0\rho_d AL$$

$$\Rightarrow \quad \exp\left(\frac{k_e x}{L}\right) = \frac{C_0\rho_d A - (k_e S_0/L)}{C_0\rho_d A - (k_e S/L)}$$

or

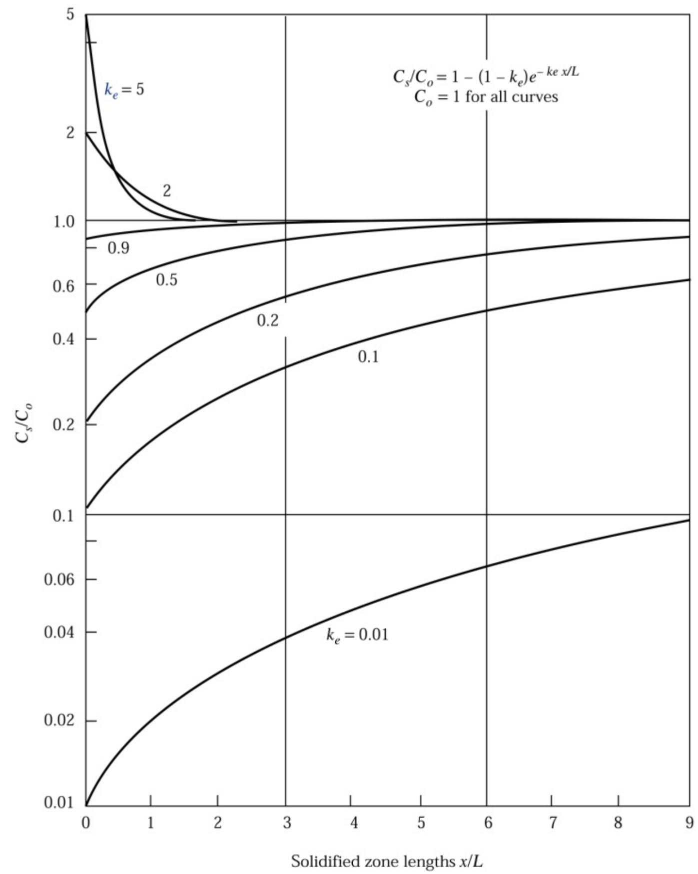
$$S = \frac{C_0\rho_d AL}{k_e}\left[1-(1-k_e)^{-k_e x/L}\right]$$

$$\Rightarrow \quad C_s = k_e(S/A\rho_d L) = C_0\left[1-(1-k_e)^{-k_e x/L}\right]$$

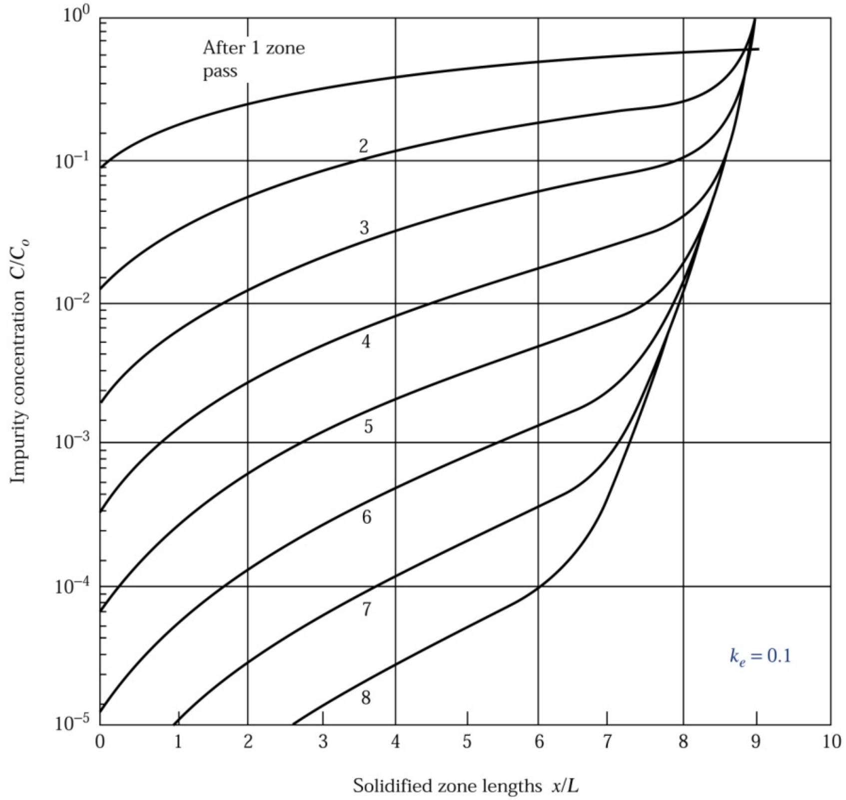
If all the dopants are introduced in the first zone $(S_o = C_1\rho_d AL)$ and C_o is negligible small $\Rightarrow S_o = Se^{k_e x/L}$

$C_s = K_e\dfrac{S}{A\rho_d L} \Rightarrow C_s = k_e C_1 e^{-k_e x/L}$ is almost constant as $k_e x/L$ is small.

Dopant Incorporation in FZ Crystal



Curves for the float-zone process showing doping concentration in the solid as a function of solidified zone lengths.

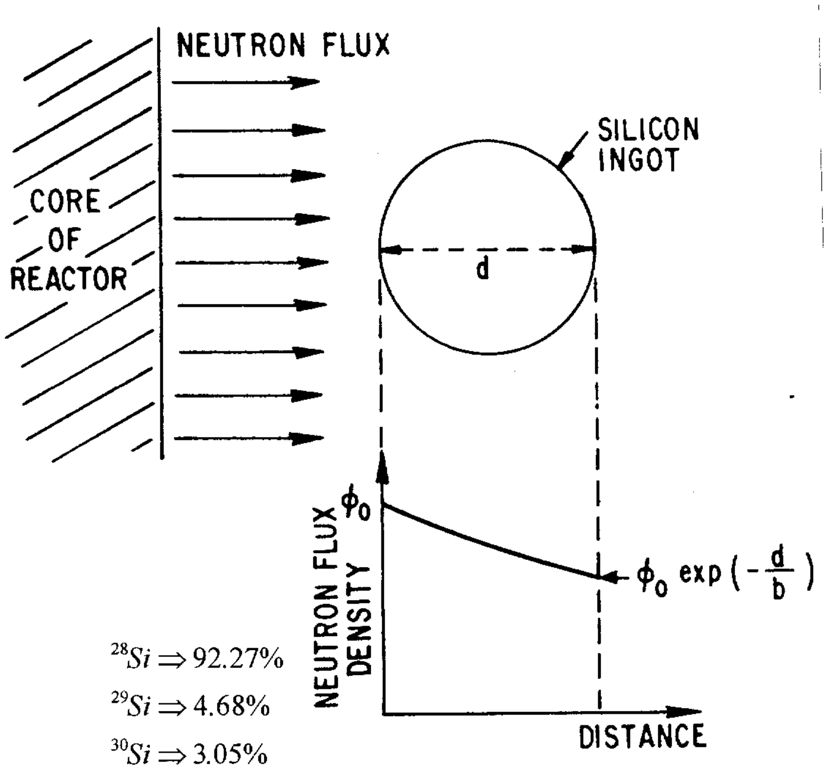


Relative impurity concentration versus zone length for a number of passes. L denotes the zone length.

Neutral Transmutation Doping (NTD)

$$Si_{14}^{30} + neutron \rightarrow Si_{14}^{31} + \gamma\text{ - ray} \xrightarrow{2.62\text{hr}} P_{15}^{31} + \beta\text{ - ray}$$

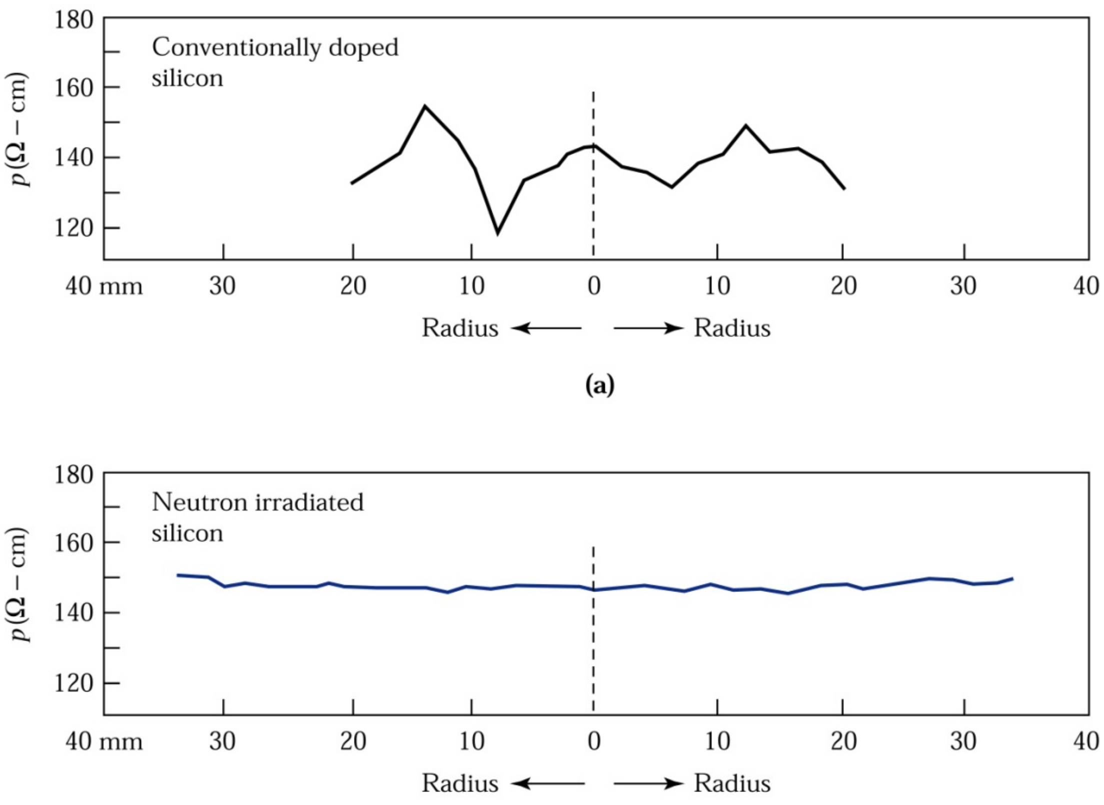
Penetration depth ~ 100 cm



$^{28}Si \Rightarrow 92.27\%$

$^{29}Si \Rightarrow 4.68\%$

$^{30}Si \Rightarrow 3.05\%$



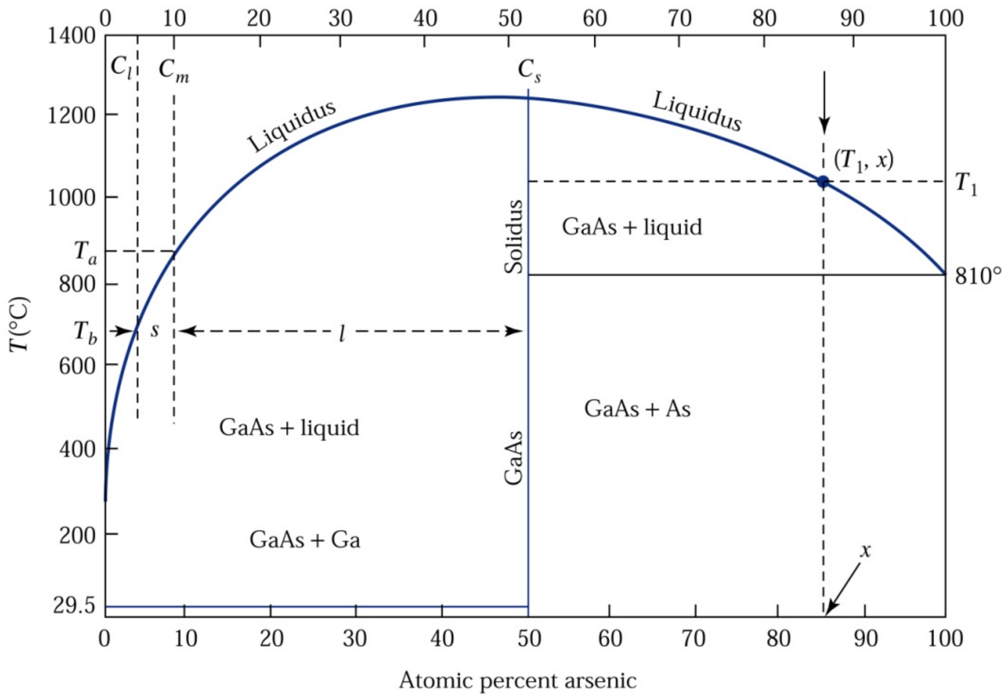
(a)

(b)

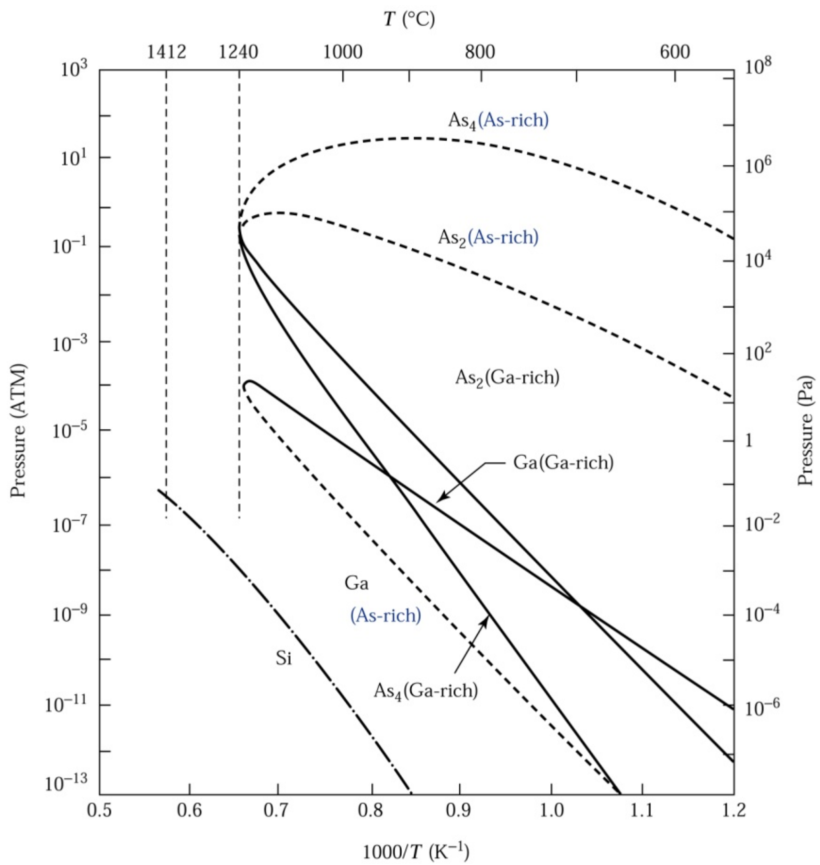
CZ versus FZ

- CZ method is more popular
  - Lower cost.
  - Larger wafer size (300 mm in production, 450 mm is ready).
  - Reusable materials.
  - O and C contamination issues need to be addressed.
  - Gettering or epi wafers is feasible.
- FZ method
  - Pure silicon crystal (no crucible).
  - More expensive, smaller wafer size (150 mm or less).
  - For specific applications (ex. power devices).

GaAs Phase Diagram



Phase diagram for the gallium-arsenic system.



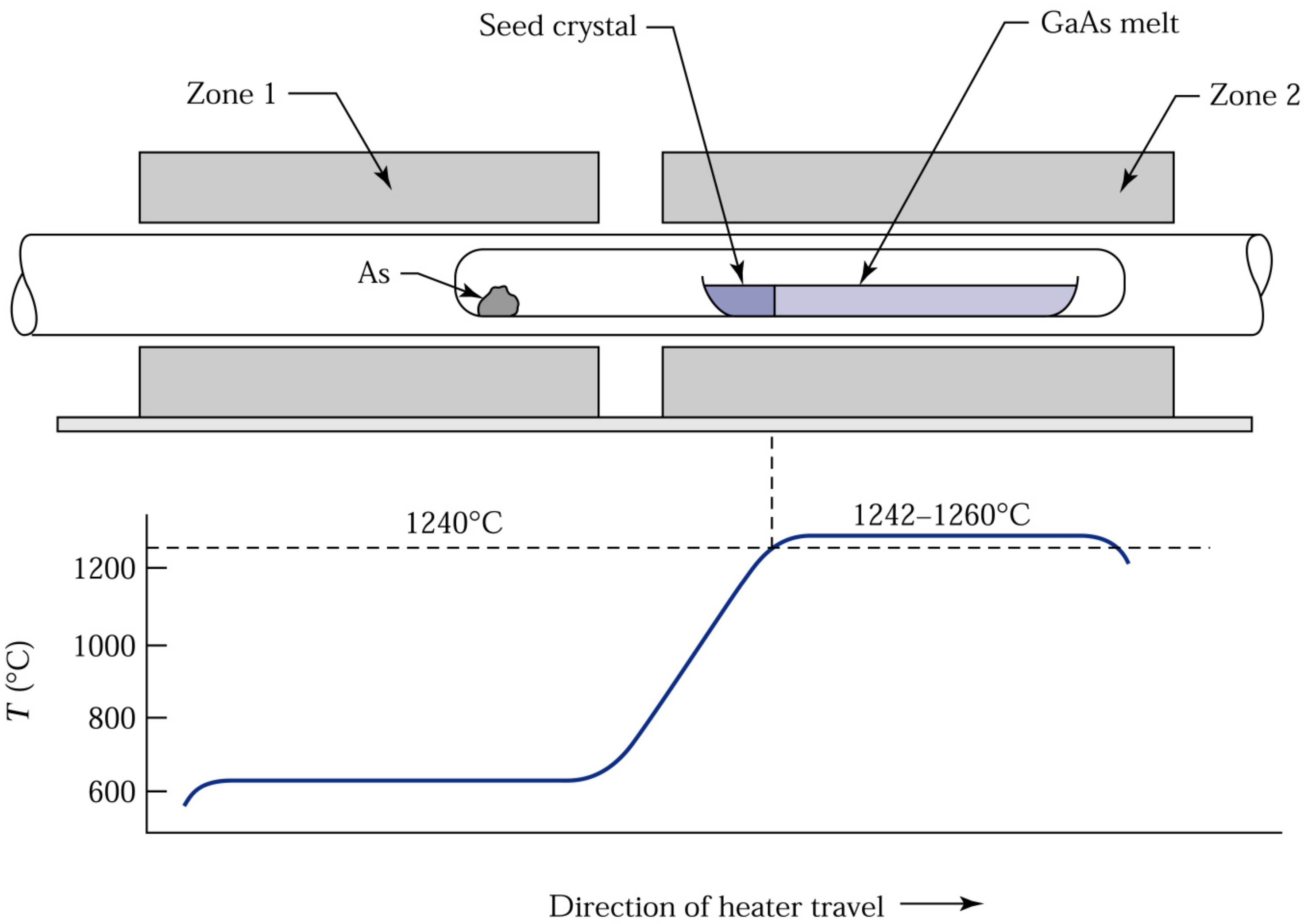
Partial pressure of gallium and arsenic over gallium arsenide as a function of temperature. Also shown is the partial pressure of silicon.

Czochralski Technique for GaAs

- Similar design to the Si puller.
- Liquid Encapsulation technique is developed.
  - A cap layer of an inert liquid is used to cover the GaAs melt.
  - Liquid B_2O_3 of 0.5-1 cm thick is commonly used.
  - B_2O_3 can dissolve SiO_2, the quartz crucible is replaced by a graphite crucible.

Dopant	Type	E_c offset (eV)	E_v offset (eV)	K_0
Be	P		0.028	3
Mg	P		0.028	0.1
Zn	P		0.031	0.4
C	n/p	0.0060	0.026	0.8
Si	n/p	0.0058	0.035	0.185
Ge	n/p	0.0061	0.040	0.0028
S	N	0.0061		0.5
Se	N	0.0059		0.5
Sn	N	0.0060		0.052
Te	N	0.0058		0068

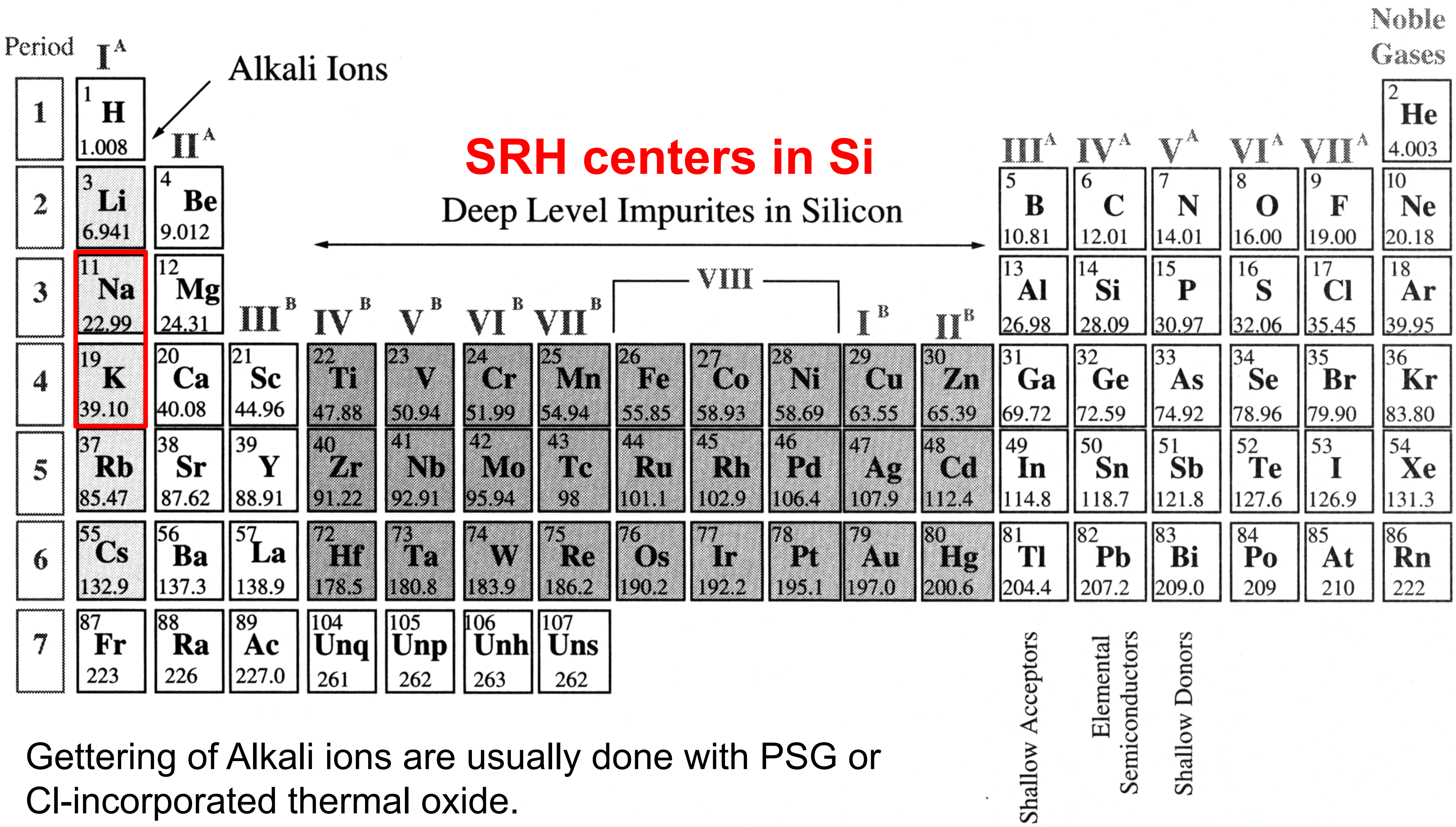
Bridgman Technique for GaAs



Gettering Technique

- It is very difficult to reduce undesirable elements such as metals (Fe, Cu, Au, etc.) and alkali ions (Na^+, K^+, etc.) in Si to levels where they have no effect on device performance.
- Fe, Cu, and Au are minority carrier lifetime killer in Si.
- Na^+ and K^+ are mobile ions in the oxide and cause instability of threshold voltage in MOSFETs.
- Gettering is a means of collecting these unwanted elements in regions of the chip where they do minimal harm.
- Methods for gettering of alkali ions:
  - PSG (phosphoslicate glass) capping.
  - Incorporation of Cl in the gate oxide.
  - Surface nitride passivation.

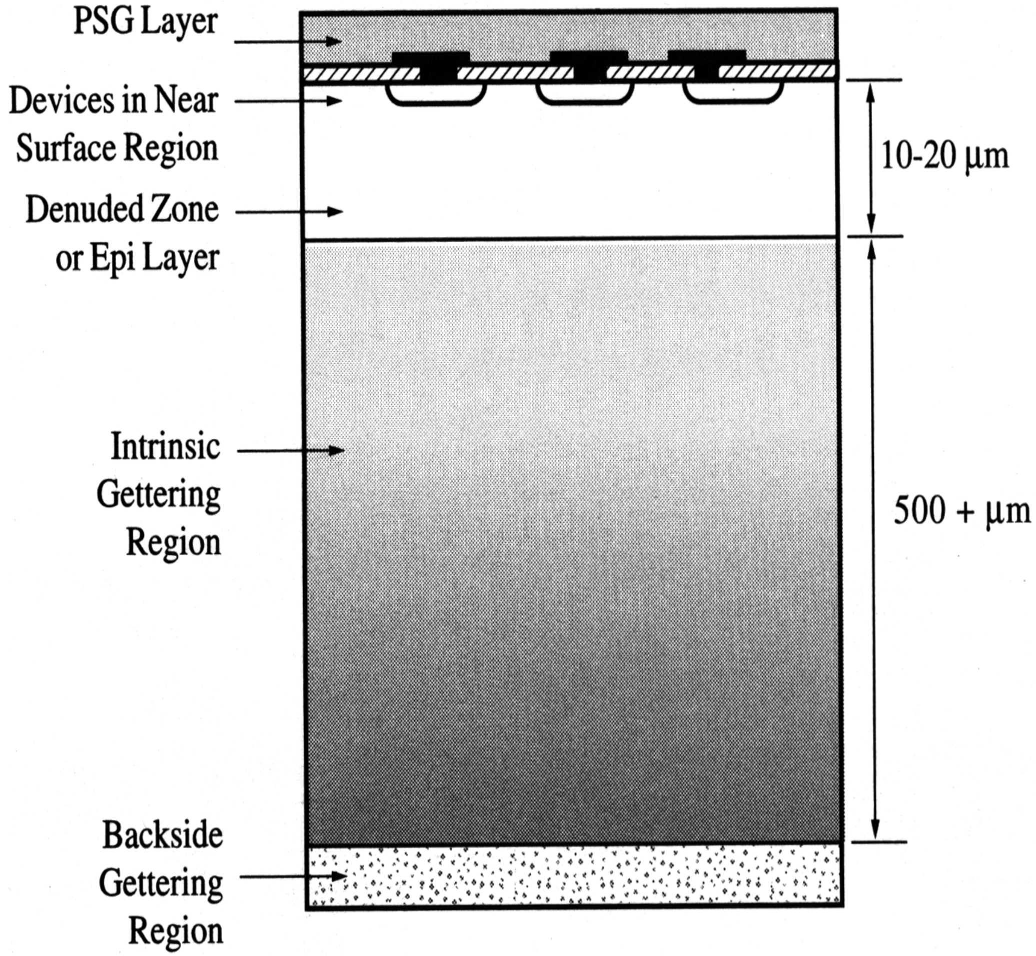
The Most Concerned Elements



Gettering of Alkali ions are usually done with PSG or Cl-incorporated thermal oxide.

Strategies for Gettering of Metals

- Intrinsic gettering
  - Formation of oxygen precipitates as the gettering centers in the bulk Si.
- Extrinsic gettering
  - Creation of gettering sites (defects) at backside of the wafer.
    - ion implantation
    - heavily phosphorus doping
    - a-Si or poly-Si deposition
    - laser melting, etc.



Intrinsic Gettering

Oxygen concentration > oxygen solubility in Si

oxygen precipitation

$2Si + 2O_i \text{ ----> } SiO_2 + Si_i$ $\quad$ Si_i silicon self interstitial

Precipitation can be divided into two steps:

1. nucleation small nuclei of condensed phase SiOx.
2. growth growth of nuclei to a larger size with a substantial decrease in O_i.

*F. S. Ham J. Phys. Chem. Solids 6, 335 (1958)

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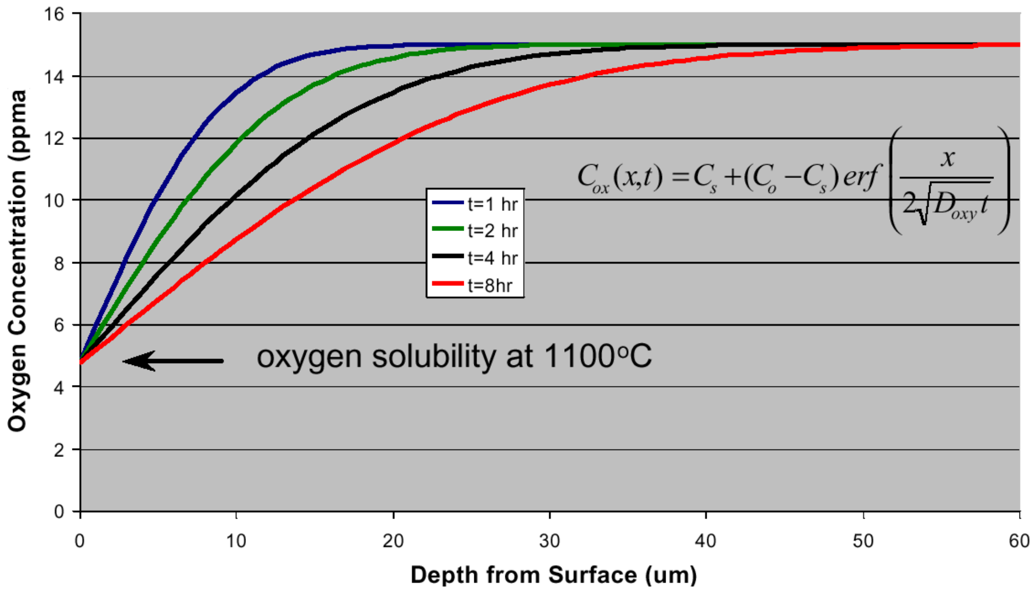
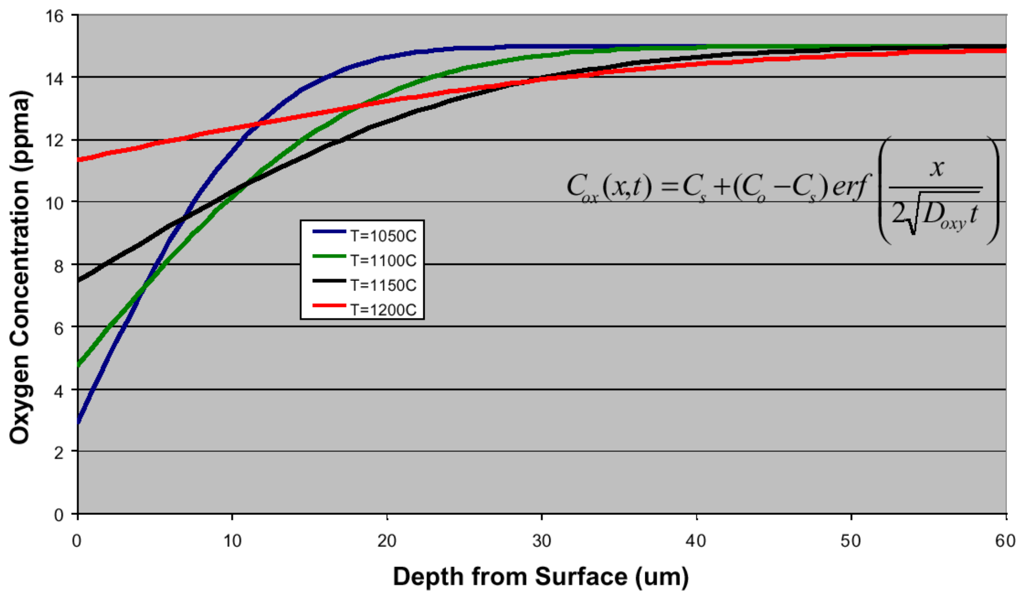
Intrinsic Gettering

Oxygen Outdiffusion Profiles
T=1100°C; Initial (O_i)=15.0ppma



Oxygen Outdiffusion Profiles
t=4 hours, Initial (O_i)=15ppma

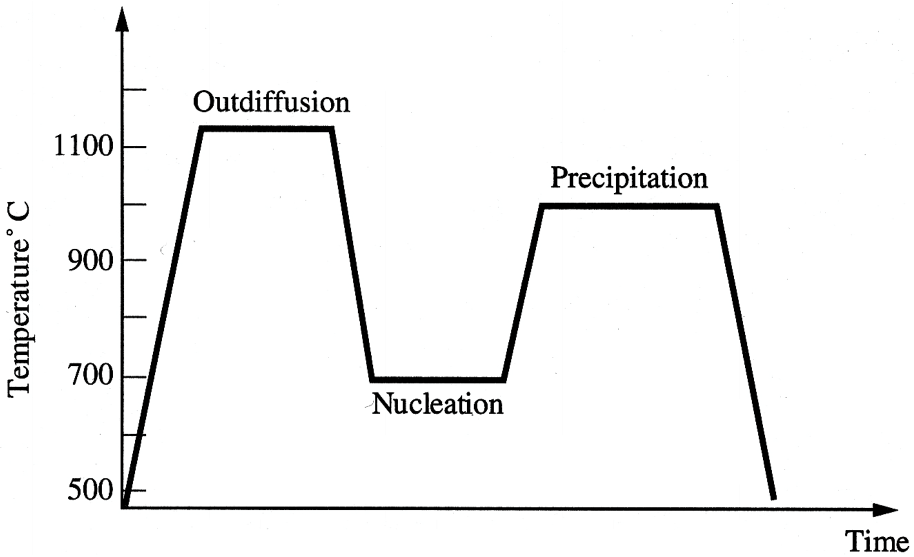


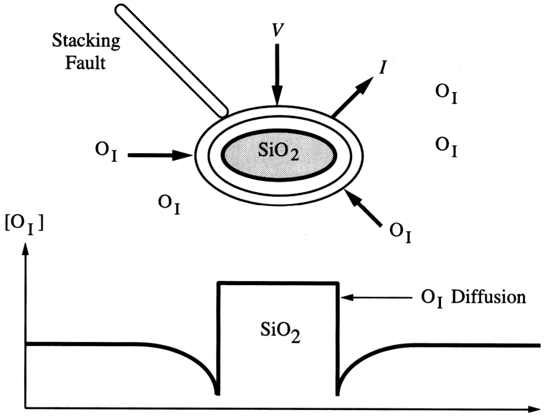
Intrinsic Gettering

Oxygen Out-diffusion (1)
- **High temperature**
- **Long times**

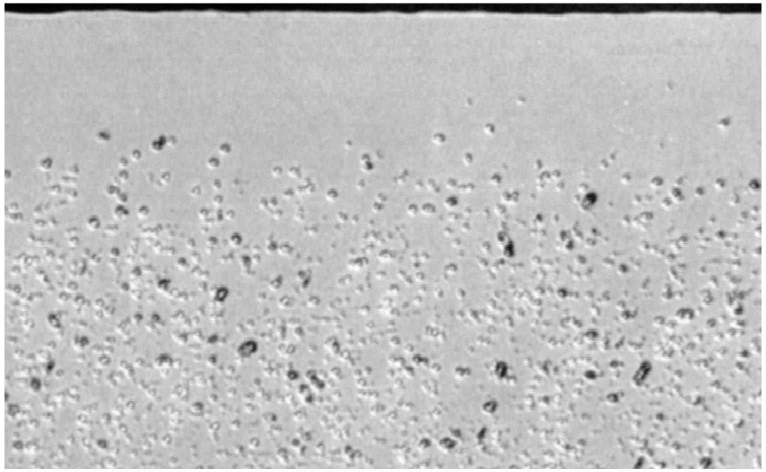
Oxygen Nucleation (2)
- **Low temperatures**
- **Long times**

Precipitate Growth (3)
- **Dependent on IC process**
- **Wafer-by-wafer variation due to:**
  - **Oxygen concentration**
  - **Thermal history of crystal**

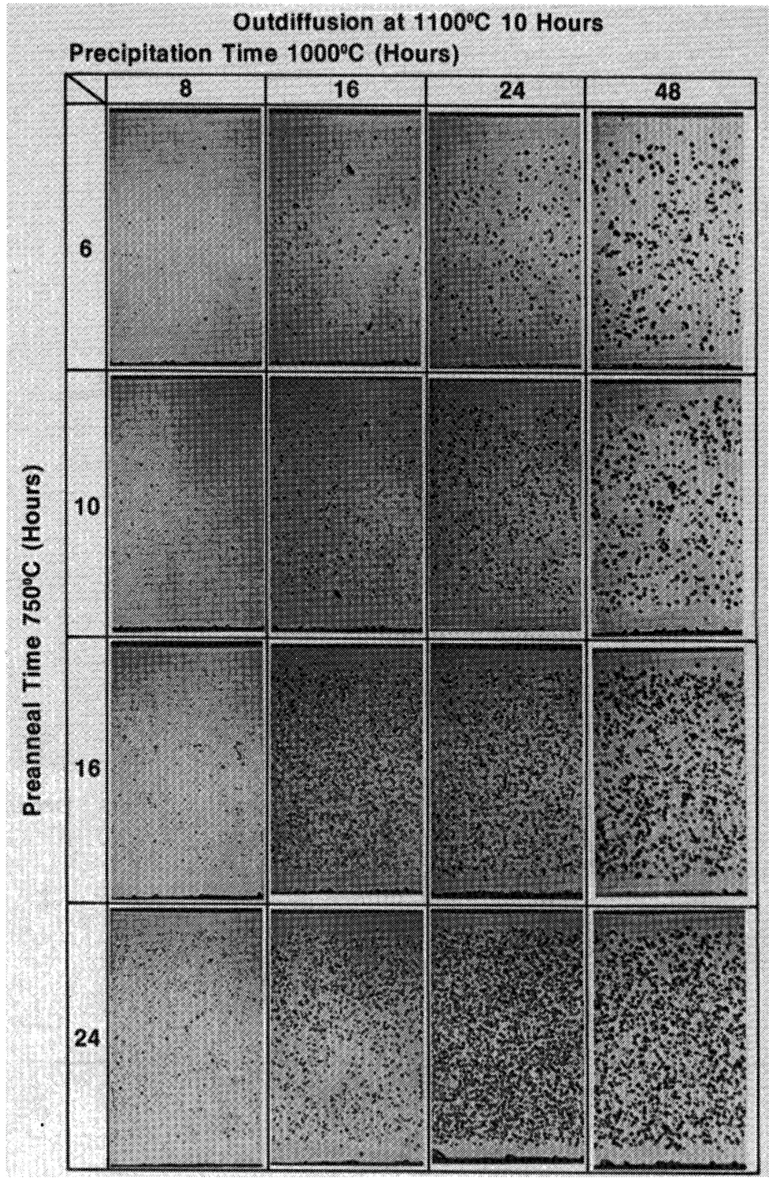




- SiO_2 embryo formation in bulk Si
- 1~3 nm at 600~700 °C
- 50~100 nm at > 1000°C



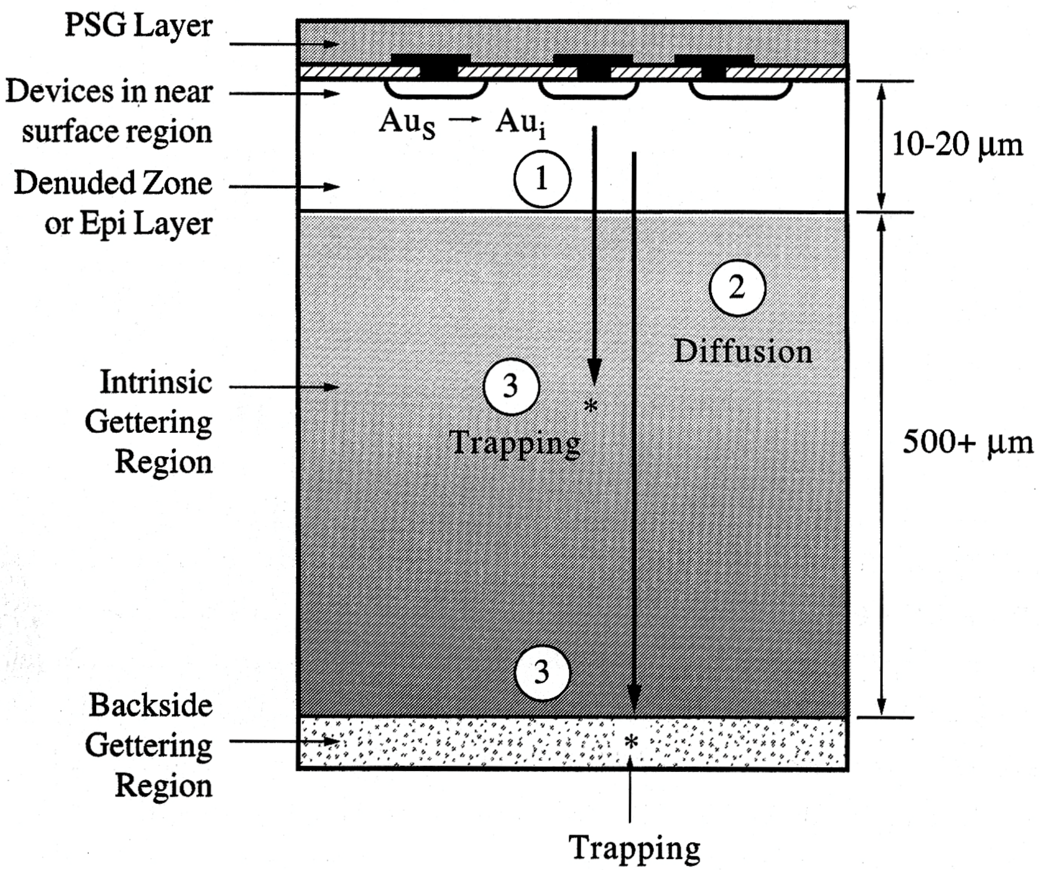
Effects of Thermal Cycle



- Cross-sectional SEM images of wafers utilizing intrinsic gettering under various process conditions.
  - A denuded zone about 25 μm deep is visible at the surface of the wafers.
  - Longer nucleation (or pre-anneal) and growth (precipitation) times result in a higher density and larger precipitates in the wafer bulk.

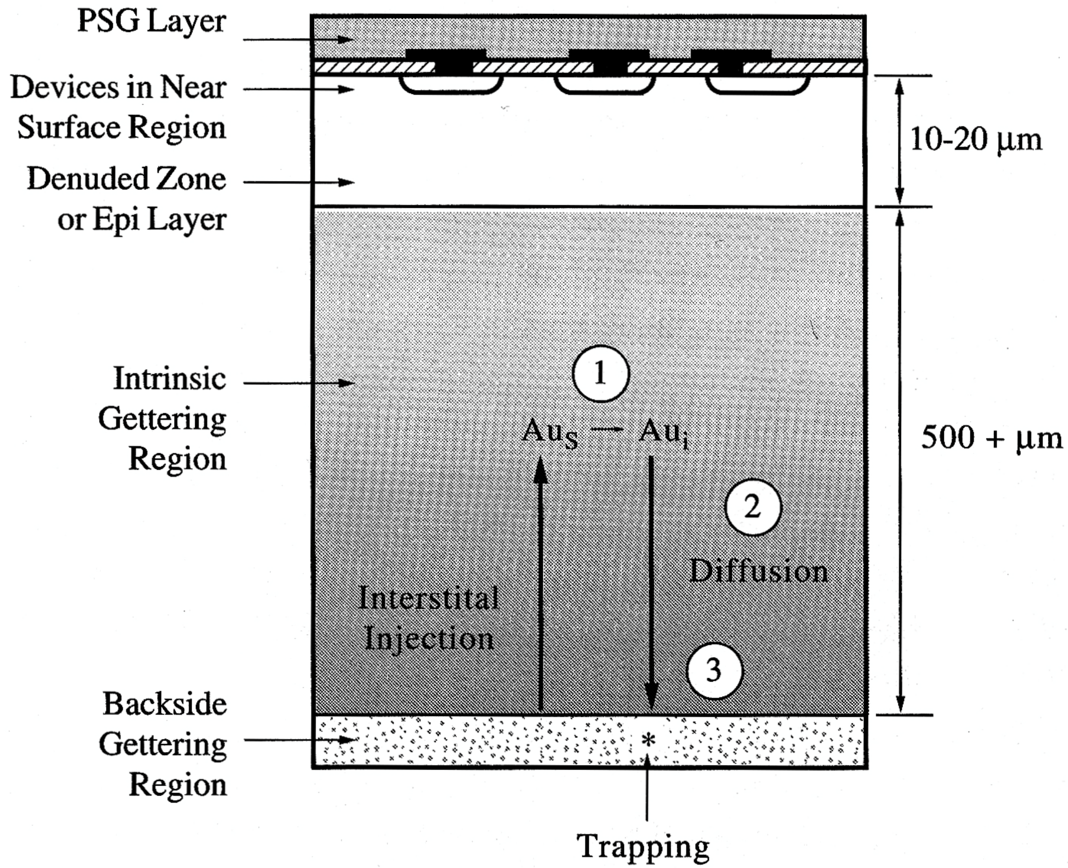
Gettering Mechanisms

3-step gettering process



Step 1: release.
Step 2: diffusion.
Step 3: trapping.

Si interstitial (*I*) injection



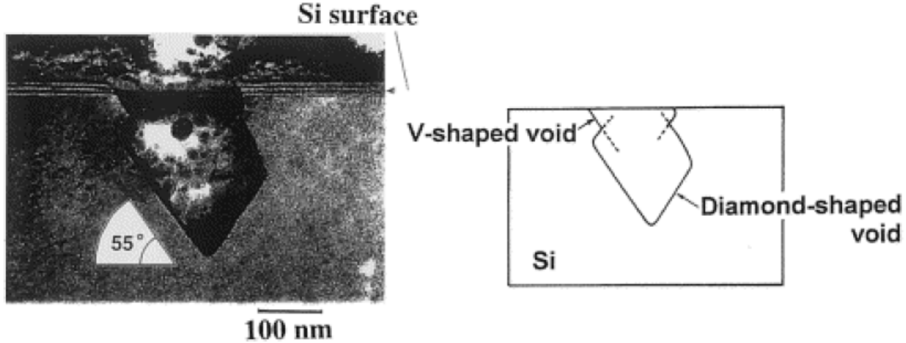
Step 1: *I* injection from the backside.
Step 2: $I + Au_S \rightarrow Si_S + Au_I$.
Step 3: backside trapping of Au.

200 mm Wafer Specifications

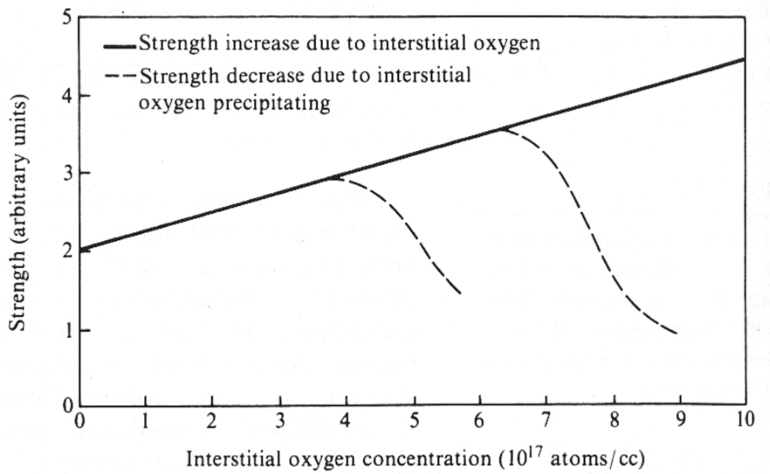
Items	Spec.	Effect
General characteristics		
Growth method	CZ	
Orientation	(100) ± 1	Oxidation
Wafer type	P-type boron doped	Oxidation
Electrical characteristics		
Resistivity (ohm-cm)	5-15	Oxidation
Radial resistivity gradient (R.R.G.)	<= 10 % (CTR-AVE)/CTR x 100	Uniformity
Minority carrier lifetime (sec)	>=1E-4	Leakage current
Chemical characteristic		
O content (ppma)	13 ± 1 (ASTM F11.88-93=0.652 ASTM F121-79)	Defects, gettering effect
Radial oxygen gradient	<= 5% (CTR-AVE)/CTR x 100	Defects, gettering effect
C content (ppma)	< 0.3 (ASTM F123-74)	Defcts
Structural characteristics		
Dislocation etch pit density (defect/cm^2) Crystal Originated Pits (COP)	< 0.13 Center cross, Edge exclusion 3 mm, Width 0.1mm	Junction leakage, Carrier lifetime, Gate oxide defects
Slip/lineage	None	Wafer crack, Junction leakage, Carrier lifetime
Swirl	None	Junction leakage, Carrier lifetime
OSF (defect/cm^2)	< 4.4 Center cross, Edge exclusion 3 mm, width 0.1mm	Junction leakage, Carrier lifetime

Wafer Specifications

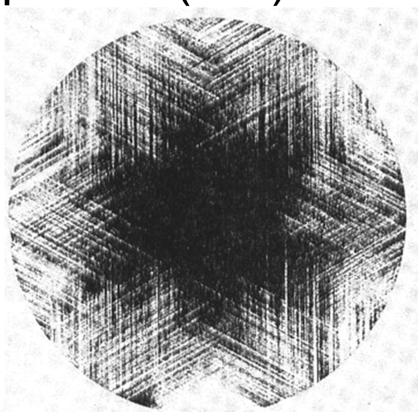
Dual-type octahedral void defect observed on CZ-Si surface

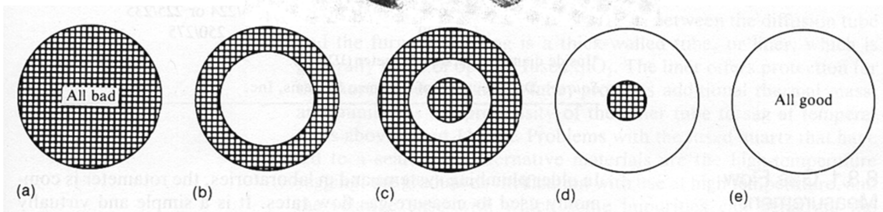


Oxygen content vs. Strength

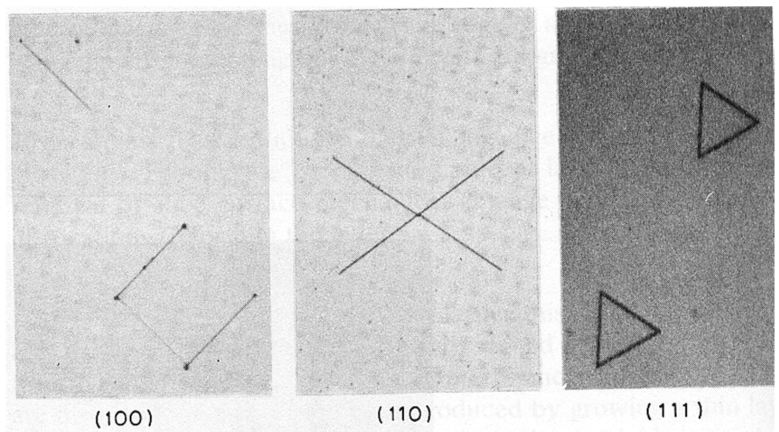


Slip of an (111)-Si wafers



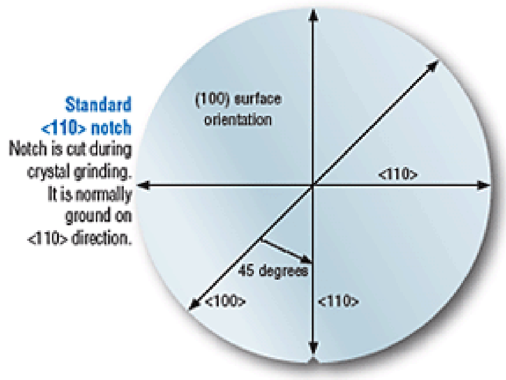


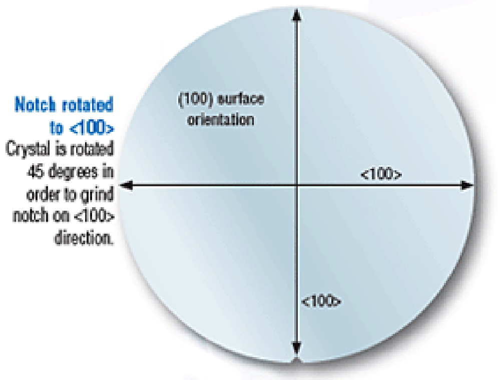
Stacking Fault after Sirtl Etch

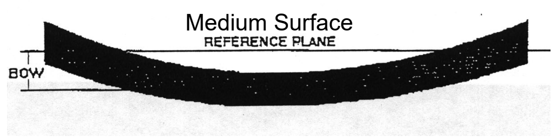


Wafer Specifications

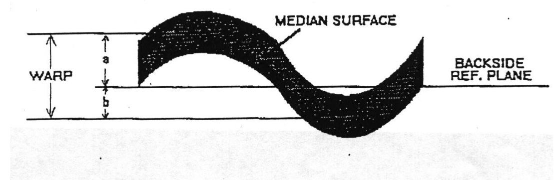
Item	Spec.	Effect
Mechanical characteristics		
Diameter (mm)	200 ± 0.2	Alignment
Notch Depth (mm)	1.00 - 1.25 (SEMI Standard)	Alignment
Notch angle (degree)	90 ± 5 (semi standard)	Alignment
Notch location	(011) ±1 (semi standard)	Alignment
Thickness (um)	725 ± 15	Wafer transfer, Wafer handling
Edge profile	Edge polished	
Bow (um)	< 65	Wafer handling, DOF
Warpage (um)	< 30	Wafer handling, DOF
TTV (um)	< 3	DOF
STIR (um) (or SFPD)	< 0.3 Reference plane : site best fit Site area 22x22 mm2	DOF
Pua (%)	100 Standard mapping, partial site inactive	Yield of flatness







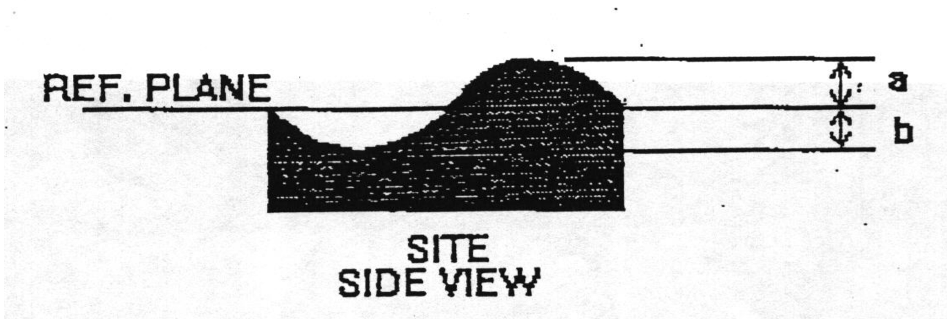
BOW



Warpage

Wafer Specifications

- Reference plane
  - Backside reference center focus
  - Frontside reference center focus
  - Site best fit
- TTV
  - Total thickness variation
  - The difference between the maximum and minimum values of thickness
- STIR
  - Site Total Indicator Reading
  - a + b
- SFPD
  - Site Focal Plane Deviation
  - Max (a, b)
- LTV
  - Local Thickness Deviation
  - STIR at backside reference center focus



Wafer Specifications

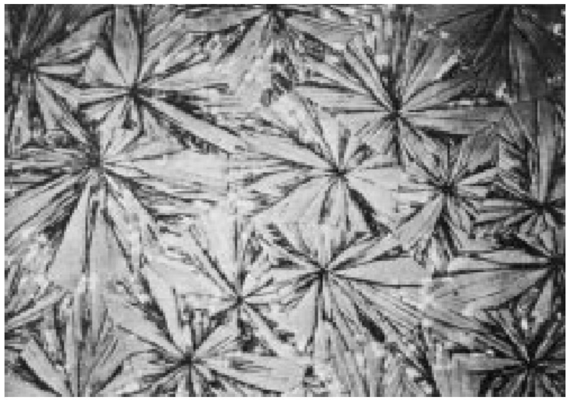
Item	Spec.	Effect
Visual inspection		
Scratch & micro scratch	None	Yield
Edge chips/Crack	None	Yield
Dimples	None	Yield
Saw marks	None	Yield
Dirt	None	Yield
Particles (cm^{-2})> 90 nm	< 0.13 Edge exclusion 3 mm	Yield
Others		
Al, Na, Ca (atom/cm^2)	$< 2x10^{10}$	Junction leakage, Carrier lifetime, Oxide charge, Oxide integrity
Zn, Cu, Fe, Ni (atom/cm^2)	$< 2x10^{10}$	Junction leakage, Carrier lifetime, Oxide charge, Oxide integrity
Backside treatment	Etched or soft backside damage	Wafer transfer
Laser mark	Yes	
Lot traceability	Yes	

Purpose of Wafer Cleaning

Contamination	Possible sources	Effects
Particles	Equipment, ambient, gas, De-ionized (DI) water, chemical	Low oxide breakdown field, Poly-Si and metal bridging-induced low yield
Metal	Equipment, chemical, reactive ion etching (RIE), implantation, ashing	Low breakdown field, Junction leakage, V_t shift, Reduced minority lifetime
Organic	Vapor in room, residue of resist, storage containers, chemical	Change in oxidation rate
Micro-roughness	Initial wafer material, chemical	Low oxide breakdown field Low mobility of carrier
Native Oxide	Ambient moisture, DI water rinse	Degraded gate oxide, low quality of epi-film, high contact resistance, poor silicide formation

Pre-oxidation Clean

- In nature, SiO_2 exists as quartz and sand.
- Thermally grown SiO_2 is amorphous.
- Tends to cross-link to form a crystal.
- Defects and particles can be the nucleation sites
- Crystallized SiO_2 with poor barrier capability.
- Need clean silicon surface before oxidation.



Silicon Dioxide Grown on Improperly Cleaned Silicon Surface.

Ultra Clean Chemistries

- $H_2SO_4 : H_2O_2$ = 3 : 1 to 5:1 (Sulfuric-peroxide mixture, SPM)
  - 65-75°C for 10-20 min.
  - Dissolve heavy organic molecules
  - Remove heavy metals
- $NH_4OH : H_2O_2 : H_2O$ = 0.25 : 1 : 5 (RCA-1, SC-1, APM)
  - 65-75°C for 10-20 min.
  - Oxidize organic molecules
  - Complex IB (Cu, Ag, Au), IIB (Zn, Cd, Hg) metals and Ni, Co, Cr, etc.
  - Remove particles (with megasonic)
- $HF : H_2O$ = 1: 50 (1 min) (Option)
- $HCl : H_2O_2 : H_2O$ = 1 : 1 : 6 (RCA-2, SC-2, HPM)
  - 65-75°C for 10-20 min.
  - Remove alkali ions and Al^{3+}, Fe^{3+}, Mg^{2+} ions, etc.
- HF-last (Option)

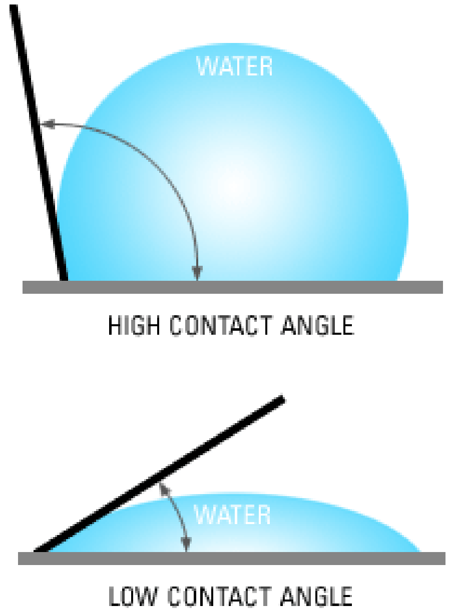
Effect of HF Dip

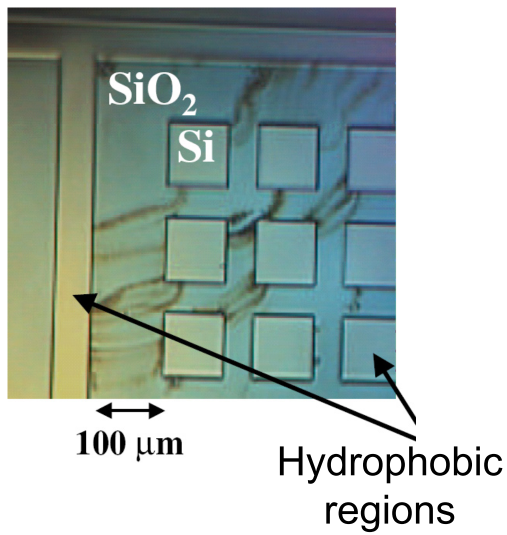
➢ HF-last

- Hydrophobic surface (large water contact angle)
- Stable H-terminated surface (no chemical or native oxide)
- Low metallic contamination levels easily obtained.
- Drying of mixed hydrophobic/hydrophilic surfaces difficult
  - Water droplets can be formed which results in formation of water marks.
  - Particle re-contamination possible.

➢ Non HF-last

- Hydrophilic surface (low water contact angle)
- Chemical oxide passivated (0.6~1 nm), long term stability.
- Hydrophilic surface can be more easily dried without water mark.
- Ultra-pure conditions needed for chemical oxide growth.
- Trade-off between particle and metal contamination (Zeta potential vs. pH)
- Higher organic contamination absorption (polar surface due to oxide).





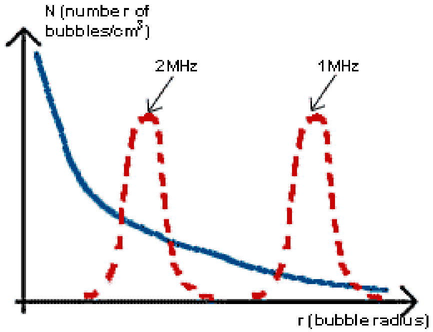
Other Clean Chemistries

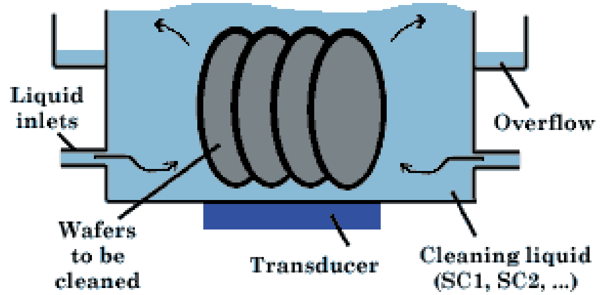
- One step ultra-cleaning
  - SC1 + DHF
  - SC1+chelating agents
    - Tetramethylammonium hydroxide (TMAH), ethylenediaminetetraacetic acid (EDTA)
- General Clean (pre-lithography clean, etc.)
  - $H_2SO_4 : H_2O_2 = 3 : 1$ or $5 : 1$
- Quartz Tube and Furnace Parts Clean
  - Dilute HNO_3
  - Dilute HF
  - D. I. Water rinse
- Solvents
  - IPA (isopropyl alcohol, C_2H_7OH, 異丙醇)
  - ACE (Acetone, 丙酮)
  - Solvents for polymer stripping

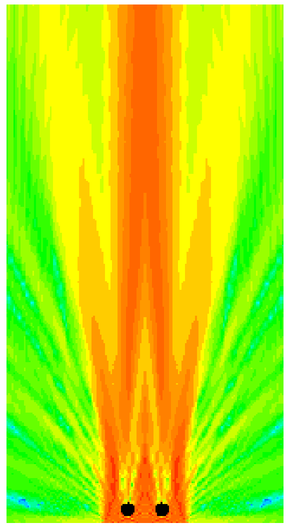
Megasonic Cleaning Technique

➢ Megasonic cleaning effects :

- **Pulsating bubbles**: When considering any liquid, there is gas dissolved in it, in the form of small bubbles (a few µm). When subjected to acoustic waves, these bubbles tend to vibrate when their diameter is adapted to the excitation frequency.
- **Microstreaming**: When high energy acoustic waves propagates in a medium, vortices are created
- **Electrical field effects**: The high pH of the solution also supplies a favorable electrokinetic environment for particle repulsion from the wafer surface because the silica particles and the oxidized wafer surface are both negative charged. This repulsion works to minimize redeposition.
- **Chemical reactions enhancement**: Megasonic waves acts as a catalyst in the reaction of creation of hydroxyl radicals. For example, if nitrogen is dissolved in the water, there will be a local creation of ammonia (and so of concentrated SC1).



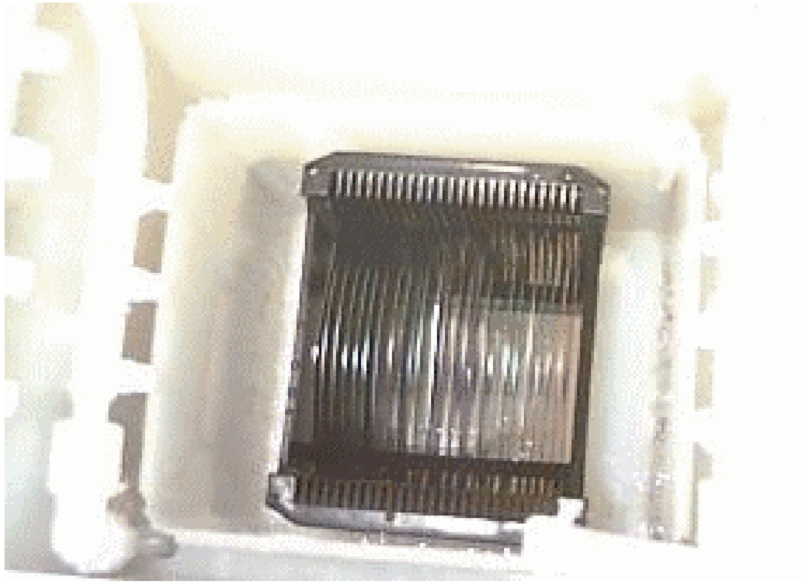




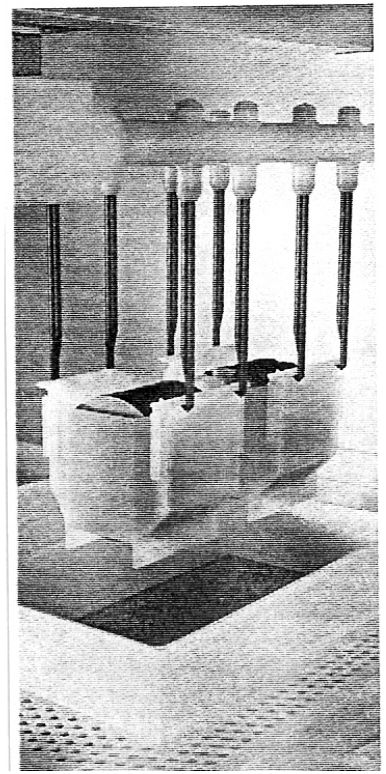
Semi-auto Wet Bench

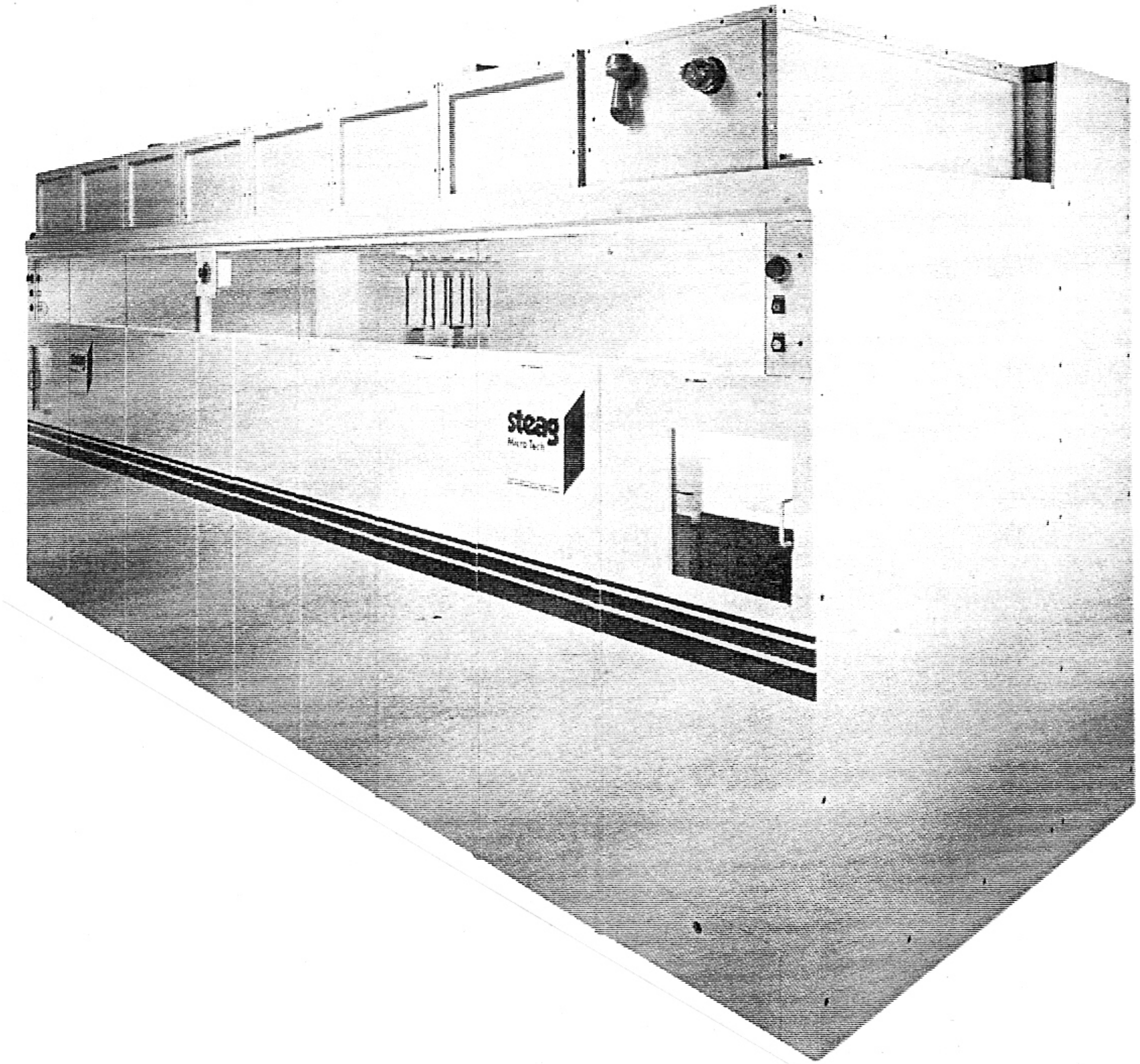
Wet Bench

DI Water Tank



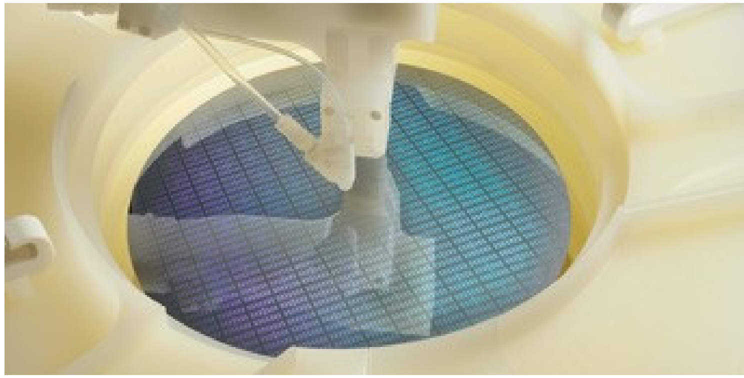
Automatic Wet Bench

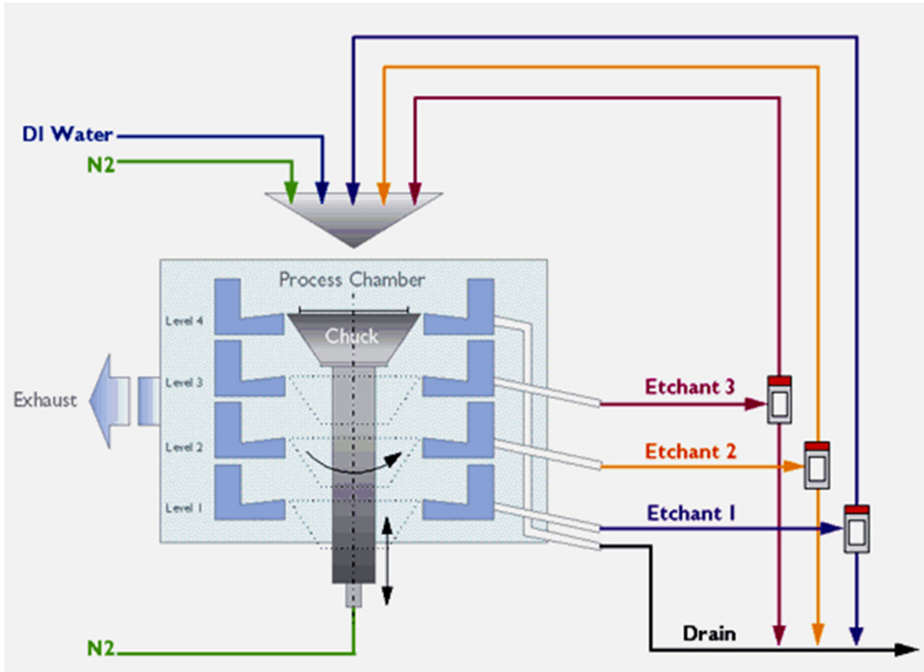




Single Wafer Wet Processor

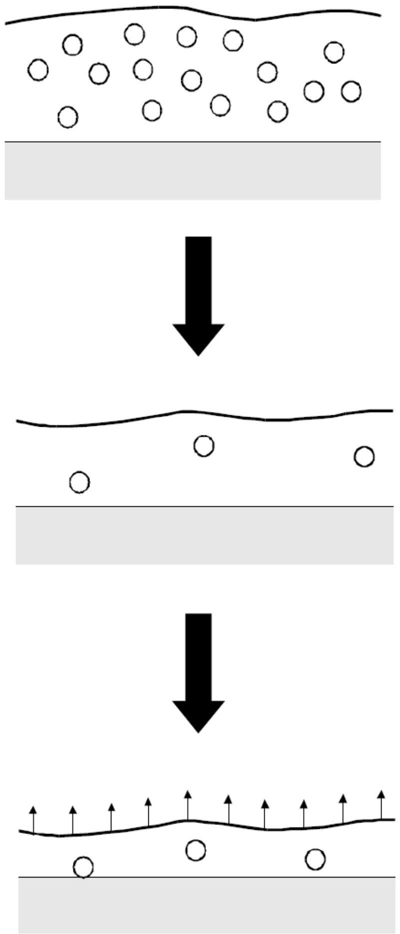
- Special features
  - Single wafer processing
  - Multi-process chamber with vertically arranged levels
  - Independent chemical lines
  - All chemicals can be recycled or drained within the system. No cross contamination occurs.
  - The opposite side of the wafer (the side not being processed) is fully protected by the N_2 cushion
  - Chuck with wafer floating on N_2 cushion





Wafer Drying

- Wet cleaning = cleaning + rinsing + drying



1: Cleaning

- Remove contaminants from surface
- Keep them in solution / suspension

2: Rinsing

- = dilution of contaminants
- Requires transport into bulk → time
- Some contaminants can stay close to the surface

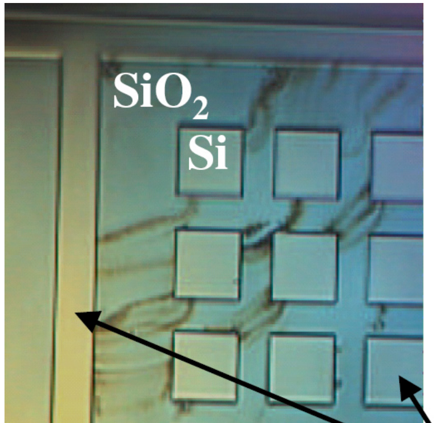
3: Drying

- Physical removal of water (e.g. high speed spinning,…)
- Evaporation (→ possibility of generating drying marks)

Spin Dryer & IPA Dryer

Stand along IPA Dryer

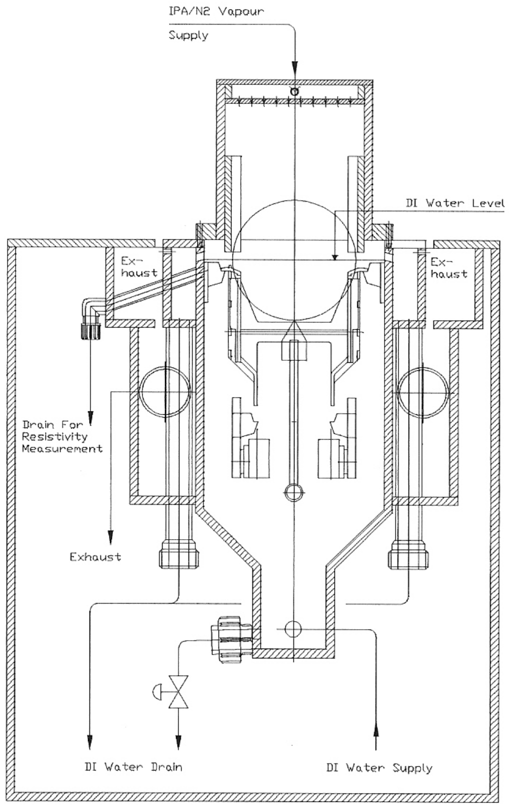
- Spin dryer
  - Centrifugal force : High rotation speed (>2000 rpm)
  - Particles entrained by air flow and risk of splash back
  - Sensitive to drying marks
- IPA spin dryer
  - Adding IPA to enhance water evaporation.
  - IPA consumption
  - Safety issue



Vertical Multi-Cassette

國立交通大學
電子工程學系暨電子研究所
National Chiao-Tung University
Department of Electronics Engineering &
Institute of electronics

Marangoni Dryer

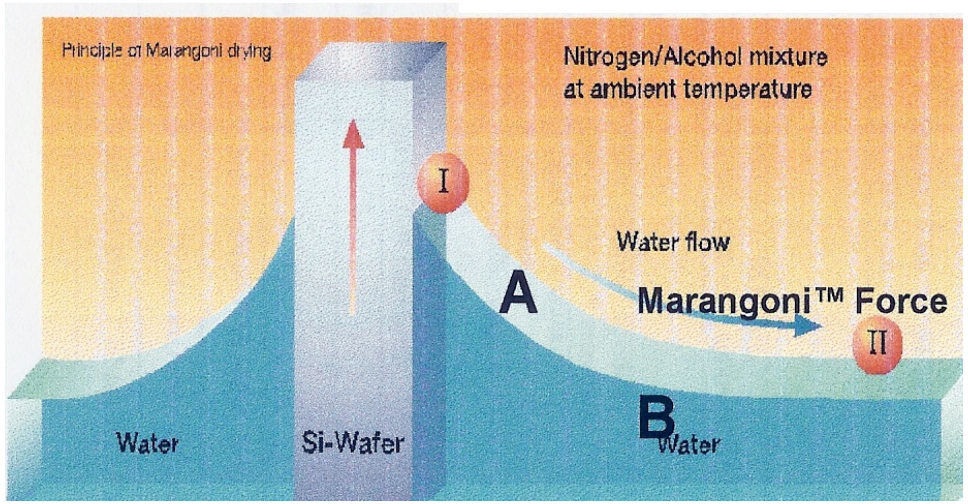


➢ Marangoni effect

- Since a liquid with a high surface tension pulls more strongly on the surrounding liquid than one with a low surface tension, the presence of a gradient in surface tension will naturally cause the liquid to flow away from regions of low surface tension. Different surface tension stress due to different IPA concentration.

➢ Drying mechanism

- IPA dissolves in water so that the surface tension stress is reduced.
- H_2O molecules migrates from low stress region toward high stress region.



Comparison of Wafer Drying Methods

- Model without evaporation [Emslie et. al., J. Appl. Phys. **29**, 858 (1958)]
  - Analytical solution
  - Newtonian liquid
  - No evaporation
  - Infinite disk

$$h(t) = \frac{h_0}{\sqrt{1 + \frac{4\rho\omega^2 h_0^2 t}{3\eta}}}$$

h: film thickness
h_0: initial thickness
ρ: liquid density
ω: rotation speed
η: liquid dynamic viscosity

	Spin Dryer	IPA Dryer	Marangoni Dryer
Drying perfromance	watermark	IPA residues	
Defect density (>0.2um) on hydrophilic surface	<0.02 /cm^2	<0.015 /cm^2	<0.01 /cm^2
Defect density (>0.2um) on hydrophobic surface	<0.05 /cm^2	<0.03 /cm^2	<0.02 /cm^2
Wafer stress	poor	good	excellent
Cost of ownership (COO)	excellent	poor	excellent
Environmental Issue	good	poor	good
Large wafer size extendibility	poor	good	excellent

- W. Kern and D. A. Puotinen, “Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology,” RCA review, vol.31, pp.187-206, 1970.