



國立交通大學
電子工程學系暨電子研究所
National Chiao-Tung University
Department of Electronics Engineering &
Institute of electronics

Introduction to IC Technology



Content

- Production of IC
- Semiconductor materials
- History of ICs
- Future trend
- IC fabrication process
- Cleanroom



Production of IC

Market Demand

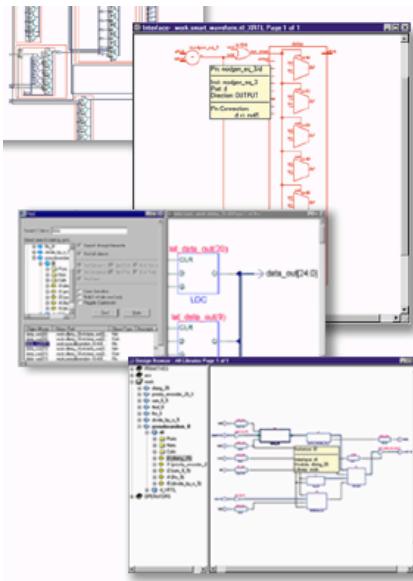
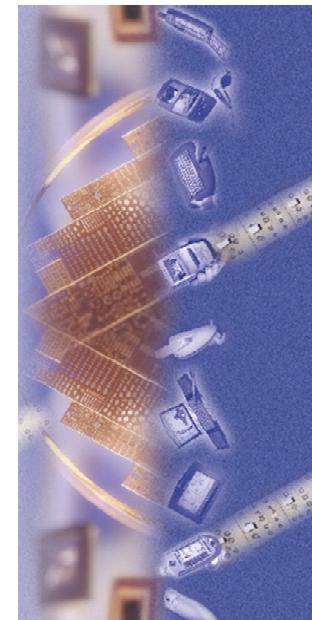
IC Design

Mask Fabrication

Wafer Process

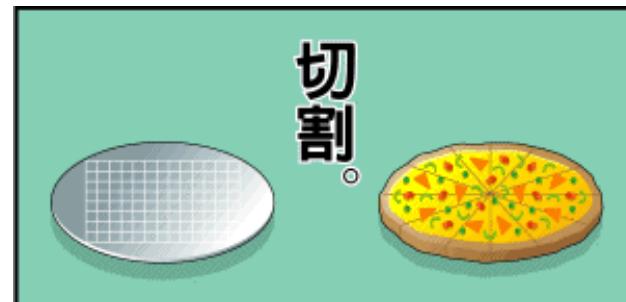
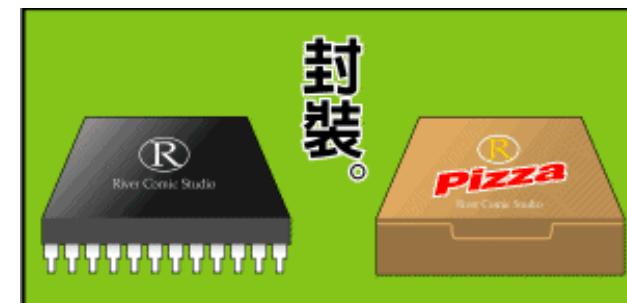
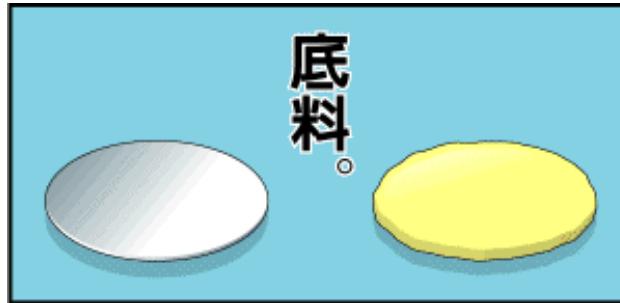
IC Package

IC Testing





Production of Pizza

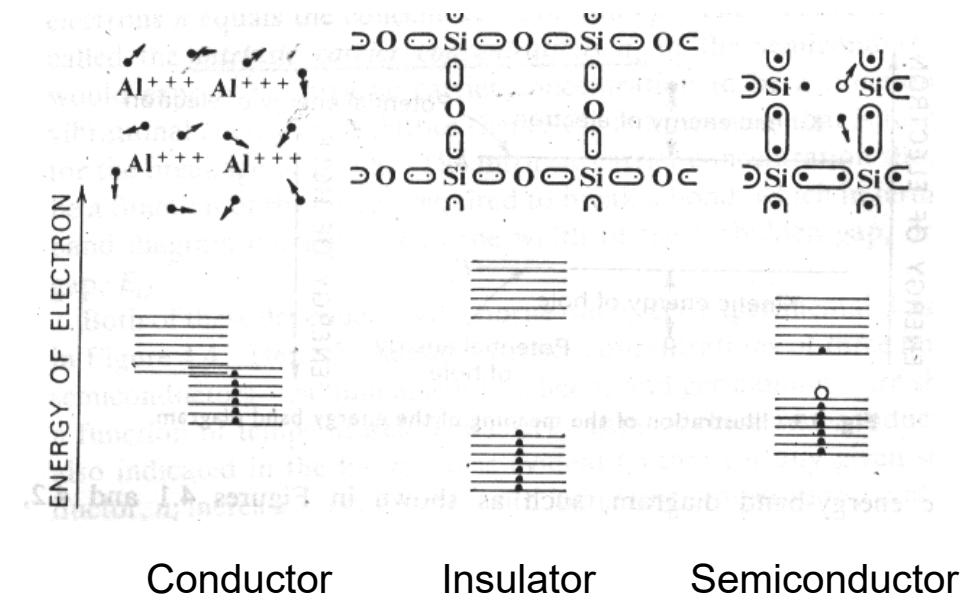
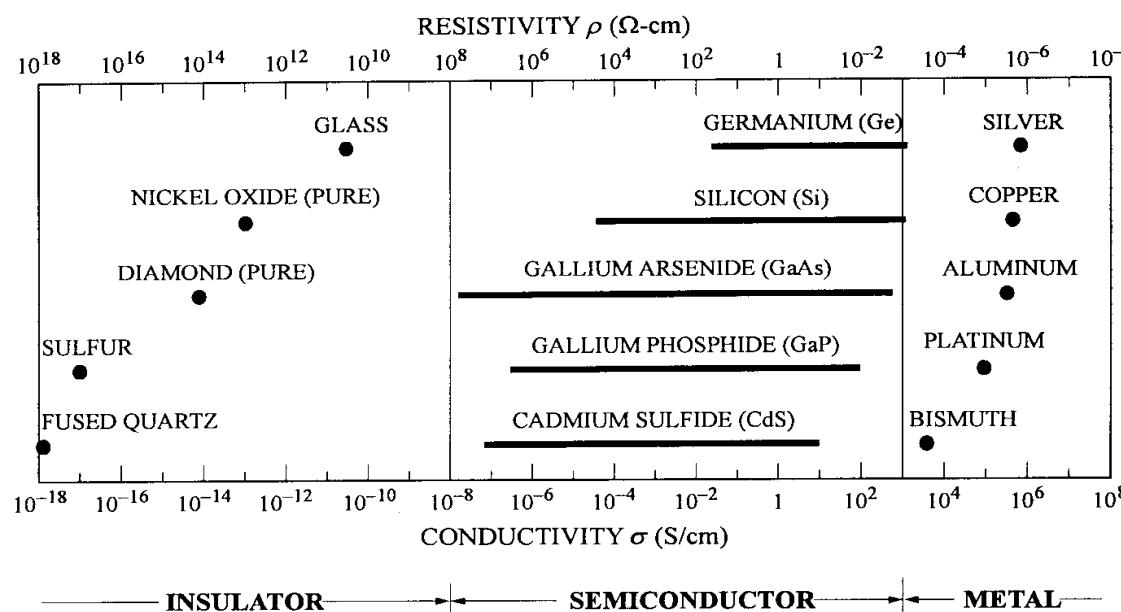


<http://www.youtube.com/watch?v=f9GXoAI8GrU>



Semiconductor

- Semiconductor is a material with conductivity between conductor and insulator.
- Elementary semiconductor- Si, Ge, C, etc.
 - Compound semiconductor - CdS, SiGe, SiC, GaAs, InAs, InP, GaP, GaN, AlGaAs, AlGaN, etc.



Basic Properties

	Ge	Si	GaAs	4H SiC	GaN	•Note
E_G (eV)	0.67	1.12	1.42	3.20	3.44	•Operation temperature •Leakage current
E_{BR} (10^5 V/cm)	1.0	5.7	6.4	33	50	•Breakdown voltage
μ_0 (cm ² /V-s)	3900	1400	4700	900	1000	•Speed
v_{peak} (10^7 cm/s)	3.1	2.3	2	1.9	2.5	•Speed
κ (W/cm-K)	0.58	1.3	0.5	2.9	1.3 Sap.0.4	•Power dissipation

- Si
 - Most commercial applications
- Compound semiconductor
 - Power devices, RF devices, special high performance devices, LED, Laser, etc.



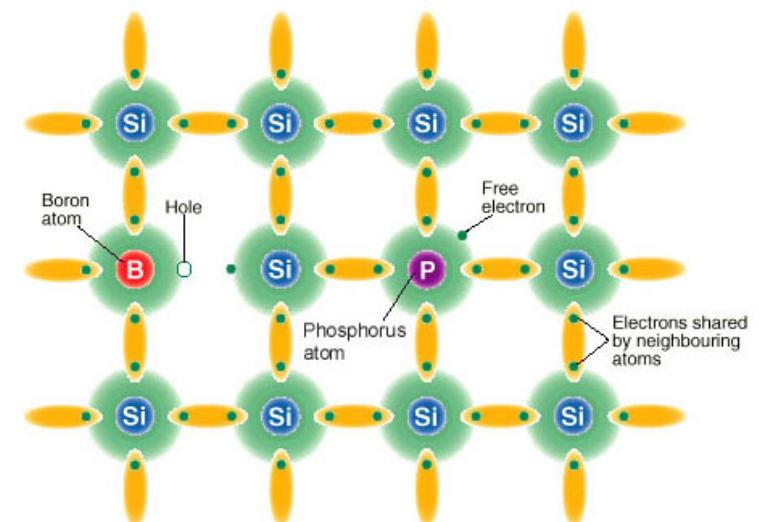
Advantages of Si

➤ Pros :

- Si is the largest amount of semiconductor element in the world.
 - 25% on the earth's surface, next to oxygen !
- It is more easy to refine high-purity Si single-crystal than the other semiconductors.
- The conductivity can be adjusted by adding dopants.
 - Adding V group elements such as P or As can increase electron concentration, n-type Si.
 - Adding III group elements such a B can increase hole concentration, p-type Si .
- React with O to form SiO_2 , an excellent insulator.
- Suitable energy band structure is suitable for most applications.
- Acceptable thermal diffusivity.

➤ Cons :

- Electron and hole mobility is not high enough.
- Si does not light.





Some Terminologies

➤ Integrated Circuit

- Integrated circuit (IC) : more than 2 semiconductor devices are fabricated on the same chip.
- Small scale ICs (SSI) < 100 devices
- Medium scale ICs (MSI) : 100-1K devices
- Large scale ICs (LSI) : 1K-20K devices (Intel 4004~2250)
- Very large scale ICs (VLSI) : 20K-1M (80286~120K)
- Ultra large scale ICs (ULSI) : 1M-10M devices (80486~1.18M, Pentium~3.1M)
- Giant scale ICs (GSI) : >10M devices (P5~13.5M, P3~24M, P4~42M)

➤ Technology generation

- If the finest resolution of a integrated process is 0.18 μm, the process is called the 0.18 μm process.
- The period between 0.18 μm and 0.13 μm is called the 0.18 μm generation.
- The finest resolution scales to 70% in each generation. The area of the same IC can be reduced by 50%.
- After 90 nm process, **technology node** is used to describe technology. The definition becomes complex.

Major Breakthroughs in Semiconductor Industry

- First transistor (point contact, polycrystalline Ge), 1947.
- First single crystal germanium (CZ wafer), 1952.
- First single crystal silicon (CZ wafer), 1954.
- First planar transistor, 1957.
- Invention of IC, 1958.
- First realized MOSFET, 1960.
- First IC product, 1960.
- 1T1C DRAM cell, 1967.
- Floating-gate device for NVM, 1967.
- Charge-coupled device (CCD), 1970.
- Flash NVM, 1984.



Inventors of Transistor



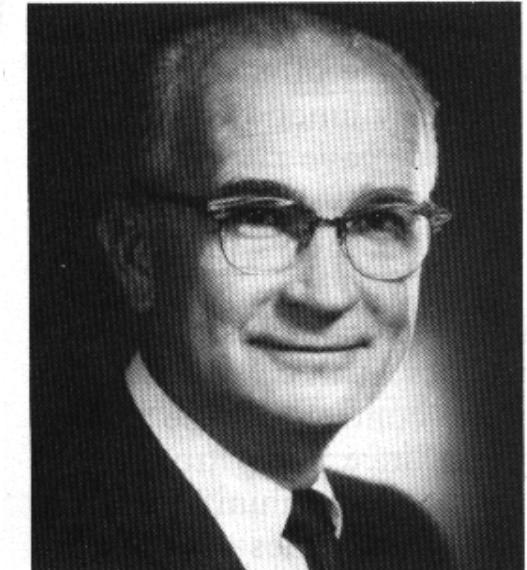
William Shockley (seated at the microscope), John Bardeen (at left), and Walter Brattain, all of Bell Telephone Laboratories, are pictured here about the time of their discovery of the point contact transistor in 1947. This work resulted in their receiving the Nobel Prize for Physics in 1956. (Source: Photograph courtesy of AT&T Archives.)



John Bardeen, co-inventor of the point contact transistor, received a second Nobel Prize in physics in 1972 for his work on the theory of superconductivity. (Source: Photograph courtesy of AT&T Archives.)



Walter Brattain was a co-inventor of the point contact transistor. (Source: Photograph courtesy of AT&T Archives.)

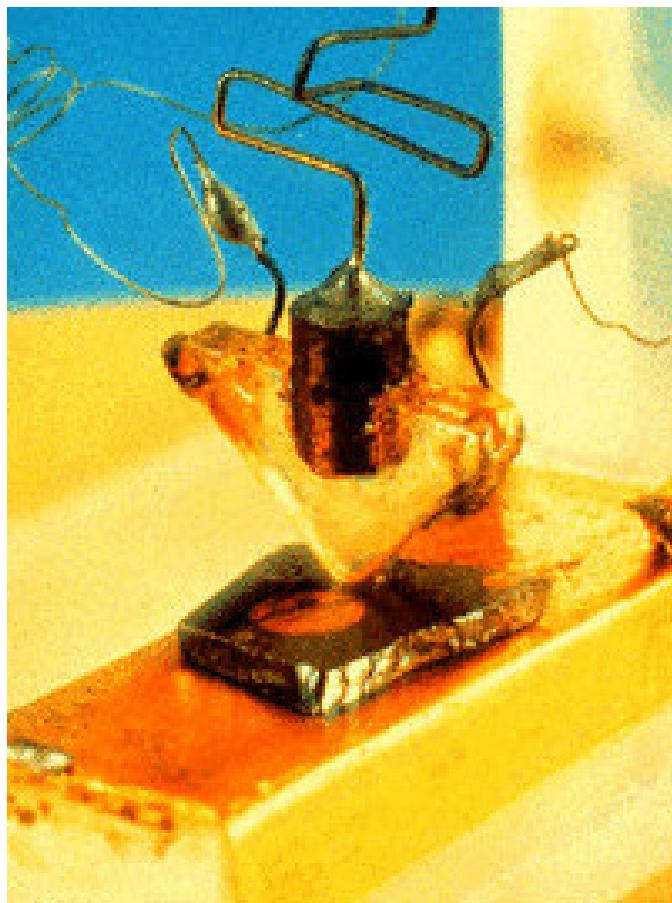


William Shockley, co-inventor of the point contact transistor, was also the inventor of the junction transistor. (Source: Photograph courtesy of AT&T Archives.)

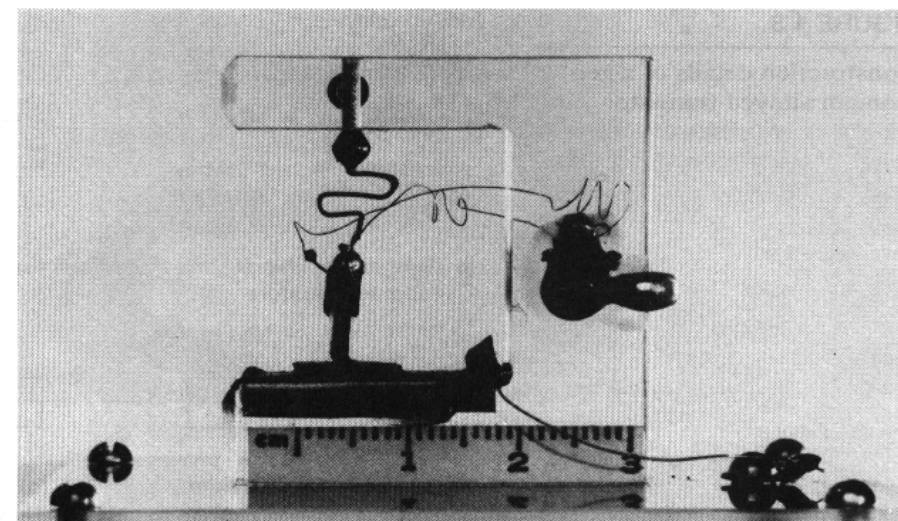


Point-contact Transistor

Point-contact transistor



- In 1947, Shockley, Bardeen, and Brattain invented point-contact transistor at Bell Lab. They received the Nobel Prize for physics in 1956.
- Bardeen received his 2nd Nobel Prize for physics in 1972 due to his pioneer contribution in superconductor.

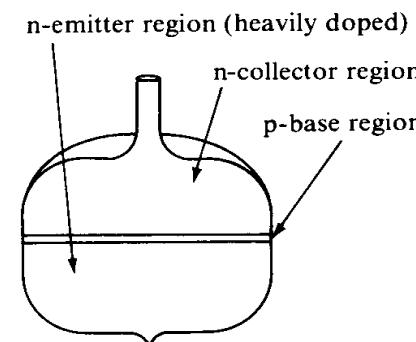
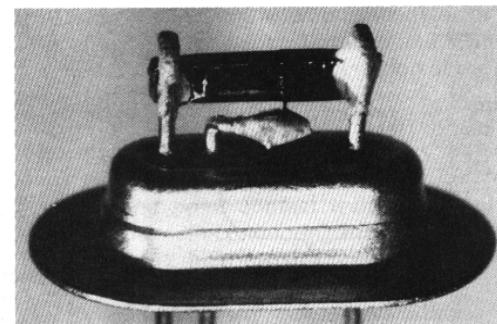


In 1951, point-contact transistor became mass-production by the Western Electronic Co.

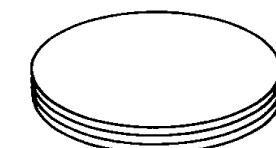


Crystal Grown Transistor

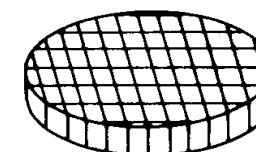
In 1951, Gordon Teal and Morgan Sparks fabricated transistor by crystal growth method.



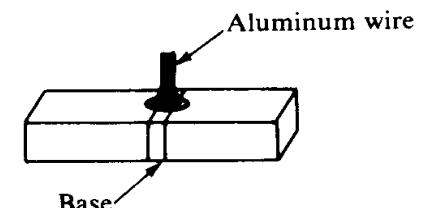
(a) Crystal cut in half for evaluation



(b) Section cut from mid-region of crystal that contains base layer and small section each of collector and emitter regions



(c) Section cut into "bars" (size, varying with power rating of transistor, but typically 30×30×150 mils)

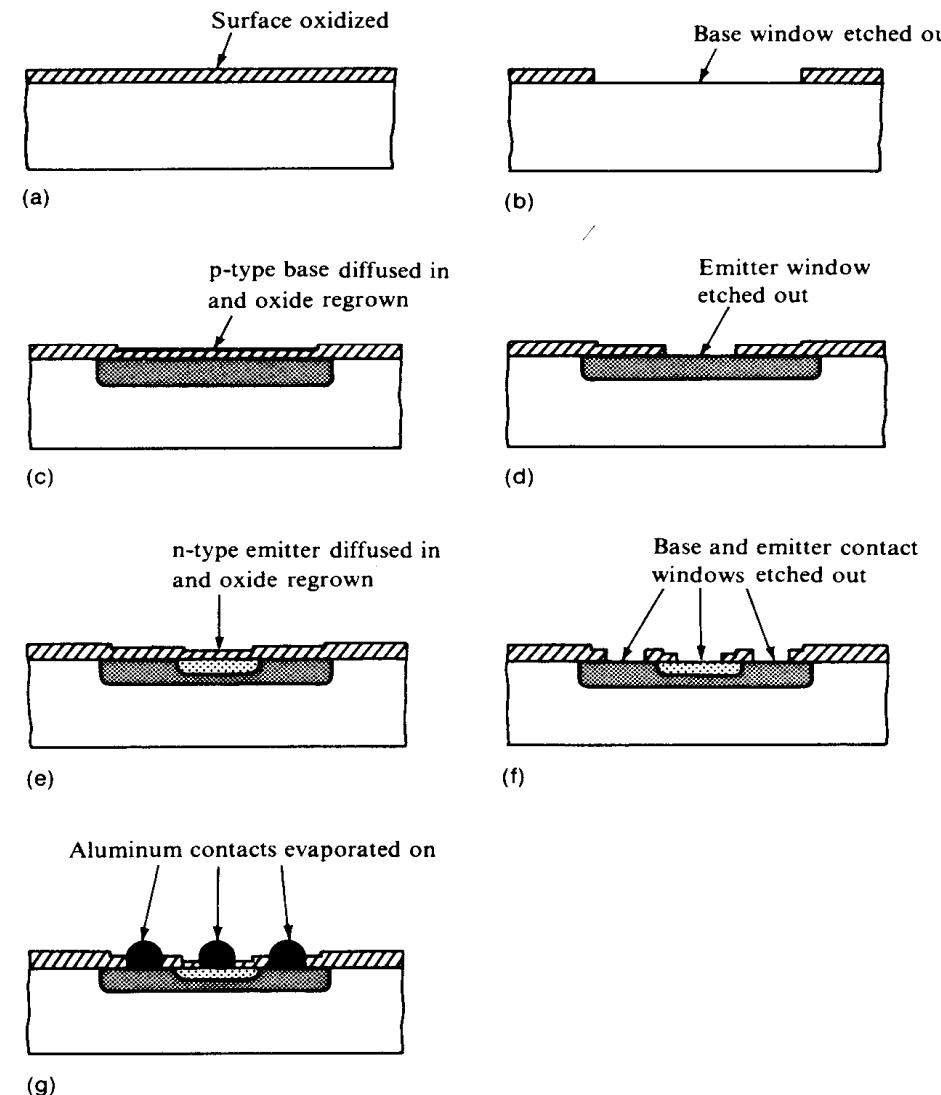
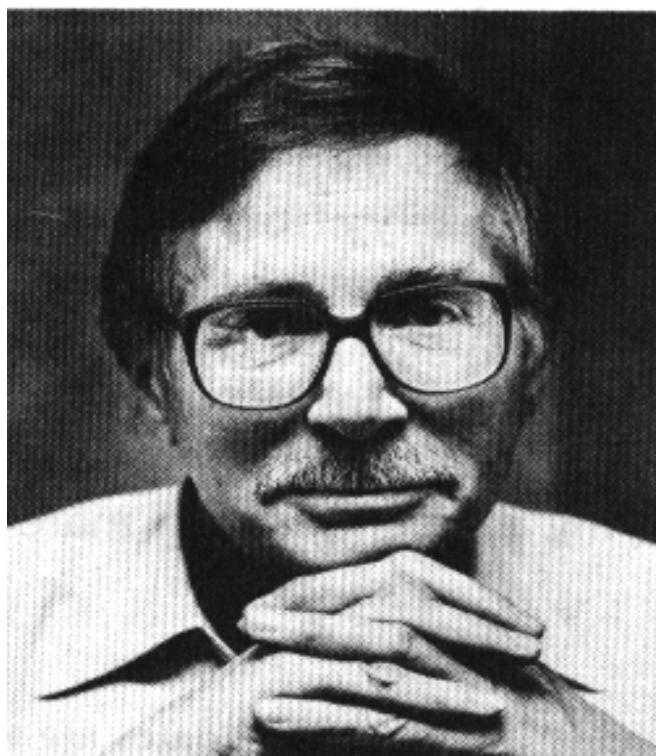


(d) Base contact formed by fusing (alloying) aluminum wire to silicon so that wire made ohmic contact to base region and rectifying contacts to collector and emitter



Planar Technology

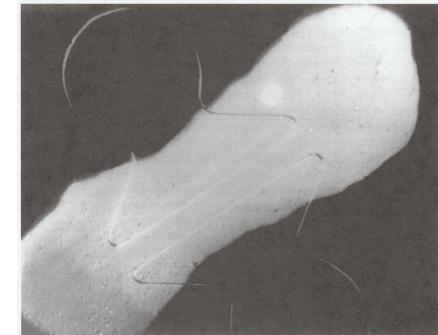
- In 1959, Jean Hoerni of Fairchild Semiconductor invented the planar technology.
- In 1961, transistors were mass-produced by the planar technology.





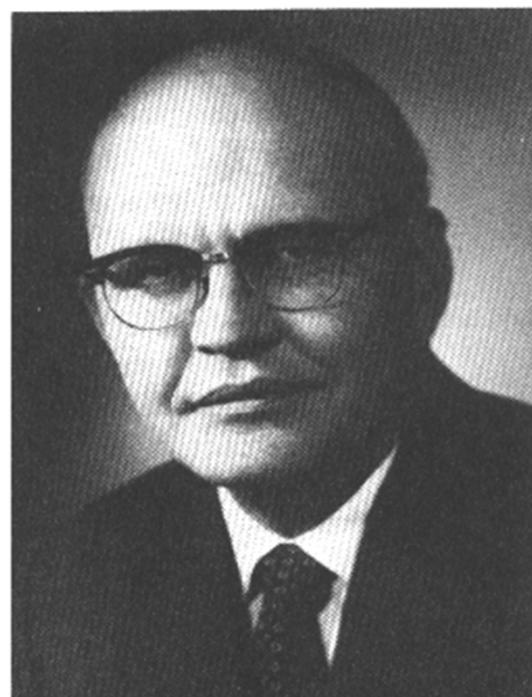
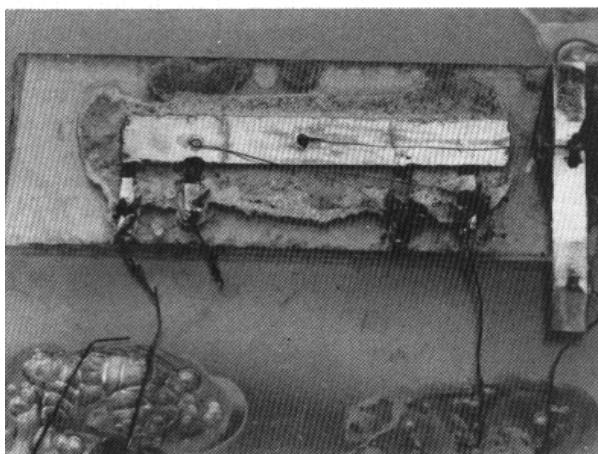
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First
MOSFET

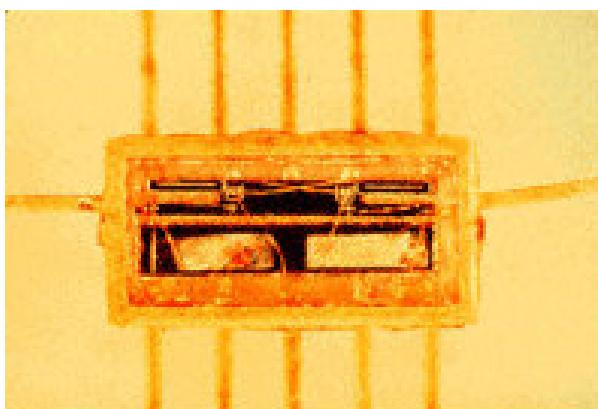


Invention of ICs

- In 1958, Jack Kilby of T. I. invented the first IC. The material is Ge. This invention was patented in 1959 and mass-produced in 1960.



Jack Kilby
2000 Nobel Prize



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semiconductor networks

Now—3 years ahead of industry's expectations—
Solid Circuit semiconductor networks from Texas Instruments for many of your high-reliability miniaturized systems!

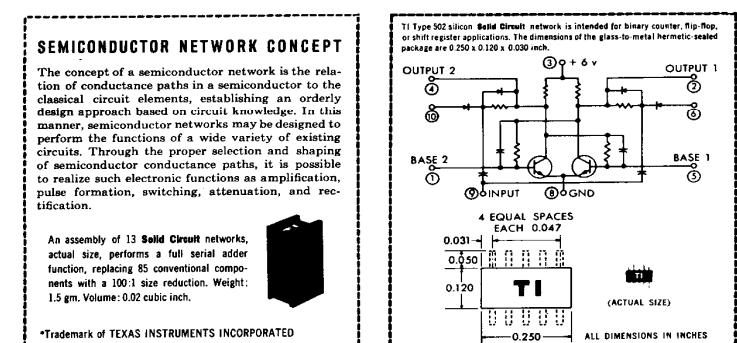
Solid Circuit networks are a major departure from conventional components because they integrate resistor, capacitor, diode, and transistor functions into a single high-purity semiconductor wafer. Protection and packaging of discrete elements is eliminated, and contacts between dissimilar materials are minimized, reducing element interconnections as much as 80%. Fabrication steps have been reduced to one-tenth those required for the same circuit function using conventional components.

SEMICONDUCTOR NETWORK CONCEPT

The concept of a semiconductor network is the relation of conductance paths in a semiconductor to the classical circuit elements, establishing an orderly design approach based on circuit knowledge. In this manner, semiconductor networks may be designed to perform the functions of a wide variety of existing circuits. Through the proper selection and shaping of semiconductor conductance paths, it is possible to realize such electronic functions as amplification, pulse formation, switching, attenuation, and rectification.

An assembly of 13 **Solid Circuit** networks, actual size, performs a full serial adder function, replacing 85 conventional components with a 100:1 size reduction. Weight: 1.5 gm. Volume: 0.02 cubic inch.

*Trademark of TEXAS INSTRUMENTS INCORPORATED



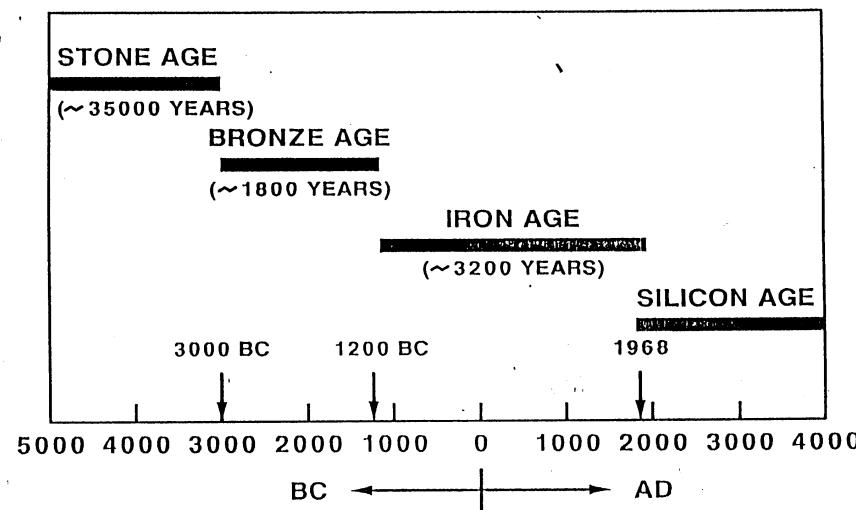
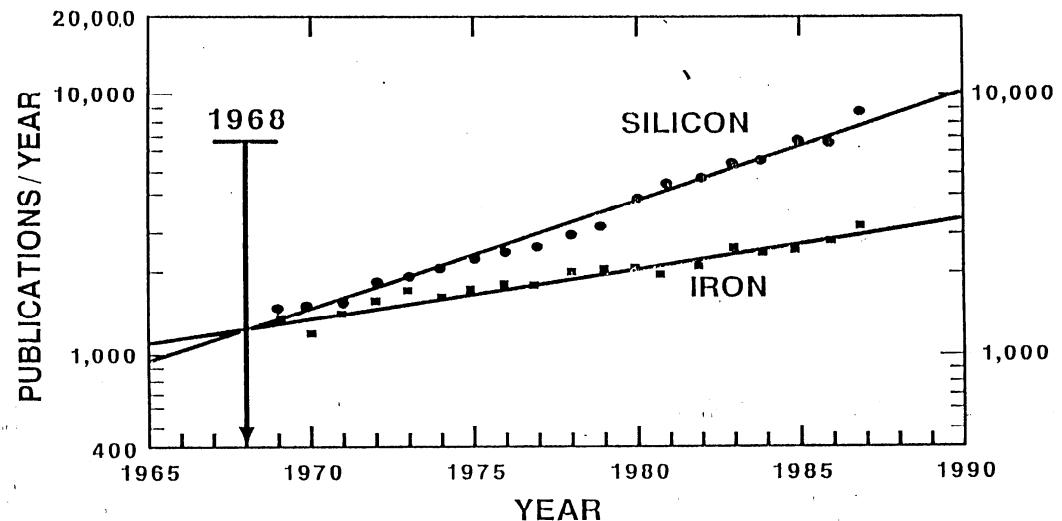
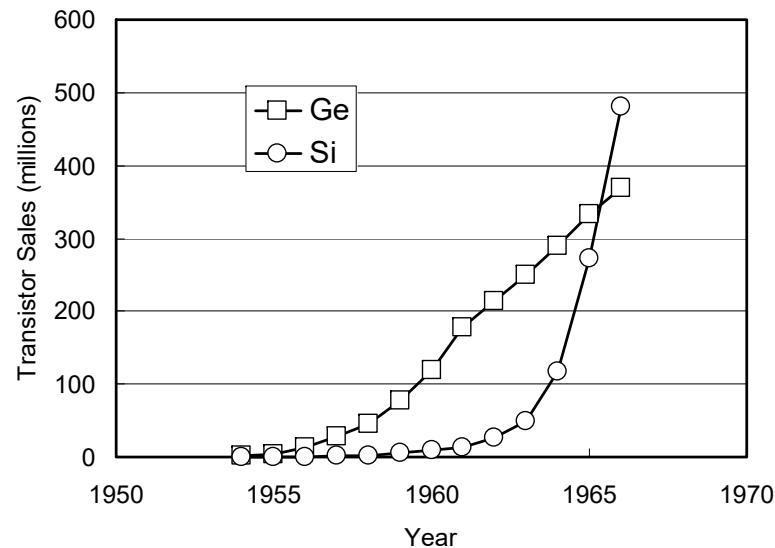
TEXAS
INSTRUMENTS
INCORPORATED

SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 312 • DALLAS, TEXAS

March 26, 1960 Business Week



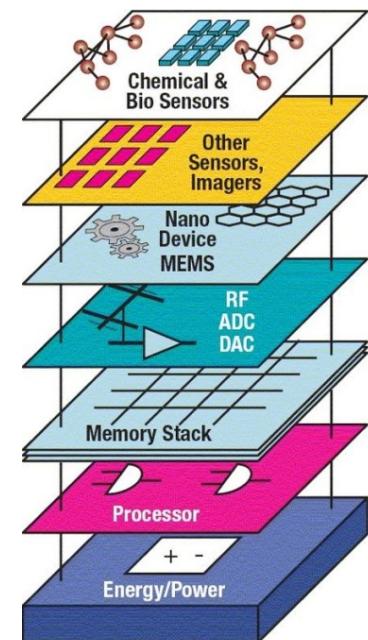
Si Age (named by S. M. Sze)



- In 1966, the amount of sales of Si transistor exceeded Ge transistor.
- In 1968, Si related papers exceeded iron related papers.

Major Breakthrough in IC Technology

- 1950' Integrated circuit
- 1960' Si replaced Ge
- 1970' MOSFET replaced BJT
Ion implantation and plasma etching are introduced
- 1980' Metal silicide process
CMP process was invented
- 1990' Shallow trench isolation LOCOS
Cu-interconnect and low-k dielectric
- 2000' Strained Si
High-k dielectric and metal gate
- 2010' 3D device (FinFET)
3D IC, Heterogeneous integration





Moore's Law

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor
division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuit will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the

machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

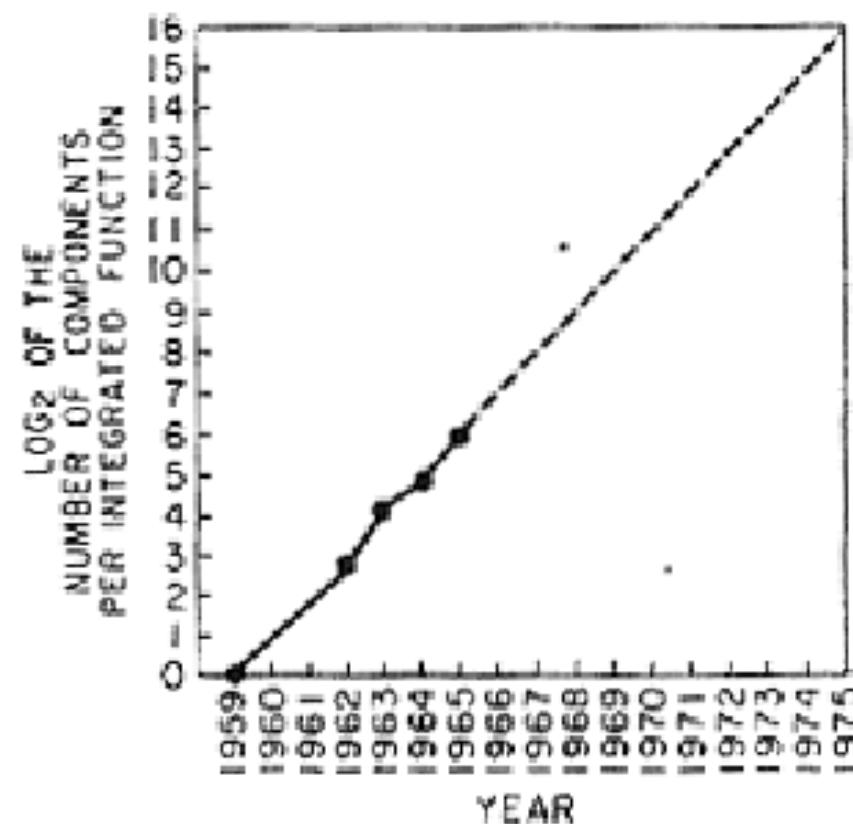
Both approaches have worked well and are being used in equipment today.



Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Electronics, Volume 38, Number 8, April 19, 1965

The complexity for minimum component costs has increased at a rate of roughly a factor of two per year (see graph on next page).

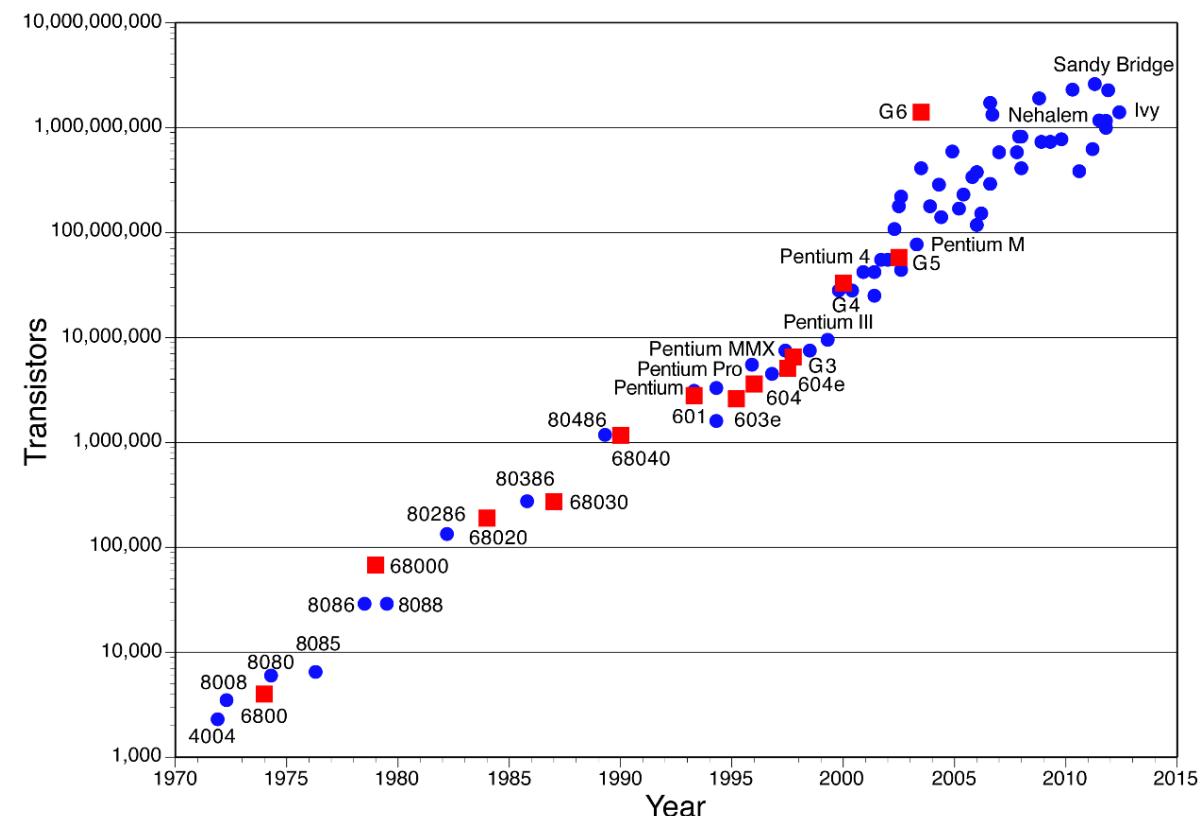




Moore's Law

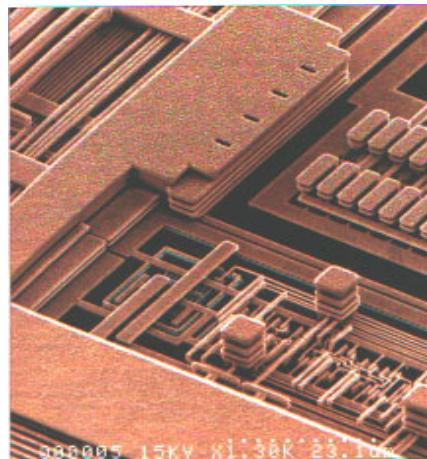
The number of the transistors per integrated circuit would double every 2 years.

	Year	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium IV processor	2000	42,000,000
Quad core Itanium	2008	2,000,000,000

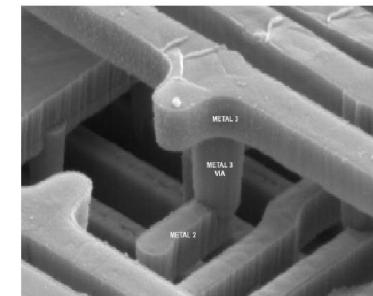
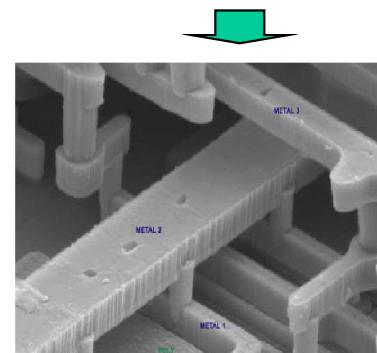




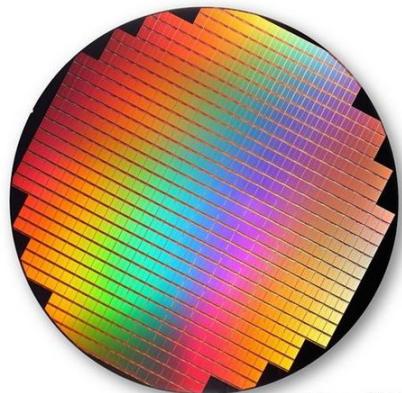
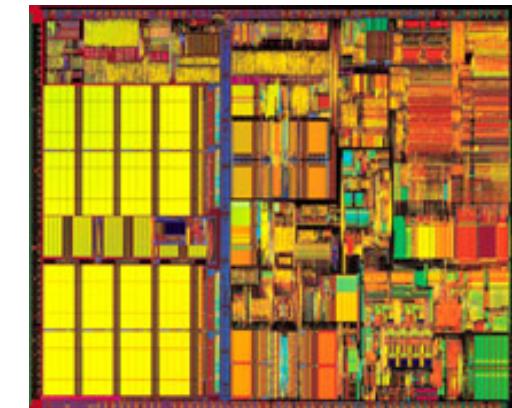
Examples of ICs



IBM, 1999



Intel, Pentium III, 1999



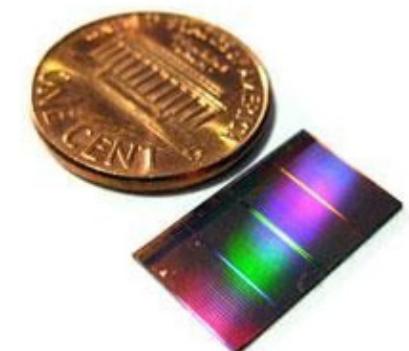
2003年
130nm
128MB

2005年
90nm
512MB

2007年
50nm
1GB

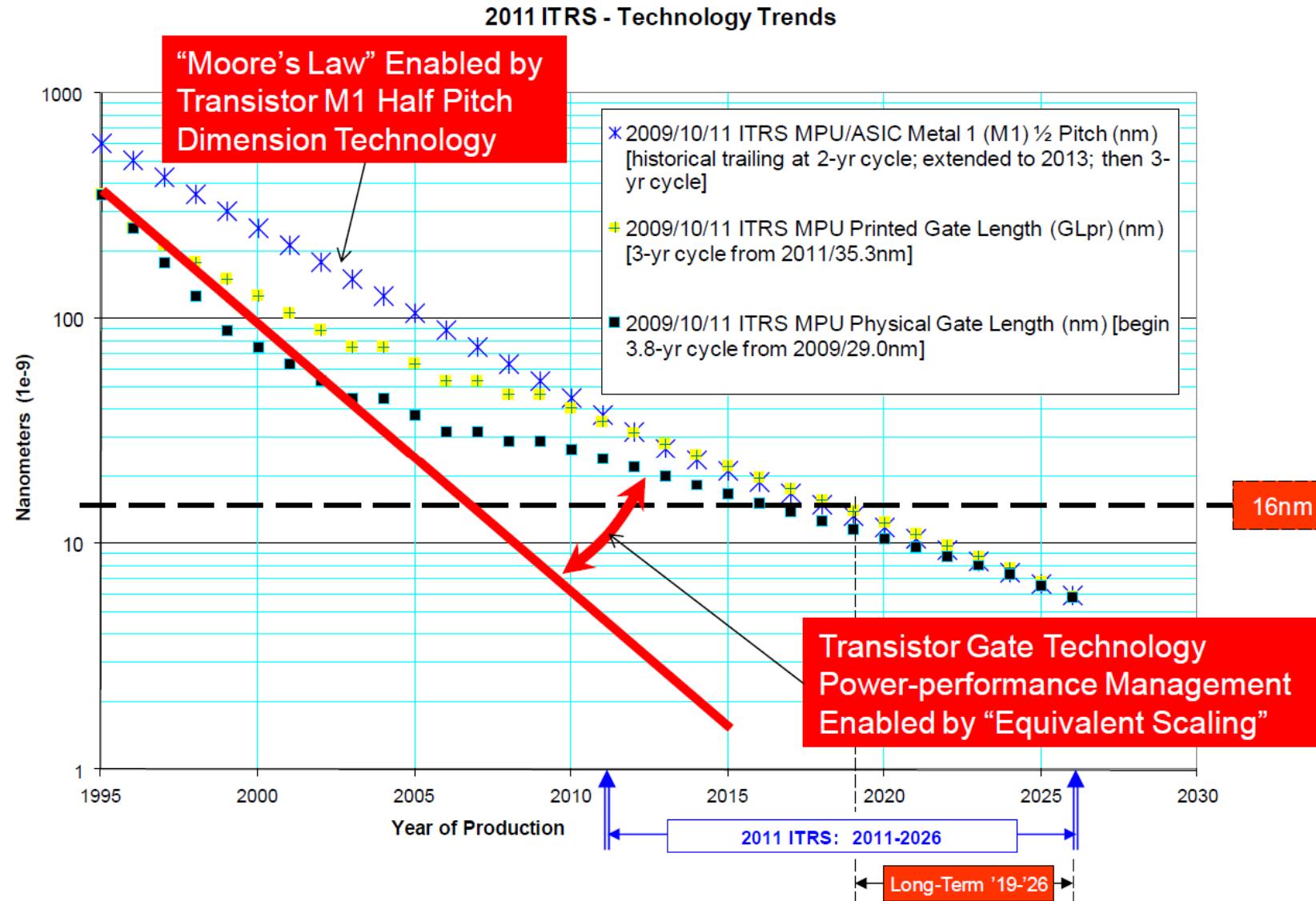
2009年
34nm
4GB

2010年
25nm
8GB



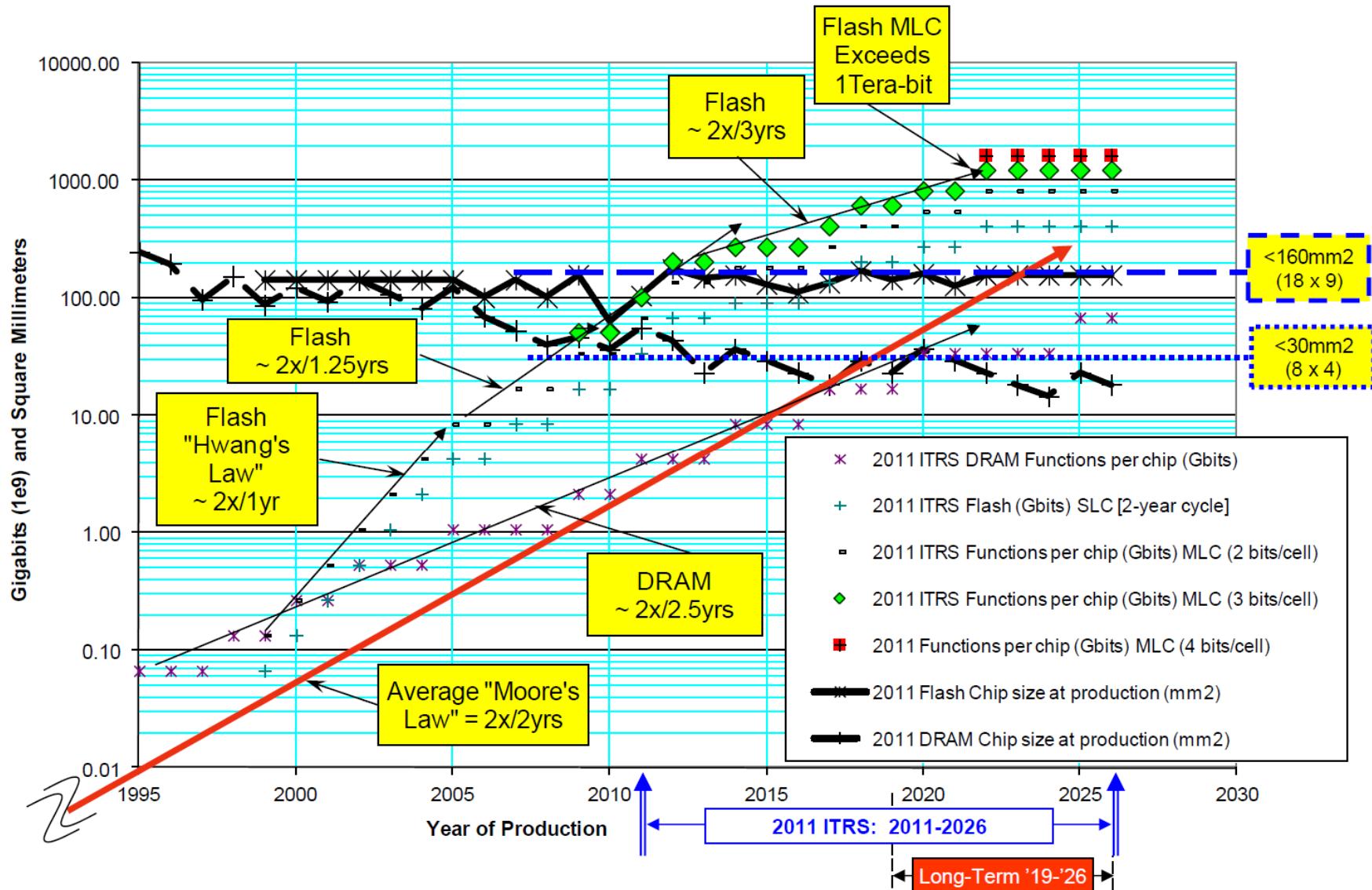


Device Scaling Trend



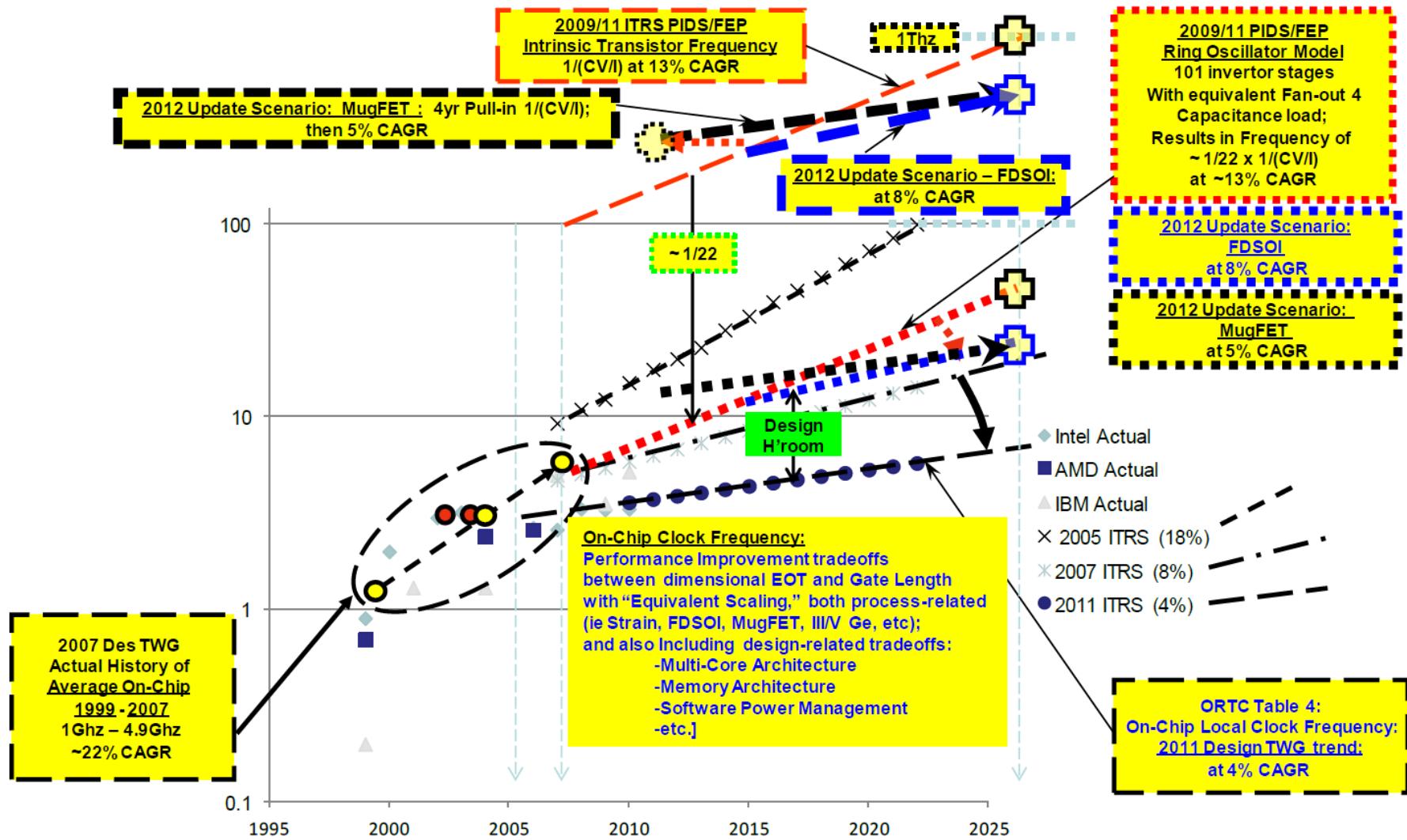


Device Density Trend



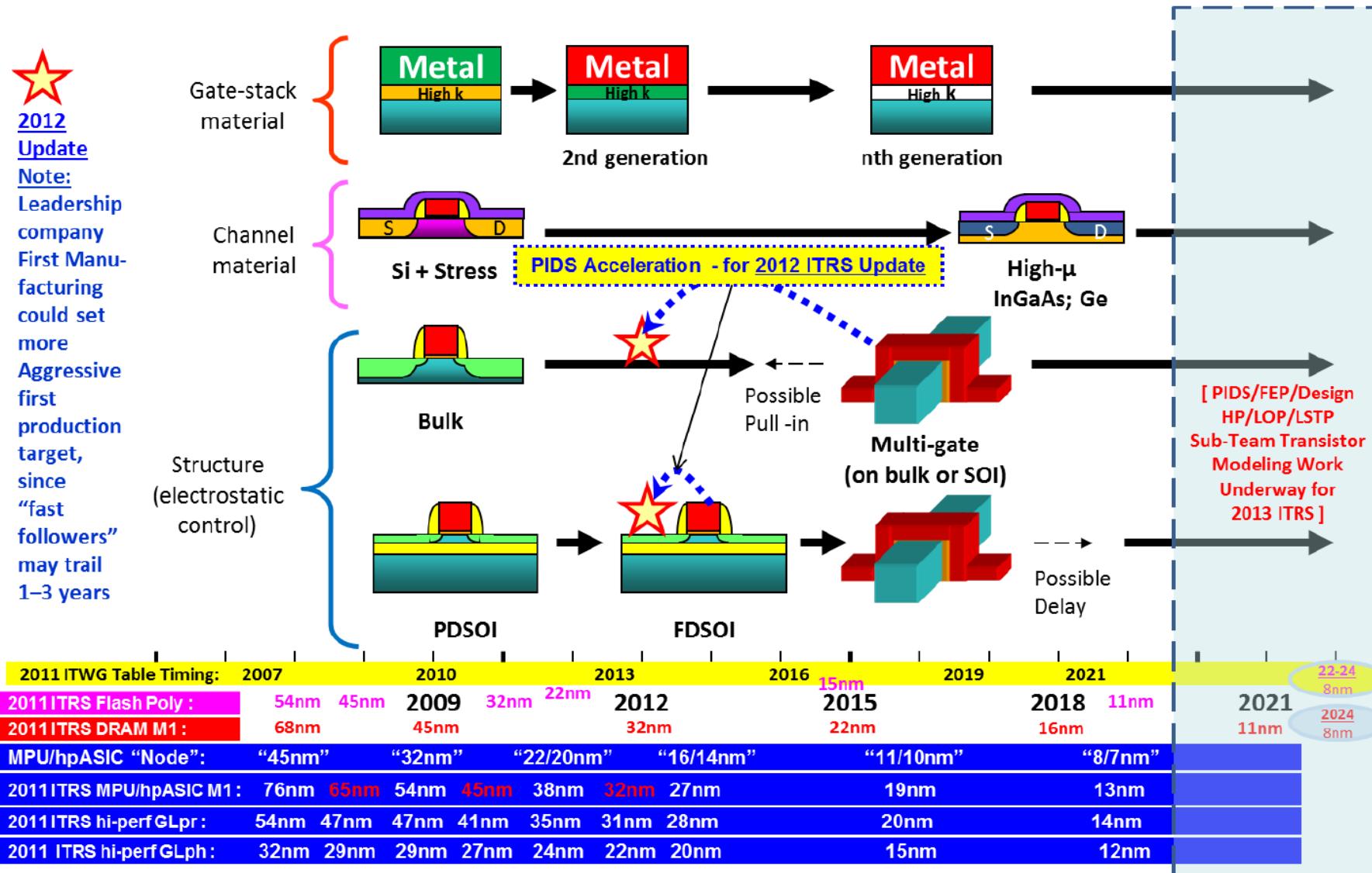


Circuit Speed Trend





Emerging Devices

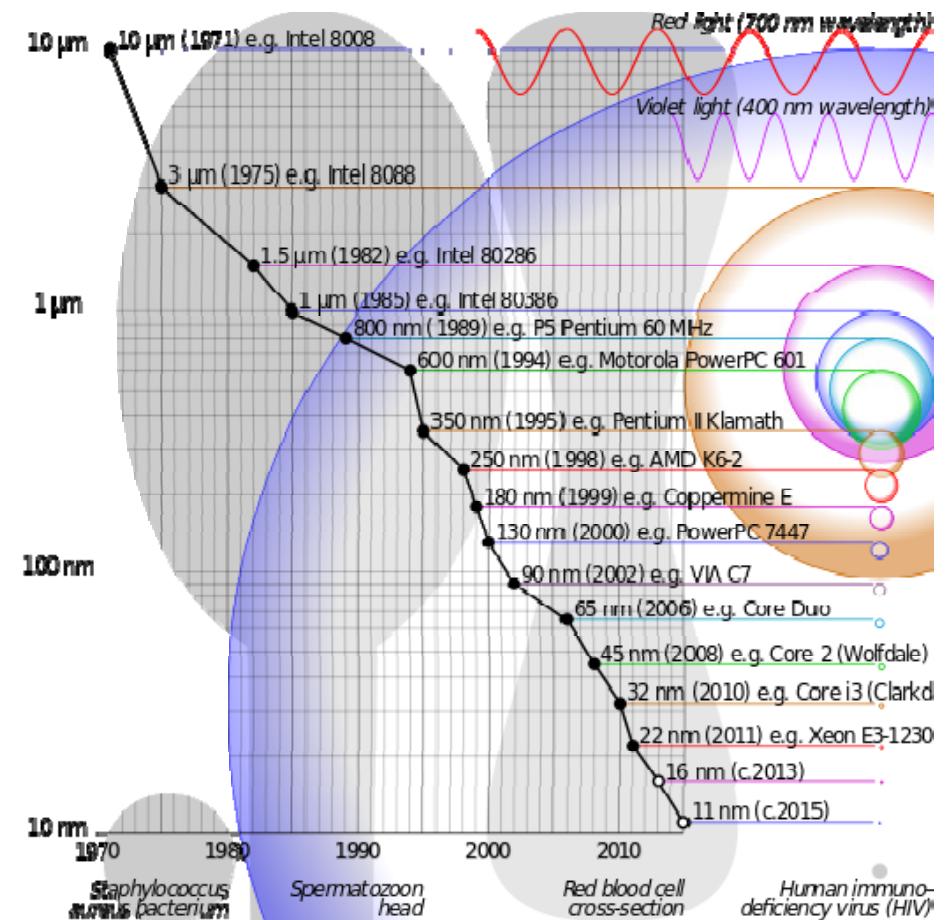




How Far Can Si Devices Go ?

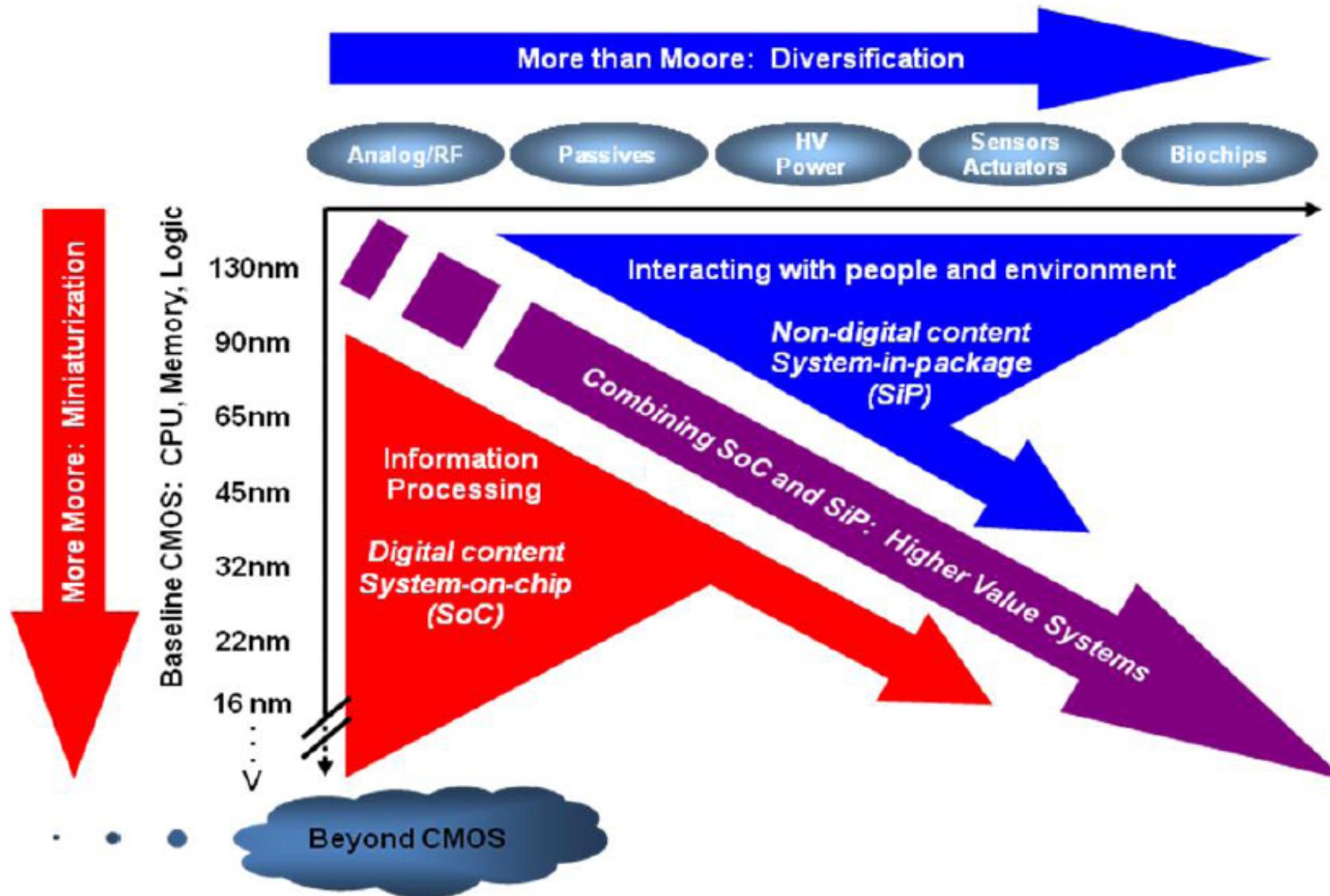
➤ Si ICs beyond 2020

- Device size < 10 nm
- Device density $\sim 10^{11}/\text{cm}^2$
- Operation speed $\sim 10^{11} \text{ Flop/sec}$
- Power consumption > 300 W
(Higher than the power density
on solar surface)
- Fab cost $\sim > \text{NT\$ 400B}$



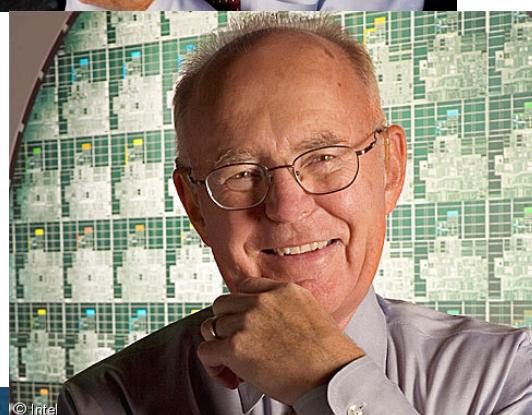
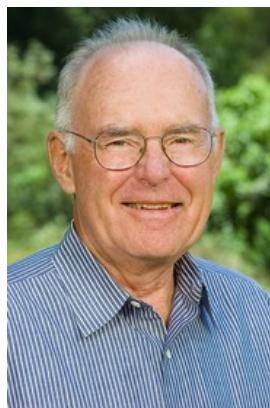
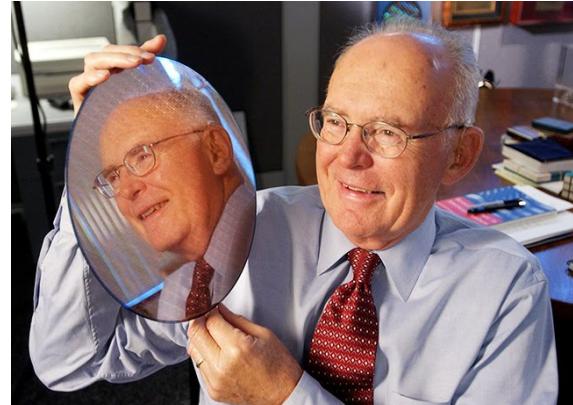
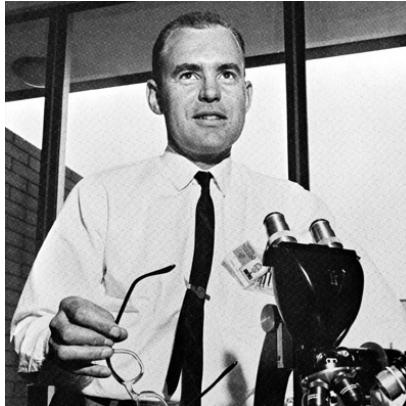


More Moore & More Than Moore





More Moore





More than Moore





IC Process

How to Fabricate IC ?

- Circuit design
- Photo mask fabrication
- Oxidation or thin-film deposition
- Coating photo-resist (PR)
- Mask alignment
- Expose
- Develop
- Etching
- PR remove

How to fabricate Souvenir ?

- Pattern design
- Print on transparency film
- Deposit 140 nm SiO_2
- Coating photo-resist (PR)
- Put slide on wafer
- Expose
- Develop
- Diluted HF etching
- PR remove



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National Chiao-Tung University
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The Lowest Price Photo Mask



A WISH
FOR YOUR BIRTHDAY



How complex of a VLSI is ?

➤ Thin film process

- Physical vapor deposition, chemical vapor deposition, electrochemical deposition, atomic layer deposition, chemical-mechanical polish, etc.
- SiO_2 , Si_3N_4 , SiON, Hf-based dielectrics, PSG, BPSG, FSG, Si, Al, Ti, Co, TiN, TaN, Cu, etc.

➤ Lithography process

- Photo-resist, light source, optical system, resolution enhancement technologies

➤ Etching process

- Wet etching: H_2SO_4 , HCl , HNO_3 , HF, H_3PO_4 , NH_4OH , H_2O_2 , etc.
- Dry etching: Ar, O_2 , H_2 , N_2 , Cl_2 , HCl , HBr , SF_6 , CF_4 , C_2F_6 , CHF_3 , C_4F_8 , etc.

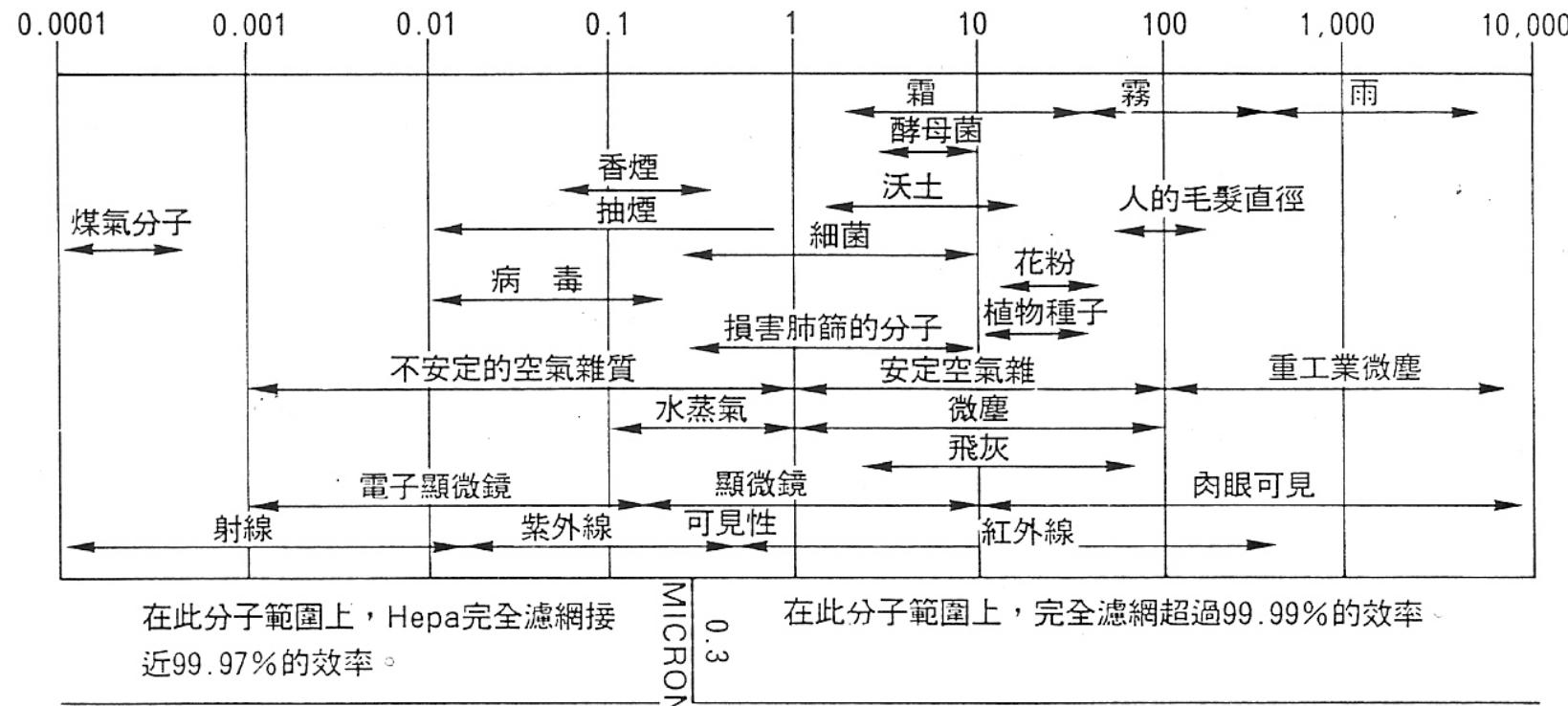
➤ Oxidation/Diffusion process

- Thermal oxidation, solid-phase diffusion, ion Implantation, rapid-thermal annealing, spike annealing, flash annealing, etc.

➤ Other novel processes



Small Objects



這代表1個10微公尺直徑的分子，是肉眼所見的最小尺寸。

- 這代表1個0.3微公尺直徑的分子，Hepa
• 完全濾網可以超過99.99%的效率除去這種大小的分子。

這個距離代表人類毛髮的直徑，100MICRONS

1 MICRON = 1 MICROMETER = 1 MILLIONTH OF A METER



Cleanroom Spec.

American Fed. 209D

潔淨室級數 (Class)	微塵粒子		壓力 mmAg	溫度					風速與換氣率 (次/hr)	照度lux	
	粒子大小 um	粒子數目 Particles/ft ³		值域°C	推 值°C	誤差 值°C	最大 MAX%	最小 MIN%			
1	0.5	1	>1.3	19.4~25	22.2	±2.8 特 殊 需 求	45	30	±10 特 殊 需 求	層流方式 0.35~0.55 m/s	1080 ~ 1620
	5.0	0									
10	0.5	10	>1.3	19.4~25	22.2	±1.4	45	30	±5	亂流方式 20 次/hr	1080 ~ 1620
	5.0	0									
100	0.5	100	>1.3	19.4~25	22.2	±1.4	45	30	±5	亂流方式 20 次/hr	1080 ~ 1620
	5.0	1									
1000	0.5	1000	>1.3	19.4~25	22.2	±1.4	45	30	±5	亂流方式 20 次/hr	1080 ~ 1620
	5.0	10									
10000	0.5	10000	>1.3	19.4~25	22.2	±1.4	45	30	±5	亂流方式 20 次/hr	1080 ~ 1620
	5.0	65									
100000	0.5	100000	>1.3	19.4~25	22.2	±1.4	45	30	±5	亂流方式 20 次/hr	1080 ~ 1620
	5.0	700									



Particle Spec.

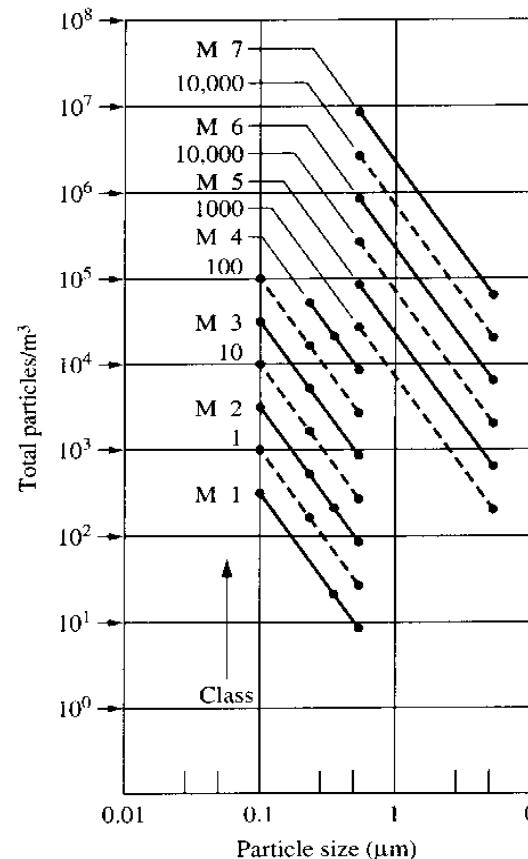
American Fed. 209E

Particles/m³

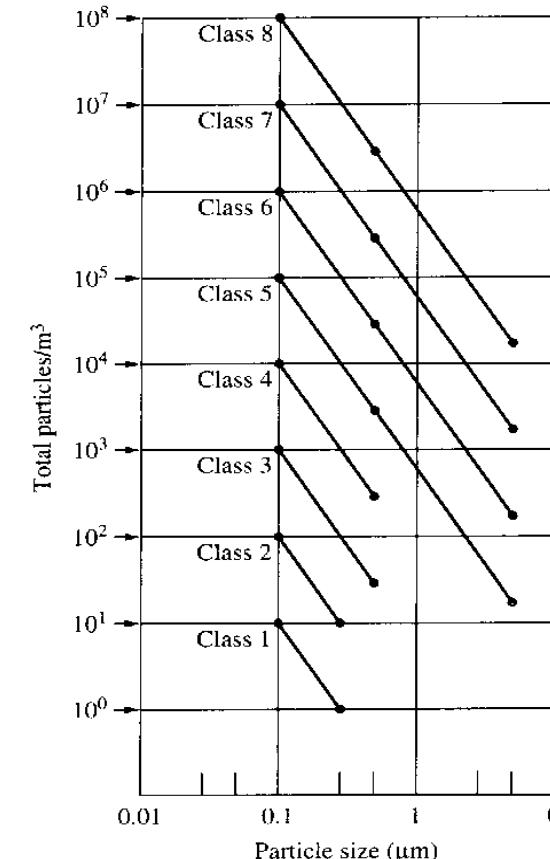
Class	0.1 μm	0.2 μm	0.3 μm	0.5 μm	5 μm
M1	3.50×10^2	7.57×10^1	3.09×10^1	1.00×10^1	
M1.5	1.24×10^3	2.65×10^2	1.06×10^2	3.53×10^1	
M2	3.50×10^3	7.57×10^2	3.09×10^2	1.00×10^2	
M2.5	1.24×10^4	2.65×10^3	1.06×10^3	3.53×10^2	
M3	3.50×10^4	7.57×10^3	3.09×10^3	1.00×10^3	
M3.5		2.65×10^4	1.06×10^4	3.53×10^3	
M4		7.57×10^4	3.09×10^4	1.00×10^4	
M4.5				3.53×10^4	2.47×10^2
M5				1.00×10^5	6.18×10^2
M5.5				3.53×10^5	2.47×10^3
M6				1.00×10^6	6.18×10^3
M6.5				3.53×10^6	2.47×10^4
M7				1.00×10^7	6.18×10^4



Particle Spec.



USA Spec.



Japan Spec.

- Class M2.5 (at $0.3\mu\text{m}$) : air with no more than $1060 \text{ particles}/\text{m}^3$ with a particle size of $0.3\mu\text{m}$ and larger.
- Class 100 (at $0.5\mu\text{m}$) : air with no more than $100 \text{ particles}/\text{ft}^3$ with a particle size of $0.5\mu\text{m}$ and larger



Example of Cleanroom Spec.

		ILLUMINATION LUX	DEGREE °C	RH %	CLEANLINESS		CEILING HEIGHT	REMARKS		
					PARTICLE @	μm				
PHOTO AREA		500	23±0.3	43±3	1	0.1	3.5M	NOISE LEVEL: NC<60		
PRODUCTION AREA		800	23±0.5	43±5						
MAIN AISLE		350	23±2	53-37						
SERVICE AREA					100	0.3				
MAIN GOWN ROOM	AIR SHOWER	350	26↓	-----	1	0.1	2.8M	NOISE LEVEL: -----		
	AIR LOCK				100					
	GOWNING AREA		23±2	53-37	100	0.1				
	SHOES EXCHANGE									
	SUPERVISOR ROOM	700	-----	-----	10000	0.3				
EQ MOVE IN ROUTE		350	23±2	53-37	1000	0.3	3.5M			
T.C.R.	PRODUCTION AREA				100	0.3	3.0M	NOISE LEVEL: NC<60		
	SERVICE AREA				10000					



Cleanroom Design

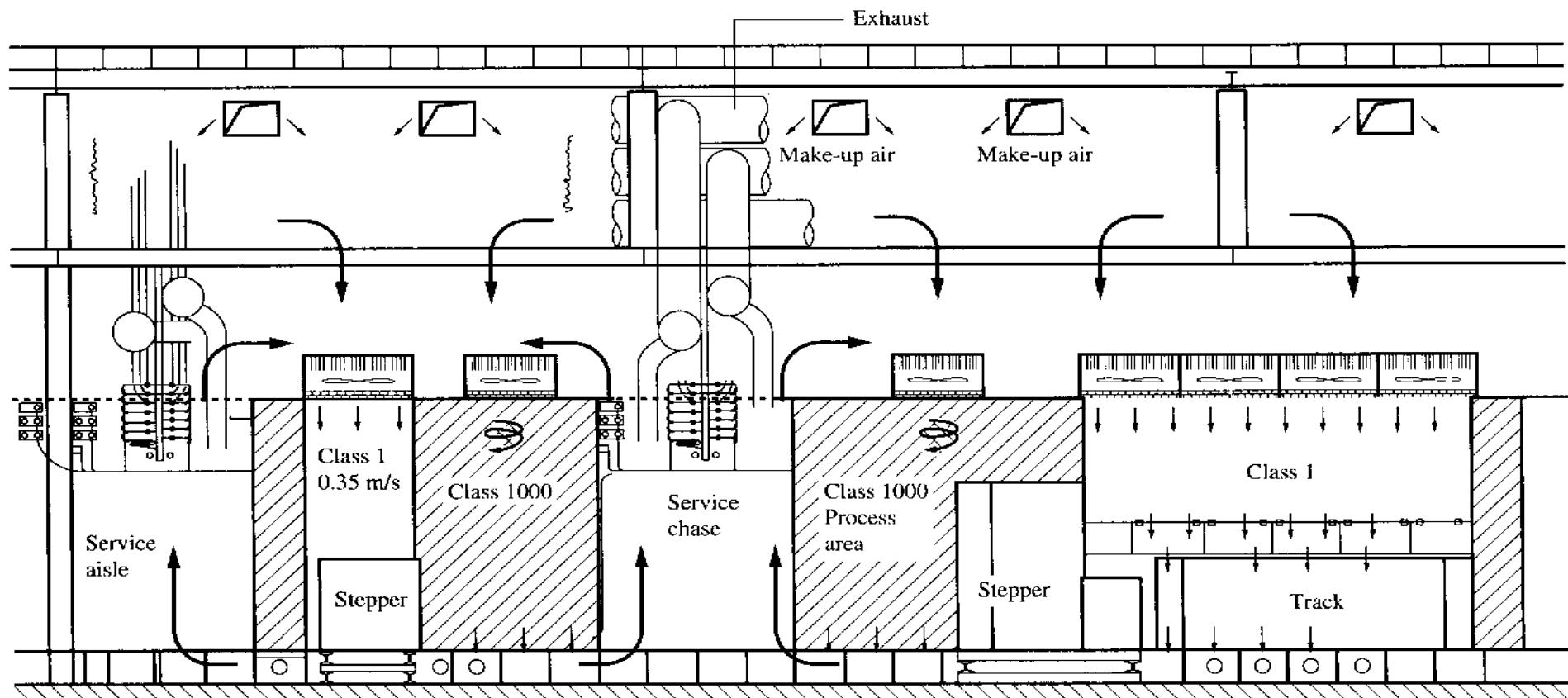


FIGURE 6

Ballroom-type cleanroom with process and service areas located on the same floor.



Cleanroom Design

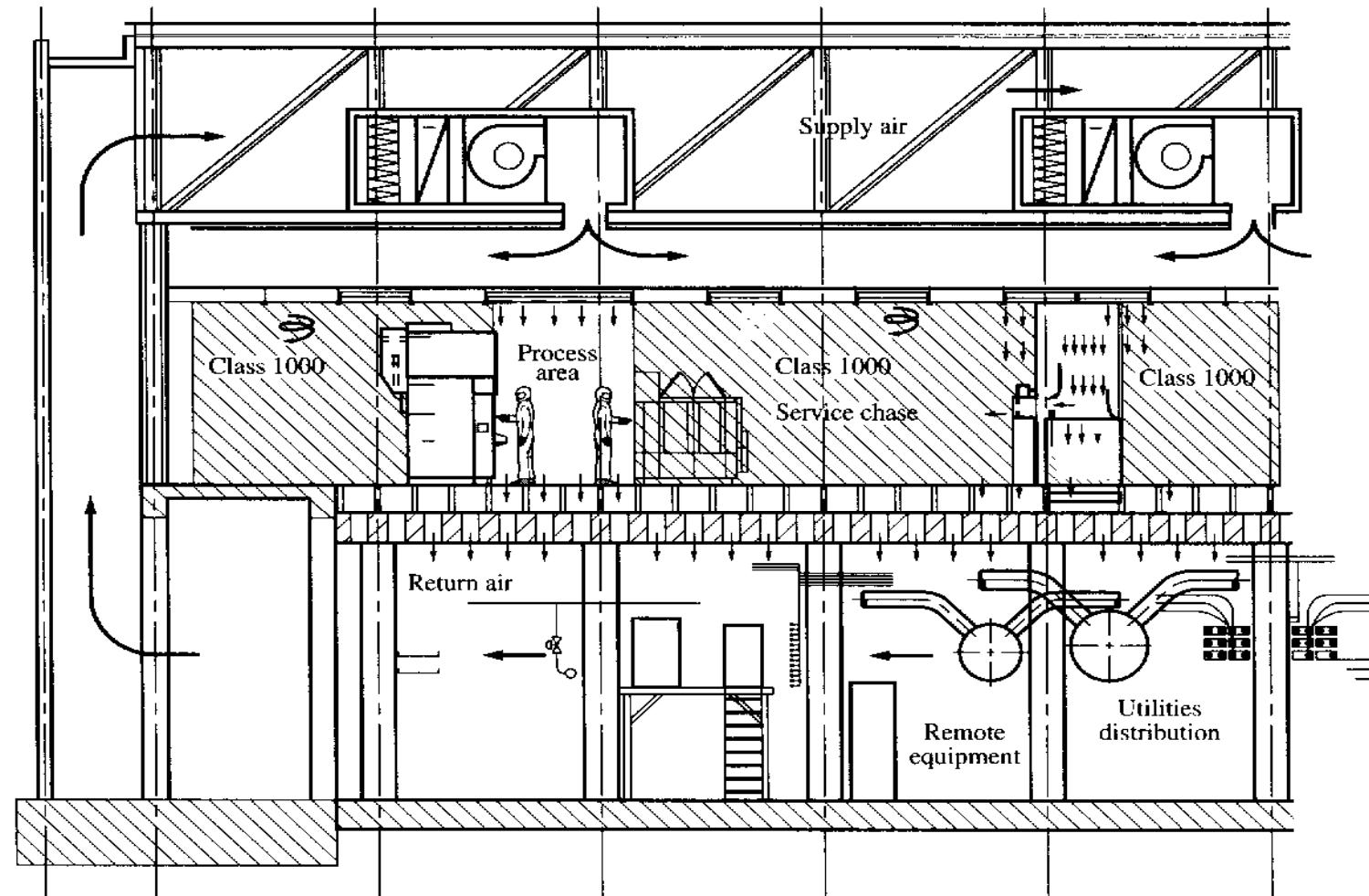


FIGURE 7

Cleanroom with centrifugal fan units installed on top of process level.



Cleanroom Design

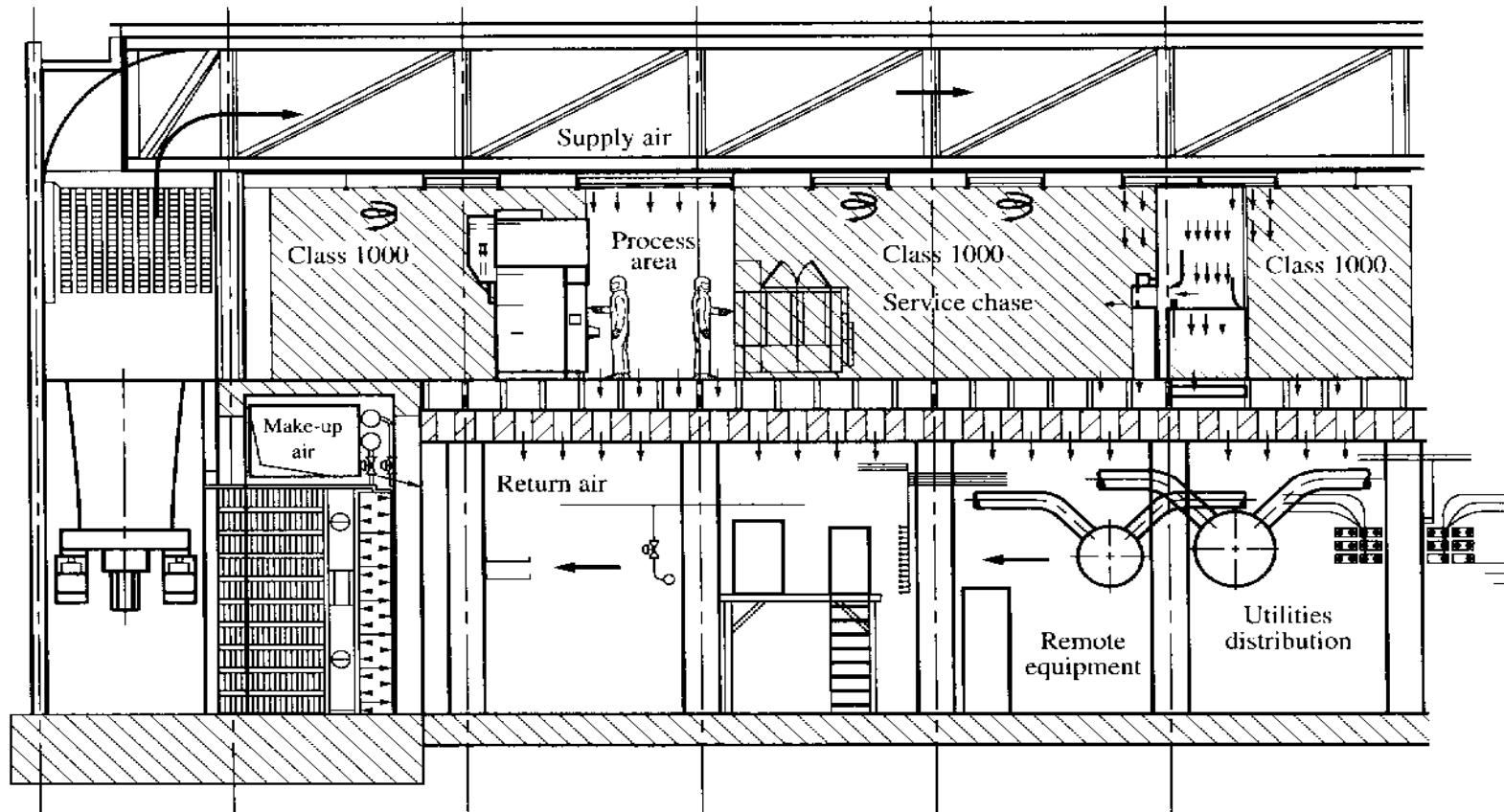


FIGURE 8

Cleanroom with axial fan units installed sideways connecting the air-supply plenum at the top and the air-return plenum at the bottom.



Cleanroom Design

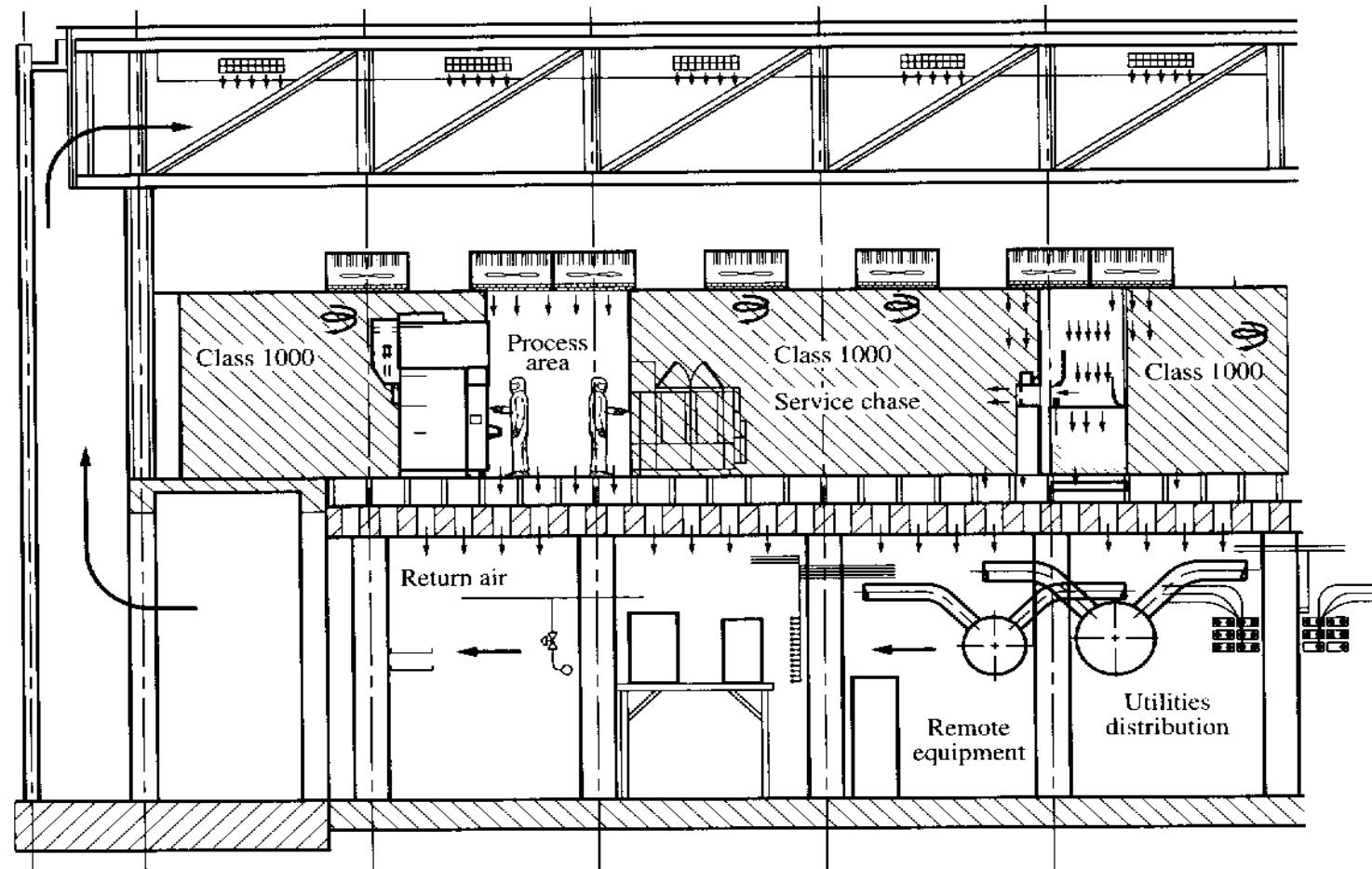


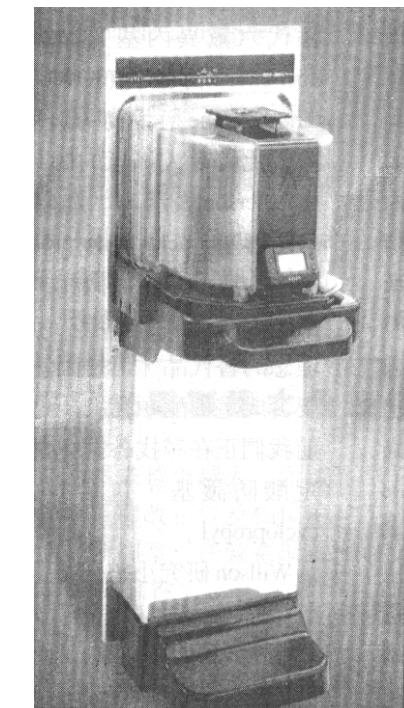
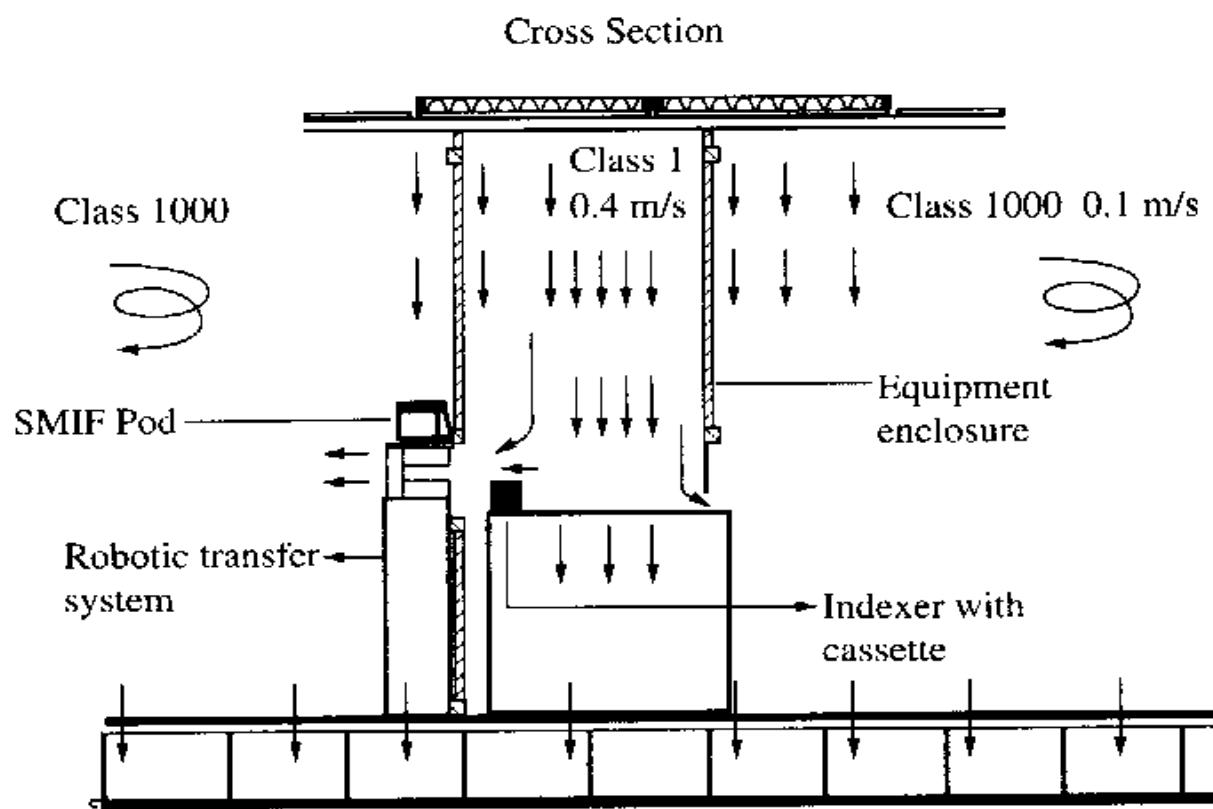
FIGURE 9

Cleanroom with filter fan units installed on the top of process area.



Cleanroom Design

- Mini-environment
- SMIF: Standard Mechanical InterFaces
- FOUP: Front Opening Unified Pod





A Glance on Cleanroom

