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1896

# Thermal Oxidation



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  - Ultra-thin  $\text{SiO}_2$
  - High dielectric constant (high-k) dielectrics
- Metrology



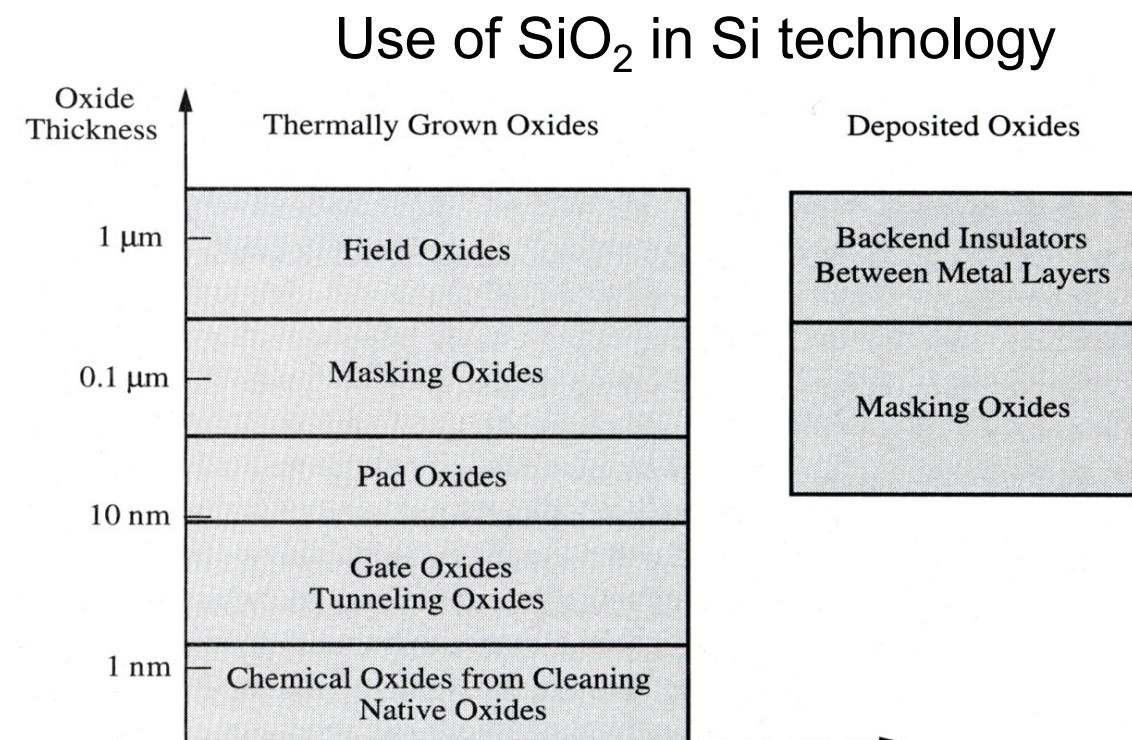
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# Oxidation Technology



# Silicon Dioxide

- $\text{SiO}_2$ , a stable oxide compound.
- Major factors that enabled the success of IC manufacturing.
  - 1950s, oxide masking and planar processes.
  - 1960, gate oxide for MOSFET.
  - Device and interconnect isolations.
  - Other applications.
- Formed by either growth (oxidation) or deposition methods.





# Deposited Oxide vs. Grown Oxide



Grown film



Bare silicon



Deposited film

## Thermal oxidation

- Oxygen is from gas phase
- Silicon from substrate
- Oxide grows into silicon
- Higher quality

## Chemical Vapor Deposition

- Both oxygen and silicon are from gas phase
- Deposit on substrate surface
- Higher growth rate at a lower temperature



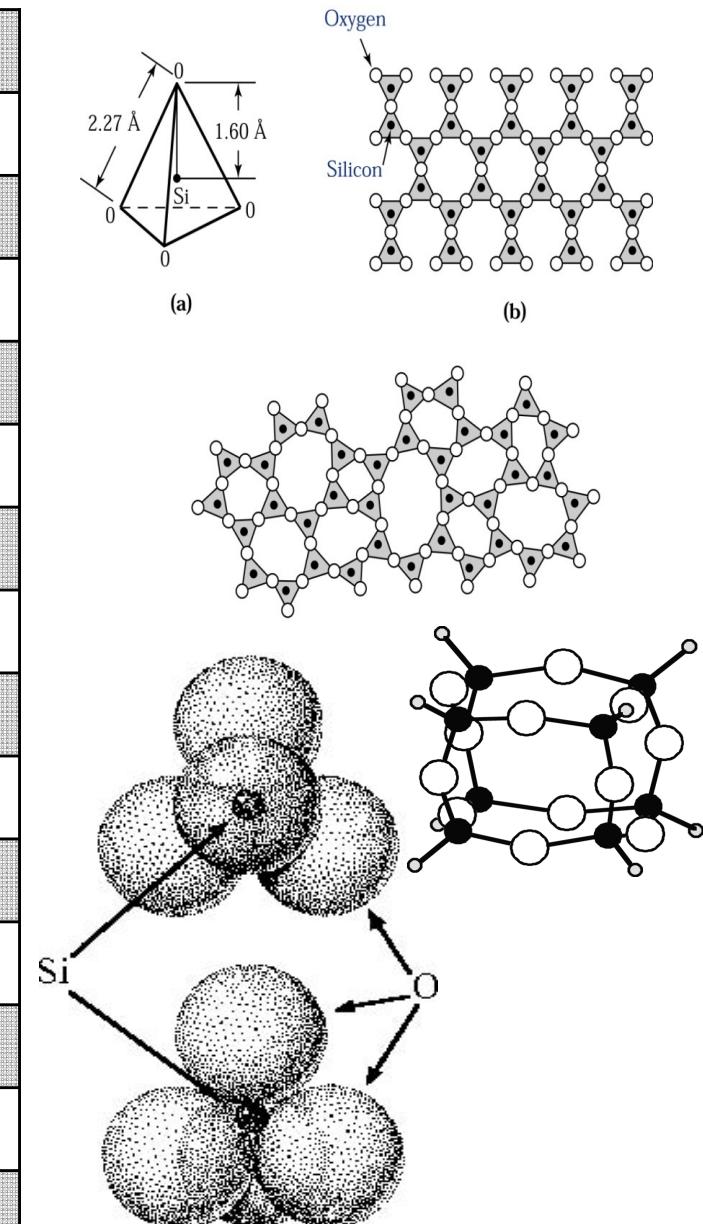
# Characteristics of SiO<sub>2</sub>

- Amorphous material
- Easy to grow on Si
- Easy to integrate in process
- Stable and insensitive to following process steps
- Water in-soluble
- Excellent insulator (bandgap = 9 eV)
- Extremely low interface-state density at SiO<sub>2</sub>/Si interface  
(typically  $< 10^{11} \text{ cm}^{-2}$ )
- Excellent scaling feasibility



# Properties of Thermal Oxide at RT

Melting point	~1600 °C
Density	2.26 g/cm <sup>3</sup>
Molecular density	2.2x10 <sup>22</sup> cm <sup>-3</sup>
Young's modulus	10 <sup>7</sup> psi
Refractive index	1.46
Dielectric constant	3.9
Average length of Si-O bond	~1.6 Å
Thermal expansion coefficient	5x10 <sup>-7</sup> °C <sup>-1</sup>
Thermal conductivity	0.014 W/cm-K
Specific heat	1 J/g-°C
DC resistivity	10 <sup>14</sup> ~10 <sup>16</sup> Ω-cm
Dielectric strength	10 <sup>7</sup> V/cm
Energy gap	~9 eV
ΔE <sub>c</sub> at SiO <sub>2</sub> /Si interface	3.2 eV
ΔE <sub>v</sub> at SiO <sub>2</sub> /Si interface	4.7 eV





# Thermal Oxidation

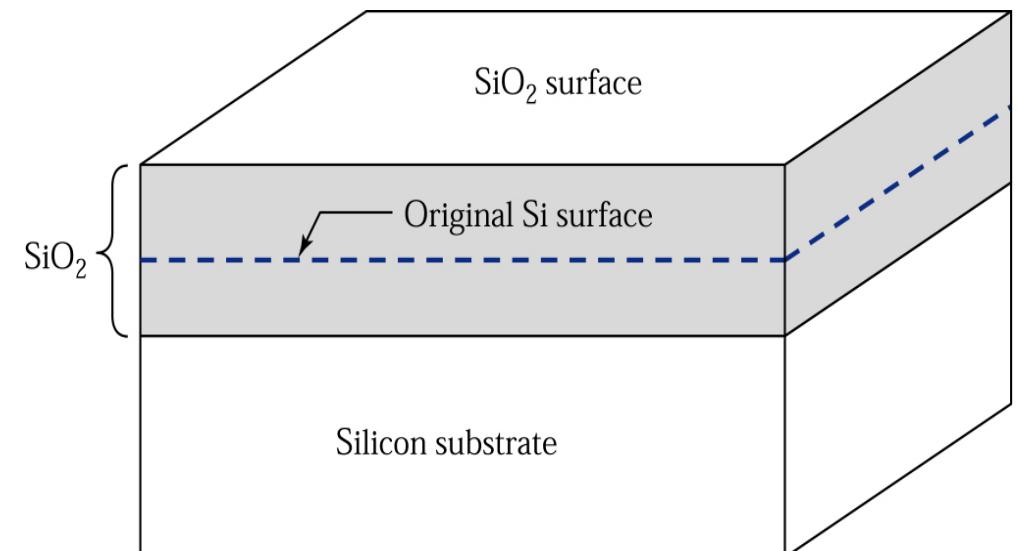
## ➤ Dry Oxidation

- $\text{Si (s)} + \text{O}_2 (\text{g}) \rightarrow \text{SiO}_2 (\text{s})$

## ➤ Wet Oxidation

- $2\text{H}_2 (\text{g}) + \text{O}_2 (\text{g}) \rightarrow \text{H}_2\text{O} (\text{g})$
- $\text{Si (s)} + \text{H}_2\text{O} (\text{g}) \rightarrow \text{SiO}_2 (\text{s}) + 2\text{H}_2 (\text{g})$

$0.44x_o \text{ Si to } 1x_o \text{ SiO}_2$





# Deal-Grove Model-1

- Oxidants must be transported from the bulk of the gas to the oxide surface.

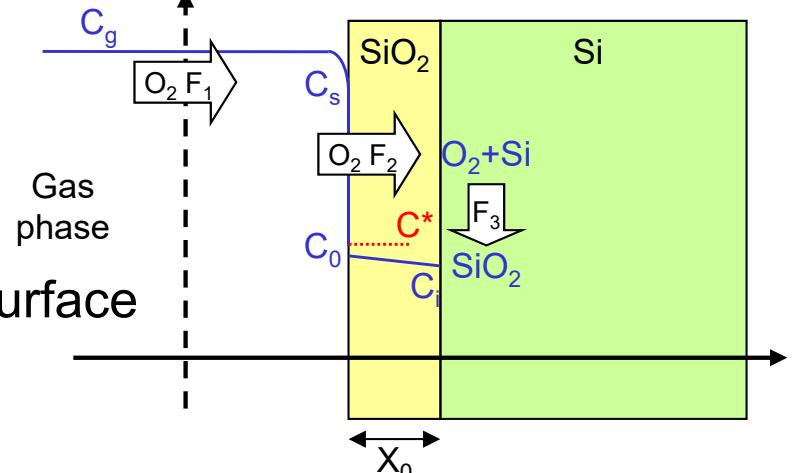
$$F_1 = h_g (C_g - C_s)$$

- $C_g$  : oxidant concentration in bulk of gas
- $C_s$  : oxidant concentration right next to the oxide surface
- $h_g$  : gas phase mass-transfer coefficient

- Henry's law

- In equilibrium, the concentration of a species within a solid is proportional to the partial pressure of that species in the surrounding gas.
- $C^* = H p_g$  (equilibrium concentration in bulk  $\text{SiO}_2$ )
- $C_o = H p_s$  (equilibrium concentration at bulk gas/ $\text{SiO}_2$  interface)
- For ideal gas  $C = p/kT$

$$\Rightarrow F_1 = h(C^* - C_o), \text{ where } h = h_g / H k T$$





# Deal-Grove Model-2

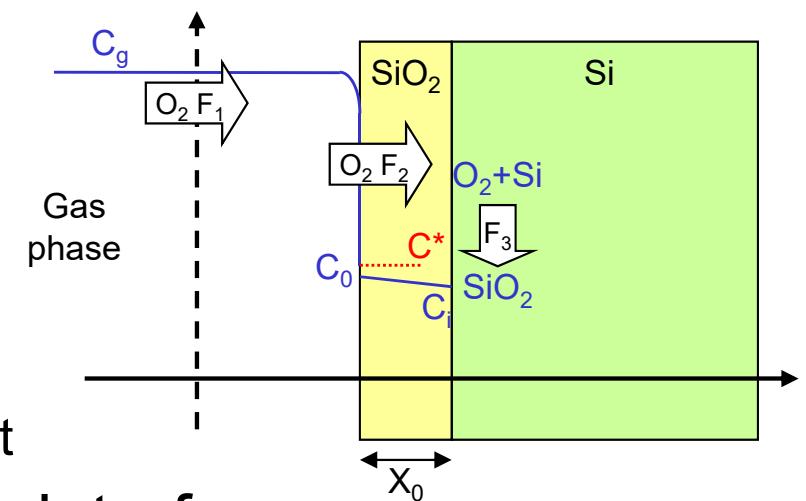
- Oxidants must diffuse across the oxide layer already present.

$$F_2 = D \frac{C_o - C_i}{x_o}$$

- D is the diffusivity of oxidant in bulk oxide
- $C_i$  is the oxidant concentration in bulk oxide at the oxide/silicon interface
- $x_o$  is the thickness of oxide layer already present

- Oxidants must react at the oxide/silicon interface

- $F_3 = k_s C_i$   
 $k_s$  is the chemical surface-reaction rate constant





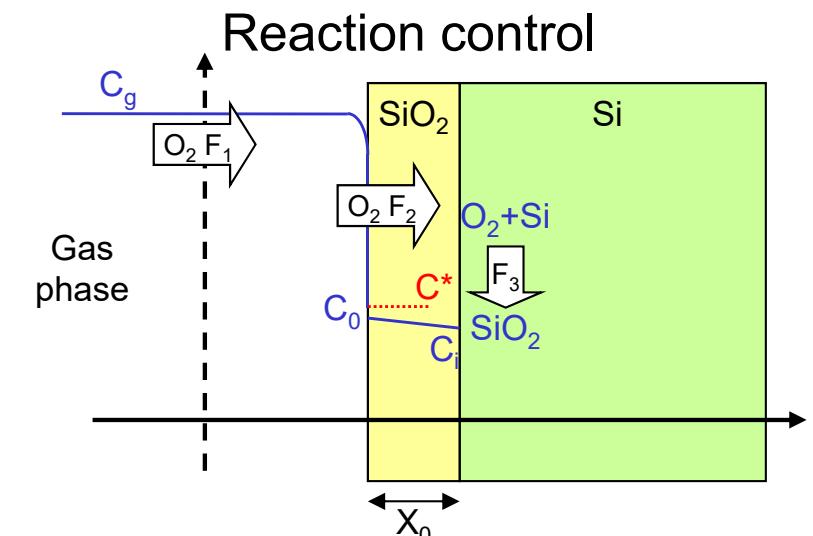
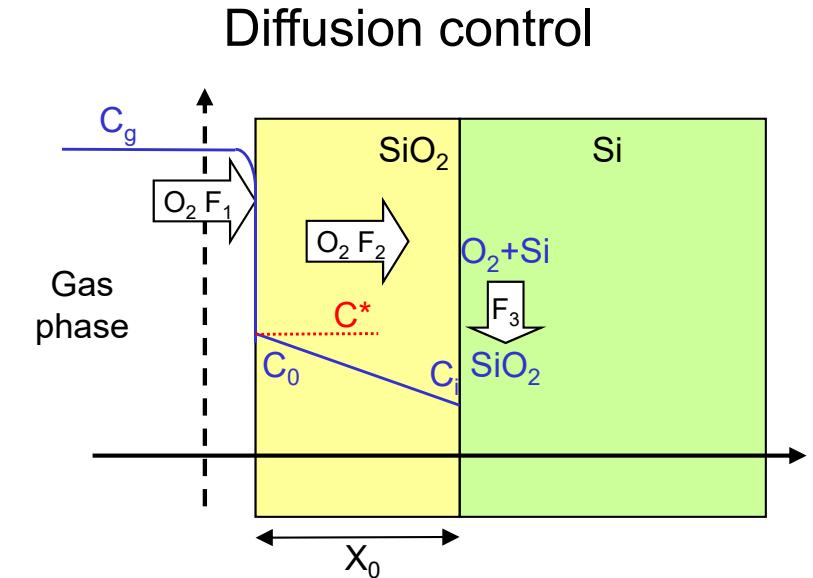
# Deal-Grove Model-3

➤ Steady state :  $F=F_1=F_2=F_3$

$$C_i = \frac{C^*}{1 + \frac{k_s}{h} + \frac{k_s x_o}{D}} \text{ and } C_o = \frac{\left(1 + \frac{k_s x_o}{D}\right) C^*}{1 + \frac{k_s}{h} + \frac{k_s x_o}{D}}$$

As  $D \rightarrow 0 \Rightarrow C_i \rightarrow 0$  and  $C_o \rightarrow C^*$

$$\text{As } k_s \rightarrow 0 \Rightarrow C_i = C_o \rightarrow \frac{C^*}{1 + \frac{k_s}{h}}$$





# Deal-Grove Model-4

➤ N : The number of oxidant molecules incorporated into a unit volume of oxide.

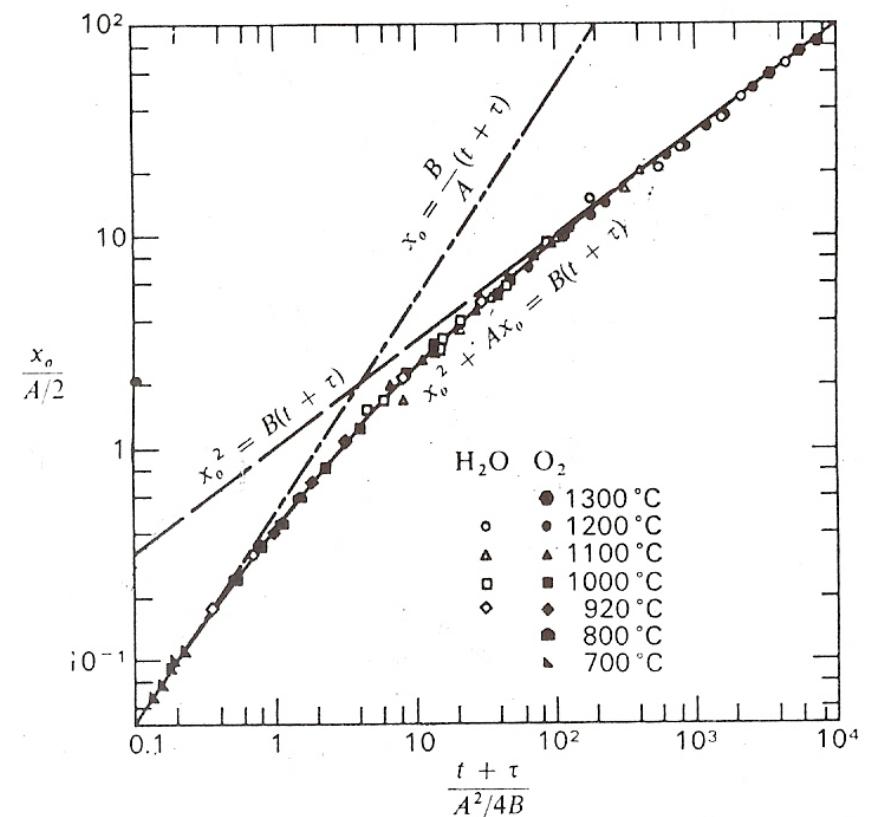
- O<sub>2</sub> oxidation : N=2.2x10<sup>22</sup> molecules/cm<sup>3</sup>
- H<sub>2</sub>O oxidation : N=4.4x10<sup>22</sup> molecules/cm<sup>3</sup>

$$N \frac{dx_o}{dt} = F = \frac{k_s C^*}{1 + \frac{k_s}{h} + \frac{k_s x_o}{D}} \Rightarrow \frac{dx_o}{dt} = \frac{B}{2x_o + A},$$

$$\text{where } A \equiv 2D \left( \frac{1}{k_s} + \frac{1}{h} \right) \text{ and } B \equiv \frac{2DC^*}{N}$$

$$\text{Initial condition } x_o(0) = x_i \Rightarrow x_o^2 + Ax_o = B(t + \tau),$$

$$\text{where } \tau \equiv \frac{x_i^2 + Ax_i}{B}$$





# Deal-Grove Model-5

From  $x_o^2 + Ax_o = B(t + \tau)$

$$\Rightarrow \frac{x_o}{A/2} = \sqrt{1 + \frac{t + \tau}{A^2/4B}} - 1$$

As  $t \gg A^2/4B$ , i.e. diffusion control

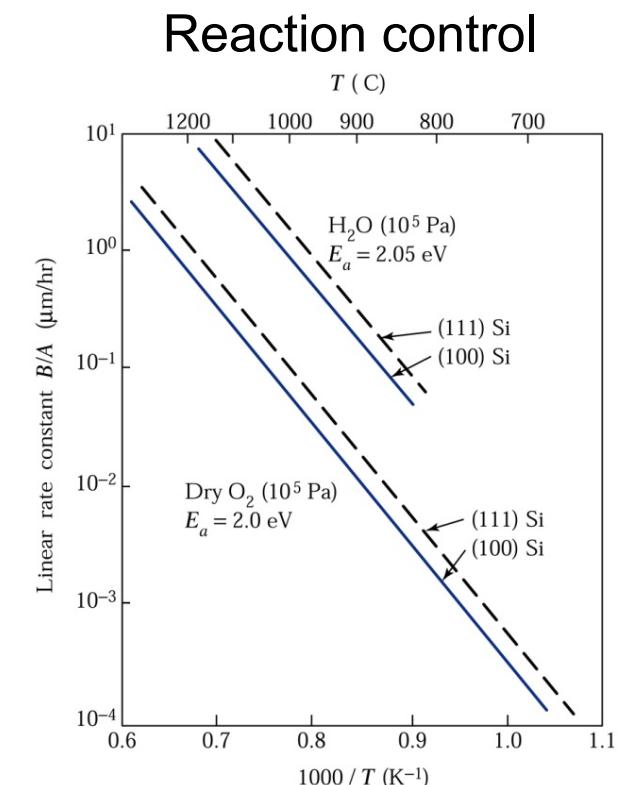
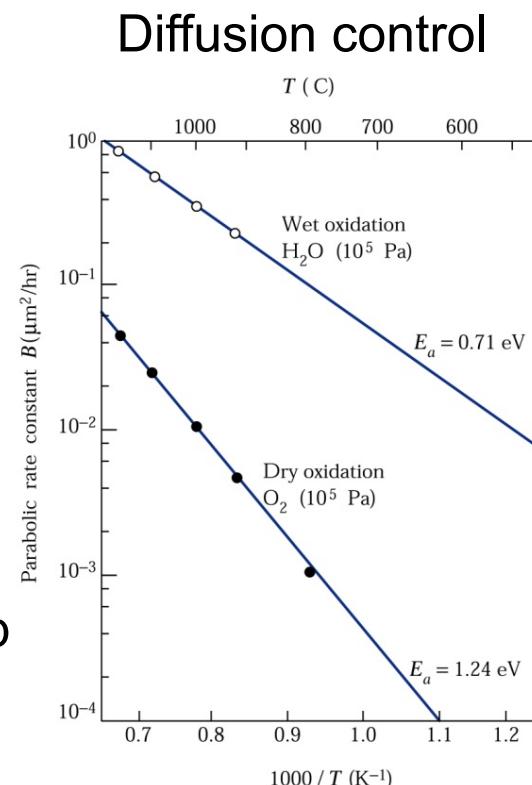
$\Rightarrow x_o^2 = Bt$  is called parabolic relationship

$B$  is the parabolic rate constant

As  $(t + \tau) \ll A^2/4B$ , i.e. reaction control

$\Rightarrow x_o = \frac{B}{A}(t + \tau)$  is called linear relationship

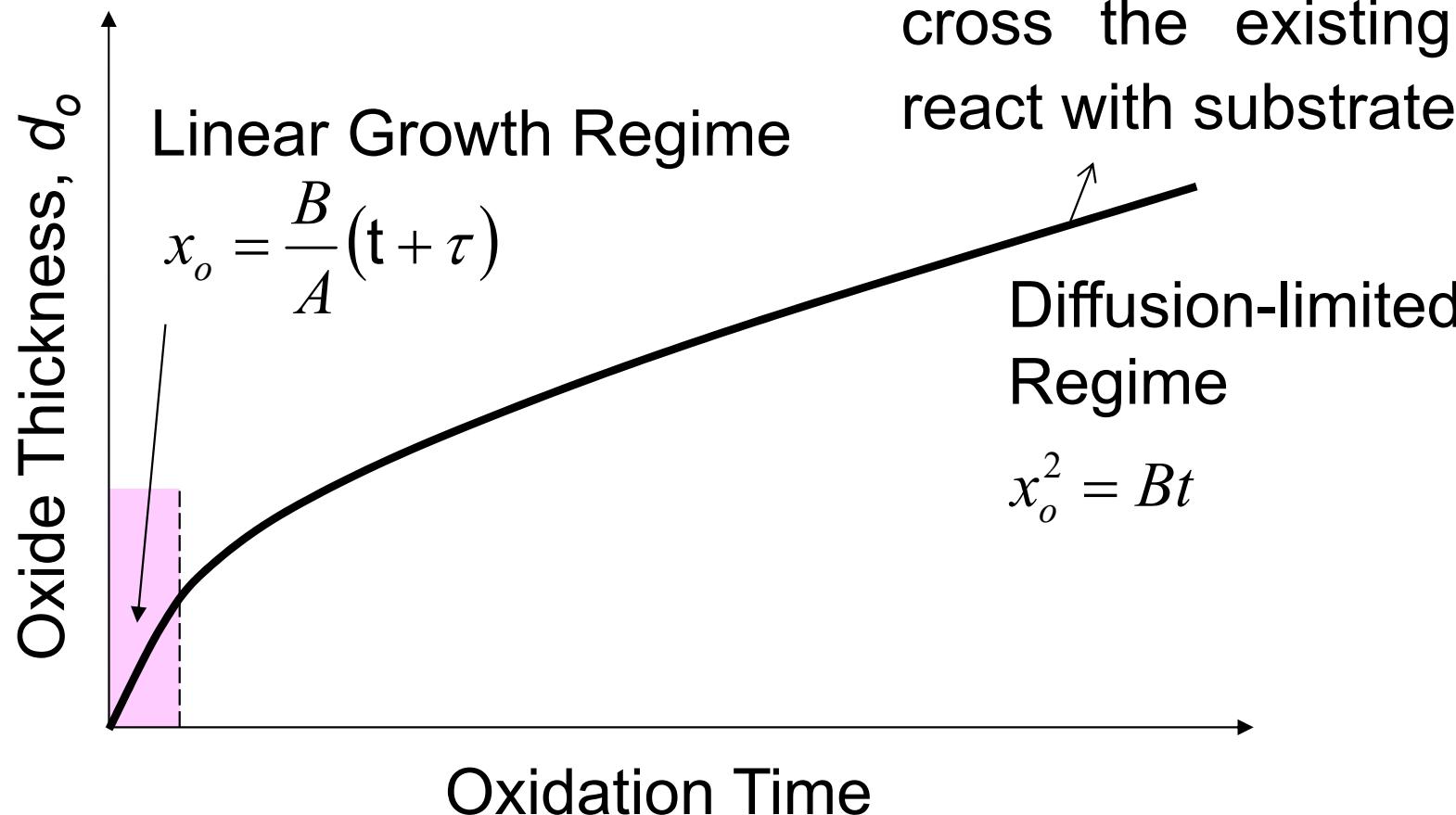
$\frac{B}{A} = \frac{k_s h}{k_s + h} \frac{C^*}{N}$  is the linear rate constant





# Oxide Growth Rate Regime

- The thicker of the oxide film is, the slower the oxidation rate is.
- Oxygen needs more time to diffuse cross the existing oxide layer to react with substrate silicon.





# Initial Fast Oxidation

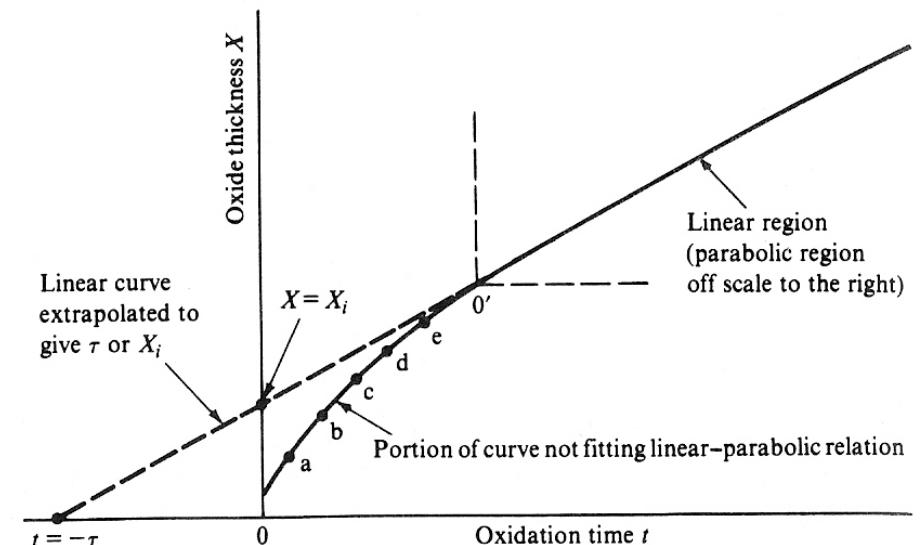
➤ Massoud's experimental model:

$$\frac{dx_o}{dt} = \frac{B}{2x_o + A} + C \exp\left(-\frac{x_o}{L}\right)$$

$$C = C_o \exp\left(-\frac{E_A}{kT}\right)$$

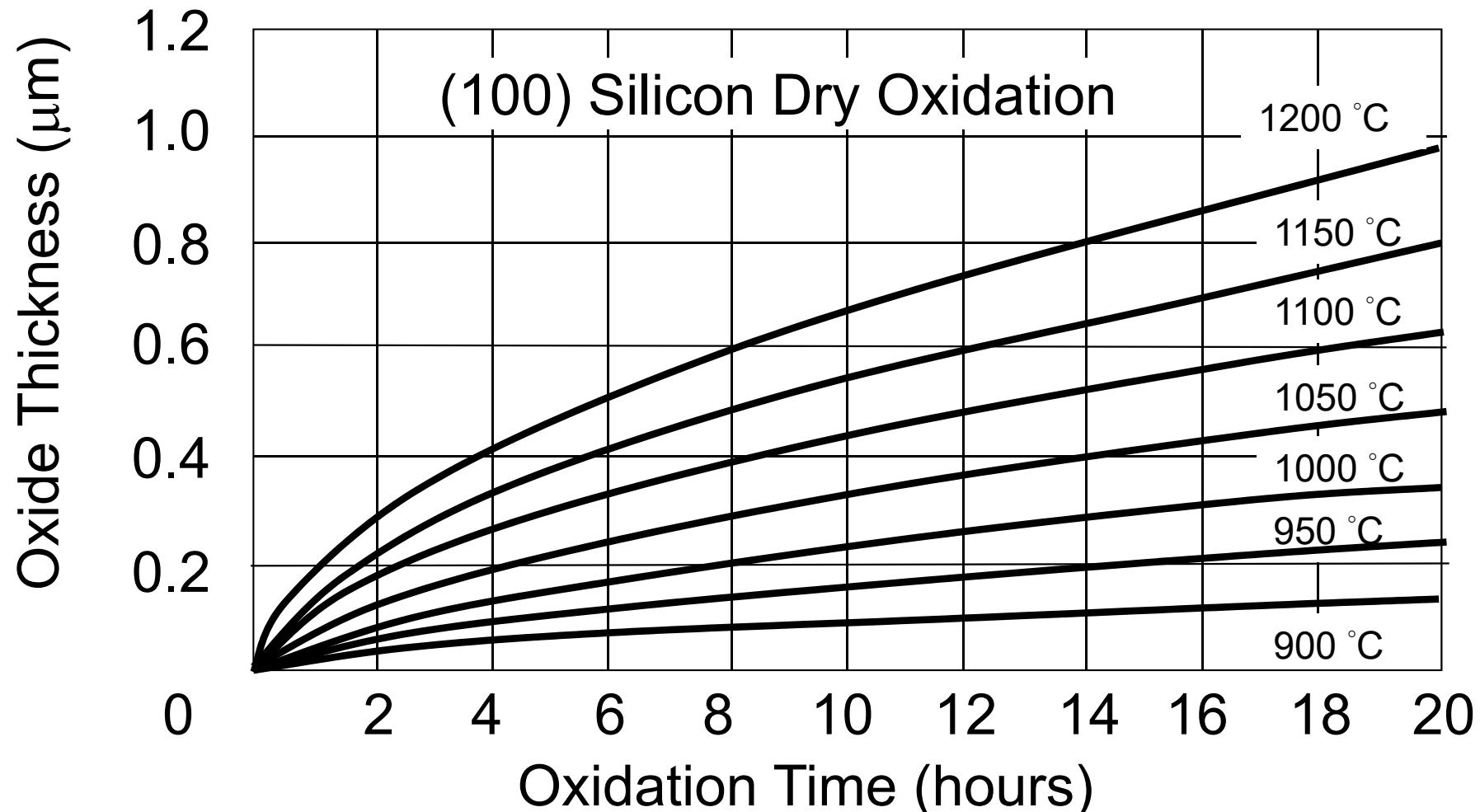
$$C_o \approx 3.6 \times 10^8 \mu\text{m/hr}, E_A \approx 2.35 \text{eV}, \text{and } L \approx 7 \text{nm}$$

- Apply to either (111) or (100) oriented Si.
- The first term is the Deal-Grove Model.
- The second term represents an additional oxidation mechanism.
- The actual mechanism is still not clear.





# (100) Silicon Dry Oxidation



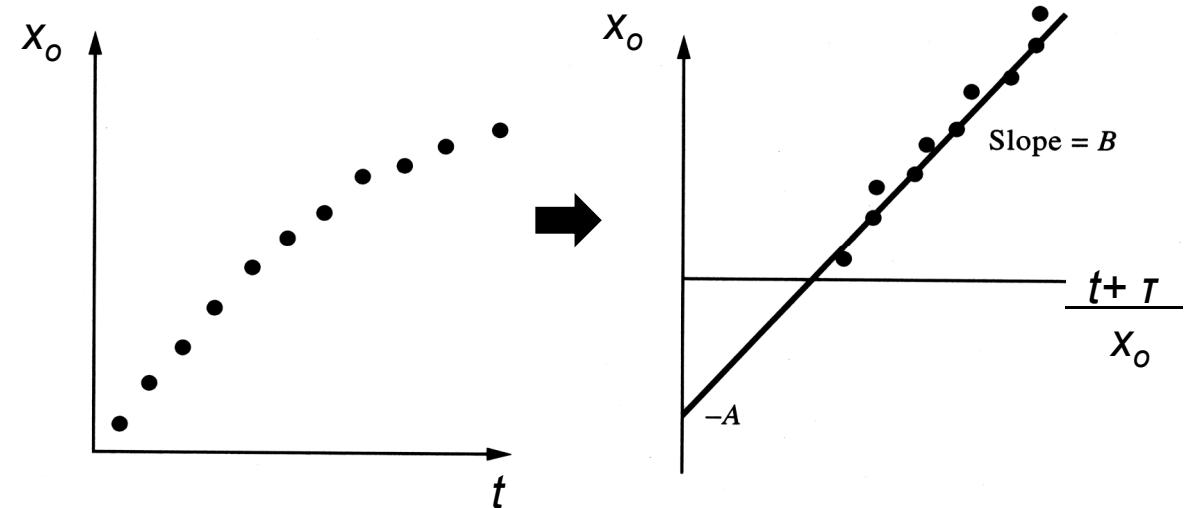


# Extraction of Rate Constants

Deal-Grove Relation:

$$x_o^2 + Ax_o = B(t + \tau)$$

$$\Rightarrow x_o = \frac{B}{x_o} (t + \tau) - A$$



- For oxidation performed on flat (unpatterned) surfaces, on lightly doped substrates, in simple O<sub>2</sub> or H<sub>2</sub>O ambient and when x<sub>o</sub> is thicker than about 20 nm, the experimentally extracted rate constants are well described by Arrhenius expression of the form:

$$B = C_1 \exp(-E_1 / kT)$$

$$\frac{B}{A} = C_2 \exp(-E_2 / kT)$$

C<sub>1</sub>, C<sub>2</sub>: constants

E<sub>1</sub>, E<sub>2</sub>: activation energies

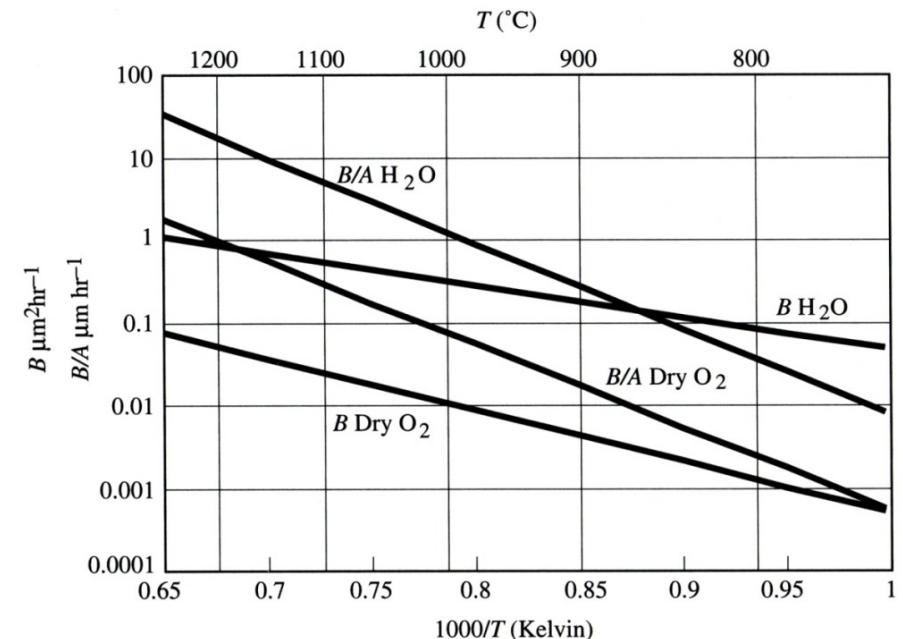


# Physical Mechanisms

**Table 6-2** Rate constants describing (111) silicon oxidation kinetics at 1 Atm total pressure. For the corresponding values for (100) silicon, all  $C_2$  values should be divided by 1.68.

Ambient	B	B/A
Dry O <sub>2</sub>	$C_1 = 7.72 \times 10^2 \mu\text{m}^2 \text{hr}^{-1}$ $E_1 = 1.23 \text{ eV}$	$C_2 = 6.23 \times 10^6 \mu\text{m hr}^{-1}$ $E_2 = 2.0 \text{ eV}$
Wet O <sub>2</sub>	$C_1 = 2.14 \times 10^2 \mu\text{m}^2 \text{hr}^{-1}$ $E_1 = 0.71 \text{ eV}$	$C_2 = 8.95 \times 10^7 \mu\text{m hr}^{-1}$ $E_2 = 2.05 \text{ eV}$
H <sub>2</sub> O	$C_1 = 3.86 \times 10^2 \mu\text{m}^2 \text{hr}^{-1}$ $E_1 = 0.78 \text{ eV}$	$C_2 = 1.63 \times 10^8 \mu\text{m hr}^{-1}$ $E_2 = 2.05 \text{ eV}$

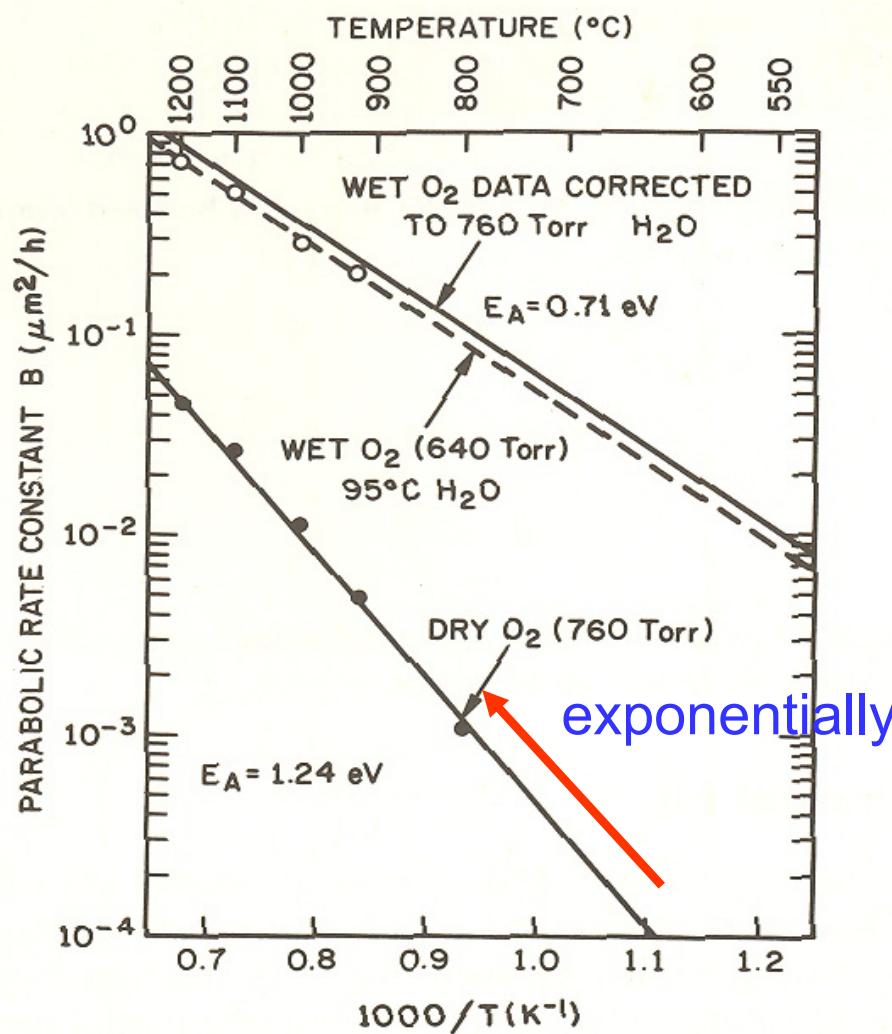
Wet O<sub>2</sub>: Mixture of O<sub>2</sub> and H<sub>2</sub>O



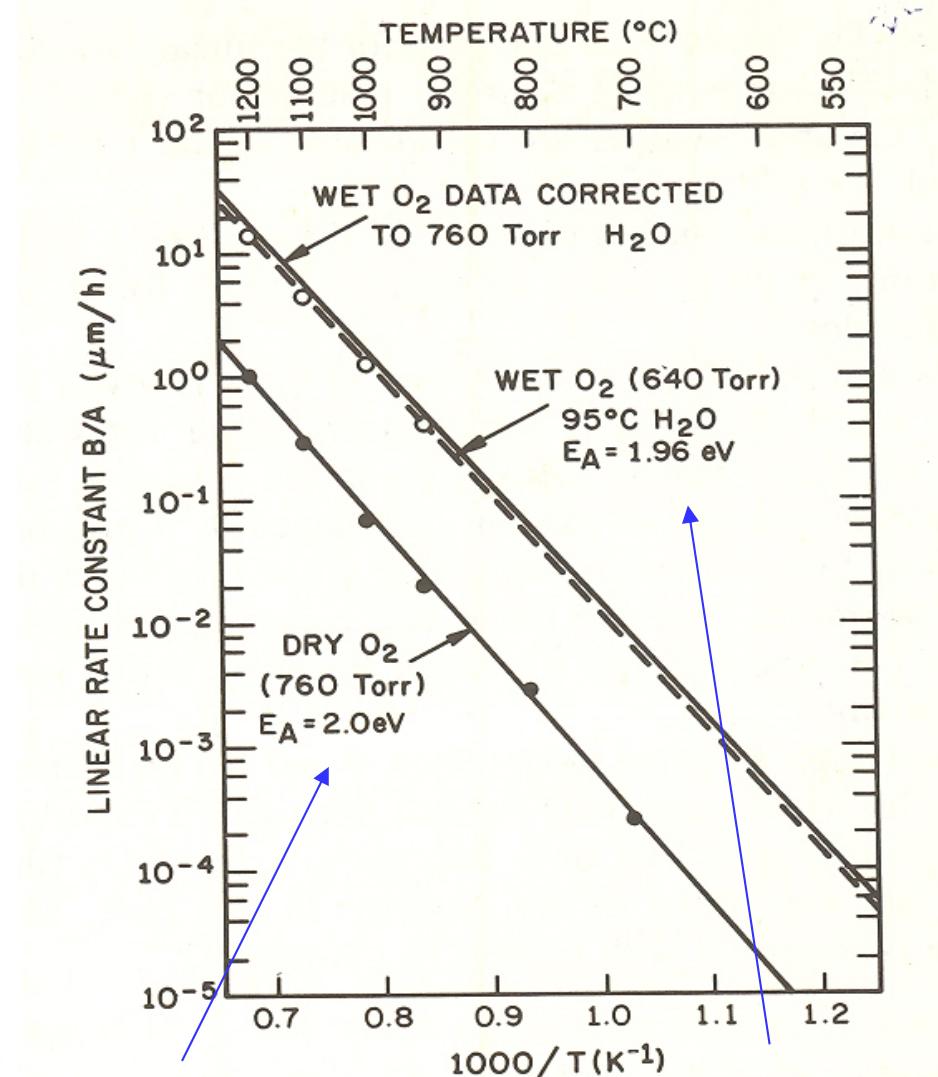
- $E_1$  is quite different for O<sub>2</sub> and H<sub>2</sub>O ambients, suggesting that it might be related to the oxidant diffusion through the SiO<sub>2</sub>.
- $E_2$  of all splits are quite close to 2eV, suggesting its physical origin is likely connected with the interface reaction rate constant  $k_s$ . Traditionally, it has been associated with the Si-Si bond breaking process, but other processes like oxidant dissociation (O<sub>2</sub> → 2O) and SiO bond formation may also affect the experimental B/A values.



# Deal and Grove's Data on (111) Si



(VLSI Technology, S.M. Sze)

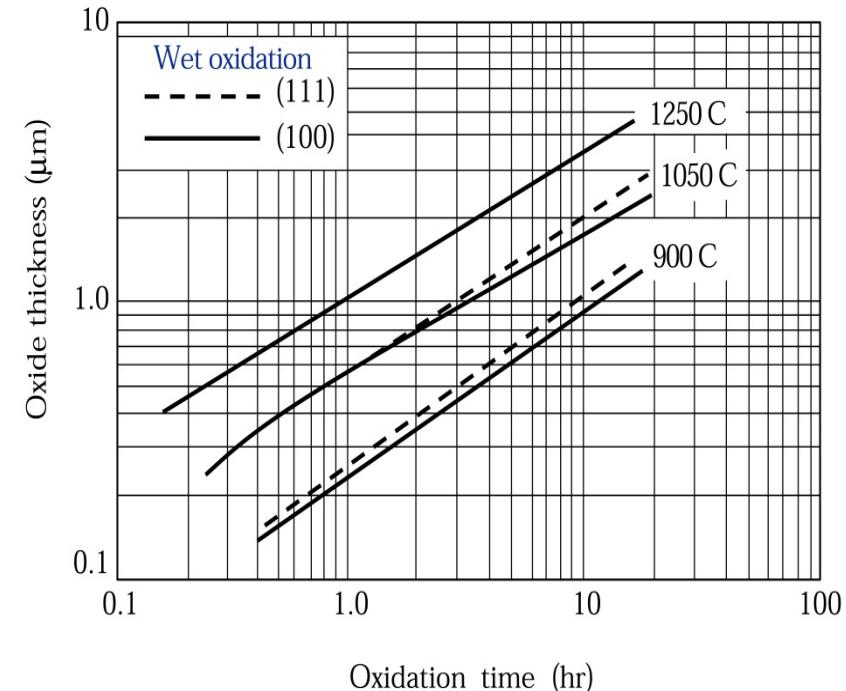
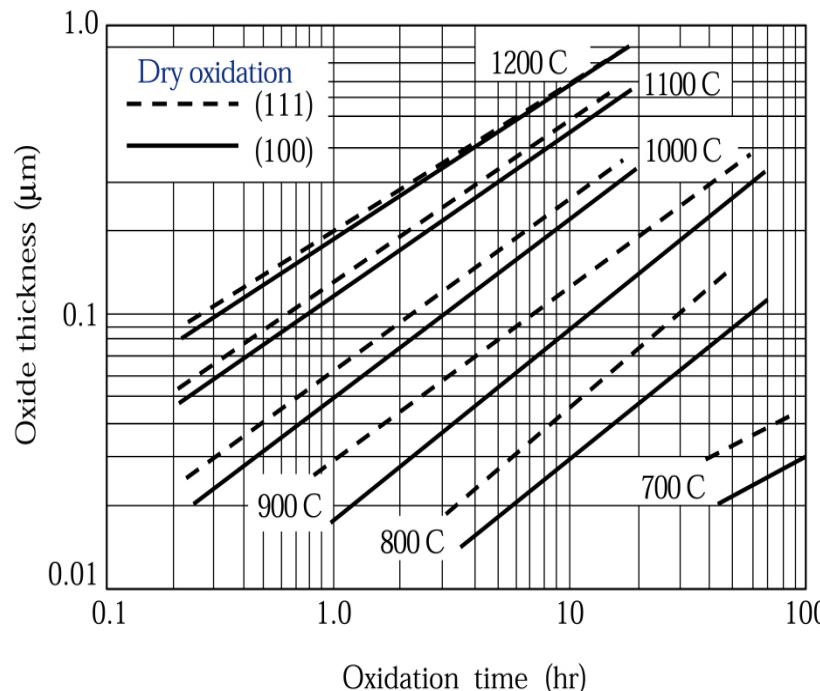


near to Si-Si bond breaking ~ 1.83eV



# Effect of Oxidation Ambient

- Wet oxidation rate is much higher than dry oxidation rate because the oxidant solubility in  $\text{SiO}_2$  ( $C^*$ ) is much higher (orders of magnitude) for  $\text{H}_2\text{O}$  than for  $\text{O}_2$ .
- The diffusion coefficient of  $\text{H}_2\text{O}$  is slightly higher (several times) than that of  $\text{O}_2$ .





# Mixed Ambient Oxidation

- Modeling of mixed ambient is assumed each of the oxidants acts independently.

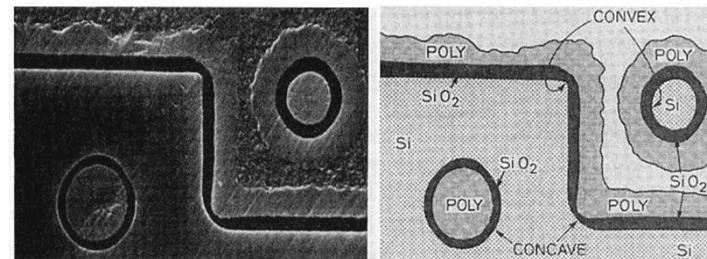
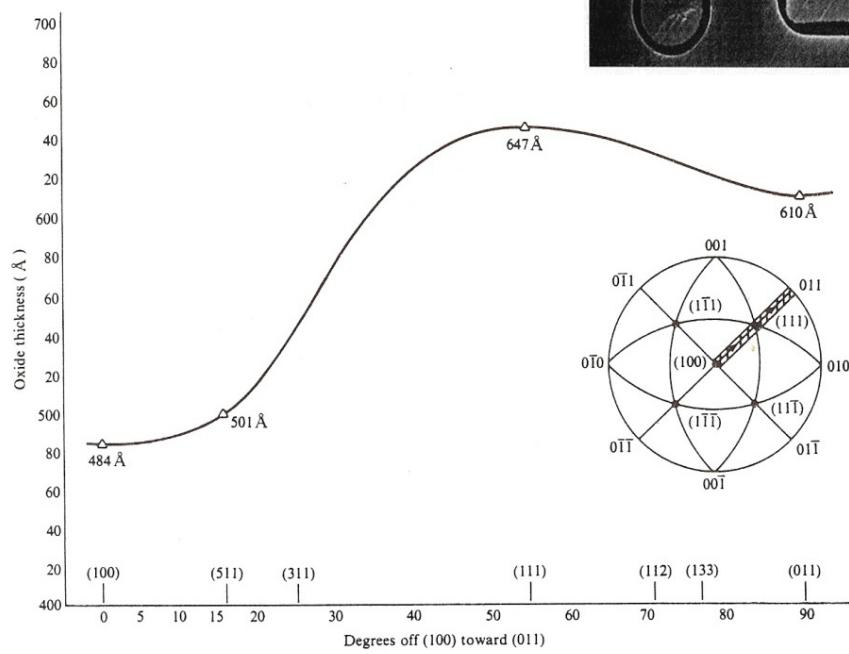
$$\frac{dx_o}{dt} = \sum_i \frac{B_i}{2x_o + A_i}, \text{ where } A_i \text{ and } B_i \text{ are corresponding to the ith oxidant.}$$

- Each B and B/A value must be corrected for the appropriate partial pressure of the corresponding oxidant.
- This simple approach works well in some cases such as H<sub>2</sub>O/O<sub>2</sub> and H<sub>2</sub>O/HCl mixtures.
- The assumption of independent reaction is not correct in the O<sub>2</sub>/HCl mixture so that this simple approach is not valid.

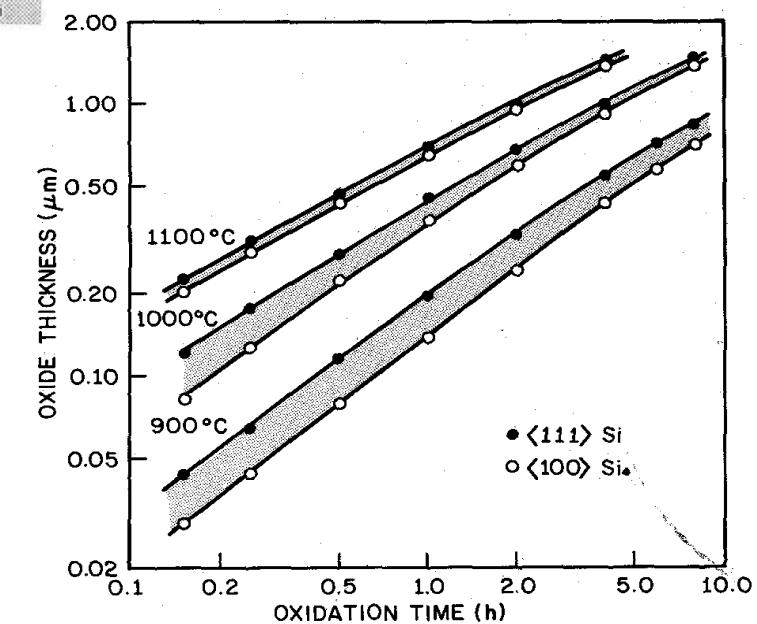


# Effect of Crystal Orientation

- Effect of crystal orientation is explained by the differences in the surface density of silicon atoms on the various crystal faces.



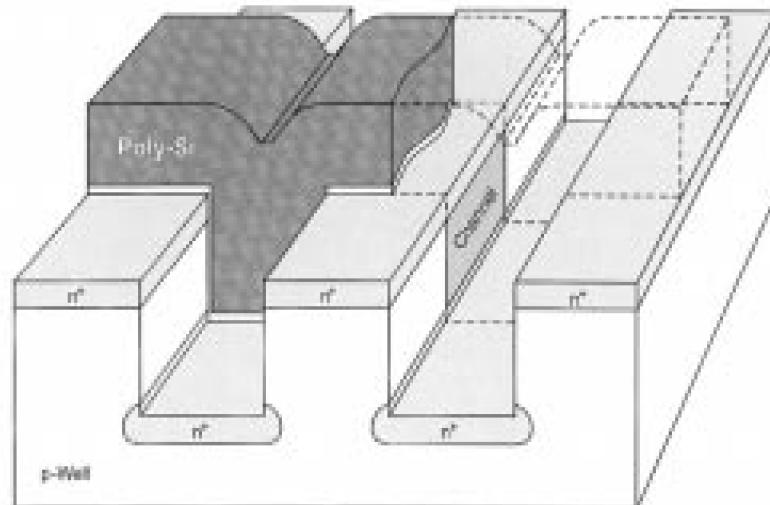
Dry O<sub>2</sub>/1000°C/1hr





# Gate Oxide in Vertical-channel

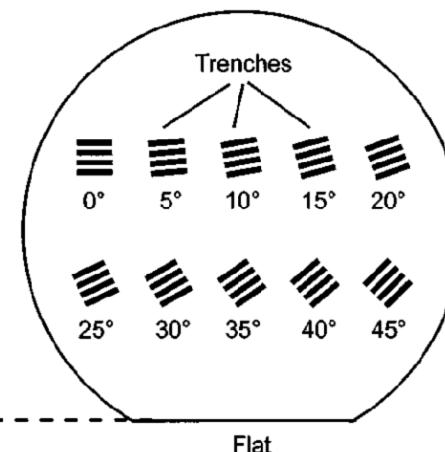
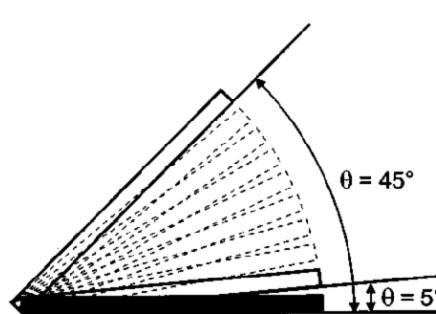
IEEE Trans. Electron Devices, Vol. 48, p.897 (2001)



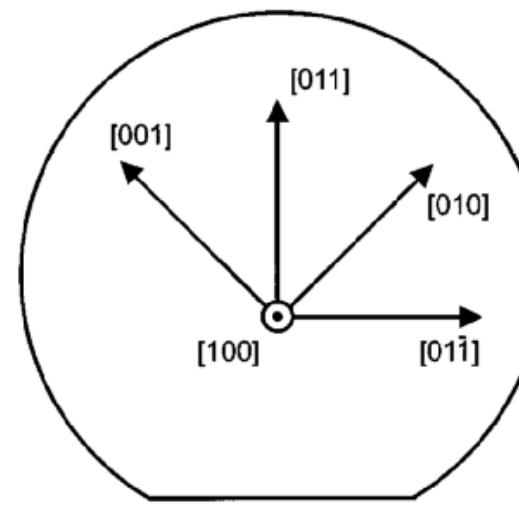
- Oxidation rate and dielectric properties strongly depend on the channel orientation.

Cystallographic orientation of the substrates

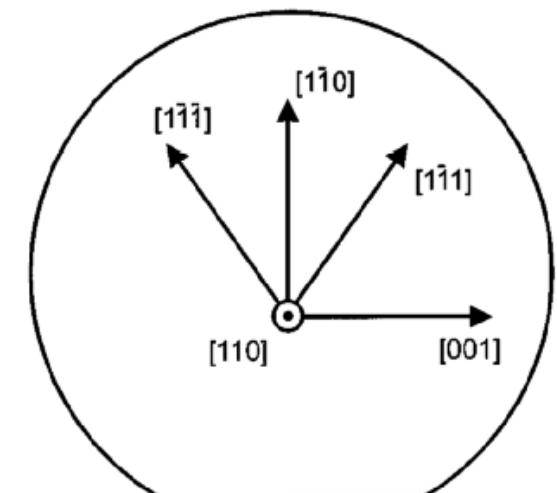
Rotationangle  $\theta$  (Relative to Flat)



Definition of  $\theta$



Flat: Parallel to [01̄1]



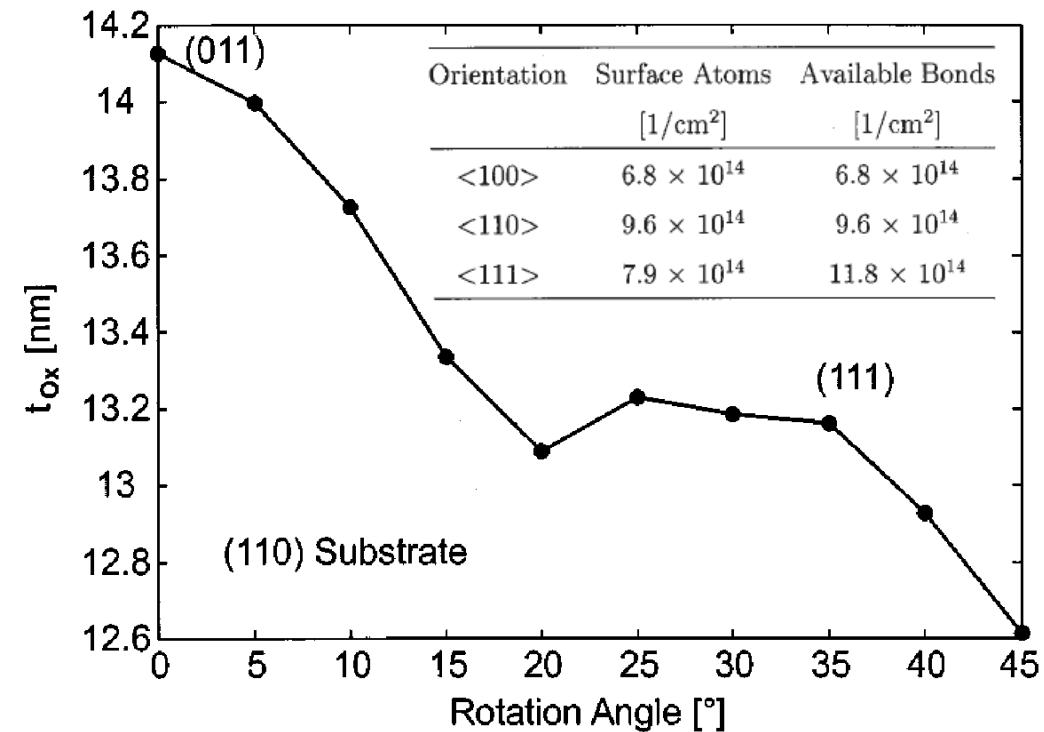
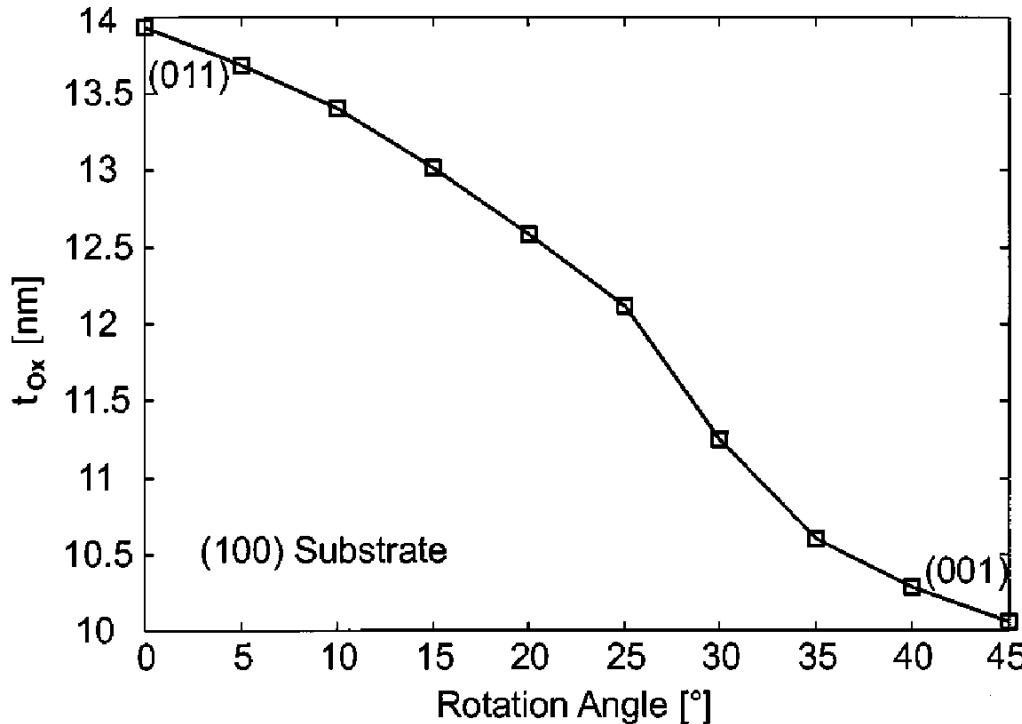
Flat: Parallel to [001]



# Orientation-dependent Oxide Thickness

IEEE Trans. Electron Devices, Vol. 48, p.897 (2001)

- Electrically measured gate oxide thicknesses at trench sidewalls featuring different crystallographic orientations.
  - Thin oxide: oxidation rate is dominated by the available Si atoms per unit area.
  - Thick oxide: the available bonds becomes more important.



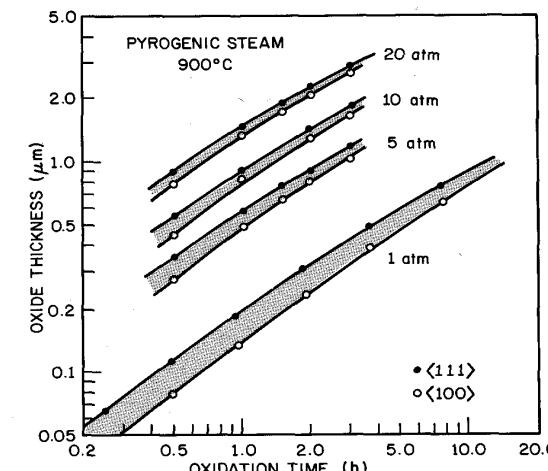
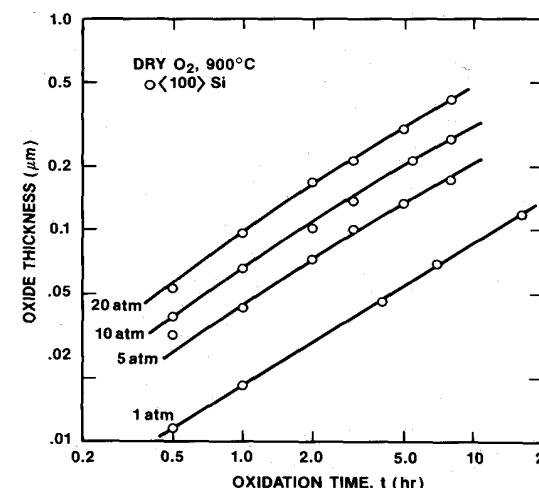


# Effect of Pressure

- The concentration of oxidant inside the oxide at the gas/SiO<sub>2</sub> interface C\* is proportional to p<sub>g</sub>, then both B and B/A are proportional to p<sub>g</sub>.
  - For a constant growth rate, every 1atm increase can lower down growth temperature by 30°C.
  - Higher dielectric strength can be obtained with high pressure processing.

$$\frac{B}{A} = \left( \frac{B}{A} \right)^i P \text{ and } B = (B)^i P \text{ for H}_2\text{O, where } i \text{ refers the respective values at 1 atm.}$$

$$\frac{B}{A} = \left( \frac{B}{A} \right)^i P^n \text{ and } B = (B)^i P^n \text{ for O}_2, \text{ where } n \approx 0.7 \sim 0.8.$$

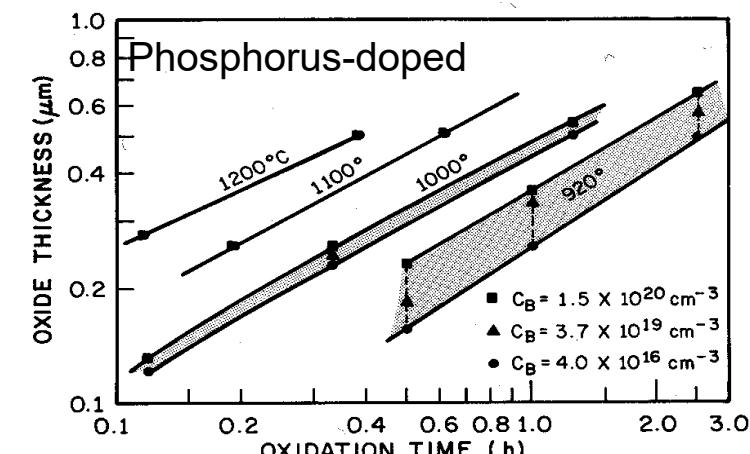
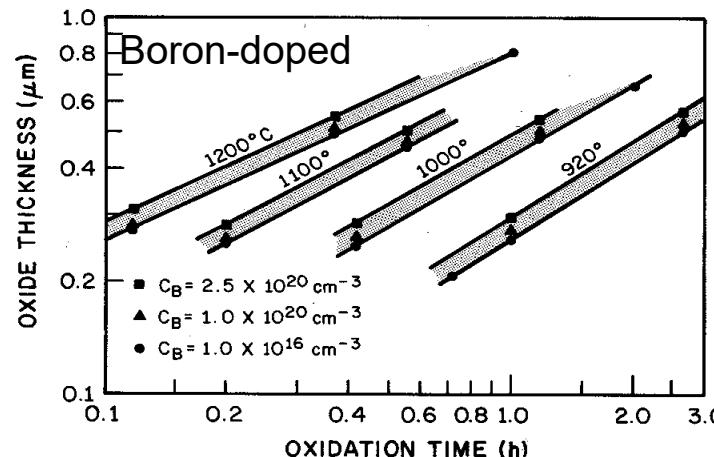




# Effect of Impurity Concentration

- The mechanism associates with the faster oxidation at the  $\text{SiO}_2/\text{Si}$  interface due to higher vacancy concentration, i.e. B/A is affected.

- $\frac{B}{A} = R_1 + KC_{V^T}$ , where  $R_1$  represent all mechanisms other than the vacancy driven process and  $C_{V^T}$  is the total vacancy population at the oxidation temperature.
- The differences of oxidation rate is more pronounced for  $n^+$  Si than for  $p^+$  Si and is more pronounced for low temperature oxidation compared to high-temperature oxidations.





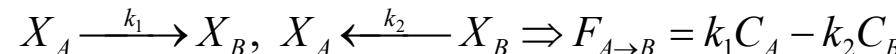
# Dopant Segregation - 1

## ➤ Dopant segregation coefficient

- The ratio of the equilibrium doping concentration on each side of the interface.
- The difference in a dopant's solubility in each phase drives a diffusion flux until the chemical potential equalizes.

## ➤ Consider two separate phases A and B

- The flux of material X from A to B is

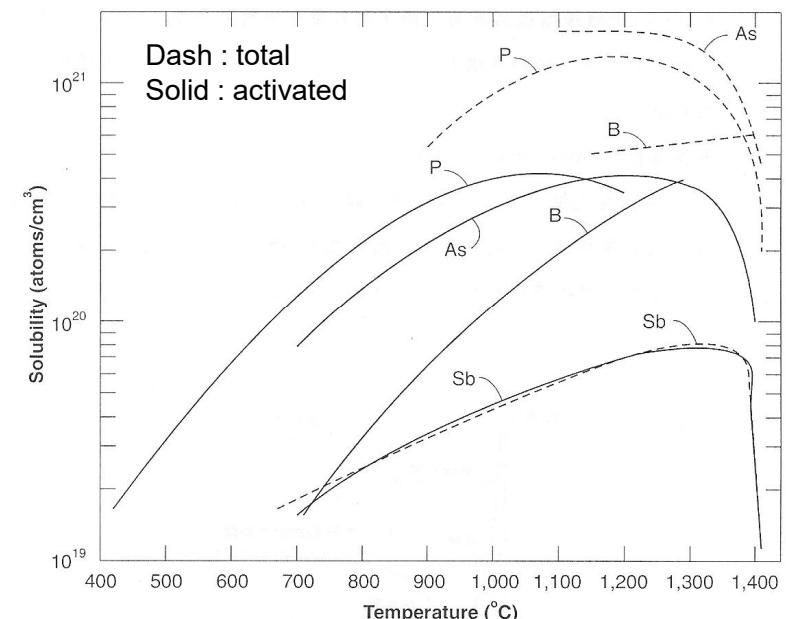


- In steady-state,

$$F_{A \rightarrow B} = 0 \Rightarrow \frac{C_B}{C_A} = \frac{k_1}{k_2} = k_0$$

$$\therefore F = k_1 \left( C_A - \frac{C_B}{k_0} \right) = h \left( C_A - \frac{C_B}{k_0} \right)$$

, where  $h$  is the interface transfer coefficient (cm/sec)  
and  $k_0$  is the segregation coefficient.



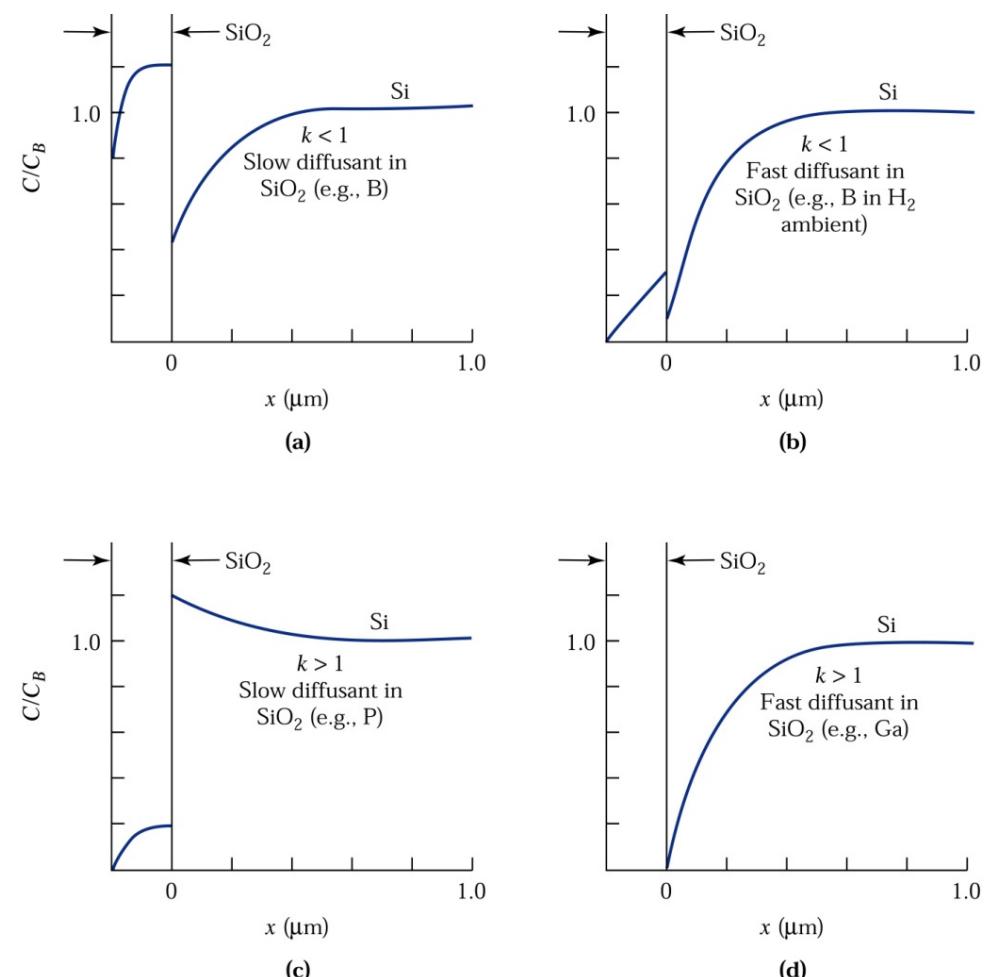


# Dopant Segregation - 2

- Dopant Segregation and dopant diffusivity determine the final profile.
- Segregation coefficient

$$k_0 = \frac{\text{equilibrium concentration in Si}}{\text{equilibrium concentration in } \text{SiO}_2}$$

$$k_0 = \begin{cases} 0.3 \text{ for B} \\ 10 \text{ for As} \\ 10 \text{ for Sb} \\ 10 \text{ for P} \end{cases}$$



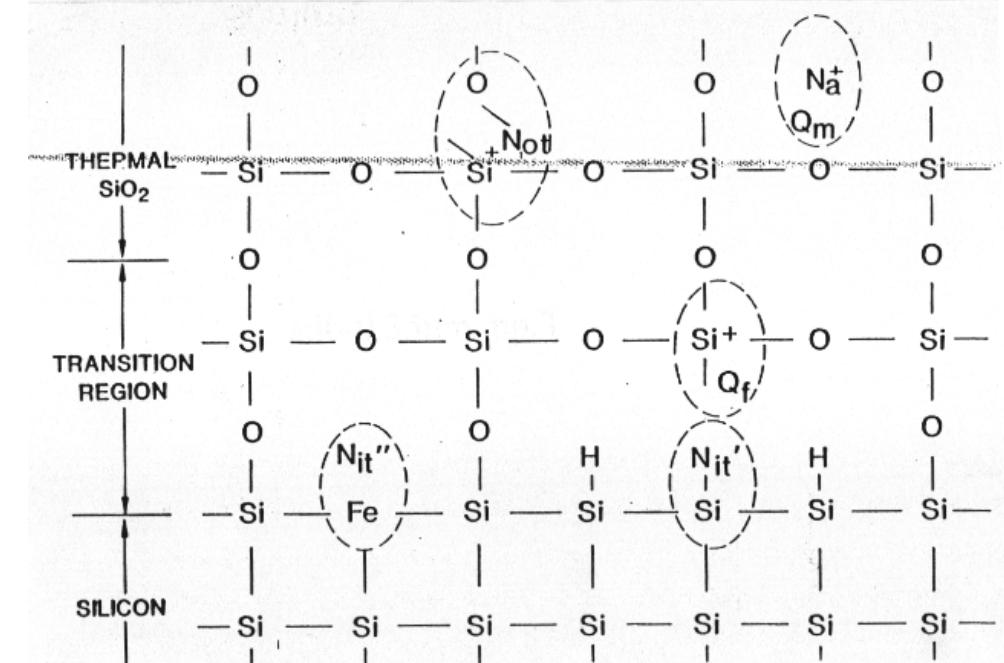
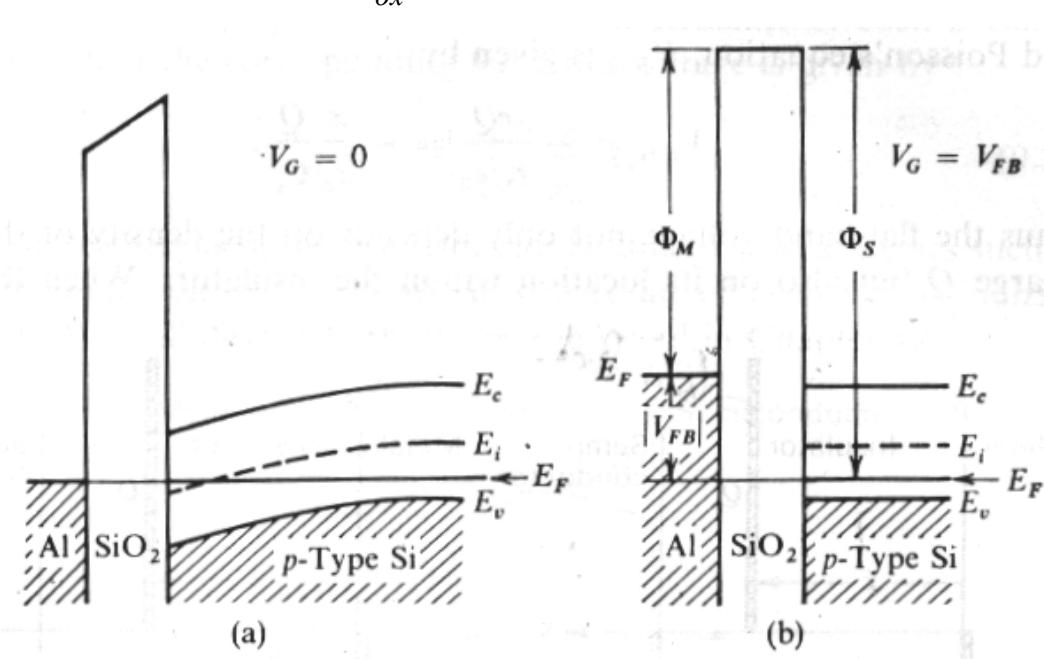


# Oxide Charges

- Flat-band voltage ( $V_{fb}$ ) and threshold voltage ( $V_{th}$ )

$$V_{fb} = \phi_{ms} - \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{T_{ox}} \left[ \frac{x}{T_{ox}} \rho_m(x) \right] dx$$

$$V_{th} = V_{fb} - \frac{Q_{Si}}{C_{ox}} + 2\phi_F$$

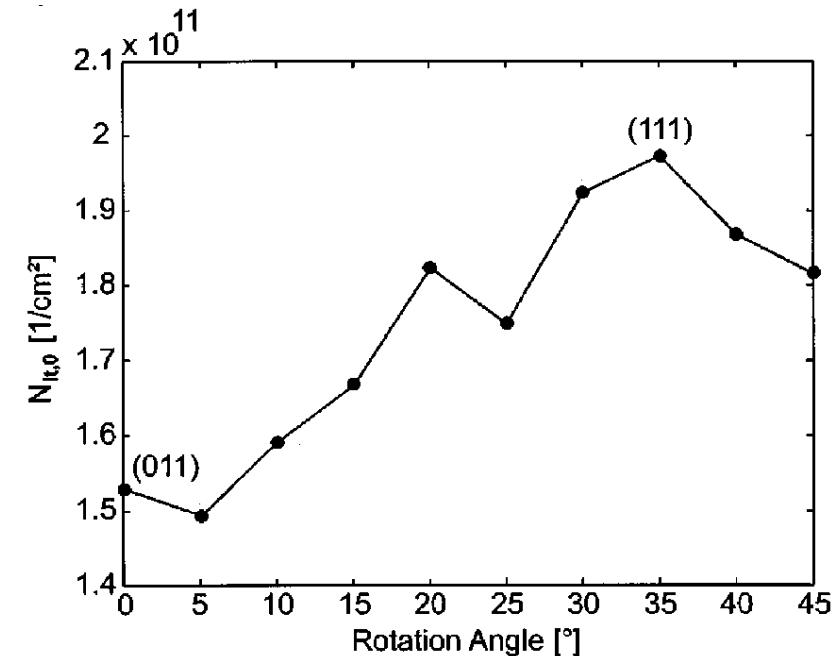
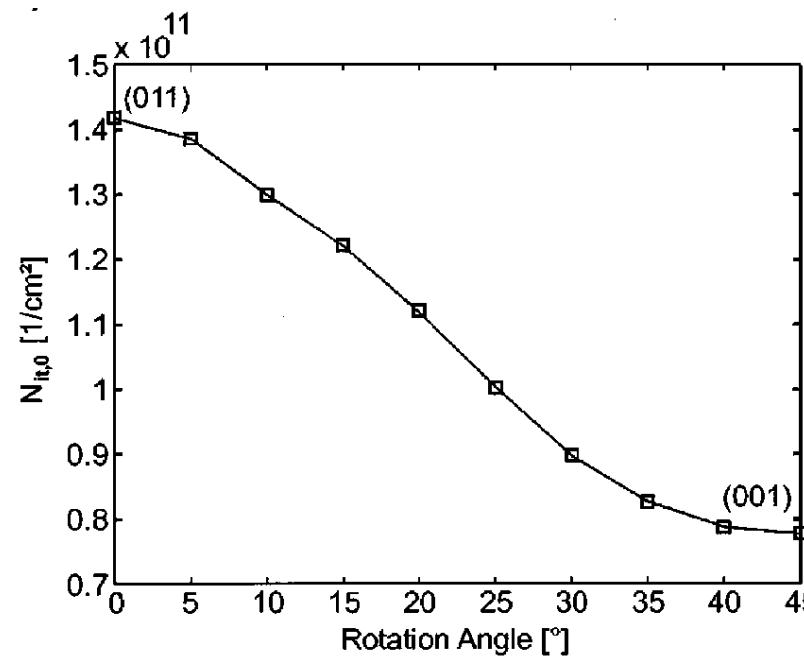




# Oxide Charges

## ➤ Interface charge ( $Q_{it}$ )

- Magnitude depends on Si orientation :  $(111) > (110) > (100)$
- Magnitude depends on surface impurity and interface bonding
- Magnitude can be reduced by annealing at 400-500°C in H<sub>2</sub> ambient.
- Nitrogen or Fluorine passivation can reduce  $Q_{it}$ .



(IEEE Trans. Electron Devices, Vol.48, p.897, 2001)



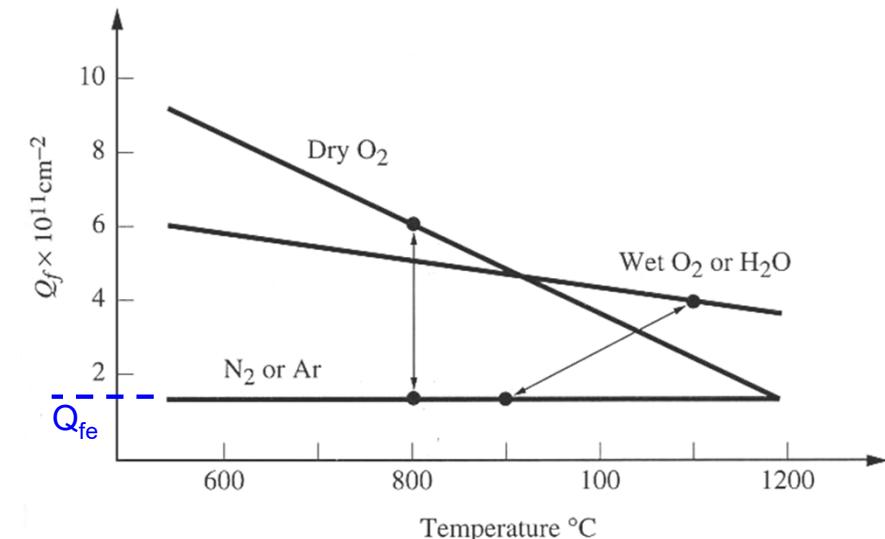
# Oxide Charges

## ➤ Fixed charge ( $Q_f$ )

- Immobile and independent of surface potential.
- Depends on Si orientation and oxidation condition.
- In the  $Q_f$  triangle plot, each curve represents equilibrium values for the ambient and that temperature. The arrows indicate that any point on any curve can be reached simply by changing the temperature and ambient in the furnace.  $Q_{fe}$  is the value in  $N_2$  or Ar ambient.
- When an oxidation ambient is switched to an Ar ambient,  $Q_f$  reduces with the following time dependence:

$$Q_f(t) = (Q_f(0) - Q_{fe}) e^{\frac{-t}{\tau}} + Q_{fe}, \text{ where } \tau = 5.41 \times 10^{-10} e^{2.42eV/k_B T} \text{ min,}$$

$$Q_{fe} = 5.24 \times 10^9 e^{0.36eV/k_B T} \text{ cm}^{-2} \text{ for (111), } Q_{fe} = 5.22 \times 10^7 e^{0.69eV/k_B T} \text{ cm}^{-2} \text{ for (100).}$$





# Oxide Charges

## ➤ Mobile ion ( $Q_m$ )

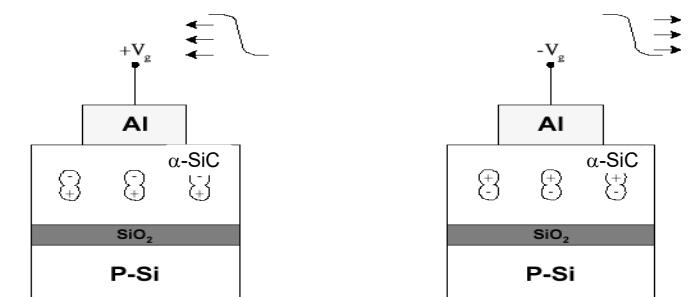
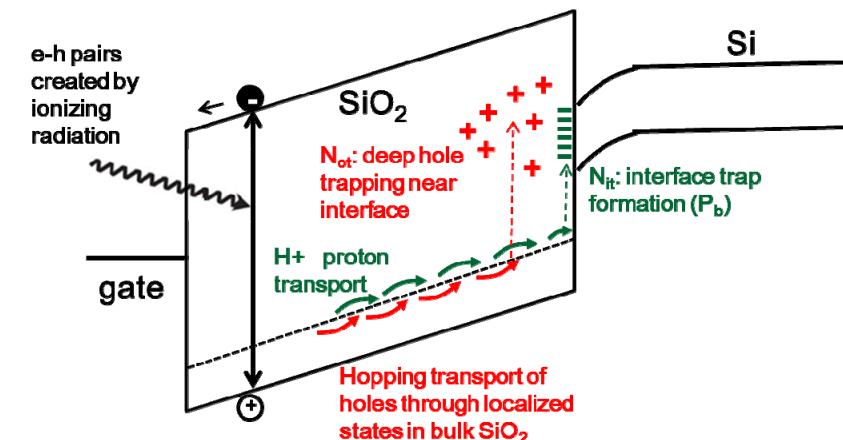
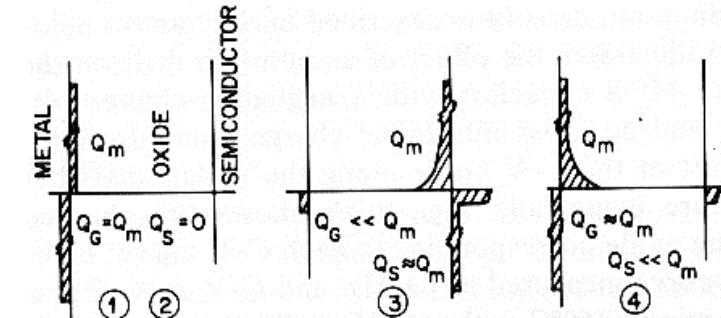
- Comes from metals contamination
- Drift rate is thermally activated and is field dependent

## ➤ Trapped charge ( $Q_{ot}$ )

- Maybe positive or negative
- Maybe caused by ionization radiation or carrier injection
- Trap site comes from defect in oxide layer
- Low temperature annealing can not remove trap site but cause neutralization or compensation of trapped charge.

## ➤ Polarization charges ( $Q_p$ )

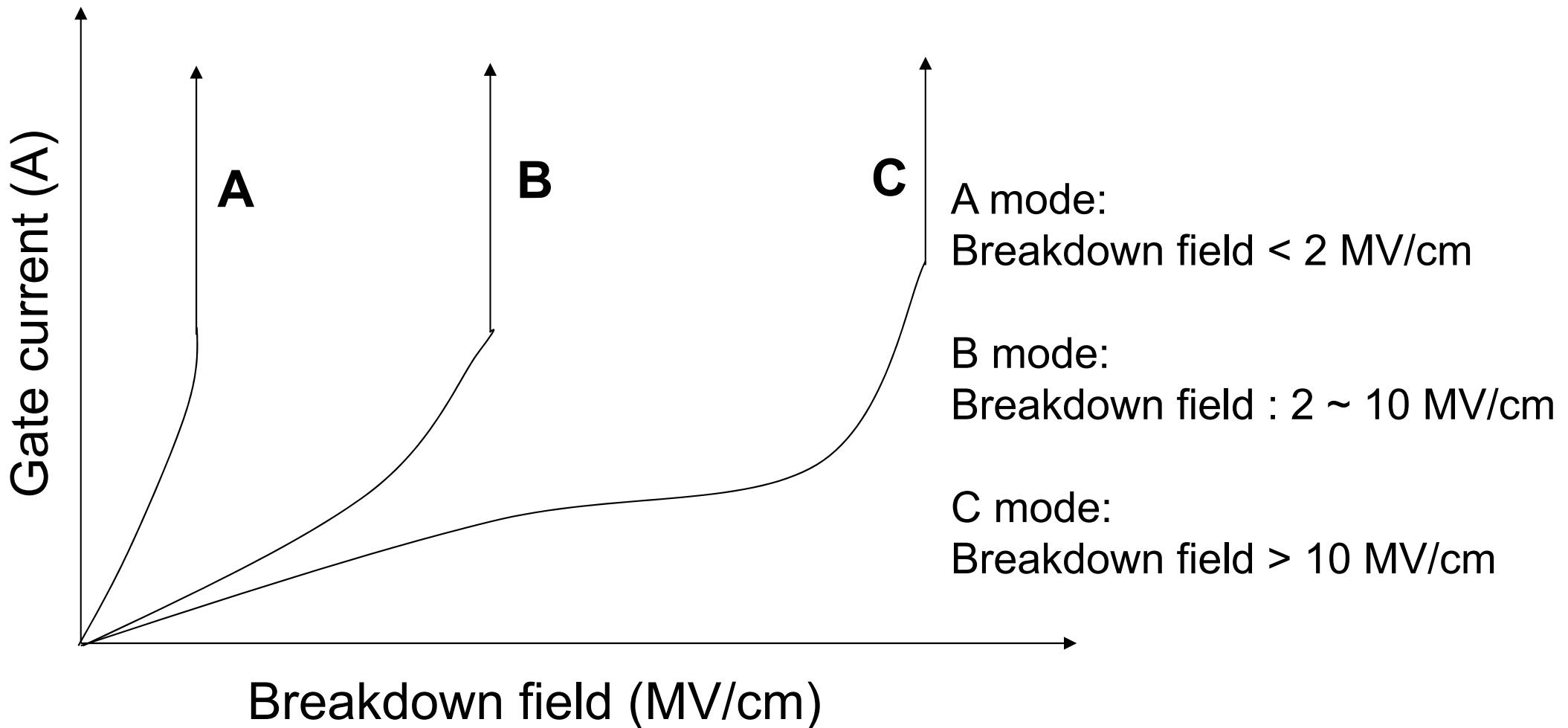
- Comes from electric field induced dipole.





# Ramped-voltage Breakdown - 1

(suitable for testing oxide thicker than 6 nm)



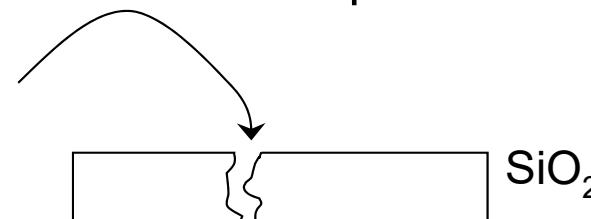


# Ramped-voltage Breakdown - 2

(suitable for testing oxide thicker than 6 nm)

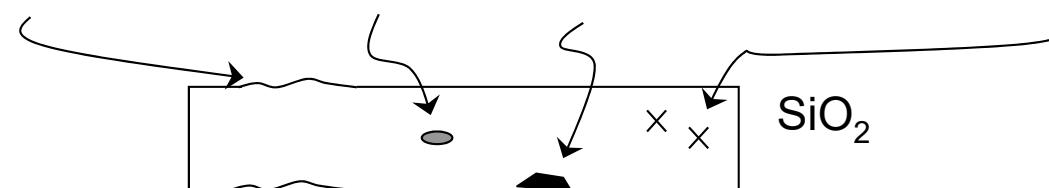
## ➤ A mode (nearly short)

- Surface contamination or pinhole



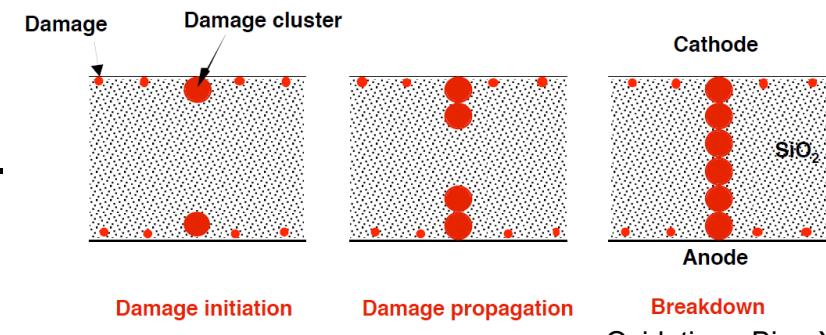
## ➤ B mode (middle-field breakdown)

- Interface roughness, impurity, precipitates, structural weakness



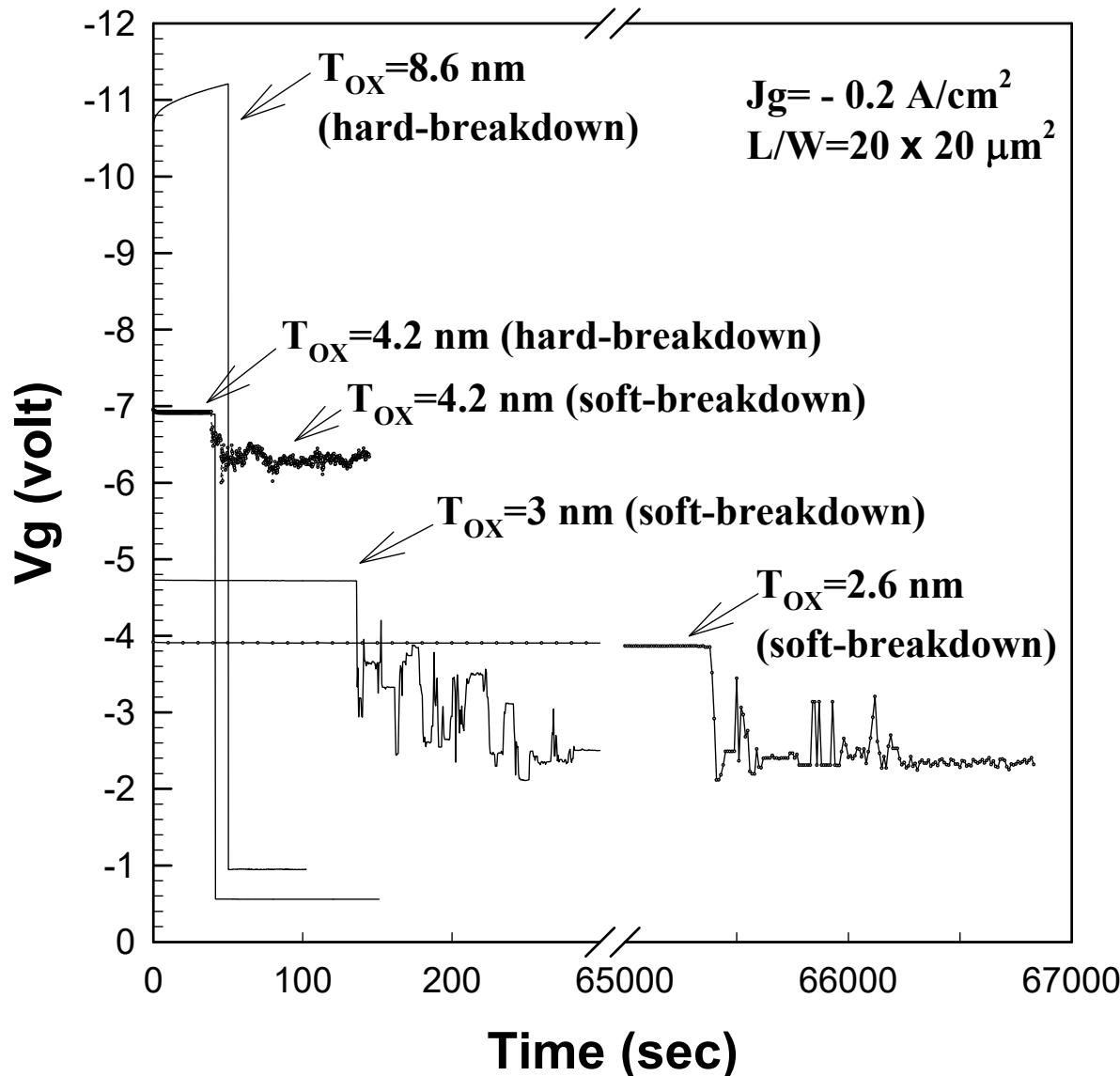
## ➤ C mode

- Intrinsic breakdown
- A and B modes are extrinsic breakdown.





# Breakdown Modes in Thin Oxides



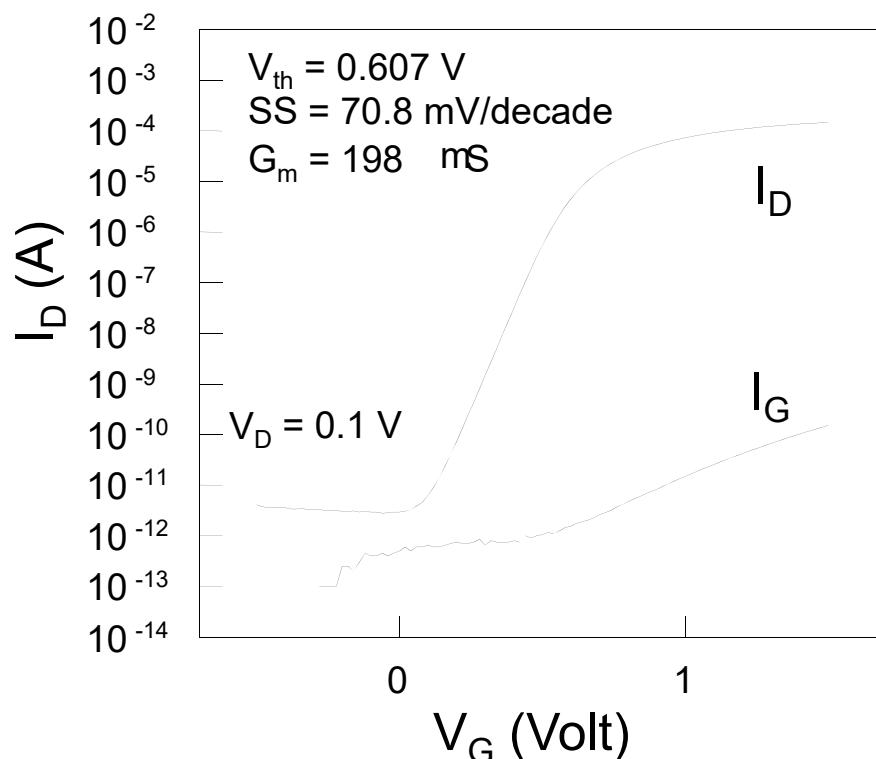
- $T_{ox} > 6\text{ nm}:$ 
  - Hard-breakdown dominates
- $6\text{ nm} > T_{ox} > 3\text{ nm}:$ 
  - Probability of soft-breakdown increases with decreasing  $T_{ox}$ .
- $T_{ox} < 3\text{ nm}:$ 
  - Soft-breakdown (SBD) dominates
  - Stress induced leakage current (SILC)



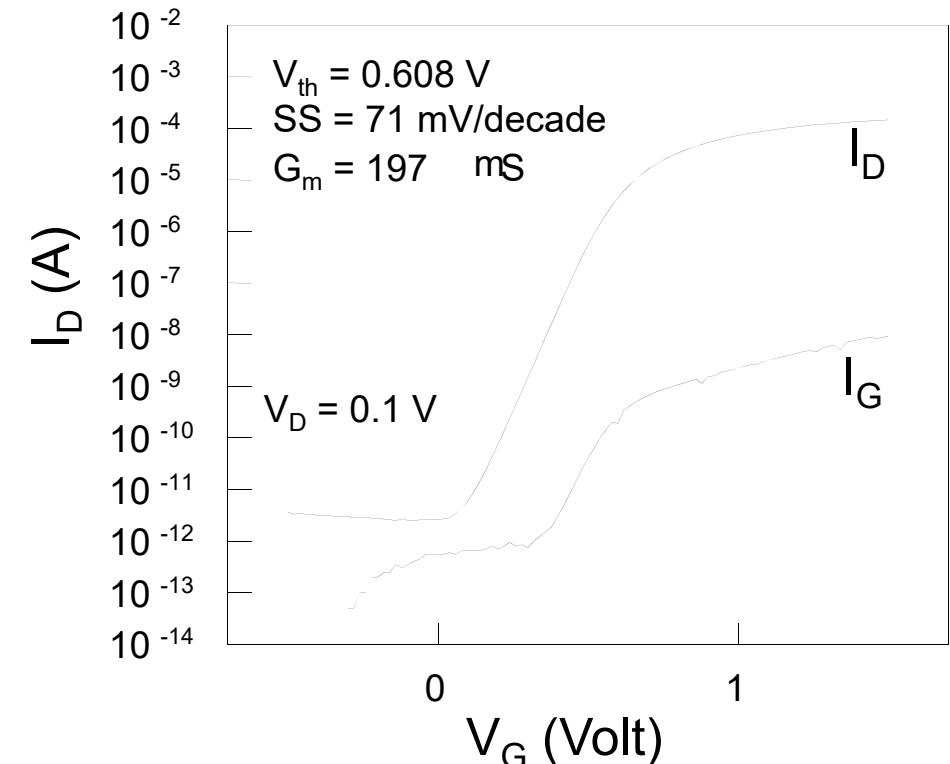
# Impact of Soft-Breakdown

- Occurrence of SBD may not affect the operation of a transistor.

$$T_{ox} = 2.5 \text{ nm}$$



Fresh device



After SBD



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電子工程學系暨電子研究所  
National Chiao-Tung University  
Department of Electronics Engineering &  
Institute of electronics

# Oxide Hardness



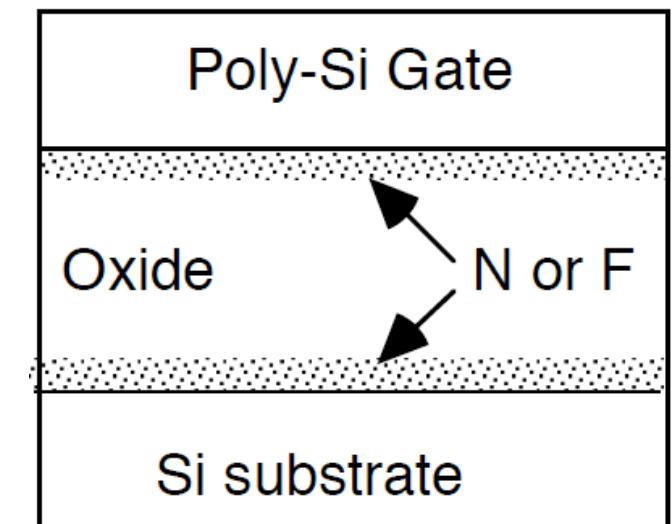
# Chlorine Incorporation

- A small amount of Cl-containing species is often added during oxidation. Effective for dry oxidation only.
  - It can clean the furnace by reacting with the unwanted metallic species to form gaseous by-products. Ex:  $TiCl_4$ ,  $FeCl_3$ , etc.
  - Cl can also be incorporated in the oxide (mostly near the oxide/Si interface) to provide some degree of protection from trace amount of mobile ions ( $Na^+$ ,  $K^+$ ) through gettering action.
  - Lower interface state density and lower defect density can be achieved.
  - Cl concentration incorporated in the oxide is small (typically <3%) to avoid device degradation.
  - Oxidation rate is increased with Cl addition (typically 1 ~ 15%) due to
$$4HCl + O_2 \rightarrow Cl_2 + 2H_2O$$
  - High Cl concentration (TCA>8%) would results in rough  $SiO_2/Si$  interface.
  - Cl sources: HCl, TCE ( $C_2HCl_3$ ), TCA ( $CH_3CCl_3$ ), or Trans-LC (DCE,  $C_2H_2Cl_2$ ).



# Fluorine Incorporation

- The weaker interface can be strengthened substantially by incorporating another atom like N or F.
- The Si-H bond is about 3.1 eV whereas that of Si-F bond is about 5.6 eV and Si-N bond is 4.75 eV.
- Methods
  - HF surface immersion
  - $F_2$  or  $NF_3$  plasma surface treatment
  - Oxidation with  $NF_3$  additive
  - $F^+$  implantation into Si or oxide
- Fluorine effects
  - Enhanced oxidation rate.
  - Better oxide quality but the process window is small.
  - Enhanced boron penetration.
  - Lower dielectric constant and poorer dielectric reliability with excess fluorine.





# Effect of Nitrogen Incorporation

## ➤ Advantages

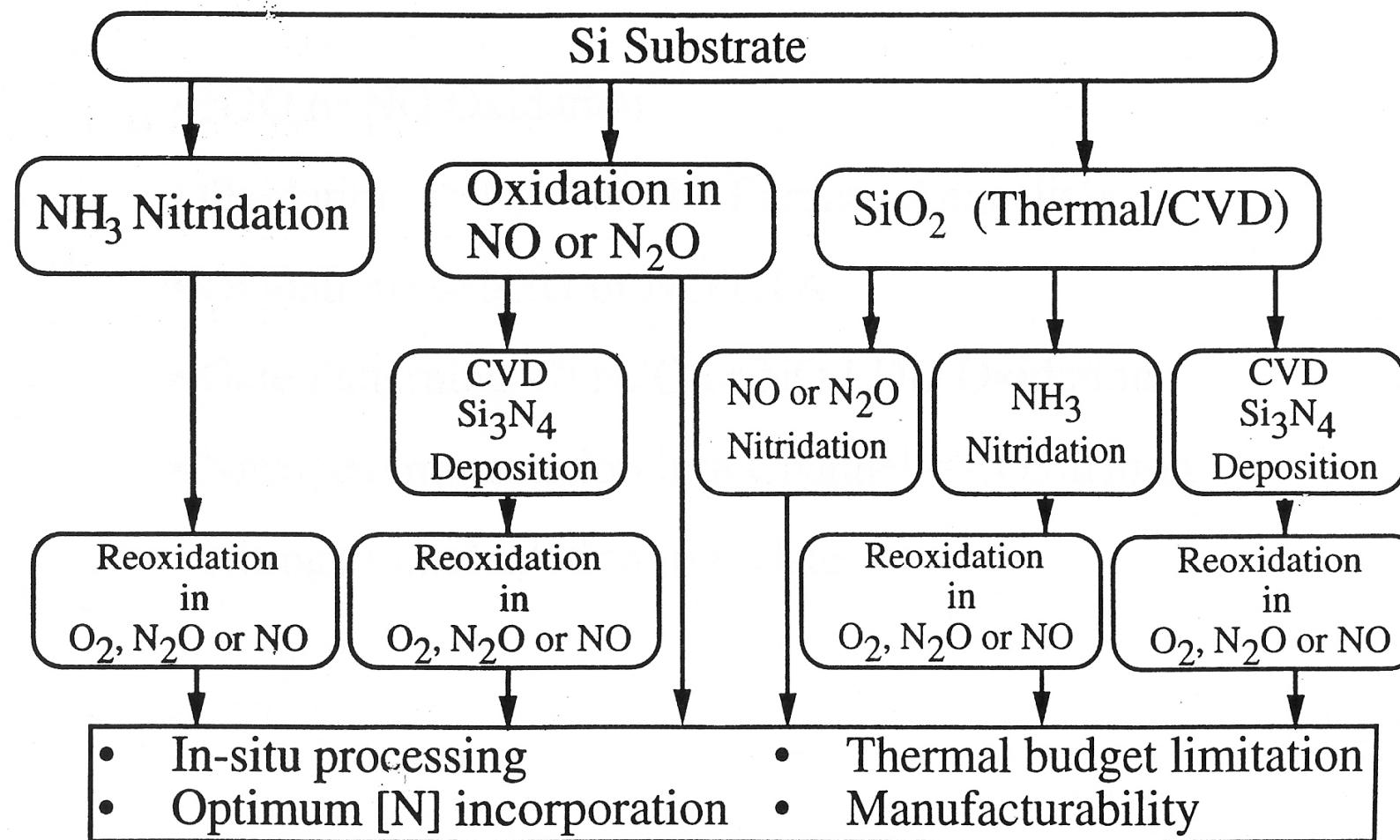
- Reduced leakage (as compared with the oxide).
- Effective dielectric constant is higher in heavily nitrided oxides.
- Strengthen the structure. Strain energy in the interfacial transition layer could be significantly reduced.
- Improved immunity to SILC.
- Improved immunity to hot-carrier effect.
- Increased resistance to impurity (e.g., boron, metal) diffusion.

## ➤ Disadvantages

- More fixed charges
- Degrade low  $V_G$  transconductance
- Noise performance
- NBTI



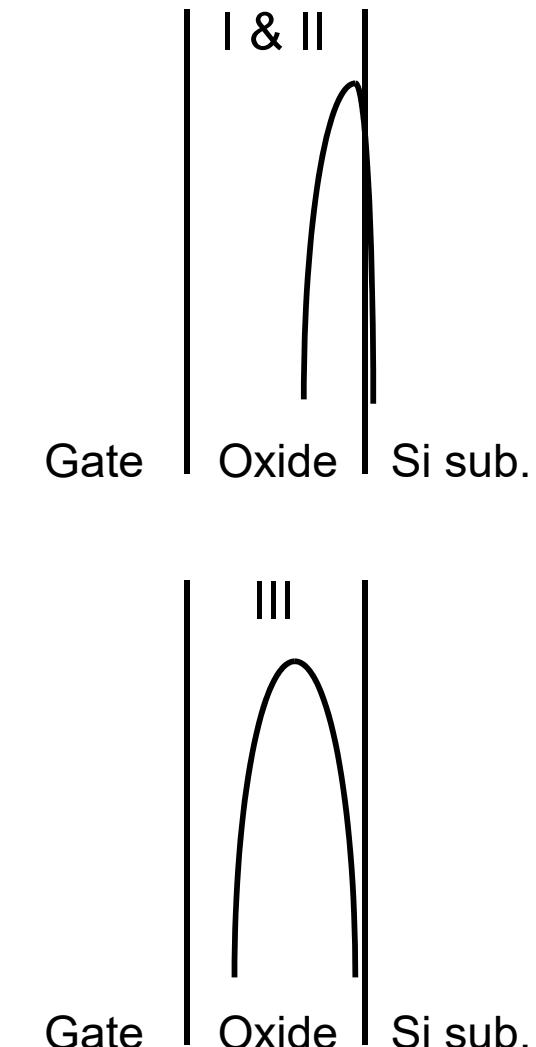
# Nitrogen Incorporation Technique





# Nitrogen Distribution - 1

- Method I: oxidation in an ambient containing  $\text{N}_2\text{O}$ 
  - IEDM, p.421 (1990)
  - IEEE EDL-14, p.342 (1993)
- Method II: (1) oxidation in  $\text{O}_2$  +  
(2) annealing in NO or  $\text{N}_2\text{O}$ 
  - Symp. VLSI Technol., p.43 (1991), p.105 (1994), p.49 (1997)
- Method III: (1) nitrogen ions implantation into Si +  
(2) oxidation in  $\text{O}_2$ 
  - IEEE, EDL, p.301 (1995), p.105 and 212 (1997)
  - IEDM, p.499 (1996), p.643 (1997)



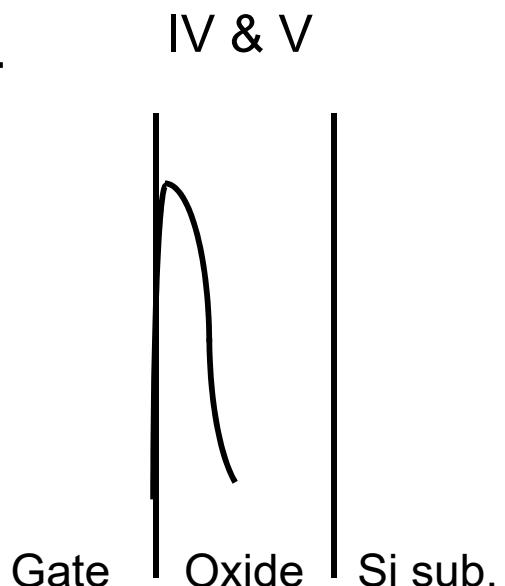


# Nitrogen Distribution - 2

➤ Method IV:(1) oxidation in  $O_2$  +  
(2) remote plasma nitridation

- IEDM, p.495 (1996), p.459 (1997)
- Symp. VLSI Technol., p.47 (1997)

➤ Method V: (1) deposition of nitride by CVD +  
(2) re-oxidation in  $O_2$   
• Symp. VLSI Technol., p.45 (1997)

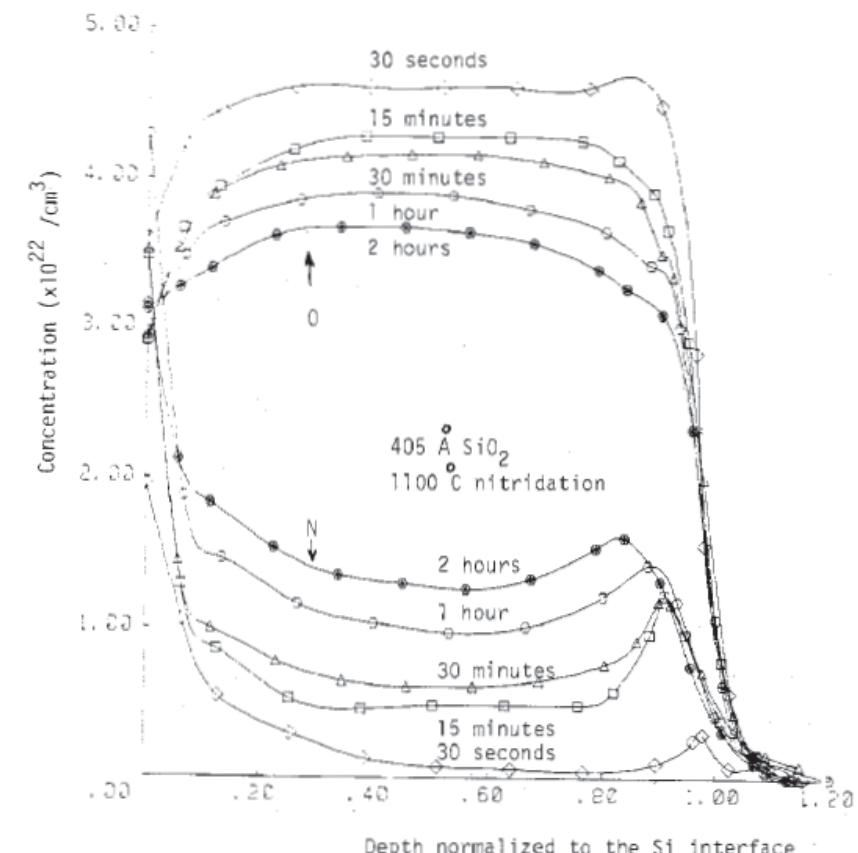




# Notes on Nitrogen Incorporation - 1

## ➤ By $\text{NH}_3$

- If the nitridation is done for a short time, N is incorporated only at the interface and the surface. However longer times and higher temperatures lead to N in the bulk also, which is undesirable because it causes bulk traps.
- Nitroxide formed by  $\text{NH}_3$  anneal of  $\text{SiO}_2$  contains lots of hydrogen. As a result oxide properties deteriorate rather than improving.



# Notes on Nitrogen Incorporation - 2

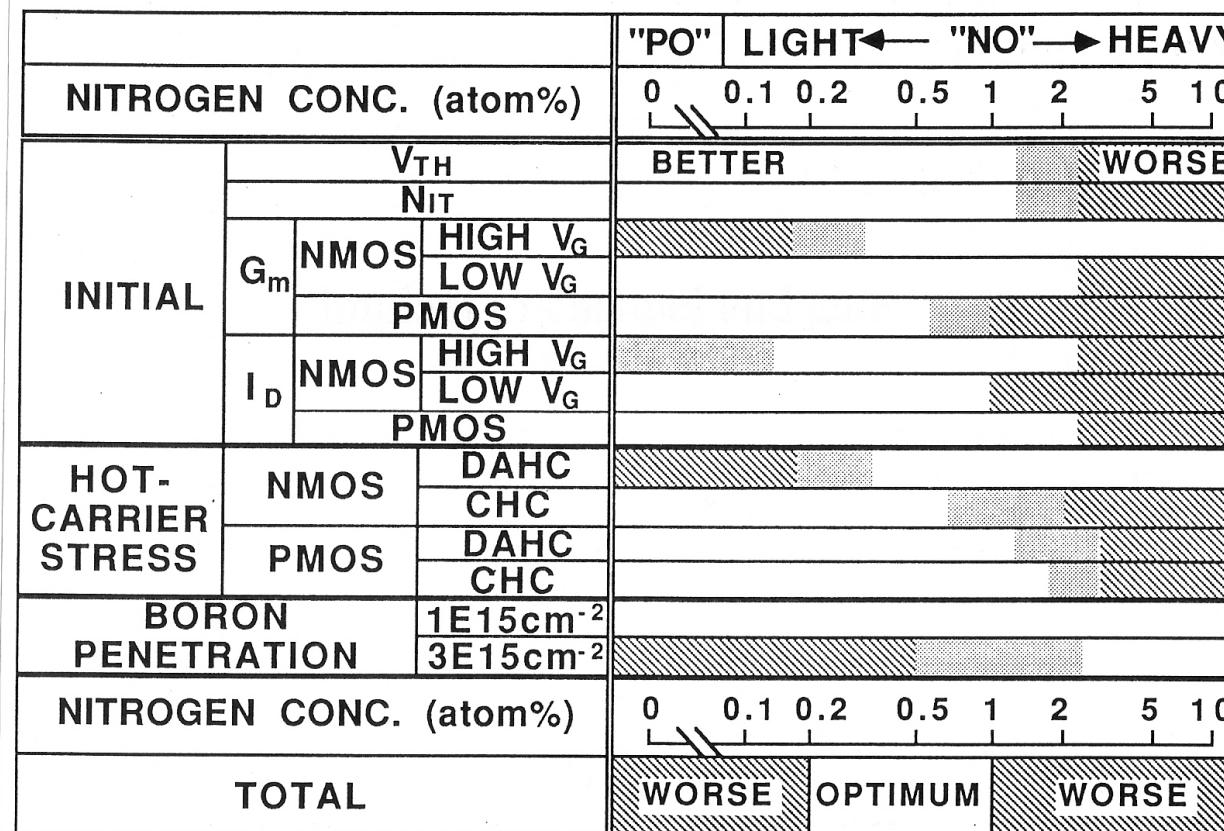
## ➤ By NO or N<sub>2</sub>O

- The mechanism of nitridation involves N<sub>2</sub>O splitting into NO and nitrogen upon heating
$$\text{N}_2\text{O} \rightarrow \text{N}_2 + \text{O}$$
$$\text{N}_2\text{O} + \text{O} \rightarrow 2\text{NO}$$
- Since NO is the critical species for nitridation it may be more efficient to use NO directly for nitridation rather than N<sub>2</sub>O.
- Fowler-Nordheim stressing of MOS devices shows less degradation after nitridation of gate oxide on NO. The anneal of SiO<sub>2</sub> in N<sub>2</sub>O or NO causes some increase in the gate oxide thickness due to the presence of oxygen.
- With high nitrogen concentration at the interface the effective mobility decreases at low electric field but at higher E-field it improves.
- This field dependence of mobility is speculated to be due to the increase in acceptor-like traps below the conduction band and reduction of interface states above the conduction band edge upon nitridation of oxide.



# Process Window of Nitrogen-incorporation

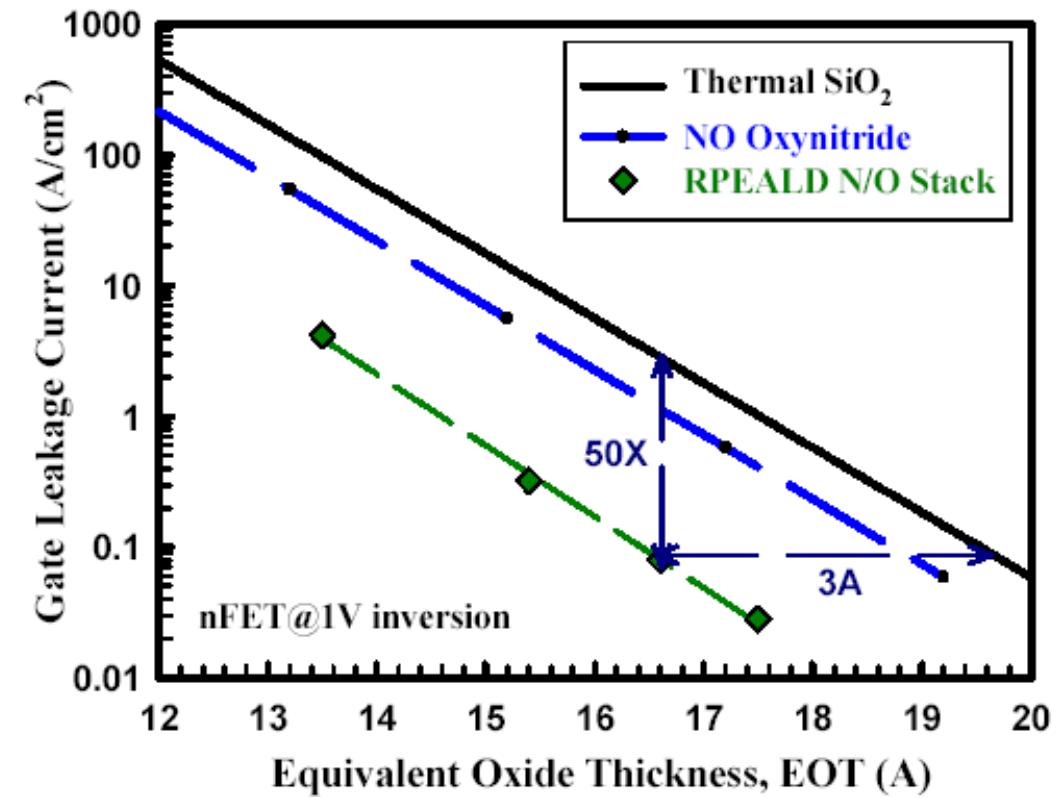
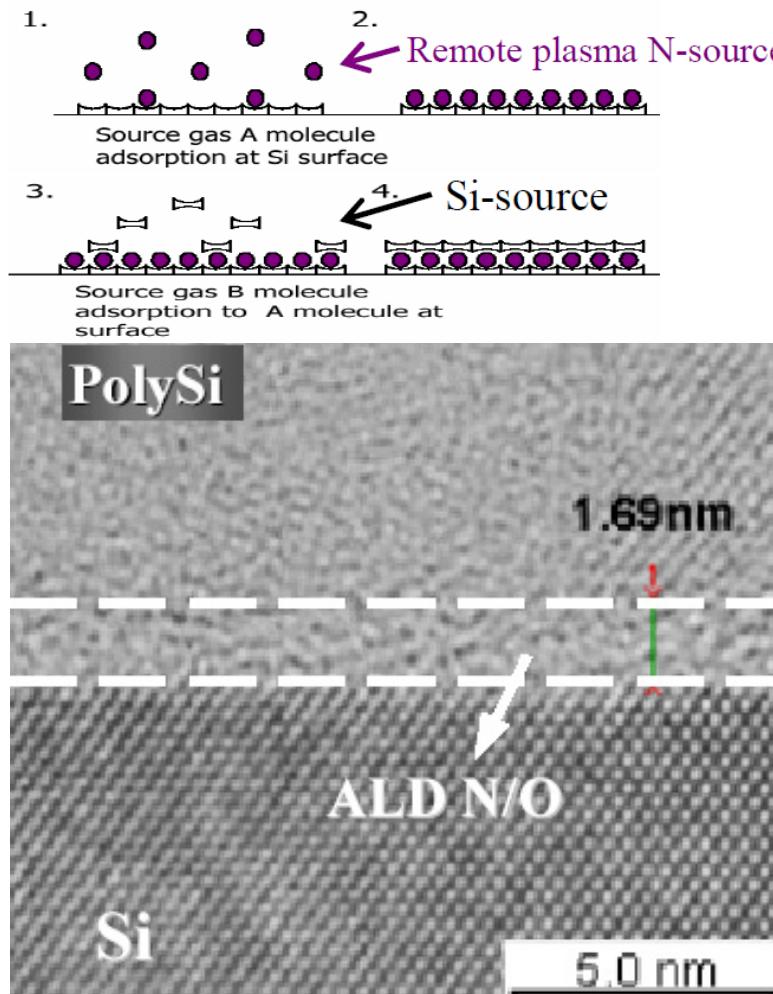
- Lower low field mobility
- Higher high field mobility
- Lower defect density
- Higher reliability
- Stronger radiation immunity
- Slower boron penetration





# Ultra-thin N/O Stack Gate Dielectric

(VLSI' 03, p.141)

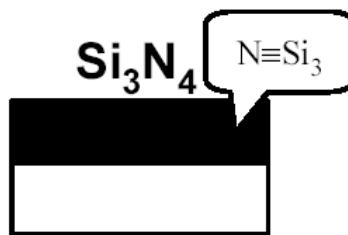




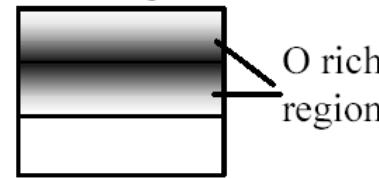
# Extreme Result of SiON Gate Dielectric

Novel Fabrication Process to Realize Ultra-thin ( $EOT = 0.7\text{nm}$ ) and Ultra-low Leakage SiON Gate Dielectrics (Toshiba, VLSI'04)

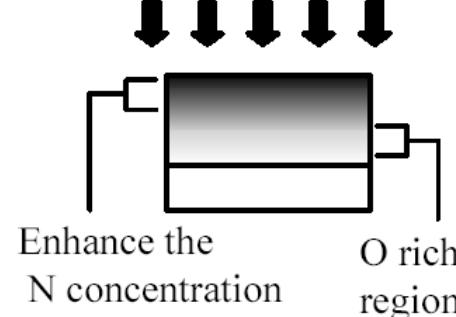
(1) Nitridation process



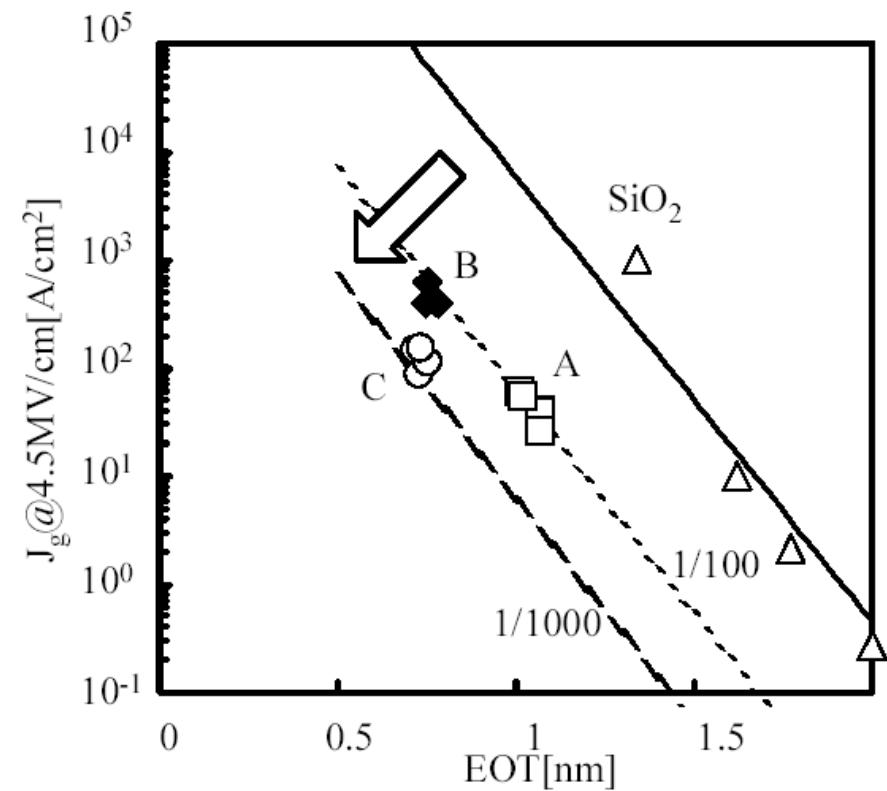
(2) Oxidation process



(3) Re-nitridation process



	Low temp.	High temp.
High press.	A	B
Low press.	—	C





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National Chiao-Tung University  
Department of Electronics Engineering &  
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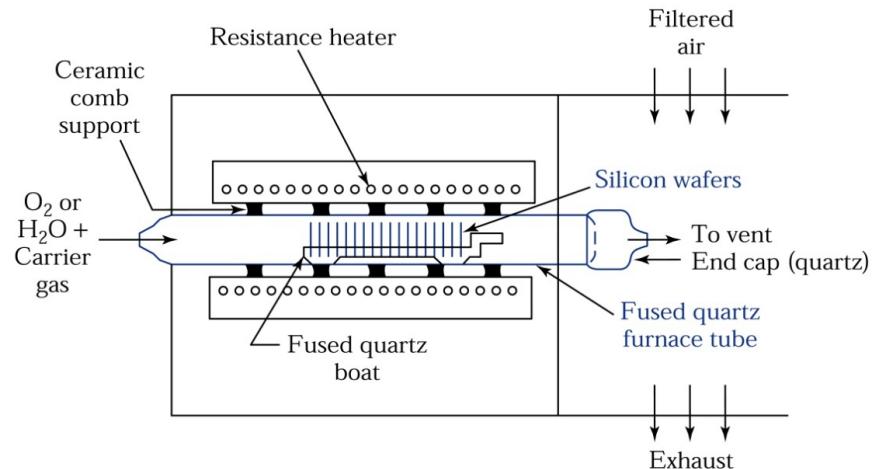
# Oxidation Equipments



# Oxidation Equipments

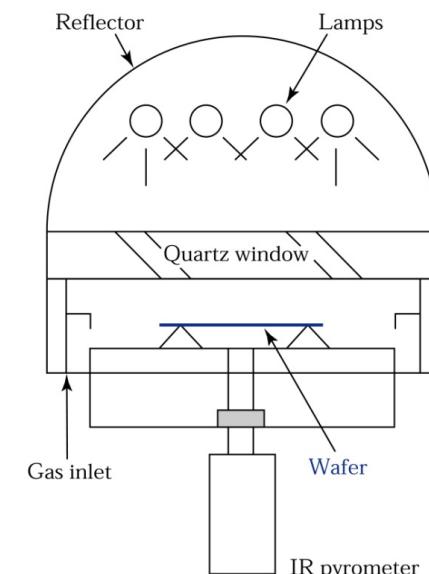
## ➤ Furnace systems (Hot wall)

- Multi-wafer (batch) processing
- Horizontal and vertical furnaces
- High pressure systems



## ➤ Rapid thermal processing (RTP) systems (Cold wall)

- Single wafer processing
- Much reduced thermal budget

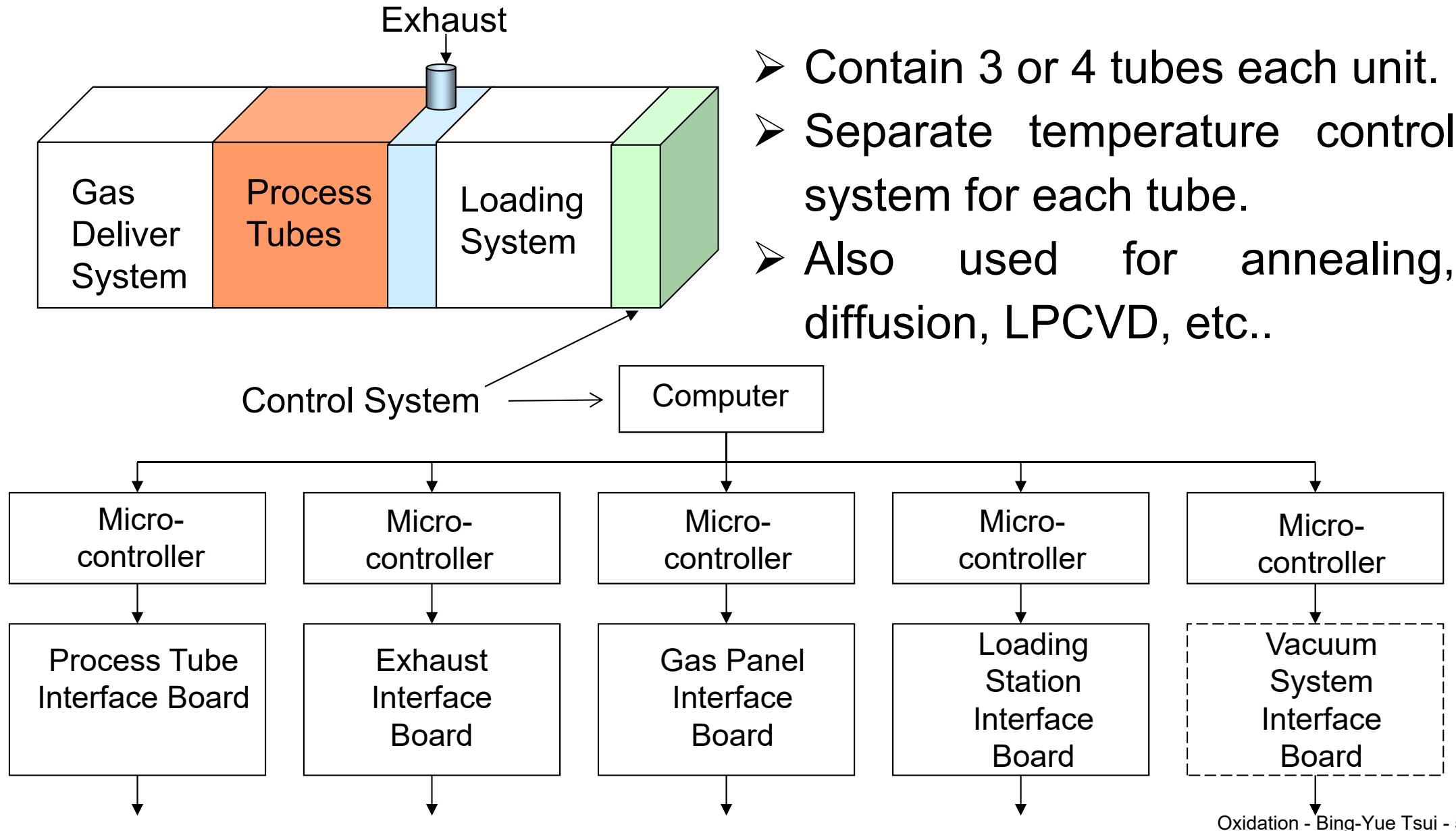


## ➤ Plasma oxidation systems

- Seldom used

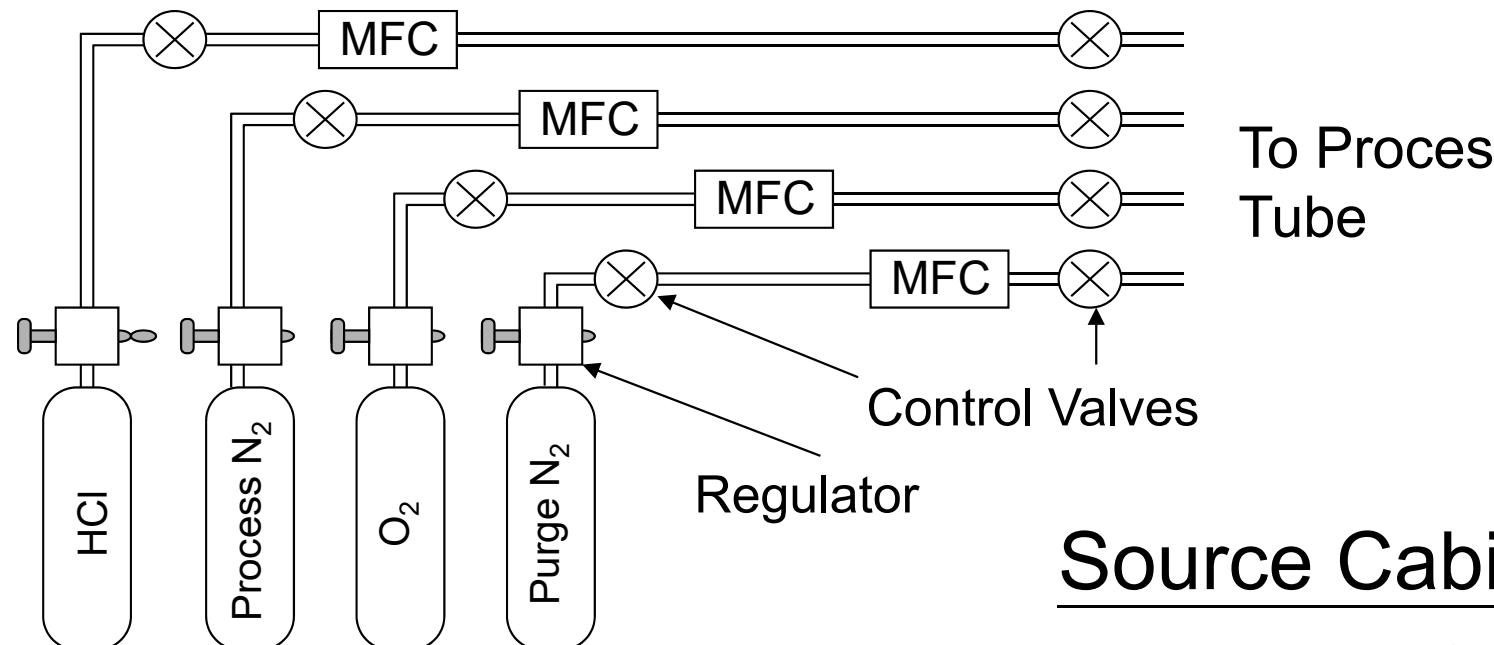


# Horizontal Furnace





# Gases and Piping for Dry Oxidation

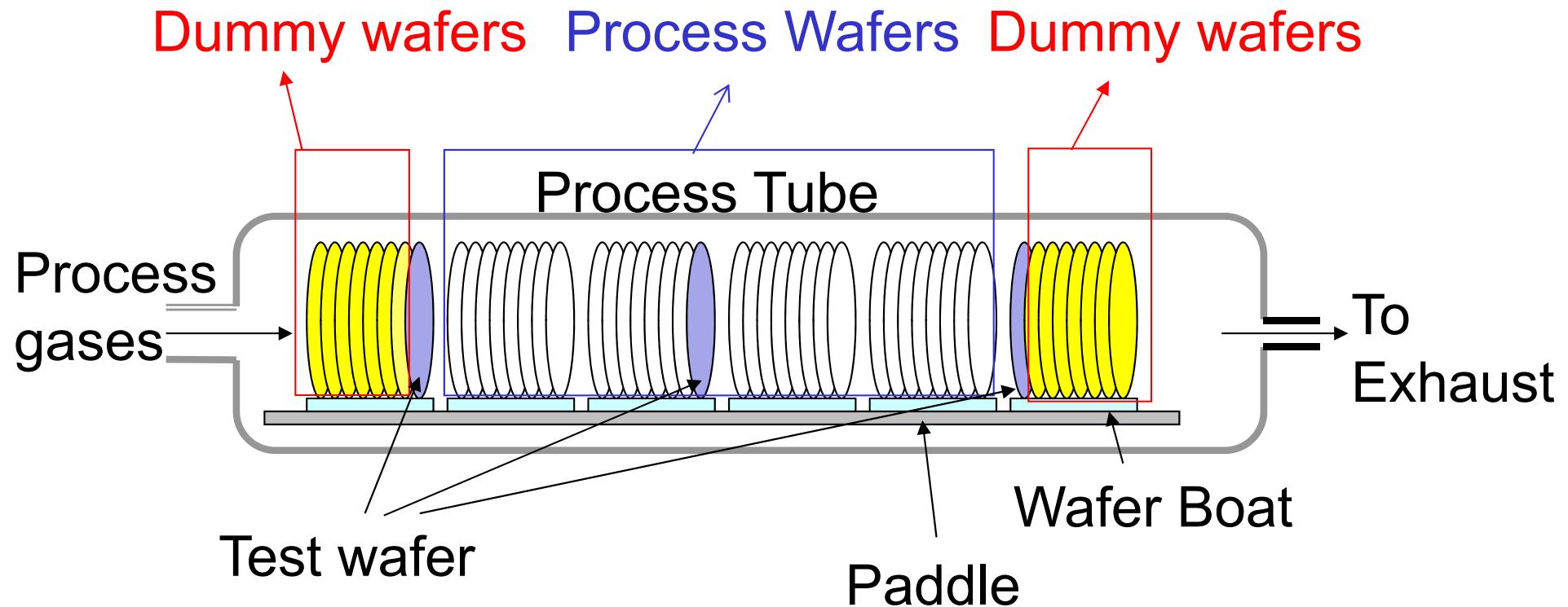


## Source Cabinet

- Source Gases
  - O<sub>2</sub>
  - H<sub>2</sub>O or H<sub>2</sub>
  - N<sub>2</sub>
  - HCl or trans-LC
  - N<sub>2</sub>O, NO
- Gas control panel
- Gas (mass) flow controller (MFC)
- Gas flow meter



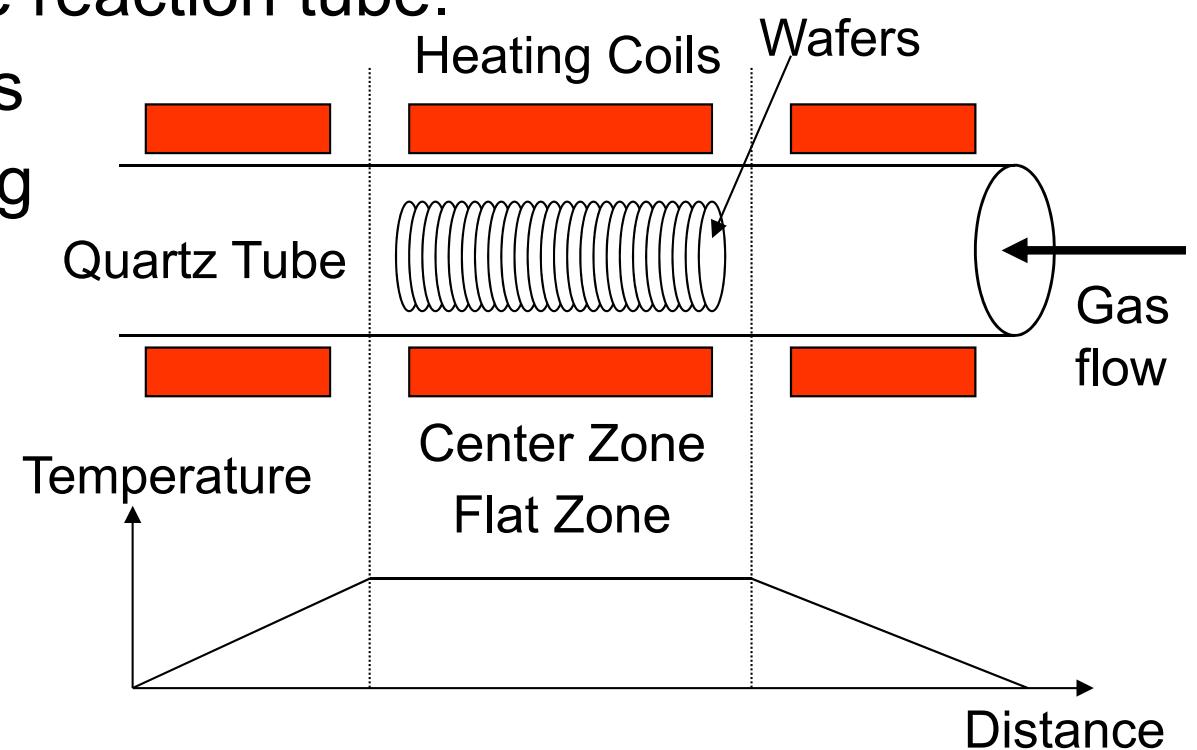
# Wafer Loading, Horizontal System





# Temperature Control

- Heating by metal resistance coils wrapped around the tube.
- Thermal processes are very sensitive to the temperature.
- Precise temperature control is vital.
- Multi-zone (usually 3-zone or 5-zone) system is used.
- Thermocouples touching the reaction tube.
- Proportional band controllers feed the power to the heating coils.
- Typical specifications:
  - $\pm 0.5^\circ\text{C}$  at central zone.
  - $\pm 0.05\%$  at  $1000^\circ\text{C}$ .





# Tube Materials

## ➤ High-purity quartz tube

- Pros:
  - Stability at high temperature;
  - Basic cleanliness.
- Cons:
  - Fragility;
  - Some metallic ions;
  - Not a sodium barrier;
  - Small flakes at  $> 1200^{\circ}\text{C}$ .

## ➤ Silicon carbide tube

- Pros:
  - Higher thermal tolerance;
  - Better metallic ion barrier;
  - Improved adhesion of deposited thin film to the tube wall (for LPCVD).
- Cons:
  - Heavier;
  - Much more expensive.

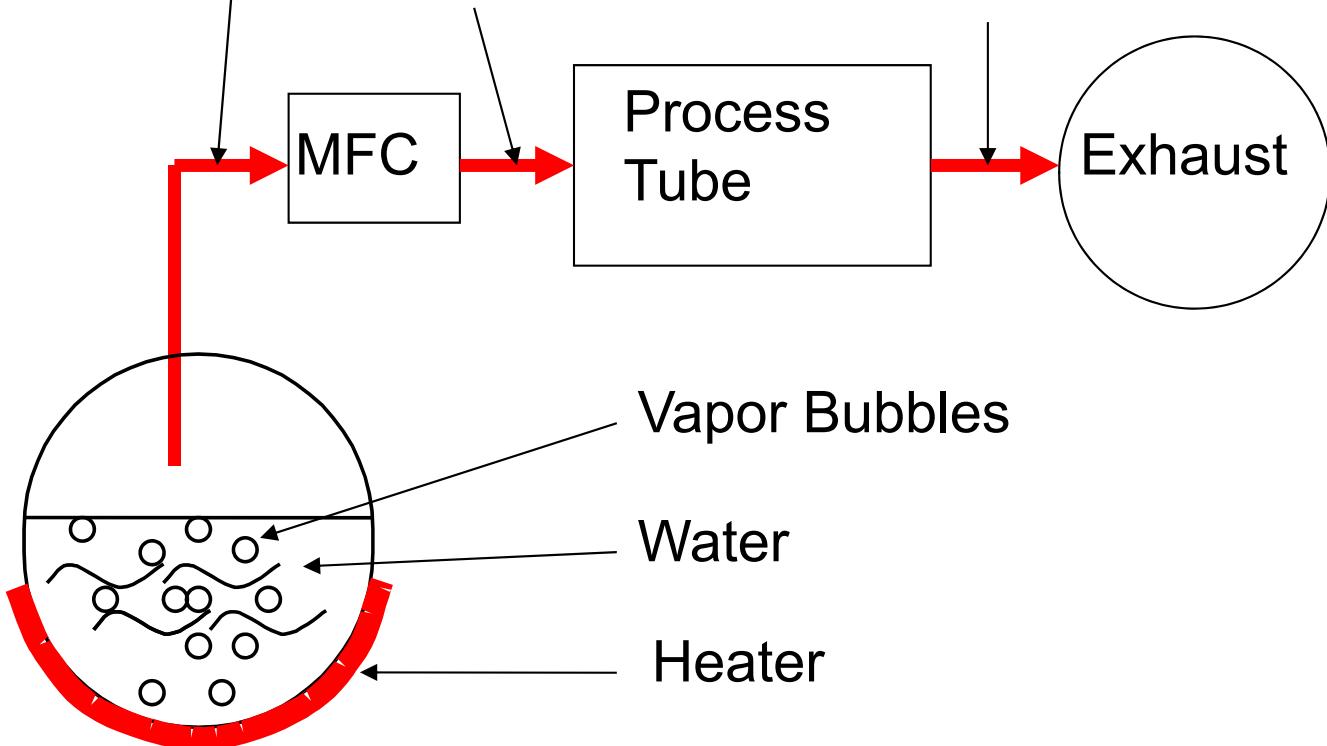


# Water Vapor Sources for Wet Oxidation

- Boiler
- Bubbler
- Flush
- Pyrogenic

## Boiling System

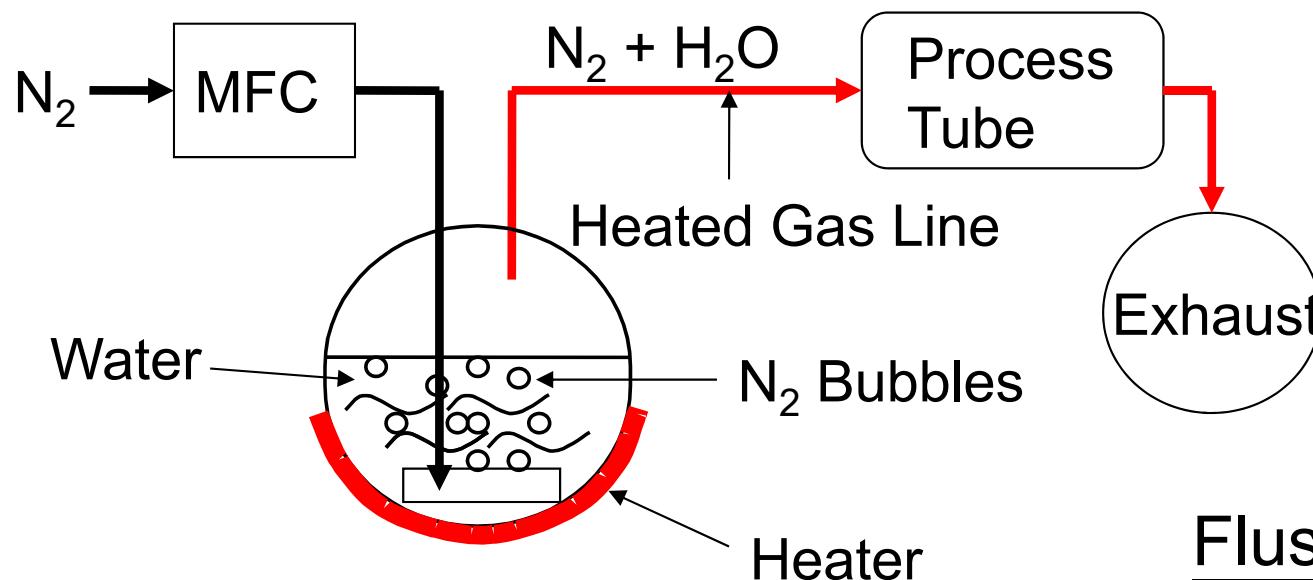
Heated Gas line                          Heated Fore line



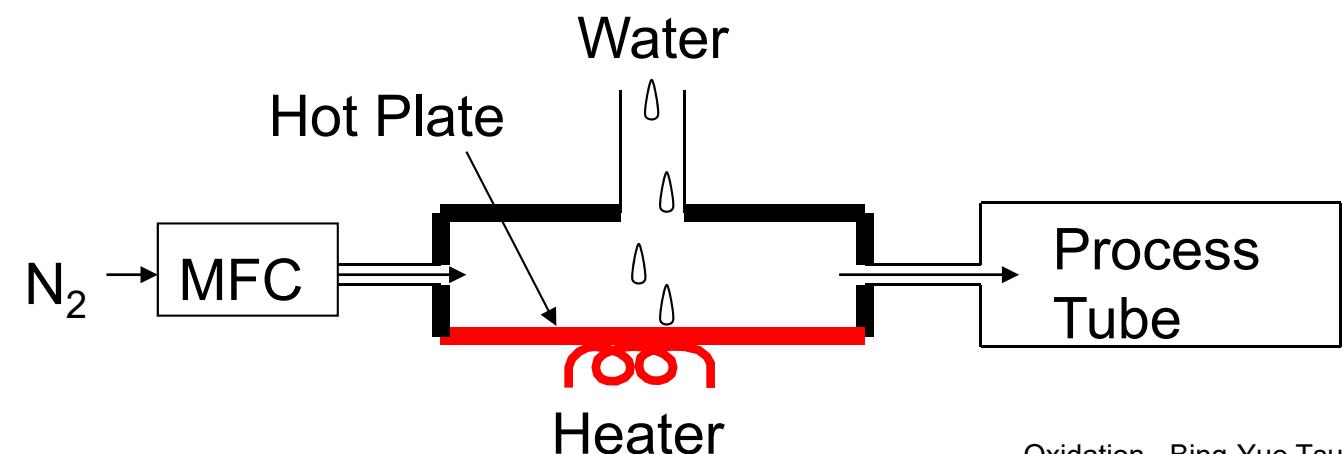


# Water Vapor Sources for Wet Oxidation

## Bubbler System



## Flush System





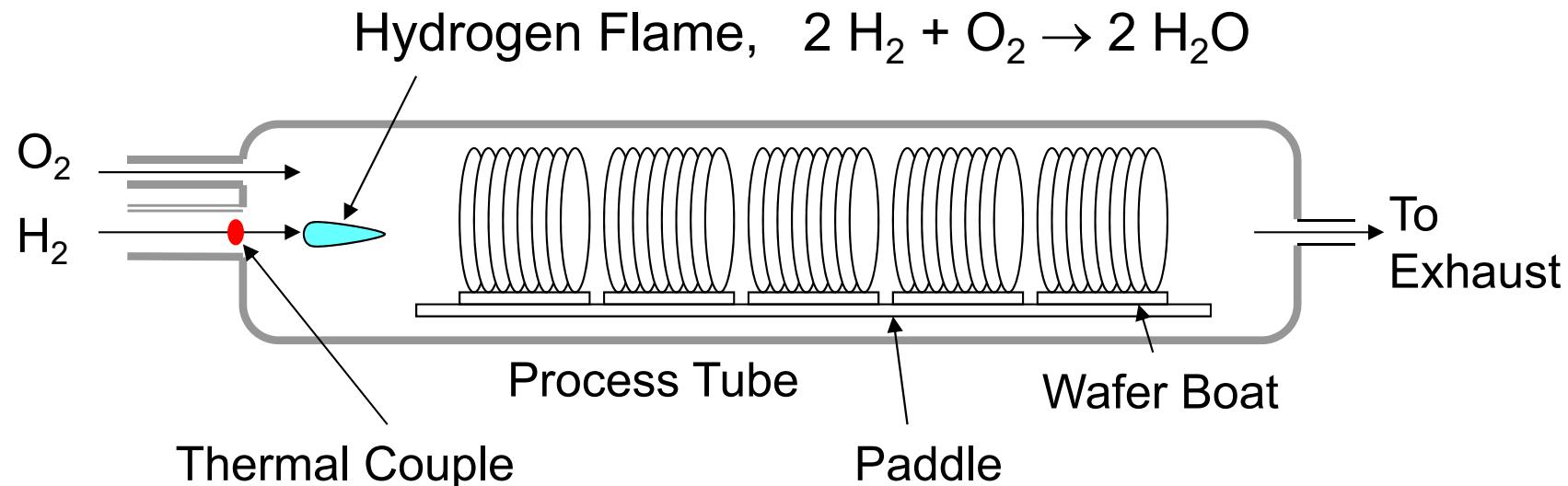
# Pyrogenic System

## ➤ Advantages:

- All gas system.
- Precise control of flow rates.

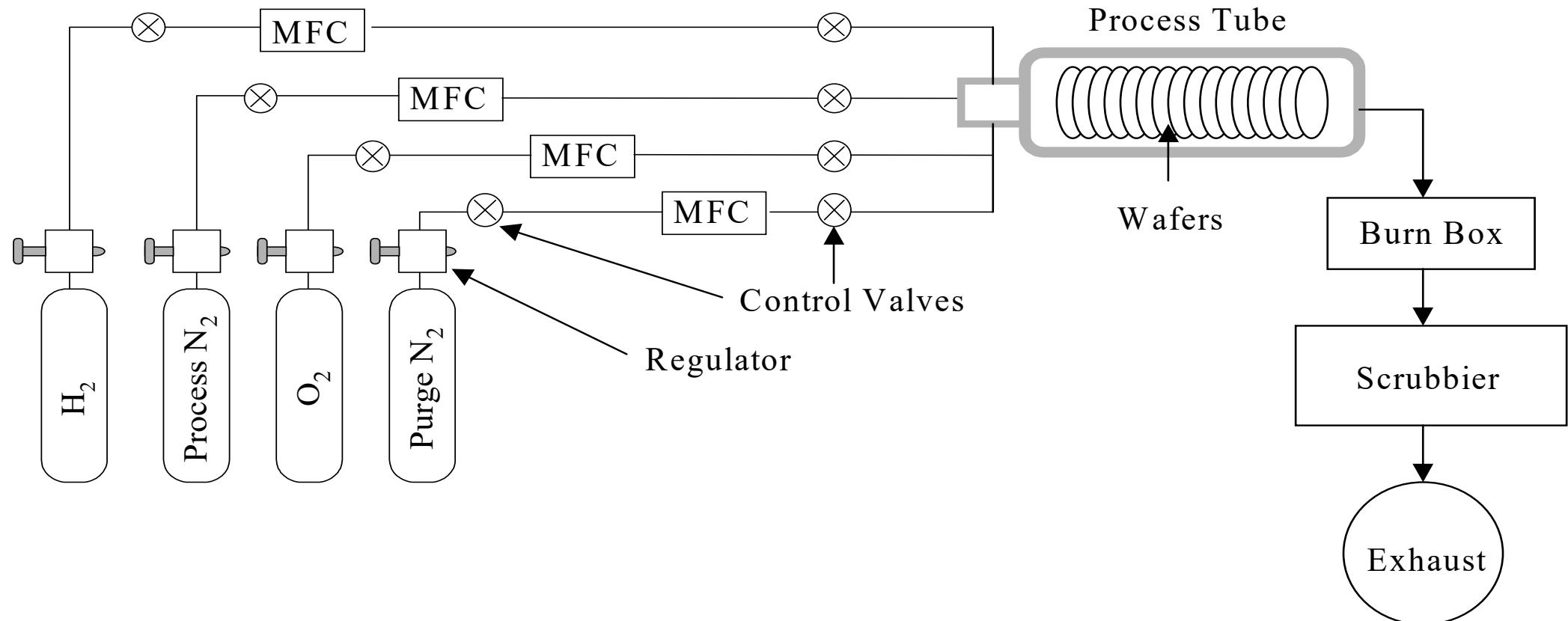
## ➤ Disadvantage:

- Introducing of flammable, explosive hydrogen.
- Typical H<sub>2</sub>:O<sub>2</sub> ratio is between 1.8:1 to 1.9:1.





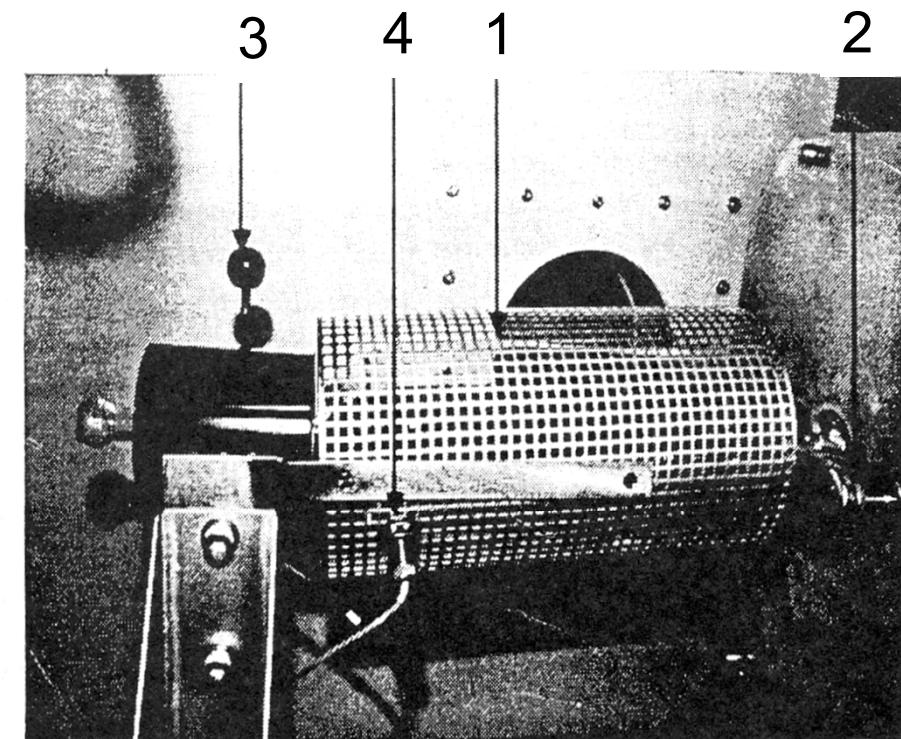
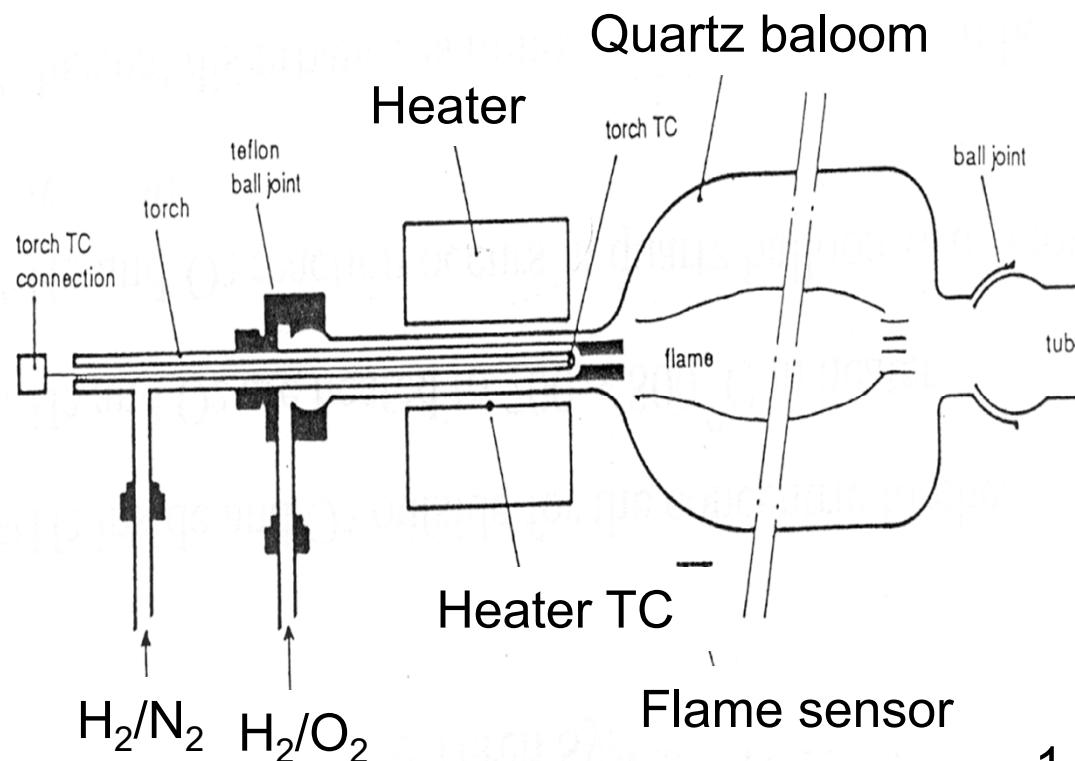
# Pyrogenic Wet Oxidation System





# Outside Torch System (OTS)

## An example for pyrogenic source

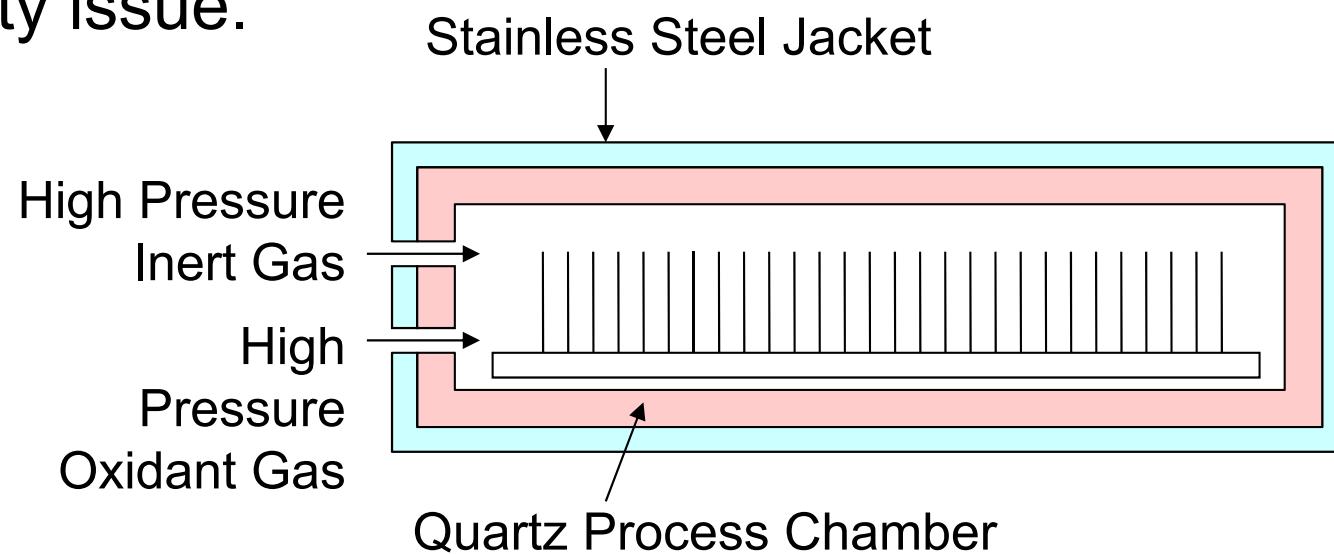


1. Protective cage.
2. Ball joint clamp, connection to process tube
3. Lever for opening OTS heater.
4. UV Flame sensor.



# High Pressure Oxidation System

- Not widely used in IC production because of system complexity and safety issue.



Time to grow  $1\mu\text{m}$  wet oxide

Temperature	Pressure	Time
1000 °C	1 atm	5 hours
1000 °C	5 atm	1 hour
1000 °C	25 atm	12 minutes



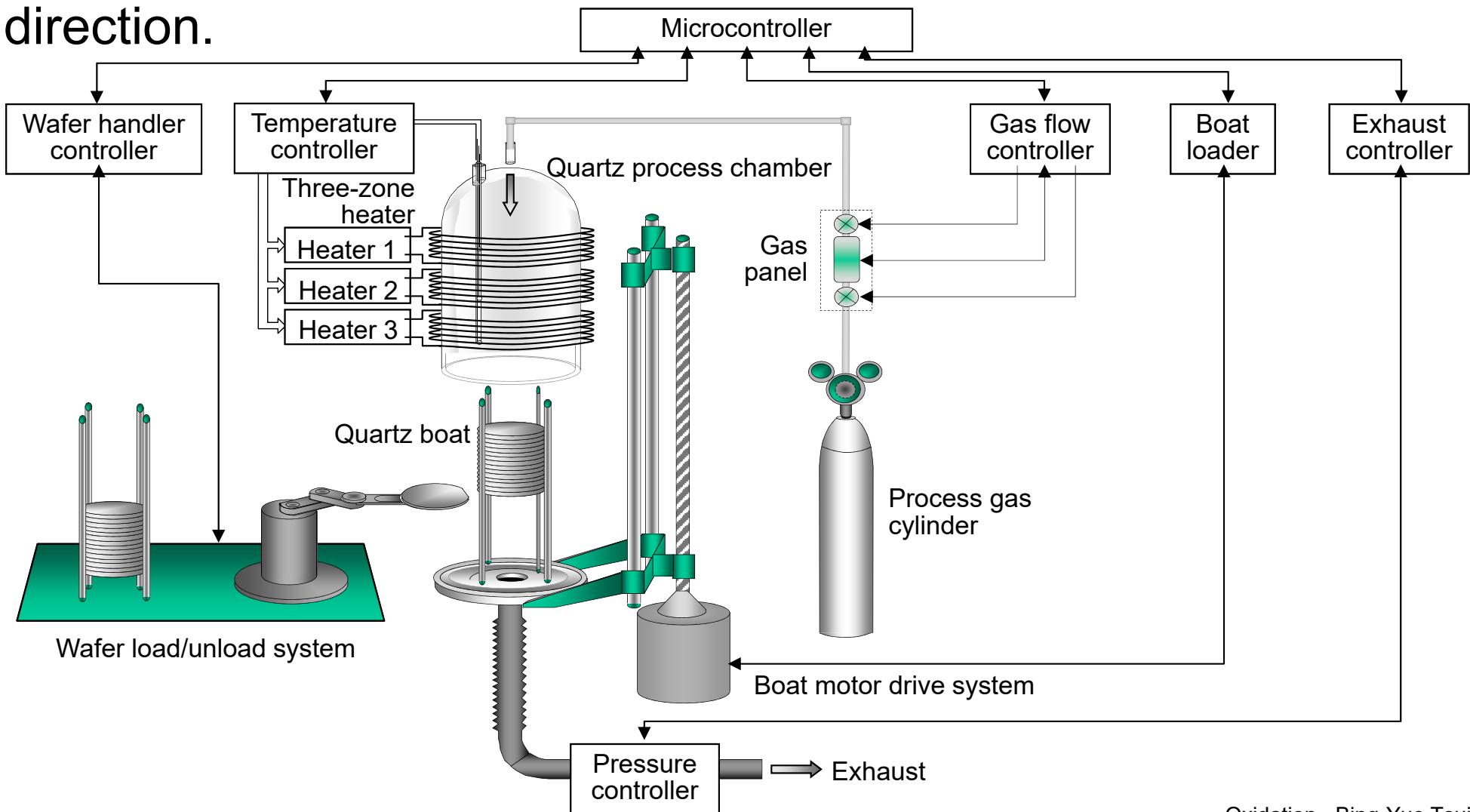
# Why Vertical Furnace ?

- Better contamination control with mini-environment capability.
- Better wafer handling with automatic loading and unloading procedure.
- Suitable for cluster tool development.
- Higher throughput with parallel processing capability
- Uniformity improved by better control over gas flow dynamics and wafer rotation.
- Lower maintenance cost and higher uptime.
- Smaller footprint (reduced cost of ownership (COO)).



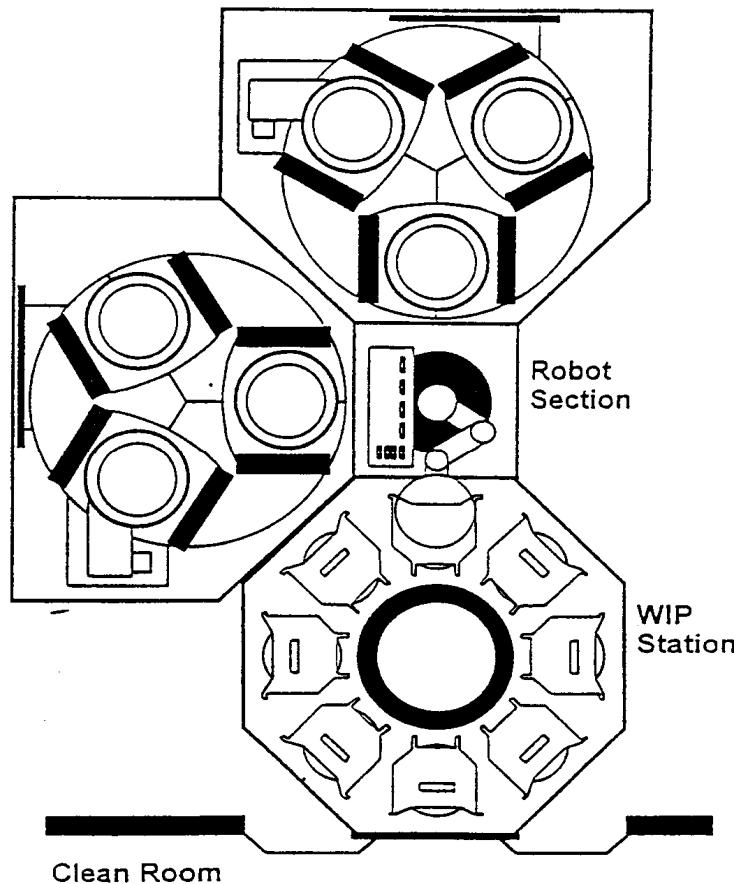
# Vertical Furnace

- Introduced in 1990s. Place the process tube in vertical direction.

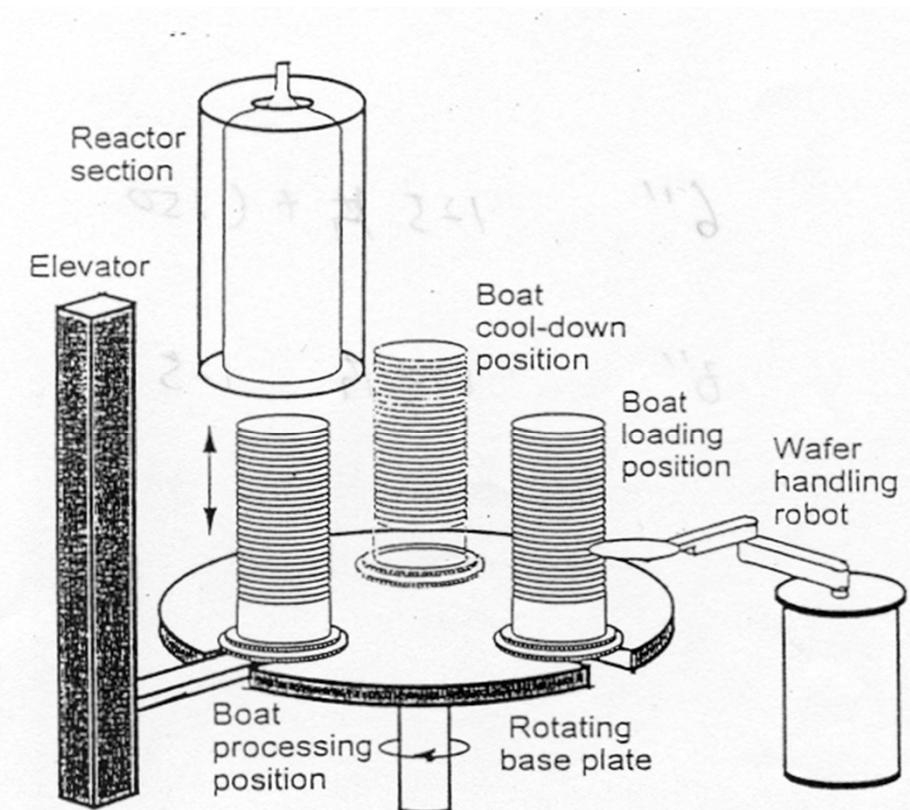




# ASM A-400 System



Top view

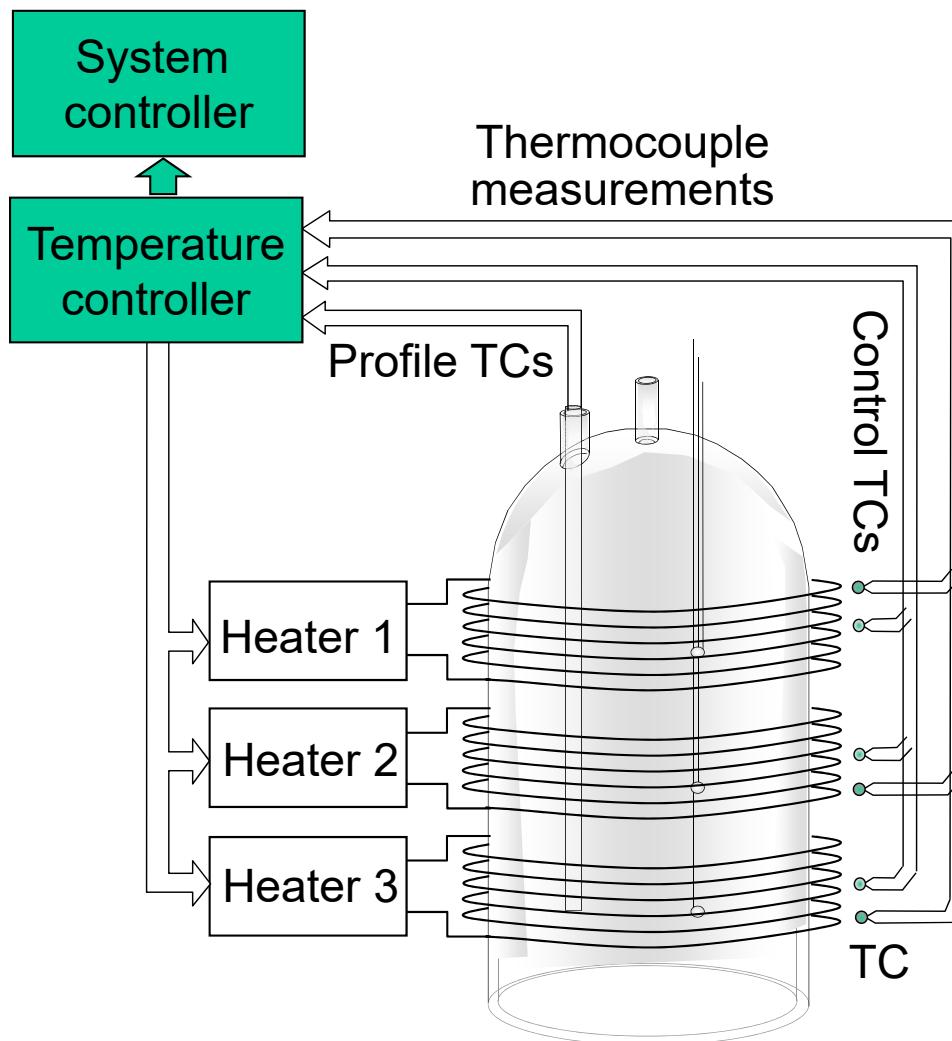


Side view

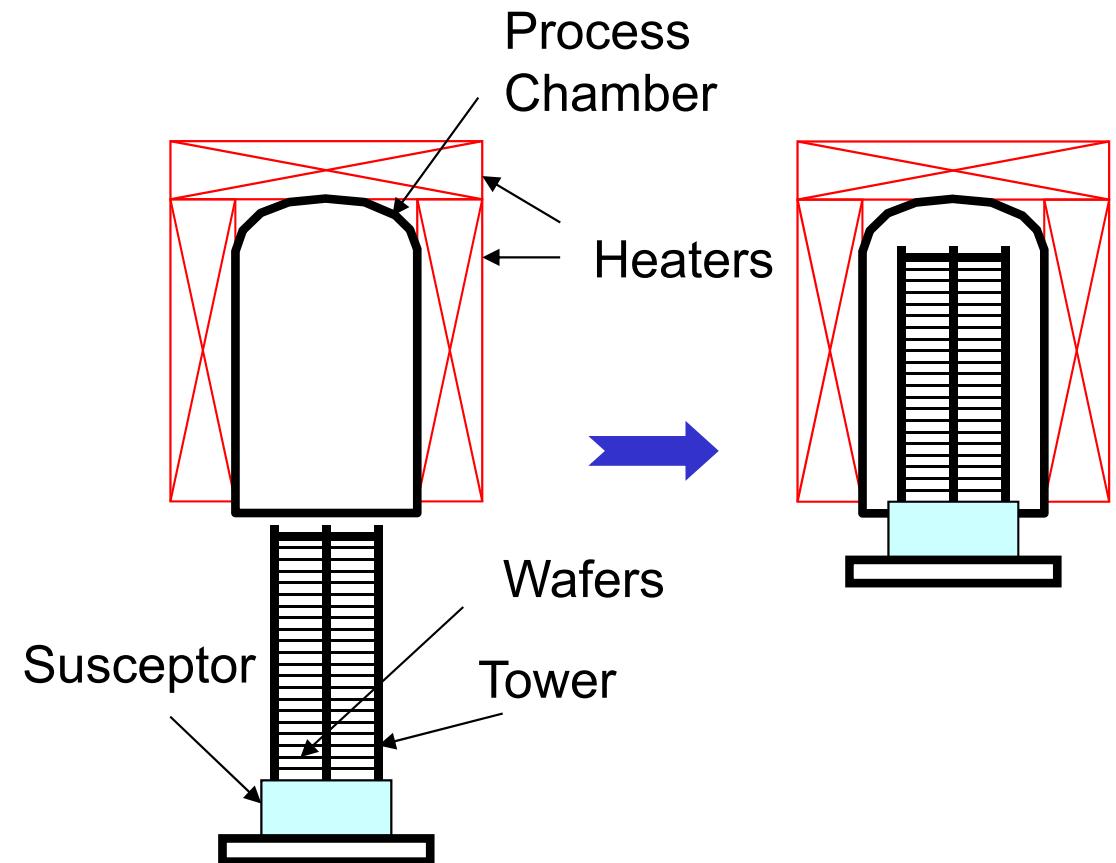


# ASM A-400 System

## Heating system

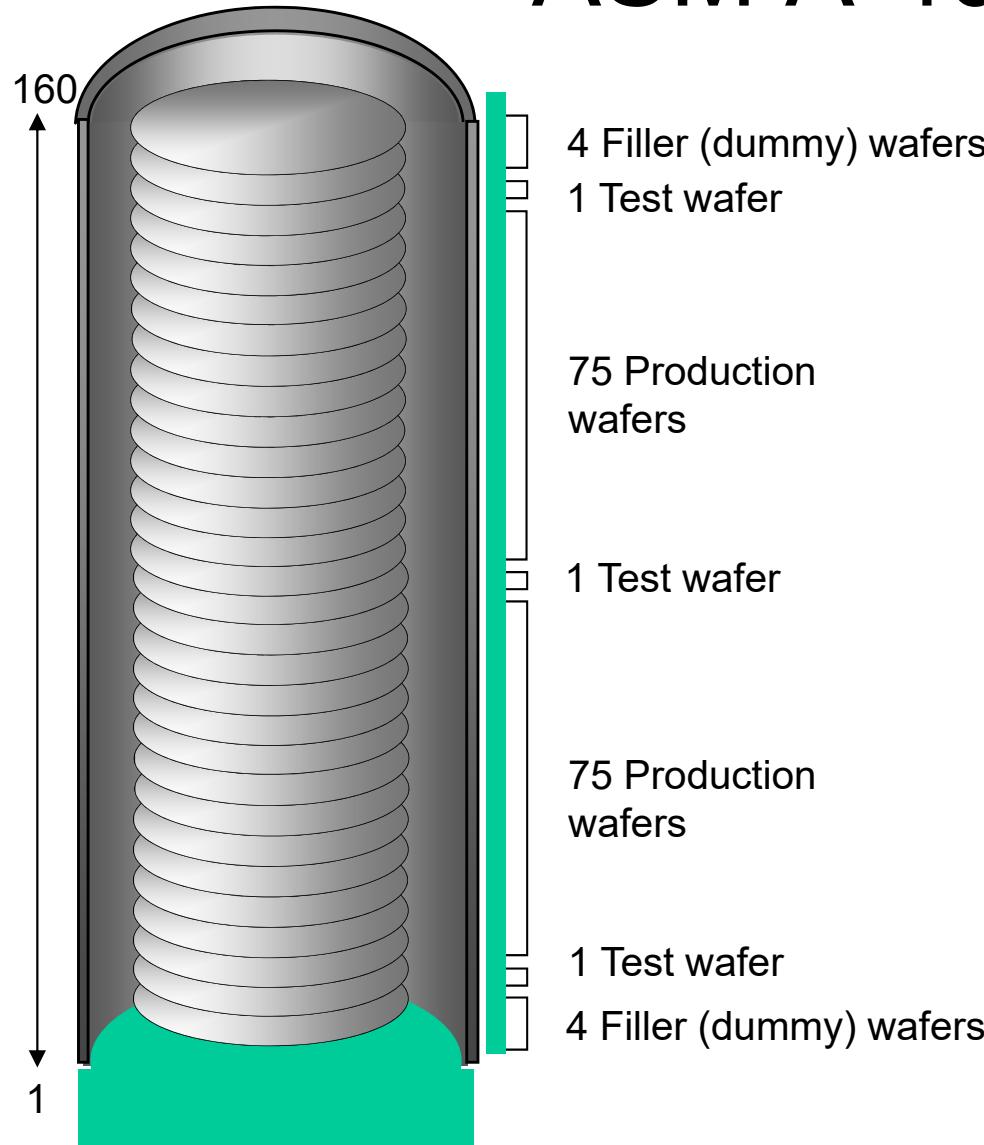


## Loading and Unloading Position





# ASM A-400 System



## Features

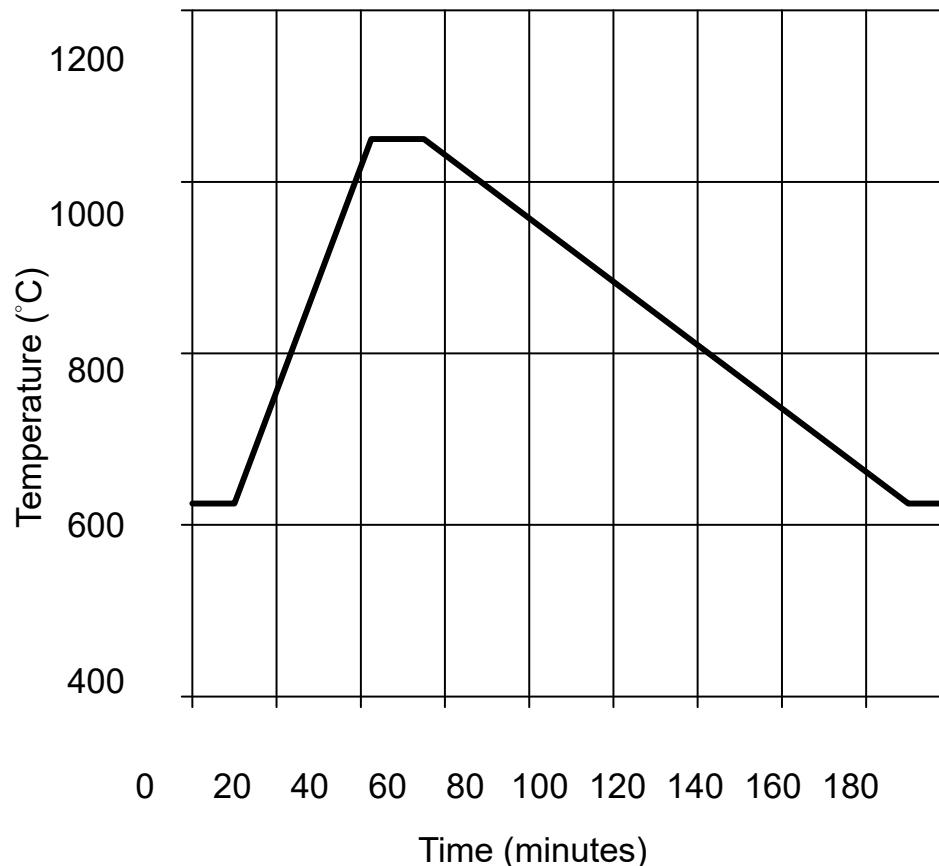
- Boat size: 160 wafers
- Boat pitch: 0.14 inch
- Wafer size: 8 inches
- Elevator speed: 9.29 cm/min
- Cool down delay: 20 minutes



# Fast Ramp Vertical Furnace

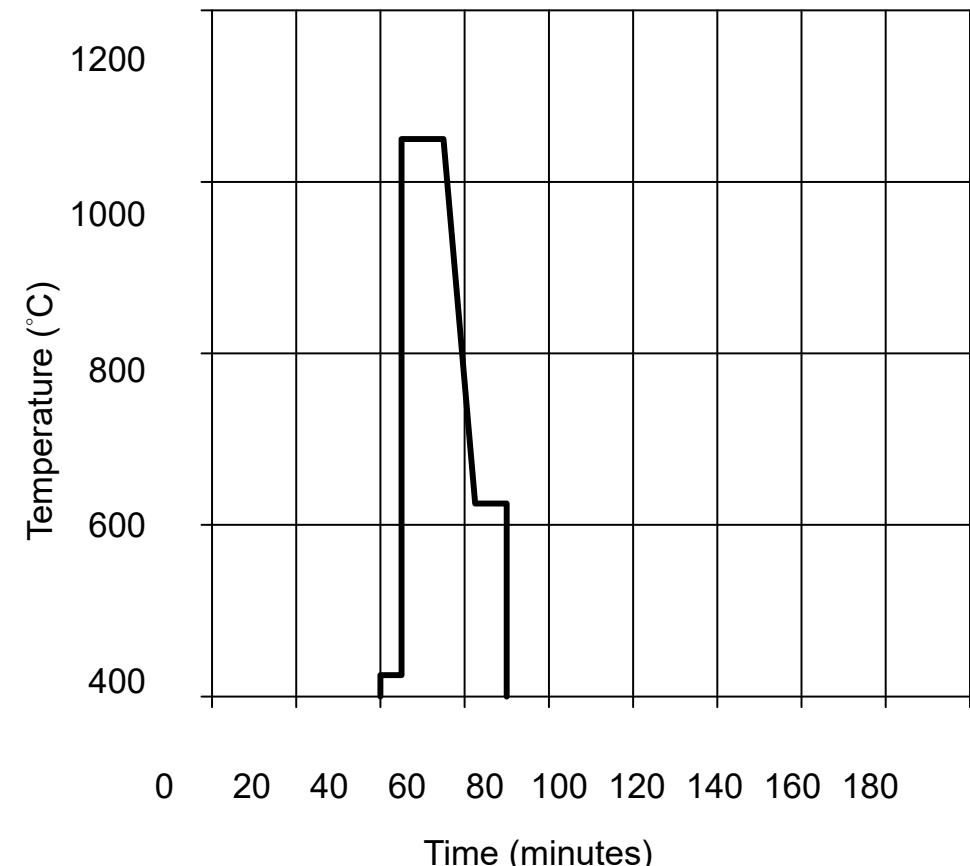
Solid State Technology (June 1996)

## Conventional



Ramp-up rate  $\sim 10$  °C/min  
Cooling rate  $\sim 4$  °C/min

## Fast Ramp



Ramp-up rate  $\sim 100$  °C/min  
Cooling rate  $\sim 60$  °C/min



# Horizontal versus Vertical Furnaces

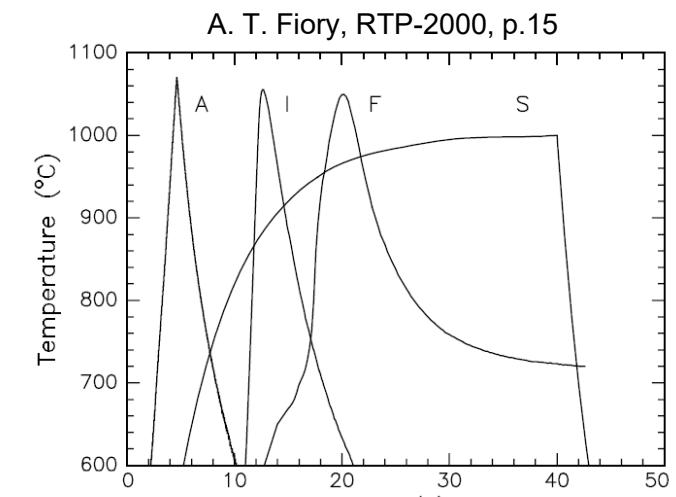
Performance Factor	Performance Objective	Horizontal Furnace	Vertical Furnace
Typical wafer loading size	Small, for process flexibility	200 wafers/batch	100 wafers/batch
Clean room footprint	Small, to use less space	Larger, but has 4 process tubes	Smaller (single process tube)
Parallel processing	Ideal for process flexibility	Not capable	Capable of loading/unloading wafers during process, which increases throughput
Gas flow dynamics (GFD)	Optimize for uniformity	Worse due to paddle and boat hardware. Bouyancy and gravity effects cause non-uniform radial gas distribution.	Superior GFD and symmetric/uniform gas distribution
Boat rotation for improved film uniformity	Ideal condition	Impossible to design	Easy to include
Temperature gradient across wafer	Ideally small	Large, due to radiant shadow of paddle	Small
Particle control during loading/unloading	Minimum particles	Relatively poor	Improved particle control from top-down loading scheme
Quartz change	Easily done in short time	More involved and slow	Easier and quicker, leading to reduced downtime
Wafer loading technique	Ideally automated	Difficult to automate in a successful fashion	Easily automated with robotics
Pre-and post-process control of furnace ambient	Control is desirable	Relatively difficult to control	Excellent control, with options of either vacuum or neutral ambient



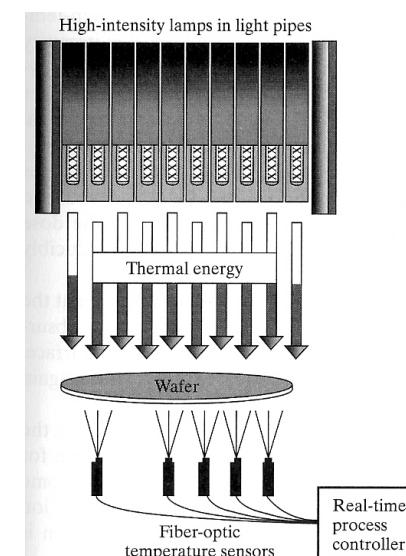
# Rapid Thermal Oxidation (RTO)

## ➤ Optical illumination

- Tungsten Halogen Bulbs: As tungsten filament gets hot, the W evaporates and begins to coat the glass. The halogen species forms volatile W-halogen compounds that diffuse back to the hot filament, break apart and redeposit the W. Thus, longer bulb life is obtained.
- Arc Noble Gas Discharge Lamps: A fused silica tube containing a noble gas (or mixtures) is ignited with a high voltage pulse to ionize the gas. Once ionized the bulb can carry a huge DC current. The effect is a very intense light source with very high color temperature and additional discrete gas line spectra superimposed on the radiant exitance. Low melting point metals such as Hg are also used to increase output power in certain desired wavelengths.



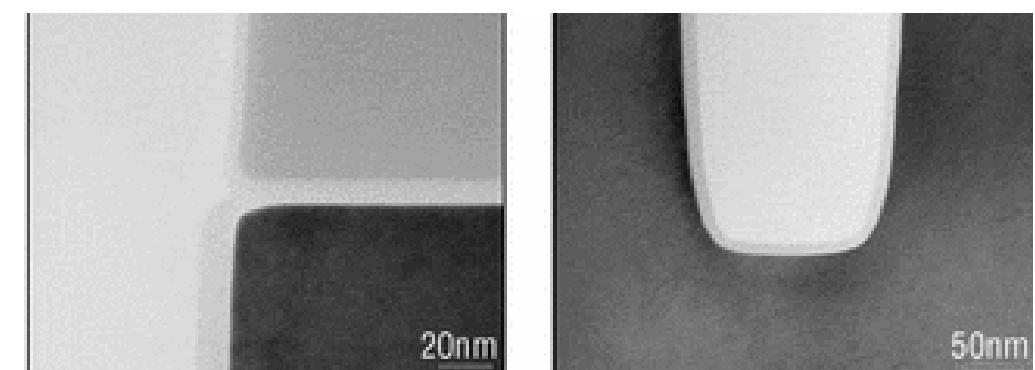
A: arc lamp; I: incandescent lamp;  
F: bell-jar furnace; S: susceptor furnace.





# In-Situ Steam Generation (ISSG)

- ISSG oxidation is a low-pressure process performed in a cold-wall RTP reactor.
  - The main characteristic of the process is the introduction of H<sub>2</sub> and O<sub>2</sub> gases directly in the chamber without pre-combustion.
  - The hot wafer acting as an ignition source, gases react in situ to give primary species including hydroxyl groups -OH and atomic oxygen O\*.
  - Low pressure processes are diffusion-limited
- Example:
  - Pressure ~ 10 Torr.
  - Oxidation temperature 900 ~ 1150 °C
  - H<sub>2</sub>:O<sub>2</sub> dilution rate ~ 30%.

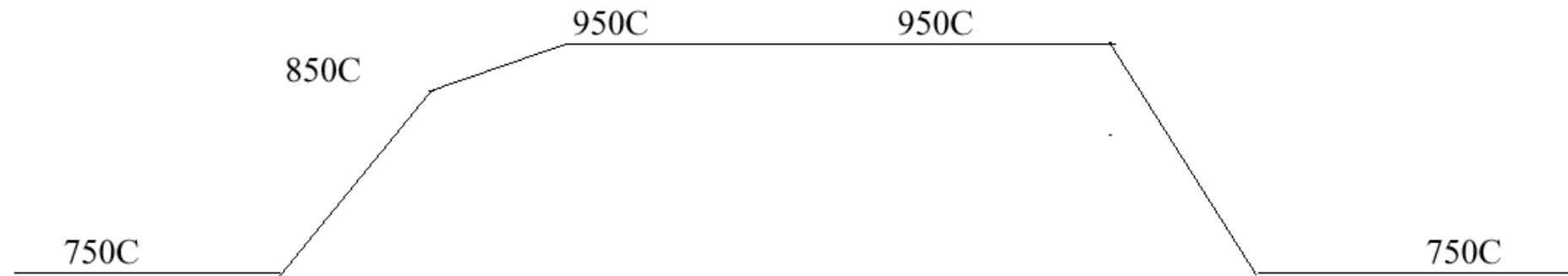


Solid State Technology May, 2003



# Furnace Oxidation Recipe

Dry oxidation recipe:  $25 \pm 2$  nm

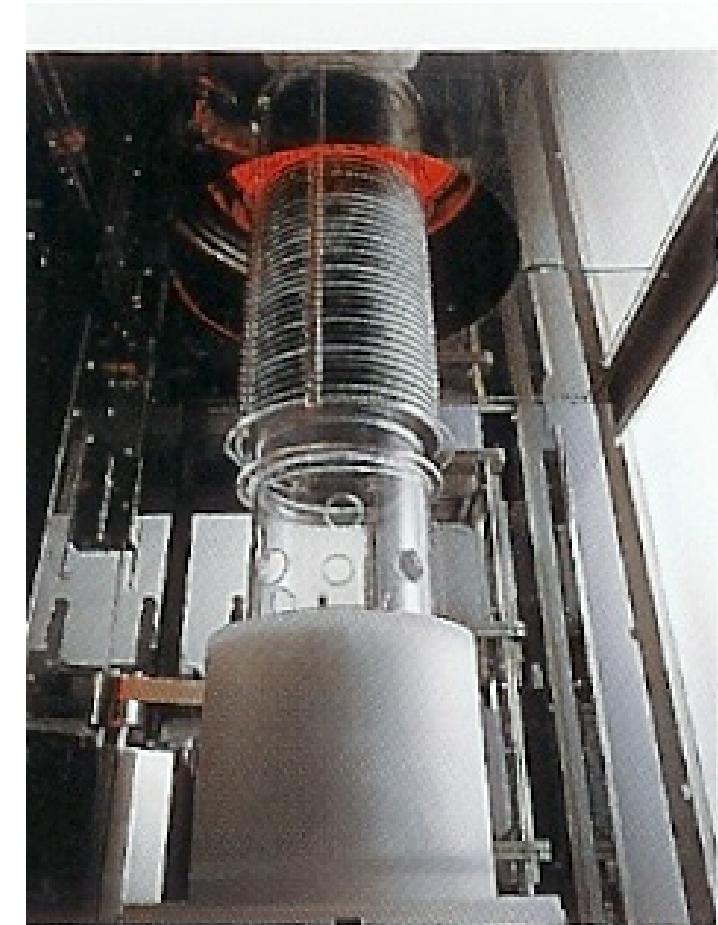


step	0	1	2	3	4	5	6	7	8	9	10	11
time		A:1hr	P*	P*	5'	7'	24'	5'	10'	P*	1hr	10'
N2 flow (L)	5	10	10	10	10				10	10	10	10
O2 flow (L)						15	15	15				
H2 flow (L)												
HCL flow (L)							0.11					
LO2 flow (L)	0.1	0.1	0.1	0.1								
boat		in									out	end
remark			10C/min	5C/min					3C/min			



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# Oxidation Furnaces





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# Scale Down Issues



# Carrier Injection

## ➤ Tunneling Mechanism

- Schottky Emission
- Fowler-Nordheim Tunneling or Field Emission
- Frenkel-Pool Emission
- Direct Tunneling
- Ionic Conduction
- Space Charge Limited
- Ohmic

$$J = A^* T^2 \exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_I})}{kT}\right] \sim T^2 \exp\left(\frac{+a\sqrt{V}}{T} - \frac{q\phi_B}{kT}\right)$$

$$J = E^2 \exp\left[\frac{-4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q E}\right] \sim V^2 \exp\left(-\frac{b}{V}\right)$$

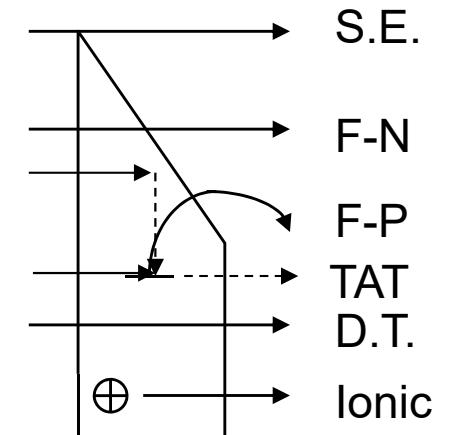
$$J = E \exp\left[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_I})}{kT}\right] \sim V \exp\left(\frac{+2a\sqrt{V}}{T} - \frac{q\phi_B}{kT}\right)$$

$$J = \frac{BE_{ox}^2}{\left[1 - (\phi_s - qV_{ox}/\phi_s)^{1/2}\right]^p} \exp\left[-\frac{C}{E_{ox}} \frac{\phi_s^{3/2} - (\phi_s - qV_{ox})^{3/2}}{\phi_s^{3/2}}\right]$$

$$J = \frac{E}{T} \exp\left[\frac{-\Delta E_a}{kT}\right] \sim \frac{V}{T} \exp\left(-\frac{c}{T}\right)$$

$$J = \zeta \frac{\varepsilon}{4\pi} \frac{\mu V^2}{L^3} \sim V^2$$

$$J = E \exp\left[\frac{-\Delta E_a}{kT}\right] \sim V \exp\left(-\frac{c'}{T}\right)$$





# Issues of Thin Oxide - 1

## ➤ Direct tunneling current

$$J_{DT} = \frac{BE_{ox}^2}{\left[1 - \left(\frac{\phi_s - qV_{ox}}{\phi_s}\right)^{1/2}\right]^2} \exp\left[-\frac{C}{E_{ox}} \frac{\phi_s^{3/2} - (\phi_s - qV_{ox})^{3/2}}{\phi_s^{3/2}}\right]$$

$$B = \frac{q^3}{16\pi^2 \phi_s}$$

$$C = \frac{4(2m_{ox})^{1/2}}{3q} \phi_s^{3/2}$$

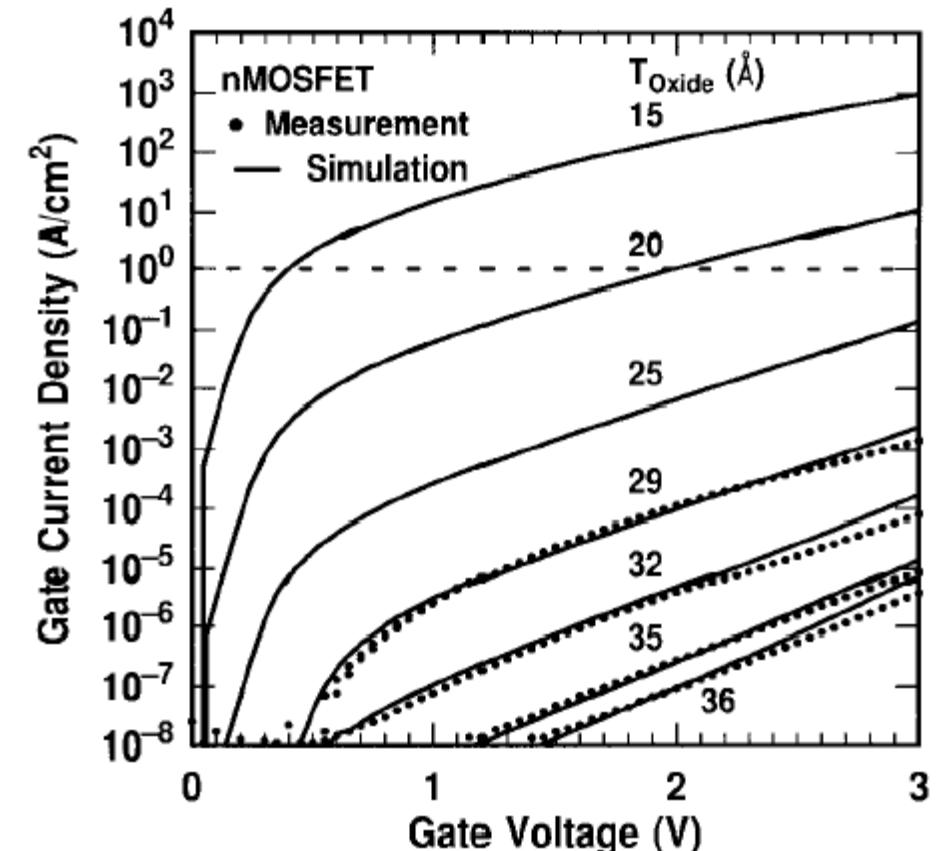
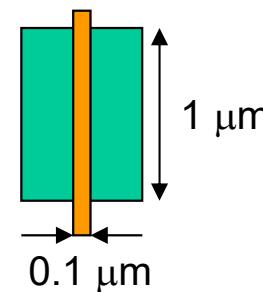
## ➤ Maximum tolerable $I_{gate} < I_{off}$

$$I_{gate} < I_{off} \approx 1nA/\mu m$$

$$\text{As } L_{gate} = 0.1 \mu m$$

$$I_{gate} = (1nA/\mu m) / (0.1 \mu m)$$

$$= 1 A/cm^2$$





# Issues of Thin Oxide - 2

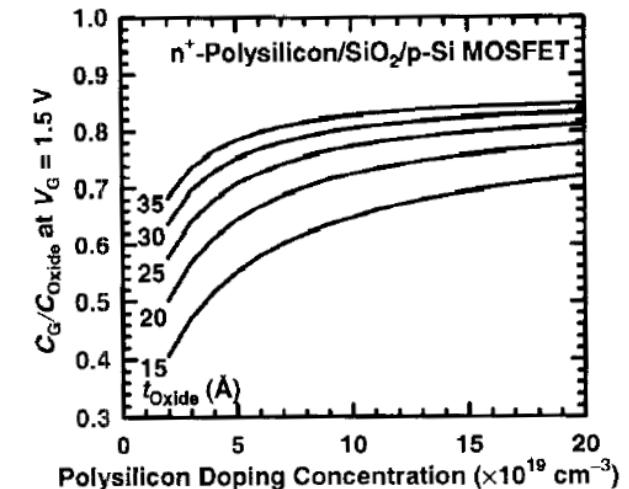
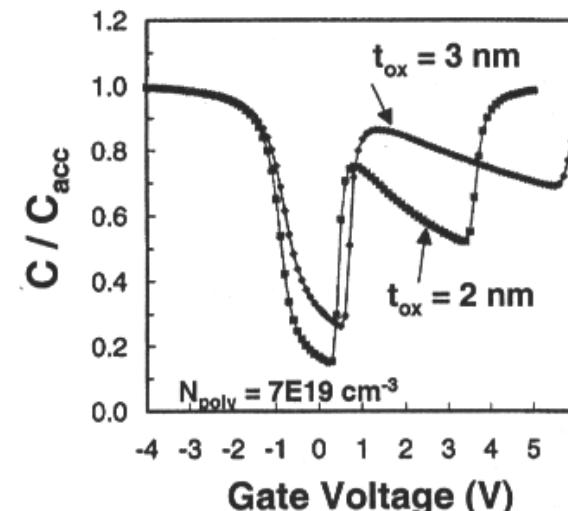
## ➤ Poly-Si depletion

$$V_g = V_{fb} + V_{Si} + V_{ox} + V_{poly}$$

$$V_{poly} \propto \frac{Q_{Si}^2}{N_{poly}}$$

$$T_{ox,inv}^2 = T_{ox,acc}^2 + \frac{2\epsilon_{ox}^2 V_g}{q\epsilon_{Si} N_{poly}}$$

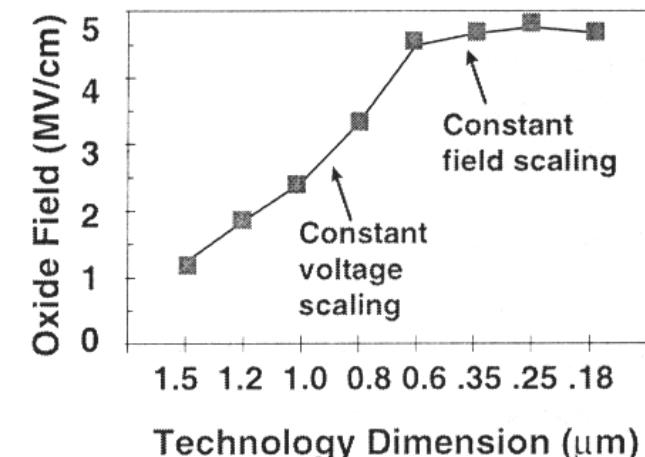
M. Rodder, IEDM p. 879, 1993



## ➤ Influence

- Constant field & constant  $N_{poly}$   
=> constant  $V_{poly}$
- An 0.3-0.5 nm thick CET loss is inevitable.

$$CET = \frac{\epsilon_{ox} \epsilon_o A}{C_{meas}}$$





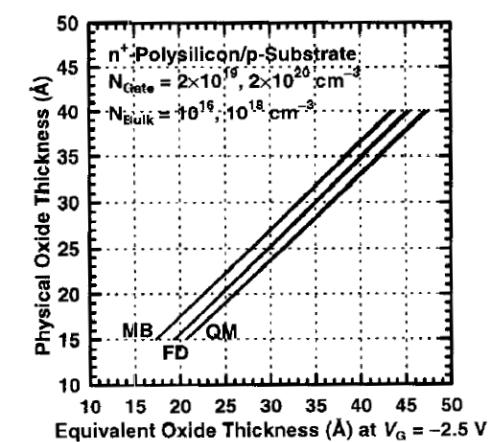
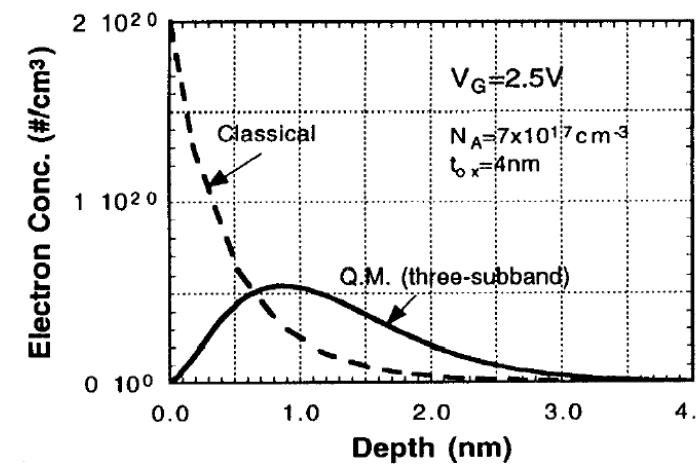
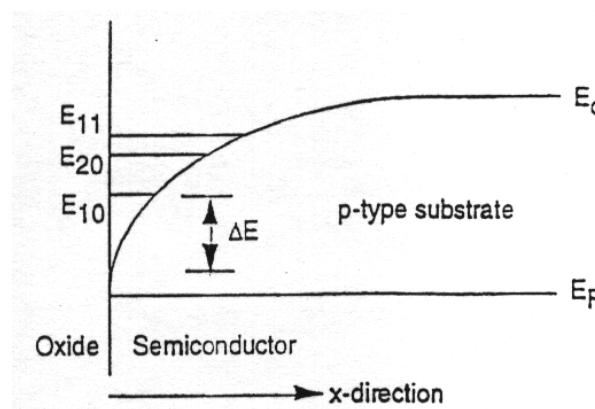
# Issues of Thin Oxide - 3

## ➤ Quantum effect

- Because of the conduction band triangular like well at the surface, electron states are a series of discrete levels above the edge of the conduction band.
- The surface potential is larger than classical predicted.
- Charge is located 0.5-1.0 nm away from surface than classical predicted.

## ➤ Consequences

- A 0.3 nm increase of CET.
- An increased depletion layer charge density.



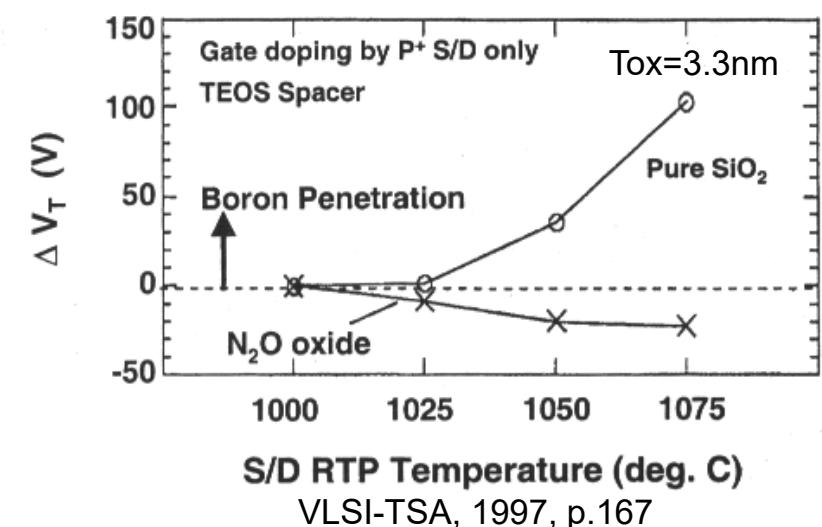
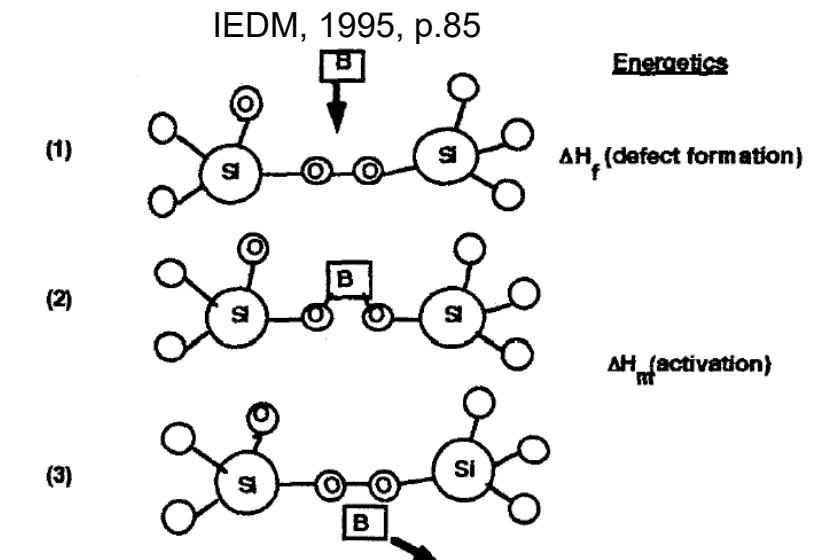


# Issues of Thin Oxide - 4

## ➤ Boron penetration

- Boron may diffuse through gate oxide from p<sup>+</sup> poly-Si gate of PMOSFET.
  - Positive flat-band voltage shift
  - Degradation of oxide wearout properties
- Thinner oxides result in severer boron penetration effect.
- Fluorine and hydrogen enhance boron diffusion.
- Crystallized a-Si retards boron diffusion.
- Nitrided oxides reduce boron diffusivity.

## ➤ Trade-off between boron penetration and poly depletion



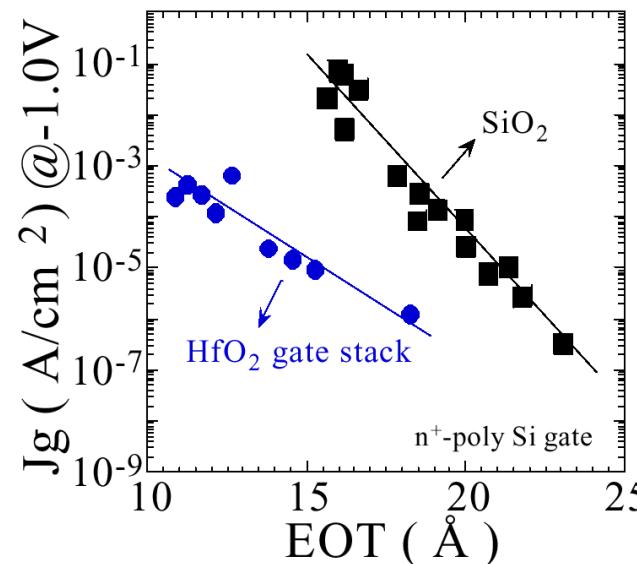


# Advantages of High K Dielectric

- Thicker physical thickness

$$T_{HK} = \frac{\epsilon_{HK}}{\epsilon_{SiO_2}} T_{SiO_2}$$

- Thinner effective oxide thickness (EOT)
- Lower tunneling current



Legend:

- ☒ = Not a solid at 1000 K
- ☢ = Radioactive
- ① = Failed reaction 1:  $Si + MO_x \rightarrow M + SiO_2$
- ② = Failed reaction 2:  $Si + MO_x \rightarrow MSi_x + SiO_2$
- ⑥ = Failed reaction 6:  $Si + MO_x \rightarrow M + MSi_xO_y$

H	Li	Be	Mg	Al	Si	P	S	Cl	Ar									
B	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr		
C	Sr	Y	Zr	Nb	Ta	Mo	Tc	Pu	Rh	Pd	Ag	Tl	In	Sn	Sh	Te	I	Xe
N	Ca	↑	Hf	Ta	W	Re	Ds	Ir	Pt	Au	Hg	Hf	Pb	Hg	Pt	At	Rn	
O	Rb																	

Insufficient Thermodynamic Data to Complete Calculations

† La	Ce	Pr	Nd	钷	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
‡ Ac	Th	Pa	U	𬬻	𬬻	𬬻	𬬻	𬬻	𬬻	𬬻	𬬻	𬬻	𬬻	𬬻

Experimentally Demonstrated



# Requirement of High K Dielectric

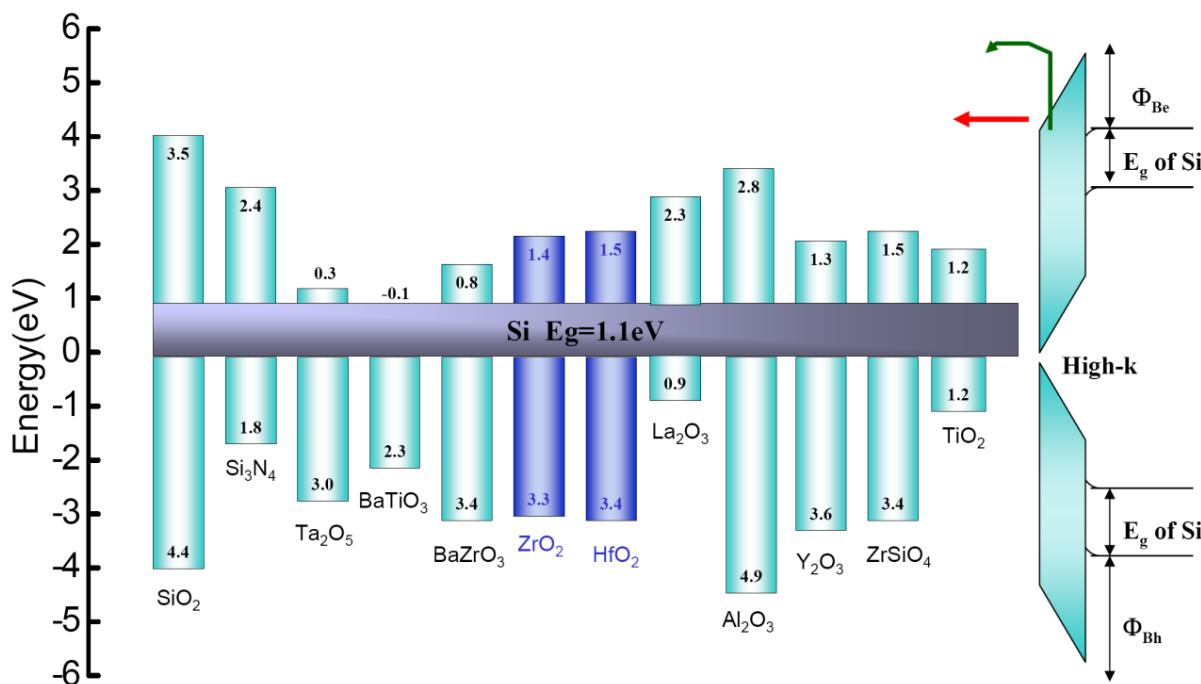
Criteria	Requirement
EOT scalability < 1 nm	Dielectric constant > 15
Negligible FIBL effect	Dielectric constant < 60
Leakage current < 1A/cm <sup>2</sup>	Band gap > 5eV Barrier height > 1eV
Thermal stability	No silicidation and reduction
Hysteresis	< 20mV
Frequency dispersion	<1% /dec. of frequency
Interface state density	<10 <sup>11</sup> 1/eV/cm <sup>2</sup>
Mobility	>85% of SiO <sub>2</sub>
Reliability	> 10 years



# Band Alignment Consideration

- Energy gap of dielectric depends on dielectric constant.

$$\text{Clausius - Mossotti Equation: } E_g \approx 20 \left( \frac{3}{\epsilon + 2} \right)^2$$



Oxide	Dielectric Constant
$\text{SiO}_2$	3.9
$\text{Si}_3\text{N}_4$	7-9
$\text{HfO}_2$	~30
$\text{ZrO}_2$	~25
$\text{Al}_2\text{O}_3$	9-13
$\text{Y}_2\text{O}_3$	11-17
$\text{Ta}_2\text{O}_5$	25-45
$\text{La}_2\text{O}_3$	21

• J. Robertson, Journal of Vacuum Science & Technology B, vol. 18, p. 1785, 2000.

• G.D. Wilk, J. Appl. Phys., Vol., 89, No. 10, 2001, p. 5254



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# Metrology



# Metrology

## ➤ Direct inspection

- Color chart

## ➤ Optical methods

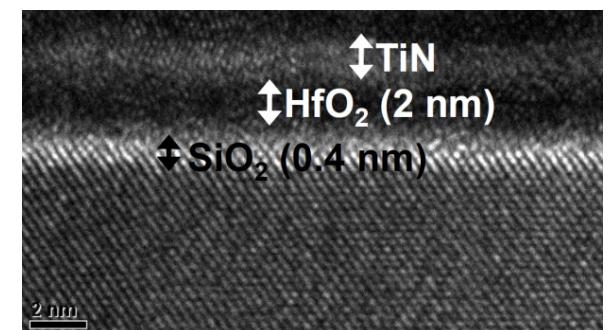
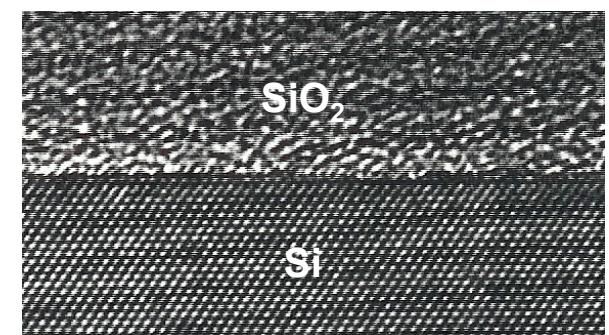
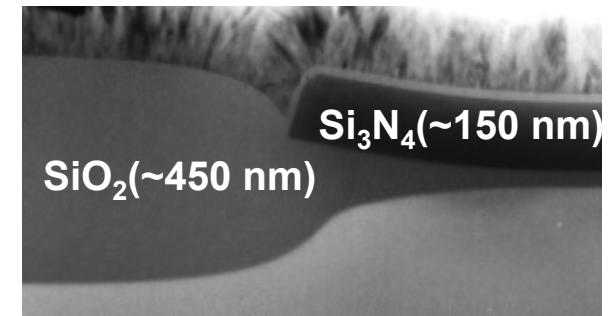
- Ellipsometer: thickness (T), refraction index (n), absorption index (k)

## ➤ Physical methods

- Scanning Electron Microscope (SEM) for thick layer ( $>10$  nm)
- Transmission Electron Microscope (TEM) for thin layer and interface ( $<10$  nm),
- Surface Profiler and Atomic Force Microscopy (AFM) for topography and surface roughness

## ➤ Electrical methods

- I-V, C-V, etc.





# Color Chart

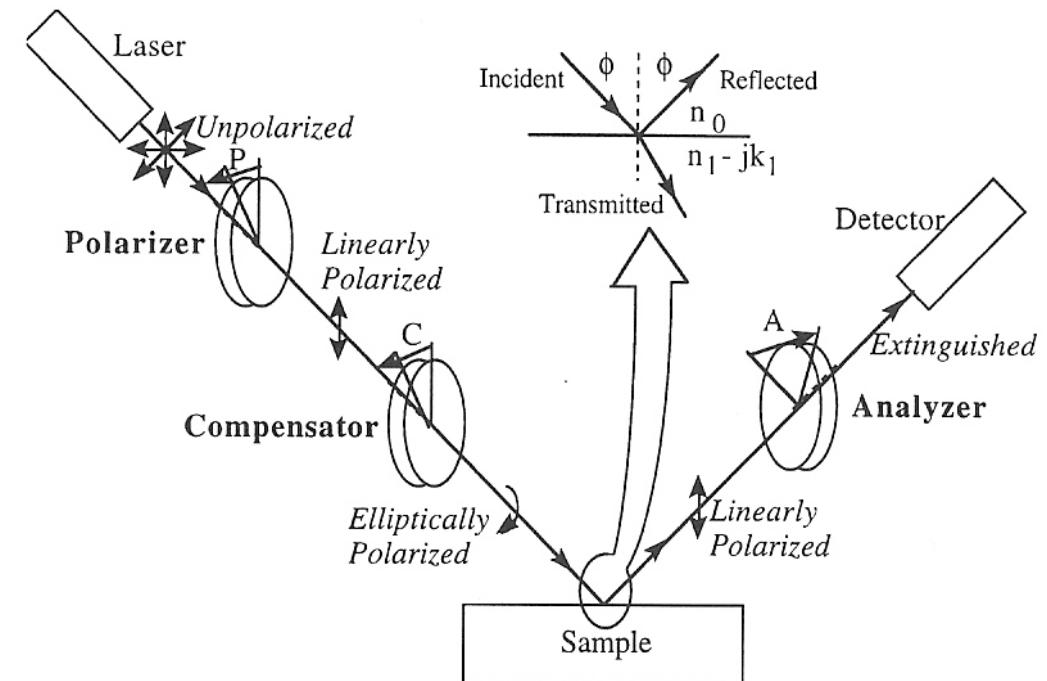
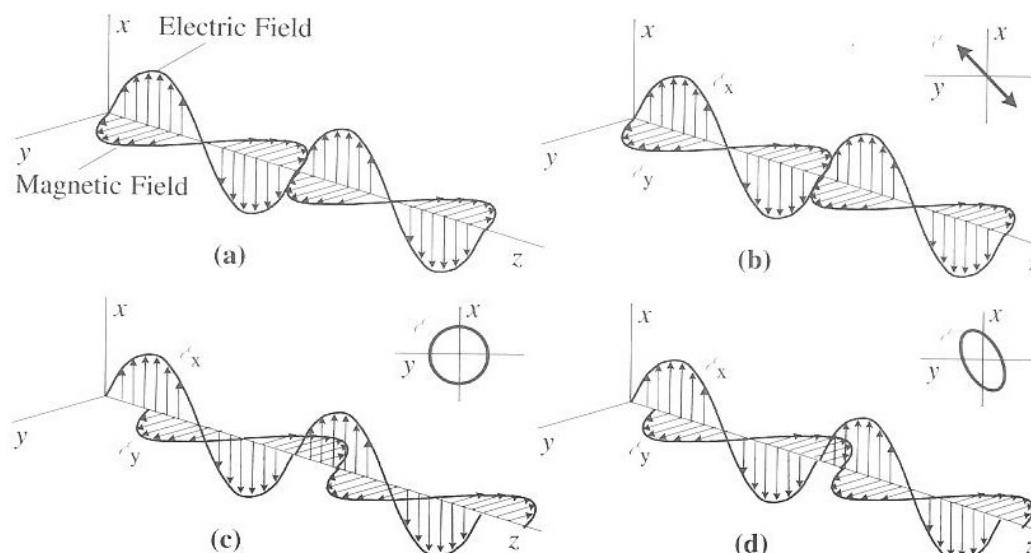
Thickness ( $\mu\text{m}$ )	Color and Comments	Thickness ( $\mu\text{m}$ )	Color and Comments
0.05	Tan	0.27	Red violet
0.07	Brown	0.30	Blue to violet blue
0.10	Dark violet to red violet	0.31	Blue
0.12	Royal blue	0.32	Blue to blue green
0.15	Light blue to metallic blue	0.34	Light green
0.17	Metallic to very light yellow green	0.35	Green to yellow green
0.20	Light gold or yellow; slightly metallic	0.36	Yellow green
0.22	Gold with slight yellow orange	0.37	Green yellow
0.25	Orange to melon	0.39	Yellow



# Ellipsometer - 1

## ➤ Elliptical polarization

- Compensator or retarder changes the linearly polarized light to elliptically polarized light.
- The compensator contains a fast and a slow optical axis perpendicular to the direction of transmission so that the component of electric field parallel to the slow axis is retarded.





# Ellipsometer -2

$$R_p = \frac{E_p(\text{reflected})}{E_p(\text{incident})}; R_s = \frac{E_s(\text{reflected})}{E_s(\text{incident})}$$

The complex reflection ratio  $\rho = \frac{R_p}{R_s} = \tan(\Phi)e^{j\Delta}$

The ellipsometric angles  $\Phi(0^\circ - 90^\circ)$  and  $\Delta(0^\circ - 360^\circ)$  are measurable.

$\Phi = f(\phi, \lambda, n_o, n_i, k_i, t_i, n_s, k_s)$  with all  $i \geq 1$

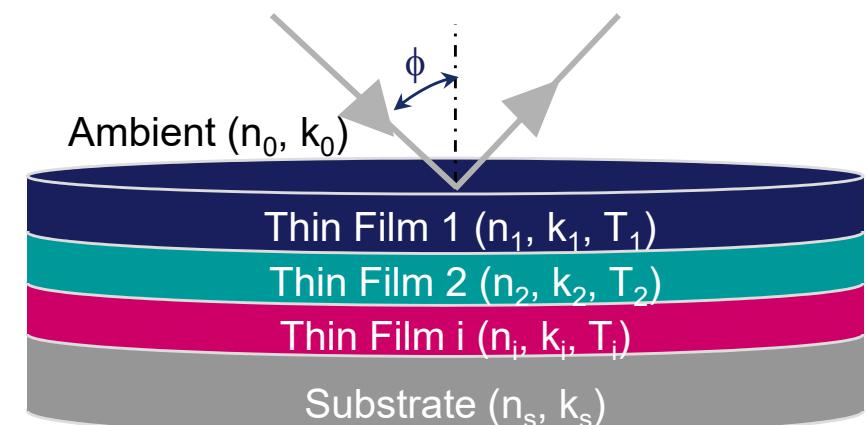
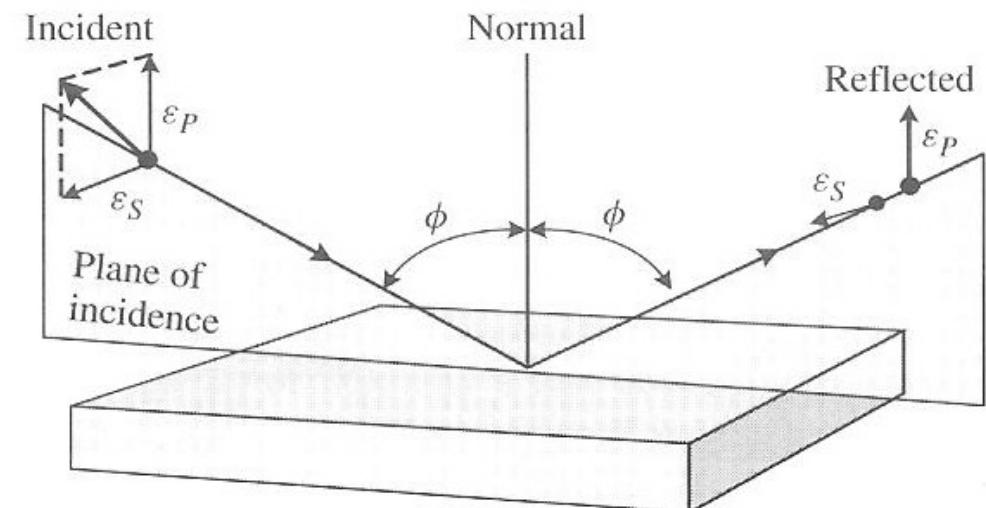
$\Delta = f(\phi, \lambda, n_o, n_i, k_i, t_i, n_s, k_s)$  with all  $i \geq 1$

$n_o$  the refraction index of air

$n_i$  the refraction index of the  $i$ th layer

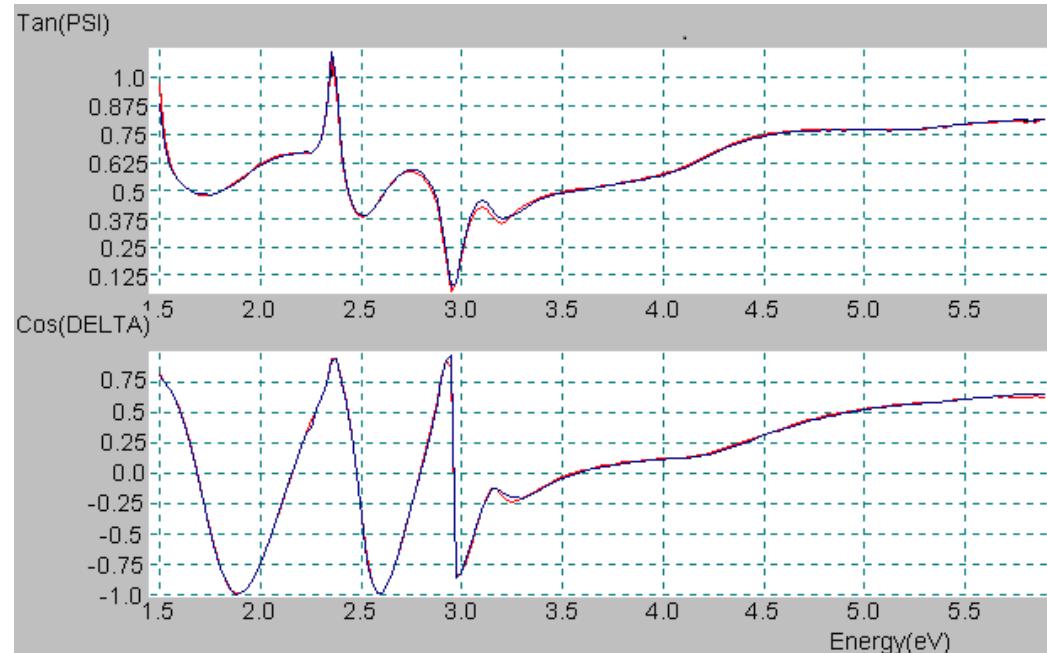
$k_i$  the absorption index of the  $i$ th layer

$t_i$  the thickness of the  $i$ th layer



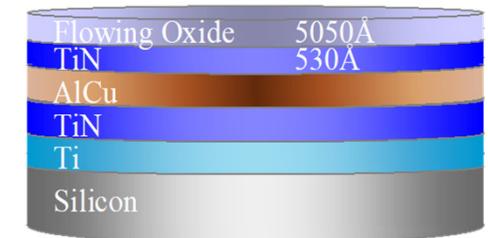


# Spectrum Ellipsometer



SiO <sub>2</sub>	60 Å
SiN	47 Å
SiO <sub>2</sub>	21 Å
POLY	1290 Å
SiO <sub>2</sub>	1290 Å
Silicon	

Multilayers : ONOPO



Multilayers: SiO<sub>2</sub> / TiN / AlCu

