PRODUCTION DATA – May 21, 2013

RoHS compliant

Features

- Minimum Component Ultrasonic Park Assist Solution
- Bi-directional Communication via Supply (E524.02)
- One Wire I/O to Program and Receive Echo Signal (E524.03)
- Single Transceiver Architecture
- Programmable to Transducer Frequencies 40kHz to 58kHz
- Supports “Receive Only” mode
- High Sensitivity and Low Noise Down to 0.5µV_{RMS}
- Driver Power and Signal Gain Programmable
- Digital Filtering and Signal Processing
- 14 Programmable Threshold / Time Settings
- Embedded EEPROM to Store Settings
- Automotive Supply and I/O Protection
- AEC-Q100 Qualification

Applications

- Ultrasonic Park Assist (USPA / UPA / PAS)
- Industrial Distance Measuring
- Robotics

Ordering Information

Product ID	*Temp Range*	*Interface*	*Package*
E524.02	-40°C to +85°C	2-wire	QFN20L4
E524.03	-40°C to +85°C	3-wire	QFN20L4

General Description

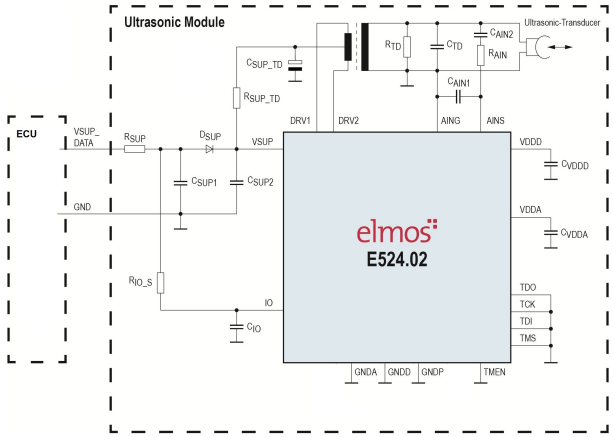
The E524.02 and E524.03 offer ultrasonic range detection with minimum component count.

In transmit mode, the IC drives a center tapped transformer directly. Driver frequency, transmitted burst power and other parameters are user configurable and stored in embedded EEPROM via a single wire IO pin at assembly. Both devices feature settings for short and long distance measurement.

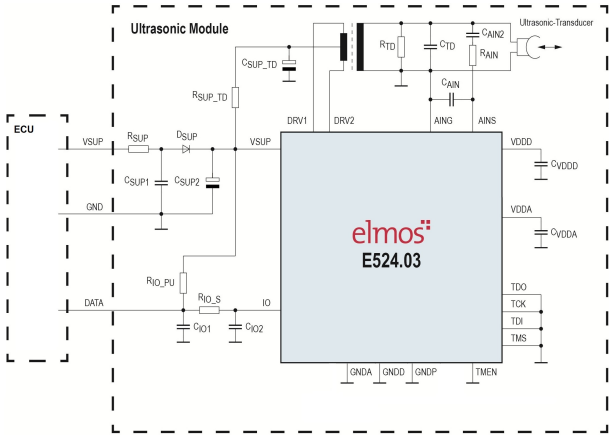
In receive mode, the echo signal is first amplified with a programmable gain amplifier and converted by an internal analog-to-digital converter. The signal is subsequently digitally filtered and compared. Comparator thresholds are adjustable via registers for defined interval lengths within a measurement period. The resulting signal is available at pin IO for the hosting BCU. A “Receive Only” mode enables the reception of indirect echos..

The E524.03 interfaces with the BCU via one dedicated IO-line. To minimize wires, the E524.02 supports communication over a single power supply line.

Typical Application Circuits

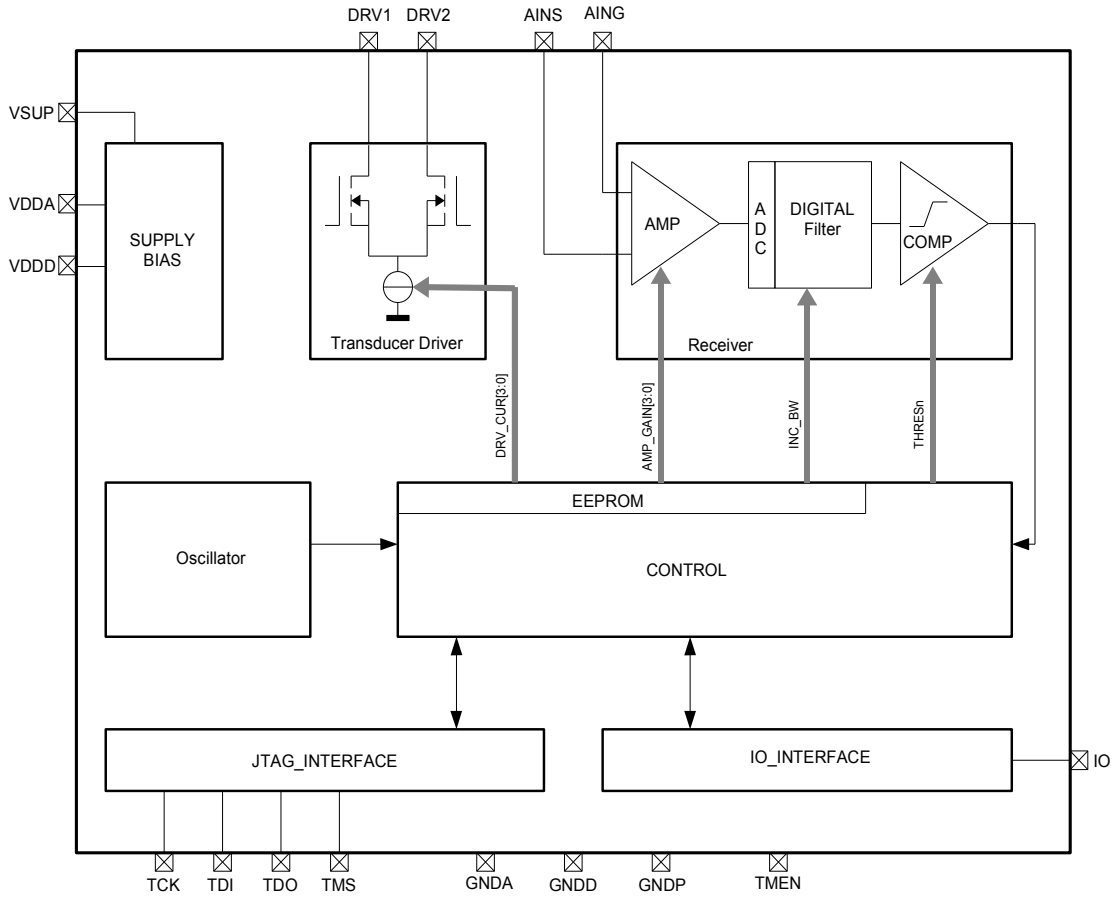


E524.02 supports a bi-directional communication via supply line.



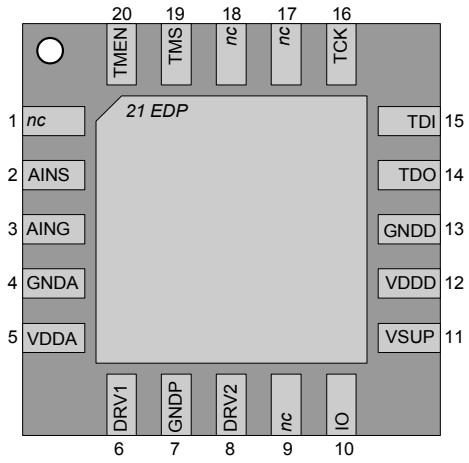
E524.03 supports a dedicated IO-line for data transfer.

Functional Diagram



Pin Configuration

Top View



QFN20L4, not to scale.

Pin Description

Pin	Name	Type	Description
1	*n.c.*	-	No Connection. Connect to GNDA.
2	AINS	I	Positive Analog Signal Input from Transducer.
3	AING	I	Negative Analog Signal Input from Transducer.
4	GNDA	S	Analog Ground
5	VDDA	S	Analog Supply Voltage. Bypass with C_{VDDA} to GNDA.
6	DRV1	O	Driver Output 1. Connects to push-pull-transformer.
7	GNDP	S	Ground for Driver Outputs and I/O Interface. Connect to ground plane to ensure low-impedance path for driver outputs.
8	DRV2	O	Driver Output 2. Connects to push-pull-transformer.
9	*n.c.*	-	No Connection. Connect to GNDP.
10	IO	I/O	Bidirectional Interface. As an input, commands are transmitted by the hosting BCU. In output mode, the E524.02 and E524.03 transmit echo signal data to the host. *The E524.03 communicates to the BCU through a dedicated I/O line (DATA). The E524.02 communicates to the BCU through the supply line (VSUP_DATA)*
11	VSUP	S	Battery Supply Input. Connect to voltage source with reverse polarity protection circuit as shown in Typical Applications Circuit.
12	VDDD	S	Digital Supply Output. Bypass with C_{VDDD} to GNDD
13	GNDD	S	Digital Ground
14	TDO	O	JTAG Data Output. Connect to GNDD if not in test mode.
15	TDI	I	JTAG Data Input. Connect to GNDD if not in test mode.
16	TCK	I	JTAG Clock Input. Connect to GNDD if not in test mode.
17	*n.c.*	-	No Connection. Connect to GNDA.
18	*n.c.*	-	No Connection. Connect to GNDA.
19	TMS	I	JTAG Select Input. Connect to GNDD if not in test mode.
20	TMEM	I	JTAG Test Mode Enable Input. Connect to GNDD if not in test mode.
-	*EP*	S	Exposed Pad. Connect to large copper ground plane for optimal heat dissipation. Connect to GNDA and GNDD.

Note: S = Supply, I/O = Input/Output

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
Supply Voltage		VSUP	-0.3	30	V
Supply Voltage	t < 500 ms	VSUP	-0.3	40	V
Voltage at Pin IO		V_{IO}	-0.3	30	V
Voltage at Pin IO	t < 500 ms	V_{IO}	-0.3	40	V
Voltage at Digital Pins (VDDD, TCK, TDO, TDI, TMS, TMEN)		V_D	-0.3	3.6, V_{VDDD}+0.3	V
Voltage at Analog Pins (VDDA, AINS, AING)		V_A	-0.3	3.6, V_{VDDA}+0.3	V
Voltage at Pins DRV1 and DRV2		V_{DRV}	-0.3	40	V
Power Dissipation	T_{AMB} <=85°C	P_{TOT}		1.5	W
Thermal Resistance Junction to Ambient		$R_{T,J-A}$	30	33	°C/W
Ambient Temperature		T_{AMB}	-40	+85	°C
Junction Temperature		T_J	-40	+125	°C
Storage Temperature		T_{STG}	- 55	+125	°C

2 ESD Protection

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
ESD HBM Protection at pin VSUP, IO	1)	$V_{VSUP,}$ V_{IO}	+/- 4	-	kV
ESD HBM, all other Pins	1)	$V_{VSUP,}$ V_{IO}	+/- 2	-	kV
ESD CDM at pins near corners (Pins 1,5,6,10,11,15,16,20)	2)	V_{PINS_EDGE}	+/- 0.75	-	kV
ESD CDM at all other pins	2)	V_{PINS_OTHER}	+/- 0.5	-	kV

1) According to AEC-Q100-002 (HBM) chip level test
2) According to AEC-Q100-011 (CDM) chip level test

3 Recommended Operating Conditions

- Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified.
- The first electrical potential connected to the ASSP must be GND.
- In the operating range from $V_{SUP,PORHL}$ ... 7V function is guaranteed with limited parameters.

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage Range		VSUP	7		18	V
Programming EEPROM Voltage at pin IO		VPROG	23	25	27	V
DC Voltage at pins AINS, AING		AINS / AING	-0.3		0.3	V
Current into pins AINS, AING		AINS / AING	-20		20	mA

4 Electrical Characteristics

(V_{VSUP} = +7V to +18V, T_{AMB} = -40°C to +85°C, unless otherwise noted. Slew rate at pin VSUP < 1V/µs. Typical values are at V_{VSUP} = +13.5V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltages						
Supply Current		I_{VSUP}		7	12	mA
Level at VSUP where the power-on reset state is entered.		$V_{SUP,PORHL}$			5.0	V
Level at VSUP where the power-on reset state is exit.		$V_{SUP,PORLH}$			5.2	V
Internal Analog Supply Voltage	C_{VDDA} connected	VDDA	3.0	3.3	3.6	V
Internal Digital Supply Voltage	C_{VDDD} connected	VDDD	3.0	3.3	3.6	V
VDDA Short Circuit Current	Short to VDDA	$I_{VDDA,SHORT}$	-30			mA
VDDD Short Circuit Current	Short to VDDD	$I_{VDDD,SHORT}$	-75			mA
Transducer Driver						
Current into DRVn[1)]	$V_{DRV1,2}$ = 36V corresponding DRV path switched off	$I_{CLAMP,DRV}$		<2	500	µA
Leakage Current	$V_{DRV1,2}$ = 0V, 12V	$I_{LEAK,DRV}$	-100		100	nA
Current Adjustment Steps		N_{IDRV}		15		
Adjustment Step Size		$STEP_{IDRV}$		13.5		mA
Minimum Current Adjustment	DRV_CUR[3:0]= '0000'	$IDRV_{min}$		108		mA
Maximum Current Adjustment	DRV_CUR[3:0]= '1111'	$IDRV_{max}$		310		mA
Transducer Frequency Range	F_DRV_ADJ[6:0]	f_{DRV}	40		58	kHz
Adjustment Frequency Step Width		LSB_{f_DRV}		300		Hz
Temperature Coefficient Driver Output Frequency		TC_{f_DRV}		-400		ppm/°C
Factory Preset Driver Frequency	Temperature=+30°C	$f_{DRV,ADJ}$	45.00	48.00	51.00	kHz

Electrical Characteristics (continued)

(V_{VSUP} = +7V to +18V, T_{AMB} = -40°C to +85°C, unless otherwise noted. Slew rate at pin VSUP < 1V/µs. Typical values are at V_{VSUP} = +13.5V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Receiver Amplifier						
Minimum Gain	@ f_{DRV}=52 kHz	G_{MIN}	63	67	71	dB
Maximum Gain	@ f_{DRV}=52 kHz	G_{MAX}	78	82	86	dB
Step Size	@ f_{DRV}=52 kHz	ΔGC	0.5	1.0	1.5	dB
Number of Steps		N_G		15		
Gain Reduction	@ f_{DRV}=52 kHz	GRED	10.5	12	13.5	dB
Input Impedance	AINS to GNDA, AING to GNDA	R_{IN}		100		kΩ
Noise Level	@ f_{DRV}=52 kHz [1)]	e_N		7.3		$\frac{nV}{\sqrt{Hz}}$
Digital Filter						
Center Frequency		$f_{c,filt}$		1		f_{DRV}
-3dB-Bandwidth	8 Bursts FILTADJUST=0	$BW,DFILT_{8,0}$		0.2191		f_{DRV}
-3dB-Bandwidth	8 Bursts FILTADJUST=1	$BW,DFILT_{8,1}$		0.1058		f_{DRV}
-3dB-Bandwidth	16 Bursts FILTADJUST=0	$BW,DFILT_{16,0}$		0.1058		f_{DRV}
-3dB-Bandwidth	16 Bursts FILTADJUST=1	$BW,DFILT_{16,1}$		0.0520		f_{DRV}
Comparator						
Masking Time Output Comparator	COMP_MASK=1	T_{CMASK}	-	16	-	1 / f_{DRV}
I/O Interface						
Voltage Threshold Low Input Signal		V_{IO_IL}	0.29	0.33	0.36	VSUP
Voltage Threshold High Input Signal		V_{IO_IH}	0.62	0.67	0.70	VSUP
Voltage at Pin IO to Output Low Level	E524.02 I_{OUT} = 2mA	V_{IO_OL4}			0.5	V
Voltage at Pin IO to Output Low Level	E524.03 I_{OUT} = 4mA	V_{IO_OL2}			0.5	V
Short Circuit Current Limit	V_{OUT} < 18V	I_{IO_SHORT}			60	mA

Electrical Characteristics (continued)

(V_{VSUP} = +7V to +18V, T_{AMB} = -40°C to +85°C, unless otherwise noted. Slew rate at pin VSUP < 1V/µs. Typical values are at V_{VSUP} = +13.5V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Slew Rate		SR_{VIO}	-	1.7	-	V/µs
Input Debouncer		T_{DEB}	0		1	$1/f_{DRV}$
IO Low Period Send Request		T_{SND}	4.5	6	8.92	$1/f_{DRV}$
IO Low Period Receive Request		T_{REC}	9	12	14.92	$1/f_{DRV}$
IO Low Period to Enter Command Mode		T_{CMD}	15	18	20.92	$1/f_{DRV}$
IO Low Period to Enter Programming Command Mode		T_{CMD_PROG}	15	18	20.92	$1/f_{DRV}$
IO High Phase After T_{CMD} and T_{CMD_PROG}		T_D	1.08	3	4.42	$1/f_{DRV}$
Setup Time for V_{PROG}		T_{VPROG}			5	ms
Programming Time		T_{PROG}		20		ms
Bit Length, (BCU to E524.02/03)		T_{BIT_WR}	9	12	14.92	$1/f_{DRV}$
IO Low Period for logical '0', (BCU to E524.02/03)		T_{BIT0_WR}	4.5	6	8.92	$1/f_{DRV}$
IO Low Phase for logical '1', (BCU to E524.02/03)		T_{BIT1_WR}	1.08	3	4.42	$1/f_{DRV}$
Bit Length, (E524.02/03 to BCU)		T_{BIT}		12		$1/f_{DRV}$
IO Low Phase for logical '0', (E524.02/03 to BCU)		T_{BIT0}		6		$1/f_{DRV}$
IO Low phase for a logical '1', (E524.02/03 to BCU)		T_{BIT1}		3		$1/f_{DRV}$
Pulse Width Echo Event (only E524.02)	only E524.02	$T_{ECHO2WIRE}$		3		$1/f_{DRV}$
Pulse Width Low Frequency Calibration Pulse		T_{CAL}		12		$1/f_{DRV}$
EEPROM						
Data Retention Time		t_{RET_EE}			10	Year
Program / Erase Endurance		$N_{END\_EE\_85}$			10^4	Cycle

[1)] Not production tested

5 Functional Description

5.1 Overview

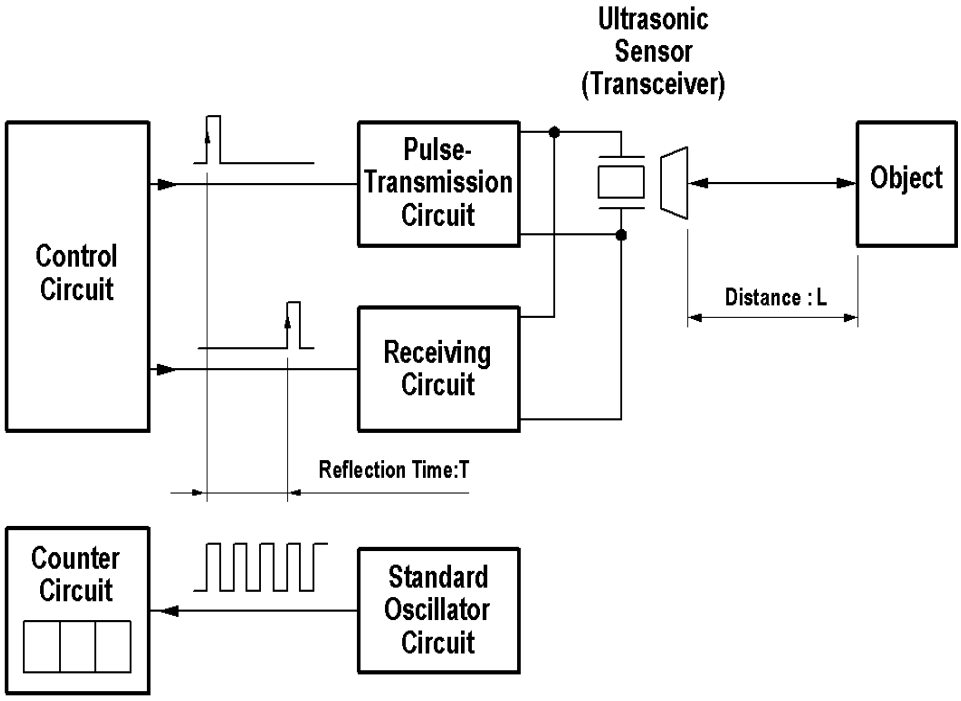


Figure 1. Ultrasonic Distance Measuring

The principle of ultrasonic distance measuring is based on transmitting a pulse and measuring the reflection time of the received pulse as shown in Figure 1. The relationship between the distance from the transducer to the object L and the time T it takes to receive the echo is L = C * T/2, where C is the velocity of sound. The E524.02 and E524.03 require only one transducer which acts as a transmitter and receives the reflected pulse with a time delay. The time delay is proportional to the distance to measure.

A measurement is started by a SEND or RECEIVE request by the body control unit (BCU) via a single I/O wire. Internal logic generates a burst for the transducer first. For a set number of intervals, incoming reflected pulses are digitally filtered and compared to programed threshold levels. If the echo pulse exceeds the set threshold level, the comparator is triggered. In SEND / RECEIVE mode, the comparator output drives the single IO pin. The time elapsed from sending out a burst signal to receiving an echo signal from an object is proportional to the distance of the object.

E524.02

The E524.02 requires only two wires for the communication of ultrasonic module and BCU: Ground (GND) and the supply wire (VSUP_DATA). As illustrated in Figure 22, bidirectional data travels between ultrasonic module and BCU by modulating voltage on the supply wire.

E524.03

The E524.03 requires three wires to communicate from the ultrasonic module with the BCU. As shown in the front page Typical Application Circuit, the three wires are ground (GND), supply (VSUP) and one signal line (DATA).

5.2 Command Structure Summary

The E524.02 and E524.03 support nine commands from the hosting BCU.

- SEND initiates a burst signal via the internal drivers followed by a measurement sequence.
- RECEIVE initiates a measurement sequence without preceding burst, useful for triangulation in systems with multiple transducers.
- CONFIGURE defines the number of burst pulses and digital filter gain.
- THRESHOLD writes individual threshold values for up to 15 timing intervals and scaling factors into device.
- READ_STATUS verifies previous transmission of threshold values and reads current noise level
- EE_WRITE allows to pre-load settings for the oscillator frequency, driver current levels, amplifier gain and filter into the device.
- EE_PROGRAM programs settings pre-loaded with EE_WRITE into the internal EEPROM.
- EE_READ reads the EEPROM contents with three read voltage levels to verify successful programming.
- FREQUENCY_CALIBRATION returns 8 defined clock periods to the ECU for transducer calibration purposes.

5.3 SEND / RECEIVE Command Overview

The SEND command initiates a burst following a measurement sequence. A RECEIVE command is identical to the SEND command but skips the burst. The initial threshold value in RECEIVE is defined by bit THRES_INI.

SEND or RECEIVE mode is requested from the BCU by holding Pin I/O low for T_{SND} or $T_{REC.}$ SEND or RECEIVE mode is entered with the rising edge of the corresponding command. In SEND and RECEIVE mode, a filter output signal exceeding the comparator threshold indicates a received echo. Threshold values are passed to the comparator in SEND and RECEIVE mode over a defined number of up to 15 time intervals. The individual threshold value is comprised of several components:

- Initial programmable raw value
- Scaling factor
- Additional offset

The threshold values are connected by linear interpolation over the interval duration. As long as the E524.02 and E524.03 operate in SEND or RECEIVE mode, no instructions coming over the IO-Interface are accepted. The interface is ready to receive new instructions when a high level remains at pin IO for at least T_{DEB} to debounce after SEND or RECEIVE mode has ended.

The E524.02 and E524.03 can diagnose the proper operation of transducer and transformer. After the SEND command, the transducer driver is activated and sends out a burst for the length T_{TX}. This also causes high signal levels at the receiving amplifier and triggers the comparator. After the transducer driver is deactivated, the transducer continues to oscillate for a brief release time as shown in Figure 2 and Figure 4.

5.4 SEND and RECEIVE

E524.02

For the E524.02 a pulse is also generated the first time the signal line becomes lower than the threshold to indicate proper operation.

Figure 2 illustrates the SEND command timing for the E524.02 with an example.

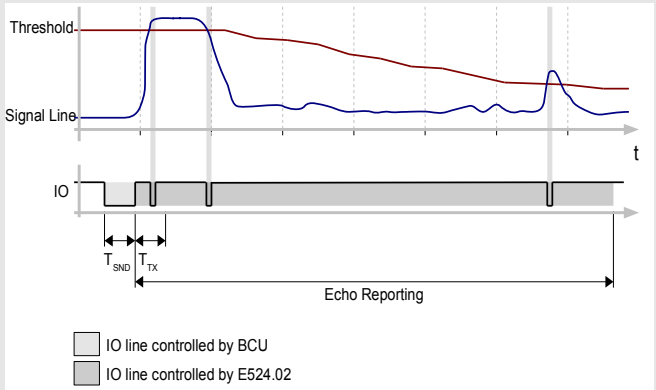


Figure 2. E524.02 Send Command Timing

During and shortly after the burst the threshold is held at maximum and then programmed to decline slowly. A echo is defined as the signal level rising above the threshold and is reported with a low pulse of $T_{ECHO2WIRE}$. In the example, the first low pulse is reported during burst, the second low pulse indicates correct operation and the end of the reporting period, a third pulse is triggered by an echo signal.

Figure 3 shows the timing for a E524.02 RECEIVE command.

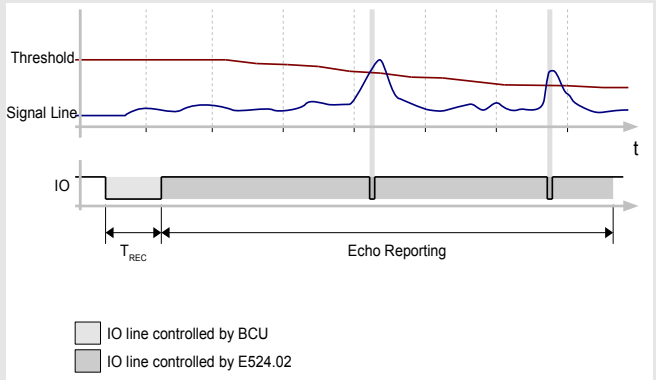


Figure 3. E524.02 RECEIVE Command Timing

The E524.02 operates purely in receiving mode for the entire sequence. In the example, two echoes are received and pull Pin IO low for $T_{ECHO2WIRE}$. The thresholds are scalable to 25%, 50%, 75% or 100% with bit THRES_SCALE, part of the THRESHOLD command.

E524.03

For the E524.03, a rising edge on the IO Pin shortly after T_{TX} signals correct operation of the transducer / transformer circuit.

Figure 4 illustrates the SEND command timing for the E524.03 with an example.

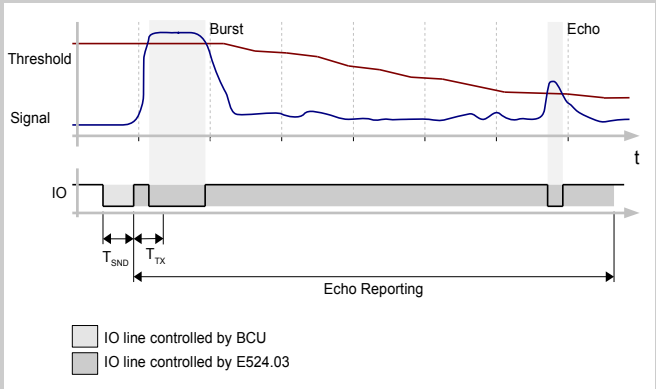


Figure 4. E524.03 Send Command Timing

During and shortly after the burst the threshold is held at maximum and then programmed to decline slowly. At the end of the echo reporting period, an echo triggers the comparator with its rising and falling edge.

Figure 5 shows the timing for a E524.03 RECEIVE command.

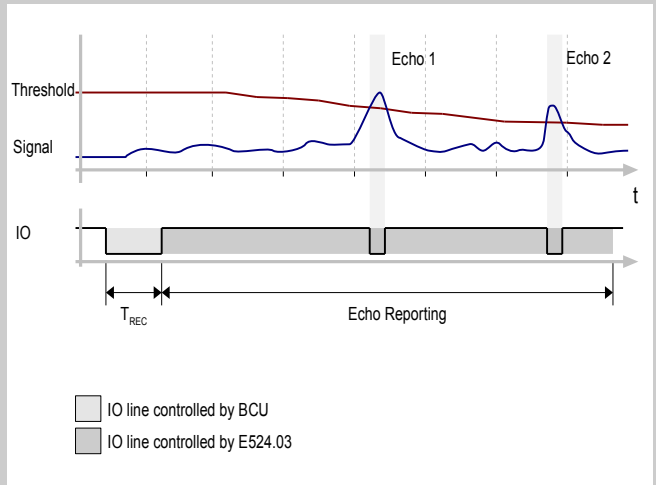


Figure 5. E524.03 RECEIVE Command Timing

The E524.03 operates purely in receiving mode for the entire sequence. In the example, two echoes are received and pull Pin IO low. The thresholds are scalable to 25%, 50%, 75% or 100% with bit THRES_SCALE, part of the THRESHOLD command.

5.5 Threshold Level Intervals and Exponents

In SEND or RECEIVE mode, the measurement cycle is divided into up to 15 fixed intervals (Interval 0 through 14). For each of the 15 intervals individual threshold values are programmable.

The interval length is inversely proportional to the transducer frequency f_{DRV}. Threshold levels are divided into 32 threshold exponents. Each exponent represents a raw threshold value which in turn represents a threshold level measured in mV.

As an example, Table 2 shows a threshold exponent of 21 having a raw threshold value of 233 which translates into an actual comparator threshold of 375.8mV.

The threshold value for the initial interval 0 is set to maximum (threshold exponent 31) in SEND mode. In RECEIVE mode, the THRES_INI bit determines the threshold value as shown in Table 1. THRES_INI is set in the THRESHOLD Command.

Table 1. THRES_INI Receive Mode

THRES_INI	Function in Receive Mode
0	Initial threshold exponent = 31
1	Initial threshold exponent = THRES1

The threshold values for intervals 1 through 14 can be programmed into the device in registers addresses THRES1 through THRES14. Table 4 shows the interval length for two transducer frequencies in short and long range mode with their respective threshold exponent register addresses THRES1 through THRES14.

During each interval, the actual threshold levels change with linear interpolation. The threshold of the initial interval 0 is always constant. For intervals 1 through 14, the threshold value starts with the value of the previous interval and changes linearly until it reaches its programmed value at the end of the interval. Figure 6 illustrates the linear interpolation of different threshold values with an threshold profile example.

The raw threshold values for threshold exponent $THRES_{ndez}$ 0 to 31 can be calculated by following formula:

$$threshold\_value\_n = 62 \cdot 10^{\frac{THRESn,dez}{31}} - 62$$

Table 2 shows the resulting raw threshold values for THRESn and corresponding comparator voltage levels.

The threshold is stored into volatile memory and set to the default value after power on.

Table 2. Threshold Values

Threshold Exponent	Raw Threshold Value (Without Offset and Scaling)	Typical Voltage [mV]
0	0	0
1	5	8.1
2	10	16.1
3	15	24.2
4	21	33.9
5	28	45.2
6	35	56.5
7	42	67.7
8	50	80.6
9	59	95.2
10	68	109.7
11	78	125.8
12	89	143.5
13	101	162.9
14	113	182.3
15	127	204.8
16	141	227.4
17	157	253.2
18	174	280.6
19	192	309.7
20	212	341.9
21	233	375.8
22	256	412.9
23	280	451.6
24	307	495.2
25	335	540.3
26	366	590.3
27	399	643.5
28	434	700.0
29	472	761.3
30	514	829.0
31	558	900.0

5.6 Long / Short Range and Offset Setting

In SEND or RECEIVE mode, the measurement cycle is divided into up to 15 fixed intervals. The duration of these intervals is selected by bit THRES_LEN as shown in Table 3. If short range is selected, 15 intervals end at 18 ms for f_{DRV} = 48kHz. In long range under the same conditions, the duration doubles to 36ms (Table 4).

The THRES_LEN bit also changes the threshold offset value to accommodate a stronger echo signal in short range. THRES_LEN is set in the THRESHOLD command.

Table 3. Threshold Length and Offset

THRES_LEN	Function	Range
0	Short intervals selected, threshold offset set to high value=62	Short Range
1	Long intervals selected, threshold offset set to low value=31	Long Range

Table 4. Intervals Short and Long Range

Interval Number	Threshold Exponent Register Name	Interval [ms] Short Range f_{DRV}=48kHz	Interval [ms] Short Range f_{DRV}=58kHz	Interval [ms] Long Range f_{DRV}=48kHz	Interval [ms] Long Range f_{DRV}=58kHz
0	initial	0 - 2.0	0 - 1.66	0 - 2.0	0 - 1.66
1	THRES1	2.0 -3.0	1.66 - 2.48	2.0 - 4.0	1.66 - 3.31
2	THRES2	3.0 - 4.0	2.48 - 3.31	4.0 - 6.0	3.31 - 4.97
3	THRES3	4.0 - 5.0	3.31 - 4.14	6.0 - 8.0	4.97 - 6.62
4	THRES4	5.0 - 6.0	4.14 - 4.97	8.0 - 10.0	6.62 - 8.28
5	THRES5	6.0 - 7.0	4.97 - 5.79	10.0 - 12.0	8.28 - 9.93
6	THRES6	7.0 - 8.0	5.79 - 6.62	12.0 - 14.0	9.93 - 11.59
7	THRES7	8.0 - 9.0	6.62 - 7.45	14.0 - 16.0	11.59 - 13.24
8	THRES8	9.0 - 10.0	7.45 - 8.28	16.0 - 18.0	13.24 - 14.90
9	THRES9	10.0 - 11.0	8.28 - 9.10	18.0 - 21.0	14.90 - 17.38
10	THRES10	11.0 - 12.0	9.10 - 9.93	21.0 - 24.0	17.38 - 19.86
11	THRES11	12.0 - 13.0	9.93 - 10.76	24.0 - 27.0	19.86 - 22.34
12	THRES12	13.0 - 14.0	10.76 - 11.59	27.0 - 30.0	22.34 - 24.83
13	THRES13	14.0 - 15.0	11.59 - 12.41	30.0 - 33.0	24.83 - 27.31
14	THRES14	15.0 - 18.0	12.41 - 14.90	33.0 - 36.0	27.31 - 29.79

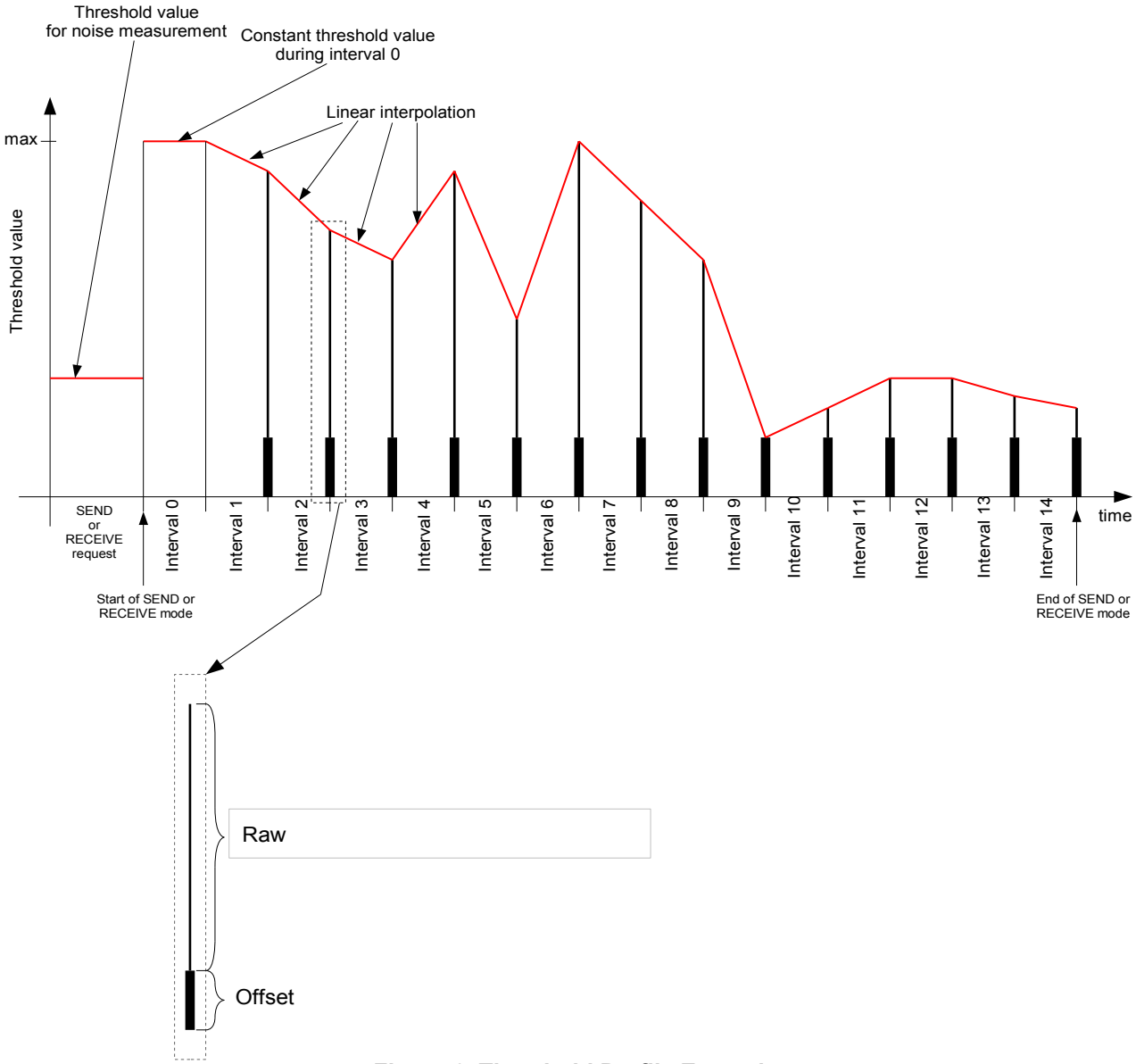


Figure 6. Threshold Profile Example

In short range, SEND and RECEIVE mode always utilizes the entire possible cycle time and evaluation terminates after interval 14.

In long range, the measurement cycle can be shortened. SEND and RECEIVE mode end earliest after interval 7 and latest after the 14th interval, depending on the programmed values THRES7 - THRES14. If value THRESn (for n = 8-14) is set to maximum value and higher than the previous value THRES (n-1), SEND and RECEIVE mode ends after interval n-1, else after interval 14.

As an example if THRES11 = 6 and THRES12 = 31 (maximum value), SEND or RECEIVE mode ends after interval 11.

5.7 Threshold Scaling THRES_SCALE[1:0]

In RECEIVE mode the threshold sensitivity can be increased by a scaling factor. All threshold values defined by THRES1 - THRES14 are multiplied with this scaling factor.

The scaling factor is set by bits THRES_SCALE[1:0] and shown in Table 5. THRES_SCALE is part of the THRESHOLD Command. The scaling factor in SEND mode is always 1.

Table 5. Receive Threshold Scaling

THRES_SCALE[1]	THRES_SCALE[0]	SCALING_FACTOR
0	0	0.25
0	1	0.5
1	0	0.75
1	1	1.0

In summary, actual threshold values are the result of the threshold exponent, a scaling factor and an offset as defined in Table 3 and shown in Figure 6. Values used in the interpolation algorithm are calculated by:

$$threshold\_value\_n = \left(62 \cdot 10^{\frac{THRESn,dez}{31}} - 62\right) \cdot SCALING\_FACTOR + OFFSET$$

Example 1:

Short range, SEND mode request, THRESn programmed to 15

$$threshold\_value\_n = \left(62 \cdot 10^{\frac{15}{31}} - 62\right) \cdot 1.0 + 62 = 127 \cdot 1.0 + 62 = 189$$

The result is a voltage level of approximately 290mV at the comparator.

Example 2:

Long range, RECEIVE mode request, scaling_factor=0.75, THRESn programmed to 7

$$threshold\_value\_n = \left(62 \cdot 10^{\frac{7}{31}} - 62\right) \cdot 0.75 + 31 = 42 \cdot 0.75 + 31 = 62$$

A threshold value of 62 translates to a voltage level of approximately 100mV at the comparator.

5.8 Initial Noise Measurement

Ambient supersonic noise levels can be evaluated by the E524.02 and E524.03 just before entering a measurement cycle as shown in Figure 6. The evaluation takes place during the low phase of the SEND or RECEIVE command (T_{SND} / T_{REC}). The output of the digital filter is compared to a threshold value set with bit NOISE_CFG, part of the EE_WRITE command. Table 6 shows the available threshold value settings.

The READ_STATUS command returns the noise information with one bit. After power-on, the threshold value for the first noise measurement is at maximum value of 1023.

Table 6. Noise Measurement Configuration

NOISE_CFG[1]	NOISE_CFG[0]	Threshold Value
0	0	Threshold value at the end of previous SEND or RECEIVE mode with SCALING_FACTOR fixed to 1.0
0	1	62
1	0	124
1	1	620

5.9 THRESHOLD Command

As shown in Table 7 and Figure 7, the THRESHOLD command writes threshold values for 15 intervals, scaling information, threshold length and several control bits for error detecting into the E524.02 and E524.03. The first bit transmitted on the IO line is the MSB of THRES1 (bit 0) and the last bit is the PARITY4 bit 78.

Table 7. THRESHOLD Command

Bit	Number of Bits	Function	Name	Default (bin)
0-4	5	1st threshold value	THRES1	31
5-9	5	2nd threshold value	THRES2	31
10-14	5	3rd threshold value	THRES3	31
15-19	5	4th threshold value	THRES4	30
20-24	5	5th threshold value	THRES5	29
25-29	5	6th threshold value	THRES6	28
30-34	5	7th threshold value	THRES7	27
35-39	5	8th threshold value	THRES8	25
40-44	5	9th threshold value	THRES9	22
45-49	5	10th threshold value	THRES10	14
50-54	5	11th threshold value	THRES11	10
55-59	5	12th threshold value	THRES12	6
60-64	5	13th threshold value	THRES13	0
65-69	5	14th threshold value	THRES14	0
70-71	2	Scaling for receive operation	TRES_SCALE[1:0]	2
72	1	Initial threshold value	THRES_INI	0
73	1	Length of measurement cycle	THRES_LEN	0
74	1	Even parity bit for bit 73-58	PARITY0	-
75	1	Even parity bit for bit 57-42	PARITY1	-
76	1	Even parity bit for bit 41-26	PARITY2	-
77	1	Even parity bit for bit 25-10	PARITY3	-
78	1	Even_parity bit for bit 9-0	PARITY4	-

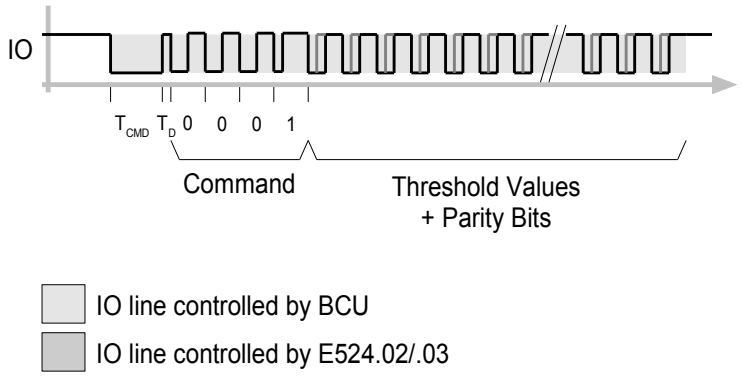


Figure 7. Threshold Command Timing

5.10 READ_STATUS Command

Figure 8 and Table 8 show how the READ_STATUS command is used to verify the previous write operation of THRESHOLD. Two additional bits return information about the noise level of the most recent SEND or RECEIVE request. See chapter 5.8 “Initial Noise Measurement” how to set threshold to evaluate the noise level.

Table 8. READ_STATUS Command

Bit Number	Value	Description
1	0	Last data reception incorrect, default data active.
1	1	Last data reception successful, transmitted data active.
2	0	No noise detected during last measurement cycle
2	1	Noise detected during last measurement cycle

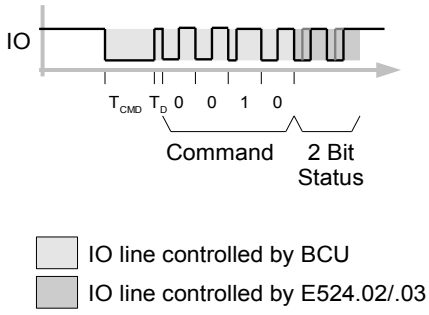


Figure 8. READ_STATUS Timing

6 Transducer

The main components of the pulse transmission circuit are internal drivers, a transformer and one transducer. A push-pull center-tapped transformer ensures maximum efficiency and reduced EMI-radiation.

6.1 Transducer Driver Current Adjust

The transducer power is controlled by an adjustable current source. Current steering achieves a more stable sound pressure level over temperature and supply voltage. The driver output current can be varied in 15 steps. Currents are set by register DRV_CUR[3:0] and adjustable in the range of 108mA to 310mA. DRV_CUR is set with the EE_WRITE command as shown in Table 12. The relationship between the driver current I_{DRV} and the bits in register DRV_CUR is given by:

$$I_{DRV} = IDRV_{min} + STEP_{IDRV} \cdot DRV\_CUR[3:0]$$

The center tap of the transformer is directly connected to VSUP. The 'SEND REQUEST' command activates the transducer driver. Pins DRV1 and DRV2 are alternately pulled to ground with driver frequency f_{DRV}. Bursts of 8 or 16 periods are set in Table 9. *Measurement Configuration Register*. Activate the transducer with the 'SEND REQUEST' command.

6.2 Transducer Driver Frequency Adjust and Calibration

The frequency f_{DRV} can be adjusted by EEPROM register F_DRV_ADJ[6:0]. The adjustment range is guaranteed from $f_{DRV,MIN}$ = 40kHz in steps of 300Hz to $f_{DRV,MAX}$ = 58kHz. The actual adjustment range is higher. The frequency is strictly monotonic increasing with an increasing value of F_DRV_ADJ[6:0].

The E524.02 and E524.03 are shipped with a preset transducer frequency of $f_{DRV,ADJ}$ = 48kHz. Because the effective adjustment range is larger than the guaranteed adjustment range, a setting of register F_DRV_ADJ[6:0] = 0 or 127 will return frequencies outside $f_{DRV,MIN}$ and $f_{DRV,MAX}$.

The actual frequency f_{DRV} is measured with the FREQUENCY CALIBRATION command. As shown in Figure 9, the sensor returns eight pulses with a defined width of $T_{CAL} = 12/f_{DRV}$. The measured frequency $f_{measure} = 12 / T_{CAL}$.

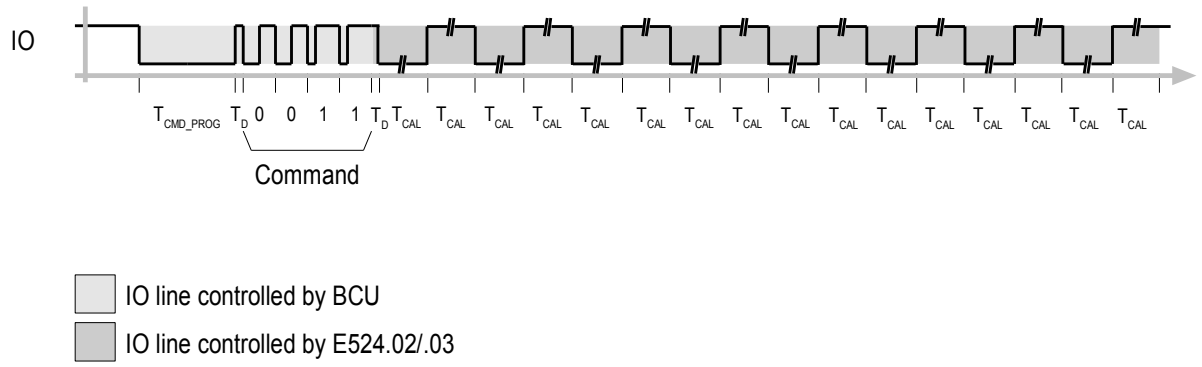


Figure 9. FREQUENCY_CALIBRATION Command

Following steps calibrate the E524.02 or E524.03 transducer frequency to the desired transducer resonance frequency:

1. Read current settings of F_DRV_ADJ[6:0] with EE_READ
2. Measure actual frequency $f_{measure}$ = 12 / $T_{CAL.}$
3. Calculate the difference f_{DIFF} = target frequency f_{DRV} - actual frequency $f_{measure}$
4. Increase / decrease by one step n as shown in Figure 11. Alternatively, calculate the rough number n of steps corresponding to f_{DIFF} by n = f_{DIFF} / 300Hz.
5. Adjust register F_DRV_ADJ[6:0] by n
6. Repeat until the target frequency is reached
7. Store setting for register F_DRV_ADJ[6:0] in EEPROM.

A new value for f_{DRV} will also change the I/O interface timing characteristics. Figure 11 summarizes the frequency adjustment flow and the necessary commands.

6.3 Transducer Driver Waveforms

Figure 10 shows simplified waveforms at pins DRV1 and DRV2 before and during transmission. The voltages at pins DRV1 and DRV2 exceed the supply voltage VSUP in operation. Use a clamping zener diode ZD_TD as shown in Figure 22, if the supply voltage at pin VSUP is close to the absolute maximum rating.

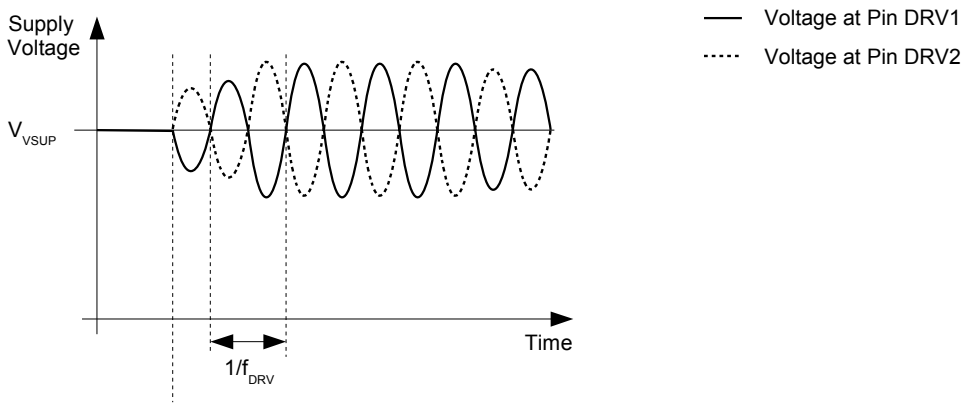


Figure 10. Transducer Driver DRV1 and DRV2 Waveforms

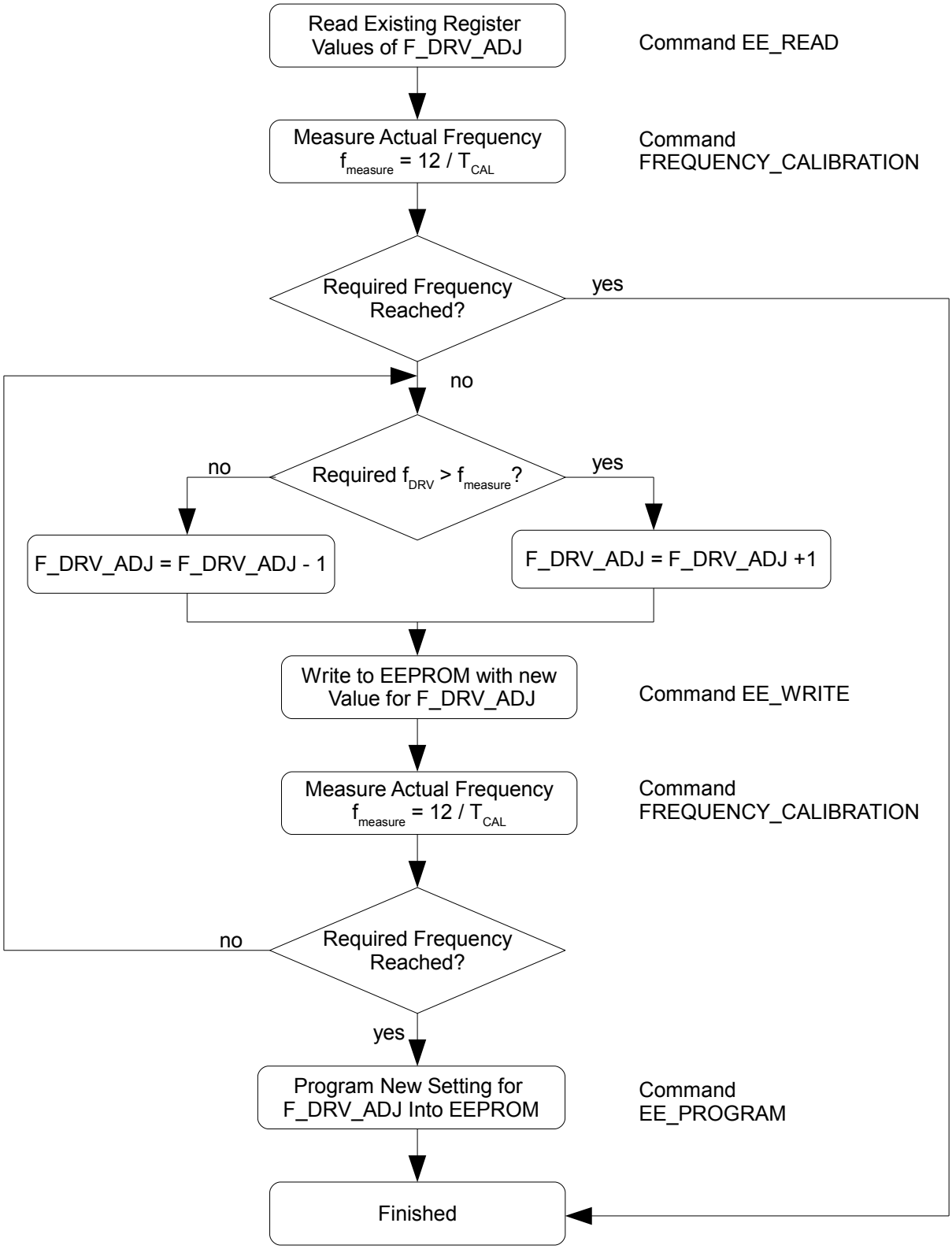


Figure 11. Frequency Adjustment Flowchart

7 Receiver

7.1 Overview

As shown in Figure 12. “Receiver Block Diagram”, the echo signal is picked up from the transducer at pins AINS and AING. The signal goes through a programmable gain stage first. After digitization, the signal is further processed by a programmable digital filter. Finally, the filter output goes through a register programmable comparator stage before data is sent via pin IO to the body control unit.

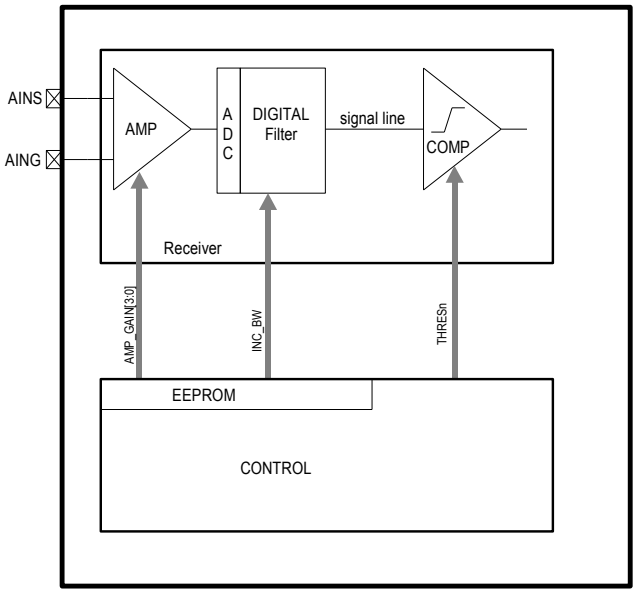


Figure 12. Receiver Block Diagram

7.2 Amplifier Gain Setting

Transducer output signal levels vary by type and application. The differential input of the amplifier minimizes pickup of unwanted signals. One input is typically used as signal input while the other input is tied to signal ground.

The incoming analog echo signal has to be amplified before it is converted by an ADC. The amplifier gain is programmable with a range of 15dB with 1dB resolution to ensure an optimum amplifier output voltage range. Gain settings are programmed with AMP_GAIN[3:0] and stored in EEPROM. The total gain can be calculated using the following formula:

$$Gain = G_{MIN} + \Delta GC \cdot AMP\_GAIN[3:0]$$

To improve short distance detection of objects, the gain can be reduced by 12dB with bit GRED as shown in Table 9 “Measurement Configuration Register”. The amplifier output is internally connected to an ADC.

8 Signal Processing

8.1 Digital Filter

Following the digitalization, the signal is processed by a digital filter. Since the clock of the transducer driver and the ADC / filter clock are synchronized, the digital filter finds the sending frequency reliably. The output of the digitally matched filter (DMF) represents the envelope of the echo signal. One digit of the 10bit value of the digital filter corresponds to:

$$V_{DIGIT} = \frac{VDD}{2} \cdot \frac{1}{1023} \approx 1.6mV$$

8.2 Setting Filter Gain and Burst Length

The characteristic of the digital filter depends on the number of transmitted burst pulses and the setting of the bit FILTADJUST. To achieve improved short distance capability of the sensor, reduce gain and burst length. Table 9, Table 10 and Figure 13 show the different commands and timing to set burst length and gain.

Table 9. Measurement Configuration Register

Command (bin)	Number of Burst-pulses / N_{BURST}	Gain Reduction / GRED	Default Configuration
1 1 0 0	8	OFF	
1 1 0 1	16	OFF	∅
1 1 1 0	8	ON	
1 1 1 1	16	ON	

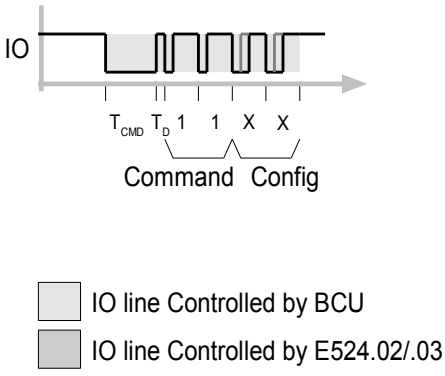


Figure 13. Command Configure Timing

Table 10. Digital Filter Bandwidth for Burst Length and FILTADJUST

Burst Pulse Number	Bit FILTADJUST	-3dB Bandwidth f_{DRV}
8	0	0.2191
8	1	0.1058
16	0	0.1058
16	1	0.0520

Filter characteristics for two burst lengths are illustrated in Figure 14 and Figure 15 . The FILTADJUST bit is set with EE_WRITE shown in Table 12.

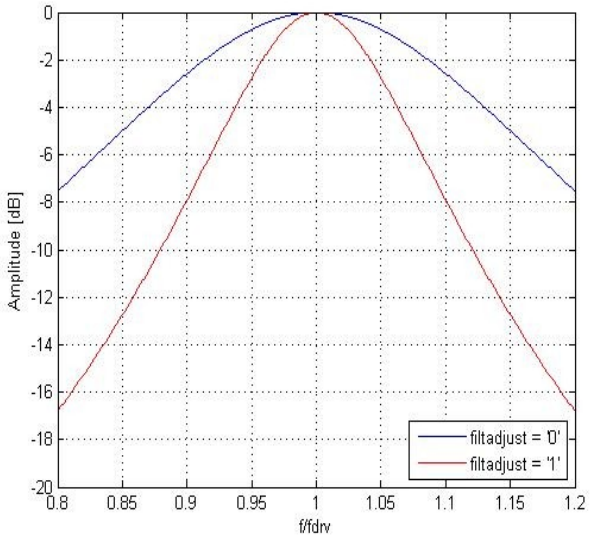


Figure 14. Bandpass Characteristic for 8 Busts

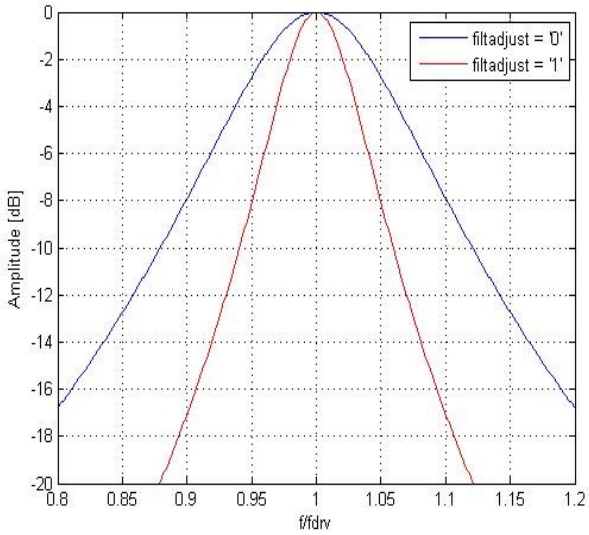


Figure 15. Bandpass Characteristic for 16 Bursts

8.3 Comparator

The digital comparator stage compares the digital filter output to a programmed threshold value for a given time interval. The comparator output appears at pin IO in SEND / RECEIVE mode.

The comparator output can be masked for the time T_{CMASK} (330µs for f_{DRV}=48kHz) after the output signal of the digital filter drops below the comparator threshold. This functionality might be useful if the IC is operated with high gain and low comparator threshold. In this combination even low noise coupling from the IO line to the analog input circuitry e.g. the transformer can cause false comparator triggering. The masking can be enabled with bit COMP_MASK as shown in Table 11.

Table 11. Comparator Masking

COMP_MASK	Function
0	Comparator masking **not** active
1	Comparator masking active

9 I/O Interface

9.1 Overview

Data is exchanged with the BCU via one pin labled IO. It is used to program the E524.02 or E524.03 from the hosting BCU and to transmit echo signal and status information to the BCU. A SEND or RECEIVE command is initiated by a BCU pulling pin IO low for T_{SND} or $T_{REC.}$ The internal EEPROM is programmed by pre-loading data in respective registers and raising the voltage to VPROG = 25V at pin IO for T_{PROG} = 20ms. For all other commands, the BCU pulls IO low for T_{CMD} and issues a 4 bit command sequence.

The bit length T_{BIT} is fixed to $12/f_{DRV}$ or 250µs for f_{DRV} = 48kHz. A logic '0' is signaled with pulling the line low for $T_{BIT0} = 6/f_{DRV}$ and a logic '1' with $T_{BIT1} = 3/f_{DRV}$ as shown in Figure 16. The bit length and all other timing parameters are proportional to the programmed driver frequency $f_{DRV.}$

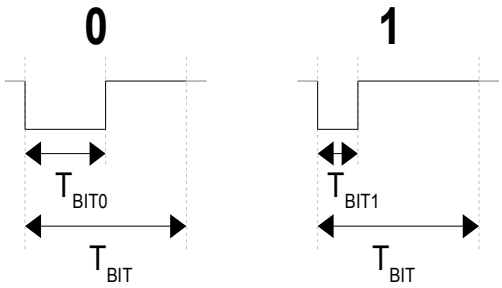


Figure 16. IO Pin Bit Encoding

E524.02

Data is sent between the E524.02 and BCU by modulating voltage on the supply wire VSUP_DATA. The block diagram in Figure 22 and Table 13 show the location and size of the external components to ensure secure bidirectional communication. During communication, tank capacitors C_{SUP2} and C_{SUP_TD} supply the E524.02 at pin VSUP.

To send data to the E524.02, the supply line voltage has to be modulated by the ECU. A voltage at the pin IO below VIO_IL will be detected as a low level, a voltage above VIO_IH as a high level. A debouncing circuit suppresses interference shorter than $T_{DEB} = 1/f_{DRV.}$

Data is transmitted from the E524.02 to the BCU by modulating pull-down current I_{PD_IO} into pin IO. I_{PD_IO} increases the supply current coming from the BCU via VSUP_DATA. Increasing I_{PD_IO} will increase the voltage drop over R_i and decrease the voltage at V_{I_BCU} which is recognized as a low level by the BCU.

Consider plug and wire resistances for VSUP_DATA and GND connecting ultrasonic module and BCU to establish proper voltage levels at pin IO.

E524.03

Data is sent between the E524.03 and BCU by pulling the single line DATA low for defined periods of time. The block diagram in Figure 23 and Table 14 show the location and size of the external components to ensure secure communication via DATA.

Incoming data to the E524.03 is recognized as a low if V_{IO} is below 1/3 of the voltage at VSUP. A de-bouncing circuit suppresses interference shorter than $T_{DEB} = 1/f_{DRV}$. Outgoing data transmission to the BCU is accomplished by pulling pin IO low overcoming pull-up resistors R_{IO_PU} and $R_{IO\_PU\_BCU}$. To reduce EMI, the slew rate pulling low is limited to SR_{VIO}. The slew rate of the rising edge is defined by external circuitry.

10 EEPROM Programming

The internal 20 bit EEPROM holds values for driver frequency and currents, filter settings, amplifier gain and noise analysis thresholds. The programming and verification via the single IO pin is done in three steps. EE_WRITE allows to pre-load initial settings. After calibration, EE_PROGRAM stores the final settings in EEPROM. To verify successful programming, EE_Read reads the register content back.

10.1 EE_WRITE Command

Both E524.02 and E524.03 are shipped with factory default settings shown in Table 12. After assembly with a transducer, the optimum values for driver frequency and current, amplifier gain and filter bandwidth are found in functional testing and calibration. The EE_WRITE command loads data into the E524.02 and E524.03 as shown in Table 12.

In EE_WRITE, data bits follow directly after the command bits. The transmitted data bits overwrite previous EEPROM data. The first bit transmitted on the IO line is bit 0 and the last bit is the LSB of AMP_GAIN (bit 19).

Table 12. EE Programming

Bit	Number of Bits	Name	Function	Default (decimal)
0	1	SPARE_BIT	EEPROM bit without internal functionality, can be used for customer specific purposes	0
1	1	IOMASK	Disable change on IO after rising edge on IO	0
2-3	2	NOISE_CFG	Noise strategy	0
4	1	FILTADJUST	Adjustment of filter bandwidth	0
5-11	7	F_DRV_ADJ	Driver frequency adjustment	Factory adjusted to f_{DRV} = 48kHz
12-15	4	DRV_CUR	Transducer current adjustment	8
16-19	4	AMP_GAIN	Amplifier gain adjustment	8

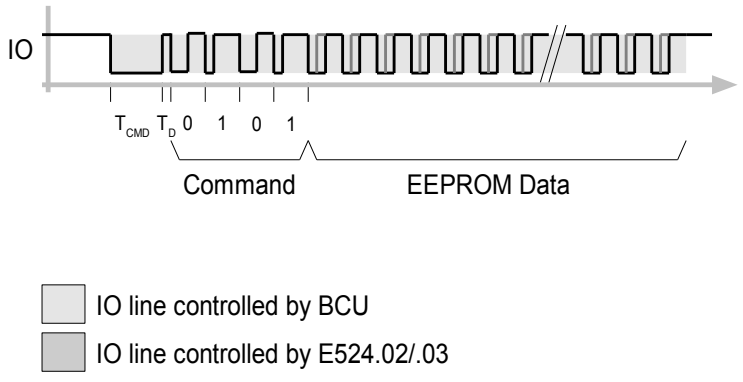


Figure 17. EE_WRITE Command

10.2 EE Programming

With the EE_Program command, the EEPROM cells are programmed with the current register contents. After sending out the command, the voltage at the IO pin has to be raised to VPROG = 25V within T_{VPROG} = 5ms. As shown in Figure 18, the programming time T_{PROG} at pin IO is 20ms.

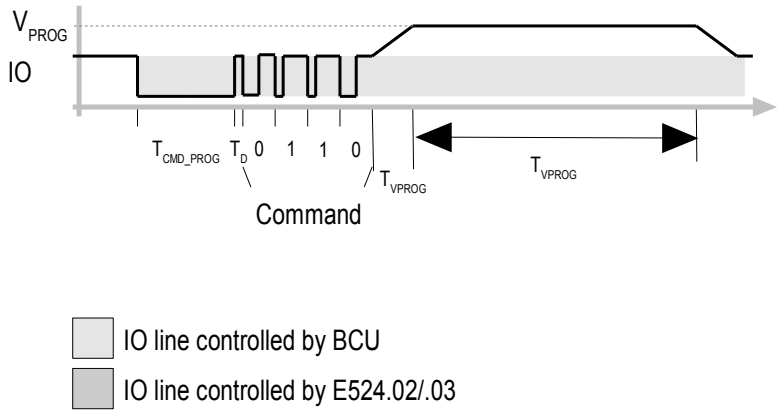


Figure 18. EE_PROGRAM Command

10.3 EE_READ Command

To verify successful programming, the EE_READ command loads EEPROM data into registers and transmits the data at the IO pin, see Figure 19. The EEPROM data is read with a nominal, low and high read voltage and presented sequentially at the output IO indicating data integrity.

Additionally, one EE_STATUS bit is appended to the end of the 20 EEPROM bits being read each time. The EE_STATUS contains the output of a comparator observing the programming voltage during programming. A high level shows the programming voltage has been within limits, a low levels indicates that the programming was not correct.

The first bit transmitted on the IO line is bit 0, the last bit is the LSB of AMP_GAIN (bit 19) and an additional bit 20 (EE_STATUS) with a nominal read voltage. The sequence is repeated with a low and a high read voltage.

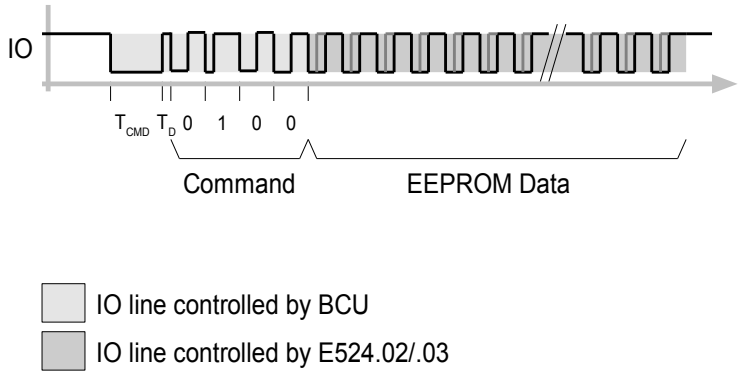


Figure 19. EE_READ Command

11 Applications Information

11.1 Supply Voltages

The E524.02 and E524.03 are designed to operate in rugged automotive environments.
The operating voltage range is 7V to 18V. VSUP is connected to the center tab of the transducer transformer and is subject to inductive kickback. Use a clamping zener diode ZD_TD as shown in Figures 22 or 23 if the voltage is close to the absolute maximum rating.

The voltage at VSUP feed internal power supplies to generate analog, digital and bias voltages. Place bypass capacitors C_{VDDA} and C_{VDDD} close to analog and digital voltage pins VDDA / GNDA and VDDD / GNDD. Both 3.3V supplies are short circuit protected and are not designed to power external loads.

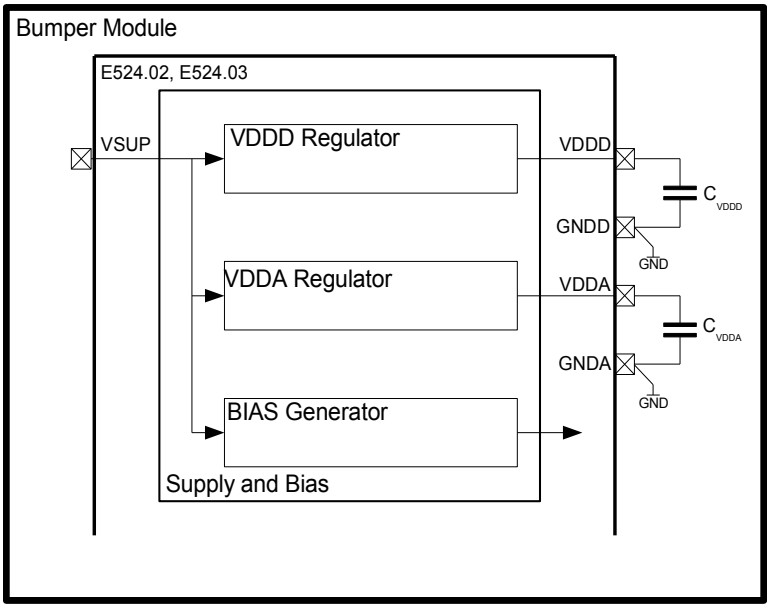


Figure 20: Supply and Bias Block Diagram

11.2 Limited performance between $V_{SUP,min}$ and $V_{SUP,PORHL}$

The digital part is running, when the power-on-reset is high. When the power-on-reset goes from high to low state, the digital part is in reset state. This results in full functionality down to $V_{SUP,min}$ and a still working digital part down to $V_{SUP,PORHL}$. Between $V_{SUP,PORHL}$ and $V_{SUP,min}$ the performance is limited, but communication with the control unit is still possible.

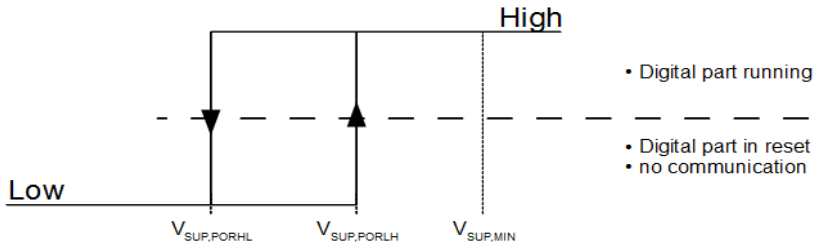


Figure 21: Power-on-reset functionality

11.3 Typical Application Circuit E524.02

The E524.02 supports a wide range of ultrasound transducers and their associated transformers. Circuit diagrams may contain components not manufactured by Elmos Semiconductor AG, which are included as means of illustrating a typical application. Elmos Semiconductor does not endorse or warrant performance specifications beyond the Electrical Characteristics for the E524.02. Please contact Elmos Semiconductor for further assistance and application notes for sizing transducer and transformer.

Figure 22 and Table 13 show the typical operating circuit and external components for the E524.02. The BCU and transducer assembly are connected with two wires VSUP_DATA and GND. Data is exchanged via shared supply line VSUP_DATA.

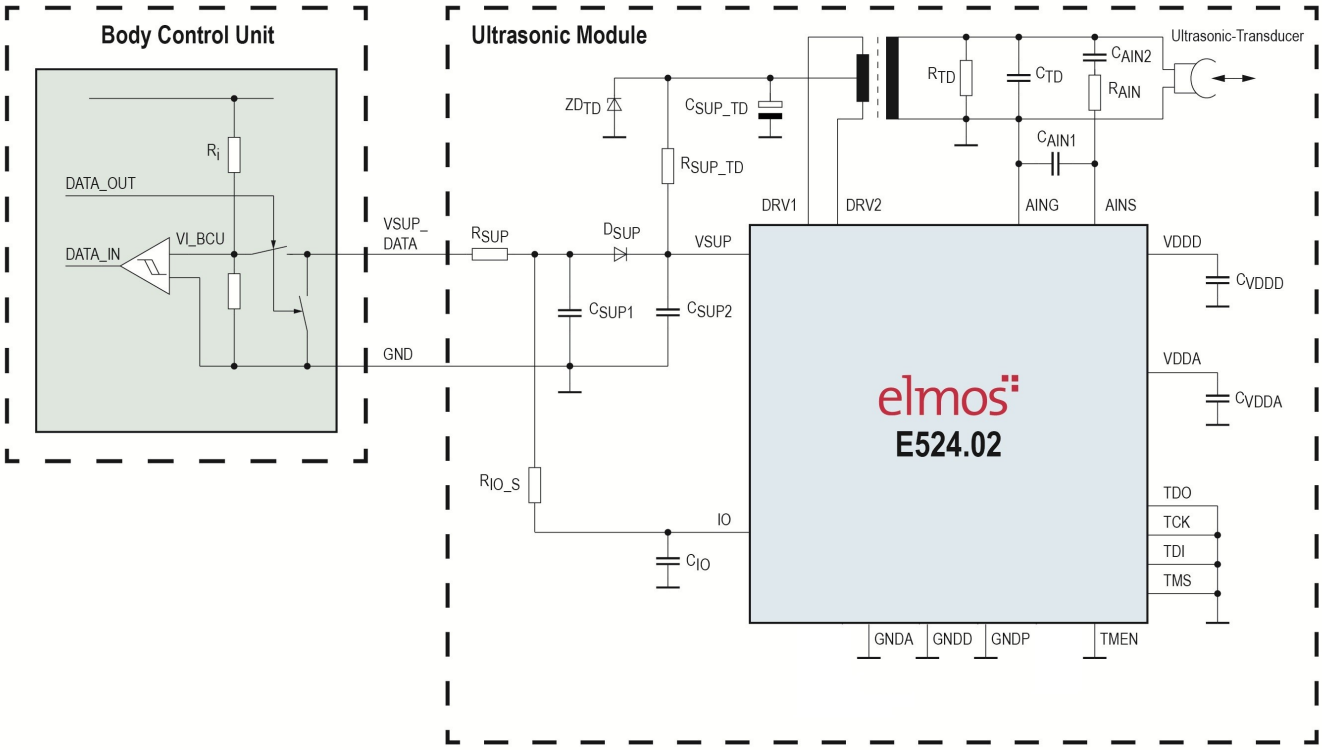


Figure 22. E524.02 Typical Application Circuit

Table 13. E524.02 External Component List

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Serial Supply Resistor	>1/3 Watt [1)]	RSUP	13	15	17	Ω
Reverse Polarity Protection Diode	BAS321 general purpose diode or equivalent	DSUP	200			$V_{Reverse}$
Blocking Supply Capacitor 1		CSUP1	1.5	2.2	2.9	nF
Blocking Supply Capacitor 2		CSUP2	150	220	300	nF
Serial Resistor for Transducer Supply	>250mW	RSUP_TD	73	82	91	Ω
Reservoir Capacitor for Transducer	Stores charge for burst, 50V, ESR<180mΩ	CSUP_TD	70	100	130	µF
Clamping Zener Diode to Clamp DRV1,2 Voltages below 40V		ZD_TD	-	25	-	V
Serial resistor for IO line	5%, 1/8W	RIO_S	135	150	165	Ω
Capacitor for IO line	10%	CIO	3.2	4.7	6.2	nF
Filter Capacitor for Transducer Signal	5%, 100V	CAIN1	7	10	13	pF
Filter Resistor for Transducer Signal	5%, 1/8W	RAIN	90	100	110	Ω
AC Coupling Capacitor for Transducer Signal	5%, 100V	CAIN2	130	330	430	pF
Blocking Capacitor for Analog Supply	10%, 50V, ESR <0.2Ω at 1MHz	CVDDA	70	100	130	nF
Blocking Capacitor for Digital Supply	10%, 50V, ESR <0.2Ω at 1MHz	CVDDD	70	100	130	nF
Transducer Resonance Resistor	5%, >100V [2)]	RTD		6.2		kΩ
Transducer Resonance Capacitor	10%, >100V [2)]	CTD		1.2		nF
Transformer	Sugg. winding ratio 1:1:7, Toko P615LN-0232ASV			2.7		mH
Transducer	Murata MA58AF14-0N			58		kHz

1) Replace resistor with inductor to achieve better EMC performance.

2) Adjust to transducer.

11.4 Typical Application Circuit E524.03

The E524.03 supports a wide range of ultrasound transducers and their associated transformers. Circuit diagrams may contain components not manufactured by Elmos Semiconductor AG, which are included as means of illustrating a typical application. Elmos Semiconductor does not endorse or warrant performance specifications beyond the Electrical Characteristics for the E524.03. Please contact Elmos Semiconductor for further assistance and application notes for sizing transducer and transformer.

The typical operational circuit for the E524.03 is shown in Figure 23, Table 14 lists external components. Three wires (GND, VSUP and DATA) connect BCU and ultrasonic module.

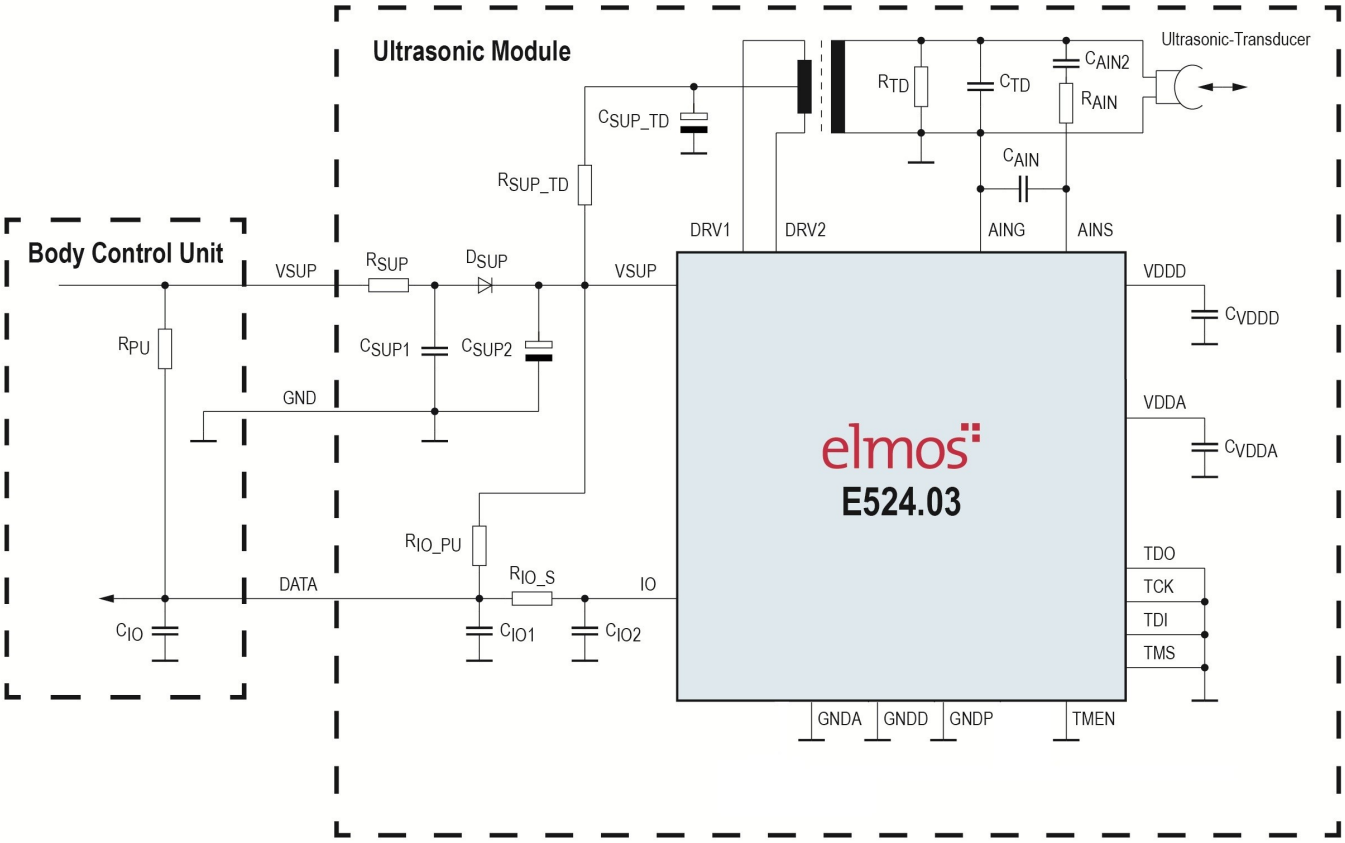


Figure 23. E524.03 Typical Operating Circuit

Table 14. E524.03 External Component List

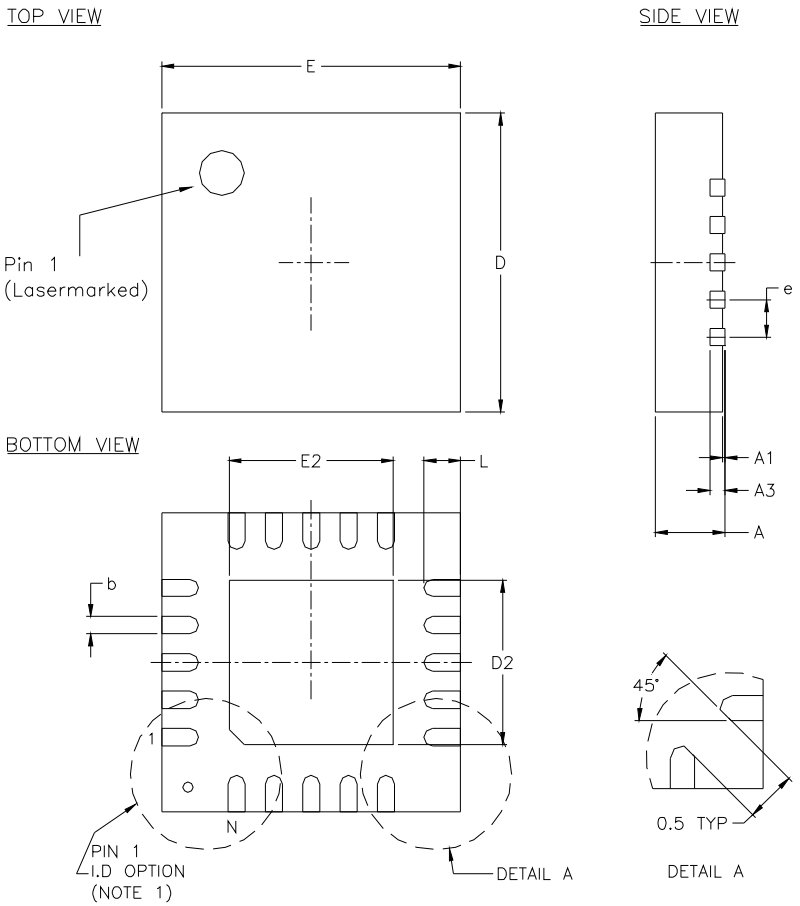
Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Serial Supply Resistor	>1/3 Watt [1)]	RSUP	13	15	17	Ω
Reverse Polarity Protection Diode	BAS321 general purpose diode or equivalent	DSUP	200			$V_{Reverse}$
Blocking Supply Capacitor 1		CSUP1	1.5	2.2	2.9	nF
Blocking Supply Capacitor 2		CSUP2	150	220	300	nF
Serial Resistor for Transducer Supply	>250mW	RSUP_TD	73	82	91	Ω
Reservoir Capacitor for Transducer	Stores charge for burst, 50V, ESR<180mΩ	CSUP_TD	70	100	130	µF
Clamping Zener Diode to Clamp DRV1,2 Voltages below 40V		ZD_TD	-	25	-	V
Serial resistor for IO line	5%, 1/8W	RIO_S	0.9	1	1.1	kΩ
Pull up resistor for IO line	5%, 1/8W	RIO_PU	9	10	11	kΩ
Capacitor for IO line	5%	CIO1	230	330	430	pF
Capacitor for IO line	10%	CIO2	1.5	2.2	2.9	nF
Filter Capacitor for Transducer Signal	5%, 100V	CAIN1	7	10	13	pF
Filter Resistor for Transducer Signal	5%, 1/8W	RAIN	90	100	110	Ω
AC Coupling Capacitor for Transducer Signal	5%, 100V	CAIN2	130	330	430	pF
Blocking Capacitor for Analog Supply	10%, 50V, ESR <0.2Ω at 1MHz	CVDDA	70	100	130	nF
Blocking Capacitor for Digital Supply	10%, 50V, ESR <0.2Ω at 1MHz	CVDDD	70	100	130	nF
Transducer Resonance Resistor	5%, >100V [2)]	RTD		6.2		kΩ
Transducer Resonance Capacitor	10%, >100V [2)]	CTD		1.2		nF
Transformer	Sugg. winding ratio 1:1:7, Toko P615LN-0232ASV			2.7		mH
Transducer	Murata MA58AF14-0N			58		kHz

1) Replace resistor with inductor to achieve better EMC performance.

2) Adjust to transducer.

12 Package Information

The E524.02 and E524.03 are available in a Pb free, RoHs compliant, QFN20L4 plastic package according to JEDEC MO-220 K, variant VGGD-5. Thermal resistance junction to ambient $R_{th,ja}$ is 33 °C/W, based on JEDEC standard JESD-51-6 and JESD-51-7.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.18	0.25	0.30	0.0071	0.0098	0.012
Package length / width	D / E	--	4.00 BSC	--	--	0.157 BSC	--
Length / width of exposed pad	D2 / E2	2.50	2.65	2.80	0.098	0.104	0.110
Lead pitch	e	--	0.50 BSC	--	--	0.020 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		20			20	

Note: Values in mm are true; dimensions in inches contain rounding errors.

13 Marking

13.1 Top Side

Elmos
52402
YWW*#
AXXXP

Table 15: Top Side marking of device E524.02

Elmos
52403
YWW*#
AXXXP

Table 16: Top Side marking of device E524.03

Signature	***Explanation***
52402 or 52403	Elmos project number
YWW	Year and week of assembly
*	Mask revision code
#	Elmos internal code
A	Elmos project revision code
XXX	Production lot number
P	Assembler code

Table 17: Explanation of marking signatures

13.2 Bottom side

No marking

WARNING – Life Support Applications Policy

Elmos Semiconductor AG is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing Elmos Semiconductor AG products, to observe standards of safety, and to avoid situations in which malfunction or failure of an Elmos Semiconductor AG Product could cause loss of human life, body injury or damage to property. In the development of your design, please ensure that Elmos Semiconductor AG products are used within specified operating ranges as set forth in the most recent product specifications.

General Disclaimer

Information furnished by Elmos Semiconductor AG is believed to be accurate and reliable. However, no responsibility is assumed by Elmos Semiconductor AG for its use, nor for any infringements of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Elmos Semiconductor AG. Elmos Semiconductor AG reserves the right to make changes to this document or the products contained therein without prior notice, to improve performance, reliability, or manufacturability .

Application Disclaimer

Circuit diagrams may contain components not manufactured by Elmos Semiconductor AG, which are included as means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. The information in the application examples has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Elmos Semiconductor AG or others.

Contact Info

Headquarters Elmos Semiconductor AG Heinrich-Hertz-Str. 1 44227 Dortmund (Germany)	Phone: +49 (0) 231 / 75 49-100 Fax: +49 (0) 231 / 75 49-149	Sales-germany@ elmos.com
Regional Sales and Application Support Office Munich Elmos Semiconductor AG Am Gefl uegelhof 12 85716 Unterschleißheim/Eching (Germany)	Phone: +49 (0) 89 / 31 83 70-0 Fax: +49 (0) 89 / 31 83 70-31	Sales-germany@ elmos.com
Sales and Application Support Office North America Elmos NA. Inc. 32255 Northwestern Highway, Suite 45 Farmington Hills, MI 48334 (United States)	Phone: +1 (0) 248 / 8 65 32 00	Sales-usa@ elmosna.com
Sales and Application Support Office Korea and Japan Elmos Korea B-1007, U-Space 2, #670 Daewangpangyo-ro, Sampyoung-dong, Bunddang-gu, Sungnam-si Kyounggi-do 463-400 Korea	Phone: +82 (0)31 / 7 14 11 31	Sales-korea@ elmos.com
Sales and Application Support Office China Elmos Semiconductor Technology (Shanghai) Co., Ltd. Unit London, 1BF GC Tower, No. 1088 YuanShen Road, Pudong New District, Shanghai, PR China, 200122	Phone: +86 (0) 21 / 51 78 51 88	Sales-china@ elmos.com
Sales and Application Support Office Singapore Elmos Semiconductor Singapore Pte Ltd. 60 Alexandra Terrace 09-31 The Comtech Singapore 118502	Phone: +65 (0) 663 / 5 11 41 Fax: +65 (0) 663 / 5 11 40	Sales-singapore@ elmos.com