JOSÉ DELFIM RIBEIRO VALVERDE

8th July 1994 | https://dvalverde.com | Porto, Portugal | https://linkedin.com/in/jdelfimvalverde/

WORK EXPERIENCE

ASIC Digital Design Engr, Staff Engineer

Synopsys Inc, Porto

June 2017 – Ongoing | Porto, Portugal

Digital Designer in a mixed signal IP design team developing (System) Verilog blocks implementing Consumer and Enterprise SERDES PHYs for commonly used communication protocols (f.e PCIE/USB/Ethernet)

- Enrolled in focus groups specialized in the development of optimized solutions for High-Speed (112/224Gbps) SERDES designs to reduce power and BER
- Study and implementations of DSP specialized blocks like MSLD and FFE/DFE architectures
- Lead designer on Consumer grade SERDES digital designs: implementation of new features and debugging already implement features on the client side
- Worked in joint teams of analog and digital designers to design (Analog modeling and Digital Front-End using Verilog) and Verify (creation and analysis of System Verilog Testbench) mixed signal designs
- Usage and implementation of physical design flows on Synopsys tools - Synthesis with DFT (Design Compiler/Fusion Compiler), Static Timing Analysis (PrimeTime). Collaborating with backend teams to P&R 13nm to 3nm designs
- Hands-on on CDC and RDC analysis (Spyglass / VC Spyglass)
- Focus on implementing new DFT technologies (Stuck at, TDF, OCC, Boundary Scan), and implementing flows for verification using Synopsys tools (TMAX)
- On-call client support for debugs and SoC implementation
- Exposed to scripting languages like TCL, Python, Bash/Shell to optimize verification and releasing time
- Using DevOps expertise (mainly Jenkins) to implement new release and testing solutions for ongoing project

Summer Intern

Synopsys Inc

July 2016 – September 2016 | Porto, Portugal

- Developed Python scripts to aid the design and verification of digital blocks
- Designed Clock Gating insertion techniques for digital designs: using Design Compiler and RTL optimization on existing designs

Teaching Assistant

Faculdade de Engenharia da U.Porto

September 2015 – February 2016 | Porto, Portugal

- Conducted classroom practical C Programming classes to first-year students, Assessed student performance and holding occasional doubt clearing sessions

PROJECTS/HOBBYS

Personal Projects

Ongoing

- **Home automation**: Using micro-controller (Raspberry) and microprocessors (Arduino) combining multiple DevOps techniques: using Python, JavaScript (NodeJS) and Jenkins

Faculdade de Engenharia da U.Porto

September 2014 – September 2016 | Porto, Portugal

- **Straplex Program – Software/Microcontroller Engineer**: Development and maintenance of Stratosphere balloons software controllers (Arduinos/Rasperry) / Participation on BEXUS ESA program
- **Student council – Vowal**: Head of Logistical Department

EDUCATION

M.Sc. in Electrical and Computers Engineering

Faculdade de Engenharia da U.Porto

September 2012 – December 2016

- Telecommunications, Electronics and Computers: Microelectronics and Embedded Systems

Faculdade de Engenharia da U.Porto & Synopsys Inc, Porto

January 2017 – June 2017

- **Thesis Title:** Automatic implementation of a re-configurable logic over ASIC design flow
- Implementation of a FPGA type design in a ASIC to reduced time-to-market and increase the ability to debug designs

SKILLS

Programming Languages

(System) Verilog | Python | TCL | Shell Scripting(Bash) | Perl | HTML/CSS/Javascript(nodejs) | C

IC Tools

Design Compiler/Fusion Compiler | Prime-Time | DFT compiler | TMAX | VCS | Verdi | NCV | Cadence Virtuoso

Databases

MySQL | PostgreSQL

Version

Perforce | Git | Subversion

DevOps

Jenkins | Travis CI

SOFTSKILLS

Open-mindedness | Critical Thinking | Problem Solving | Creativity | Adaptability | Friendly Personality

LANGUAGES

Portuguese
English
Spanish