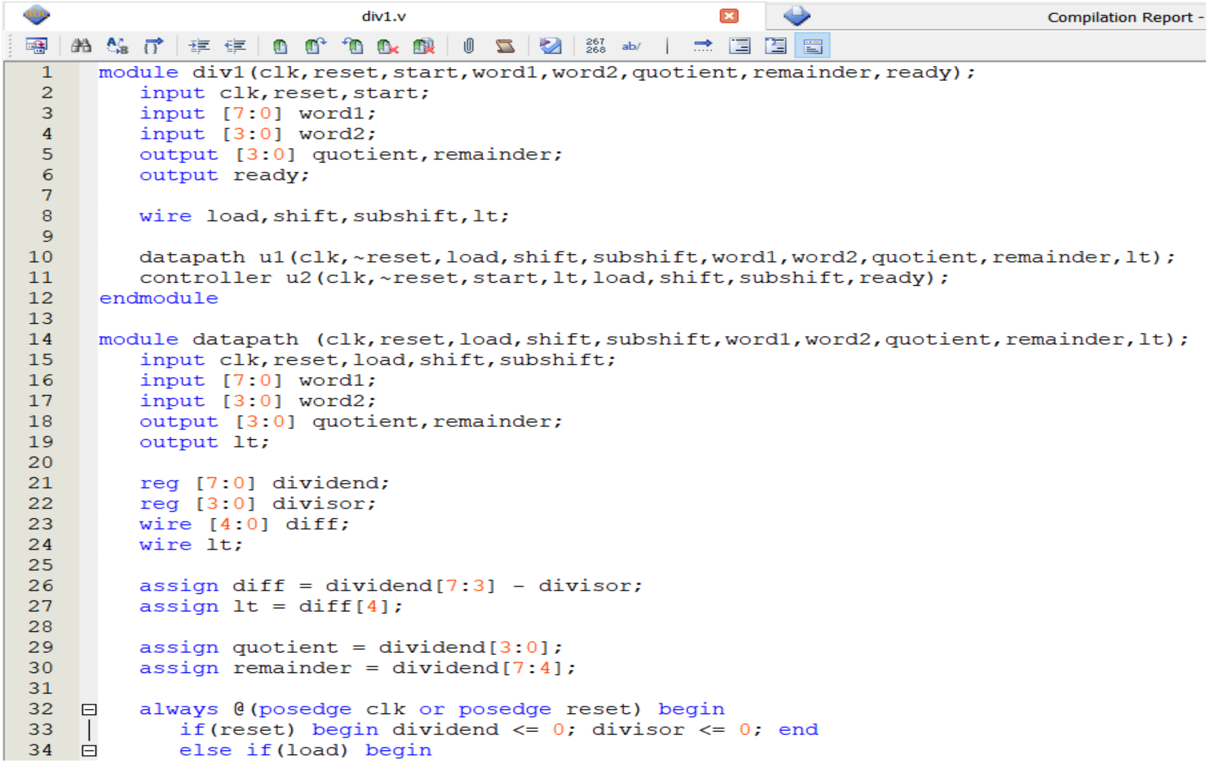
< 실습과제 8 >

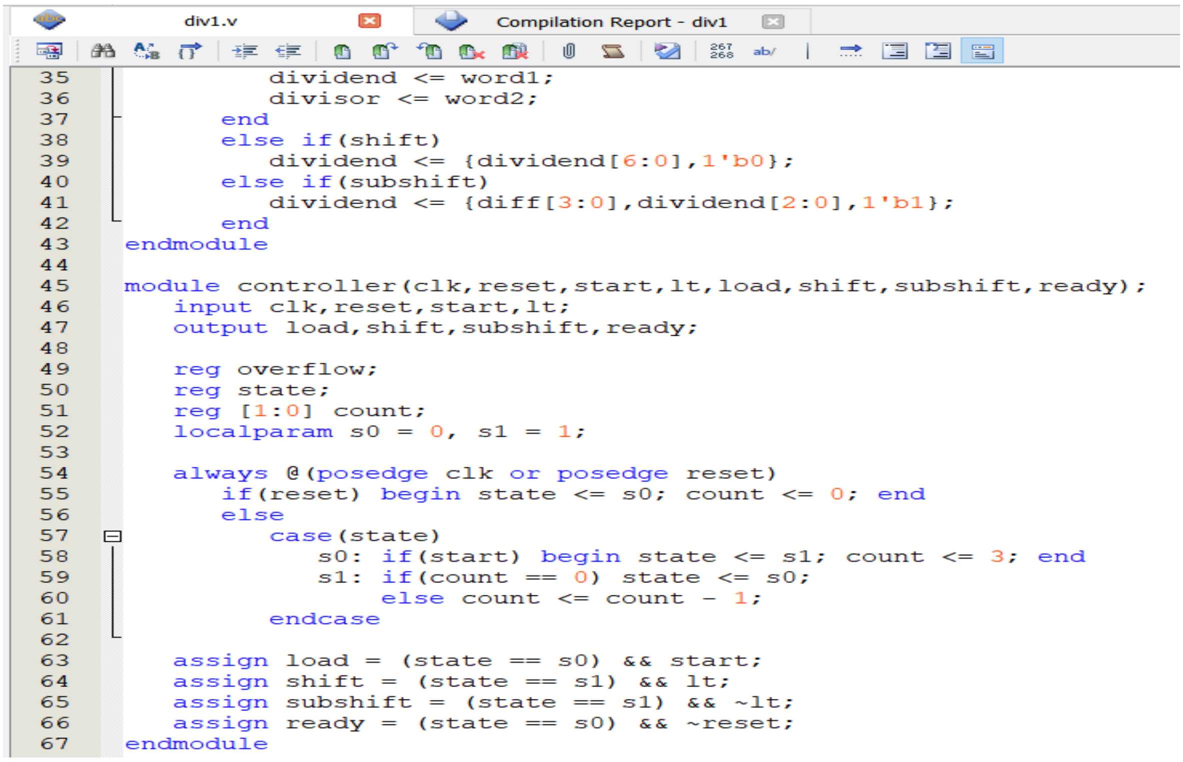
2017253041 홍성우

1..

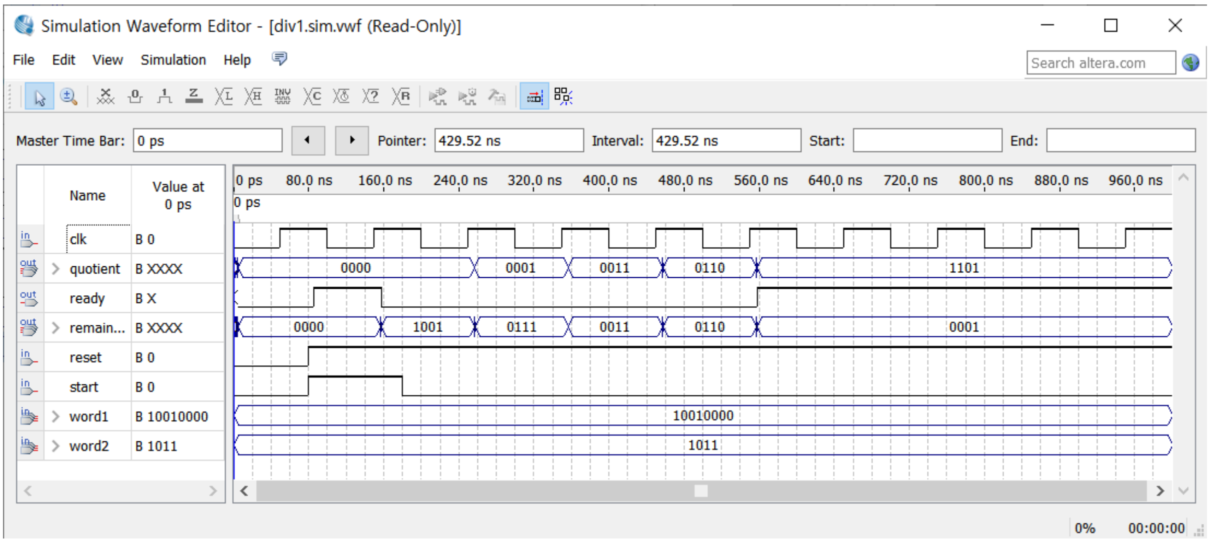
(1)



```
module div1(clk,reset,start,word1,word2,quotient,remainder,ready);
   input clk,reset,start;
   input [7:0] word1;
   input [3:0] word2;
   output [3:0] quotient,remainder;
   output ready;

   wire load,shift,subshift,lt;

   datapath u1(clk,~reset,load,shift,subshift,word1,word2,quotient,remainder,lt);
   controller u2(clk,~reset,start,lt,load,shift,subshift,ready);
endmodule

module datapath (clk,reset,load,shift,subshift,word1,word2,quotient,remainder,lt);
   input clk,reset,load,shift,subshift;
   input [7:0] word1;
   input [3:0] word2;
   output [3:0] quotient,remainder;
   output lt;

   reg [7:0] dividend;
   reg [3:0] divisor;
   wire [4:0] diff;
   wire lt;

   assign diff = dividend[7:3] - divisor;
   assign lt = diff[4];

   assign quotient = dividend[3:0];
   assign remainder = dividend[7:4];

   always @(posedge clk or posedge reset) begin
      if(reset) begin dividend <= 0; divisor <= 0; end
      else if(load) begin
```

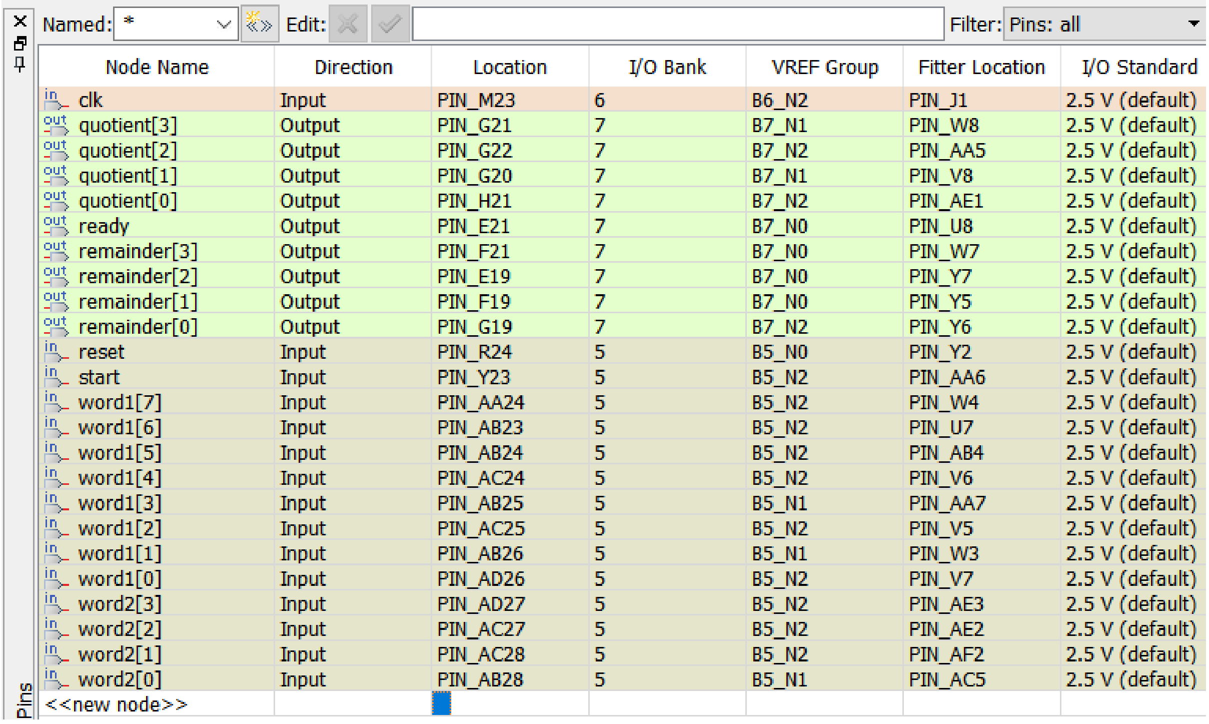


```
         dividend <= word1;
         divisor <= word2;
      end
      else if(shift)
         dividend <= {dividend[6:0],1'b0};
      else if(subshift)
         dividend <= {diff[3:0],dividend[2:0],1'b1};
      end
endmodule

module controller(clk,reset,start,lt,load,shift,subshift,ready);
   input clk,reset,start,lt;
   output load,shift,subshift,ready;

   reg overflow;
   reg state;
   reg [1:0] count;
   localparam s0 = 0, s1 = 1;

   always @(posedge clk or posedge reset)
      if(reset) begin state <= s0; count <= 0; end
      else
         case(state)
            s0: if(start) begin state <= s1; count <= 3; end
            s1: if(count == 0) state <= s0;
                else count <= count - 1;
         endcase

   assign load = (state == s0) && start;
   assign shift = (state == s1) && lt;
   assign subshift = (state == s1) && ~lt;
   assign ready = (state == s0) && ~reset;
endmodule
```


Simulation Waveform Editor - [div1.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 429.52 ns
Interval: 429.52 ns
Start:
End:
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0 ps
0000
0001
0011
0110
1101
0000
1001
0111
0011
0110
0001
10010000
1011
0%
00:00:00

Name	Value at 0 ps
clk	B 0
quotient	B XXXX
ready	B X
remain...	B XXXX
reset	B 0
start	B 0
word1	B 10010000
word2	B 1011

(2)



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
clk	Input	PIN_M23	6	B6_N2	PIN_J1	2.5 V (default)
quotient[3]	Output	PIN_G21	7	B7_N1	PIN_W8	2.5 V (default)
quotient[2]	Output	PIN_G22	7	B7_N2	PIN_AA5	2.5 V (default)
quotient[1]	Output	PIN_G20	7	B7_N1	PIN_V8	2.5 V (default)
quotient[0]	Output	PIN_H21	7	B7_N2	PIN_AE1	2.5 V (default)
ready	Output	PIN_E21	7	B7_N0	PIN_U8	2.5 V (default)
remainder[3]	Output	PIN_F21	7	B7_N0	PIN_W7	2.5 V (default)
remainder[2]	Output	PIN_E19	7	B7_N0	PIN_Y7	2.5 V (default)
remainder[1]	Output	PIN_F19	7	B7_N0	PIN_Y5	2.5 V (default)
remainder[0]	Output	PIN_G19	7	B7_N2	PIN_Y6	2.5 V (default)
reset	Input	PIN_R24	5	B5_N0	PIN_Y2	2.5 V (default)
start	Input	PIN_Y23	5	B5_N2	PIN_AA6	2.5 V (default)
word1[7]	Input	PIN_AA24	5	B5_N2	PIN_W4	2.5 V (default)
word1[6]	Input	PIN_AB23	5	B5_N2	PIN_U7	2.5 V (default)
word1[5]	Input	PIN_AB24	5	B5_N2	PIN_AB4	2.5 V (default)
word1[4]	Input	PIN_AC24	5	B5_N2	PIN_V6	2.5 V (default)
word1[3]	Input	PIN_AB25	5	B5_N1	PIN_AA7	2.5 V (default)
word1[2]	Input	PIN_AC25	5	B5_N2	PIN_V5	2.5 V (default)
word1[1]	Input	PIN_AB26	5	B5_N1	PIN_W3	2.5 V (default)
word1[0]	Input	PIN_AD26	5	B5_N2	PIN_V7	2.5 V (default)
word2[3]	Input	PIN_AD27	5	B5_N2	PIN_AE3	2.5 V (default)
word2[2]	Input	PIN_AC27	5	B5_N2	PIN_AE2	2.5 V (default)
word2[1]	Input	PIN_AC28	5	B5_N2	PIN_AF2	2.5 V (default)
word2[0]	Input	PIN_AB28	5	B5_N1	PIN_AC5	2.5 V (default)
<<new node>>						

start -> SW[17]

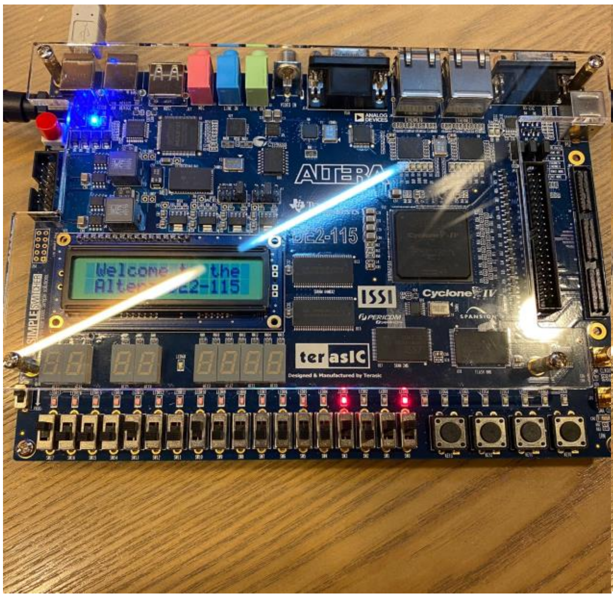
reset -> KEY[3]

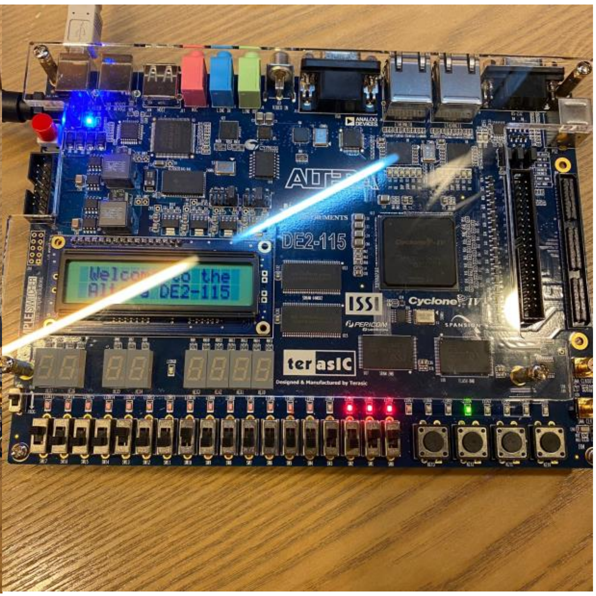
clk -> KEY[0]

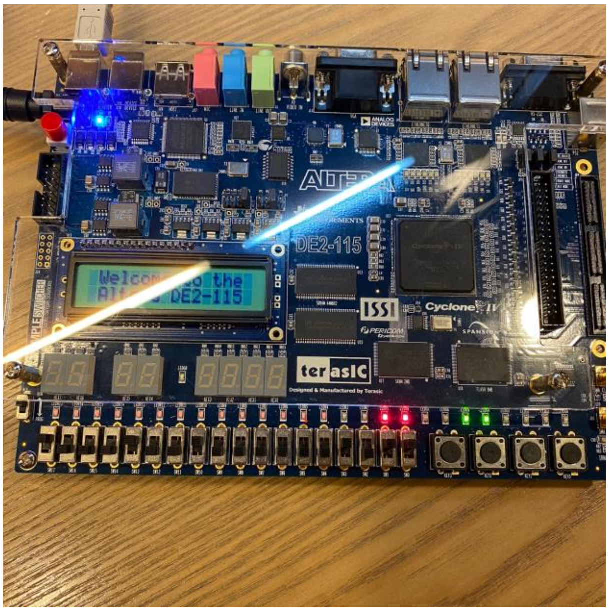
ready -> LEDG[0]

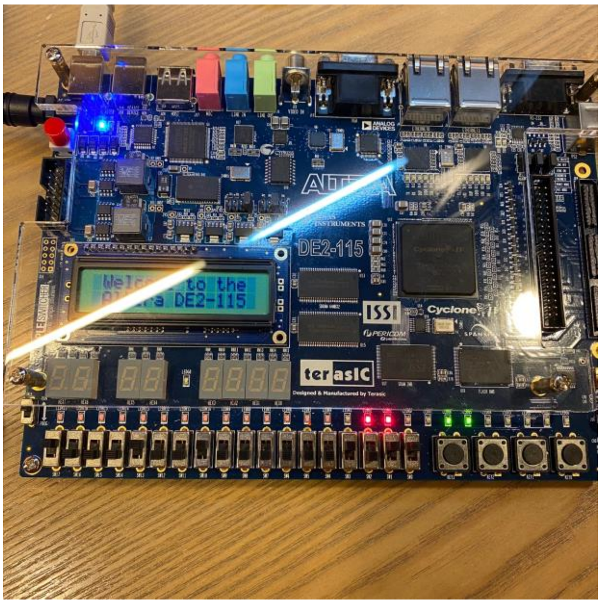
word1 -> SW[13] ~ SW[6]

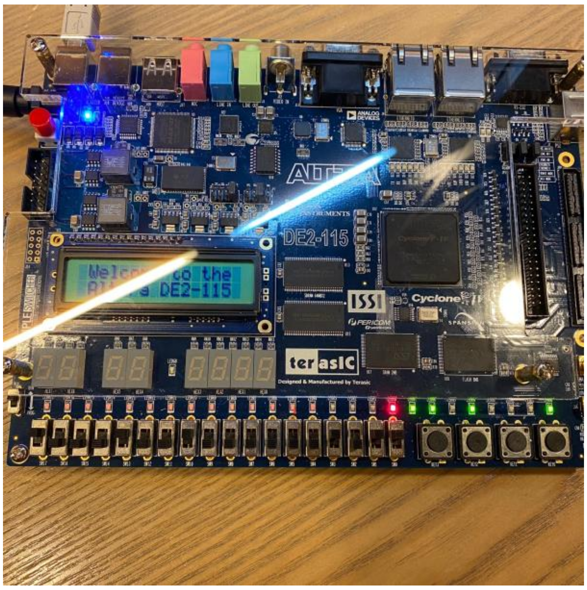
word2 -> SW[3] ~ SW[0]







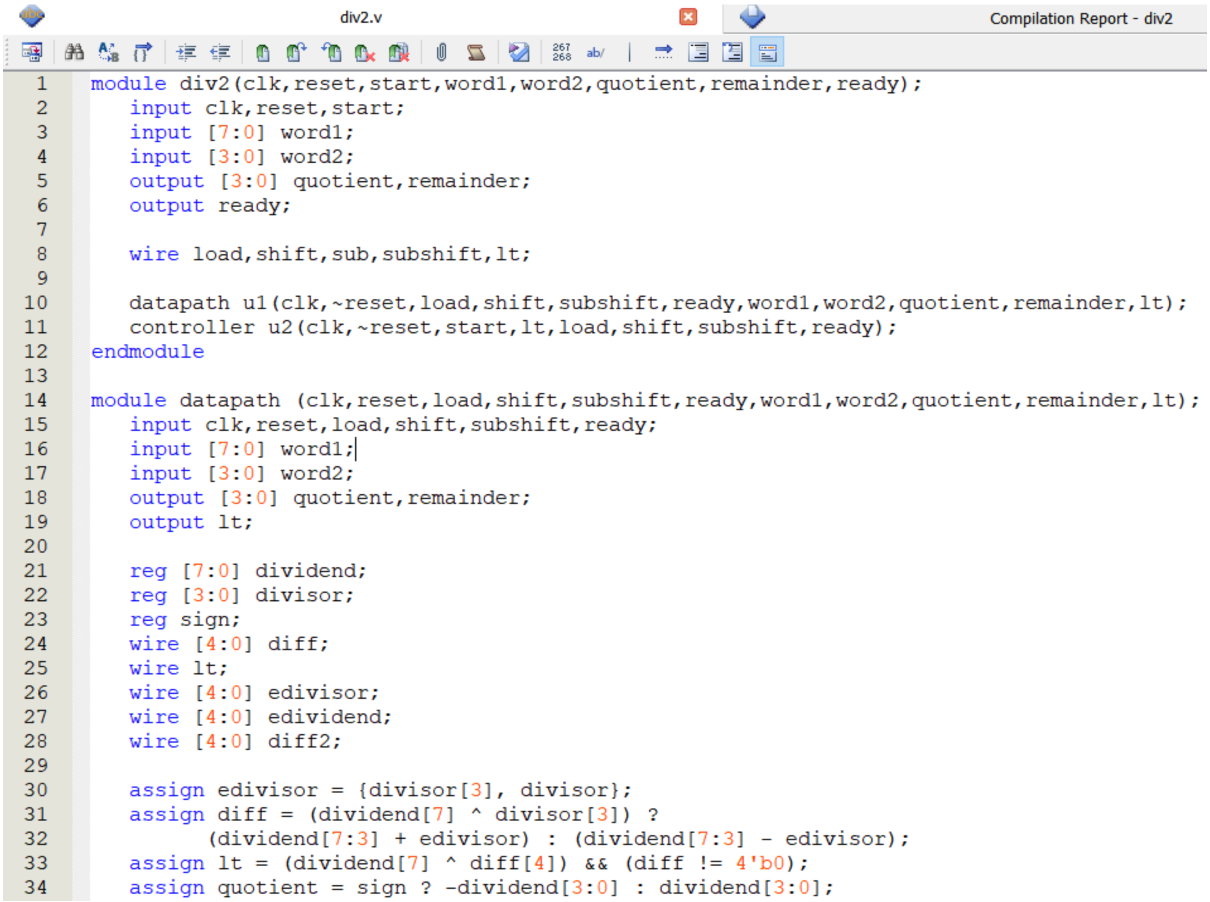




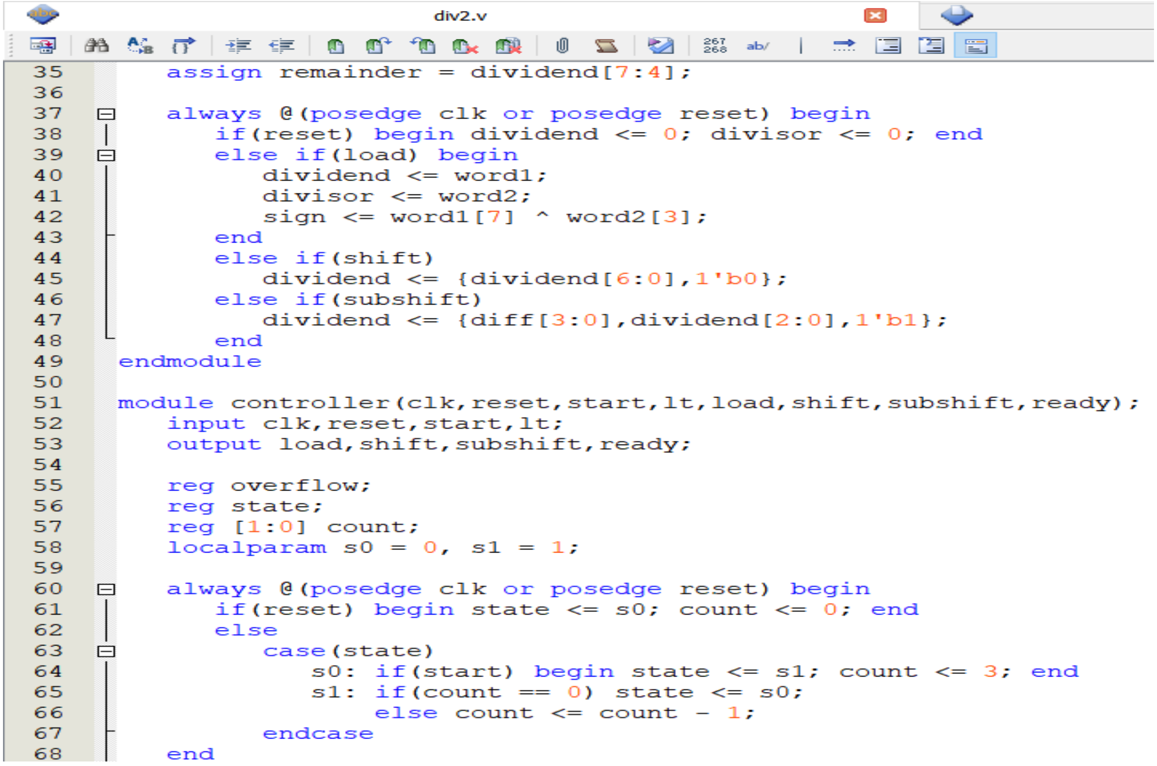
-> 144 / 11 = 13 1

2.

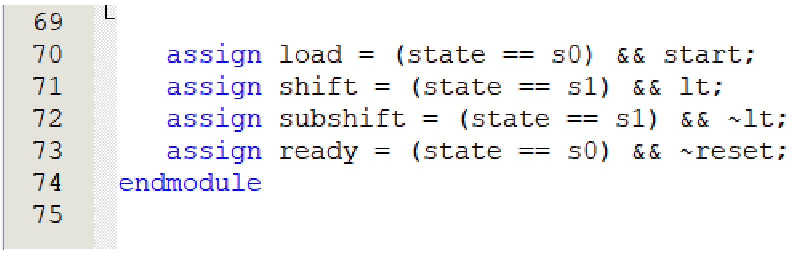
(1)



```
module div2(clk,reset,start,word1,word2,quotient,remainder,ready);
   input clk,reset,start;
   input [7:0] word1;
   input [3:0] word2;
   output [3:0] quotient,remainder;
   output ready;

   wire load,shift,sub,subshift,lt;

   datapath u1(clk,~reset,load,shift,subshift,ready,word1,word2,quotient,remainder,lt);
   controller u2(clk,~reset,start,lt,load,shift,subshift,ready);
endmodule

module datapath (clk,reset,load,shift,subshift,ready,word1,word2,quotient,remainder,lt);
   input clk,reset,load,shift,subshift,ready;
   input [7:0] word1;
   input [3:0] word2;
   output [3:0] quotient,remainder;
   output lt;

   reg [7:0] dividend;
   reg [3:0] divisor;
   reg sign;
   wire [4:0] diff;
   wire lt;
   wire [4:0] edivisor;
   wire [4:0] edividend;
   wire [4:0] diff2;

   assign edivisor = {divisor[3], divisor};
   assign diff = (dividend[7] ^ divisor[3]) ?
         (dividend[7:3] + edivisor) : (dividend[7:3] - edivisor);
   assign lt = (dividend[7] ^ diff[4]) && (diff != 4'b0);
   assign quotient = sign ? -dividend[3:0] : dividend[3:0];
```

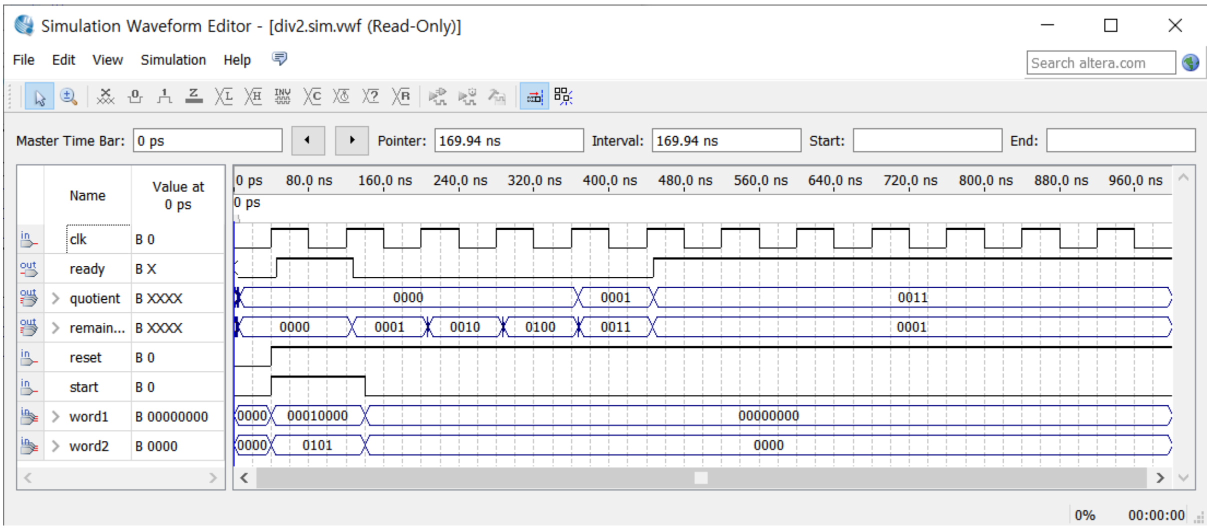


```
   assign remainder = dividend[7:4];

   always @(posedge clk or posedge reset) begin
      if(reset) begin dividend <= 0; divisor <= 0; end
      else if(load) begin
         dividend <= word1;
         divisor <= word2;
         sign <= word1[7] ^ word2[3];
      end
      else if(shift)
         dividend <= {dividend[6:0],1'b0};
      else if(subshift)
         dividend <= {diff[3:0],dividend[2:0],1'b1};
      end
endmodule

module controller(clk,reset,start,lt,load,shift,subshift,ready);
   input clk,reset,start,lt;
   output load,shift,subshift,ready;

   reg overflow;
   reg state;
   reg [1:0] count;
   localparam s0 = 0, s1 = 1;

   always @(posedge clk or posedge reset) begin
      if(reset) begin state <= s0; count <= 0; end
      else
         case(state)
            s0: if(start) begin state <= s1; count <= 3; end
            s1: if(count == 0) state <= s0;
                else count <= count - 1;
         endcase
   end
```



```
    assign load = (state == s0) && start;
    assign shift = (state == s1) && lt;
    assign subshift = (state == s1) && ~lt;
    assign ready = (state == s0) && ~reset;
endmodule
```

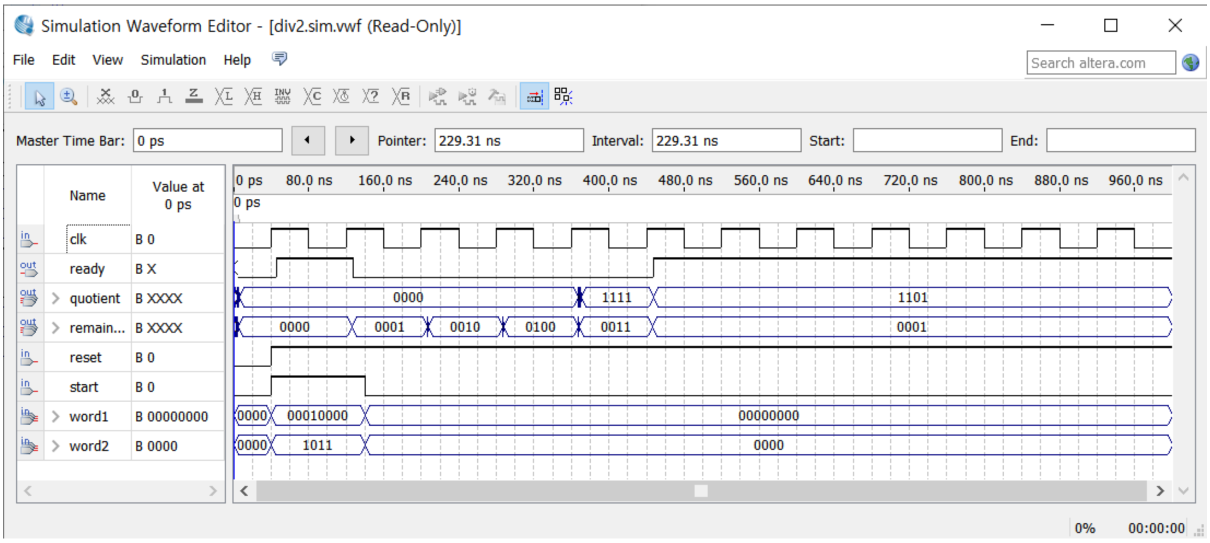
(양수/양수) -> (16 / 5 = 3 ...1)



Master Time Bar: 0 ps Pointer: 169.94 ns Interval: 169.94 ns Start: End:

Name	Value at 0 ps
clk	B 0
ready	B X
quotient	B XXXX
remain...	B XXXX
reset	B 0
start	B 0
word1	B 00000000
word2	B 0000

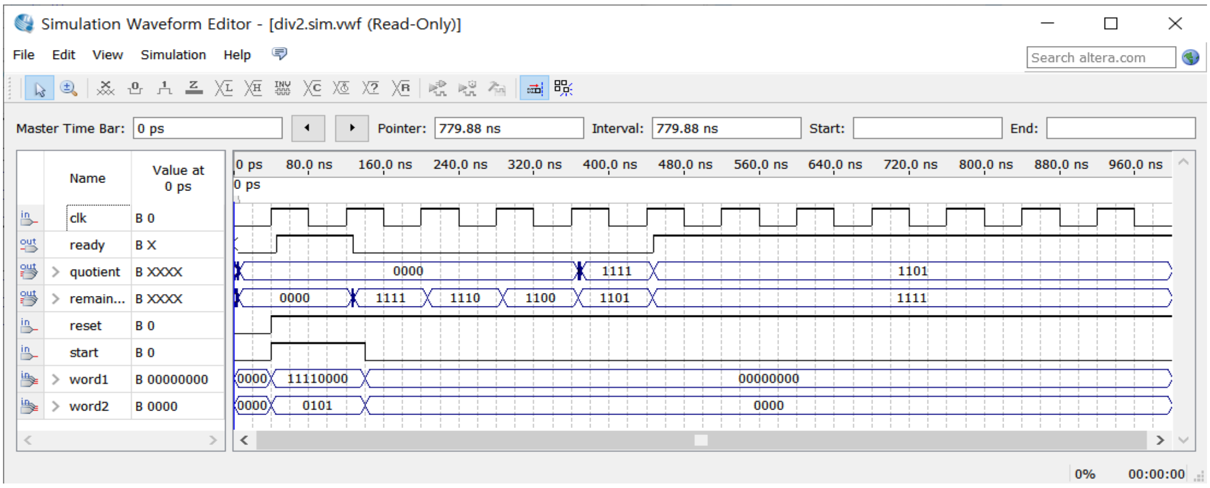
(양수/음수) -> (16 / -5 = -3 ...1)



Master Time Bar: 0 ps Pointer: 229.31 ns Interval: 229.31 ns Start: End:

Name	Value at 0 ps
clk	B 0
ready	B X
quotient	B XXXX
remain...	B XXXX
reset	B 0
start	B 0
word1	B 00000000
word2	B 0000

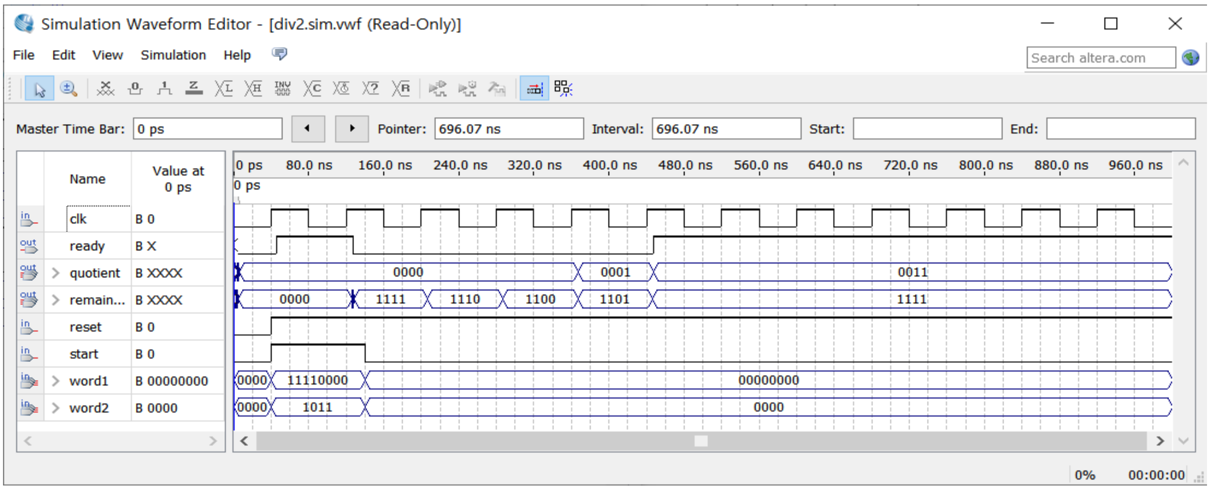
(음수/양수) -> (-16 / 5 = -3 ...-1)



Simulation Waveform Editor - [div2.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 779.88 ns Interval: 779.88 ns Start: End:

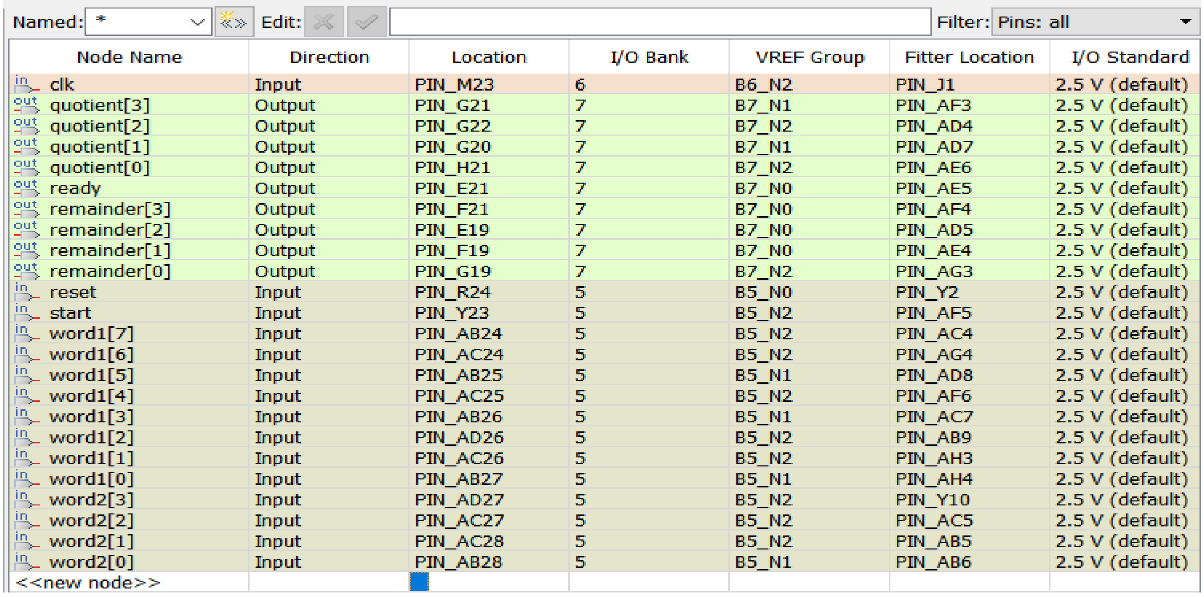
(음수/음수) -> (-16 / -5 = 3 ...-1)



Simulation Waveform Editor - [div2.sim.vwf (Read-Only)]

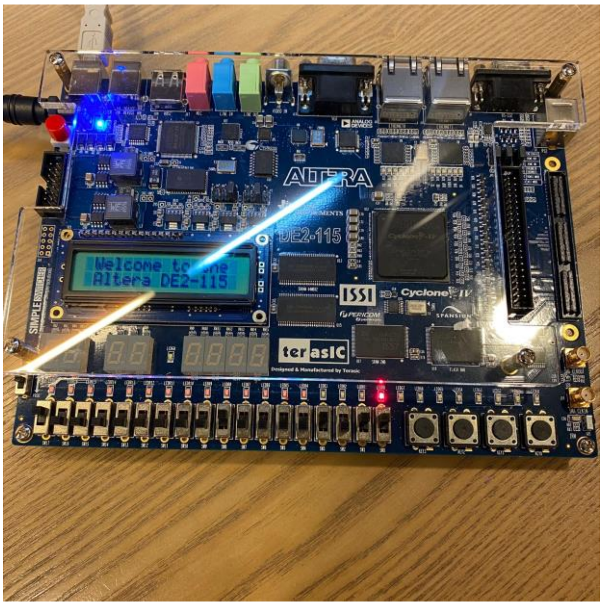
Master Time Bar: 0 ps Pointer: 696.07 ns Interval: 696.07 ns Start: End:

(2)



Named: * Edit: Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
clk	Input	PIN_M23	6	B6_N2	PIN_J1	2.5 V (default)
quotient[3]	Output	PIN_G21	7	B7_N1	PIN_AF3	2.5 V (default)
quotient[2]	Output	PIN_G22	7	B7_N2	PIN_AD4	2.5 V (default)
quotient[1]	Output	PIN_G20	7	B7_N1	PIN_AD7	2.5 V (default)
quotient[0]	Output	PIN_H21	7	B7_N2	PIN_AE6	2.5 V (default)
ready	Output	PIN_E21	7	B7_N0	PIN_AE5	2.5 V (default)
remainder[3]	Output	PIN_F21	7	B7_N0	PIN_AF4	2.5 V (default)
remainder[2]	Output	PIN_E19	7	B7_N0	PIN_AD5	2.5 V (default)
remainder[1]	Output	PIN_F19	7	B7_N0	PIN_AE4	2.5 V (default)
remainder[0]	Output	PIN_G19	7	B7_N2	PIN_AG3	2.5 V (default)
reset	Input	PIN_R24	5	B5_N0	PIN_Y2	2.5 V (default)
start	Input	PIN_Y23	5	B5_N2	PIN_AF5	2.5 V (default)
word1[7]	Input	PIN_AB24	5	B5_N2	PIN_AC4	2.5 V (default)
word1[6]	Input	PIN_AC24	5	B5_N2	PIN_AG4	2.5 V (default)
word1[5]	Input	PIN_AB25	5	B5_N1	PIN_AD8	2.5 V (default)
word1[4]	Input	PIN_AC25	5	B5_N2	PIN_AF6	2.5 V (default)
word1[3]	Input	PIN_AB26	5	B5_N1	PIN_AC7	2.5 V (default)
word1[2]	Input	PIN_AD26	5	B5_N2	PIN_AB9	2.5 V (default)
word1[1]	Input	PIN_AC26	5	B5_N2	PIN_AH3	2.5 V (default)
word1[0]	Input	PIN_AB27	5	B5_N1	PIN_AH4	2.5 V (default)
word2[3]	Input	PIN_AD27	5	B5_N2	PIN_Y10	2.5 V (default)
word2[2]	Input	PIN_AC27	5	B5_N2	PIN_AC5	2.5 V (default)
word2[1]	Input	PIN_AC28	5	B5_N2	PIN_AB5	2.5 V (default)
word2[0]	Input	PIN_AB28	5	B5_N1	PIN_AB6	2.5 V (default)
<<new node>>						


Welcome to the
Altera DE2-115
ALTERA
DE2-115
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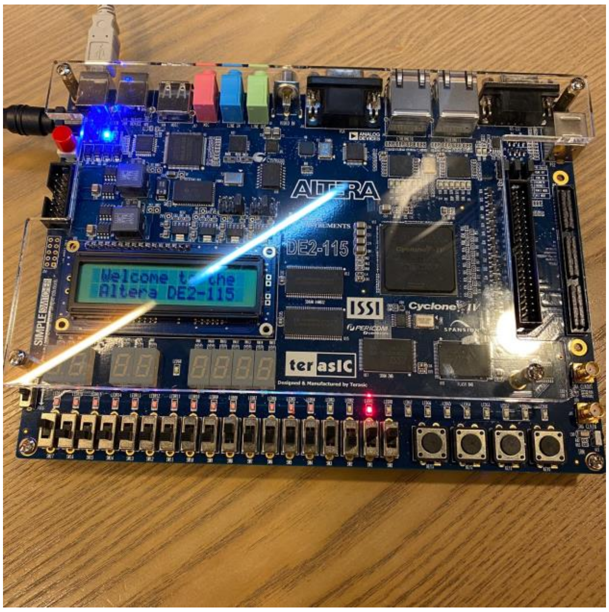
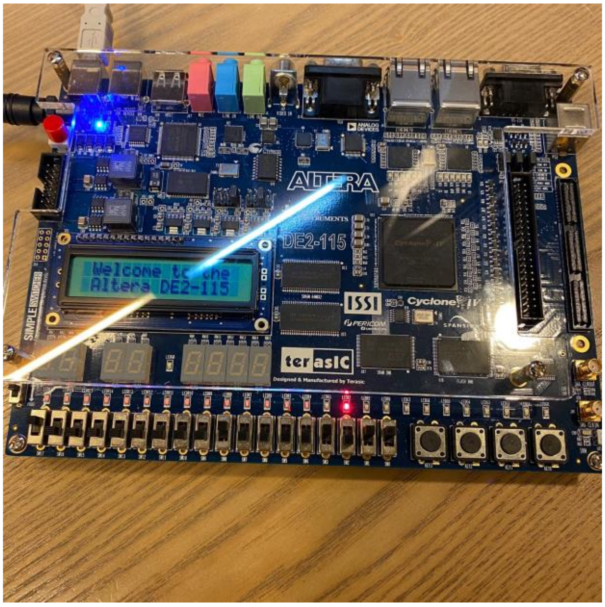
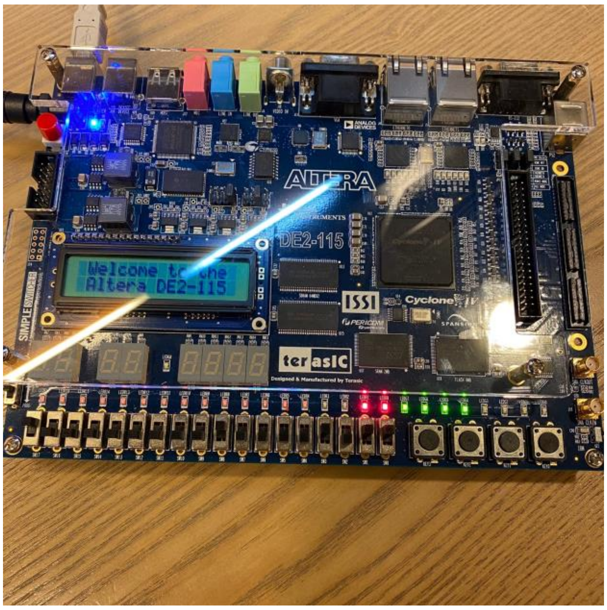
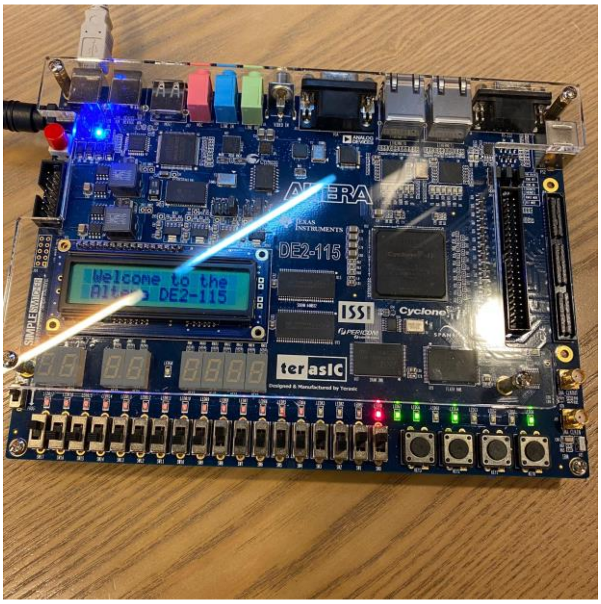
Cyclone IV


Welcome to the
Altera DE2-115
ALTERA
DE2-115
terasIC
Cyclone IV


Welcome to the
Altera DE2-115
ALTERA
DE2-115
terasIC
Cyclone IV


Welcome to the
Altera DE2-115
ALTERA
DE2-115
terasIC
Cyclone IV


Welcome to the
Altera DE2-115
ALTERA
DE2-115
terasIC
Cyclone IV

-> 16 / -5 = -3 1

start -> SW[17]

reset -> KEY[3]

clk -> KEY[0]

ready -> LEDG[0]

word1 -> SW[11] ~ SW[4]

word2 -> SW[3] ~ SW[0]