< 실습과제 2 >

2017253041_홍성우

#1

(1)

mux2_4.v - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module mux2_4(y,data1,data0,select);
        output [3:0] y;
        input [3:0] data1,data0;
        input select;
        assign y = select ? data1 : data0;
endmodule
```

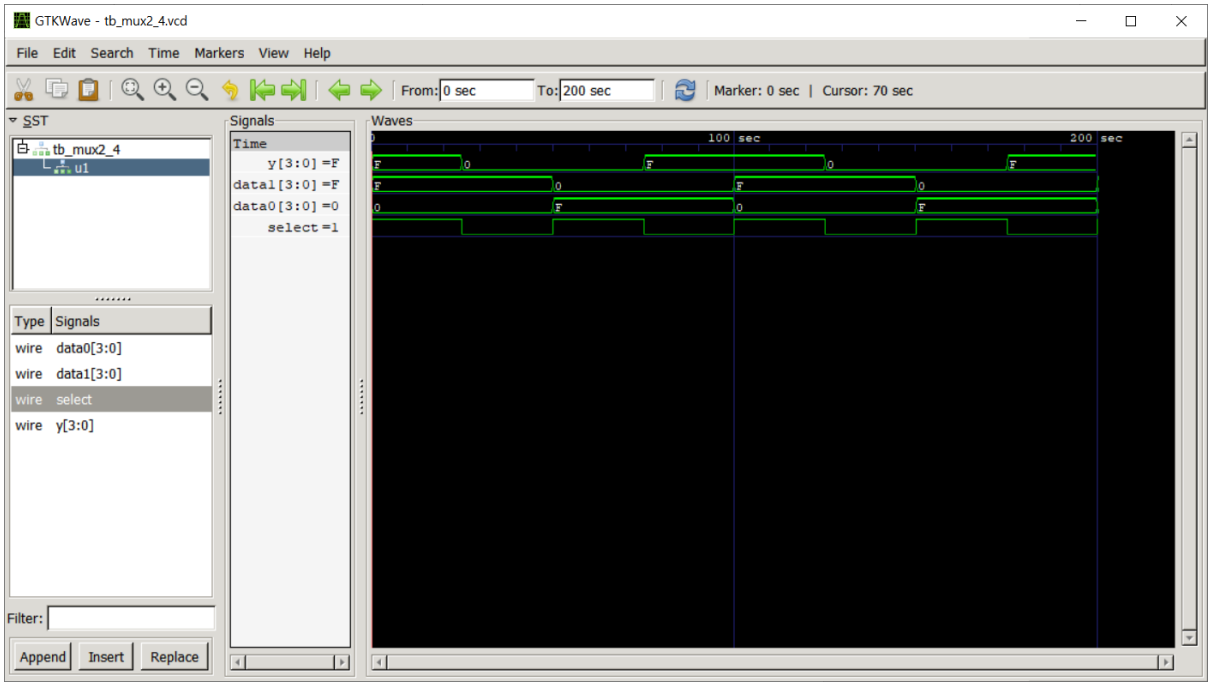
Ln 1, Col 1 100% Windows (CRLF) UTF-8

tb_mux2_4.v - Windows 메모장

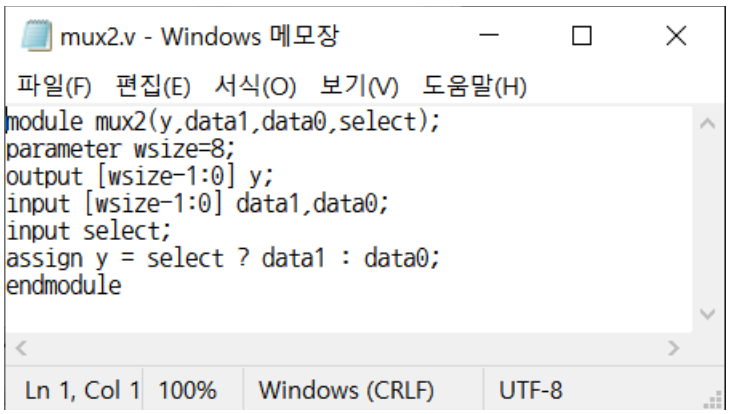
파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module tb_mux2_4();
wire [3:0] y;
reg [3:0] data1,data0;
reg select;

mux2_4 u1(y,data1,data0,select);

initial begin
data1=4'b1111;data0=4'b0000;select=1'b1;
#200
$finish;
end

initial begin
$dumpfile("tb_mux2_4.vcd");
$dumpvars(0,u1);
end

initial begin
#25 select=0;
#25 data1=4'b0000;data0=4'b1111;select=1'b1;
#25 select=1'b0;
#25 data1=4'b1111;data0=4'b0000;select=1'b1;
#25 select=1'b0;
#25 data1=4'b0000;data0=4'b1111;select=1'b1;
#25 select=1'b0;
#25 data1=4'b1111;data0=4'b0000;select=1'b1;
end
endmodule
```

Ln 27, Col 100% Windows (CRLF) UTF-8


GTKWave - tb_mux2_4.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 200 sec
Marker: 0 sec | Cursor: 70 sec
SST
tb_mux2_4
u1
Type Signals
wire data0[3:0]
wire data1[3:0]
wire select
wire y[3:0]
Filter:
Append Insert Replace
Signals
Time
y[3:0] =F
data1[3:0] =F
data0[3:0] =0
select =1
Waves
100 sec
200 sec

(2)

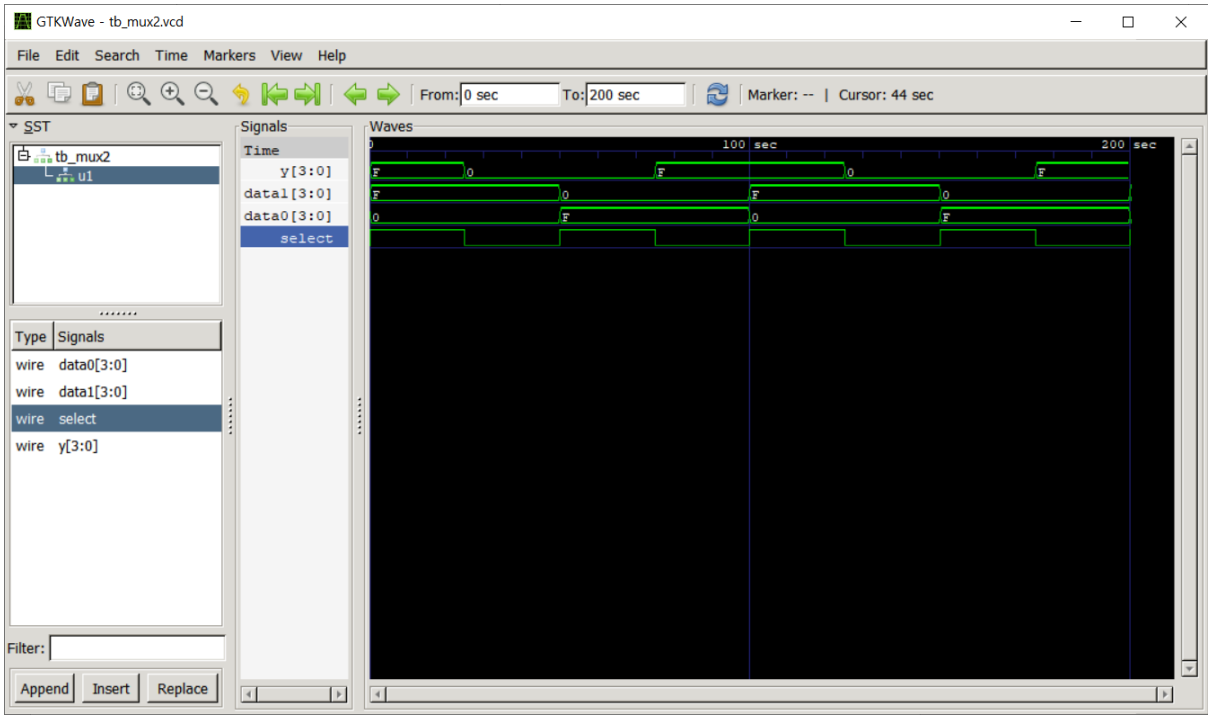

mux2.v - Windows 메모장
파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)
module mux2(y,data1,data0,select);
parameter wsize=8;
output [wsize-1:0] y;
input [wsize-1:0] data1,data0;
input select;
assign y = select ? data1 : data0;
endmodule
Ln 1, Col 1
100%
Windows (CRLF)
UTF-8

tb_mux2.v - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module tb_mux2();
wire [3:0] y;
reg [3:0] data1,data0;
reg select;

mux2 #(4) u1(y,data1,data0,select);

initial begin
data1=4'b1111;data0=4'b0000;select=1'b1;
#200
$finish;
end

initial begin
$dumpfile("tb_mux2.vcd");
$dumpvars(0,u1);
end

initial begin
#25 select=0;
#25 data1=4'b0000;data0=4'b1111;select=1'b1;
#25 select=1'b0;
#25 data1=4'b1111;data0=4'b0000;select=1'b1;
#25 select=1'b0;
#25 data1=4'b0000;data0=4'b1111;select=1'b1;
#25 select=1'b0;
#25 data1=4'b1111;data0=4'b0000;select=1'b1;
end
endmodule
```

Ln 11, Col 100% Windows (CRLF) UTF-8



#2

(1)

comparator1.v - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module comparator1(eq,lt,gt,a,b);
output eq,lt,gt;
input a,b;
assign eq=~a&~b|a&b;
assign lt=~a&b;
assign gt=a&~b;
endmodule
```

Ln 8, Col 1 100% Windows (CRLF) UTF-8

combine.v - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module combine(eq,lt,gt,eq1,lt1,gt1,eq0,lt0,gt0);
output eq,lt,gt;
input eq1,lt1,gt1,eq0,lt0,gt0;
assign eq=eq1&eq0;
assign lt=lt1|eq1&lt0;
assign gt=gt1|eq1&gt0;
endmodule
```

Ln 8, Col 1 100% Windows (CRLF) UTF-8

(2)

comparator2.v - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module comparator2(eq,lt,gt,a,b);
output eq,lt,gt;
input [1:0] a,b;
wire eq1,lt1,gt1,eq0,lt0,gt0;
comparator1 u1(eq1,lt1,gt1,a[1],b[1]);
comparator1 u2(eq0,lt0,gt0,a[0],b[0]);
combine u3(eq,lt,gt,eq1,lt1,gt1,eq0,lt0,gt0);
endmodule

module combine(eq,lt,gt,eq1,lt1,gt1,eq0,lt0,gt0);
output eq,lt,gt;
input eq1,lt1,gt1,eq0,lt0,gt0;
assign eq=eq1&eq0;
assign lt=lt1|eq1&lt0;
assign gt=gt1|eq1&gt0;
endmodule

module comparator1(eq,lt,gt,a,b);
output eq,lt,gt;
input a,b;
assign eq=~a&~b|a&b;
assign lt=~a&b;
assign gt=a&~b;
endmodule
```

Ln 24, Col 100% Windows (CRLF) UTF-8

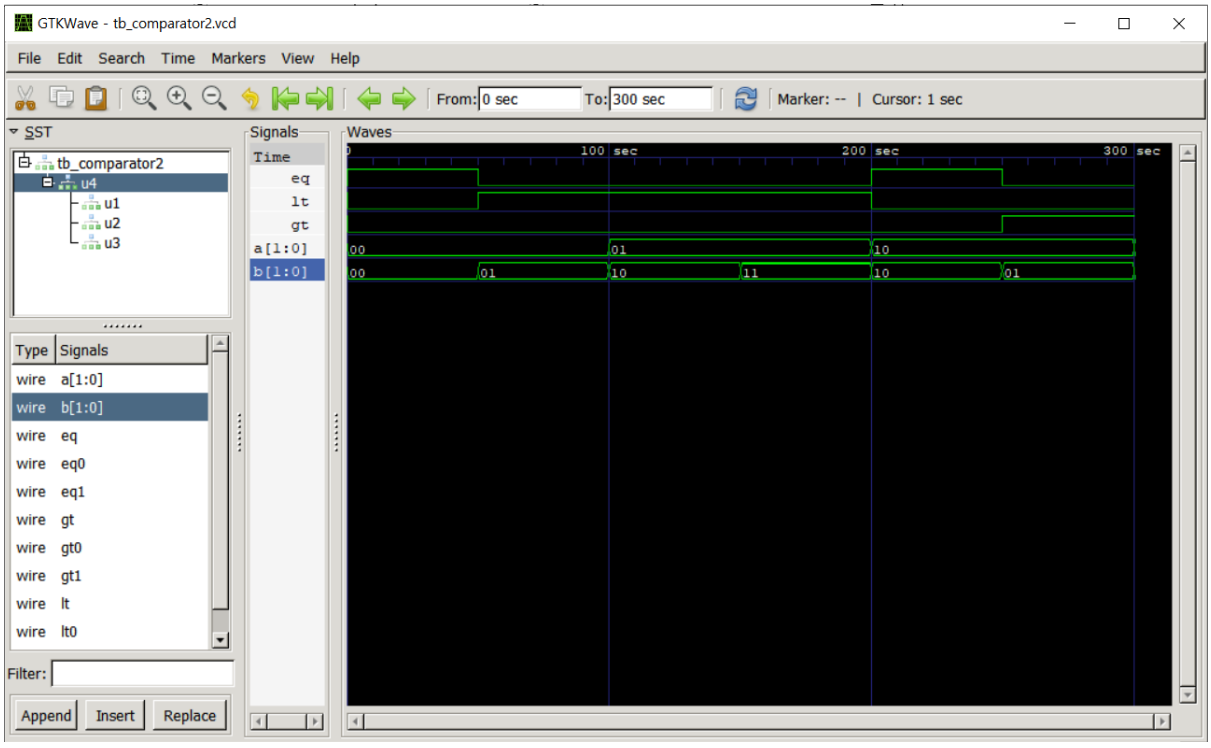
(3)

tb_comparator2.v - Windows 메모...

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module tb_comparator2();
wire eq,lt,gt;
reg [1:0] a,b;

comparator2 u4(eq,lt,gt,a,b);

initial begin
a=2'b00;b=2'b00;
#300
$finish;
end

initial begin
$dumpfile("tb_comparator2.vcd");
$dumpvars(0,u4);
end

initial begin
#50 b=2'b01;
#50 a=2'b01;b=2'b10;
#50 b=2'b11;
#50 a=2'b10;b=2'b10;
#50 b=2'b01;
#50 a=2'b11;b=2'b00;
end
endmodule
```

Ln 3, Col 1 100% Windows (CRLF) UTF-8



#3

(1)

cmp.v - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module cmp(eq,lt,gt,a,b);
output eq,lt,gt;
input [1:0] a,b;
assign eq=a==b;
assign lt=a<b;
assign gt=a>b;
endmodule
```

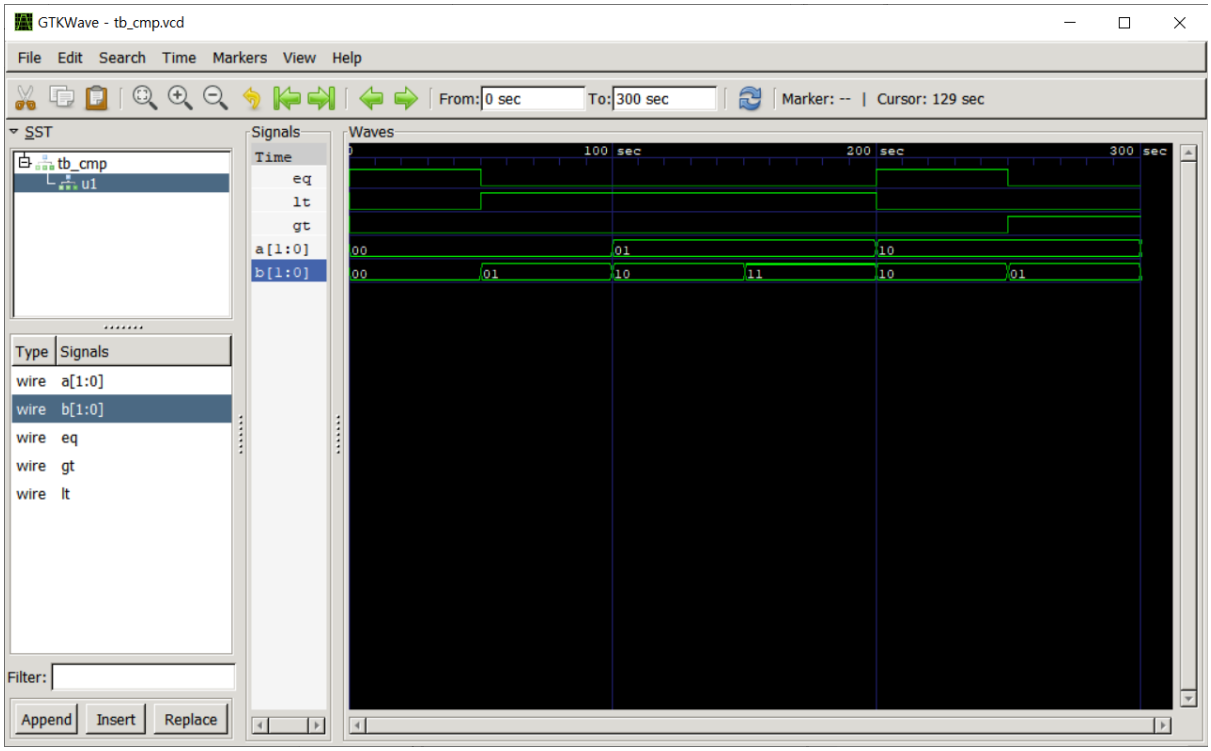
Ln 1, Col 1 100% Windows (CRLF) UTF-8

tb_cmp.v - Windows 메모장

파일(F) 편집(E) 서식(O) 보기(V) 도움말(H)

```
module tb_cmp();
wire eq,lt,gt;
reg [1:0] a,b;

cmp u1(eq,lt,gt,a,b);

initial begin
a=2'b00;b=2'b00;
#300
$finish;
end

initial begin
$dumpfile("tb_cmp.vcd");
$dumpvars(0,u1);
end

initial begin
#50 b=2'b01;
#50 a=2'b01;b=2'b10;
#50 b=2'b11;
#50 a=2'b10;b=2'b10;
#50 b=2'b01;
#50 a=2'b11;b=2'b00;
end
endmodule
```

Ln 17, Col 100% Windows (CRLF) UTF-8



(2)

2번의 비교기 설계와 같은 동작을 한다. 3번의 비교기 설계 방식이 훨씬 간단하고 편리하게 작성할 수 있는 것 같다.