실습과제 5

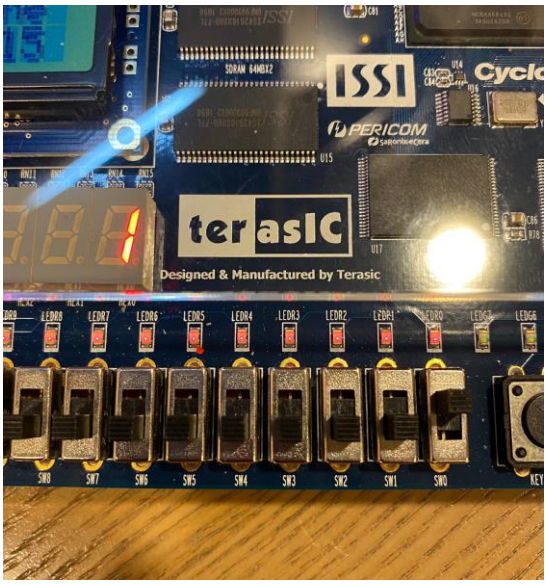
2017253041_홍성우

1.

(1)

decoder.v

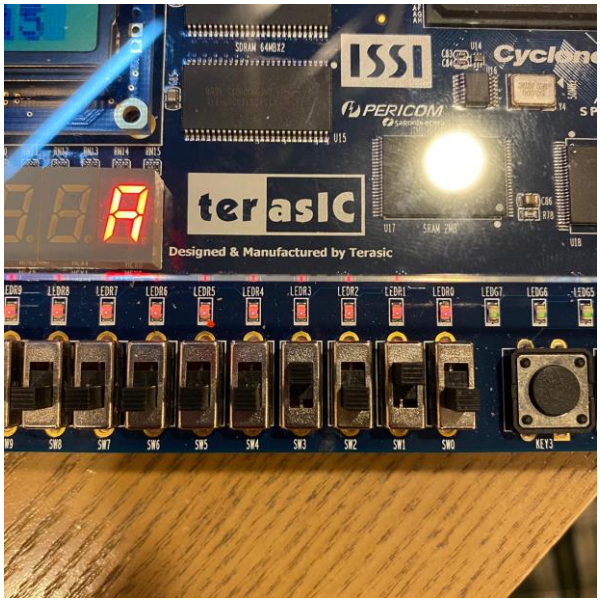
```
1  module decoder(bcd,disp);
2     input [3:0] bcd;
3     output [0:6] disp;
4     reg [0:6] display;
5
6     assign disp = ~display;
7
8     always @(*) begin
9        case (bcd)
10       0: display = 7'b111_1110;
11       1: display = 7'b011_0000;
12       2: display = 7'b110_1101;
13       3: display = 7'b111_1001;
14       4: display = 7'b011_0011;
15       5: display = 7'b101_1011;
16       6: display = 7'b101_1111;
17       7: display = 7'b111_0000;
18       8: display = 7'b111_1111;
19       9: display = 7'b111_1011;
20       default: display = 7'b000_0000;
21       endcase
22    end
23 endmodule
24
25
```

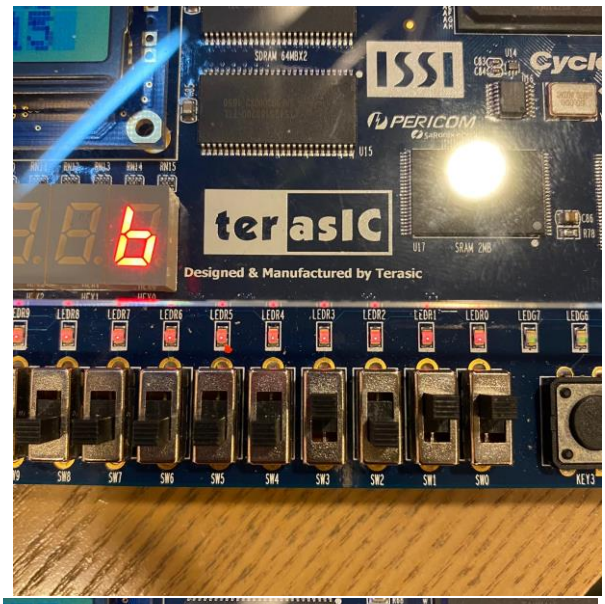


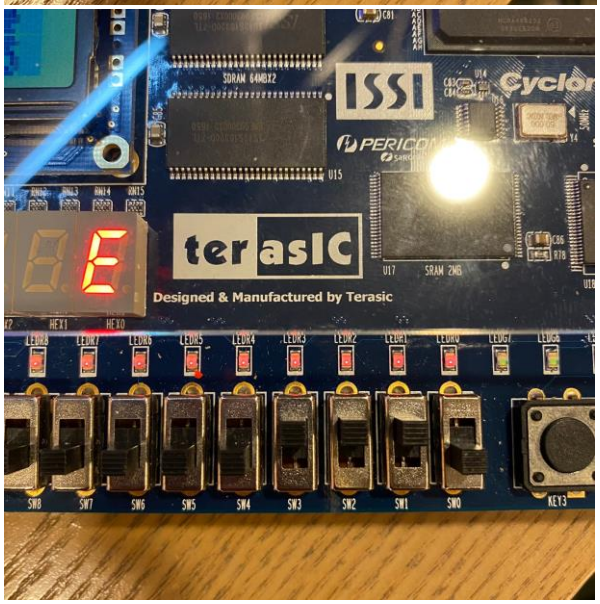
(2)

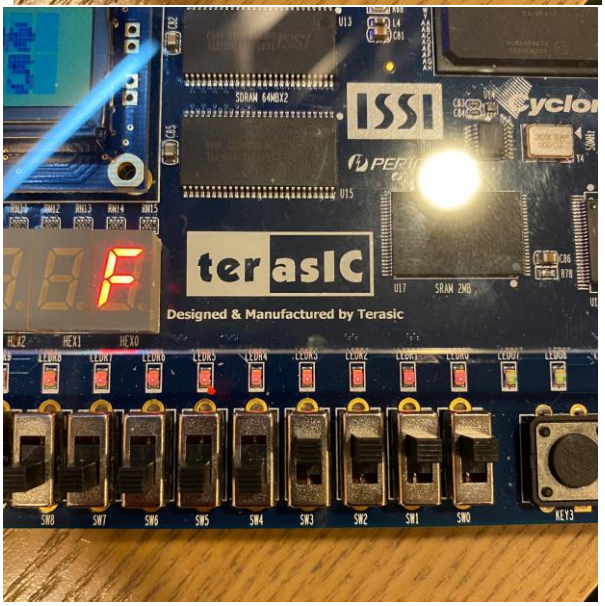
decoder.v | Compilation Report - decoder

```
1  module decoder(bcd,disp);
2     input [3:0] bcd;
3     output [0:6] disp;
4     reg [0:6] display;
5
6     assign disp = ~display;
7
8     always @(*) begin
9        case (bcd)
10       0: display = 7'b111_1110;
11       1: display = 7'b011_0000;
12       2: display = 7'b110_1101;
13       3: display = 7'b111_1001;
14       4: display = 7'b011_0011;
15       5: display = 7'b101_1011;
16       6: display = 7'b101_1111;
17       7: display = 7'b111_0000;
18       8: display = 7'b111_1111;
19       9: display = 7'b111_1011;
20       10: display = 7'b111_0111;
21       11: display = 7'b001_1111;
22       12: display = 7'b100_1110;
23       13: display = 7'b011_1101;
24       14: display = 7'b100_1111;
25       15: display = 7'b100_0111;
26       default: display = 7'b000_0000;
27       endcase
28    end
29 endmodule
```







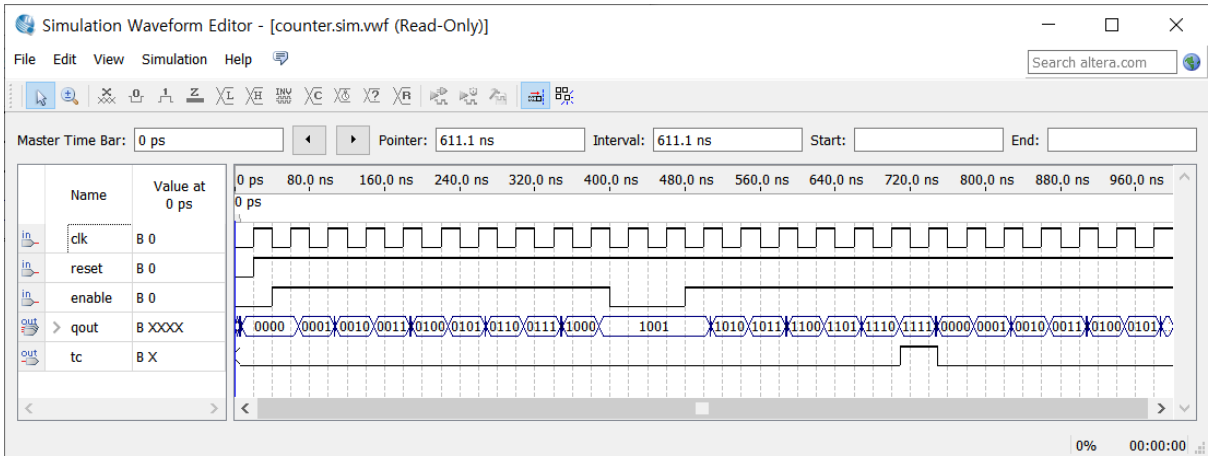


2.

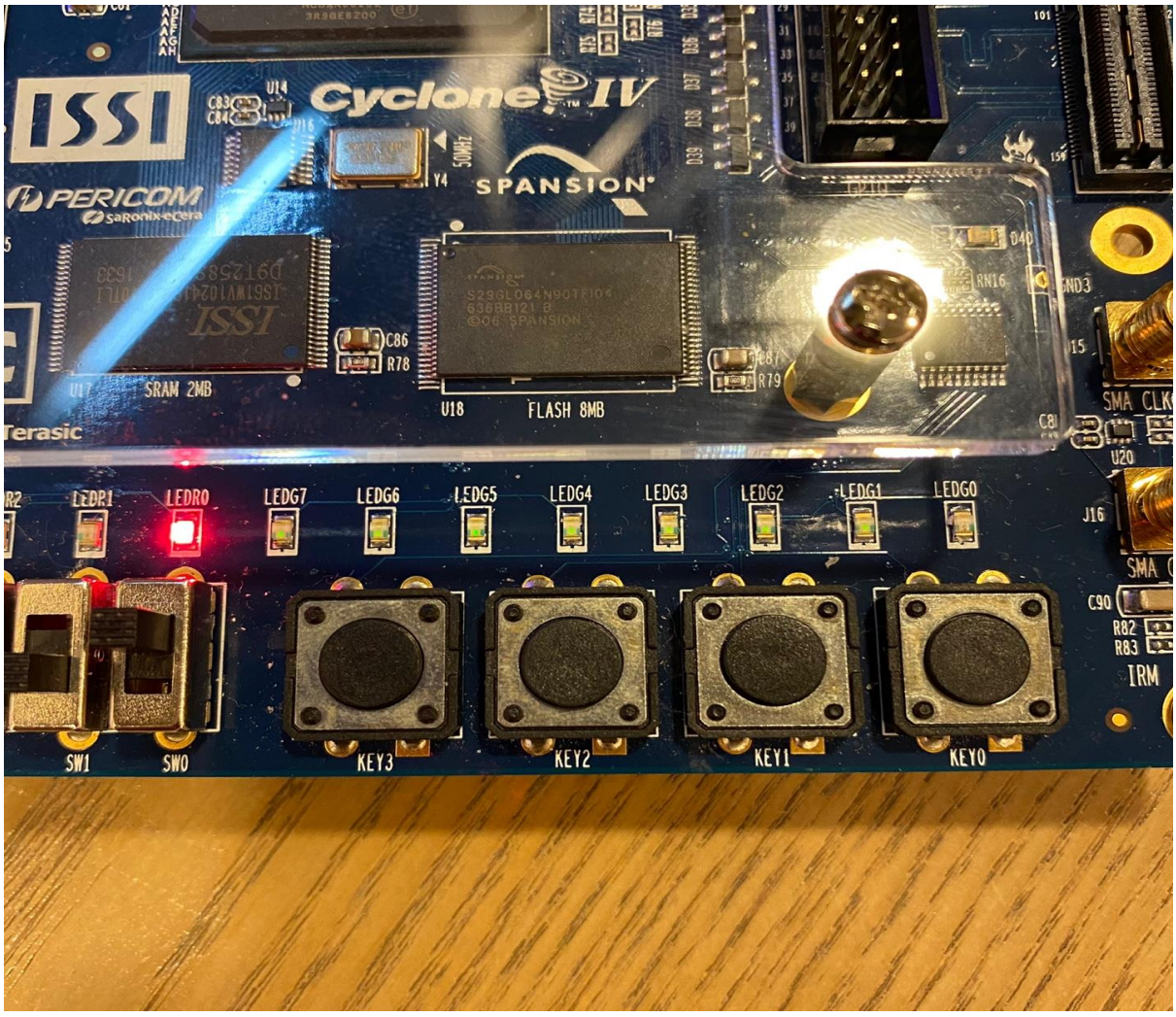
(1)

counter.v | Compilation Report - counter

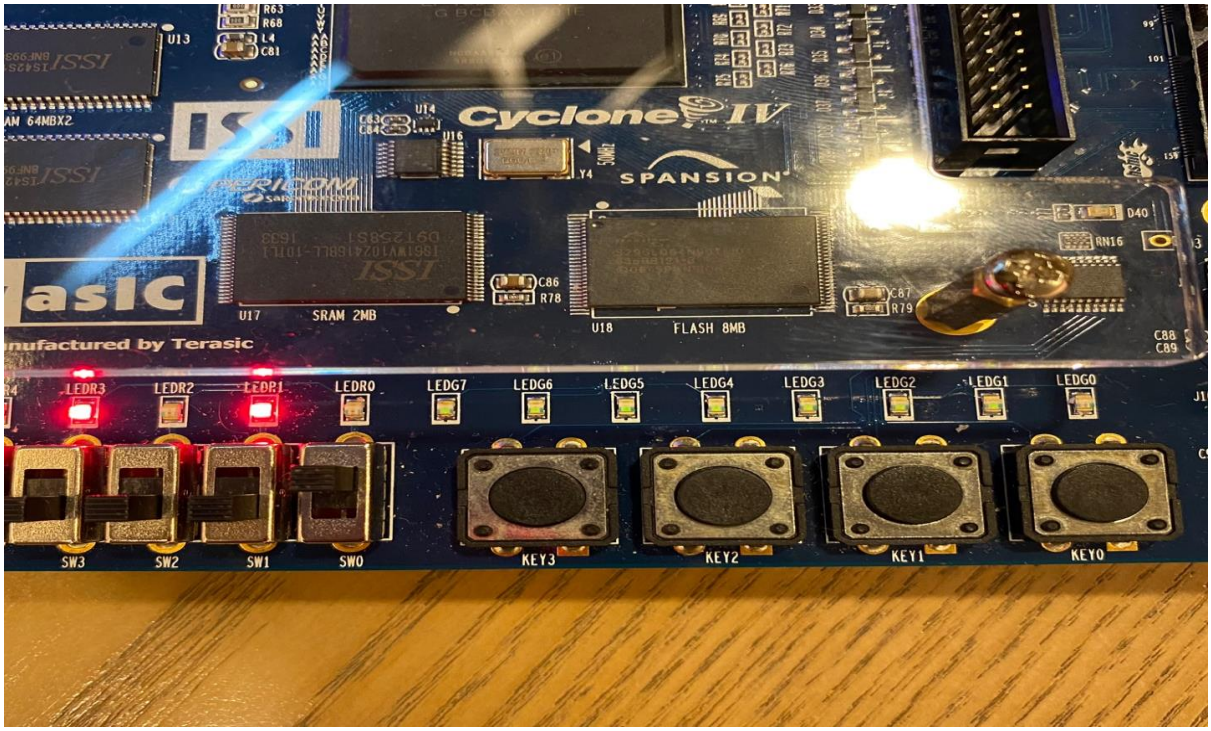
```
1   module counter(clk,reset,enable,qout,tc);
2      input clk,reset,enable;
3      output reg[3:0] qout;
4      output tc;
5
6      always @(posedge clk or negedge reset) begin
7         if(~reset) qout <= 0;
8         else if(enable) qout <= qout + 1;
9      end
10
11     assign tc = enable && (qout == 4'b1111);
12  endmodule
13
```



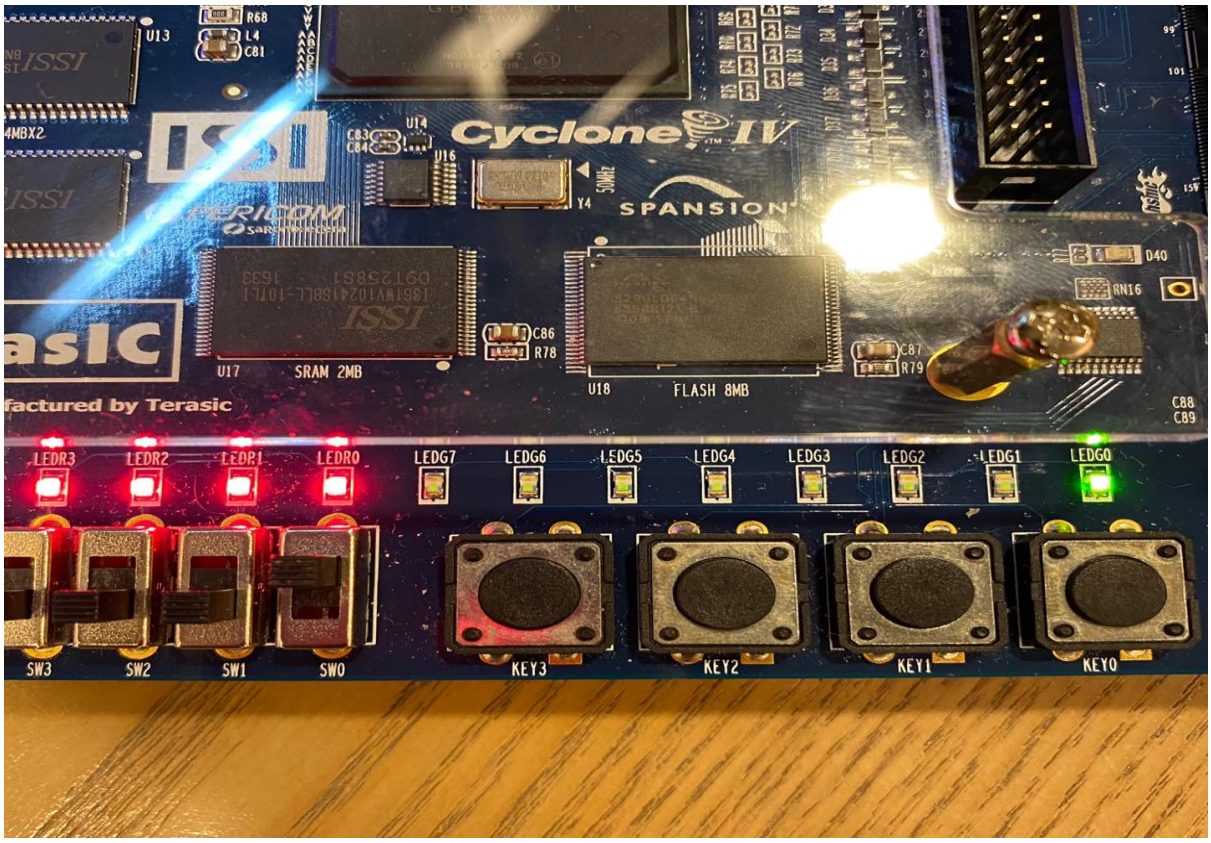
(2)



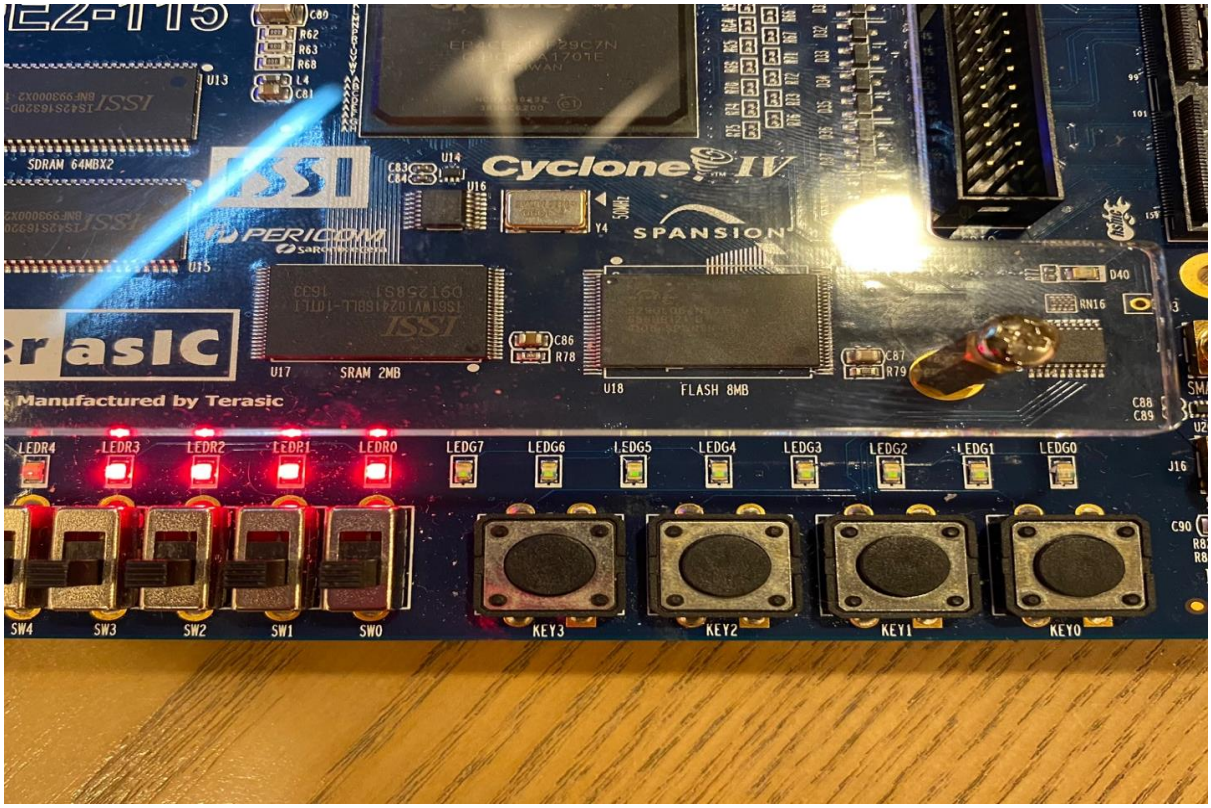
enable, reset 입력이 1일 때 clk 신호를 주니 qout이 1부터 증가하기 시작함



enable, reset 입력이 1일 때 clk 신호를 주니 qout이 1씩 증가함



qout이 4'b1111이고 enable이 1일 때 tc가 1이 됨



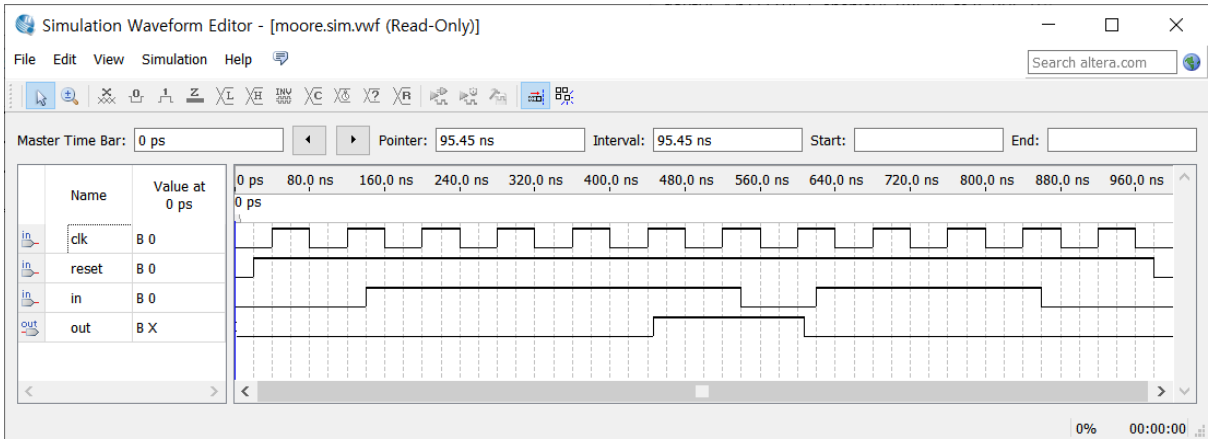
qout이 4'b1111이고 enable이 0일 때 tc가 0이 됨

3.

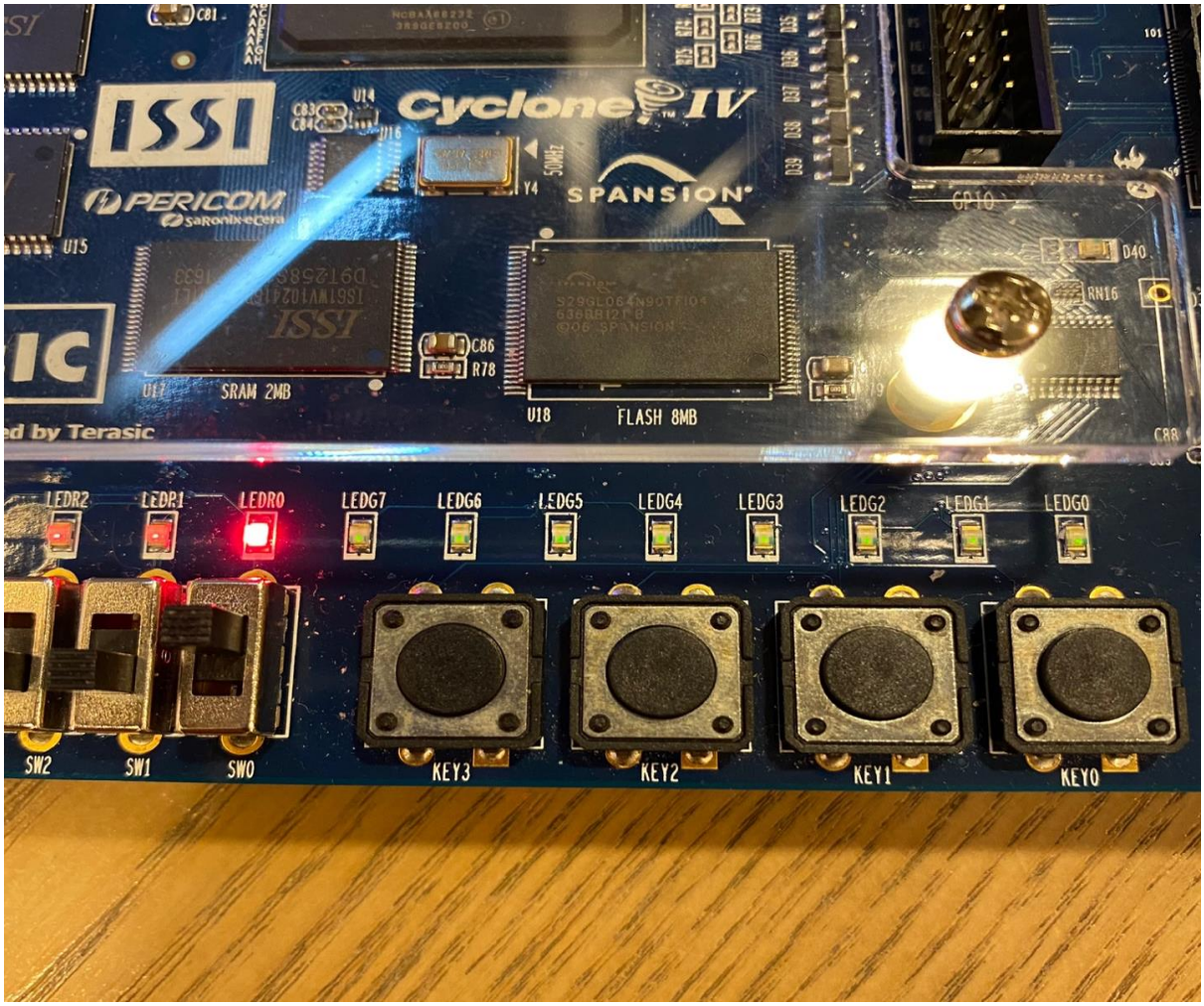
(1)

moore.v | Compilation Report - moore

```
1  module moore(clk,reset,in,out);
2     input clk,reset,in;
3     output out;
4     reg[2:0] state,ns;
5     localparam a=0,b=1,c=2,d=3,e=4;
6
7     always @(posedge clk, negedge reset) begin
8        if(~reset) state <= 0;
9        else state <= ns;
10    end
11
12    always @(*) begin
13       case(state)
14       a: if(in) ns = b; else ns = a;
15       b: if(in) ns = c; else ns = a;
16       c: if(in) ns = d; else ns = a;
17       d: if(in) ns = e; else ns = a;
18       e: if(in) ns = e; else ns = a;
19       default: ns = 3'bx;
20       endcase
21    end
22
23    assign out = (state == e);
24 endmodule
25
```



(2)



연속 4번 1을 입력해야지만 out이 1이 됨

4.

이번 실습과제로 FPGA를 다루기 위한 전반적인 기초학습을 했고 앞으로의 내용이 더욱 어려워질 것 같다.