EE533 - Laboratory Assignment 2
Instructor: Young Cho

NOTE: You must use GitHub to store all source codes and reports associated with the lab assignments. You must commit/push all modifications to the assignments with detailed descriptions at least once daily while working on the lab assignment. Please submit the GitHub link and record of your commits and detailed commit description to Brightspace before the due date.

1. Xilinx ISE 10.1 In-depth Tutorial

You will go through the in-depth Xilinx ISE CAD tool version 10.1 tutorial for this assignment. It is important that you use version 10.1 rather than the latest version. This is because the Xilinx FPGA on the NetFPGA is no longer supported by ISE 11 and later.

This assignment should be done individually. You may ask others for help with the tutorial, but you must complete all tasks, including drawing schematics and behavioral simulations.

Download the exported Virtual Machine (Tutorial.ova) with Windows XP and the ISE package installed. You should be able to use either VirtualBox or VMWare to run the VM.

https://drive.google.com/file/d/1CrlI9OBYNcrOj_LMk7_sy1O1yOTHkv3q/view?usp=sharing

Download the PDF document and the zipped tutorial files to go through the in-depth tutorial tasks.

https://drive.google.com/file/d/1IYssVuhtX8eO9Wucj-Ro61SvYaQaO-fE/view?usp=sharing

https://drive.google.com/file/d/1WeGw-Nghcaf9s-SmwzSFKmKTbkIdaiGx/view?usp=sharing

You are welcome to complete all tasks in the document, but you may skip pages 23-48, 68- 88, and 107-end for this class.

Please use the Forum and/or Piazza with questions and respond if you know the answers.

You must include the following in the report and describe them in the demonstration video:

- Screen capture of your schematics
- Screen capture of the waveforms generated by the tools

2. Designing and Simulating a Synchronous 8-bit Adder

For this part, you must go through the same steps taken in the in-depth tutorial (Part 1) to build and simulate an 8-bit adder using eight 1-bit full adders and D-flip flops available **(DO NOT USE THE IP CORE TO GENERATE ANY OF THE COMPONENTS)**

A synchronous adder has a D-flip flop before the input pins and a D-flip flop after the output pins of the adder circuit.

The following must be turned in:

1. Screen capture of your schematics
2. Screen capture of the waveforms generated by the behavioral simulation tools

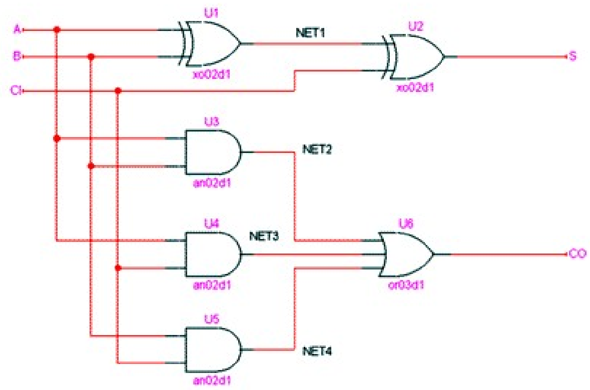

Figure 1: 1-bit Full Adder

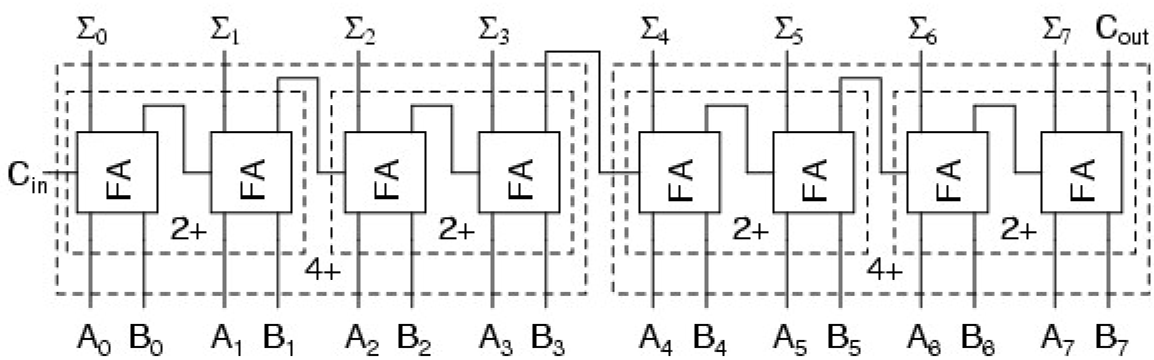

Figure 2: 8-bit Adder

3. Extending Adder into 32-bit ALU

DO NOT USE THE IP CORE

A Extend the 8-bit Adder into a 32-bit Adder by instantiating and connecting 4 adders

Turn in the following:

1. Screen capture of your schematics
2. Screen capture of the waveforms generated by the behavioral simulation tools

B Extend the 32-bit Adder to have other functions, including a subtractor, a shifter, and two other functions of your choice. Go through the mapping process of the tools to get the gate counts, such as the number of D-FF and LUTs.

Turn in the following:

1. Brief description of all of the functions

2. Screen capture of your schematics
3. Screen capture of the waveforms generated by the behavioral simulation tools
4. Log file of the mapper

C Write a Verilog equivalent of a 32-bit ALU

Turn in the following:

1. Screen capture of the waveforms generated by the behavioral simulation tools
2. Log file of the mapper
3. Brief comment on the number of gates as compared to the schematic version

If you are having many problems, here is my tutorial video on designing circuits using the ISE tools.

http://oasysresearch.com/ise_tutorial.mkv