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The AT&T 5ESS hardware design environment: a large system's hardware design process

KENNETH A RADTKE, Nokia Bell Labs, Murray, NJ, United States

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The AT&T 5ESS™ Hardware Design Environment: A Large Systems's Hardware Design Process

Kenneth A. Radtke
AT&T Bell Laboratories
1200 E. Warrenville Road
Naperville, Illinois 60566

Abstract - Large telecommunications switching systems are very complex products consisting of millions of lines of software code running on a system of hundreds of circuit boards. AT&T's 5ESS™ Switch product is globally designed and manufactured at multiple sites working under a common process. Competitive pressure in the communications industry forces the following ongoing *improvement directives* on the design process:

1. **reduce the product's cycle time and time to market**
2. **improve product quality and reliability**
3. **reduce product cost and improve designer productivity**

These directives lead to several major considerations in the hardware design environment, and the importance of those considerations is multiplied in large products. This paper describes at a high level the process and support structures for the ongoing hardware development of AT&T's 5ESS™ Switch, focusing on the following:

1. **A disciplined hardware process, with a well defined process maintenance structure aimed at continual improvement.**
2. **The implementation of new tool technologies in a controlled manner. Our data shows that occasional paradigm shifts lead to very significant improvements.**
3. **A well structured hardware design support environment supporting rapid change in process and to "usher in" new technologies.**
4. ***The use of Concurrent Engineering* is critical in large projects to enable meeting the improvement directives.**

An overview of the electrical hardware design process will be given, describing how design technologies are employed toward achieving these improvements.

1. Introduction

New feature development for the AT&T 5ESS Switch™ is a large ongoing effort, as is the *redesign* of its older packs to best utilize new technology. Many sub-projects exist concurrently in support of the mature but evolving switch product. The 5ESS switch development undergoes more than 100 new designs and more than 200 design changes each year.

A Project Example

An example of a large feature project for 5ESS™ was the recent 5ESS-2000™ development, which redesigned much of the core of the switch and introduced more than 30 new boards (with more than 15 ASICs and numerous off the shelf components). The project had to be developed in a shorter interval than previous projects, hence there was no time to prototype boards and then redesign them. Boards and ASICs essentially had to work the first time. Through the application of system level simulation and other processes described in this paper, the boards and ASICs *did* work the first time, with most boards subsequently getting only minor design changes before final production.

Environment/Process Overview

A brief overview of the environment will set the context. The 5ESS hardware design *environment* consists of a variety of both internally developed and outside vendor tools, running on a distributed network of more than 150 workstations. The design *process* is fully documented on-line, is owned by teams of designers, is ISO certified, and is continually improved. It is applied globally across multiple locations. A hierarchy of support organized at the project, product, and corporate level maintain the environment and usher in new technologies.

Careful management of component selection and lifecycle, and close coupling of the designers to the factories (concurrent processes) help reduce product cost and improve quality to customers.

Technology Use Overview

The early use of newer design technologies (such as ASIC synthesis, system level simulation, and automated test generation schemes) have significantly improved designer productivity and system reliability. Many of these technologies

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were proved in the 5ESS-2000™ project mentioned earlier. Technology payoffs have been tracked and will be presented here.

2. Process Maintenance and Improvement

As stated, competitive pressures in the Telecommunications industry have forced the following continual improvement goals on our processes:

1. Reduction of the design interval
2. Improvement of quality and reliability of the product
3. Cost reduction of our product, and productivity improvement for our designers

The 5ESS™ design process is ISO compliant. It is maintained by a series of *Process Management Teams* (PMTs). Each PMT has a functional scope (e.g. device design PMT, board design PMT, simulation PMT). Each consists of a team of experts who are people that *execute* that process and have formal quality training. The PMT fully owns its process and is empowered to change it. Formal entry of process problems, and suggestions of *Opportunities For Improvement* are available to anyone in the project. The PMT encourages and oversees *trials* of process changes, in which data is carefully gathered to measure the effect of the change, then approved and documented if successful.

As a requirement of distributed global design and manufacture, the 5ESS™ processes are fully documented and maintained on-line. Executers of a given process are expected to follow the on-line documentation, unless trialing a process change, and they are notified of process changes by electronic mail.

To summarize, process adherence is enforced, but there is a well defined process maintenance structure. Continual improvement is encouraged with change being driven by data from trials.

The Role of Technology

Technology advances in fabrication and design tools have enabled significant improvements for 5ESS™ hardware design over 10 years [1]. Figure 1 shows the trend of measured 10 year increase in complexity of typical ASICs (Gate Arrays and Semi-Custom) for 5ESS™ projects. Semiconductor fabrication technologies have made this possible, and design tool technology improvements have been made similarly to enable full use of the "newly available silicon."

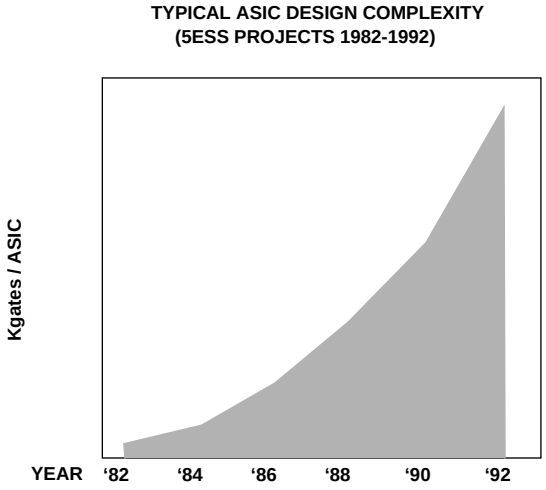

Figure 1

Figure 2 shows the measured 10 year productivity improvement of ASIC designers in those years. Improvements are largely due to tool technology improvements, and will discussed next.

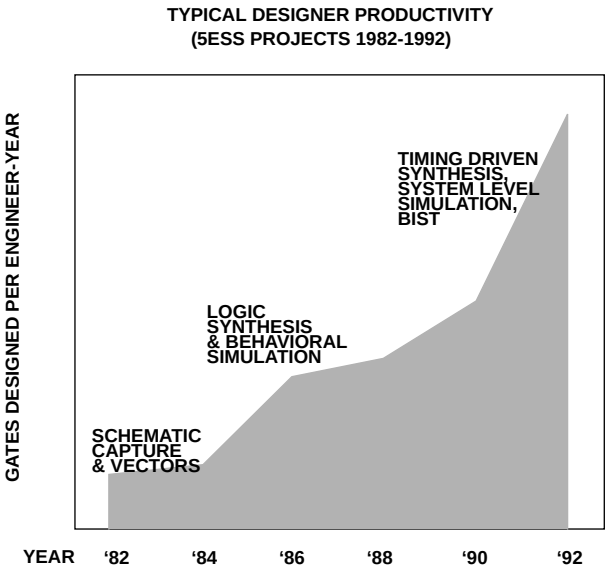

Figure 2

Key Technology Shifts

Process improvements are the result of:

1. *gradual improvement*, such as improved designer experience, continual process changes, incremental tool improvements, and so on.
2. *key technology shifts* in the tools, sometimes called *paradigm shifts*, which occur from time to time and dramatically improve designer productivity and reduce design

intervals.

The latter are infrequent and their effects are harder to predict. But they can have big payoffs. Some key technology shifts in the timeframe of Figure 1 and 2 have been:

1. The shift away from schematic capture and into basic high-level logic synthesis. Another shift occurred in the move to timing-driven synthesis (now used for all our ASICs).
2. The shift away from prototyping boards in a lab, and into system level simulation without the need for prototypes.
3. The shift away from hand writing test vectors, into automatic test generation via BIST and Boundary Scan tools.
4. The shift away from hand writing functional simulation vectors, to the use of high level 'C' and 'C++' software drivers and automatic verifiers.

We've observed that key technology shifts in a given functional tool area have occurred 4 or 5 years apart.The improvement effects of *technology shifts* are so significant compared to the *gradual improvements*, that we now seed and actively search for "the next paradigm". For example, we are tracking AT&T Bell Laboratories work in Formal Design Verification(COSPAN [2]) with the hope that it may payoff as *the* next verification methodology.

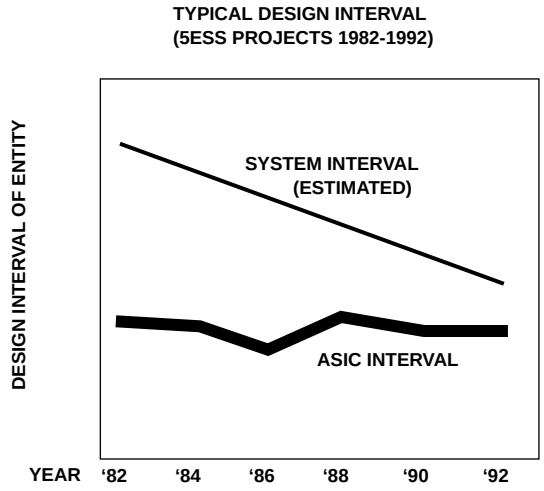

Figure 3

Figure 3 shows the overall project intervals. Despite increasing ASIC and system complexity, the productivity gains have enabled designers to design ASICs in roughly the same interval. But note, that means that during a similar interval in 1992 they can design about 8 times more circuitry than in 1982, and it fits on a smaller percentage of available wafer. Tool technology improvements have enabled full use of fabrication and interconnection technology gains.

Meanwhile, system design intervals have been cut in half, largely due to tool technologies (e.g. system-level simulation). While this is good, it is evident that key technology shifts have had less impact in system and board design productivity than in ASICs.

3. Ushering in Technologies: The Tool Support Structure

The support structure for hardware design is very important to new technology introduction, therefore important to the ongoing success of very large products. 5ESS™ designer and tool support has evolved to a layered structure which will be briefly described.

Corporate/Vendor Tool Support

At the highest level we rely on an internal corporate organization, AT&T Design Automation™, for the integration of tools and for ownership of the end to end design through manufacturing capability. An "open system" is maintained so that outside vendor tools can be plugged in wherever it's to our advantage. Some key reasons for having *integration* as an internal corporate function are:

1. our design and manufacturing capability is a strategic competency,
2. internal groups might have more motivation for rapid tool customizations than an outside vendor,
3. they can handle internal proprietary technologies as they arise, and keep them proprietary.

Local Centers of Expertise

The 5ESS™ product maintains a small localized "Advanced Design Process" group to support the circuit designers with new technologies. The primary role of the group has been in providing simulation and synthesis consulting, modeling, and direction to circuit engineers. Having such a center of simulation and synthesis expertise was a key to the successful standardization of those technologies into our process, as in the 5ESS-2000™ project example mentioned earlier. Reasons for the need for a centralized technology support group are:

1. Track design metrics, trends, and problems, as well as new technologies. Identify and even seed or sponsor new technologies.
2. Ushering in new technologies requires expertise and application engineering at staffing levels beyond what individual projects can usually afford.

Once a new technology is proved in on a project, it becomes the “standard process”, and expertise within the design community grows to become self supporting on that technology.

There are other local centralized *centers of expertise*. Some examples are the component library administration team; the component information management team; the electromagnetic compatibility (EMC) team.

4. A Process Overview

Key points of this section are:

1. An overview of the 5ESS^{TM} electrical hardware design process is presented.
2. The process is well integrated from design through manufacture.
3. The process is both serial and concurrent. Being a large organization, more concurrency is required to meet our improvement directives.

The electrical hardware design process is both serial and concurrent. Figure 4 indicates the conceptual application/ data model enabled by our tools and distributed environment.

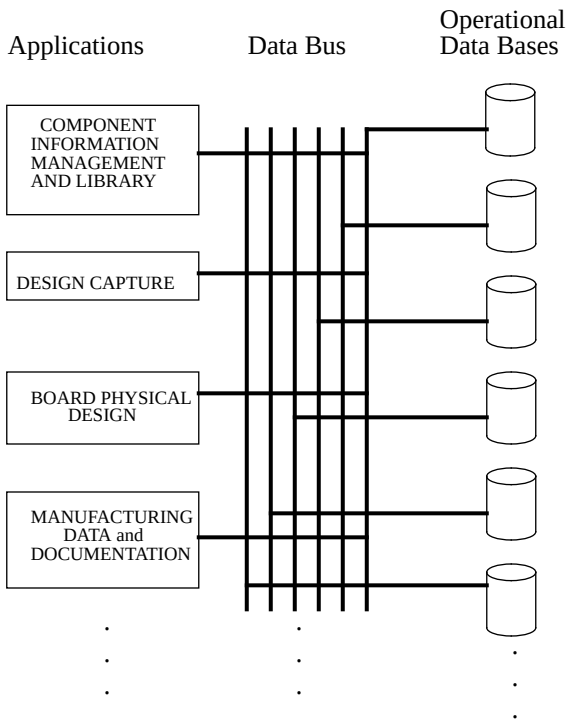

Figure 4

For illustration, only four major value adding “applications” are drawn here. Within each are many tools accessing data. Each application tends to correspond to an organization. Three tend to be more sequential: 1) electrical design; 2) board layout and physical design; and 3) manufacturing and product documentation. Component Information Management has highly concurrent roles throughout the design process.

Concurrent Engineering

Concurrent Engineering has become important to large projects [3]. Our process is *driven* by the product’s data, but is based on well documented process and product requirements coming from the manufacturer. The *primary data flow*, or value adding to the product design over time, is generally top to bottom in Figure 4. The *flow of requirements* from manufacturing is generally from bottom to top. Yet each application is completely coupled to each of the others in a bidirectional manner. Thus there are numerous points of concurrency and data cross-transfer. Some typical uses of process concurrency include:

1. allowing “downstream” steps to influence “upstream” steps early. Changes can become an order of magnitude more expensive with each step, so the earlier the faults are eliminated, the better. Example: The factory is involved in early design reviews, involving tool-assisted conferencing of schematics or layouts, in order to recommend design changes for improved manufacturability and testability before the design is committed. Requirements flow to the design early.
2. making “upstream” component choices immediately available downstream (well ahead of the design). For example: early component stocklists from the design are forwarded and can prime the component vendor selection and purchasing operations from the manufacturing data system.

The term *DFX* pertains to areas where the process steps are usually concurrent, where X = testability, manufacturability, etc. DFX data, rules and considerations concurrently bridge the major applications with data and requirements flowing each direction throughout the design duration.

Electrical Design and Intent Capture

We now look into process activities, which are supported by tool applications and data in Figure 4, starting with design capture. Board designs are captured schematically. ASICs are entirely designed in a ‘C’ based HDL [4] and then simulated. Designers are knowledgeable in writing in ‘C’ language and frequently automate the design process with custom software scripts to control tools, automate procedures, etc.

Multiple boards and their ASICs are always simulated together as a system. Regression simulation scripts are built and maintained for use as design changes occur. Portions of

the product's software are simulated with the hardware as both are being developed concurrently. AT&T Design Automation's ATT-SIM™ simulation/verification toolset is used across all levels of design simulation, because it has advanced mixed-signal simulation capabilities and the ability to do min/max timing simulation at the system level. Test generation is accomplished via Built In Self Test (BIST) at the device level, and often at the board level. Boundary Scan is sometimes used.

Component Information Management

The component selection and management process is highly concurrent with the other design steps. Advice and data from the Component Management team aids designers in component selection based on criteria such as cost, availability, reliability of the vendor, lifecycle phase of the part, and others. New components added to the stocklist initiate a process of preparing downstream organizations, from purchasing through manufacturing, to assist the product realization.
Data pertaining to substitutions is maintained, and is in fact used for system simulation to assure robust design and manufacture tolerance.

Board Layout

The board layout and physical design process is generally accomplished by skilled technicians who are familiar with layout tools and the many considerations involved in physical design (thermal, high frequency layout, manufacturability, etc.). The layout technician works with the electrical designer early in the project, and there are a series of formal data transfers. Rule-driven design and extensive DFX audit tools are of prime importance in assuring manufacturability in the first design pass. The design rules and audits are data [requirements] pulled back from the manufacturing system.

Manufacturing Data and Documentation

The data interface to manufacturing is an internally supported system named FOCUS. It provides a tight coupling of *product data management* with *assembly process management* (e.g. machine insertion). It stores design and change information for the factory, maintains final stocklists and coordinates ordering information, product documentation, and so on. The tools provide factory representatives with access to schematic, layout, bill of materials, firmware, assembly, and testability information early in the process to affect the product's design before changes would become costly.

Many other aspects of hardware design occur which are not described herein, such as equipment and cabinet design for example. Data from these manufacturable entities are similarly integrated in the FOCUS system.

5. Future

For a project as large as 5ESS™ there is on
ongoing list of opportunities for improvement to the hardware design environment. The need for additional simulation power for faster system level simulations is high on the list. Improved ability to simulate the product's software with the hardware would be desirable. Additional concurrency is being built in an effort to further reduce product realization interval. And, as mentioned earlier, the quest for the next *design paradigm shift* is ongoing.

Other extensions include: Expansion of DFX to installation and field engineering; Workflow management; data warehousing as an extension to the "databus" for additional concurrency.

6. Conclusion

The design environment and process overview of a large hardware product was presented. Designers and process experts on more than 150 networked workstations are involved in the electrical design of the 5ESS™ switch. Much attention is put into continual and controlled process improvement. New technology also plays a critical role in meeting goals of improving quality, reducing interval, and reducing costs. The structure of the support organization is important in implementing new technologies.

7. Acknowledgments

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