TDK SEMICONDUCTOR CORP.

78Q8411
10/100 PCI/CardBus Fast Ethernet Controller

Target Datasheet

November 2001

DESCRIPTION

The 78Q8411 is a high performance Mini PCI/PCI/CardBus Fast Ethernet controller which supports 10BASE-T and 100BASE-TX applications, as well as HPNA 1.X

The 78Q8411 was designed in an advanced CMOS technology to provide a glueless 32-bit bus master interface for CardBus, a boot ROM interface, CSMA/CD protocol for Fast Ethernet, as well as the Media Independent Interface (MII) compliant with IEEE802.3u specification.

The 78Q8411 provides both half-duplex and full-duplex operation, as well as support for full-duplex flow control.

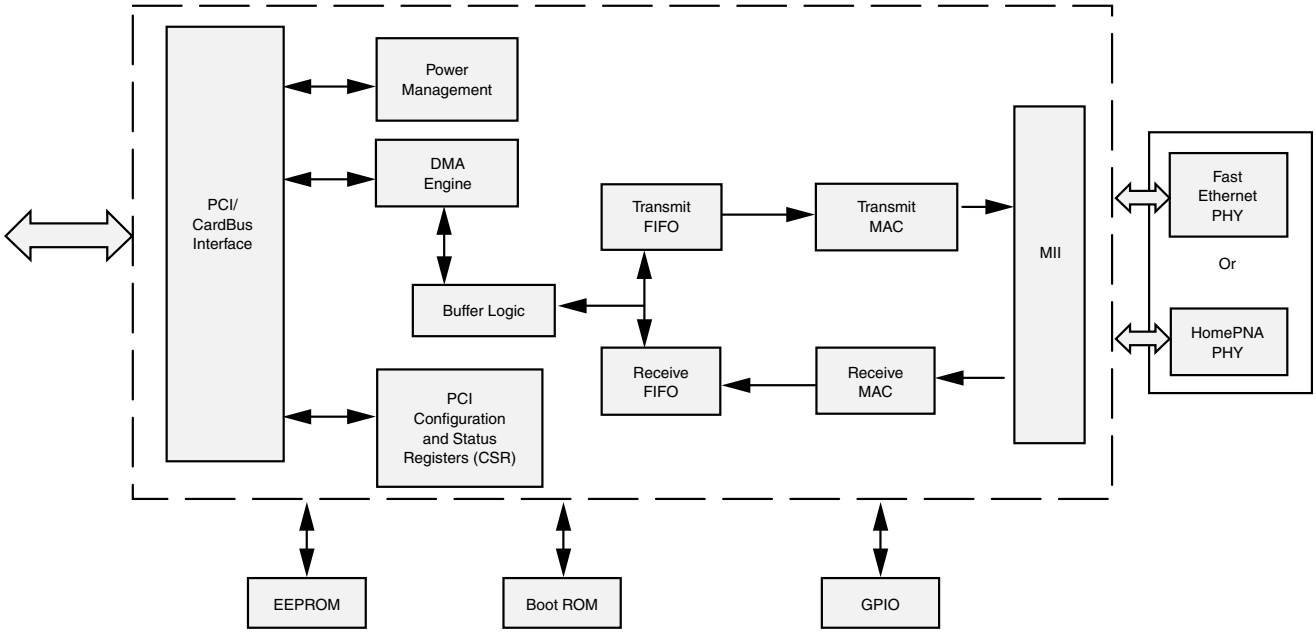
It provides long FIFO buffers for transmission and reception, and an early interrupt mechanism to enhance performance.

The 78Q8411 also supports ACPI 1.0 and PCI 2.2 compliant power management interface specification (PM 1.1) and Magic Packet™ wake-up event.

FEATURES

- **IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant**
- **Support for IEEE802.3x flow control**
- **IEEE802.3u MII compliant**
- **HPNA 1.X Support**
- **ACPI, PCI (PM) power management, and Microsoft's OnNow compliant**
- **Supports PC98/99/2001 wake on LAN**
- **Provides 32-bit PCI & CardBus bus master data transfer**
- **Supports PCI and CardBus clock with frequency from 0Hz to 33MHz**
- **Supports network operation with PCI and CardBus system clock from 20MHz to 33MHz**
- **Provides burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization**
- **Operates at 3.3V core with 5V tolerant I/O**
- **144 Lead TQFP (JEDEC LQFP) package**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The 78Q8411 is a 10/100 Fast Ethernet Controller that provides a direct interface to a Mini PCI, PCI or CardBus and a Media Independent Interface (MII) to an external 10/100 Physical Layer device (PHY) or HomePNA Physical Layer device.

The 78Q8411 is optimized for low power PCI or CardBus based systems and supports ACPI 1.0, PCI 2.2 PM 1.0 and Magic Packet™ Wake on LAN. The device is PC98/99/2001 compliant.

The 78Q8411 complies with the IEEE 802.3x flow control. Integrated transmit and receive FIFOs allow efficient operation with long latency systems. The 78Q8411 also has an interface for an up-gradable Boot ROM.

Media Access Controller (MAC)

The 78Q8411 supports the IEEE 802.3 MAC sublayer. It can operate in half-duplex, full duplex, and loopback modes.

In half-duplex mode, the 78Q8411 checks the line condition before starting to transmit. If the condition is clear, the 78Q8411 starts transmitting. Full duplex operation allows simultaneous transmissions and reception of data that can effectively double data throughput to 20 or 200 Mbps for 10 or 100 Ethernet systems respectively.

Buffer Management

The 78Q8411 provides a buffer management scheme supporting either chain or ring buffer structure, for flexible buffer management. Two Direct Memory Access (DMA) engines shuttle the receive and transmit data between the host and the 78Q8411 automatically.

The buffer management architecture minimizes data handling of the information, thereby reducing CPU overhead. The packet can be in a single fragment or broken into multiple fragments, and is referenced by either single or multiple descriptors respectively. This allows quick access and minimal handling of the data. Data is transferred in the most efficient manner using PCI burst transfers and direct memory access.

Two large independent internal FIFOs, each 32-bit wide, provide multiple data packet transmit and receive buffering with programmable thresholds and store-and-forward modes. Both receive and transmit FIFO are 2K bytes.

ADDRESS FILTERING

The 78Q8411 supports five types of address filtering. Each is described in more detail in the following sections. The filtering is configured through setup frames sent to the 78Q8411.

16-bit perfect filtering: The 78Q8411 provides support for the perfect filtering of up to 16 Ethernet unicast or multicast addresses. Any mix of addresses can be used.

One unicast address perfect filtering: The 78Q8411 supports one, single unicast address to be perfectly filtered. Frames with this physical destination address are checked against the single physical address.

Unlimited multicast address imperfect filtering: An unlimited number of multicast addresses can be imperfectly filtered. Imperfect filtering is when multicast frames not addressed to this station may pass through, but it still decreases the number of frames that can be received.

Promiscuous mode: Supports reception of all good frames.

Pass all multicast: Supports the reception of all multicast frames.

LOOP BACK OPERATIONS

The 78Q8411 supports internal and external loopback modes. Internal loopback mode can be used to verify correct operation of internal logic. External loopback mode can be used to verify that the logic operations up to the Ethernet PHY and wire interface function correctly.

POWER MANAGEMENT FEATURES

PC/98/99/2001 Compliance: The 78Q8411 implements power management features to minimize system power consumption. The device complies with PCI 2.2 and Power Management (PM v1.1) specification and the ACPI Communications and Network Class Power Management Specification v1.1. This assures that the device will comply with Microsoft's OnNow and PC98/99/2001 specifications.

POWER STATES

DO (Fully On)

In this state the 78Q8411 operates as full functionality and consumes its normal power. While in the D0 state, if the CardBus clock is lower than 16MHz, the 78Q8411 may not receive or transmit frames properly.

D1 & D2

These low power states are not supported at this time.

$D3_{cold}$ (Power Removed)

In this state all function context is lost. When power is restored, the function will return to D0.

$D3_{cold}$ (Auxiliary Power)

If an auxiliary power source is supplied, when the 78Q8411 is brought back to D0 from $D3_{cold}$ the software must perform a full initialization.

$D3_{hot}$ (Software Visible D3)

When the 78Q8411 is brought back to D0 from $D3_{hot}$ the software must perform a full initialization.

The 78Q8411 in the $D3_{hot}$ state respond to configurations cycles as long as power and clock are supplied. This requires the device to perform an internal reset and return to a power-up reset condition without the RST# pin asserted.

The device is able to initiate a wake-up event in $D3_{hot.}$

WAKE-UP TECHNOLOGIES

The 78Q8411 can assert a signal to wake up the system when it received a Magic Packet™ from the network.

The Magic Packet ™ format:

A valid destination address must be received, which passes the address filter of the 78Q8411.

The payload of frame must include at least six contiguous 'FF' followed immediately by 16 repetitions of IEEE address.

The frame can contain multiple 'six FF + sixteen IEEE address' pattern.

Once the LAN controller has been put into the Magic Packet™ mode, it scans all incoming frames addressed for a specific data sequence, which indicates to the controller that this is a Magic Packet™ frame. A Magic Packet™ frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a MULTICAST address which includes the BROADCAST address), and CRC. The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of FFh. The device will also accept a BROADCAST frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened. If the IEEE address for a particular node on the network was 11h 22h 33h 44h 55h 66h, then (assuming an Ethernet Frame) the LAN controller would be scanning for the data sequence:

DESTINATION SOURCE MISC.

FF FF FF FF FF FF 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 MISC. CRC.

There are no other restrictions on a Magic Packet™ frame. For instance, the sequence could be in a TCP/IP packet, an IPX packet, etc. The frame may be bridged or routed across the network, without affecting its ability to wake up a node at the destination of the frame.

If the LAN controller scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the controller detects the data sequence, however, then it alerts the PC's power management circuitry to wake up the system.

The Wake on LAN operation

The Wake on LAN enable function is controlled by bit 18 of CSR18, and it is loaded from EEPROM after reset or programmed by driver to enable Wake on LAN function. If the bit 18 of CSR18 is set and the 78Q8411 receives a Magic Packet™, it will assert the PME# /CSTSCHG signal (drive to low) to indicate receiving a wake up frame as well as to set the PME status bit (bit 15 of CSR20).

PCI / CardBus Mode Selection

The PCI_cardz pin determines which mode the 78Q8411 operates. Connect to a "high" for PCI bus, and to a "low" for CardBus operation.

PIN DESCRIPTION

LEGEND

TYPE	DESCRIPTION
A	Analog Pin
I	Digital Input
O	Digital Output
T	Test Pin
I/O	Digital Bi-directional Pin
O/D	Open Drain Output Pin
S	Supply Pin

MII INTERFACE

NAME	PIN	TYPE	DESCRIPTION
CRS	1	I	CARRIER SENSE: Provided by the PHY to indicate that Carrier is currently present on the physical media.
COL	2	I	COLLISION INDICATION: Provided by the PHY to indicate that a collision has been detected on the physical media.
TXD[3]	3	O	TRANSMIT DATA[3]: Transmit data bus from the MAC to the PHY.
TXD[2]	4	O	TRANSMIT DATA[2]: Transmit data bus from the MAC to the PHY.
TXD[1]	5	O	TRANSMIT DATA[1]: Transmit data bus from the MAC to the PHY.
TXD[0]	6	O	TRANSMIT DATA[0]: Transmit data bus from the MAC to the PHY.
TXEN	9	O	TRANSMIT ENABLE: Transmit enable indicator from MAC to PHY indicates that valid data is being presented to the PHY.
TXCLK	10	I	TRANSMIT CLOCK: Transmit clock from the PHY to the MAC.
TXER	11	O	TRANSMIT ERROR: Used by the MAC to indicate to the PHY that a coding or transmit under run error has occurred.
RXER	12	I	RECEIVE ERROR: Produced by the PHY to indicate that it has detected as error in the current packet.
RXCLK	13	I	RECEIVE CLOCK: Produced by the PHY as a timing reference for the MAC.
RXDV	14	I	RECEIVE DATA VALID: Provided by the PHY to indicate to the MAC that valid data is available.
RXD[0]	15	I	RECEIVE DATA[0]: Receive data bus from the PHY to the MAC.
RXD[1]	16	I	RECEIVE DATA[1]: Receive data bus from the PHY to the MAC.
RXD[2]	17	I	RECEIVE DATA[2]: Receive data bus from the PHY to the MAC.
RXD[3]	18	I	RECEIVE DATA[3]: Receive data bus from the PHY to the MAC.
MDC	19	O	MANAGEMENT DATA CLOCK: Clock for Serial Management Interface (SMI)
MDIO	20	I/O	SERIAL MANAGEMENT DATA INPUT/OUPUT: I/O signal for SMI

PCI / CardBus INTERFACE

INTA# / CINTA#	22	O/D	PCI/CardBus INTERRUPT ACKNOWLEDGE: The 78Q8411 asserts this signal when one of the interrupt events occur.
RST# / CRST#	23	I	RESET: PCI/CardBus signal to initialize the 78Q8411: The active reset signal should be sustained at least 100µs to guarantee that the 78Q8411 has completed initializing activity. During the reset period, all the output pins of the 78Q8411 will be tri-stated, and all the open drain (O/D) pins are floated.
PCI-CLK / CCLK	25	I	PCI/CardBus CLOCK INPUT: This clock input to the 78Q8411 for CardBus relative circuits synchronizes the timing base with CardBus. The Bus signals are recognized on rising edge of PCI-CLK. For proper operation, the frequency of PCI-CLK should be between 20MHz and 33MHz when the network functions are operating.
GNT# / CGNT#	27	I	PCI/CardBus GRANTED: This signal indicates that the 78Q8411's bus request has been accepted.
REQ# / CREQ#	28	O	PCI/CardBus REQUEST: Bus request is asserted by the 78Q8411 to indicate to the bus arbiter that it wants to use the bus.
PME# / CSTSCHG	29	I/O O/D	PCI POWER MANAGEMENT EVENT/CardBus STAUS CHANGE: This signal is an open drain, active low signal for PCI (PME#) and active high signal for CardBus (CSTSCHG). When WOL bit (bit 18) of CSR18 is set to "1", the 78Q8411 is set into Wake On LAN mode. In this mode, when the 78Q8411 receives a Magic Packet™ frame from the network, the 78Q8411 will activate this signal by pulling it high. In the Wake On LAN mode, with LWS-bit (bit 17) of CSR18 set into "1", it indicates that the PME#/CSTSCHG signal is CardBus signal, or active high.

PCI / CardBus Interface (continued)

NAME	PIN	TYPE	DESCRIPTION
AD-31/ CAD-31	31	I/O	PCI/CardBus ADDRESS AND DATA: These are multiplexed address and data pins. AD-# refers to PCI, and CAD-# to CardBus signal naming convention.
AD-30	32		
AD-29	34		
AD-28	35		
AD-27	36		
AD-26	37		
AD-25	40		
AD-24	41		
AD-23	45		
AD-22	46		
AD-21	49		
AD-20	50		
AD-19	51		
AD-18	52		
AD-17	55		
AD-16	57		
AD-15	72		
AD-14	73		
AD-13	74		
AD-12	76		
AD-11	79		
AD-10	80		
AD-9	81		
AD-8	83		
AD-7	87		
AD-6	88		
AD-5	89		
AD-4	90		
AD-3	93		
AD-2	94		
AD-1	96		
AD-0 / CAD-0	97		

PCI / CardBus Interface (continued)

NAME	PIN	TYPE	DESCRIPTION
C/BE3# / CBE3# C/BE2# / CBE2# C/BE1# / CBE1# C/BE0# / CBE0#	42 58 71 86	I/O	BUS COMMAND AND BYTE ENABLE: Multiplexed signals, that during the address phase define the type of bus operation. During the data phase, they are byte enable signals. C/BE3# follows the PCI signal naming convention and CBE3# follows CardBus convention.
IDSEL	43	I	INITIALIZATION DEVICE SELECT: This signal is asserted when host issues the configuration cycles to the 78Q8411.
FRAME# CFRAME#	59	I/O	FRAME: The FRAME# pin is asserted by master device at the beginning of the bus access, and released for the last data transfer.
IRDY# / CIRDY#	60	I/O	INITIATOR READY: Master device is ready for data transaction.
TRDY# / CTRDY#	63	I/O	TARGET READY: Slave device is ready for data transaction.
DEVSEL# / CDEVSEL#	64	I/O	DEVICE SELECT: Target is driving to indicate a valid address is decoded.
STOP# / CSTOP#	65	I/O	STOP: Target device requests the master device to stop the current transaction.
PERR# / CPERR#	66	I/O	PARITY ERROR: When a parity error is detected by the target, it drives the PERR# pin low.
SERR# / CSERR#	67	O/D	SYSTEM PARITY ERROR: When an address parity error is detected, the target drives the SERR# pin low.
PAR / CPAR	70	I/O	PARITY: Even parity (AD[31:0] + C/BE[3:0]) is employed. The master drives the PAR pin for address and write data phases; the target drives PAR for read data phase.
CLKRUN / CCLKRUN	95	I/O O/D	CLOCK RUN for PCI/CardBus system. In normal operation, the Host asserts this signal to indicate to the 78Q8411, normal clock operation. On the other hand, the Host will de-assert this signal when the clock is going down to a non-operating frequency. When 78Q8411 recognizes the de-asserted status of CLKRUN, then it can assert CLKRUN to request host to maintain or restore normal clock operation. When CLKRUN function is disabled, the 78Q8411 will set CLKRUN in tri-state.

BOOTROM / EEPROM Interface (continued)

NAME	PIN	TYPE	DESCRIPTION
BRA0	102	O	BootROM Address 0:16
BRA1	103		
BRA2	105		
BRA3	106		
BRA4	112		
BRA5	113		
BRA6	114		
BRA7	115		
BRA8	116		
BRA9	117		
BRA10	132		
BRA11	133		
BRA12	134		
BRA13	135		
BRA14	136		
BRA15	137		
BRA16	111		
BRD0	120	I/O	BootROM Data 0:4
BRD1	121		
BRD2	123		
BRD3	124		
BRD4	126		
			BootROM data bus bits (5~7), and
BRD5/EEDO	127	O/I	EEDO: Data Output of serial EEPROM (Input data to 78Q8411)
BRD6/EEDI	128	O/I	EEDI: Data Input of serial EEPROM (78Q8411 output data to EEPROM)
BRD7/EECK	129	O/I	EECK: Clock input to serial EEPROM (The 78Q8411 outputs the clock signal to EEPROM.)
EECS	130	O	Chip Select of serial EEPROM
$\overline{\text{BRCS}}$	131	O	BootROM Chip Select: $\overline{\text{BRCS}}$ is typically active low.
$\overline{\text{BROE}}$	118	O	BootROM Read Enable: $\overline{\text{BROE}}$ is active low for flash ROM application.
$\overline{\text{BRWE}}$	119	O	BootROM Write Enable: $\overline{\text{BRWE}}$ is active low for flash ROM application.

PHYSICAL INTERFACE

sysclk	139	I	SYSTEM CLOCK inputs: Connected to a 25MHz reference signal.
Gpio0 Gpio1 Gpio2 Gpio3	141 142 143 144	I/O	GENERAL PURPOSE I/O: These pin performs the input function at the initialization after power-on or hardware reset. This input impedance when performing an input function is typically larger than 30K. This pin can be configured by software to perform either an input or output function, including a status LED
Vaux	99	I	AUXILIARY POWER INDICATOR: When this pin is asserted, it indicates an auxiliary power source is supported. ACPI purpose is for detecting the auxiliary power source. This pin should be or-wired connected to 1) 3.3V when PCI2.2 / 3.3Vaux support , or 2) 5V when 5Vaux support from 3-way switch.
Vcc-detect	100	I	VCC DETECTION: When this pin is asserted, it indicates that the PCI/CardBus power source is supported. ACPI purpose is for detecting if the main power is present. This pin should be connected to PCI/CardBus bus power source +5V/3.3V.
Vdd_5V_3V	101	I(A)	I/O VOLTAGE REFERENCE: This pin is the analog input voltage reference for 3v/5v tolerance I/O cells. The voltage depends on the type of bus connected (PCI or CardBus). i.e. typically PCI 1.0 (5V), or CardBus (3.3V) 1) 5V when +5V main power exists or 2) 3.3V when 3.3Vaux support (PCI 2.2 , D3cold , no 5V power source) , or 3) 5V when +5 Vaux support from 3-way switch. (D3cold mode)
$\overline{\text{PHY}}$_link	107	I	PHY LINK: Active low when link is established.
PCI_cardz	109	I	PCI / CardBus MODE SELECT: Connect PCI_cardz to Vcc for PCI bus, and to Ground (GND) for CardBus operation. Use a 10k series resistor.
Test(GND)	110	T	TEST: This pin is used for test only. Make connection to ground through 10k resistor for normal operation.

POWER SUPPLY

Vcc (3.3V)	7, 26, 33, 39, 48, 54, 62, 69, 78, 85, 92, 104, 122	S	SUPPLY VOLTAGE:
Vcc-IR (3.3V)	21, 56, 75, 138	S	SUPPLY VOLTAGE-INTERNAL REFERENCE: Core supply connections
GND (Ground)	8, 30, 38, 47, 53, 61, 68, 77, 84, 91, 98, 108, 125	S	GROUND:
GND-IR (Ground)	24, 44, 82, 140	S	GROUND-INTERNAL REFERENCE: Core supply return connections

REGISTER DESCRIPTIONS

The configuration registers are used to initialize and configure the 78Q8411 for identifying and querying the 78Q8411.

The PCI/CardBus control/status registers are used to communicate between the host and the 78Q8411. The host can initialize, control, and read the status of the 78Q8411 through the mapped I/O or memory address space.

The 78Q8411 also provides receive and transmit descriptors for packet buffering and management. These descriptors are detailed in the following section

CONFIGURATION REGISTERS

The configuration registers initialize and configure 78Q8411. All of the contents of configuration registers are set to default value when any hardware reset occurs. On the other hand, there is no effect to their value when the software reset occurs. To access these configuration registers, the 78Q8411 provides byte, word, and double word data access length.

CONFIGURATION REGISTERS LIST

OFFSET	INDEX	NAME	DESCRIPTION
00h	CR0	LID	Loaded Device ID and Vendor ID
04h	CR1	CSC	Configuration Status and Command
08h	CR2	CC	Class Code and revision number
0ch	CR3	LT	Latency Timer
10h	CR4	IOBA	IO Base Address
14h	CR5	MBA	Memory Base Address
28h	CR10	CIS	Card Information Structure (for CardBus)
2ch	CR11	SID	Subsystem ID and vendor ID
30h	CR12	BRBA	Boot ROM Base Address (ROM size = 256KB)
34h	CR13	CP	Capability Pointer
3ch	CR15	CINT	Configuration Interrupt
40h	CR16	DS	Driver Space for special purpose
80h	CR32	SIG	Signature of 78Q8411
c0h	CR48	PMR0	Power Management Register 0
c4h	CR49	PMR1	Power Management Register 1

CONFIGURATION REGISTERS TABLE

offset	bit31 ------- bit16		bit15 ------- bit0		
00h	Device ID*		Vendor ID*		
04h	Status		Command		
08h	Base Class Code	Subclass	-------	Revision #	Step #
0ch	-------	-------	Latency Timer	cache line size	
10h	Base I/O address				
14h	Base memory address				
18h~ 24h	Reserved				
28h	**ROM-im***	**Address space offset***			**Add-indi***
2ch	Subsystem ID*		Subsystem Vendor ID*		
30h	**Boot ROM base address**				
34h	Reserved				Capabilities Pointer
38h	Reserved				
3ch	Max_Lat*	Min_Gnt*	Interrupt pin	Interrupt line	
40h	Reserved		**Driver Space**	Reserved	
80h	**Signature of 78Q8411**				
c0h	**PMC**		**Next_Item_Ptr**	**Cap_ID**	
c4h	Reserved		**PMCSR**		

Note: *: automatically recalled from EEPROM when PCI reset is de-asserted
CIS(28h) is a read-only register
DS(40h), bit 15-8 is read/write able register
SIG(80h) is hard wired register, read only

CONFIGURATION REGISTERS DESCRIPTIONS

Default Value: From EEPROM = Loaded from EEPROM. X = Not applicable or Don't Care
RW Type: RO = Read only. R/W = Read and Write capable. R/W1C: = Read and Write 1 cleared.

CR0 (offset=00h), LID – Loaded Device Identification (ID) of and Vendor ID.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~16	LDID	LOADED DEVICE ID: The device ID number is loaded from serial EEPROM.	From EEPROM	RO
15~0	LVID	LOADED VENDOR ID: The vendor ID number is loaded from serial EEPROM.	From EEPROM	RO

CR1 (offset=04h), CSC – Configuration Status and Command

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31	SPE	STATUS OF PARITY ERROR: 1: indicates that the 78Q8411 detected a parity error. This bit will be set in this condition, even if the parity error response(bit 6 of CR1) is disabled.	0	R/W
30	SES	STATUS OF SYSTEM ERROR: 1: indicates that the 78Q8411 asserted the system error pin, SERR#.	0	R/W
29	SMA	STATUS OF MASTER ABORT: 1: indicates that the 78Q8411 received a master abort and terminated a master transaction.	0	R/W
28	STA	STATUS OF TARGET ABORT: 1: indicates that the 78Q8411 received a target abort and terminated a master transaction.	0	R/W
27	---	Reserved.		
26, 25	SDST	STATUS OF DEVICE SELECT TIMING: The timing of the assertion of device select. 01: indicates a medium assertion of DEVSEL#	01	RO
24	SDPR	STATUS OF DATA PARITY REPORT: 1: when three conditions are met: a. 78Q8411 asserted parity error - $\overline{\text{PERR}}$, or it detected parity error asserted by other device. b. 78Q8411 is operating as a bus master. c. 78Q8411's parity error response bit(bit 6 of CR1) is enabled.	0	R/W

CONFIGURATION REGISTERS DESCRIPTIONS (continued)

CR1 (offset=04h), CSC – Configuration Status and Command (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
23	SFBB	STATUS OF FAST BACK-TO-BACK: Always 1, since 78Q8411 has the ability to accept fast back to back transactions.	1	RO
22~21	---	Reserved.		
20	NC	NEW CAPABILITIES: This bit indicates whether the 78Q8411 provides a list of extended capabilities, such as PCI power management. 1: the 78Q8411 provides PCI management function. 0: the 78Q8411 doesn't provide New Capabilities.	Same as bit 19 of CSR18	RO
19~ 9	---	Reserved.		
8	CSE	COMMAND OF SYSTEM ERROR RESPONSE: 1: enable system error response. The 78Q8411 will assert SERR# when it finds a parity error during the address phase.	0	R/W
7	---	Reserved.		
6	CPE	COMMAND OF PARITY ERROR RESPONSE: 0: disable parity error response. The 78Q8411 will ignore any detected parity error and keep on its operating. Default value is 0. 1: enable parity error response. The 78Q8411 will assert system error (bit 13 of CSR5) when a parity error is detected.	0	R/W
5~ 3	---	Reserved.		
2	CMO	COMMAND OF MASTER OPERATION ABILITY: 0: disable the bus master ability. 1: enable the CardBus bus master ability. Default value is 1 for normal operation.	0	R/W
1	CMSA	COMMAND OF MEMORY SPACE ACCESS: 0: disable the memory space access capability. 1: enable the memory space access capability.	0	R/W
0	CIOSA	COMMAND OF I/O SPACE ACCESS: 0: enable the I/O space access capability. 1: disable the I/O space access capability.	0	R/W

CONFIGURATION REGISTERS DESCRIPTIONS (continued)

CR2 (offset=08h), CC – Class Code and Revision Number

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~24	BCC	BASE CLASS CODE: It indicates the 78Q8411 is network controller.	02h	RO
23~16	SC	SUBCLASS CODE: It indicates the 78Q8411 is a Fast Ethernet Controller.	00h	RO
15~ 8	---	Reserved.		
7 ~ 4	RN	REVISION NUMBER: Identifies the revision number of the 78Q8411.	1h	RO
3 ~ 0	SN	STEP NUMBER: Identifies the 78Q8411 steps within the current revision.	1h	RO

CR3 (offset=0ch), LT – Latency Timer

31~16	---	Reserved.		
15~ 8	LT	LATENCY TIMER: This value specifies the latency timer of the 78Q8411 in units of PCI bus clock. Once the 78Q8411 asserts FRAME#, the latency timer starts to count. If the latency timer expires and the 78Q8411 still asserted FRAME#, then the 78Q8411 will terminate the data transaction as soon as its GNT# is removed.	0	R/W
7 ~ 0	CLS	CACHE LINE SIZE: This value specifies the system cache line size in units of 32-bit double words (DW). The 78Q8411 supports 8, 16, and 32 DW of cache line size. This value is used by the 78Q8411 driver to program the cache alignment bits (bit 14 and 15 of CSR0). The cache alignment bits are used for cache oriented PCI commands, say memory-read-line, memory-read-multiple, and memory-write-and-invalidate.	0	R/W

CR4 (offset=10h), IOBA – I/O Base Address

31~ 8	IOBA	I/O BASE ADDRESS: This value indicates the base address of PCI control and status register (CSR0~28).	0	R/W
7 ~ 1	---	Reserved.		
0	IOSI	I/O SPACE INDICATOR: 1: indicates that the configuration registers map into the I/O space.	1	RO

CONFIGURATION REGISTERS DESCRIPTIONS (continued)

CR5 (offset=14h), MBA – Memory Base Address.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~ 10	MBA	MEMORY BASE ADDRESS:. This value indicates the base address of PCI control and status register(CSR0~28)	0	R/W
9 ~ 1	---	Reserved.		
0	IOSI	MEMORY SPACE INDICATOR: 1: indicates that the configuration registers map into the I/O space.	0	RO

CR10 (offset=28h), CIS – card Information Structure. This register is used to point one of the possible address spaces where the CIS begins. This register is designed for CardBus environment. Its data is auto-loaded from the serial EEPROM after power on or hardware reset.

31~28	RI	ROM IMAGE: This ROM image value is applied when the CIS is stored in a boot ROM. This value is loaded from serial EEPROM.	From EEPROM	RO
27~ 3	ASO	ADDRESS SPACE OFFSET: This value indicate the offset within the address space. The address space is specified by address space indicator (bit 2~0 of CR10).	From EEPROM	RO
2 ~ 0	ASI	ADDRESS SPACE INDICATOR: This value indicates the location where the CIS address space begins. 7: indicates that the CIS begins in the boot ROM space. Other than 7: makes all the bits of CIS reset to 0.	From EEPROM	RO

CR11 (offset=2ch), SID – Subsystem and Vendor ID.

31~16	SID	SUBSYSTEM ID: This value is loaded from EEPROM after power on or hardware reset.	From EEPROM	RO
15~ 0	SVID	SUBSYSTEM VENDOR ID: This value is loaded from EEPROM after power on or hardware reset.	From EEPROM	RO

CR12 (offset=30h), BRBA – Boot ROM Base Address.

31~17	BRBA	BOOT ROM BASE ADDRESS: This value indicates the address mapping of the boot ROM field. Furthermore, it also defines the boot ROM size. The value of bits 16~1 is set to 0, as the 78Q8411 supports up to 128kB of boot ROM.	X: b31~17	R/W
16 ~ 1	---	Reserved	0: b16~1	
0	BRE	BOOT ROM ENABLE: The 78Q8411 enables its boot ROM access only if both the memory space access bit, CMSA, (bit 1 of CR1) and this bit are set to 1. 1: enable Boot ROM. (Combines with bit 1 of CR1)	0	R/W

CONFIGURATION REGISTERS DESCRIPTIONS (continued)

CR13 (offset=34h), CP – Capabilities Pointer.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~8	---	Reserved		
7~0	CP	CAPABILITIES POINTER. Points to the location (offset in hex) of the power-management register block in the PCI configuration space.	c0h	RO

CR15 (offset=3ch), CINT – Configuration Interrupt.

31~24	ML	Max_Lat REGISTER: This value indicates "how often" the 78Q8411 needs to access to the CardBus bus in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset.	From EEPROM	RO
23~16	MG	Min_Gnt REGISTER: This value indicates how long the 78Q8411 needs to retain the CardBus bus ownership whenever it initiates a transaction, in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset.	From EEPROM	RO
15~ 8	IP	INTERRUPT PIN. This value indicates which of the four interrupt request pins that the 78Q8411 is connected to. Always 01h: indicates the 78Q8411 connects to INTA#	01h	RO
7 ~ 0	IL	INTERRUPT LINE. This value indicates which of the system interrupt request lines the INTA# of 78Q8411 is routed to. The BIOS will write this field when it initializes and configures the system. The 78Q8411 driver can use this value to determine priority and vector information.	X	R/W

CR16 (offset=40ch), DS – Driver Space for Special Purpose.

31~16	---	Reserved		
15~8	DS	DRIVER SPACE FOR SPECIAL PURPOSE: Since this area won't be cleared in the software reset. The 78Q8411 driver can use this R/W area for special purpose.	X	R/W
7 ~ 0	---	Reserved		

CR32 (offset=80ch), SIG – Signature of 78Q8411.

31~16	DID	DEVICE ID: This is the number of the 78Q8411.	8410h	RO
15~0	VID	VENDOR ID: This is the number for TDK Semiconductor.	1626h	RO

CONFIGURATION REGISTERS DESCRIPTIONS (continued)

CR48 (offset=c0h), PMR0 – Power Management Register 0.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~27	PMES	PME_Support: The 78Q8411 may assert PME#/CSTSCHG signal while in the D0, D1, D2, D3hot, and D3cold power state. The 78Q8411 supports Wake-up from the above states.	11111b	RO
26	D2S	D2_Support: The 78Q8411 supports D2 Power Management State.	1	RO
25	D1S	D1_Support: The 78Q8411 supports D1 Power Management State.	1	RO
24~22	AUXC	AUX CURRENT: These three bits report the maximum 3.3 Vaux current requirements for 78Q8411. If bit 31 of PMR0 is '1', the default value is 111b, which indicates the 78Q8411 needs 375 mA to support remote wake-up from D3cold power state. Otherwise, default value is 000b, which indicates the 78Q8411 does not support remote wake-up from D3cold power state.	111b or 000b	RO
21	DSI	DEVICE SPECIFIC INITIALIZATION: This bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. 0: indicates that the function does not require a device specific initialization sequence following transition to the D0 un-initialized state.	0	RO
20	---	Reserved.	0	RO
19	PMEC	PME CLOCK: When "1" it indicates that the 78Q8411 relies on the presence of the PCI clock for PME#/CSTSCHG operation. While "0" indicates that no PCI clock is required for the 78Q8411 to command the PME#/CSTSCHG pin.	0	RO
18~16	VER	VERSION: The value of 010b indicates that the 78Q8411 complies with Revision 1.0a of the PCI Power Management Interface Specification.	010b	RO
15~8	NIP	NEXT ITEM POINTER: This value is always 00h, indicating that there are no additional items in the Capabilities List.	00h	RO
7~0	CAPID	CAPABILITY IDENTIFIER: This value is always 01h, indicating the link list item as being the PCI Power Management Registers.	01h	RO

CONFIGURATION REGISTERS DESCRIPTIONS (continued)

CR49 (offset=c4h), PMR1 – Power Management Register 1.
(This register maps read only to CSR20 (offset = 90h) - PMCSR, Power Management Command and Status.)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~16	---	Reserved		
15	PMES	PME_Status: This bit is set when the 78Q8411 would normally assert the PME#/CSTSCHG signal for a wake-up event. This bit is independent of the state of the PME-En (bit 8). Writing a "1" to this bit will clear it and cause the 78Q8411 to stop asserting a PME#/CSTSCHG (if enabled by PME-En (bit 8).). Writing a "0" has no effect.	0	R/W1C
14,13	DSCAL	DATA_SCALE: indicates the scaling factor to be used when interpreting the value of the Data register. The 78Q8411 doesn't support Data register and Data_Scale.	00b	RO
12~9	DSEL	DATA_SELECT: This four bit field is used to select which data is to be reported through the Data register and Data_Scale field. The 78Q8411 doesn't support Data_Select.	0h	R/W
8	PME_En	PME_Enable: "1" enables the 78Q8411 to assert PME#/CSTSCHG. "0" disables the PME#/CSTSCHG assertion. This bit defaults to "0" if the function does not support PME#/CSTSCHG generation from D3cold. Magic Packet™ default enable : CSR18< WOL bit 18> and CSR18< PM bit 19> set → CSR13< MPRE bit 9> set , then PME#/CSTSCHG asserts regardless of PME_En state.	0	R/W
7~2	---	Reserved.	000000b	RO
1,0	PWRS	POWER STATE: This two bit field is used both to determine the current power state of the 78Q8411 and to set the 78Q8411 into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot This field is auto cleared to D0 when power resumed. If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus, however, the data is discarded and no state change occurs.	00b	R/W

PCI/CardBus CONTROL REGISTERS

PCI/CARDBUS CONTROL/STATUS REGISTERS LIST

offset from base address of CSR	INDEX	NAME	DESCRIPTION
00h	CSR0	PAR	PCI/CardBus access register
08h	CSR1	TDR	Transmit Demand Register
10h	CSR2	RDR	Receive Demand Register
18h	CSR3	RDB	Receive Descriptor Base Address
20h	CSR4	TDB	Transmit Descriptor Base Address
28h	CSR5	SR	Status Register
30h	CSR6	NAR	Network Access Register
38h	CSR7	IER	Interrupt Enable Register
40h	CSR8	LPC	Lost Packet Counter
48h	CSR9	SPR	Serial Port Register
50h	CSR10	---	Reserved
58h	CSR11	TMR	Timer
60h	CSR12	---	Reserved
68h	CSR13	---	Reserved
70h	CSR14	---	Reserved
78h	CSR15	WTMR	Watchdog Timer
80h	CSR16	ACSR5	Status Register 2
84h	CSR17	ACSR7	Interrupt Enable Register 2
88h	CSR18	CR	Command Register
8ch	CSR19	PCIC	PCI Bus Performance Counter
90h	CSR20	PMCSR	Power Management Command And Status
94h	CSR21	WTDP	Current Transmit Descriptor Point
98h	CSR22	WRDP	Current Receive Descriptor Point
9ch	CSR23	TXBR	Transmit Burst Counter/Time-Out Register
a0h	CSR24	FROM	Flash(Boot) ROM Port
a4h	CSR25	PAR0	Physical Address Register 0
a8h	CSR26	PAR1	Physical Address Register 1
ach	CSR27	MAR0	Multicast Address Hash Table Register 0
b0h	CSR28	MAR1	Multicast Address Hash Table Register 1
100h		FER	Function Event Register
104h		FEMR	Function Event Mask Register
108h		FPSR	Function Present State Register
10ch		FFER	Function Force Event Register

CONTROL/STATUS REGISTER DESCRIPTION

Default Value: From EEPROM = Loaded from EEPROM. X = Not applicable or Don't Care

RW Type: RO = Read only. R/W = Read and Write capable. R/W1C: = Read and Write 1 cleared.
R/W-TxRxStop = Read and Write capable. Before writing, the transmit and receive operations should be stopped.
R/W-TxStop = Read and Write capable. Before writing, the transmit and receive operations should be stopped.
R/W-RxStop = Read and Write capable. Before writing, the receive operations should be stopped.
R/W-TxSup = Read and Write capable. Before writing, the transmit process should be in the suspended state.
R/W-RxSup = Read and Write capable. Before writing, the receive process should be in the suspended state.
RO/LHC = Read only, latching high and cleared after read.
RO/LH-W1C = Read only, latching high and cleared by writing 1.
RO-RC = Read only and cleared by reading.

CSR0 (offset=00h), PAR – PCI/CardBus Access Register.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~25	---	Reserved		
24	MWIE	MEMORY WRITE AND INVALIDATE ENABLE: 1: enables the 78Q8411 to generate memory write invalidate command. The 78Q8411 will generate this command while writing full cache lines. 0: disables the 78Q8411 from generating memory write invalidate command and uses memory write commands instead.	0	R/W-TxRxStop
23	MRLE	MEMORY READ LINE ENABLE: 1: enables the 78Q8411 to generate memory read line command, while read access instruction reach the cache line boundary. If the read access instruction doesn't reach the cache line boundary, then the 78Q8411 uses the memory read command instead.	0	R/W-TxRxStop
22	---	Reserved		
21	MRME	MEMORY READ MULTIPLE ENABLE: 1: enables the 78Q8411 to generate memory read multiple command while reading full cache line. If the memory is not cache aligned, the 78Q8411 uses memory read command instead.	0	R/W-TxRxStop
20~19	---	Reserved		
18,17	TAP	TRANSMIT AUTO-POLLING in transmit suspended state: 00: disable auto-polling (default) 01: polling TES0 OWN <bit 31> every 200 us 10: polling TES0 OWN <bit 31> every 800 us 11: polling TES0 OWN <bit 31> every 1600 us	00b	R/W-TxRxStop
16	---	Reserved		

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR0 (offset=00h), PAR – PCI/CardBus Access Register. (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
15, 14	CAL	CACHE ALIGNMENT: This is the address boundary for data burst. It is set after reset. 01: 8 DW boundary alignment 10: 16 DW boundary alignment	10b	R/W-TxRxStop
13 ~ 8	PBL	PROGRAMMABLE BURST LENGTH: This value defines the maximum number of DW to be transferred in one DMA transaction. values: 8 or 16(default)	010000b	R/W-TxRxStop
7	BLE	BIG OR LITTLE ENDIAN selection: 0: little endian (e.g. INTEL) 1: big endian (only for data buffer)	0	R/W-TxRxStop
6 ~ 2	DSL	DESCRIPTOR SKIP LENGTH: Defines the gap between two descriptions in the units of DW (32-bit double words).	00000b	R/W-TxRxStop
1	BAR	BUS ARBITRATION: 0: receive is higher priority. 1: transmit is higher priority.	0	R/W-TxRxStop
0	SWR	SOFTWARE RESET: 1: resets all internal hardware, except configuration registers. This signal will be cleared by 78Q8411 itself after it completed the reset process.	0	R/W-TxRxStop

CSR1 (offset=08h), TDR – Transmit Demand Register.

31~ 0	TPDM	TRANSMIT POLL DEMAND: When written any value in suspended state, trigger read-tx-descriptor process and check the TES0 OWN <bit 31> , if it = 1, then start transmit process	ffffffffh	R/W-TxSup

CSR2 (offset=10h), RDR – Receive Demand Register.

31 ~ 0	RPDM	RECEIVE POLL DEMAND: When written any value in suspended state, trigger the read-rx-descriptor process and check RDES0 OWN <bit 31> , if it = 1, then start move data to buffer from FIFO	ffffffffh	R/W-RxSup

CSR3 (offset=18h), RDB – Receive Descriptor Base Address.

31~ 2	SAR	START ADDRESS OF RECEIVE descriptor	xxxxxxx	R/W-RxSup
1, 0	RBND	RECEIVE DW BOUNDRY: Is set to 00.	00	RO

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR4 (offset=20h), TDB – Transmit Descriptor Base Address.

31~ 2	SAT	START ADDRESS OF TRANSMIT descriptor	xxxxxx	R/W-TxSup
1, 0	TBND	TRANSMIT DW BOUNDRY: Is set to 00.	00	RO

R/W* = Before writing, the transmit process should be stopped. xxxxxxx = not applicable.

CSR5 (offset=28h), SR – Status Register

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~ 26	----	Reserved		
25~ 23	BET	BUS ERROR TYPE: This field is valid only when FBE, fatal bus error, bit 13, of CSR5 is set. There is no interrupt generated by this field. Values: 000: Parity Error, 001: Master Abort, 010: Target Abort 011, 1xx:Reserved	000b	RO
22~ 20	TS	TRANSMIT STATE: Report the current transmission state only, no interrupt will be generated. 000: Stop 001: Read Descriptor 010: Transmitting 011: FIFO fill, read data from memory and put into FIFO 100: & 101: Reserved 110: Suspended, Unavailable Transmit Descriptor Or FIFO Overflow 111: Write Descriptor	000b	RO
19~17	RS	RECEIVE STATE: Report current receive state only, no interrupt will be generated. 000: stop 001: read descriptor 010: check this packet and pre-fetch next descriptor 011: wait for receiving data 100: suspended 101: write descriptor 110: flush the current FIFO 111: FIFO drain, move data from receiving FIFO into memory	000b	RO
16	NISS	NORMAL INTERRUPT STATUS SUMMARY: It's set if any of below bits of CSR5 asserted.(combines with bit 16 of ACSR5) bit 0, TCI, transmit completed interrupt bit 2, TDU, transmit descriptor unavailable bit 6, RCI, receive descriptor interrupt	0	RO/LH-W1C

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR5 (offset=28h), SR – Status Register (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
15	AISS	ABNORMAL INTERRUPT STATUS SUMMARY: It's set if any of below bits of CSR5 asserted. (Combines with AAISS, Added Abnormal Interrupt Status Summary, bit 15 of ACSR5.) bit 1, TPS, Transmit Process Stopped bit 3, TJT, Transmit Jabber Timer Time-Out bit 5, TUF, Transmit Under-Flow bit 7, RDU, Receive Descriptor Unavailable bit 8, RPS, Receive Processor Stopped bit 9, RWT, Receive Watchdog Time-Out bit 11, GPTT, General Purpose Timer Time-Out bit 13, FBE, Fatal Bus Error	0	RO/LH-W1C
14	----	Reserved		
13	FBE	FATAL BUS ERROR: 1: while any of Parity Error, Master Abort, or Target Abort occurred (see bits 25~23 of CSR5). The 78Q8411 will disable all bus access. The way to recover parity error is by setting an software reset.	0	RO/LH-W1C
12	GI1	GENERAL PURPOSE INTERRUPT 1	0	RO/LH-W1C
11	GPTT	GENERAL PURPOSE TIMER TIME-OUT: It's based on CSR11 timer register, bits 15~0	0	RO/LH-W1C
10	GI0	GENERAL PURPOSE INTERRUPT 0	0	RO/LH-W1C
9	RWT	RECEIVE WATCHDOG TIME-OUT: based on CSR15 watchdog timer register	0	RO/LH-W1C
8	RPS	RECEIVE PROCESS STOPPED: receive state = stop	0	RO/LH-W1C
7	RDU	RECEIVE DESCRIPTOR UNAVAILABLE: 1: while the next receive descriptor can't be applied by 78Q8411. The receive process is suspended in this situation. To restart the receive process, the ownership bit of next receive descriptor should be set to 78Q8411 and a receive poll demand command should be issued (or a new recognized frame is received, if the receive poll demand is not issued).	0	RO/LH-W1C
6	RCI	RECEIVE COMPLETED INTERRUPT: 1: while a frame reception is completed.	0	RO/LH-W1C
5	TUF	TRANSMIT UNDER-FLOW: 1: while the transmit FIFO had an under-flow condition during transmitting. The transmit process will enter the suspended state and report the under-flow error on bit1 of TDES0.	0	RO/LH-W1C

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR5 (offset=28h), SR – Status Register (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
4	---	Reserved		
3	TJT	TRANSMIT JABBER TIME-OUT: 1: while the transmit jabber timer expired. The transmit processor will enter the stop state and the transmit jabber time-out flag of bit 14 of TDES0 will be asserted.	0	RO/LH-W1C
2	TDU	TRANSMIT DESCRIPTOR UNAVAILABLE: 1: while the next transmit descriptor can't be applied by 78Q8411. The transmission process is suspended in this situation. To restart the transmission process, the ownership bit of next transmit descriptor should be set to 78Q8411 and if the transmit automatic polling is not enabled then a transmit poll demand command should be issued.	0	RO/LH-W1C
1	TPS	TRANSMIT PROCESS STOPPED: 1: while transmit state = stop	0	RO/LH-W1C
0	TCI	TRANSMIT COMPLETED INTERRUPT: 1: indicates a frame transmission is completed while bit 31 of TDES1 is asserted in the first transmit descriptor of the frame.	0	RO/LH-W1C

CSR6 (offset=30h), NAR – Network Access Register.

31~23	---	Reserved		
22		TRANSMIT THRESHOLD MODE: 0: 100 transmit threshold mode 1: 10 transmit threshold mode	0	R/W-TxStop
21	SF	STORE AND FORWARD for transmit: 0: disable 1: enable, ignores the transmit threshold setting	0	R/W-TxStop
20	---	Reserved		
19	SQE	SQE DISABLE: 0: enable SQE function for 10BASE-T operation. The 78Q8411 provides SQE test function for 10BASE-T half duplex operation. 1: disable SQE function.	1	R/W-TxStop
18~16	-----	Reserved		

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR6 (offset=30h), NAR – Network Access Register (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
15~14	TR	TRANSMIT THRESHOLD CONTROL: 00: 128-byte (100Mbps), 72-byte (10Mbps) 01: 256-byte (100Mbps), 96-byte (10Mbps) 10: 512-byte (100Mbps), 128-byte (10Mbps) 00: 1024-byte (100Mbps), 160-byte (10Mbps)	00b	R/W-TxStop
13	ST	STOP TRANSMIT: 0: stop (default) 1: start	0	R/W
12	FC	FORCE COLLISION MODE: 0: disable 1: generate collision when transmit (for test in loop-back mode)	0	R/W-TxRxStop
11, 10	OM	OPERATING MODE: 00: normal 01: MAC loop-back 10,11: Reserved	00	R/W-TxRxStop
9	FD	FULL DUPLEX MODE: 0: half duplex mode 1: full duplex mode	1	R/W-TxRxStop
8	---	Reserved		
7	MM	MULTICAST MODE: 1: receive all multicast packets	0	R/W-RxStop
6	PR	PROMISCUOUS MODE: 1: receive any good packet. 0: receive only the right destination address packets	1	R/W-RxStop
5	SBC	STOP BACK-OFF COUNTER: 1: back-off counter stop when carrier is active, and resume when carrier drop. 0: back-off counter is not effected by carrier	0	R/W-TxRxStop
4	---	Reserved		
3	PB	PASS BAD PACKET 1: receives any packets, if pass address filter, including runt packets, CRC error, truncated packets... For receiving all bad packets, the bit 6 of CSR6 should be set to 1. 0: filters all bad packets	0	R/W-RxStop

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR6 (offset=30h), NAR – Network Access Register (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
2	---	Reserved		
1	SR	START/STOP RECEIVE 0: receive processor will enter stop state after the current reception frame completed. This value is effective only when the receive processor is in the running or suspending state. Notice: In "Stop Receive" state, the PAUSE packet and Remote Wake Up packet won't be effected and can be received if the corresponding function is enabled. 1: receive processor will enter running state.	0	R/W
0	---	Reserved		

CSR7 (offset=38h), IER – Interrupt Enable Register

31~17	---	Reserved		
16	NIE	NORMAL INTERRUPT ENABLE: 1: enable all the normal interrupt bits. (See NISS, bit 16 of CSR5)	0	R/W
15	AIE	ABNORMAL INTERRUPT ENABLE: 1: enable all the abnormal interrupt bits. (See AISS, bit 15 of CSR5)	0	R/W
14	---	Reserved		
13	FBEIE	FATAL BUS ERROR INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable fatal bus error interrupt	0	R/W
12	GIE1	GENERAL INTERRUPT ENABLE ON Gpio1 PIN: (Note : make sure GPC CSR15< bit 27> =1 and GPMD1 CSR15< bit 17>=0) 1: the interrupt from Gpio1 pin is enabled. After a hardware or software reset, the interrupt is disabled.	0	R/W
11	GPTIE	GENERAL PURPOSE TIMER INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable general purpose timer expired interrupt.	0	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR7 (offset=38h), IER – Interrupt Enable Register (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
10	GIE0	GENERAL INTERRUPT ENABLE ON Gpio0 Pin: (Link change) 1: the interrupt from Gpio0 pin is enabled. After a hardware or software reset, the interrupt is disabled	0	R/W
9	RWTIE	RECEIVE WATCHDOG TIME-OUT INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable receive watchdog time-out interrupt.	0	R/W
8	RSIE	RECEIVE STOPPED INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable receive stopped interrupt.	0	R/W
7	RUIE	RECEIVE DESCRIPTOR UNAVAILABLE INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable receive descriptor unavailable interrupt.	0	R/W
6	RCIE	RECEIVE COMPLETED INTERRUPT ENABLE: 1: combine this bit and AIE, bit 16 of CSR7, to enable receive completed interrupt.	0	R/W
5	TUIE	TRANSMIT UNDER-FLOW INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable transmit under-flow interrupt.	0	R/W
4	---	Reserved		
3	TJTTIE	TRANSMIT JABBER TIMER TIME-OUT INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable transmit jabber timer time-out interrupt.	0	R/W
2	TDUIE	TRANSMIT DESCRIPTOR UNAVAILABLE INTERRUPT ENABLE: 1: combine this bit and AIE, bit 16 of CSR7, to enable transmit descriptor unavailable interrupt.	0	R/W
1	TPSIE	TRANSMIT PROCESSOR STOPPED INTERRUPT ENABLE: 1: combine this bit and AIE, bit 15 of CSR7, to enable transmit processor stopped interrupt.	0	R/W
0	TCIE	TRANSMIT COMPLETED INTERRUPT ENABLE: 1: combine this bit and AIE, bit 16 of CSR7, to enable transmit completed interrupt.	0	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR8 (offset=40h), LPC – Lost Packet Counter

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~17	---	Reserved		
16	LPCO	LOST PACKET COUNTER OVERFLOW: 1: while lost packet counter overflowed. Cleared after read.	0	RO/LHC
15~0	LPC	LOST PACKET COUNTER: Increment the counter while packet discarded since there was no host receive descriptors available. Cleared after read.	0	RO/LHC

CSR9 (offset=48h), SPR – Serial Port Register

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~20	---	Reserved		
19	MDI	MII MANAGEMENT DATA INPUT: Specified read data from the external PHY.	0	RW
18	MMC	MII MANAGEMENT CONTROL: 0: Write operation to the external PHY. 1: Read operation from the external PHY.	1	RW
17	MDO	MII MANAGEMENT DATA OUTPUT: Specified Write Data to the external PHY.	0	RW
16	MDC	MII MANAGEMENT CLOCK: 1: MII Management Clock is a output reference clock to the external PHY	0	RW
15	---	Reserved		
14	SRC	SERIAL EEPROM READ CONTROL:	X	RW
13	SWC	SERIAL EEPROM WRITE CONTROL:	X	RW
12	---	Reserved		
11	SRS	SERIAL EEPROM SELECT:	X	RW
10~4	---	Reserved		
3	SDO	SERIAL EEPROM DATA OUT: This bit serially shifts data from the EEPROM to the 78Q8411.	1	RO
2	SDI	SERIAL EEPROM DATA IN: This bit serially shifts data from the 78Q8411 to the EEPROM.	1	R/W
1	SCLK	SERIAL EEPROM CLOCK: High/Low: this bit provides the clock signal for EEPROM.	1	R/W
0	SCS	SERIAL EEPROM CHIP SELECT: 1: selects the serial EEPROM chip.	1	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR11 (offset=58h), TMR – General-purpose Timer.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~17	---	Reserved		
16	COM	CONTINUOUS OPERATION MODE: 1: sets the general-purpose timer in continuous operating mode.	0	R/W
15~0	GTV	GENERAL-PURPOSE TIMER VALUE: Sets the counter value. This is a count-down counter with the cycle time of 204us.	0	R/W

CSR13 (offset=68h), WCSR – Wake-up Control/Status Register

31	---	Reserved		
30	CRCT	CRC-16 TYPE 0: Initial contents = 0000h 1: Initial contents = ffffh	0	R/W
29	WP1E	Wake-up Pattern One Matched Enable:	0	R/W
28	WP2E	Wake-up Pattern Two Matched Enable:	0	R/W
27	WP3E	Wake-up Pattern Three Matched Enable:	0	R/W
26	WP4E	Wake-up Pattern Four Matched Enable:	0	R/W
25	WP5E	Wake-up Pattern Five Matched Enable:	0	R/W
24-18	---	Reserved		
17	LinkOFF	LINK OFF DETECT ENABLE: The 78Q8411 will set the LSC bit after it has detected that link status changed from ON to OFF.	0	R/W
16	LinkON	LINK ON DETECT ENABLE: The 78Q8411 will set the LSC bit after it has detected that link status changed from OFF to ON.	0	R/W
15-11	---	Reserved		
10	WFRE	WAKE-UP FRAME RECEIVED ENABLE: The 78Q8411 will include the “Wake-up Frame Received” event into wake-up events. If this bit is set, the 78Q8411 will assert PMES, bit 15 of PMR1, after the 78Q8411 has received a matched wake-up frame.	0	R/W
9	MPRE	MAGIC PACKET™ RECEIVED ENABLE: The 78Q8411 will include the “Magic Packet™ Received” event into wake-up events. If this bit is set, the 78Q8411 will assert PMES, bit 15 of PMR1, after the 78Q8411 has received a Magic packet.	0	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR13 (offset=68h), WCSR – Wake-up Control/Status Register (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
8	LSCE	LINK STATUS CHANGED ENABLE: The 78Q8411 will include the "Link Status Changed" event into wake-up events. If this bit is set, the 78Q8411 will assert PMES, bit 15 of PMR1, after the 78Q8411 has detected a link status changed event.	0	R/W
7-3	---	Reserved		
2	WFR	WAKE-UP FRAME RECEIVED: 1: Indicates the 78Q8411 has received a wake-up frame. It is cleared by writing 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C
1	MPR	MAGIC PACKET™ RECEIVED: 1: Indicates the 78Q8411 has received a magic packet. It is cleared by writing 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C
0	LSC	LINK STATUS CHANGED: 1: Indicates 78Q8411 has detected a link status change event. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset.	X	R/W1C

CSR14 (offset=70h), WPDR – Wake-up Pattern Data Register

0000h	Wake-up pattern 1 mask bits 31:0		
0004h	Wake-up pattern 1 mask bits 63:32		
0008h	Wake-up pattern 1 mask bits 95:64		
000ch	Wake-up pattern 1 mask bits 127:96		
0010h	CRC16 of pattern 1	0010h	CRC16 of pattern 1
0014h	Wake-up pattern 2 mask bits 31:0		
0018h	Wake-up pattern 2 mask bits 63:32		
001ch	Wake-up pattern 2 mask bits 95:64		
0020h	Wake-up pattern 2 mask bits 127:96		
0024h	CRC16 of pattern 2	0024h	CRC16 of pattern 2
0028h	Wake-up pattern 3 mask bits 31:0		
002ch	Wake-up pattern 3 mask bits 63:32		
0030h	Wake-up pattern 3 mask bits 95:64		
0034h	Wake-up pattern 3 mask bits 127:96		
0038h	CRC16 of pattern 3	0038h	CRC16 of pattern 3
003ch	Wake-up pattern 4 mask bits 31:0		
0040h	Wake-up pattern 4 mask bits 63:32		

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR14 (offset=70h), WPDR – Wake-up Pattern Data Register (continued)

0044h	Wake-up pattern 4 mask bits 95:64		
0048h	Wake-up pattern 4 mask bits 127:96		
004ch	CRC16 of pattern 4	004ch	CRC16 of pattern 4
0050h	Wake-up pattern 5 mask bits 31:0		
0054h	Wake-up pattern 5 mask bits 63:32		
0058h	Wake-up pattern 5 mask bits 95:64		
005ch	Wake-up pattern 5 mask bits 127:96		
0060h	CRC16 of pattern 5	0060h	CRC16 of pattern 5

1. CRC-16 polynomial: It is downloaded through the software driver.
2. Offset value is from 0-255 (8-bit width).
3. To load the whole wake-up frame filtering information, write consecutive long words to CSR14.

CSR15 (offset=78h), WTMR – Watchdog Timer.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~28	---	Reserved		
27	GPC	GENERAL-PURPOSE PINS CONTROL: 1: the value on bit 19~16 of CSR15 will control the I/O type of the general-purpose I/O (Gpio)pins. 0: the value on bit 19~16 of CSR15 will be the output data when the general-purpose pin is set to output pin.	0	R/W
26~20	---	Reserved		
19~16	GPMD3 ~ GPMD0	GENERAL PURPOSE MODE AND DATA for Gpio0~Gpio3 When the GPC, bit 27 of CSR15, is set, the value that is written to the GPMD3~GPMD0 sets the I/O type of pins Gpio3~0. 1: output pin 0: input pin When the GPC, bit 27 of CSR15, is reset, the values are shown of the pins that are configured as output pins. When Gpio1 pin is selected as input pin and the GIE1, bit 12 of CSR7, is enabled , an interrupt occurred when either this pin changes state from 0 to1 or 1 to 0	0	R/W
15~6		Reserved		
5	RWR	RECEIVE WATCHDOG RELEASE: This is the release time of the watchdog timer from last carrier deasserted. 0: 24 bit-time 1: 48 bit-time	0	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR15 (offset=78h), WTMR – Watchdog Timer (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
4	RWD	RECEIVE WATCHDOG DISABLE: 0: If the receiving packet's length is longer than 2560 bytes, the watchdog timer will be expired. 1: disable the receive watchdog.	0	R/W
3	---	Reserved		
2	JCLK	JABBER CLOCK: 0: cut off transmission after 2.6 ms (100Mbps) or 26 ms (10Mbps). 1: cut off transmission after 2560 byte-time.	0	R/W
1	NJ	NON-JABBER: 0: if jabber expired, re-enable transmit function after 42 ms (100Mbps) or 420ms (10Mbps) 1: immediately re-enable the transmit function after jabber expired.	0	R/W
0	JBD	JABBER DISABLE: 1: disable transmit jabber function	0	R/W

CSR16 (offset=80h), ACSR5 – Assistant CSR5 (Status Register 2)

31	TEIS	TRANSMIT EARLY INTERRUPT STATUS: Transmit early interrupt status is set to 1 when Transmit early interrupt function is enabled (set bit 31 of CSR17 = 1) and the transmitted packet is moved completed from descriptors to TX-FIFO buffer. This bit is cleared by writing 1.	0	RO/LH-W1C
30	REIS	RECEIVE EARLY INTERRUPT STATUS: Receive early interrupt status is set to 1 when Receive early interrupt function is enabled (set bit 30 of CSR17 = 1) and the received packet fills up its first receive descriptor. This bit is cleared by writing 1.	0	RO/LH-W1C
29	LCS	LINK CHANGE STATUS:	0	RO/LH-W1C
28	TDIS	TRANSMIT DEFERRED INTERRUPT STATUS:	0	RO/LH-W1C
27	---	Reserved		
26	PFR	PAUSE FRAME RECEIVED INTERRUPT STATUS: 1: indicates a PAUSE frame was received when the PAUSE function is enabled.	0	RO/LH-W1C
25~17	---	Reserved		
16	ANISS	ADDED NORMAL INTERRUPT STATUS SUMMARY: 1: any of the added normal interrupts occurred.	0	RO/LH-W1C

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR16 (offset=80h), ACSR5 – Assistant CSR5 (Status Register 2) (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
15	AAISS	ADDED ABNORMAL INTERRUPT STATUS SUMMARY: 1: any of added abnormal interrupts occurred.	0	RO/LH-W1C
14~0		These bits are the same as the status register of CSR5. You can access those status bits through either CSR5 or CSR16.		RO/LH-W1C

CSR17 (offset=84h), ACSR7 – Assistant CSR7 (Interrupt Enable Register 2).

31	TEIE	TRANSMIT EARLY INTERRUPT ENABLE:	0	R/W
30	REIE	RECEIVE EARLY INTERRUPT ENABLE:	0	R/W
29	LCIE	LINK CHANGE INTERRUPT ENABLE:	0	R/W
28	TDIE	TRANSMIT DEFERRED INTERRUPT ENABLE:	0	R/W
27	---	Reserved		
26	PFRIE	PAUSE FRAME RECEIVED INTERRUPT ENABLE:	0	R/W
25~17	---	Reserved		
16	ANISE	ADDED NORMAL INTERRUPT SUMMARY ENABLE: 1: adds the interrupts of bit 30 REIE and 31 TEIE of ACSR7 to the normal interrupt summary (bit 16 of CSR5).	0	R/W
15	AAIE	ADDED ABNORMAL INTERRUPT SUMMARY ENABLE.: 1: adds the interrupt of bit 26 (PFRIE), 28 (TDIE) and 29 (LCIE) of ACSR7 to the abnormal interrupt summary (bit 15 of CSR5)..	0	R/W
14~0		These bits are the same as the interrupt enable register of CSR7. You can access those interrupt enable bits through either CSR7 or CSR16.		R/W

CSR18 (offset=88h), CR – Command Register, bit31 to bit16 automatically recall from EEPROM.

31	D3CS	D3 Cold Support , mapped to CR48<31>	1 from EEPROM	R/W
30-28	AUXCL	AUX. CURRENT LOAD: These three bits report the maximum 3.3Vaux current requirements for the network function, including the 78Q8411 and PHY. If bit 31 of PMR0 is '1', then the default value in EEPROM indicates the current requirements. Typical value is 100b, indicating it needs 220mA to support remote wake-up in D3cold power state. Otherwise, default value is 000, indicating the 78Q8411 does not support remote wake-up from D3cold state. Current requirements are decoded as the following: 111 375 mA 110 320 mA 101 270 mA 100 220 mA 011 160 mA 010 100 mA 001 55 mA 000 0 (self powered)	100b from EEPROM Or 000b	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR18 (offset=88h), CR – Command Register, bit31 to bit16 automatically recall from EEPROM. (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
27-23		Reserved		
22, 21	RFS	RECEIVE FIFO SIZE CONTROL 11: 1K 10: 2K 01,00: Reserved	10 from EEPROM	R/W
20	CRD	CLOCK RUN (CLKRUN pin) DISABLE: 1: disables the function of clock run support for CardBus.	1 from EEPROM	R/W
19	PM	POWER MANAGEMENT: This bit enables the 78Q8411 to activate the Power Management capabilities. When this bit is set into “0” the 78Q8411 will set the CP register (CR13) to zero, indicating no PCI compliant power management capabilities. This bit will be mapped to NC, bit 20 of CR1. In PCI Power Management mode, the Wake-up events include “Wake-up Frame Received”, “Magic Packet™ Received” and “Link Status Changed”, depending on the CSR13 register WCSR settings.	0 from EEPROM	RO
18	WOL	WAKE ON LAN MODE ENABLE: When this bit is set to ‘1’, then the 78Q8411 is set into Wake On LAN mode and enter sleep state. When the 78Q8411 enter sleep state, it won’t wake up until either the Wake Up event occurs, this WOL bit is cleared, or a software (or hardware) reset happens.	0 from EEPROM	R/W
17	LWS	LAN WAKE SIGNAL: Should be 1 to indicate CardBus mode, 0 for PCI.	1 from EEPROM	R/W
16~7	---	Reserved		
6	RWP	RESET WAKE-UP PATTERN DATA REGISTER: POINTER: 0: Normal. 1: Reset.	0	R/W
5	PAUSE	PAUSE: This bit to enables or disables the PAUSE function for flow control. The default value of PAUSE is decided by the result of Auto-Negotiation. Driver can force to enable or disable it after Auto-Negotiation is completed. 0: PAUSE function is disabled. 1: PAUSE function is enabled.	0	R/W
4	RTE	RECEIVE THRESHOLD ENABLE: 1: the receive FIFO threshold is enabled. 0: disable the receive FIFO threshold selection in bit 3~2 of this register, the receive threshold is set to 64-byte.	0	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR18 (offset=88h), CR – Command Register, bit31 to bit16 automatically recall from EEPROM. (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
3~2	DRT	DRAIN RECEIVE THRESHOLD: 00: 32 bytes (8 DW). 01: 64 bytes (16 DW). 10: store-and –forward. 11: Reserved	01	R/W
1	SINT	SOFTWARE INTERRUPT:	0	R/W
0	ATUR	AUTOMATICALLY TRANSMIT-UNDERRUN ENABLE: Set to 1 for automatic recovery.	0	R/W

CSR19 (offset=8ch), PCIC, PCI Bus Performance Counter.

31~16	CLKCNT	CLOCK COUNT: The number of PCI clock from read request asserted until access is completed. This PCI clock number accumulated all the read command cycles from last CSR19 read to current CSR19 read.	0	RO-RC
15~8	---	Reserved		
7~0	DWCNT	DOUBLE WORD COUNT: The number of double words accessed by the last bus master. This double word number is accumulated all the bus master data transactions from last CSR19 read to current CSR19 read.	0	RO-RC

CSR20 (offset=90h), PMCSR, Power Management Command and Status.
(This register value maps from CR49 - PMR1 – Power Management Register 1.)

31~16	---	Reserved		
15	PMES	PME_STATUS: This bit is set when the 78Q8411 would normally assert the PME#/CSTSCHG signal for wakeup event. This bit is independent of the state of the PME-En bit. (bit 8).	0	RO
14,13	DSCAL	DATA_SCALE, indicates the scaling factor to be used when interpreting the value of the Data register. The 78Q8411 doesn't support Data register and Data_Scale.	00b	RO
12~9	DSEL	DATA_SELECT: This four bit field is used to select which data is to be reported through the Data register and Data_Scale field. The 78Q8411 doesn't support Data_Select.	0000b	RO

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR20 (offset=90h), PMCSR, Power Management Command and Status. (The same register value mapping to CR49-PMR1.) (continued)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
8	PME_En	PME_En: "1" enables the 78Q8411 to assert PME#/CSTSCHG. "0" disables the PME#/CSTSCHG assertion. Magic Packet™ default enable : CSR18< WOL bit 18> and CSR18< PM bit 19> set → CSR13< MPRE bit 9> set , then PME#/CSTSCHG asserts regardless of PME_En state. This bit defaults to "0" if the function does not support PME#/CSTSCHG generation from D3cold.	0	RO
7~2	---	Reserved.	000000b	RO
1,0	PWRS	POWER STATE: This two bit field is used both to determine the current power state of the 78Q8411 and to set the 78Q8411 into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus, however the data is discarded an no state change occurs.	00b	RO

CSR21 (offset=94h), WTDP, The Current Working Transmit Descriptor Pointer.

31~0	WTDP	The current working transmit descriptor pointer for driver's double checking or other special purpose.	X	RO

CSR22 (offset=98h), WRDP, The Current Working Receive Descriptor Pointer.

31~0	WRDP	The current working receive descriptor pointer for driver's double checking or other special purpose.	X	RO

CSR23 (offset=9ch), TXBR, Transmit Burst Count/Time-Out.

31~21	---	Reserved		
20~16	TBCNT	TRANSMIT BURST COUNT: After this number of consecutive successful transmit, transmit completed interrupt will be generated. Continuously do this function if no reset.	00000b	R/W
11~0	TTO	TRANSMIT TIME-OUT = (deferred time + back-off time). When the TDIE (bit28 of ACSR7) is set, the timer is decreased in unit of 2.56us(100M) or 25.6us(10M). If the timer expires before another packet transmit begin, then the TDIE interrupt will be generated.	000h	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR24 (offset=A0h), FROM, Flash ROM (Also The Boot ROM) Port.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31	BRA16_ on	This bit is no effect when 3_LED scheme applied 1: no effect to BRA16 0: BRA16 = fd/col LED path driver need to program this bit when 4_LED applied especially when boot rom read.	1	R/W
30~28	---	Reserved		
27	REN	READ ENABLE, clear if read data is ready in DATA, bit7-0 of FROM.	0	R/W
26	WEN	WRITE ENABLE, cleared if write completed	0	R/W
25~8	ADDR	FLASH ROM ADDRESS	0	R/W
7~0	DATA	READ/WRITE DATA of flash ROM	0	R/W

CSR25 (offset=a4h), PAR0, Physical Address Register 0, automatically recall from EEPROM.

31~24	PAB3	PHYSICAL ADDRESS BYTE 3	X	R/W
23~16	PAB2	PHYSICAL ADDRESS BYTE 2	X	R/W
15~8	PAB1	PHYSICAL ADDRESS BYTE 1	X	R/W
7~0	PAB0	PHYSICAL ADDRESS BYTE 0	X	R/W

CSR26 (offset=a8h), PAR1, Physical Address Register 1, automatically recall from EEPROM.

31~24	---	Reserved		
23~16	---	Reserved		
15~8	PAB5	PHYSICAL ADDRESS BYTE 5	X	R/W
7~0	PAB4	PHYSICAL ADDRESS BYTE 4	X	R/W

For example, if physical address = 00-00-e8-11-22-33

PAR0 = 11 e8 00 00

PAR1 = xx xx 33 22

PAR0 and PAR1 are readable, but can be written only if the receive state is in stopped (CSR5 bit19-17=000).

CSR27 (offset=ach), MAR0, Multicast Address Register 0.

31~24	MAB3	MULTICAST ADDRESS BYTE 3 (hash table 31:24)	X	R/W
23~16	MAB2	MULTICAST ADDRESS BYTE 2 (hash table 23:16)	X	R/W
15~8	MAB1	MULTICAST ADDRESS BYTE 1 (hash table 15:8)	X	R/W
7~0	MAB0	MULTICAST ADDRESS BYTE 0 (hash table 7:0)	X	R/W

CONTROL/STATUS REGISTER DESCRIPTION (continued)

CSR28 (offset=b0h), MAR1, Multicast Address Register 1.

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~24	MAB7	MULTICAST ADDRESS BYTE 7 (hash table 63:56)	X	R/W
23~16	MAB6	MULTICAST ADDRESS BYTE 6 (hash table 55:48)	X	R/W
15~8	MAB5	MULTICAST ADDRESS BYTE 5 (hash table 47:40)	X	R/W
7~0	MAB4	MULTICAST ADDRESS BYTE 4 (hash table 39:32)	X	R/W

MAR0 and MAR1 are readable, but can be written only if the receive state is in stopped (CSR5 bits19-17=000).

Function Event Register (Memory Base Offset 100h)

31~16	Reserved	Bits [31:16] are reserved in the PCI Specification.		
15	INTR_EVENT	This bit is used for the interrupt bit. It is set when the Ethernet interrupt source is set, regardless of the mask value. It is cleared when the OS writes 1 to this field and the interrupt source has been serviced. Writing 0 to this field has no effect.	0	RO/LH-W1C
14~5	Reserved	Bits [14:5] are reserved in the PCI Specification.		
4	GWAKE_EVENT	This bit is used for general wake-up. It is set when the Ethernet wake-up source is set, regardless of the mask value. Writing 1 to this field clears this bit and the PME Status bit in the PMCSR. Writing 0 to this field has no effect. Note that writing 1 to the PME Status bit in the PMCSR has the same effect.	0	R/W1C
3~0	Reserved	Bits [3:0] are reserved in the PCI Specification.		

Function Event Mask Register (Memory Base Offset 104h)

31~16	Reserved	Bits [31:16] are reserved in the PCI Specification.		
15	INTR_EN	The bit is the interrupt mask. When this bit equals 0b, it masks the Ethernet function INTA# line but has no effect on the Function Event register. The interrupt mask bit affects the INTA# masking.	1	R/W
14	WKUP_EN	This bit is the wake-up mask. When this bit equals 0b, it masks the Ethernet function PME#/CSTSCHG signal but has no effect on the Function Event register. This bit is dependent on bit 4 of this register.	0	R/W
13~5	Reserved	Bits [13:5] are reserved in the PCI Specification.		
4	GWAKE_EN	This bit is the general wake-up mask. When this bit equals 0b, it masks the Ethernet function wake-up events towards the PME#/CSTSCHG signal. It has no effect on the Function Event register. The 78Q8411 can assert the PME#/CSTSCHG signal in the following configuration of masked bits: wake-up bit AND general wake-up bit, or PME Enable bit in the PMCSR register only.	0	R/W
3~0	Reserved	Bits [3:0] are reserved in the PCI Specification.		

CONTROL/STATUS REGISTER DESCRIPTION (continued)

Function Present State Register (Memory Base Offset 108h)

BIT NO.	NAME	DESCRIPTION	DEFAULT VAL	RW TYPE
31~16	Reserved	Bits [31:16] are reserved in the PCI Specification.		
15	INTR_STATUS	This bit is used for interrupts. It reflects the current state of the Ethernet source of the interrupt regardless of the mask value. It is set when the Ethernet function has a pending interrupt and cleared when the software driver acknowledges all active interrupts through the SCB Command Word.	0	RO
14~5	Reserved	Bits [14:5] are reserved in the PCI Specification.		
4	WAKEUP_STATUS	This bit is used for general wake-up. It reflects the current state of the Ethernet source of CSTSCHG. It is a logical OR result of the gated three most significant bits in the PMDR: Link Status change bit is gated by the Link Status Change Wake Enable bit in the Configuration command. The Magic Packet™ bit is gated by the Magic Packet™ Wake-up disable bit in the Configuration command. The Interesting Packet bit is gated by the programmable filter command.	0	RO
3~0	Reserved	Bits [3:0] are reserved in the PCI Specification.		

Function Force Event Register (Memory Base Offset 10ch)

31~16	Reserved	Bits [31:16] are reserved in the PCI Specification.		
15	INTA_FORCE	This bit is used for interrupts. Writing 1b in this field will set the interrupt bit in the Function Event register. If the INTA# pin is not masked, then it will also be activated. Writing 0b has no effect.	0	W
14~5	Reserved	Bits [14:5] are reserved in the PCI Specification.		
4	GWAKE_FORCE	This bit is used for general wake-up. Writing 1b in this field will set the CSTSCHG bit in the Function Event register. If the CSTSCHG pin is not masked, then it will also be activated. Writing 0b has no effect.	0	W
3~0	Reserved	Bits [3:0] are reserved in the PCI Specification.		

DESCRIPTORS

The 78Q8411 provides receive and transmit descriptors for packet buffering and management.

RECEIVE DESCRIPTOR

Receive Descriptor Table

NAME	bit 31				bit0
RDES0	Own	Status			
RDES1		---	Control	Buffer2 byte-count	Buffer1 byte-count
RDES2	Buffer1 address (DW boundary)				
RDES3	Buffer2 address (DW boundary)				

Descriptors and receive buffers addresses must be longword alignment.

RECEIVE DESCRIPTOR

RDES0

BIT NO.	NAME	DESCRIPTION
31	OWN	OWN BIT: 1: indicate the new receiving data can be put into this descriptor. 0: Host does not move the receiving data out yet.
30-16	FL	Frame length, including CRC. This field is valid only in last descriptor.
15	ES	ERROR SUMMARY, OR of the following bits 0: overflow 1: CRC error 6: late collision 7: frame too long 11: runt packet 14: descriptor error This field is valid only in last descriptor.
14	DE	DESCRIPTOR ERROR. This bit is valid only in last descriptor 1: the current receiving packet is not able to put into the current valid descriptor. This packet is truncated.
13-12	DT	DATA TYPE. 00: normal 01: MAC loop-back 10: Transceiver loop-back 11: remote loop-back These bits are valid only in last descriptor.
11	RF	RUNT FRAME (packet length < 64 bytes). This bit is valid only in last descriptor
10	MF	MULTICAST FRAME. This bit is valid only in last descriptor.
9	FS	FIRST DESCRIPTOR.
8	LS	LAST DESCRIPTOR.

RECEIVE DESCRIPTOR (continued)

RDES0 (continued)

BIT NO.	NAME	DESCRIPTION
7	TL	TOO LONG PACKET (packet length > 1518 bytes). This bit is valid only in last descriptor.
6	CS	LATE COLLISION. Set when collision is active after 64 bytes. This bit is valid only in last descriptor
5	FT	FRAME TYPE. This bit is valid only in last descriptor. 1: Ethernet type 0: 802.3 type
4	RW	RECEIVE WATCHDOG (refer to CSR15, bit 4). This bit is valid only in last descriptor.
3	Reserved	Default = 0
2	DB	DRIBBLE BIT. This bit is valid only in last descriptor. Packet length is not integer multiple of 8-bit.
1	CE	CRC ERROR. This bit is valid only in last descriptor.
0	OF	OVERFLOW. This bit is valid only in last descriptor.

RDES1

31~26	---	Reserved
25	RER	RECEIVE END OF RING indicates this descriptor is last, return to base address of descriptor
24	RCH	SECOND ADDRESS CHAIN Use for chain structure. Indicates the buffer2 address is the next descriptor address. Ring mode takes precedence over chained mode
23~22	---	Reserved
21~11	RBS2	BUFFER 2 SIZE (DW boundary)
10~ 0	RBS1	BUFFER 1 SIZE (DW boundary)

RDES2

31~0	RBA1	RECEIVE BUFFER ADDRESS 1. This buffer address should be double word aligned.

RDES3

31~0	RBA2	RECEIVE BUFFER ADDRESS 2. This buffer address should be double word aligned.

TRANSMIT DESCRIPTOR

TRANSMIT DESCRIPTOR TABLE

NAME	bit31			bit0
TDES0	Own	Status		
TDES1	Control	Buffer2 byte-count	Buffer1 byte-count	
TDES2	Buffer1 address			
TDES3	Buffer2 address			

Descriptor addresses must be longword alignment

TDES0

BIT NO.	NAME	DESCRIPTION
31	OWN	Own bit 1: Indicate this descriptor is ready to transmit 0: Old data not for transmission
30-24	---	Reserved
23-22	UR	UNDER-RUN COUNT
21-16	---	Reserved
15	ES	ERROR SUMMARY, OR of the following bit 1: under-run error 8: excessive collision 9: late collision 10: no carrier 11: loss carrier 14: jabber time-out
14	TO	TRANSMIT JABBER TIME-OUT
13-12	-----	Reserved
11	LO	LOSS CARRIER
10	NC	NO CARRIER
9	LC	LATE COLLISION
8	EC	EXCESSIVE COLLISION
7	HF	HEARTBEAT FAIL
6-3	CC	COLLISION COUNT
2	-----	Reserved
1	UF	UNDER-RUN ERROR
0	DE	Deferred

TRANSMIT DESCRIPTOR (continued)

TDES1

BIT NO.	NAME	DESCRIPTION
31	IC	INTERRUPT COMPLETED
30	LS	LAST DESCRIPTOR
29	FS	FIRST DESCRIPTOR
28,27	---	Reserved
26	AC	DISABLE ADD CRC FUNCTION
25	TER	END OF RING
24	TCH	2ND ADDRESS CHAIN Indicate the buffer2 address is the next descriptor address
23	DPD	DISABLE PADDING FUNCTION
22	---	Reserved
21-11	TBS2	Buffer 2 size
10-0	TBS1	Buffer 1 size

TDES2

31~0	BA1	BUFFER ADDRESS 1. Without any limitation on the transmission buffer address.

TDES3

31~0	BA2	BUFFER ADDRESS 2. Without any limitation on the transmission buffer address.

DESCRIPTOR STRUCTURE TYPES

For networking operation, the 78Q8411 transmits the data packet from transmit buffers in host memory to 78Q8411 transmit FIFO and receives the data packet from 78Q8411 receive FIFO to receive buffers in host memory. The descriptors that the 78Q8411 supports to build in host memory are used as the pointers of these transmit and receive buffers.

There are two structure types for the descriptor, Ring and Chain, supported by the 78Q8411 and are shown as below. The type selection are controlled by the bit24 of RDES1 and the bit24 of TDES1.

The transmit and receive buffers are physically built in host memory. Any buffer can contain either a whole packet or just part of a packet. But it can't contain more than one packet.

Ring Structure: There are two buffers per descriptor in the ring structure. This supports receive early interrupt.

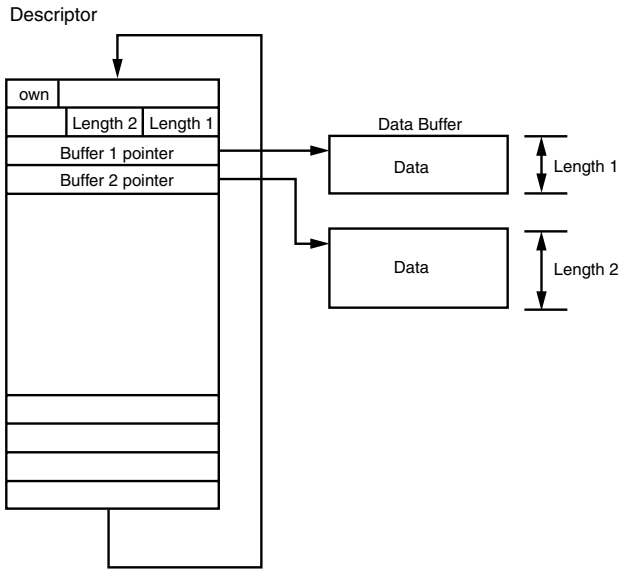


FIGURE1: Ring Structure of Frame Buffer

Chain Structure: There is only one buffer per descriptor in chain structure.

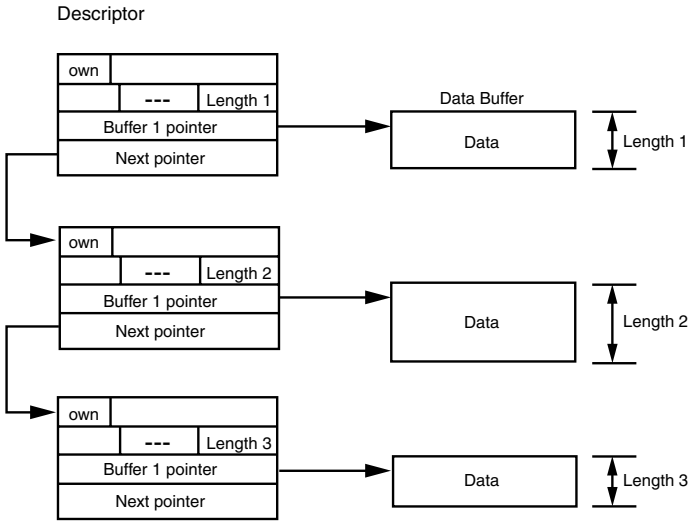


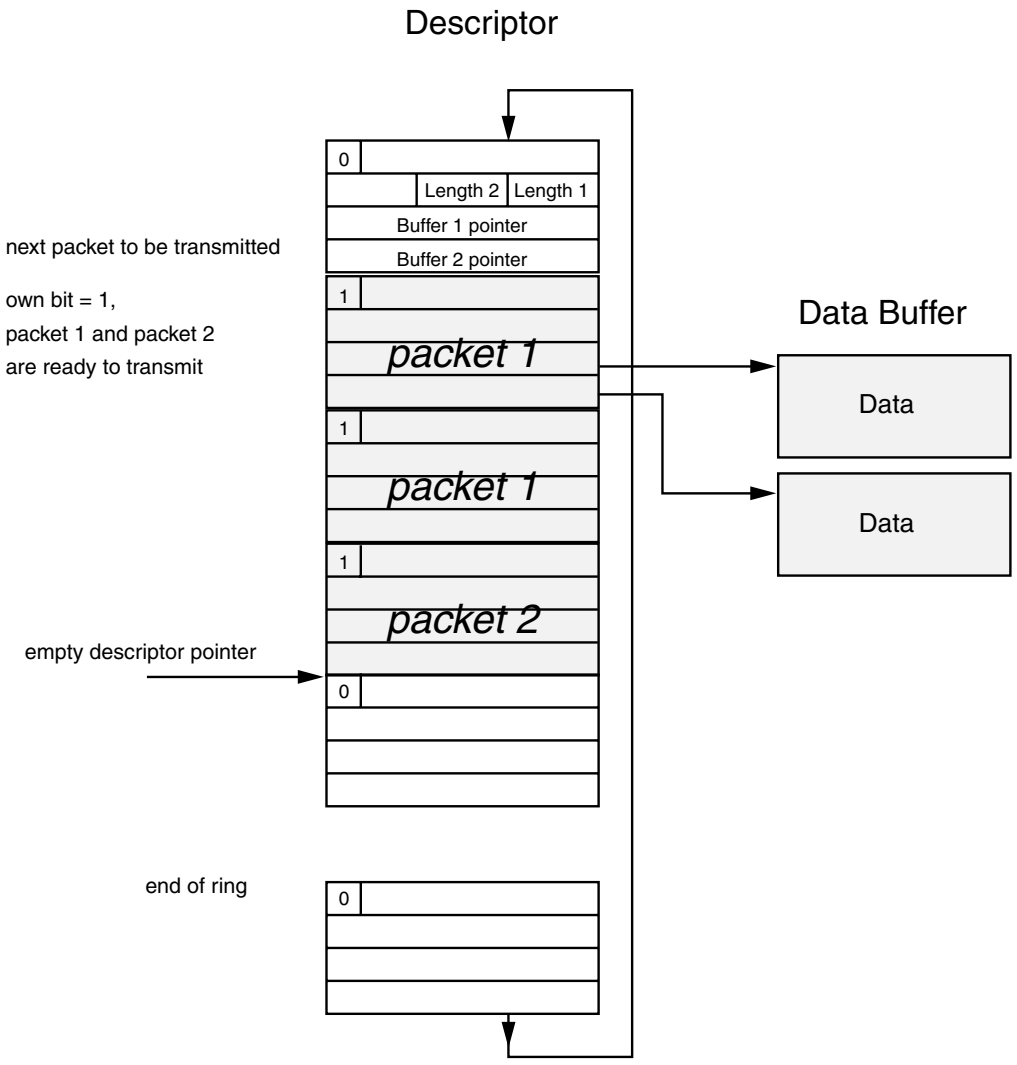
FIGURE 2: Chain Structure of Frame Buffer

DESCRIPTOR MANAGEMENT

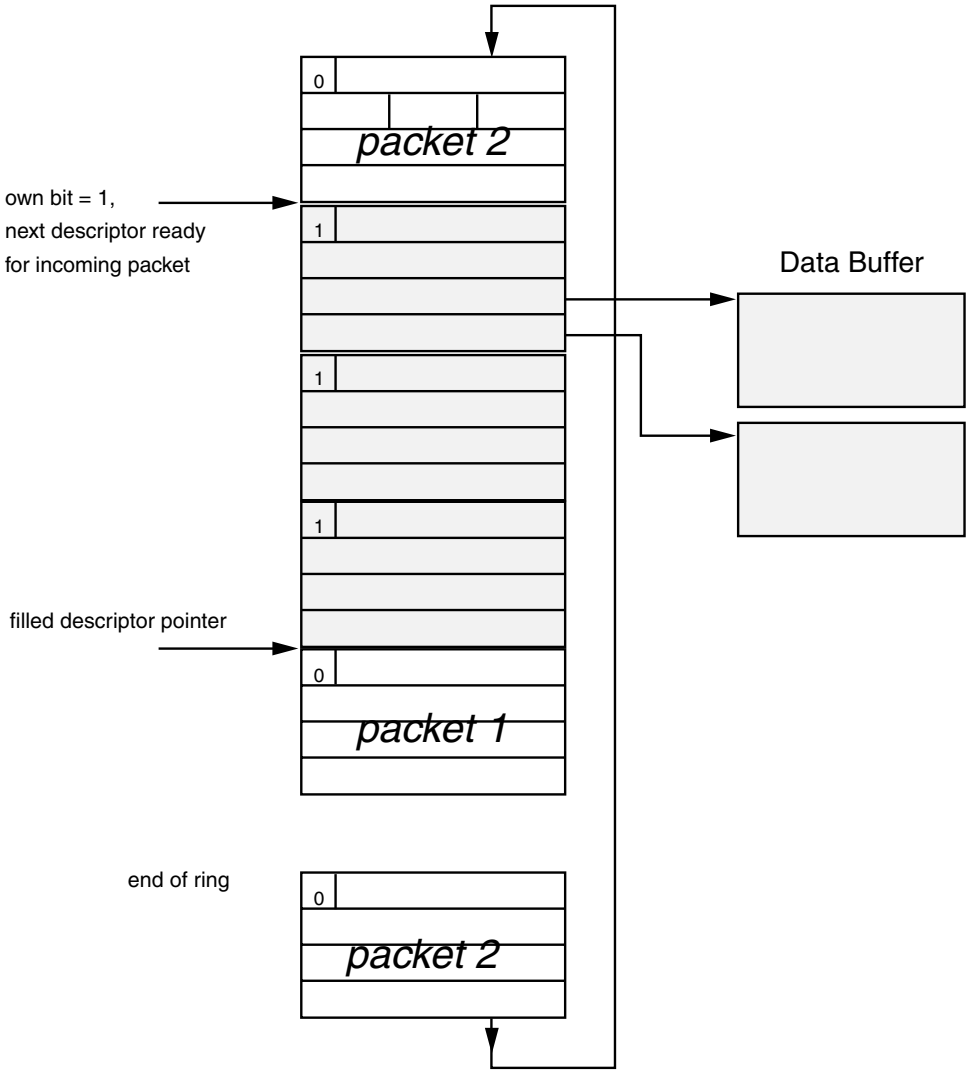
OWN bit = 1, ready for network side access.

OWN bit = 0, ready for host side access.

TRANSMIT DESCRIPTOR POINTERS



RECEIVE DESCRIPTOR POINTERS



MAC OPERATION

In the MAC (Media Access Control) portion of 78Q8411, it incorporates the essential protocol requirements for operating as an IEEE802.3 and Ethernet compliant node.

FORMAT

FIELD	DESCRIPTION
Preamble	A 7-byte field of (10101010b)
Start Frame Delimiter	A 1-byte field of (10101011b)
Destination Address	A 6-byte field
Source Address	A 6-byte field
Length/Type	A 2-byte field indicated the frame is in IEEE802.3 format or Ethernet format. IEEE802.3 format: 0000H ~ 05DCH for Length field Ethernet format: 05DD ~ FFFFH for Type field
Data	*46 ~ 1500 bytes of data information
CRC	A 32-bit cyclic redundant code for error detection

*Note: If padding is disabled (TDES1 bit23), the data field may be shorter than 46 bytes.

TRANSMIT DATA ENCAPSULATION

The differences between the encapsulation and a MAC frame while operating in the 100BASE-TX mode are listed as follow:

1. The first byte of the preamble is replaced by the JK code according to the IEE802.3u, clause 24.
2. After the CRC field of the MAC frame, the 78Q8411 insert the TR code according to the IEE802.3u, clause 24.

RECEIVE DATA DECAPSULATION

When operate in 100BASE-TX mode the 78Q8411 detects a JK code for a preamble as well as a TR code for the packet end. If a JK code is not detected, the 78Q8411 will abort this frame receiving and wait for a new JK code detection. If a TR code is not detected, the 78Q8411 will report a CRC error.

DEFERRING

The Inter-Frame Gap (IFG) time is divided into two parts:

1. IFG1 time (64-bit time): If a carrier is detected on the medium during this time, the 78Q8411 will reset the IFG1 time counter and restart to monitor the channel for an idle again.

2. IFG2 time (32-bit time): After counting the IFG2 time the 78Q8411 will access the channel even though a carrier has been sensed on the network.

COLLISION HANDLING

The scheduling of re-transmissions are determined by a controlled randomization process called “truncated binary exponential back-off”. At the end of enforcing a collision (jamming), the 78Q8411 delays before attempting to re-transmit the packet. The delay is an integer multiple of the slot time. The number of slot times delays before the nth re-transmission attempt is chosen as a uniform distributed integer r in the range:

$$0 \leqq r < 2^k \quad \text{where} \quad k = \min(n, 10)$$

FLOW CONTROL IN FULL DUPLEX APPLICATION

The PAUSE function operation is used to inhibit transmission of data frames for a specified period of time. The 78Q8411 supports full duplex protocol of IEEE802.3x. To support PAUSE function, the 78Q8411 implements the MAC Control Sub-layer functions to decode the MAC Control frames received from MAC control clients and execute the relative requests accordingly. When the Full Duplex mode and PAUSE function are selected after Auto-Negotiation completed (refer the register of XCVR configuration information of XR8), then the 78Q8411 enables the PAUSE function for flow control of full duplex application. In this section we will describe how the 78Q8411 implements the PAUSE function.

MAC Control Frame and PAUSE Frame

6 Octets	Destination Address
6 Octets	Source Address
2 Octets	Length/Type = 88-08h
2 Octets	MAC Control Opcode
	MAC Control Parameter
(minFrameSize - 160) / 8 Octets	Reserved (pads with zeroes)

FIGURE 4 MAC CONTROL FRAME FORMAT

The MAC Control frame is distinguished from other MAC frames only by their Length/Type field identifier. The MAC Control Opcode defined in MAC Control Frame format for PAUSE function is 0001h. Besides, the PAUSE time is specified in the MAC Control Parameters field with 2 Octets, unsigned integer, in the units of Slot-Times. The range of possible PAUSE time is 0 to 65535 Slot-Times.

So, a valid PAUSE frame issued by a MAC control client(could be a switch or a bridge) will contain:

The destination address is set equal to the globally assigned 48 bit multicast address 01-80-C2-00-00-01, or equal to the unicast address which the MAC control client wishes to inhibit its transmission of data frames.

1. Filled the MAC Control Opcode field with 0001h.

2 Octets of PAUSE time specified in the MAC Control parameter field to indicate the length of time for which the destination is wished to inhibit data frame transmission.

Receive Operation for PAUSE Function

Upon reception of a valid MAC Control frame, the 78Q8411 will start a timer for the length of time specified by the MAC Control Parameters field. When the timer value reaches zero then the 78Q8411 ends PAUSE state. However, a PAUSE frame should not affect the transmission of a frame that has been submitted to the MAC(started Transmit out of the MAC and can't be interrupted). On the other hand, the 78Q8411 shall not begin to transmit a frame more than one Slot-Times after received a valid PAUSE frame with a non-zero PAUSE time. If the 78Q8411 receives a PAUSE frame with a zero PAUSE time value, then the 78Q8411 ends the PAUSE state immediately.

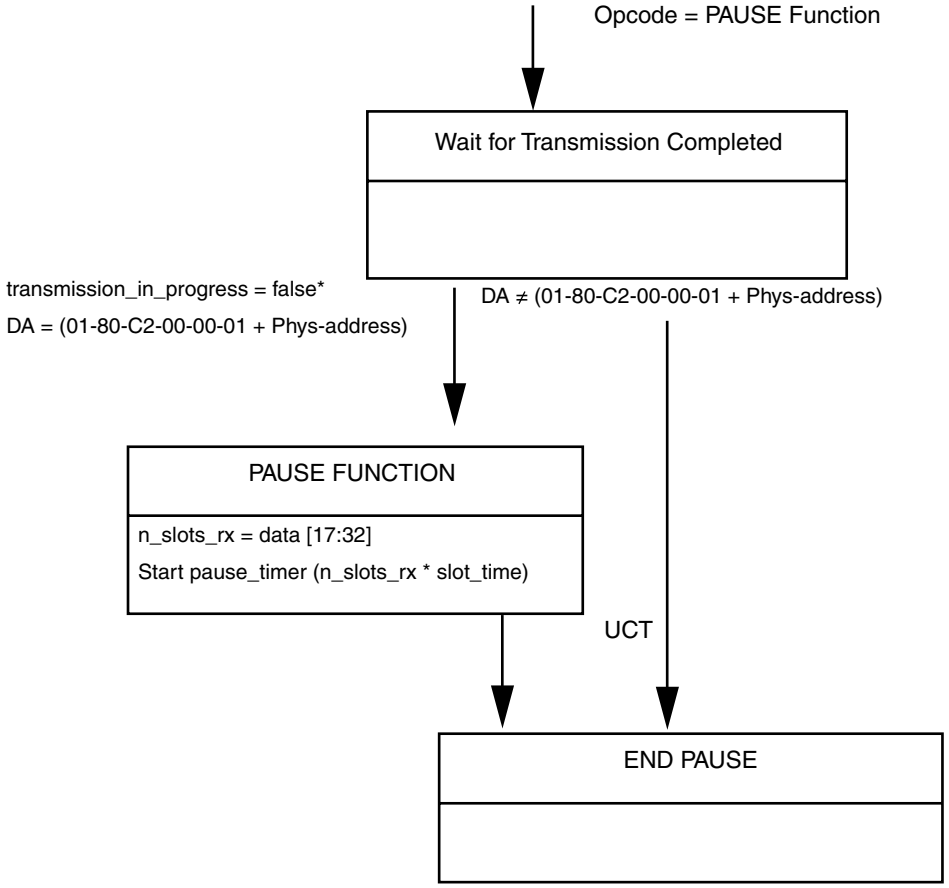


FIGURE 5: Pause Operation Receive State Diagram

RESET

There are two ways to reset the 78Q8411. First, hardware reset, the 78Q8411 can be reset via RST# pin. For ensuring proper reset operation, at least 100μs active Reset input signal is required. Second, software reset, when bit 0 of CSR0 register is set to 1, the 78Q8411 will reset entire circuits and register to default value then clear the bit 0 of CSR0 to 0.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond these limits may permanently damage the device.

PARAMETER	RATING
Supply Voltage	0.5V to 4.3 V
Storage Temperature	-65 to 150° C
Pin Voltage (PCI / CardBus interface pins)	-0.3 to (Vcc+1.5) VDC
Pin Voltage, all other pins	-0.3 to (VCC+0.3) VDC
Pin Current	±100 mA

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges:

DC Voltage Supply, Vcc	3.3 V ± 0.3 VDC
Ambient Operating Temperature, Ta	0 - 70°C

DC SPECIFICATIONS

GENERAL DC SPECIFICATIONS

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Icc	Power Supply				150	mA

PCI / CARDBUS INTERFACE DC SPECIFICATIONS

Vilp	Input LOW Voltage		-0.5		0.325Vcc	V
Vihp	Input HIGH Voltage		0.475Vcc		Vcc+0.5	V
Iilp	Input Leakage Current	0<Vin <Vcc	-10		+10	uA
Volp	Output LOW Voltage	Iout=700uA			0.1Vcc	V
Vohp	Output HIGH Voltage	Iout=-150uA	0.9Vcc			V
Cinp	Input Pin Capacitance		5		17	pF
Cclkp	CLK Pin Capacitance		10		22	pF

FLASH/EEPROM INTERFACE DC SPECIFICATIONS

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Vilf	Input LOW Voltage		0		Vcc x 0.3	V
Vihf	Input HIGH Voltage		Vcc x 0.7		Vcc + 1	V
Iif	Input Leakage Current		-10		10	uA
Volf	Output LOW Voltage				0.2	V
Vohf	Output HIGH Voltage		Vcc – 0.2			V
Cinf	Input Pin Capacitance				10	pF

AC SPECIFICATIONS

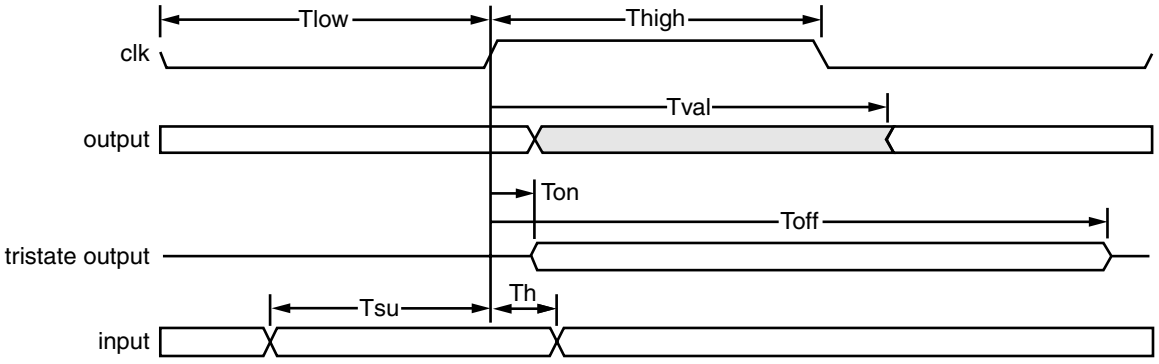
PCI / CARDBUS SIGNALING AC SPECIFICATIONS FOR 3.3V

Ioh(AC)	Switching Current High			4		mA
Iol(AC)	Switching Current Low			6		mA
	Slew Rate		0.25		1	V/ns
Icl	Low Clamp Current					mA
Tr	Unloaded Output Rise Time	0.2Vcc~0.6Vcc	1		4	V/ns
Tf	Unloaded Output Fall Time	0.6Vcc~0.2Vcc	1		4	V/ns

TIMING SPECIFICATIONS

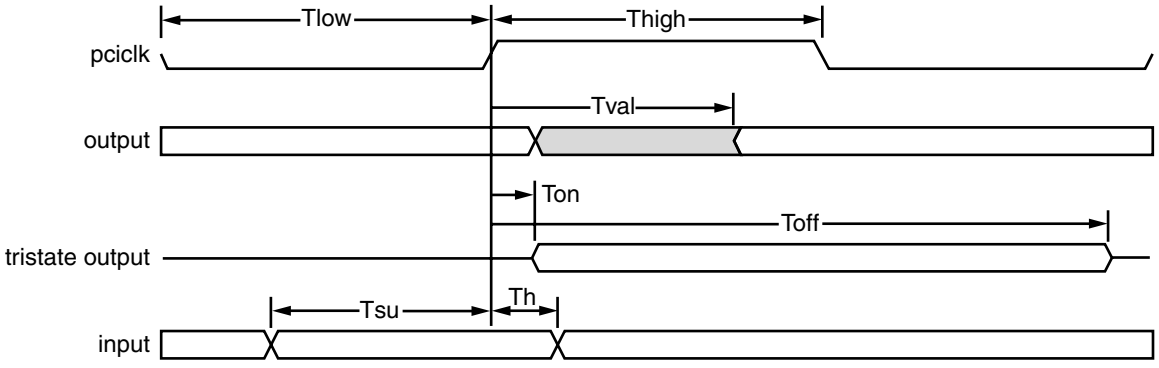
CARDBUS SPECIFICATIONS

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
	Clock Cycle Time		30			ns
Thigh	Clock High Time		12			ns
Tlow	Clock Low Time		12			ns
Tval	access time – bused signals		2		18	ns
Ton	Float to Active Delay		2			ns
Toff	Active to Float Delay				28	ns
Tsu	Input Set up Time to Clock – bused signals		7			ns
Th	Input Hold Time from Clock		0			ns



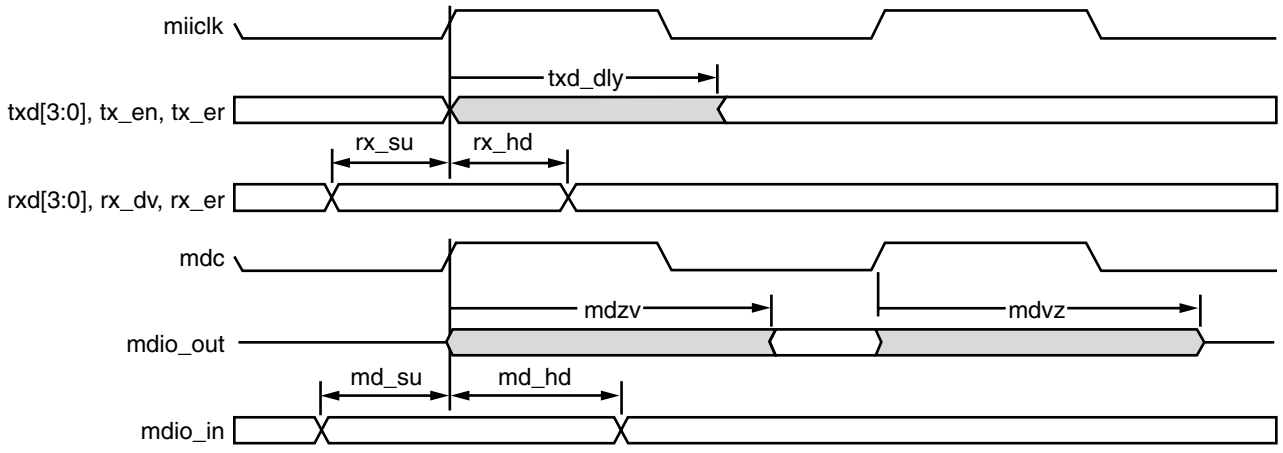
PCI BUS SPECIFICATIONS

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Tval	access time – bused signals		2		11	ns
Ton	Float to Active Delay		2			ns
Toff	Active to Float Delay				28	ns
Tsu	Input Set up Time to Clock – bused signals		10			ns
Th	Input Hold Time from Clock		0			ns
T_cyc	Clock Cycle Time		30			ns
T_high	Clock High Time		12			ns
T_low	Clock Low Time		12			ns
Trst	Reset Active Time after Power Stable		1			ms
Trst-clk	Reset Active Time after CLK Stable		100			us
Trst-off	Reset Active to Output Float delay				40	ns



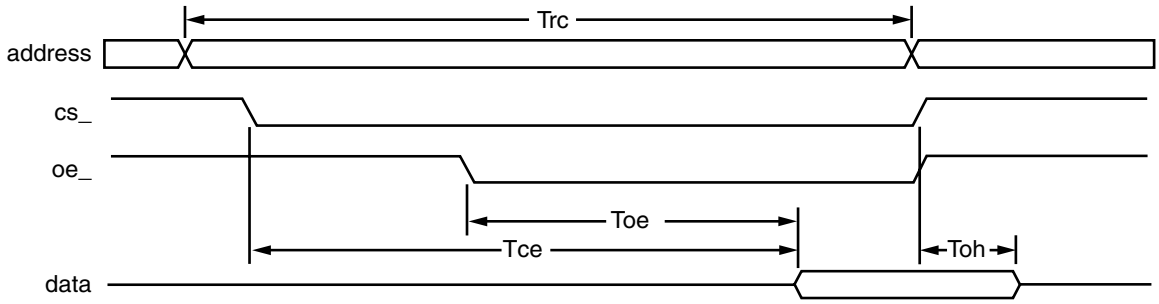
MII TIMING

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
txd_dly	MII Output Data Relay		0		25	ns
rx_su	MII RD Data Set Up Time		10			ns
rx_hd	MII Read Data Hold Time		10			ns
mdzv	MII Data High Z To Valid		0		30	ns
md_su	MDIO Input Setup Time		10			ns
md_hd	MDIO Input Hold Time		10			ns



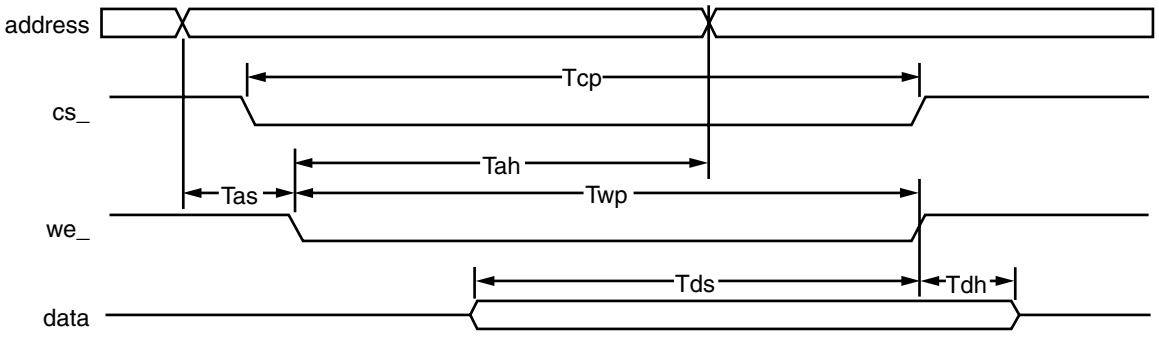
FLASH READ TIMING

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Trc	Read Cycle Time		90			ns
Tce	Chip Enable Access Time				90	ns
Toe	Output Enable Access Time				45	ns
Toh	Output Hold From Address Change		0			ns



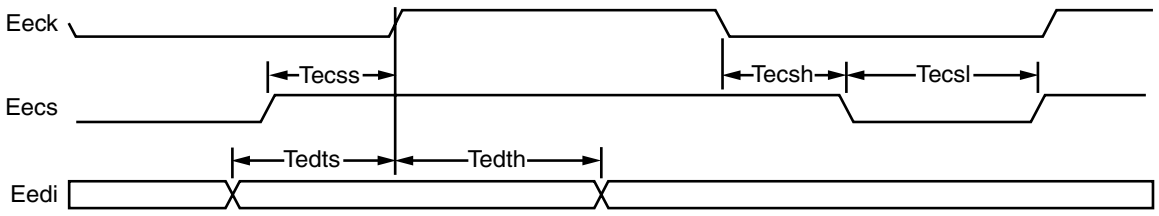
FLASH WRITE TIMING

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Tas	Address Setup Time		0			ns
Tah	Address Hold Time		50			ns
Tds	Data Setup Time		50			ns
Tdh	Data Hold Time		10			ns
Twp	WE Pulse Width		70			ns
Tcp	CE Pulse Width		70			ns

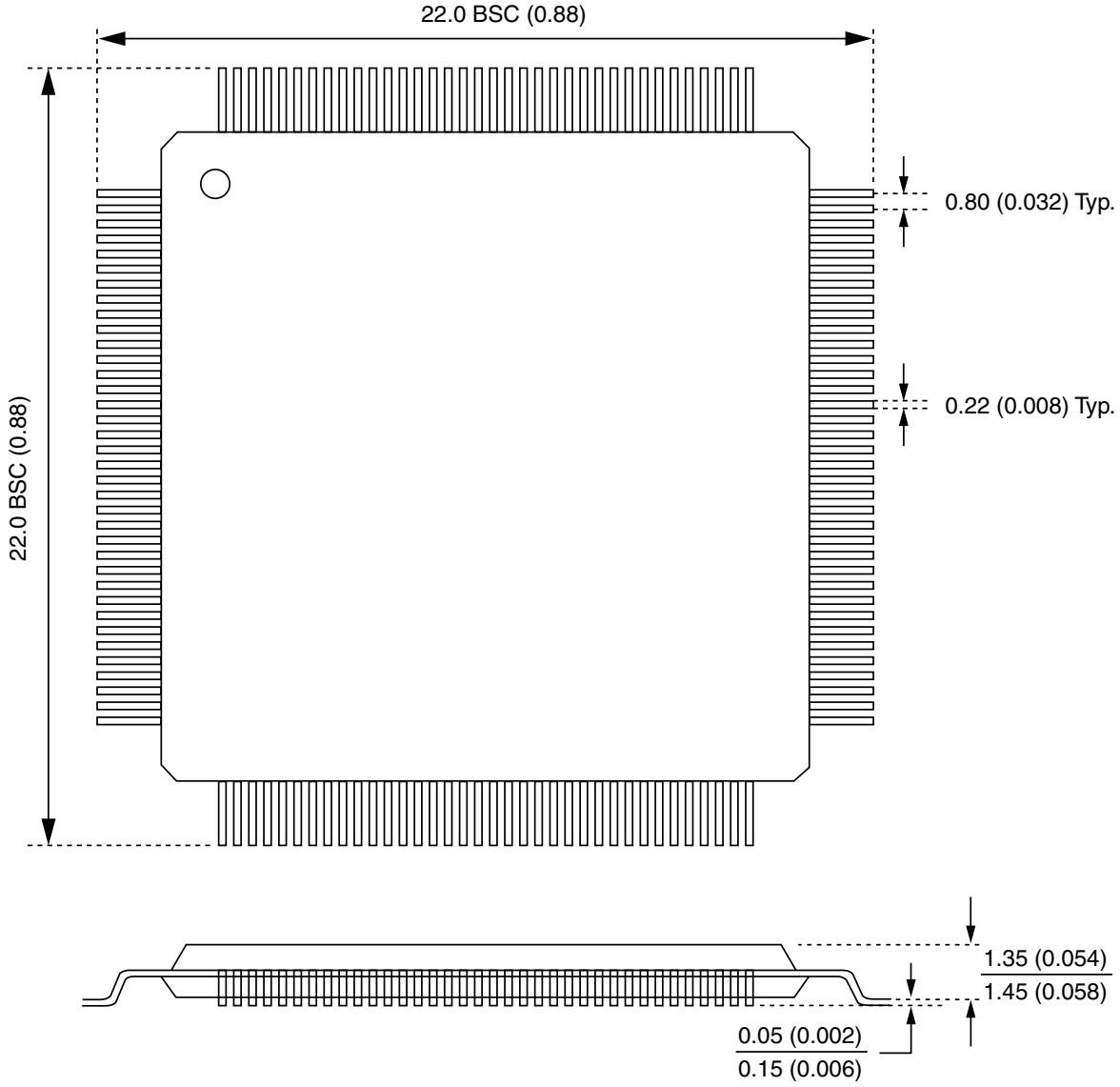


EEPROM INTERFACE TIMING

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNIT
Tscf	Serial Clock Frequency				1M	Hz
Tecss	Delay from CS High to SK High		50			ns
Tecsh	Delay from SK Low to CS Low		0			ns
Tedts	Setup Time of DI to SK		100			ns
Tedth	Hold Time of DI after SK		250			ns
Tecsl	CS Low Time		250			ns



MECHANICAL SPECIFICATIONS

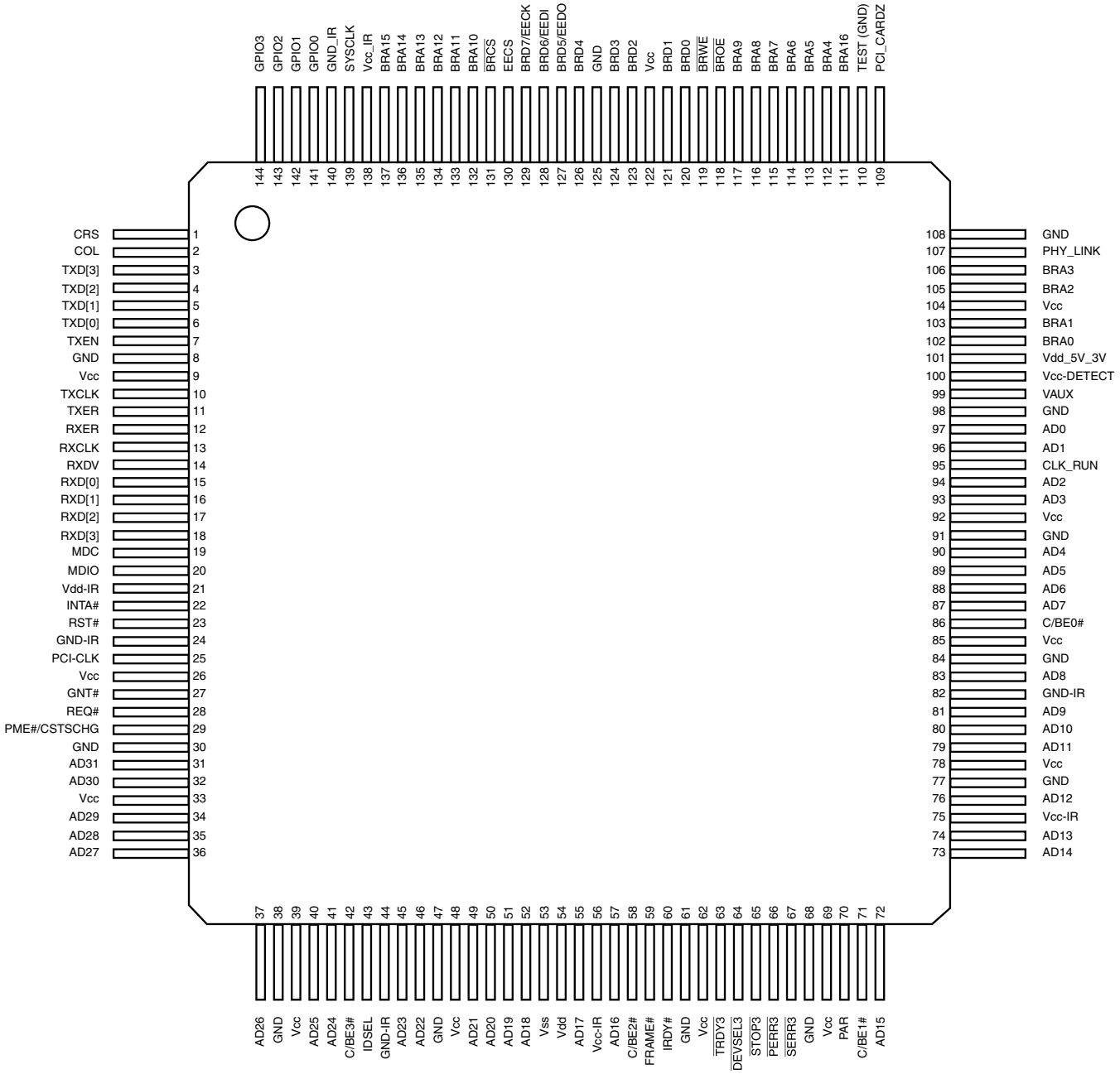


144-Lead TQFP (JEDEC LQFP)

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



144-Lead TQFP (JEDEC LQFP)
78Q8411-CGT

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
78Q8411 144-Lead Thin Quad Flatpack	78Q8411-CGT	78Q8411-CGT

TARGET SPECIFICATION: The attached Target Specification data sheet is to be approved for Beta Site and advanced customer information purposes only. It is not intended to replace the electrical specification for the specific device it represents. This document will be updated and converted into a Preliminary Data Sheet upon completion of Design Engineering Validation. Design Engineering should review this documentation for its accuracy to the definition and the design goals for the product it represents.

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