CMPEN 417 - FPGA Design
Spring 2021
Lab 1
DUE: Friday, January 29th, 11:59pm, on Canvas.

Description

In this lab you will create a MACC (Multiply Accumulate) accelerator and use static timing analysis to view the relative performance of your accelerator. The MAC operation is defined as

result = result+a*b.

Feel free to ask questions on Piazza. Your unit will take as inputs two 32-bit numbers, an accumulated signal which is enabled when high (1). Your unit should also reset the result to 0 when rst signal is high(1). The output will be a 64-bit number. You may ignore any overflow conditions.

The start code can be accessed here.
https://www.edaplayground.com/x/i2wr

Limitations:

However arbitrary, you are not allowed to use behavioral verilog in your accelerator. (i.e. no c = a*b, or c = a+b, etc.). Any function you make must be composed of logic primitives (AND, NAND, OR, NOR, XOR, etc..). **Note: The only statements banned are the addition and multiplication.**

Top Level Module Definition:

Your top level module must include **AT-LEAST** the following ports. Any extra you add may be worth bonus points, however additional will require an explanation of why they were added and how to interface with them.

```
/*
psu_id: abc123
*/
module macc_417
(
    input clk,
    input rst,
    input [31:0] a,
    input [31:0] b,
    input accumulate_enable,
    output [63:0] result
);
/* TODO INSERT YOUR HDL HERE */
endmodule
/* Any sub-modules may be declared and implemented here */
```

Final Submission Format

Your final submission will be through canvas. Your verilog file must have the name top.v. The submission document on canvas should include

1. top.v
2. Your EDA playground link
3. A screenshot of your waveform
4. A short description of what each person did to contribute to the lab

Only one group member needs to submit on Canvas.