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Direct roll transfer printed silicon nanoribbon arrays based high-performance flexible electronics

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Transfer printing of high mobility inorganic nanostructures, using an elastomeric transfer stamp, is a potential route for high-performance printed electronics. Using this method to transfer nanostructures with high yield, uniformity and excellent registration over large area remain a challenge. Herein, we present the 'direct roll transfer' as a single-step process, i.e., without using any elastomeric stamp, to print nanoribbons (NRs) on different substrates with excellent registration (retaining spacing, orientation, etc.) and transfer yield (~95%). The silicon NR based field-effect transistors printed using direct roll transfer consistently show high performance i.e., high on-state current (Ion) >1 mA, high mobility (μ_{eff}) >600 cm^2/Vs, high on/off ratio ($I_{on}/_{off}$) of around 10^6, and low hysteresis (<0.4 V). The developed versatile and transformative method can also print nanostructures based on other materials such as GaAs and thus could pave the way for direct printing of high-performance electronics on large-area flexible substrates.

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INTRODUCTION

Advances in flexible large-area electronics (LAE) have enabled novel applications across numerous areas including wearable systems, soft robotics, bendable displays, and healthcare[1–5]. This will also have an impact on the development of the Internet of Things (IoT) concept where smart objects are required to be aware of and interact with the environment[6]. Conformability of electronic devices to different shapes is indispensable for the above applications[7–13]. Further, fast computing and communication needed in many of these applications to enable myriad human-machine interactions with low latency also call for high performance of the devices. As a result, significant research efforts are being made to manufacture electronic devices and circuits with flexible form factors and high performance. For example, taking advantage of the high-performance Si technology, ultra-thin chips (UTCs) have been developed for system-in foil applications[14,15]. However, due to economic reasons and integration-related difficulties their use is limited to areas requiring compact electronics. The heterogeneous integration of advanced nanomaterials/nanostructures through printing is another manufacturing route that can bring innovations in high-performance flexible electronics[7,16–21].

Among various printing technologies, transfer printing has shown good potential for realizing high-performance flexible electronic devices and circuits[7,22] with silicon and compound semiconductor material-based nanostructures (NSs) such as micro-/nano-membranes (NMs), nanoribbons (NRs), nanowires (NWs), etc. as building blocks. In a conventional transfer printing process, the NSs are picked up from their growth/fabrication rigid substrates using soft polymeric stamps, usually made of Poly-dimethylsiloxane (PDMS), and then printed onto flexible substrates to obtain the electronic devices and circuits[22,23]. The controllable and reproducible transfer of NSs from the donor to the receiver substrate is critical for LAE, and hence a precise control over the interface properties (stamp/donor and stamp/receiver) is required during transfer printing. It is challenging to have complete control over printing parameters (e.g., retrieval/pick up velocity, adhesion switchability, stamp surface recovery, etc.) and interface properties and as a result, it is difficult to obtain high yield and reproducibility. This is due to the viscoelastic properties of soft stamps, which may cause unexpected tilt, orientation, and buckling of NSs under applied force during the printing process. Further, it is challenging to print sub-100 nm thick NSs using conventional transfer printing. This is because at such thicknesses the strain energy release rate at the stamp/NS interface decreases with respect to the NS/substrate interface, which leads to lower printing yield[24]. Few attempts have been made to address these challenges with modified transfer printing involving the surface morphology[25,26], interface engineering[27,28], thermal modulation and kinetically controlled velocity[29–31], magnet-controlled[32], and laser-driven method[18], etc. (summarized in Table 1). These modified transfer printing methods improve the yield and reliability of the process and further extend the transfer printing capacities to: (i) selective printing[33], (ii) arbitrary substrate integration[34], and (iii) deterministic assembly of nano to chip-scale structures[17,28,35]. These modified transfer printing methods have shown good potential for flexible electronics, but they also require additional excitation equipment such as laser system, and magnet actuating system, etc. In this regard, it is highly desirable to develop a precise transfer printing process that enables higher transfer yield, excellent registration, and compatibility with R2R printing without adding complex printing equipment[17,36,37].

In this work, we report a simple, cost-effective, yet robust direct roll transfer printing technique and demonstrates its efficacy for high-performance electronics by developing NR-based field-effect transistors (NRFETs). The developed technique has the following distinct advantages: (i) unlike conventional transfer printing, the presented method does not require a PDMS transfer stamp (hence, named as direct transfer printing), which means reduced number of printing steps and hence reduced printing cost and time. Further, it reduces the chance of breakage and/or wrinkling of printed nanostructures and hence helps to preserve their morphology and structure. This also offers an excellent opportunity to enhance the transfer yield and registration of printing nanostructures; (ii) The process helps to achieve high device-to-device uniformity by avoiding contamination from PDMS stamps,

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Table 1. Performance comparison for the conventional and modified transfer printing process with the developed direct troll printing technique.

Transfer printing method	Printing principle	Material/structures printed and dimensions.	Printing process parameters				
			Complexity	Yield	R2R compatibility	Registration accuracy	Ref.
Bending radius controlled	Peeling velocity bending radius	Micro-scale Si plate array (7 μm thick; 760 × 760 μm)	Medium/issue: limited to micro-scale structures	97.4%	No	≈2000 nm	[60]
Adhesion promoter assisted	Using adhesion promoter (VM652)	Si NRs arrays (70 nm thick; 5 μm × 50 μm)	Low/issue: poor registartion quality	N/A	No	≈2000 nm	[7]
Shear-assisted inspired by Gecko	Peeling velocity with angular direction dependent	Micro-scale Si, membranes, plates, etc. Si platelets (3 μm thick, 100 μm × 100 μm)	meduim/issue: low contrast in adhesion switchability)	≈90%	No	<4000 nm	[27]
Surface-relief assisted inspired by Aphid	Changing in contact area from stamp's shape memory effect	Micro-scale Si inks (squares, conical shapes, etc.)	High/issue: adhesion switching and temperature	N/A	No	1000 nm	[61]
Laser-assisted transfer printing	Laser-induced thermal mismatch	Micro-scale Si plates (100 μm × 100 μm × 0.32 μm)	High/issue: temperaturte and require expensive equipment	N/A	No	1000 nm	[62]
Shape memory assisted polymer and laser-assisted	Changing in contact area from stamp memory shape and thermal mismatch	Si nanoribbons 200 nm thick.	High/issue: possible thermal damage, and require expensive equipment	100%	No	N/A	[33]
Direct Roll Prinitng	Adhession-assisted	Si NRs (70 nm thick; 55 μm × 5 μm)	Simple/limited to PI layer	≈90%	Yes	<100 nm	This work

The table also compares the fabricated transistor performance using printed NSs as an active device channel. *N/A* data not available.

and (iii) the process is compatible with R2R fabrication which is advantageous for future LAE manufacturing. The semi-automated direct roll printing system has been used for printing sub-100 nm thick (≈70 nm) Si NR arrays directly on the target flexible receiver substrate using a custom roll system. Using a series of morphological characterizations such as Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM), we demonstrate: (a) near-perfect registration of the printed structures (<0.1 μm), (b) high yield (~95%), (c) residue-free transfer of Si NRs and (d) large area transfer (9 cm^2). The direct transfer printed Si NRs were further processed to obtain NRFETs are accomplished following our recently demonstrated room temperature (RT) fabrication process including a dielectric deposition. The developed NRFETs exhibit excellent electrical properties: average device effective mobility of ~631 cm^2/Vs, and high on/off current ratio ($I_{on}/_{off}$) of around 10^6. The response after cyclic bending tests shows the device having excellent mechanical stability and flexibility. The obtained results are also compared with the Si NRFET devices obtained using conventional transfer printing. The presented results show the significant potential of direct transfer printing as a new route towards high-performance printed LAE.

RESULTS AND DISCUSSIONS

Direct roll transfer printing method

Figure 1 schematically shows the fabrication steps for NRFETs using direct roll printing technology. The printing process is displayed in the supplementary information (Supplementary video M1 and Fig. 1). The details of the processes are given in the experimental section. To draw the comparison, Fig. 1 also illustrates the processing steps for conventional transfer printing. For both printing techniques, silicon NRs are first fabricated on the rigid wafer using a conventional nanofabrication process, as described in our previous works[7]. Briefly, the fabrication process involves anisotropic wet etching of selected exposed regions on the top side of the Si wafer, followed by undercut etching of the buried oxide (Box) using hydrofluoric acid to eventually release Si NRs structures[38–40]. Figure 1a shows the fabrication steps to obtain Si NRs from a commercial silicon-on-insulator (SOI). The SEM image of the fabricated and released NRs is also shown in figure[7]. This method produces horizontal arrays of NRs over SOI source wafers, which are transfer printed onto flexible receiver substrates. The process steps for conventional transfer printing are shown in Fig. 1b. It can be seen from this figure, it is a two-step process where the transfer mechanism can be understood by studying the competing fracture between the stamp/NS interface and the NS/substrate interface[41]. The kinetically controlled conventional transfer printing process has shown poor yield for sub-100 nm thick NRs because of difficulties in controlling the mechanics of viscoelastic PDMS stamp. As a major advance over the traditional processes, direct roll printing addresses the above issue by avoiding the use of PDMS stamp (Fig. 1c) and thus also reducing the complexity of the fabrication process. In this process, the SOI wafer with Si NRs (donor substrate) is brought into direct physical contact with the semi-cured PI thin film over the receiver substrate. A thin layer of partially cured PI is utilized to enhance the adhesion between NRs and receiver substrate during the printing process. As an immediate benefit, the direct roll printing approach leads to lower process steps, reduced complexity, shorter printing time, and lower fabrication cost compared with conventional transfer printing. Following the direct transfer printing of NRs, low-temperature steps (e.g., dielectric and metal deposition) were carried out to realize devices on flexible receiver substrates, as shown in Fig. 1d.

The semi-cured PI layer allows us to perform direct roll printing of NSs with enhanced transfer yield. However, this step could potentially make the printing process slow and pose challenges in

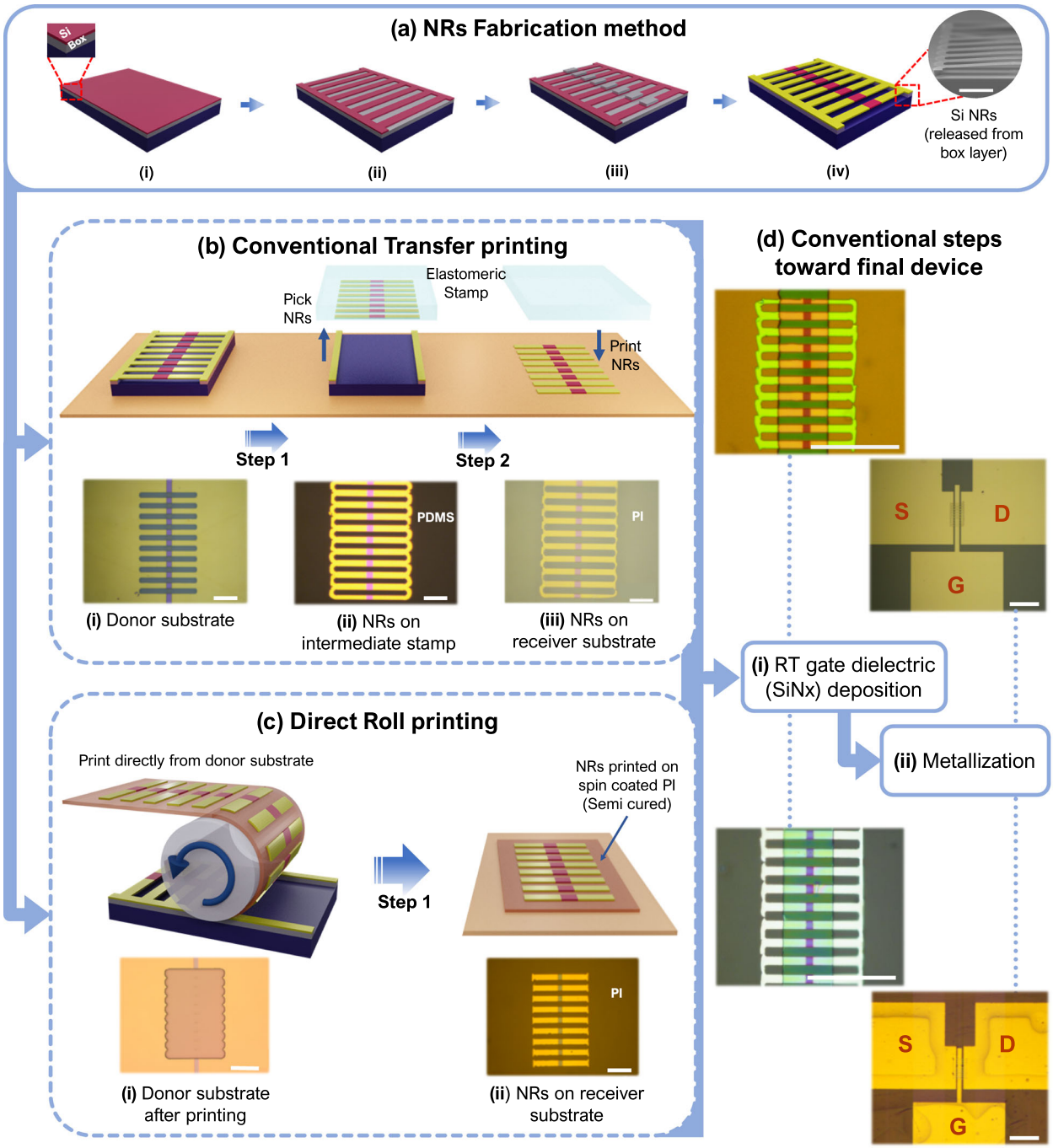

Fig. 1 Schematic illustration of the steps involved in the direct roll printing process with corresponding optical and SEM images. **a** Fabrication step of Si NRs carried out on the donor substrate with n+ selective doping followed by releasing the NRs from buried oxide (Box) layer as shown in SEM cross-sectional image (scale bar, 10 μm). **b** Conventional transfer printing steps using an elastomeric stamp (PDMS) with an optical image of each step (scale bar, 25 μm). **c** Direct roll printing of NRs from donor to the semi-cured PI substrate (scale bar, 25 μm). **d** Conventional microfabrication processing steps toward a final NRFET device (i.e., room temperature dielectric deposition, metallization, etc (scale bar, 100 μm)).

terms of printing over different substrates. This is because, after direct transfer printing, the annealing of the coated PI layer is needed. To investigate this, we have printed Si NRs over various flexible substrates such as metal foils (e.g., Al, Cu, and Mg) and polymers (e.g., Kapton sheet, PET, and PI). The data is shown in Supplementary Fig. 2. Depending on the underlying substrate and its glass transition temperature, the curing time could vary from 2 h (for PI, Kapton, and metal foils) to 4 h (PET). Indeed, 2–4 h of curing makes the printing step slower, but this drawback could be overcome by using UV-cured polymers as an adhesive layer. UV curing can speed up the process[42] and reduce the time duration of the entire printing process.

For high transfer yield in LAE, it is important to have good control over the shape, and geometrical configuration of the printed structures (high registration). To obtain the statistical data on registration, yield and to evaluate the quality of direct roll printed NRs, the morphological analysis was performed using SEM, optical microscopy, and AFM. It is to be noted that this statistical

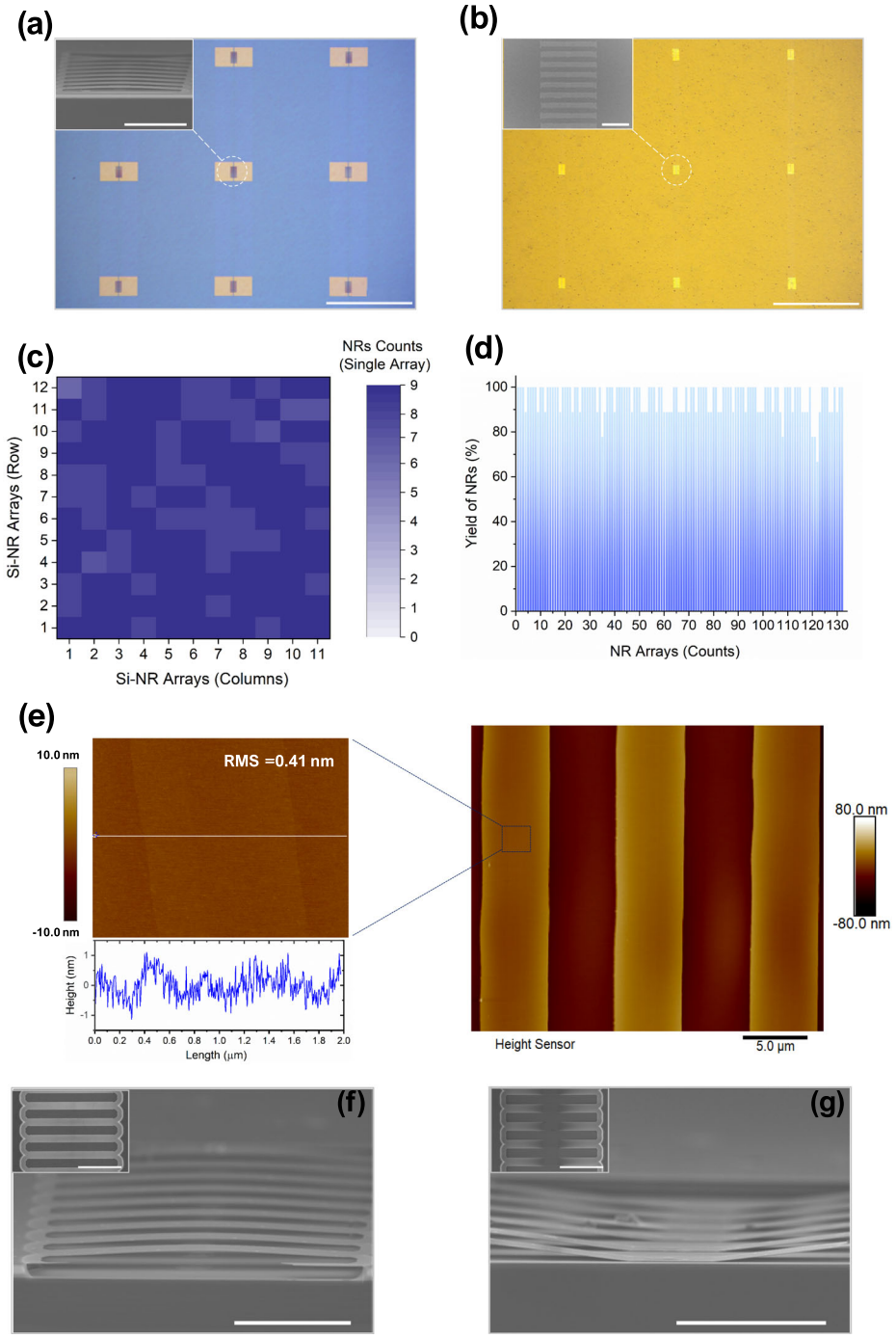

Fig. 2 Morphological analysis of direct roll printed Si NR arrays. Optical images of (**a**) Si NR array on the donor wafer before printing (scale bar, 500 μm) with corresponding SEM image (inset) (scale bar, 25 μm). **b** Transferred Si NR arrays onto flexible receiver substrate (scale bar, 500 μm) with corresponding SEM image (inset) (scale bar, 25 μm). **c**, **d** Study of the yield based on presented direct printing approach (contact area of donor/receiver during direct roll printing ~2.25 cm^2). **e** Atomic force microscopy (AFM) image of the surface of single Si NR (scan size 25 μm × 25 μm) on PI substrate. The figure also shows a high-resolution AFM scan (2 μm × 2 μm) to monitor the roughness of Si NRs. SEM cross-sectional images of anchored Si NR array after etching the Box layer with top view image of the anchor point (inset) (scale bar, 20 μm). **f** Gap anchor point = 55 μm. **g** Gap anchor point >55 μm.

data is obtained for NRs printed over PI substrate. Figure 2 shows the images of released Si NRs, before and after the direct roll printing. Figure 2a shows an optical microscopy image of selectively doped Si NR arrays over donor substrate; the inset shows the magnified SEM image of a single Si NRs array in releasable form, prepared to allow direct retrieval onto the surface of PI substrate. The inset of Fig. 2a shows the suspended NRs are anchored at both edges (5 μm width at both sides and supported by the underlying 2 μm thick of Box layer) to maintain the correct alignment. Figure 2b shows the corresponding optical image of arrays of 70 nm thick Si NRs, directly transferred onto a target PI substrate using direct roll printing. The SEM image in the inset of Fig. 2b illustrates a defect-free transfer of NRs. From fig. 2a, b and supplementary Fig. 3, it is clear that the arrays of Si NRs with perfect registration were transferred over the PI substrate (separated by 930 μm in X-direction and ~990 μm Y-direction).

These registration values perfectly match with the NRs on the donor wafer. A high registration quality of printed structures is critical for the high-performance LAE as poor registration may lead to poor control over device dimensions and hence greater variation in device-to-device performance[17]. The use of a viscoelastic soft stamp in conventional transfer printing may degrade the registration quality of the printed NSs[43,44]. For instance, periodic wavy/buckled structures formed spontaneously with specific amplitudes defined by the moduli of the materials and the thicknesses of the structures. This leads to little control over the geometries or the phases of the waves[45]. This is because of the mechanical properties of soft stamps such as PDMS. We studied this aspect using COMSOL simulations and noted that a 2 N compressive force on the PDMS surface to retrieve the NSs could introduce a lateral displacement of more than 1 µm in PDMS due to the shear strain (Supplementary Fig. 4). This means, during the retrieval step, the release of strain energy may lead to wavy/buckled structures and hence the misalignment of at least 1 µm. This misalignment is significant when we consider printed electronics in large areas. For example, this 1 µm misalignment from on a 1 cm stamp can become 10 µm on a 10 cm long substrate, which is fatal for the realization of electronic circuits on such areas, particularly when the device's dimensions are smaller than the misalignment. If the channel length of a FET device is 1 µm, one can expect huge variations in electrical performance from device to device. Although controlled wavy/buckled structures could be used for the development of small-scale stretchable electronics but for LAE it is likely to lead to poor uniformity in device-to-device performance.

The reliability and robustness of the presented printing approach were evaluated by the transfer yield of NRs from the donor to receiver substrate. High transfer yield (~100%) is desired for any practical application. To have a uniform and high printing yield over a large area, conformal contact between the semi-cured PI layer and Si NRs is needed for a direct roll printing approach. To achieve an excellent conformal contact and thus, the printing yield, dependency of applied force on transfer yield was evaluated. The contact force is one of the critical parameters that affect the final yield of the process. The optimization study with the applied force is shown in (Supplementary Fig. 5), where each single Si NR array consists of 9 NRs, the width and spacing between them are 5 µm, the length and thickness are 50 µm and 70 nm, respectively. The transfer yield results were obtained and characterized based on different applied forces from 2 to 12 N while the printing speed was fixed to 1 mm/s. As shown in this figure, the transfer yield increases with the increase in applied force and reaches 95% for the applied contact force of 12 N (the printed area was 2.25 cm^2 chip). This observation is based on the data from 11 × 12 Si NR arrays. These results can be explained as higher forces lead to more conformal contact of NRs with the semi-cured PI, which in turn enhances the adhesive strength between them. Eventually, this helps to achieve a uniform and high transfer yield. The applied 12 N is close to the max loading capacity of the present roll printing system (load cells, motors). However, with further modifications of our roll printing setup, it would be possible to apply larger forces to further enhance the transfer yield.

It is important to note that the gap between the anchor points is also critical for higher transfer yield. To optimize the gap, we have performed etching of the Box layer for various time durations. The SEM images of the NRs anchored at two ends, with different etching duration of the Box layer, are shown in Fig. 2f, g). We observed that the transfer yield is almost zero when the gap between the anchor point is >55 µm. This is because, for larger gaps between anchor points, the suspended NRs touch the base of the silicon wafer and create a bond with the bulk substrate which eventually leads to broken ribbons or the ones that cannot be retrieved from the source substrate during direct roll printing.

Following the optimization study, large-area printing was performed using SOI donor substrate having a size of 3 × 3 = 9 cm^2 (close to 2-inch wafer size) with an optimized roll printing parameter (12 N force @ 1 mm/s), as illustrated in the (Supplementary Fig. 6). By carefully optimizing the process (shown above), we managed to achieve highly uniform printing with ~95% transfer yield averaged over the printed large area. It is worth mentioning here that the present printing area is restricted only by the size of the roller and not the process itself. By increasing the roller size it will be possible to increase the print area. This marks a significant advantage over the conventional two-step transfer printing process, which usually shows a low printing yield for sub-100 nm thick NSs[24]. This is because the adhesion forces that are considered insignificant at the macro scale become dominant at the micro/nanoscale. As a result, releasing the micro-/nano structures from stamps has been a major challenge for a 'pick-and-place' assembly technique. Thereby, accuracy, yield, and throughput of the printing process are majorly compromised. As shown in Fig. 2a, b, the probability for the misalignment of printed structures during the direct roll printing process is low, as viscoelastic stamps are not involved in this process. By retaining the NRs alignment, the variation in NR density across the substrate and the overlapping of adjacent NRs are reduced, and eventually, the device-to-device uniformity is improved. Further, it leads to a higher transfer yield of the NSs (Fig. 2c, d). Table 1 summarizes these results along with a comparison with the conventional transfer printing process.

Finally, we have evaluated the surface topography of the printed NRs. It is worth mentioning that the use of an intermediate stamp in conventional transfer printing may leave residues on the surface of the NSs due to high bonding strength and strong adhesion between PDMS stamp and native oxide (SiO_2) layer[46,47]. The post-surface treatment is normally needed to remove the residues will also add few extra fabrication steps and increase the process complexity. The removal of PDMS residues typically involves plasma treatment or wet etching which could damage or introduce roughness over the NRs of sub-100 nm thickness. The elastomeric stamp residues (non-conducting material) strongly influence the electrical performance and reliability of nanostructures-based electronics since the interfacial contact between the nanostructures and deposited metal contacts are not desirable. Therefore, there is a possibility of performance degradation in the case of traditional transfer printing. Surface chemistry technique has also been demonstrated by depositing/sputtering thin SiO_2 layer on the top of the target NS to enhance stamp/NS adhesion[48]. Such steps increase complexities in the printing process and produce surface contamination on top of printed NSs, which may subsequently lead to variation in terms of device performance. The surface quality of transferred Si NRs on receiving substrate (PI) was investigated by AFM surface morphology. Figure 2e shows an AFM image (25 µm × 25 µm) of a single Si NR array directly transferred on PI substrate. The surface topography of the printed NRs was found to be free from polymer residues/contamination. Further, the surface roughness of the printed NR was calculated using a high-resolution AFM image (2 µm × 2 µm), as shown in Fig. 2e. The calculated root means square (RMS) roughness of transferred ribbons is 0.41 nm. It can be seen from Fig. 2e that sidewalls of ultrathin NS are formed on PI substrate without any polymer residues, unlike other reported approaches such as glue-assisted transfer printing[25,49,50]. The presence of residues may lead to surface contamination and defects and failures in transferred NSs, eventually degrading the device performance[51].

Direct roll transfer printed Si nanoribbon-based transistors

The direct roll printed Si NRs were used to fabricate the top-gated field-effect transistors (FETs) on the flexible (PI) substrate. The top-gate

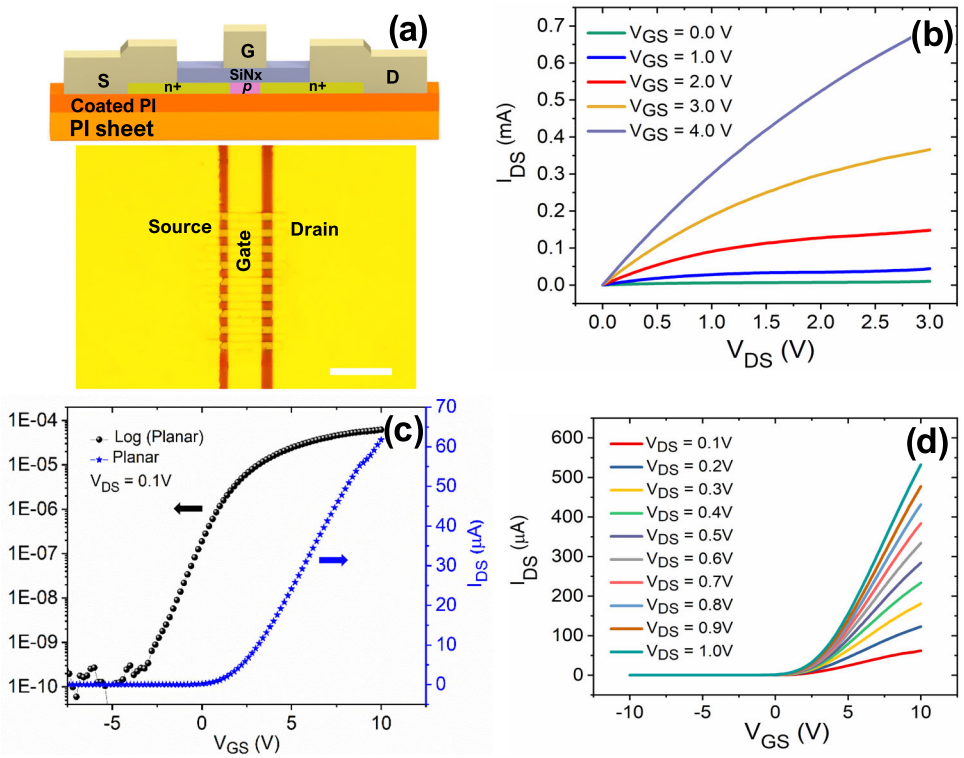

Fig. 3 Electrical characteristics of Si NRFETs. a Schematic cross-sectional view of the Si NRFET device (scale bar, 50 μm). **b** Output characteristics of Si-NRFET. **c** Transfer characteristics (I_{DS}–V_{GS}) of Si NRFET with $V_{DS} = 0.1$ V in logarithmic and linear scales. **d** Transfer characteristics (I_{DS}–V_{GS}) of Si NRFET with V_{DS} varying from 0.1 V to 1 V with the step of 0.1 V.

FET geometry is preferred here because the top-gate electrode could be wrapped around the nanostructure to effectively control the charge transport. The gate dielectric needed for the realization of top-gated FET on flexible substrates can be deposited at room temperature (RT). This gate dielectric, conformally covered over the nanostructure, should have minimal defect density at the semiconductor/dielectric interface and provide a large capacitance per unit area. In this regard, the inductively coupled plasma-chemical vapor deposition (ICP-CVD) technique offers a unique advantage as it allows high-quality dielectric (SiO_x, SiN_x, etc.) deposition at RT without any plasma related harmful effects[7]. We have used RT deposited SiN_x as our top-gate dielectric material as it has been widely explored gate dielectric material for III–V devices and oxide thin-film transistors exhibiting good device performance. Figure 3a shows the schematic and optical images of fabricated top-gated Si NR-FET devices (channel length (L) and width (W) ~5 μm and ~45 μm (9 NRs of 5 μm), respectively) and its transfer and output scans. The cross-section and optical image of the Si-NRFET are shown in Fig. 3a. The output characteristics (V_{DS}–I_{DS}) of Si NR-FET in Fig. 3b show the varying gate bias (V_{GS}) from 0 V to 4 V with the step of 1 V by sweeping drain-source bias (V_{DS}) from −3 V to +3 V (only positive V_{DS} voltages illustrated). As V_{GS} increases towards positive voltage, the corresponding drain current (I_{DS}) is also increased, confirming that the device is n-channel. Due to the n+ doping and low energetic contact barriers, the variation of I_{DS} with V_{DS} is linear without any inflection point at low-V_{DS} region ($V_{DS} \leq$~0.1 V). The transfer characteristics (I_{DS}–V_{GS}) of Si NR-FET with V_{DS} of 0.1 V were obtained by varying V_{GS} from −10 to 10 V (Fig. 3c). In terms of the electrical performance of the NR-FET, the main parameters to consider are: on-state (I_{on}), off-state current (I_{off}), current on/off ratio (I_{on}/I_{off}), and effective mobility (μ_{eff}), and subthreshold slope (SS)[52]. The logarithmic plot of the transfer curve in Fig. 3c revealed an I_{on} (~60 μA)/I_{off} (<0.1 nA) current ratio of $>10^6$ suggesting an excellent gate-channel control. Figure 3d shows the transfer characteristics of Si NRFET at various values of V_{DS}. It is worth noting from Fig. 3d that the threshold voltage (V_{th}) remains constant with applied voltage V_{DS}, indicating high stability charge transport behavior under different voltages. The field-effect mobility of the device was extracted based on the conventional MOSFET model in the linear regime[7] as given by:

$$\mu_{eff} = \frac{L}{W C_{ox}(V_{GS} - V_{th})} \frac{g_d}{} \quad (1)$$

where L and W are the gate length and width of the Si NRFET, respectively, g_d is the drain conductance, C_{ox} is the oxide capacitance, V_{GS} is the gate-source voltage and V_{th} is the threshold voltage. The thickness of the gate is negligible since, the thickness of active NRs is relatively low (~70 nm), the effective width is 45 μm (9 ribbons × 5 μm each). The threshold voltage (V_{th}) measured through extrapolation in the linear region of Si NRFET is ~0.4 V. The drain conductance g_d is extracted using the following equation:

$$g_d = \frac{\partial I_D}{\partial V_{DS}} | V_{GS} = \text{Constant} \quad (2)$$

The drain conductance was estimated from the output characteristics, at $V_{DS} = 30$ mV. The estimated drain conductance extracted by numerically differentiating the drain current with reference to the drain-source voltage under planar condition is 47 μS. Similarly, from transfer characteristics, the peak transconductance was estimated by using the following expression:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} | V_{DS} = \text{Constant} \quad (3)$$

The extracted effective mobility (μ_{eff}) is ~631 cm^2/Vs. The subthreshold slope (SS) was extracted from the logarithmic transfer characteristics by numerical differentiation based on the equation:

$$SS = \frac{1}{\partial \log(I_D)/\partial V_{GS}} \quad (4)$$

Table 2. The table compares the fabricated transistor performance using printed NSs as an active device channel.

S.No.	Transfer printing method	Si Micro/nano-structure morphology	Source wafer	Threshold voltage (V)	Subthreshold slope (mV/decades)	Mobility (cm^2/Vs)	On/off ratio	Ref.
1	Kinetically controlled transfer printing	Si membrane (300 nm thick)	SOI	~1.1 ± 0.05 V	120	680	10^7	54
2	Glue assisted transfer printing	Si membrane (100 nm thick)	SOI	~0.0 V	N/A	240	10^5	63
4	Conventional transfer printing using elastomer stamp	Nanoribbons ribbon Length (55 µm), thickness (70 nm thick)	SOI	~0.87 V	182	656	10^6	7
5	Flip transfer printing using SU8 as adhesive	Si membrane (340 nm thick)	SOI	~0.95 V	480	160	10^6	13
6	Flip transfer printing using SU8 as adhesive	Si membrane (270 nm thick)	SOI	~0.85	550	160	10^6	64
7	Conventional transfer printing using elastomer stamp	Si ribbons	Bulk Si <111>	N/A	N/A	360	10^3	65
8	Direct roll transfer printing	Nanoribbons ribbon Length (55 µm), thickness (70 nm thick)	SOI	~0.4 V	1000	631	10^6	This work

N/A data not available.

The extracted subthreshold slope is ~1000 mV/decade (using the semi-logarithmic plot of the transfer scan). Table 2 compares the extracted electrical parameters of Si NRFETs fabricated using NRs transferred through the direct roll printing process and those using other transfer printing techniques. It can be seen that the extracted mobility compares well with most of the state-of-the-art Si NR-based devices and is higher than nanomeshed Si nanomembrane-based FET devices[53]. The μ_{eff} value is marginally lower than the previously reported value (680 cm^2/Vs) employing self-assembled nanodielectrics (SAND) dielectric (15 nm thick). However, the process to deposit SAND is time-consuming and requires additional efforts in terms of solution processing in controlled ambient and hence may not be suitable for scalable high throughput processing[7]. Instead with the deposition of a thinner SiN_x dielectric, the mobility of roll printed devices could be enhanced further. The extracted subthreshold slope (SS) value is significantly higher for the roll printed devices. It may be noted that, in the absence of surface anomalies, the theoretical limit of SS is around 60 mV/dec. The calculated subthreshold swing is ~8 times higher than one of the best examples in literature (~120 mV/dec) using SAND[54], and ~16 times larger than the theoretical limit in CMOS. As mentioned above, a thin gate dielectric could improve the gate control over the channel and thus reduce the SS values close to the state of the art.

In nanomaterial-based FETs, working in depletion/accumulation mode, the dielectric/semiconductor interface quality plays a dominant role in defining the transistor performance and electric-bias stability. To this end, we quantified the occupied trap charge density at the SiNx/Si NR interface (D_{it}) using the following relation[55,56]:

$$\Delta Q = \Delta V_{th} \text{ x } Cox \quad (5)$$

To calculate the hysteresis (i.e., ΔV_{th}), the forward and reverse transfer scans were performed between $-5\,V_{GS}$ to $+10\,V_{GS}$. As shown in Supplementary Fig. 7, negligible hysteresis (0.4 V) is observed for the NRFETs. Using the hysteresis data, the Si NRFET showed a D_{it} value of 1.7×10^{11}/cm^2 ($\Delta V_{th} = 0.4$ V, and $C_{ox} = 7 \times 10^{-4}$ F/m^2). The estimated value of D_{it} at the SiNx/Si NR interface is an order of magnitude less than the SiO_2−semiconductor interface for nanomaterial-based FETs[56,57].

Electromechanical characterizations of Si NRFETs

The mechanical robustness and device stability of the fabricated flexible Si NRFETs were evaluated under different bending conditions. The electrical characterization results under bending are shown in Fig. 4. The device was subjected to tension and compression by mounting it onto 3D printed convex and concave structures. For both bending types, the radius of bending curvature was 40 mm, as shown in the inset of Fig. 4a. The transfer and output characteristics under bending are shown in Fig. 4a, b, respectively. As can be seen, the device showed slight variation in I_{on} while V_{th}, SS, and other device parameters were largely remained unchanged. The effect of mechanical stress on I_{on} of NRFET under compressive and tensile bending cycle was investigated with $V_{GS} = 5$ V and $V_{DS} = 3$ V for five randomly chosen NRFET devices (Fig. 4c). The strain resulting from mechanical bending is known to affect the semiconducting material's band structure and hence the effective mass and the mobility of the charge carriers[14,58]. The change in mobility has a direct effect on the source current of the transistor. As expected, a tensile bending strain led to a slight increase in the I_{DS}, whereas a compressive bending led to a decrease in I_{DS}[7]. To inspect the mechanical robustness the fabricated NRFETs were subjected to 100 bending cycles and corresponding drain currents are illustrated in Fig. 4d. The peak values of drain current were obtained under planar conditions after every 10 cycles of compressive and tensile bending (Rc = 40 mm). As can be seen

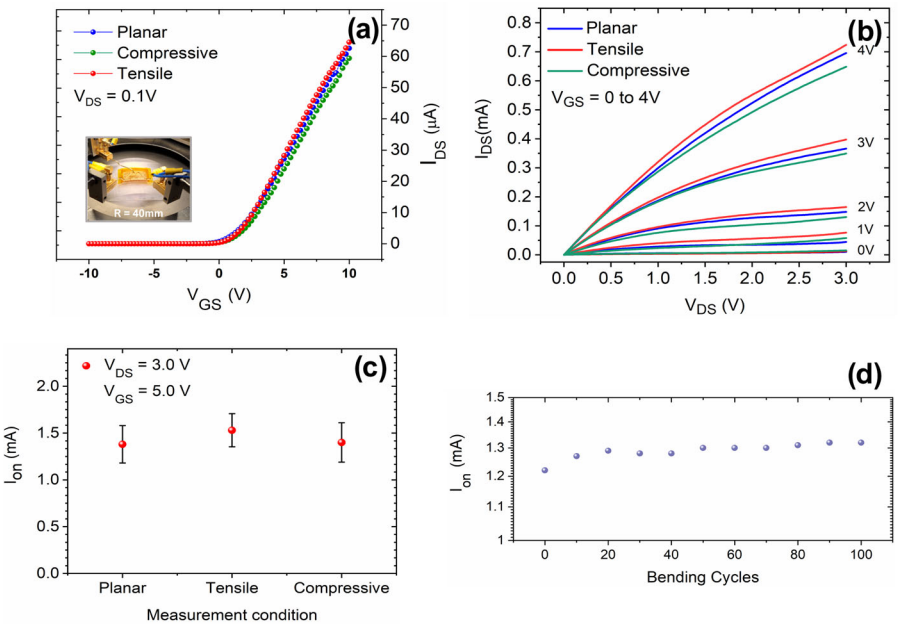

Fig. 4 Electro-mechanical characterization of printed Si NRFETs. a Measured transfer characteristic (I_{DS} vs. V_{GS}) of Si-NRFET under planar, tensile, and compressive bending conditions. **b** Output characteristics of Si-NRFET at planar, and under bending conditions (Rc = 40 mm)). **c** Variation of the on-state current at $V_{GS} = 5$ V at compressive and tensile bending cycles. **d** Variation of the drain current at planar condition during compressive and tensile bending cycles at $V_{DS} = 3$ V, $V_{GS} = 5$ V.

from this set of data, the I_{on} showed a near stable response with repeated bending. The minor variation in the electrical properties during cyclic bending is attributed to two main factors. First, the mechanical bending, which results in the change of the effective mass and hence the mobility of the charge carrier, as mentioned above[15,58]. The second is the delamination of device layers including metal contacts. These can be mitigated and addressed by adding an encapsulation layer on top of the final device/circuits. Such a layout has been demonstrated in the past with a thin layer of the polymer as an encapsulant (usually the same material as substrate) on top of Si NRFET. Such a configuration enables high flexibility along with stable electrical properties by bringing the devices to the neutral mechanical plane and prevents the device from experiencing any strain-induced variations caused during cyclic bending. This could enhance the bendability, device stability and also resolve the slight variation of the electrical properties under bending conditions[59].

In summary, we have presented a simple, efficient, and R2R compatible direct roll printing technique to transfer silicon nanoribbons (Si NRs) directly onto the flexible PI substrate. Avoiding the use of elastomeric transfer stamps, this innovative printing method minimizes the process complexity and enhances the printing yield and registration accuracy. The high transfer yield of ~95% with perfect registration has been demonstrated. The printed NRs were employed as active channel material to obtain high-performance flexible FETs and the ICP process was adapted for the deposition of high-quality dielectric (SiNx) at RT. The Si NRFETs showed excellent performance with mobility (>630 cm^2/Vs) and current on/off ratio (~10^6) at par with devices reported previously using the traditional transfer printing process. Furthermore, excellent robustness under large bending deformation was illustrated. The excellent electrical characteristic of NRFETs after 100 cycles of bending, makes them an excellent candidate for next-generation high-performance flexible LAE electronics. The presented approach could also be used for printing ultrathin micro/nanostructures based on other high mobility materials such as GaAs, GaN, etc.

METHODS

Fabrication of Si NR using SOI wafer

Si-NRs were defined on SOI wafers (donor substrate) using standard photolithography and etching process (top-down method). The commercial SOI wafer having 70 nm top Si (100) layer over 2 μm of buried oxide, supported by 600 μm bulk Si was selected as the donor substrate to fabricate NRs with same dimensions (i.e., thickness, length, and width). The SOI wafers were chemically cleaned to eliminate the surface contaminants by ultrasonication in acetone, isopropyl alcohol (IPA), and deionized (DI) water. Si NRs with a width of 5 μm and length 55 μm were defined by a mask designed with MA/BA6 mask aligner from Suss MicroTec. The sample was spin-coated S1805 photoresist (4000 rpm for 30 s), followed by soft baking at 115 °C for 60 s. At this stage, samples were exposed to UV sources, and patterns were developed by using Microposit MF-319 developer. The exposed Si was etched in a solution of nitric acid (HNO_3), ammonium fluoride (NH_4F), and water (H_2O) in a volume ratio of 126:60:5 (HNO_3: H_2O: NH_4F). The etchant solution has an etch rate of ~150 nm/min. The sample was etched for 2 min to ensure that Si is completely etched away. The photoresist mask, which was used to protect the Si nanoribbons, was dissolved in acetone and isopropanol (IPA) with ultrasonic agitation, then abundantly rinsed with de-ionized (DI) water and dried using a stream of nitrogen flow to lead to Si ribbons structure with 70 nm thickness.

Doping of source and drain region of transistors

The selective doping of the NRs was carried out using spin-on dopant (SOD) through the diffusion of phosphorus (Filmtronics, P451) at 1050 °C and ohmic contacts were created by masking channel with SiO_2. The SiO_2 diffusion barrier mask layer (thickness ~150 nm) was deposited on the top of the wafer by using the plasma-enhanced chemical vapor deposition (PECVD). The source and drain regions were patterned by using the designed mask and conventional photolithography. The resist served as a mask for selective dry etch process with a CH_3/Ar plasma using Reactive Ion Etching (RIE) system (40 sccm CH_3/Ar flow with a chamber base pressure of 30 mTorr, 200 W RF power). This process was carried out to etch the exposed areas of the oxide mask to open the active regions of the source and drain. The doping concentration, measured using 4-point-probe, was found to be higher than 1×10^{19} cm^{-3}. The remaining oxide mask layer was removed with a buffered oxide etch (BOE 5:1). The etching of Box was carried by hydrofluoric acid (HF) solution to obtain the suspended nanoribbons with delicate anchor points at both ends.

Direct printing of Si NR

Custom-made direct roll printing technology was used to transfer the fabricated Si NRs to the receiving flexible substrates including metal foils (e.g., Al, Cu, and Mg) and polymers (e.g., Kapton sheet, PET, and PI). In this approach, all the steps are carried out at low temperatures to complete the device fabrication. For a detailed statistical data study and device fabrication, PI foil (thickness of 25 µm) was used as a receiver substrate. The process details are as follows: an adhesion promoter was applied to the commercial PI substrate prior to printing. An ultrathin layer of PI-2545 precursor (from HD microsystems) was spun over the PI sheet at 2000 rpm for 60 s (thickness ~1.0 µm). The adhesion between the receiver substrate and the PI layer was promoted by coating (VM652 from Microsystems). The spun PI layer (partially cured at 120 °C for 2 mins) provided an ultrathin layer of adhesive, during direct roll printing of Si NR arrays from the SOI wafer to the PI substrate. The PI substrate is subsequently cured at 250 °C for 2 h to ensure solidification through the thickness of the thin film and to enhance the adhesion of the NRs on the receiver substrate. A reliable direct roll printing depends critically on the conformal contact at the interface of the donor/interfacial adhesion of semi-cured PI on the receiver substrate.

Silicon nanoribbon field-effect transistor fabrication

The fabrication of NRFETs was completed by the room temperature deposition of high-quality gate dielectric (SiN_x, 100 nm) on the printed NRs by using ICP-CVD system followed by metal deposition (Ti (10 nm)/Au (90 nm)) for gate, source, and drain using e-beam evaporation method and lift-off. A short dip in diluted HF was performed prior to metallization to remove the native oxide on the active Si regions, source, and drain (S/D).

Morphological and electrical characterizations

The structure and surface morphology of direct printed NRs were studied through Scanning electron Microscopy (SEM) of Hitachi SU824 and Atomic Force Microscope (Dimension Icon AFM from Bruker Nano). Electrical characterizations of fabricated Si NRs based field-effect-transistor (Si-NRFET) on the flexible (PI) substrate were performed in the ambient environment using Cascade Micro-tech Auto-guard probe station interfaced to a semiconductor parameter analyzer (B1500A, Agilent).

DATA AVAILABILITY

The datasets generated and analyzed during this study are available from the corresponding author on reasonable request.

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AUTHOR CONTRIBUTIONS

A.Z. and R.D. conceived the idea. A.Z. performed the transistor device fabrication, characterizations and wrote the manuscript. A.S.D. assisted in device electrical characterizations and data analysis. A.C. designed and built the roll printing set-up and performed COMSOL simulations. D.S., A.S.D., and R.D. contributed to the writing of the manuscript. R.D. provided overall supervision of the work. All authors have read and approved the final manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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