



SMARTRENTCOM, LLC PHOENIX, AZ USA

THIRD GENERATION SMARTRENT HUB
PROTOTYPE VERSION X2

SH_SMR19002_POWER
SMR19002_POWER.SchDoc



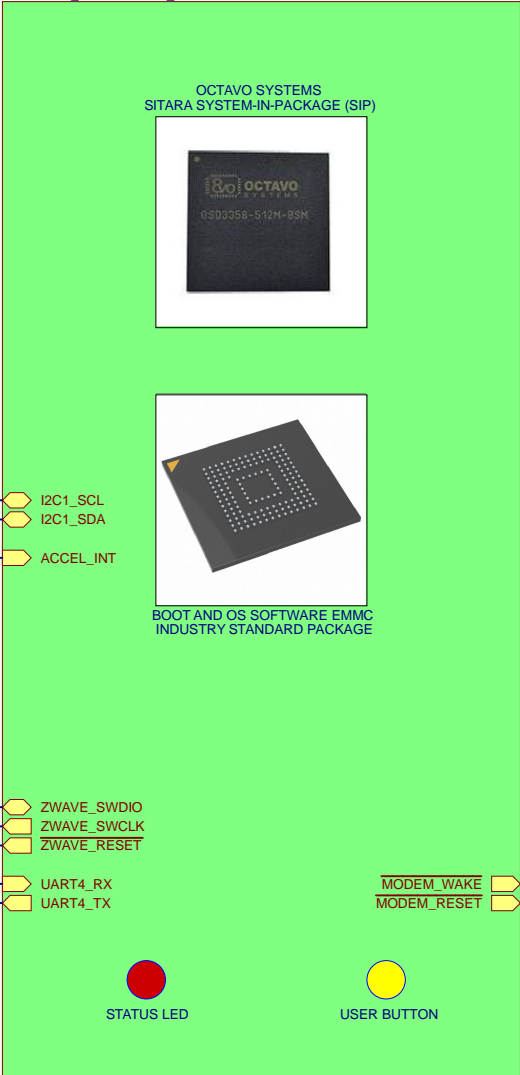
SH_SMR19002_SENSORS
SMR19002_SENSORS.SchDoc



SH_SMR19002_ZWAVE
SMR19002_ZWAVE.SchDoc



SH_SMR19002_PROCESSOR_CORE
SMR19002_PROCESSOR_CORE.SchDoc

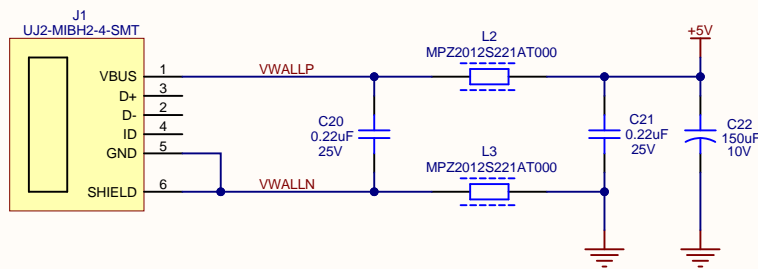


SH_SMR19002_USB
SMR19002_USB.SchDoc



WALL ADAPTER POWER INPUT (MICRO USB STYLE)

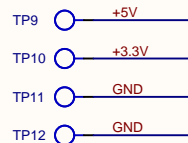
- PROVIDES LOCAL INPUT IMPEDANCE AND EMC SUPPORT
- RELATIVELY HIGH ESR RESEVOIR CAPACITORS REDUCE RINGING
- ESR OF FERRITE BEADS ALSO CONTRIBUTES TO REDUCED RINGING



CHASSIS GROUND NOTES -

- THERE IS NO DIRECT EARTH CONNECTION IN THE SYSTEM
- THE CHASSIS GROUND (CHGND) ISOLATES CABLE SHIELDS FROM SYSTEM EMI AND MAKES THOSE SHIELDS NO WORSE THAN THE WALL ADAPTER
- CHGND FORMS THE GROUND FOR THE ETHERNET BOB SMITH TERMINATION
- NOTE THAT CHGND IS NOT USED FOR USB IN AN INTERNAL-ONLY CONFIGURATION OF THE USB HOST CONNECTORS (SEE USB PAGE)

POWER TEST POINTS



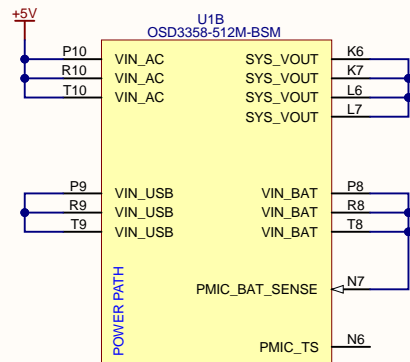
GLOBAL MECHANICAL FEATURES

- BOARD MOUNTING HOLES FOR ENCLOSURE BOSSES ARE LEFT UNCONNECTED AND UNPLATED TO IMPROVE OPTIONS



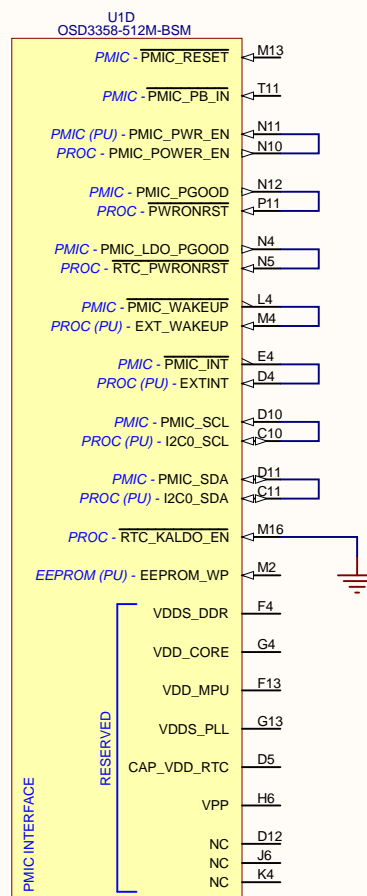
POWER PATH CONTROL

- ONLY WALL POWER IS IN USE HERE
- OUTPUT OF POWER PATH IS USED ONLY INTERNALLY TO THE SIP



PMIC POWER MANAGEMENT

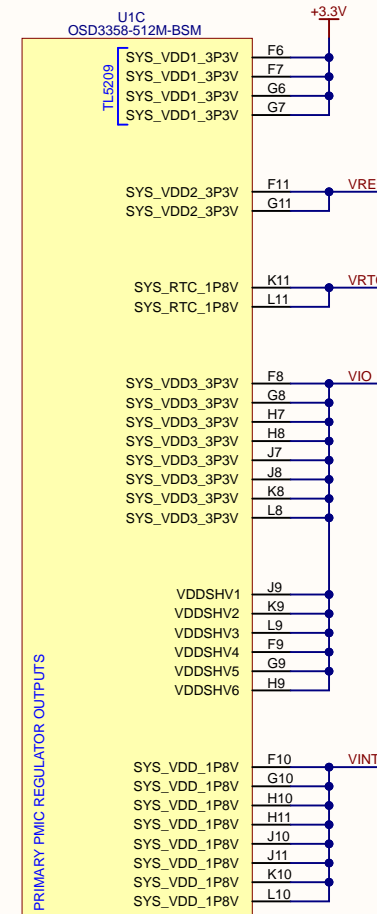
- THESE ARE GENERAL DEFAULT STRAPS AND CONFIGURATION POINTS DEFINED BY OCTAVO FOR THE SIP PART
- PROVIDES SPECIFIC RESET FEATURES AND COMMUNICATION WITH THE PMIC AND EEPROM INTERNAL DEVICES



- WE LEAVE THE EEPROM WRITE PROTECTED BECAUSE WE DON'T USE IT AND OCTAVO SUGGESTS THAT THEY MIGHT ADD DATA TO IT SOMEDAY
- OPTION TO REMOVE WP WAS REMOVED AFTER IT REMAINED UNUSED WELL INTO THE PREPRODUCTION DESIGN CYCLE
- RTC LDO IS ENABLED (SEE TIMING), AND WE FOUND NO REASON NOT TO SIMPLY GROUND THIS ENABLE SIGNAL

PMIC POWER OUTPUTS

- MOSTLY PRODUCES RAILS FOR PROCESSOR CORE NEEDS
- PROVIDES EXTERNAL 3.3V AND REFERENCES



- USE VDD1 FOR 3.3V EXTERNAL LOADS
- VDD1 IS SEPARATELY LINEAR REGULATED AND GOOD FOR RADIO LOADS LIKE IN THIS DESIGN
- THIS RAIL HAS BEEN FOUND TO RUN SLIGHTLY HIGH
- THERE IS INTERNAL DECOUPLING IN ADDITION TO ANYTHING ADDED AT THE POINT OF LOAD
- SEE NOTE ON INPUT VOLTAGE REQUIREMENTS

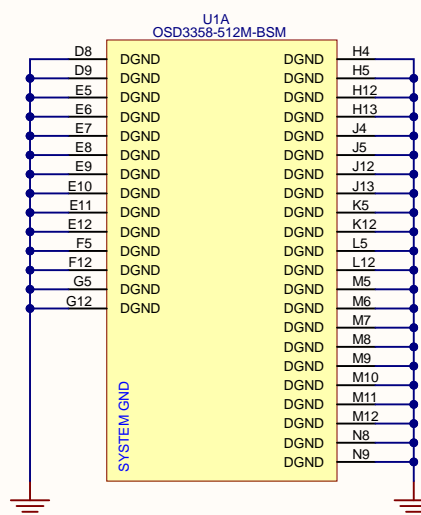
- VDD2 DOES NOT REQUIRE A MINIMUM LOAD
- NOT USED EXTERNALLY IN THIS VERSION

- WITH 10uF INTERNAL CAPACITANCE AND LOW LOAD, RTC SUPPLY SHOULD DROP SLOWER THAN THE VDDSHV RAILS
- SEE APPLICATION NOTE ON TRACKING REQUIREMENT

- VDD3 IS USED ONLY INTERNALLY
- THESE SET ALL VARIABLE LEVEL I/O TO 3.3V LOGIC

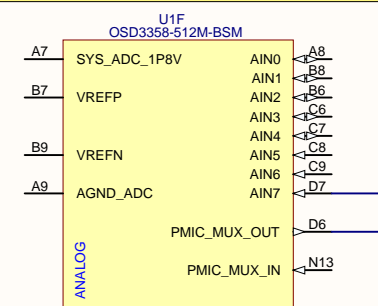
- 1.8V IS USED ONLY INTERNALLY
- ALL NECESSARY DECOUPLING IS INTERNAL

SIP MODULE DIGITAL POWER RETURNS




POWER SUPPLY MONITORING

- MONITOR INTERNAL POWER DEVICES ONLY
- INTERNAL DECOUPLING IS SUFFICIENT FOR THIS PURPOSE



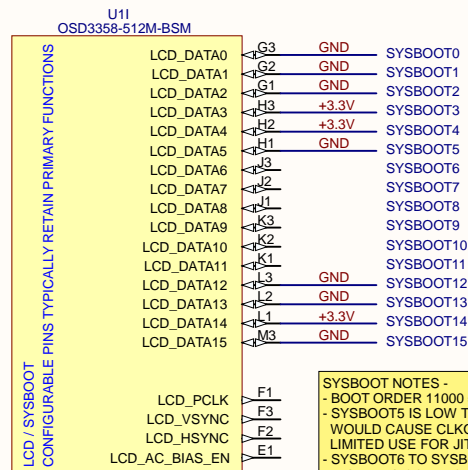
BOARD FEATURES FOR ASSEMBLY



TITLE: SMRHUB - PROCESSOR POWER		Allied Component Works 18908 Premiere Court Gaithersburg, MD 20879 (301) 996-3766  ALLIED COMPONENT WORKS
DRAWING: SMR19002_SMRHUB_X2	REVISION: X2	
MODIFIED: 4/29/2020	SHEET 2 OF 7	
CAD FILE: SMR19002_POWER.SchDoc		



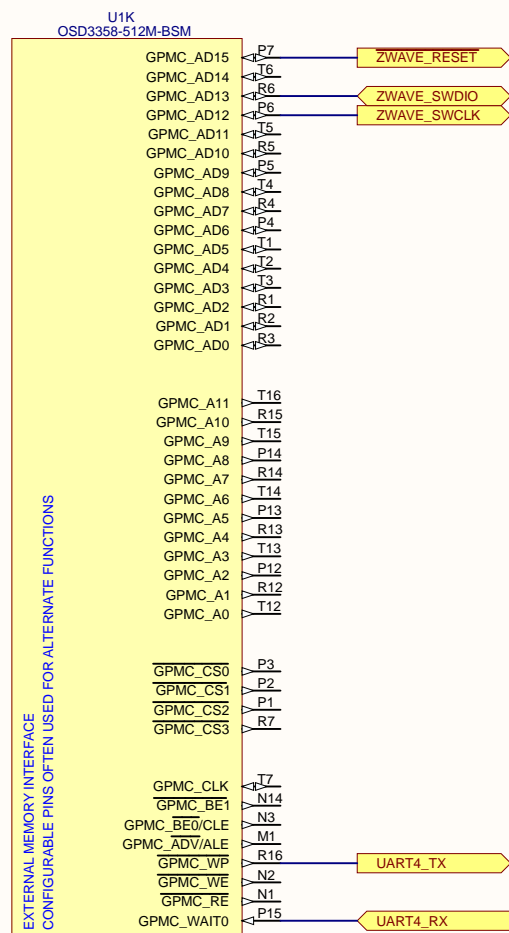
BOOT CONFIGURATION



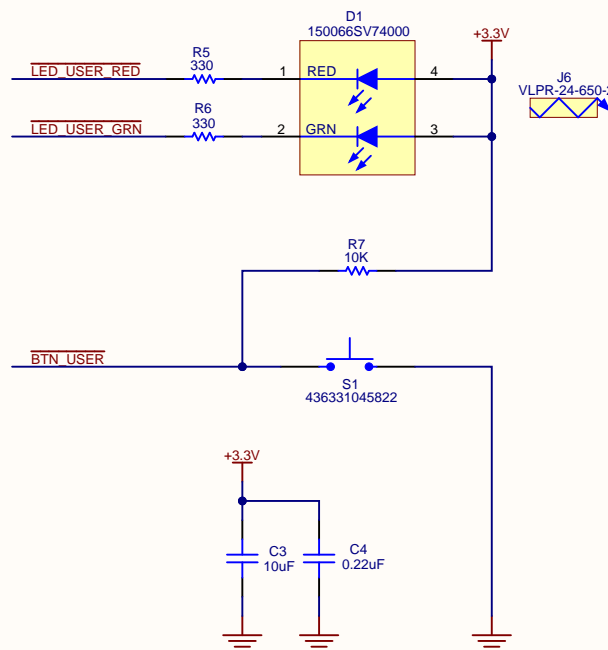
SYSBOOT NOTES -

- BOOT ORDER 11000 = SPI MMC USB UART
- SYSBOOTS IS LOW TO PREVENT CLKOUT1 FOR EMI REASONS, WHILE SYSBOOTS HIGH WOULD CAUSE CLKOUT1 TO APPEAR ON XDMA_EVENT_INTR0, BUT IT IS NOTED TO HAVE LIMITED USE FOR JITTER REASONS
- SYSBOOTS6 TO SYSBOOTS1 ARE "DON'T CARE" VALUES FOR THE SELECTED BOOT DEVICES
- HIGH BIT RATE CONTRA EXPECTED CLOCK FREQUENCY AND UNSPECIFIED INTERNAL FUNCTIONS
- THE SINGLE PULL RESISTORS ARE REDUCED TO ZERO TO LIMIT ASSEMBLY COST AND IMPROVE ROUTING, BUT WITH THE UNDERSTANDING THAT SOFTWARE MUST BE SURE TO LEAVE THESE PINS IN THE DEFAULT HIGH-Z STATE, WITH UNKNOWN POOR RESULTS EXPECTED OTHERWISE

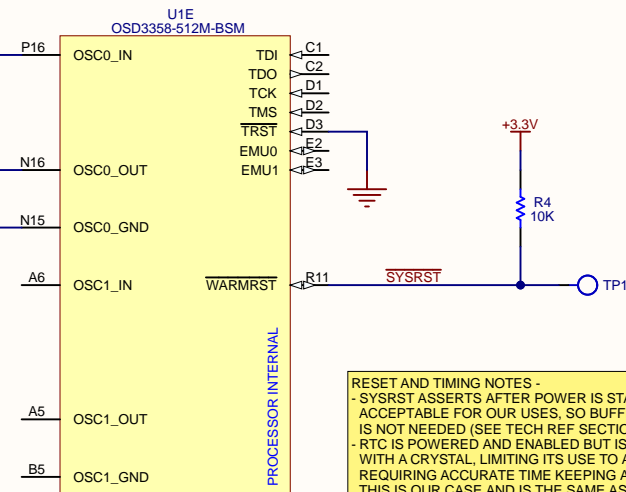
CORE I/O BLOCK



USER INTERFACE FEATURES



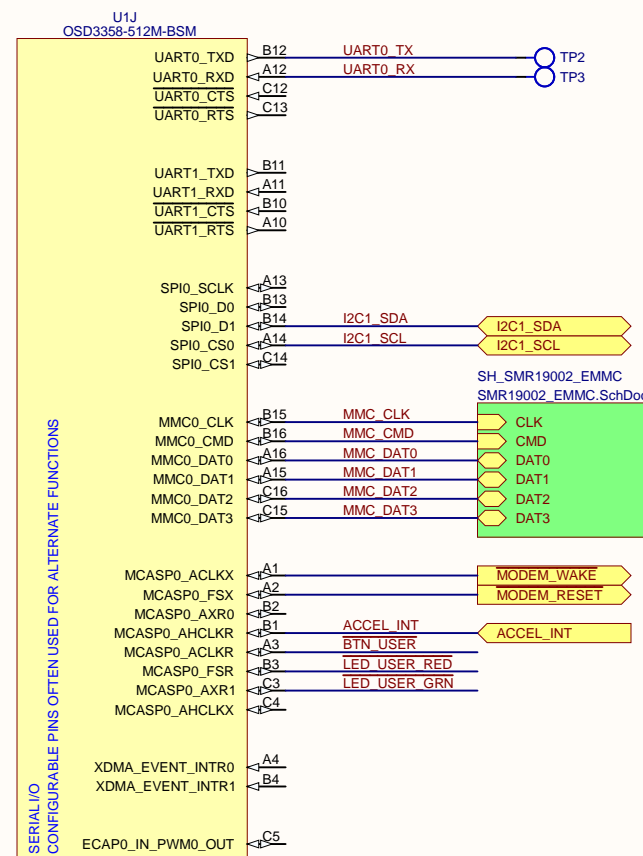
RESET AND TIMING



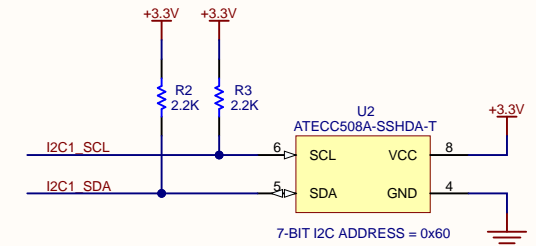
RESET AND TIMING NOTES -


- SYSRST ASSERTS AFTER POWER IS STABLE, WHICH IS ACCEPTABLE FOR OUR USES, SO BUFFER FROM PWRONRST IS NOT NEEDED (SEE TECH REF SECTION 8.1.7.3)
- RTC IS POWERED AND ENABLED BUT IS NOT PROVISIONED WITH A CRYSTAL, LIMITING ITS USE TO APPLICATIONS NOT REQUIRING ACCURATE TIME KEEPING AND/OR WITH NO BATTERY. THIS IS OUR CASE AND IS THE SAME AS THE DEFAULT FOR THE POCKET BEAGLE REFERENCE BOARD.
- JTAG IS NOT USED, SO IT IS HELD IN RESET

CORE I/O BLOCK



CRYPTOGRAPHIC COPROCESSOR



TITLE:		 ALLIED COMPONENT WORKS
SMRHUB - PROCESSOR CORE		
DRAWING: SMR19002_SMRHUB_X2	REVISION: X2	
MODIFIED: 4/29/2020	SHEET 3 OF 7	
CAD FILE: SMR19002_PROCESSOR_CORE.SchDoc		Allied Component Works 18908 Premiere Court Gaithersburg, MD 20879 (301) 996-3766



A

B

C

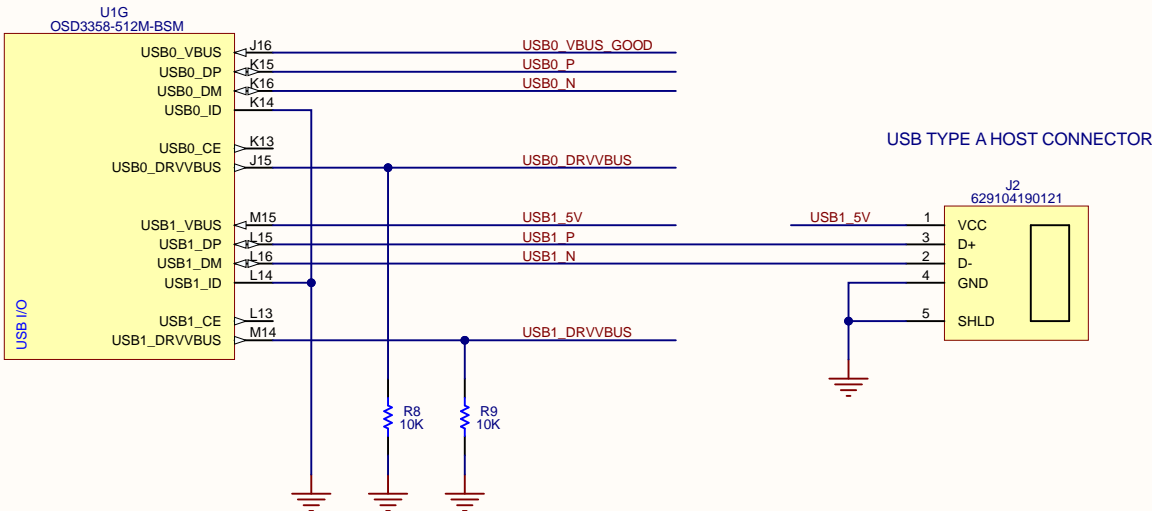
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A

B

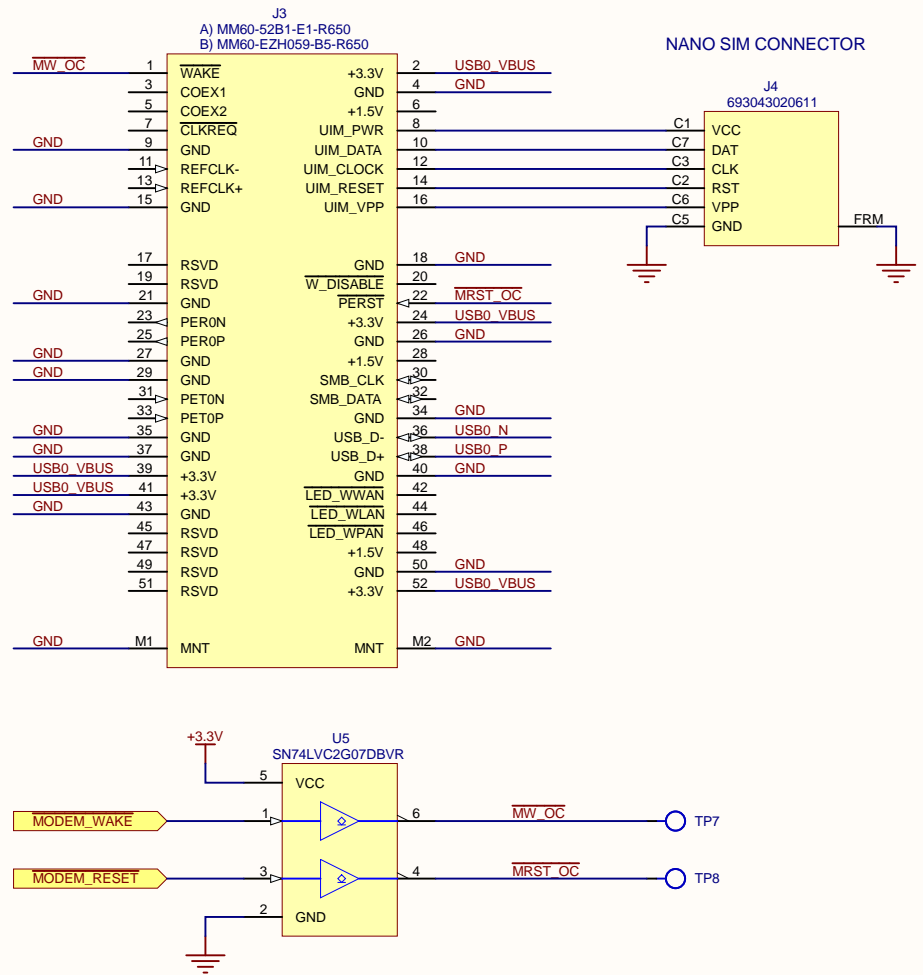
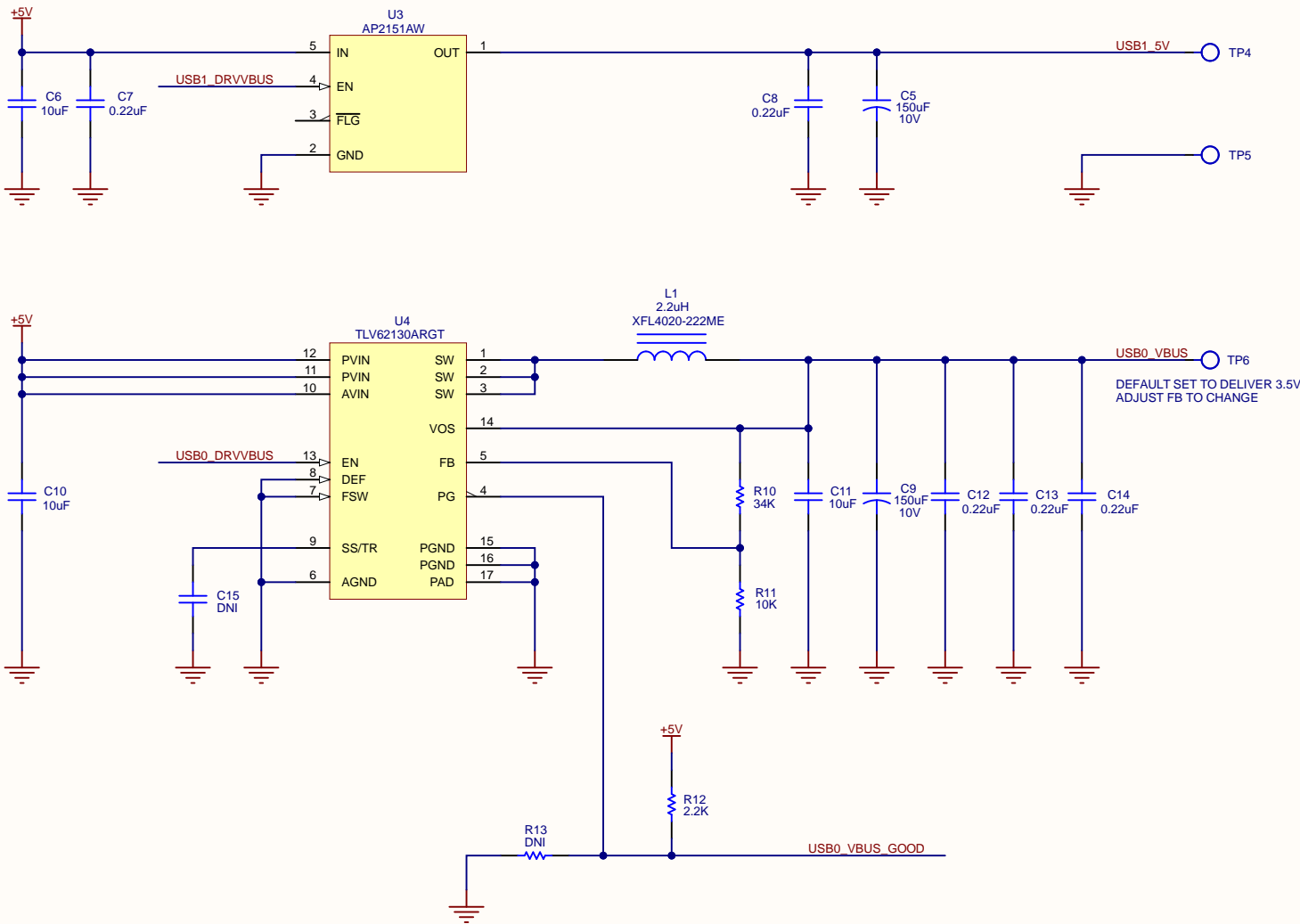
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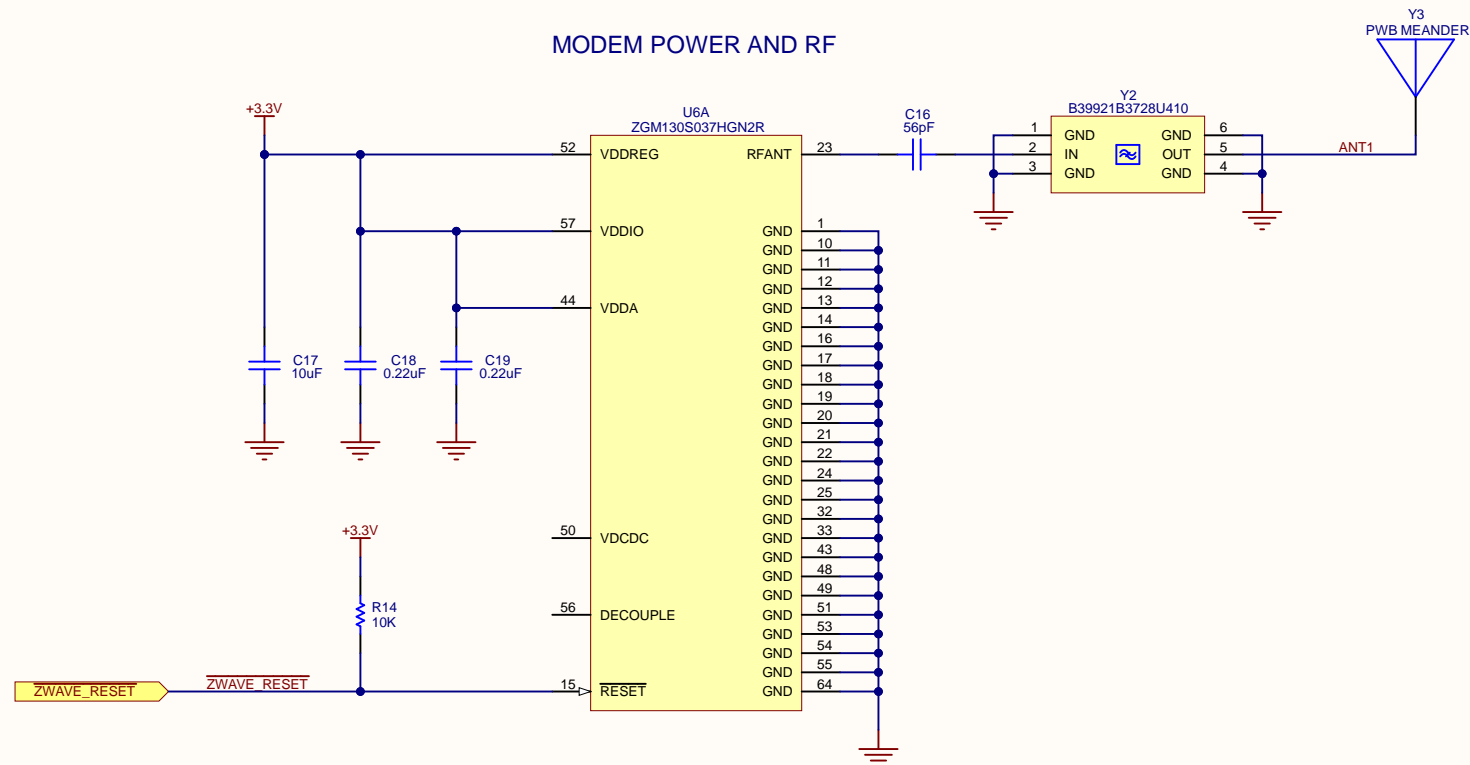
NOTES -

- THE USB HOST PORTS ARE NOT INTENDED FOR GENERAL USE, SO THEY INCLUDE SOME DETAILS TAILORED TO THE NEEDS OF THE SPECIFIC TARGET DEVICES AND LIMITATIONS THAT HELP CONTAIN COST.
- THE TYPICAL DEVICE FOR THE TYPE A CONNECTOR USES THE CONNECTOR AS AN RF SHIELD, AND SO THEY ARE BEST SERVED WITH THE SHIELD TIED TO THE SIGNAL GROUND PLANE AT THE CONNECTOR INTERFACE.
- THE MODEM INTERFACE IS IN THE FORM OF A MINI PCIe CONNECTOR, PRIMARILY DESIGNED TO SUPPORT A CAT M1 MODEM SUCH AS QUECTEL, WITH SOME SPECIFIC IMPLICATIONS AND RELATED TRADEOFFS MADE -
- A) SUPPLY VOLTAGE IS SET AT THE HIGH END OF THE MINI PCIe SPECIFICATION TO FURTHER SUPPORT POWER CONVERTERS ON THE MODULE WITH MINIMAL HUB COMPONENTS. CELLULAR MODEM MODULES DO NOT TEND TO USE THIS POWER SUPPLY DIRECTLY FOR LOGIC, PARTICULARLY FOR ANY LOGIC (ie USB) THAT IS CONNECTED TO THE HUB PROCESSOR. FINALLY, SOME CHEAPER MODULES MIGHT DEPEND ON THIS VOLTAGE BEING HIGHER THAN 3.3V, SUCH THAT THIS STARTING POINT AND AN ABILITY TO ADJUST ARE POTENTIALLY HELPFUL.
- B) THE PERSTn SIGNAL IS DRIVEN OPEN COLLECTOR BECAUSE IT IS ALWAYS PULLED UP ON A MODULE AND SOME MODULES MIGHT USE A DIFFERENT LOGIC LEVEL. THIS SHOULD BE CHANGED ONLY IN SPECIFIC KNOWN USE CASES. HW+SW SHOULD NOT DRIVE THIS SIGNAL HIGH WITH POWER OFF. SW SHOULD DRIVE THIS SIGNAL LOW UNTIL A MANAGED TIME AFTER POWER BECOMES STABLE.
- C) THE WAKEn SIGNAL IS SPECIFIED BY MINI PCIe AS AN OPEN COLLECTOR OUTPUT, OFTEN WITH WIRE-OR OPERATION AMONG SOCKETS. IN GENERAL, IT IS NOT INTENDED TO BE USED THIS WAY FOR USB DEVICES. HOWEVER, SOME MODULES DRIVE IT OPEN COLLECTOR, WHILE OTHERS HAVE USED THIS PIN AS AN INPUT FOR OPTIONAL CONTROLS. WE WIRE-OR OUR OWN OPEN COLLECTOR DRIVE TO THIS PIN TO COVER POSSIBLE FUTURE USES BUT STILL NOT INTERFERE WITH ANYTHING. SPECIFIC KNOWN CASES MIGHT REQUIRE A DIFFERENT BUFFER, BUT THIS IS THE DEFAULT FOR NOW. SW SHOULD DEFAULT THIS SIGNAL HIGH (OPEN) WHEN NOT IN USE.
- THE USB SWITCH CONTROL FROM THE HUB PROCESSOR MANAGES THE MODEM POWER, BUT THE FEEDBACK TO THE USB PORT MUST BE AT 5V, ASSUMED TO BE A COMPARATOR ONLY AND IMPLEMENTED USING THE POWER GOOD SIGNAL, THUS REQUIRING ACTIVE DRIVE OF PG WHEN DISABLED AS OFFERED BY THE 'A' SUFFIX PART. A PULL DOWN RESISTOR SITE (DNI) ALLOWS AN ALTERNATE CONFIGURATION FOR ANY FUTURE ASSEMBLY ON WHICH THE MODEM FEATURES ARE NOT INSTALLED.
- A NANO SIM CARD CONNECTOR ALLOWS CONNECTION OF THE SIM CARD FOR MODEM MODULES THAT DO NOT HAVE THE CONNECTOR. IN PRINCIPLE IT CAN BE LEFT OFF OF ASSEMBLIES THAT USE AN EQUIPPED MODEM. THIS CARD IS VERY LOW POWER, IT IS PHYSICALLY RIGHT NEXT TO THE MINI PCIe CONNECTOR, AND IT CAN'T BE REACHED WITH THE MODEM INSTALLED; ALL REDUCING THE NEED AND INCREASING THE RELATIVE RISK OF ADDING ANY NOISE CONTROL OR PROTECTION DEVICES, IN ADDITION TO CONSIDERATION OF THEIR ADDED COST.

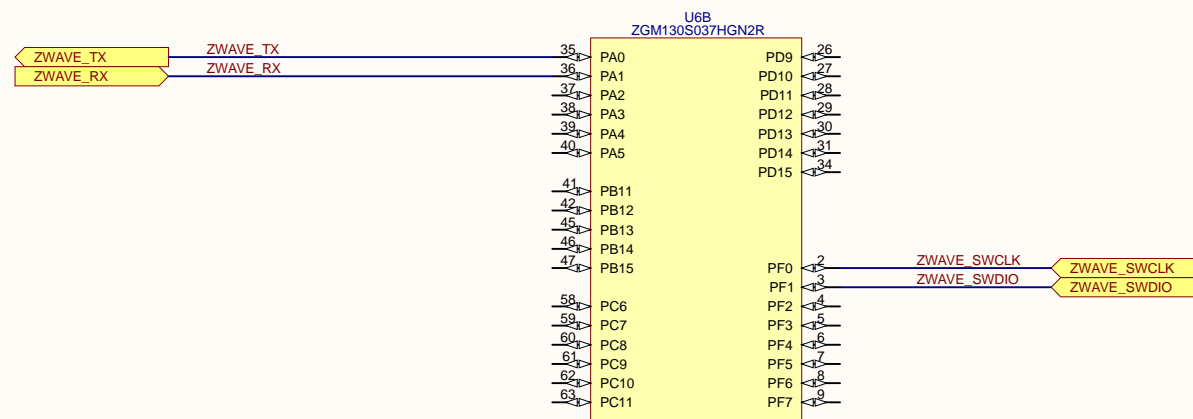


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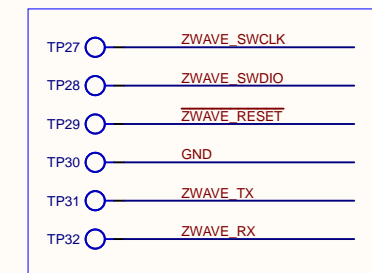
MODEM POWER AND RF




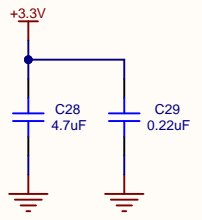
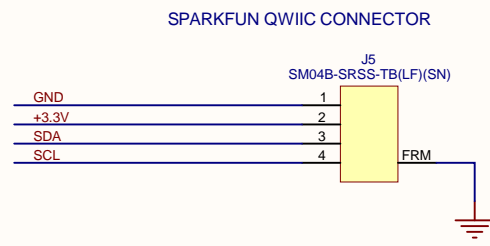
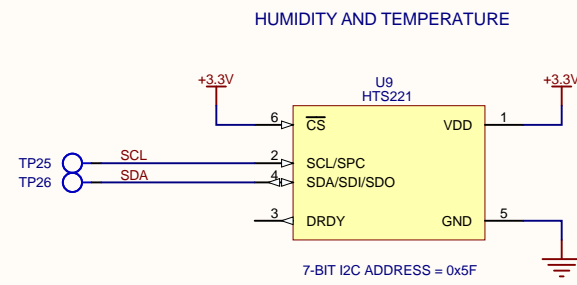
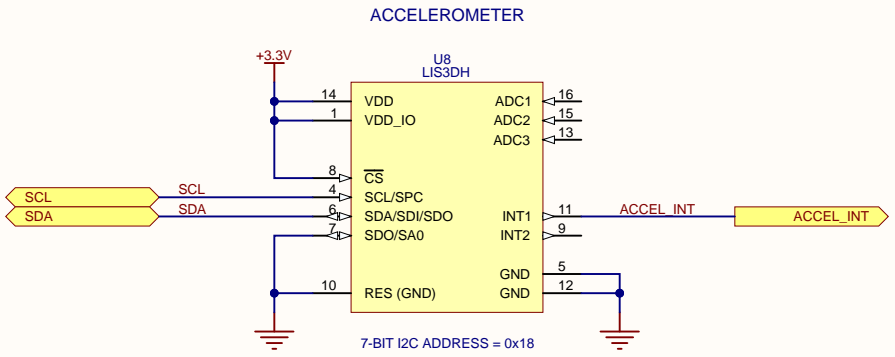
MODEM DIGITAL INTERFACE




MANUFACTURING AND TEST INTERFACE



TITLE:		 ALLIED COMPONENT WORKS
SMRHUB - Z-WAVE MODULE		
DRAWING: SMR19002_SMRHUB_X2	REVISION: X2	
MODIFIED: 4/29/2020	SHEET 6 OF 7	
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TITLE:		SMRHUB - SENSORS		<div>Allied Component Works 18908 Premiere Court Gaithersburg, MD 20879 (301) 996-3766</div> <div> ALLIED COMPONENT WORKS</div>
DRAWING:	SMR19002_SMRHUB_X2	REVISION:	X2	
MODIFIED:	4/29/2020	SHEET 7	OF 7	
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