Low Phase Noise Synthesizer optimized for Wideband 0-IF Radio Receiver

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Abstract— **In this paper the performance of two wideband PLL frequency synthesizers realized with ADF5355 and HMC833 chips respectively has been compared. Both of them were investigated as a local oscillator for 0IF receiver operating from 1 GHz to 6 GHz. In order to provide required harmonics level below -40 dBc the final solution is based on the ADF5355 followed by a switched bank of four low pass filters. The phase noise level is better than -90 dBc @ 1 kHz and spurious are lower than -70 dBc.**

Index Terms— **wideband synthesizer, PLL frequency synthesizer; LO for 0-IF receiver;**

I. INTRODUCTION

Frequency synthesizers are still one of the most crucial and essential components of each modern communication system due to a typical architecture comprising an up or down frequency conversion. In many applications the requirements for digitally controlled local oscillators (LO) are challenging in terms of the spectrum purity as well as frequency accuracy and long term stability. An optimal design of the LO thus require investigation of several possible approaches.

There are two widely known RF signal synthesis methods which enable easy digital frequency control. Historically the first one was a Phase-Locked Loop (PLL) used for stabilization of a typical Voltage-Controlled Oscillator (VCO). The PLL architecture is based on the frequency and phase comparison between reference signal (e.g. high stability crystal oscillator) and frequency divided output signal (VCO).

The other method is a Direct Digital Synthesis (DDS), which uses a combination of digital circuitry and digital-to-analog converter to synthesize any signal directly from its discrete samples. According to the Nyquist theorem, the maximum output frequency of a DDS system is less than a half of the clock frequency f_c. In practice, the maximum frequency is limited to $0.4 \times f_c$, due to the difficulty of high-order antialiasing filters realization. Currently available DDS systems work with clock signal up to 3.5 GHz [1] allowing a synthesis of sinusoidal signal with frequency of up to 1.4 GHz and tunable with a very fine resolution (in the order of µHz). For applications requiring LO above 1 GHz and similar fine frequency tuning, a combination of a PLL and DDS is

typically used [2]. An alternative to this solution is a use of a fractional-N PLL, however it causes deterioration of the phase noise.

The aim of this project was to choose optimal heterodyne solution dedicated to the 0-IF receiver, based on a wideband quadrature mixer ADL5380 (Analog Devices) [1], which block diagram is presented in Fig. 1. Its detailed description is presented in paper [3]. The requirement for the input signal frequency range covers the $1\,\text{GHz} \div 6\,\text{GHz}$ band. The intermediate frequency band for I and Q components is located between $0 \div 250\,\text{MHz}$, which results in a maximum bandwidth of a single analyzed input signal equal to 500 MHz.
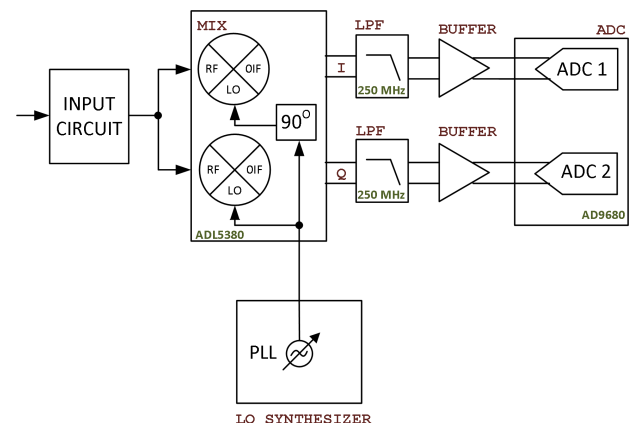

Figure 1.   Block diagram of wideband 0-IF radio receiver.

Parameters of the LO synthesizer are imposed by required receiver capabilities. Therefore, LO's tuning range should cover frequency range 1250 MHz ÷ 5750 MHz at least. Due to the DC-offset in I and Q components, the dynamic range of 0-IF receiver drops significantly in the center of reception band determined by LO frequency, what is especially troublesome in the case of narrowband signals reception located on or near the LO frequency - thus a slightly LO retuning possibility is required [4]. For this reason, tuning step of 10 MHz is proposed. It results from a compromise between the lowest level of phase noise and the use of PLL's phase detector's low comparison frequency, which eliminates the need of using

fractional-N PLL or combined PLL & DDS configuration. Moreover, due to the phenomena of reciprocal mixing, the LO's phase noise limits the receiver's dynamic range, especially near mid-band analysis. It is therefore desirable to achieve the best possible performance - phase noise level of -90dBc/Hz @ 1 kHz at least. The acceptable LO's spurious level results directly from the assumed receiver's dynamic range, and must be less than -70 dBc. Due to the use of ADL5380 quadrature mixer, which includes a polyphase filter to produce a heterodyne signal in quadrature, it is required to ensure heterodyne's harmonics level below -40 dBc.

Only four ICs available on the market equipped with reconfigurable VCOs fulfill the frequency range requirement: ADF5355 (Analog Devices) [1], HMC833 (Analog Devices, earlier Hittite) [1], LTC6946-4 (Linear Technology) [5] and MAX2870 (Maxim Integrated) [6]. After a preliminary analysis of datasheets, LTC6946-4 and MAX2870 has been rejected due to its worse performance. A reconfigurable VCO consists of integrated bank of fixed switched capacitors and varactor diodes, which results in a significant increase in the effective frequency tuning range of the whole PLL circuit, while keeping almost constant the tuning sensitivity [1].

In this paper the two other PLL synthesizers were described and compared. For this purpose, two testbeds for ADF5355 and HMC833 have been designed, fabricated and measured. Based on measurements' results, a system with better performance have been chosen, redesigned and applied in the final version of the receiver.

II. TESTBEDS FOR SYNTHESIZERS

Test boards with ADF5355 and HMC833 chips respectively, share the same block diagram shown in Fig.2 and have been fabricated on a four-layer FR4 HTG 150 substrate.
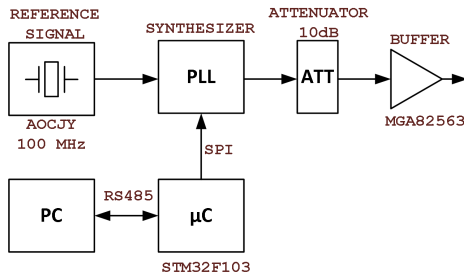

Figure 2.   Block diagram of tested synthesizers PCB.

The AOCJY OCXO oscillator from Abracon Corp. is used as a reference signal source for the PLL system [7]. It is characterized by output frequency of 100 MHz, stability of ± 5 ppb and phase noise level of -140 dBc @ 1 kHz. Digital control of internal PLL's registers and communication with PC terminal via RS485 has been realized by the STM32F103 ARM microcontroller. The RF signal sourced by the PLL chip is passed through a chain of a pi-attenuator and MGA82563 buffer (Avago) [8]. This configuration ensures linear operation of the amplifier (i.e. significantly below of the buffer's P_{1dB} compression point) and high isolation between the PLL chip and the testbed.

A. A synthesizer based on the ADF5355

The ADF5355 chip allows implementation of a fractional-N or integer-N PLL frequency synthesizer operating from 54 MHz to 13600 MHz. Such a wide range of the operating frequency is realized using of build-in divider and doubler. The VCO integrated in the ADF5355 chip is tunable in the range of 3400 MHz ÷ 6800 MHz. The subband from 54 MHz to 3400 MHz is covered by the VCO frequency division. Frequencies above 6800 MHz are obtained with using the internal doubler – however in this case the signal spectrum consists of the eligible and subharmonic products. The photo of the ADF5355 testbed is presented in Fig. 3.
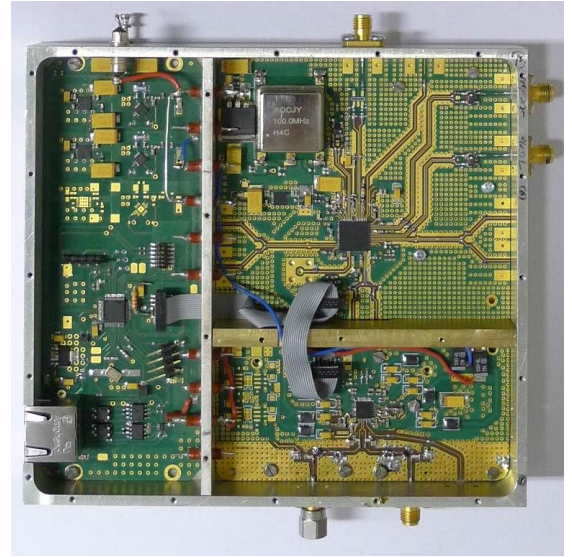

Figure 3.   The view of the synthesizer testbed with ADF5355.

B. A synthesizer based on the HMC833

The HMC833 chip, as well as the ADF5355, allows the PLL implementation with both fractional and integer N, in the range of 25 MHz ÷ 6000 MHz. The fundamental tuning range of integrated VCO covers frequencies from 1500 MHz to 3000 MHz. Signals below 1500 MHz are obtained by the frequency division while those above 3000 MHz are enabled a frequency doubler. Likewise in the system with ADF5355, there is a crosstalk of the doubler's input frequency. The photo of the synthesizer based on the HMC833 is presented in Fig. 4.
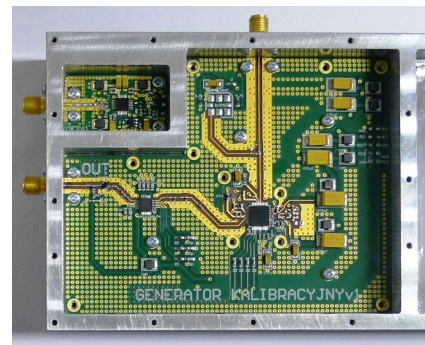

Figure 4.   The photo of the HMC833 based syntesizer.

III. MEASUREMENTS OF TESTBEDS

The testbeds measurements of phase noise, second (H2) and third (H3) harmonic and spurious level determined in ± 25 MHz frequency offset from carrier were performed using N9020 PXA signal analyzer from Keysight with automation procedures written in Python programming language.

In Table 1 phase noise levels for ADF5355 and HMC833 testbeds are collected for selected frequencies within the desired operating band and at typical frequency offsets from a carrier.

TABLE I. PHASE NOISE OF ADF5355 AND HMC833

f_{OUT}	ADF5355 [dBc]			
	@1 kHz	@10 kHz	@100 kHz	@1 MHz
1 GHz	-106.6	-110.1	-110.4	-131.7
2 GHz	-101.3	-105.1	-105.0	-131.1
3 GHz	-98.2	-99.6	-108.3	-127.7
4 GHz	-92.3	-99.4	-99.3	-126.6
5 GHz	-91.5	-95.7	-101.8	-125.4
6 GHz	-90.1	-93.7	-102.4	-122.5
	HMC833 [dBc]			
1 GHz	-111.5	-114.2	-113.2	-132.9
2 GHz	-108.2	-111.2	-108.9	-131.3
3 GHz	-106.0	-108.4	-104.9	-126.0
4 GHz	-94.0	-108.0	-103.4	-123.6
5 GHz	-94.7	-105.6	-100.9	-121.8
6 GHz	-93.5	-103.6	-99.2	-118.4

Presented results show that the phase noise performance of HMC833 is slightly better. There is also an easy noticeable natural trend of the phase noise degradation proportional to frequency in the case of the both synthesizers.

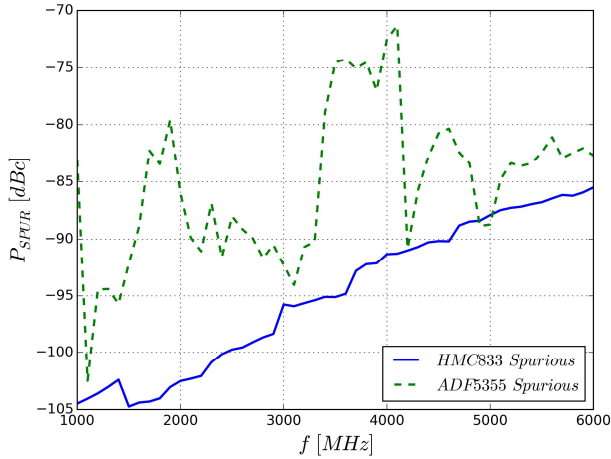Spurious levels characteristics of both testbeds are presented in Fig.5

Figure 5. Spurious levels of ADF5355 and HMC833 based testbeds.

The characteristics of H2 and H3 levels for ADF5355 and HMC833 are presented in Fig.6 and Fig.7 respectively. Additionally, in Fig.7 subharmonic level for HMC833 synthesizer is shown.
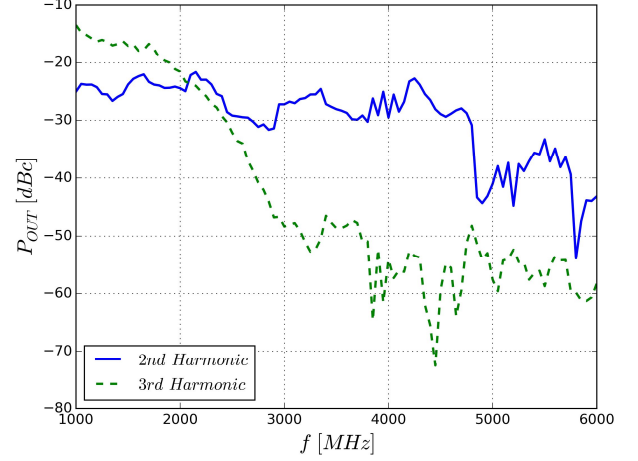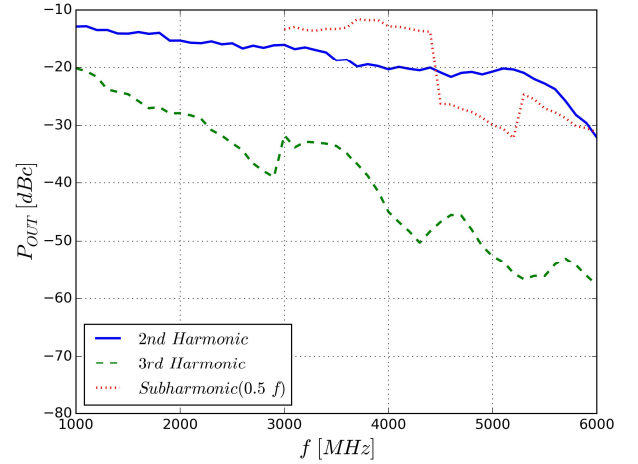

Figure 6. Harmonics levels of ADF5355.

Figure 7. Harmonics and subharmonic levels of HMC833.

The level of harmonics, especially the H2 is about 10 dB lower in the ADF5355 synthesizer. The highest spurious level in ADF5355 is significantly higher, but both synthesizers fulfill requirements for local oscillator. Moreover, it is essential that in case of the HMC833 synthesizer operating above 3 GHz, subharmonic product exceed the level of -15 dBc, which disqualifies technically its application as LO in the target wideband receiver.

IV. FINAL APPLICATION AND MEASUREMENTS

The lower spurious and harmonics level and the absence of subharmonic products were a key reason of ADF5355 chip selection for the final LO block realization in wideband receiver. Further decrease of synthesized signal's harmonics level (below assumed -40 dBc) have been obtained by additional filtering. To meet such requirements it was necessary to use four, 9-order lowpass filters, switched by HMC344 [1] according to the frequency of generated signal. The final block diagram of the synthesizer is presented in Fig. 8 and its photo is shown in Fig. 9.
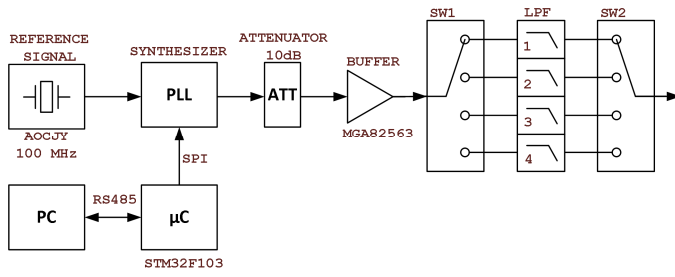
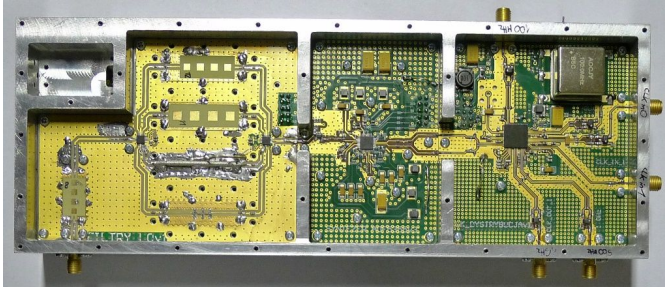Figure 8. Block diagram of final synthesizer circuit.

Figure 9. Photo of the final LO realization.

A representative spectrum measured for the signal of 5.6 GHz is presented in Fig. 10. The second and third harmonics levels of LO with and without filters are illustrated in Fig. 11.
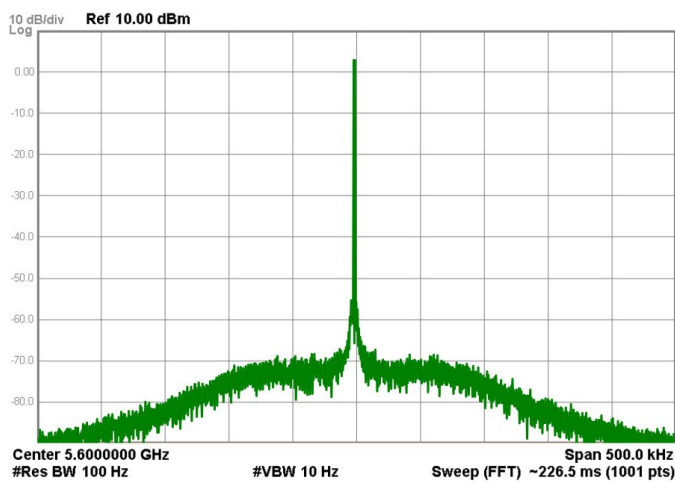

Figure 10. Spectrum of LO signal at the frequency of 5.6 GHz.

V. Conclusion

Two PLL synthesizers based on modern, wideband ADF5355 and HMC833 chips were described and compared hereabove. The HMC833 synthesizer is characterized by lower phase noise, but much higher level of harmonics and spurious.
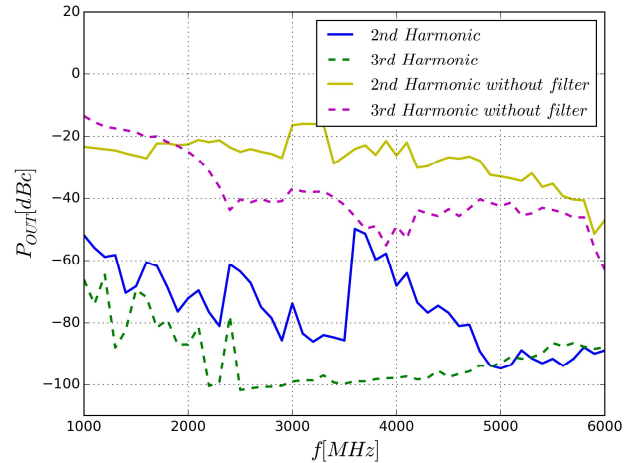

Figure 11. Harmonics levels of LO with and without output lowpass filters.

Furthermore, a relatively high subharmonic product appears while operating with fundamental signals above 3 GHz. Thus, the ADF5355 synthesizer followed by the switched bank of four low pass filters has been chosen as a more convenient solution to build a local oscillator for the 0-IF receiver. The LO block was redesigned, assembled (see Fig. 9) and optimized by means of PLL loop filter characteristic correction. The synthesizer is characterized within operating frequency range of 1 GHz to 6 GHz by phase noise better than -90 dBc @ 1 kHz and spurious products level lower than -75 dBc. The synthesizer fulfills all the requirements defined by a modern broadband receiver and its final version is used as a part of wideband 0-IF receiver frontend [9].

References

[1] Analog Devices, www.analog.com

[2] Gryglewski, D., Wojtasiak, W., "The microwave PLL/DDS for L band and S", Proceedings of Second National Conference of Electronics, Kolobrzeg, Poland, Jun.9-12, 2003, Vol. 1, pp. 295-300

[3] Rosołowski, D., Gryglewski, D., Korpas, P., Wojtasiak, W.,Modelski, J., „An Ultrawideband 1 to 6 GHz 0-IF Radio Receiver with 500 MHz of Instantaneous Bandwidth" MIKON 2016

[4] Kenington, Peter B. "RF and baseband techniques for software defined radio", Artech House on Demand, 2005.

[5] Linear Technology, LTC6946-4 datasheet

[6] Maxim Integrated, MAX2870 datasheet

[7] Abracon Corp., AOCJY OCXO oscillator datasheet

[8] Avago Technologies, MGA82563 datasheet

[9] Rosołowski, D., Gryglewski, D., Wojtasiak, W., Korpas, P., Modelski, J., and Bogdan, B., „A Wideband microwave receiver with direct 0-IF architecture", Telecommunication Review & Telecommunication News, Jun. 2015, LXXXIV, 6, 633–6