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ENSC 350 Final project part 1 report

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# Introduction

# LogicUnit

## Overview

The LogicUnit is responsible for selecting and operating Logic Bitwise operations of two 64-bit input signals, *A* and *B*. This design incorporates the following operations:

* Pass the signal of B
* The result of A xor B
* The result of A or B
* The result of A and B

These initial logical operations are computed immediately, with the results passed along by a multiplexer as signal *Y,* depending on the signal *LogicFn*. The block diagram of the LogicUnit is represented in Figure 1 and the truth table of the LogicUnit is indicated in Table 1. The VHDL representation is given in Figure 2.

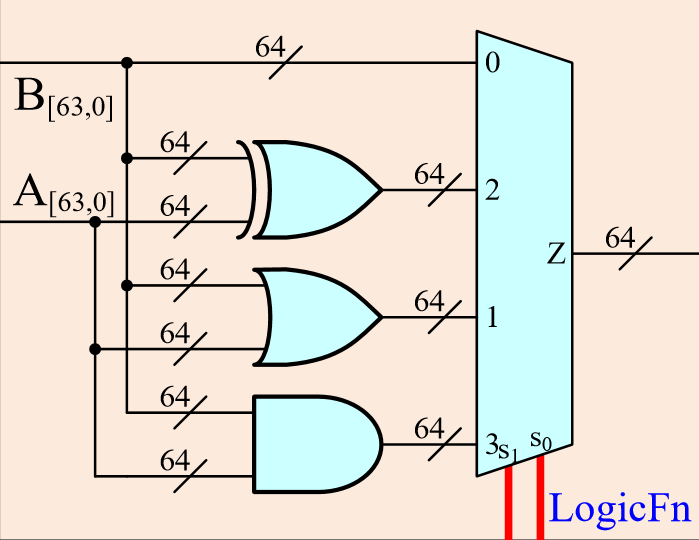


Figure 1: Block Diagram of LogicUnit Circuit

|  |  |
| --- | --- |
| **LogicFn Signal** | **Operation (Signal Y)** |
| 0 0 | B |
| 0 1 | A xor B |
| 1 0 | A or B |
| 1 1 | A and B |

Table 1: Truth Table of LogicUnit

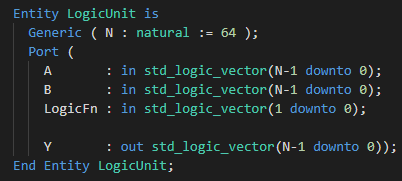


Figure 2: VHDL Interface of LogicUnit

## Functional Behaviour

The functional behaviour is given as

As indicated, the three logical diagrams are *XorGate*, *AndGate*, and *OrGate*. The VHDL interface for the three block diagrams and synthesised circuits are listed in Appendix A: Logic Gates.

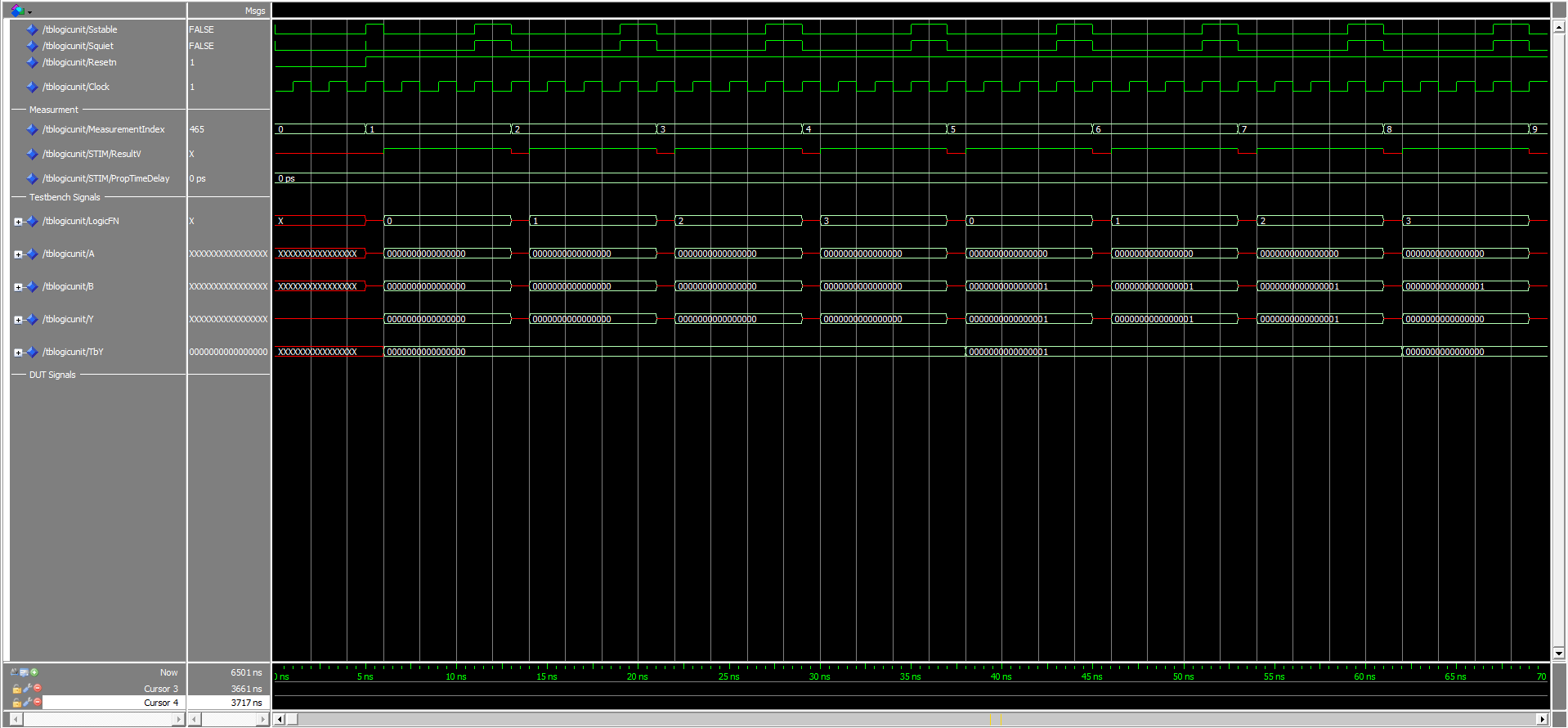


Figure 3: Functional Simulation for LogicUnit from t=0 to t=70ns

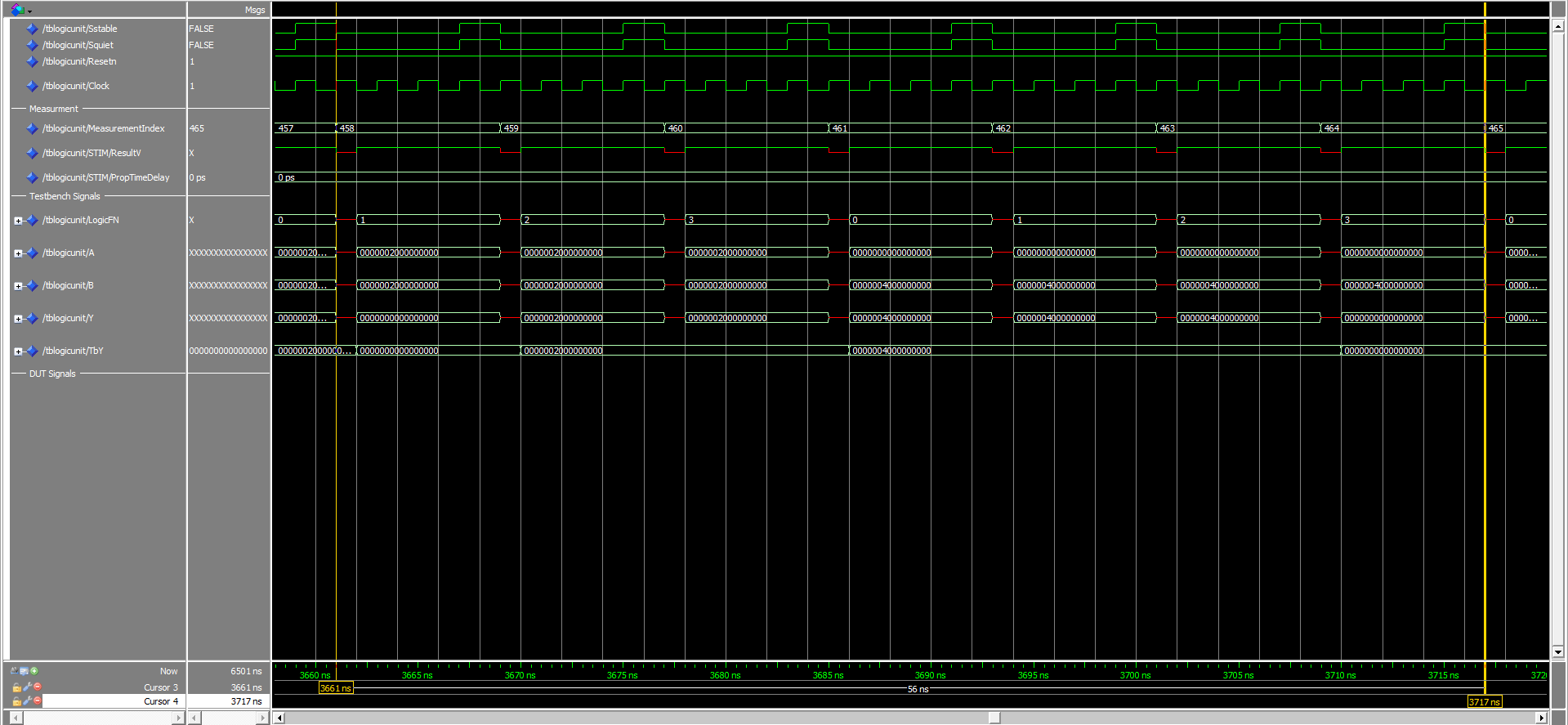


Figure 4: Functional Simulation for LogicUnit from measurement #458 to measurement #464

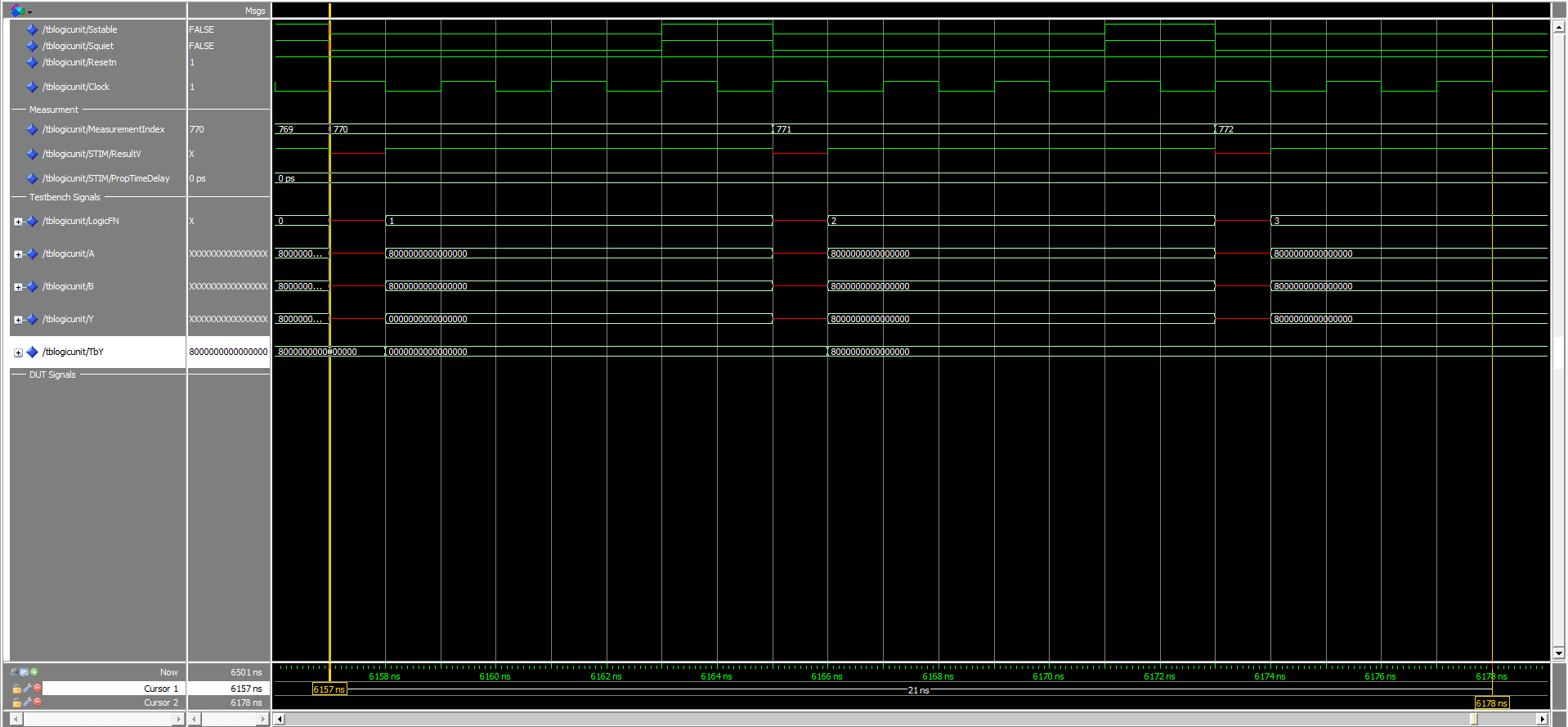


Figure 5: Functional Simulation for LogicUnit from measurement #770 to measurement #772

## Circuit Synthesis

## Timing Simulations

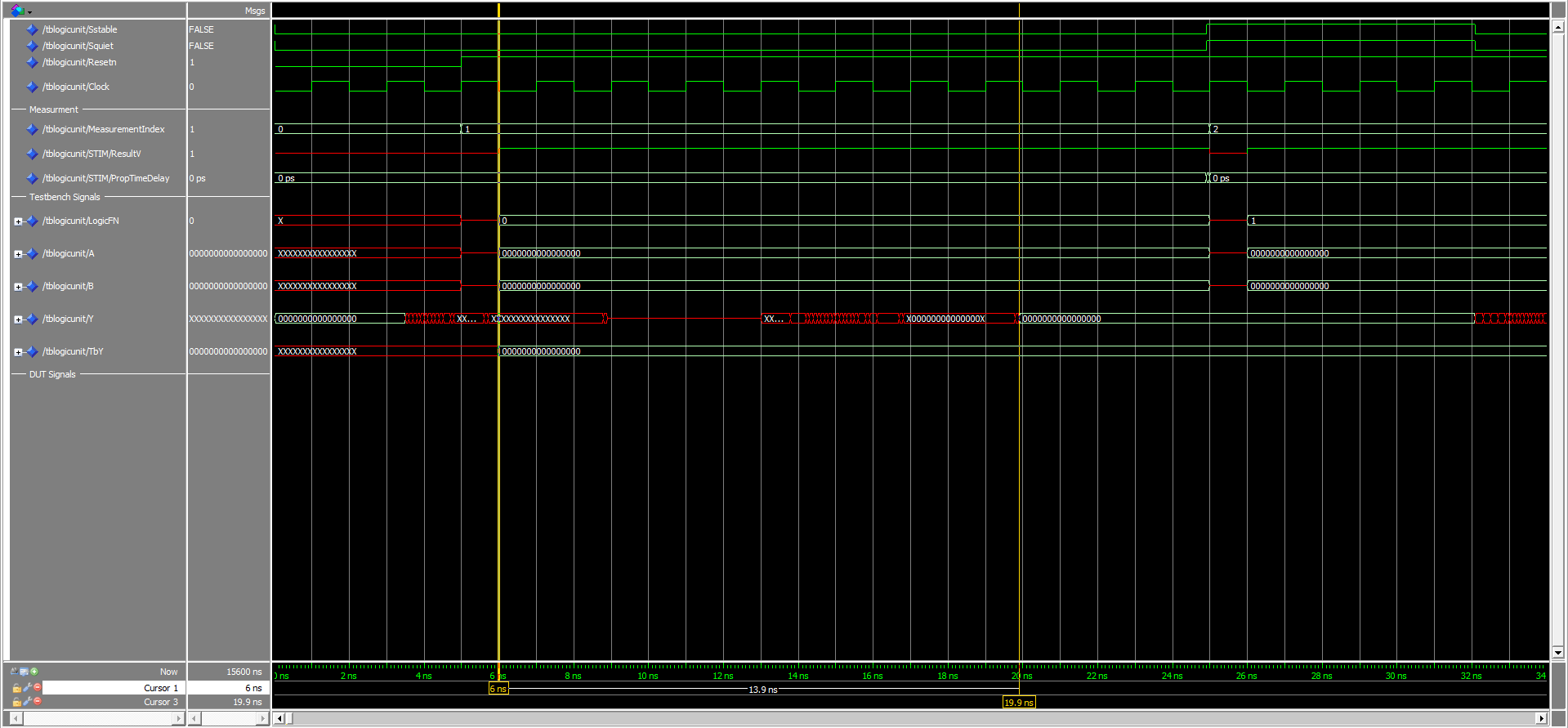


Figure 6: Timing Simulation for LogicUnit of Measurement #1

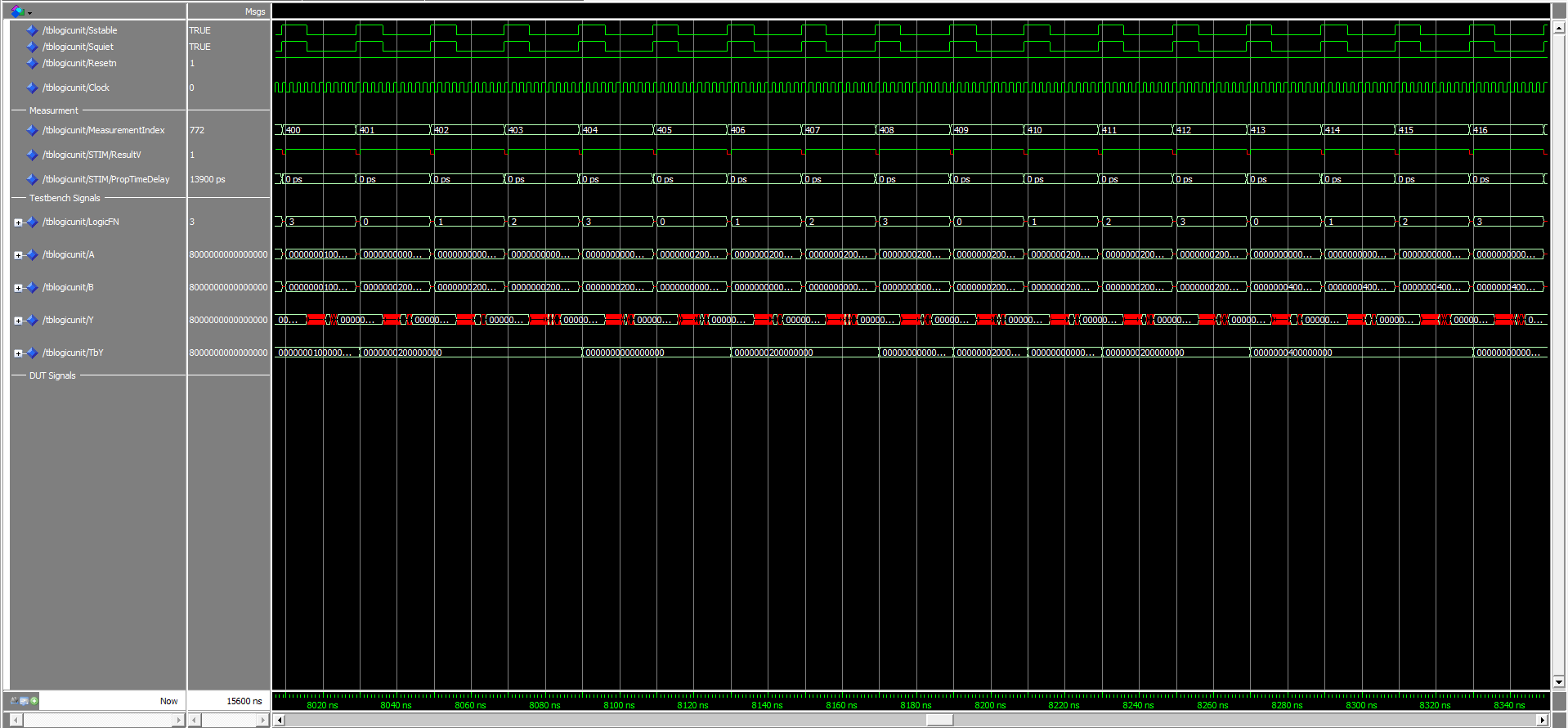


Figure 7: Timing Simulation for LogicUnit from measurement #400 to measurement #416

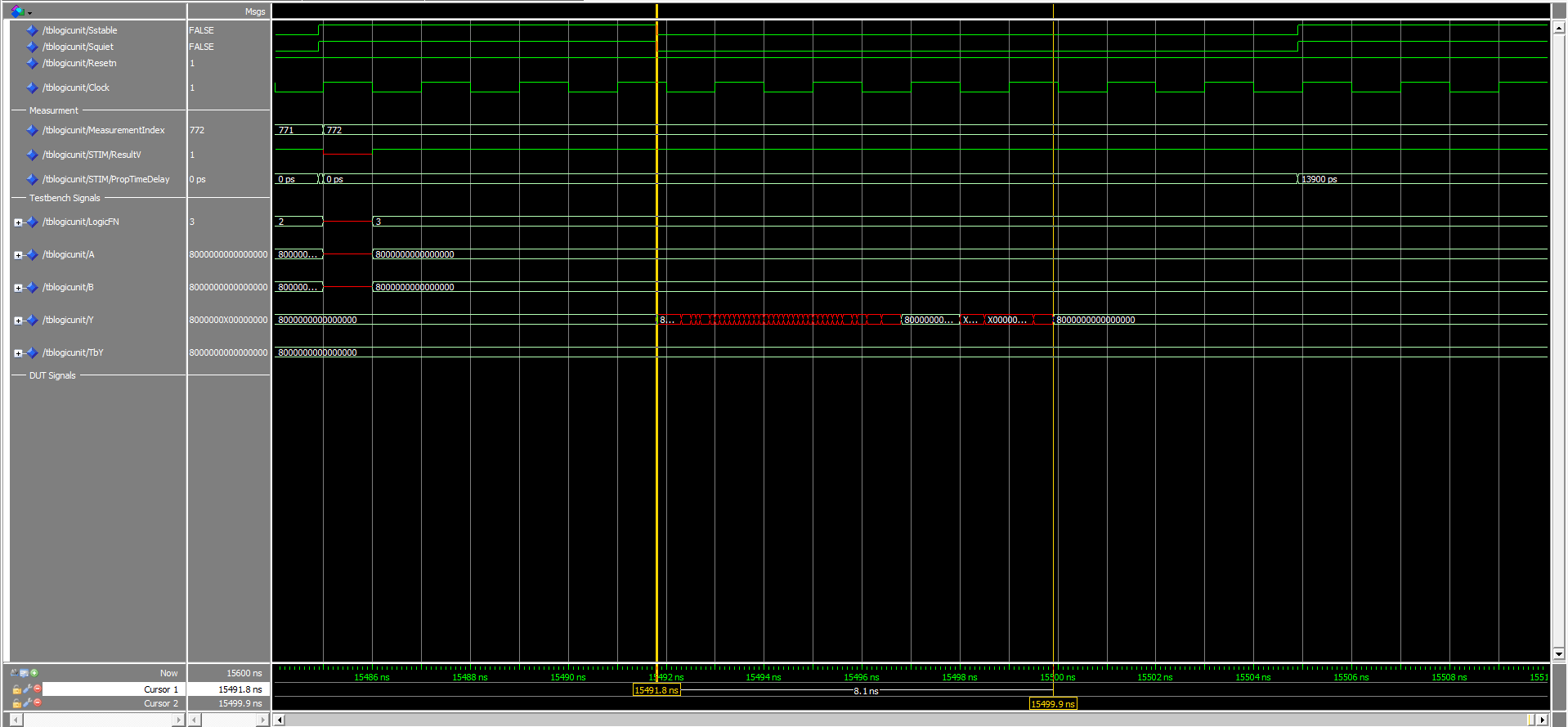


Figure 8: Timing Simulation for LogicUnit of Measurement #772

# Arithmetic Unit

# Conclusion

# References

**There are no sources in the current document.**

# Appendix

## Appendix A: Logic Gates

Inside the LogicUnit, the logic gates.

The operators *and*, *or* and *xor* are available in the IEEE standardised library. The logic gates entity interfaces and implementation for *AndGate*, *OrGate* and *XorGate* is represented in Figure 2, Figure 3 and Figure 4 respectively.

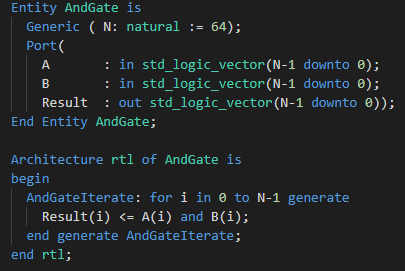


Figure 9: VHDL Interface and Implementation of AndGate

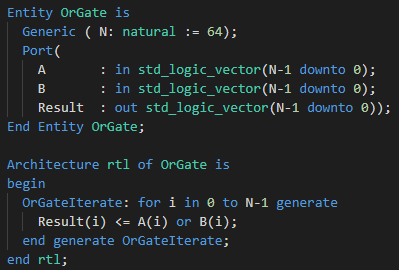


Figure 10: VHDL Interface and Implementation of OrGate

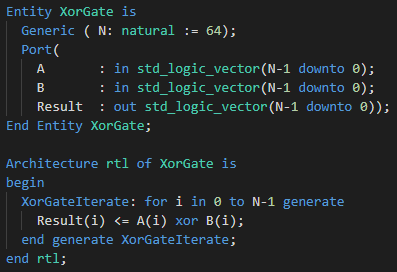


Figure 11: VHDL Interface and Implementation of XorGate

The VHDL Representation

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[Figure 4: VHDL Interface and Implementation of OrGate 4](#_Toc36938678)

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