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ENSC 350 Final project part 1 report

Table of Contents

[Introduction 2](#_Toc36937781)

[LogicUnit 2](#_Toc36937782)

[Overview 2](#_Toc36937783)

[VHDL Representation 2](#_Toc36937784)

[Circuit Synthesis 2](#_Toc36937785)

[Timing Simulations 2](#_Toc36937786)

[Conclusion 3](#_Toc36937787)

[References 3](#_Toc36937788)

[Appendix 3](#_Toc36937789)

[Logic Gates 3](#_Toc36937790)

[Table of Tables 4](#_Toc36937791)

[Table of Figures 4](#_Toc36937792)

# Introduction

# LogicUnit

# Overview

The LogicUnit is responsible for selecting and operating Logic Bitwise operations. The initial computation is done initially and the multiplexer, based on the signal *LogicFn*, selects which operation is passed. The block diagram is represented in Figure 1 and the truth table of the LogicUnit is indicated in Table 1.

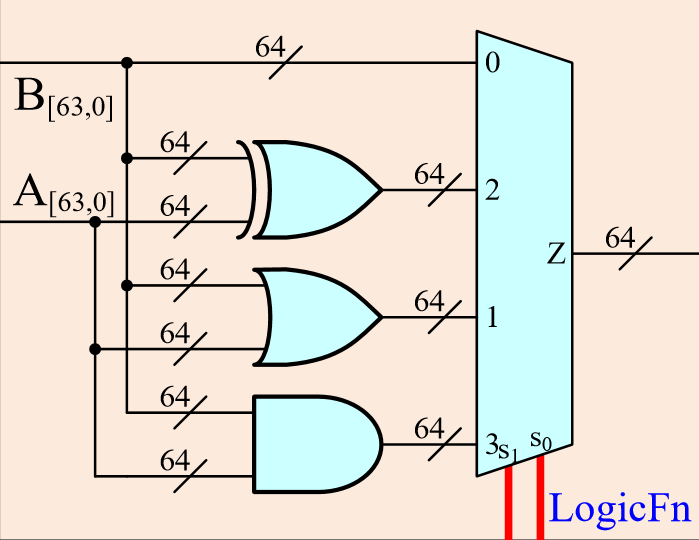


Figure 1: Block Diagram of LogicUnit Circuit

|  |  |
| --- | --- |
| **LogicFn Signal** | **Operation (Signal Y)** |
| 0 0 | B |
| 0 1 | A xor B |
| 1 0 | A orB |
| 1 1 | A and B |

Table 1: Truth Table of LogicUnit

## VHDL Representation

## Circuit Synthesis

## Timing Simulations

# Conclusion

# References

**There are no sources in the current document.**

# Appendix

## Logic Gates

Inside the LogicUnit, the logic gates.

The operators *and*, *or* and *xor* are available in the IEEE standardised library. The logic gates entity interfaces and implementation for *AndGate*, *OrGate* and *XorGate* is represented in Figure 2, Figure 3 and Figure 4 respectively.

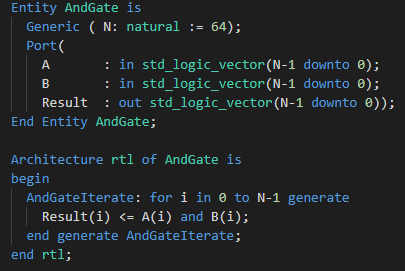


Figure 2: VHDL Interface and Implementation of AndGate

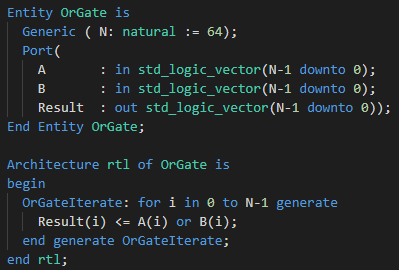


Figure 3: VHDL Interface and Implementation of OrGate

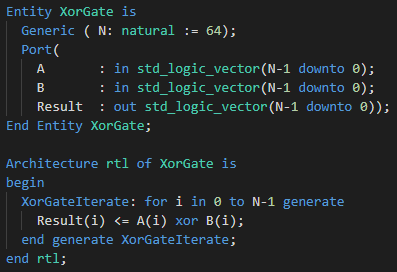


Figure 4: VHDL Interface and Implementation of XorGate

The VHDL Representation

# Table of Tables

[Table 1: Truth Table of LogicUnit 2](#_Toc36937774)

# Table of Figures

[Figure 1: Block Diagram of LogicUnit Circuit 2](#_Toc36937777)

[Figure 2: VHDL Interface and Implementation of AndGate 3](#_Toc36937778)

[Figure 3: VHDL Interface and Implementation of OrGate 4](#_Toc36937779)

[Figure 4: VHDL Interface and Implementation of XorGate 4](#_Toc36937780)