Choong Jin Ng | 301226977 | [jinn@sfu.ca](mailto:jinn@sfu.ca)

ENSC 350 Final project part 1 report

Table of Contents

[Introduction 2](#_Toc36938699)

[LogicUnit 2](#_Toc36938700)

[Overview 2](#_Toc36938701)

[Functional Behaviour 3](#_Toc36938702)

[Circuit Synthesis 3](#_Toc36938703)

[Timing Simulations 3](#_Toc36938704)

[Arithmetic Unit 3](#_Toc36938705)

[Conclusion 3](#_Toc36938706)

[References 3](#_Toc36938707)

[Appendix 3](#_Toc36938708)

[Appendix A: Logic Gates 3](#_Toc36938709)

[Table of Tables 5](#_Toc36938710)

[Table of Figures 5](#_Toc36938711)

# Introduction

# LogicUnit

## Overview

The LogicUnit is responsible for selecting and operating Logic Bitwise operations of two 64-bit input signals, *A* and *B*. This design incorporates the following operations:

* Pass the signal of B
* The result of A xor B
* The result of A or B
* The result of A and B

These initial logical operations are computed immediately, with the results passed along by a multiplexer as signal *Y,* depending on the signal *LogicFn*. The block diagram of the LogicUnit is represented in Figure 1 and the truth table of the LogicUnit is indicated in Table 1. The VHDL representation is given in Figure 2.

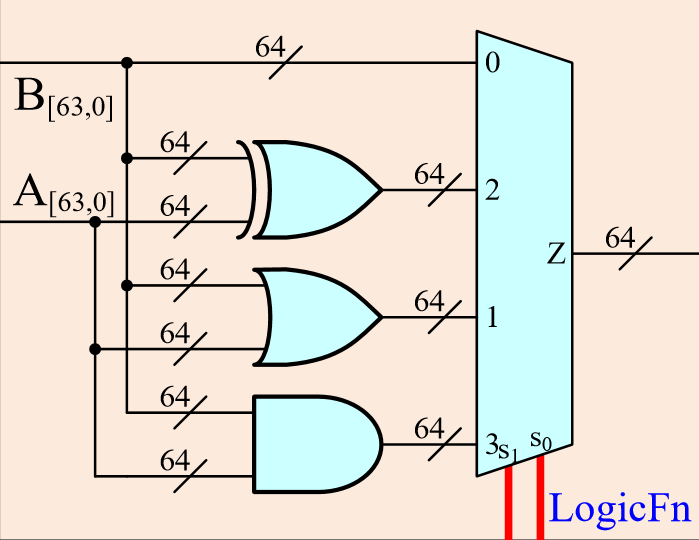


Figure 1: Block Diagram of LogicUnit Circuit

|  |  |
| --- | --- |
| **LogicFn Signal** | **Operation (Signal Y)** |
| 0 0 | B |
| 0 1 | A xor B |
| 1 0 | A or B |
| 1 1 | A and B |

Table 1: Truth Table of LogicUnit

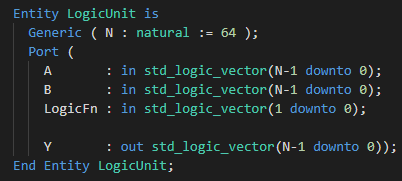


Figure 2: VHDL Interface of LogicUnit

## Functional Behaviour

The functional behaviour of LogicUnit can be demonstrated in three example diagrams Figure 3, Figure 4 and Figure 5. In Figure 3, the different *LogicFn* signals are demonstrated.

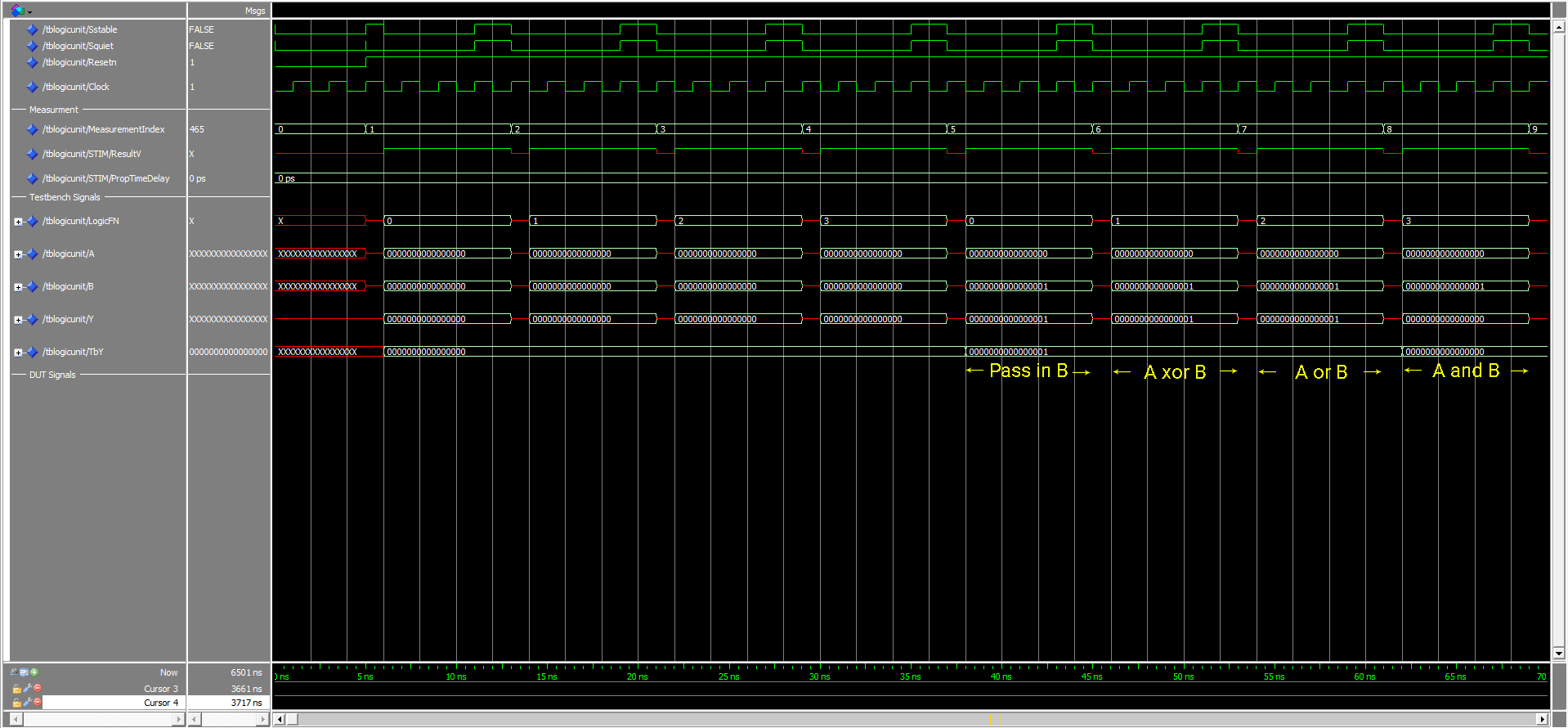


Figure 3: Functional Simulation for LogicUnit from t=0 to t=70ns

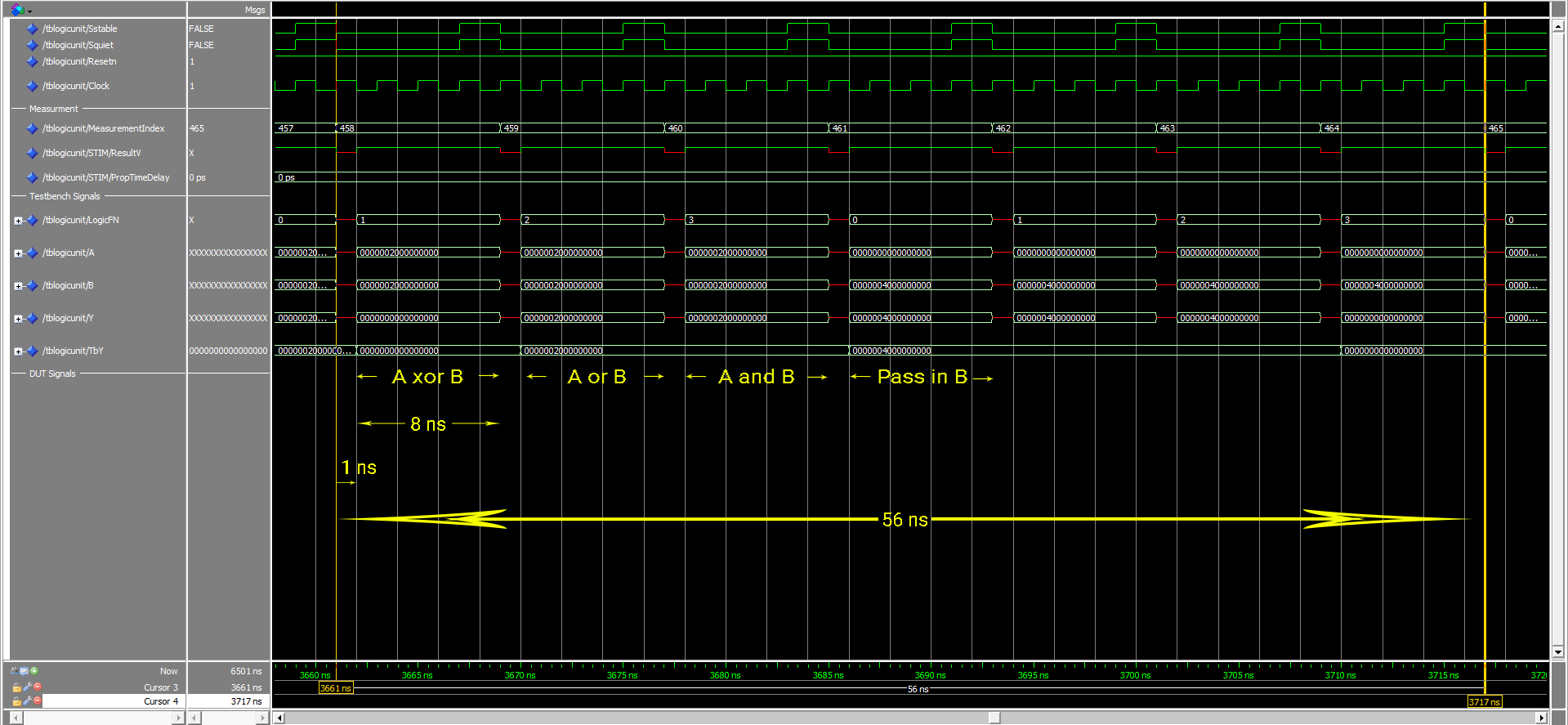


Figure 4: Functional Simulation for LogicUnit from measurement #458 to measurement #464

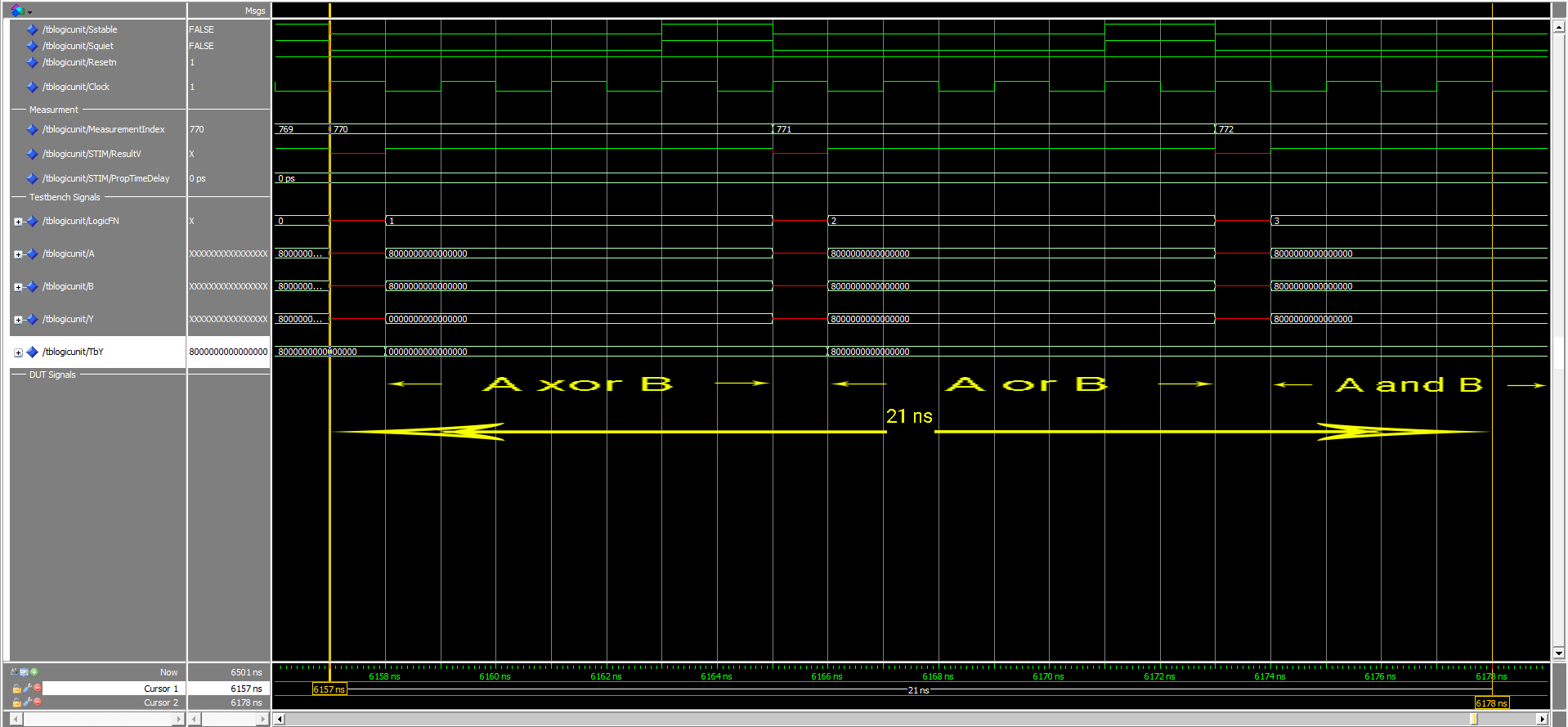


Figure 5: Functional Simulation for LogicUnit from measurement #770 to measurement #772

## Circuit Synthesis

As indicated, the three logical diagrams are *XorGate*, *AndGate*, and *OrGate*. The VHDL interface for the three block diagrams and synthesised circuits are listed in Appendix A: Logic Gates.

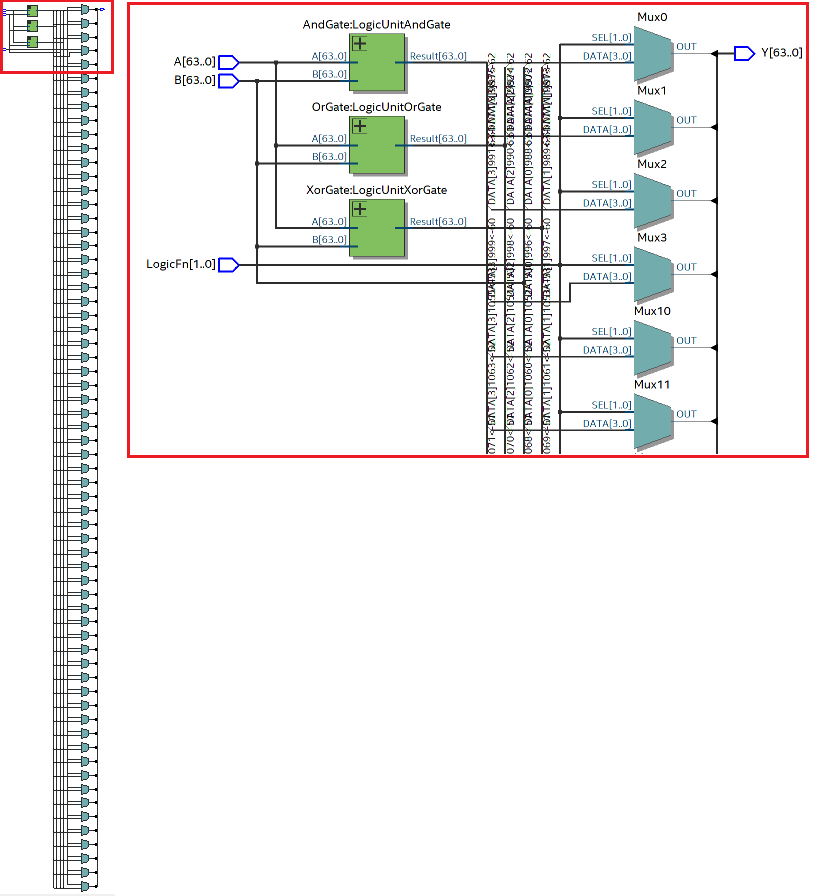


Figure 6: Synthesised Circuit of LogicUnit

## Timing Simulations

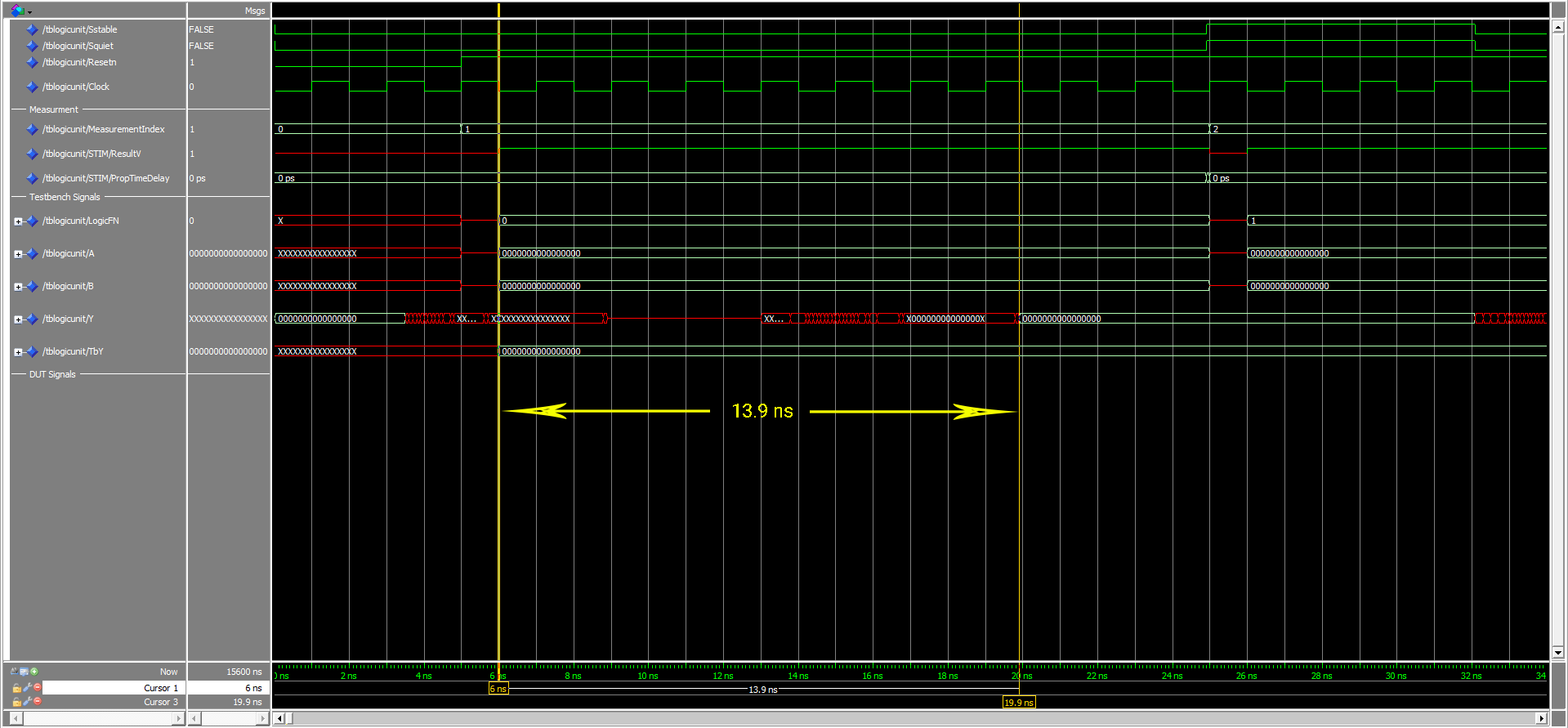


Figure 7: Timing Simulation for LogicUnit of Measurement #1

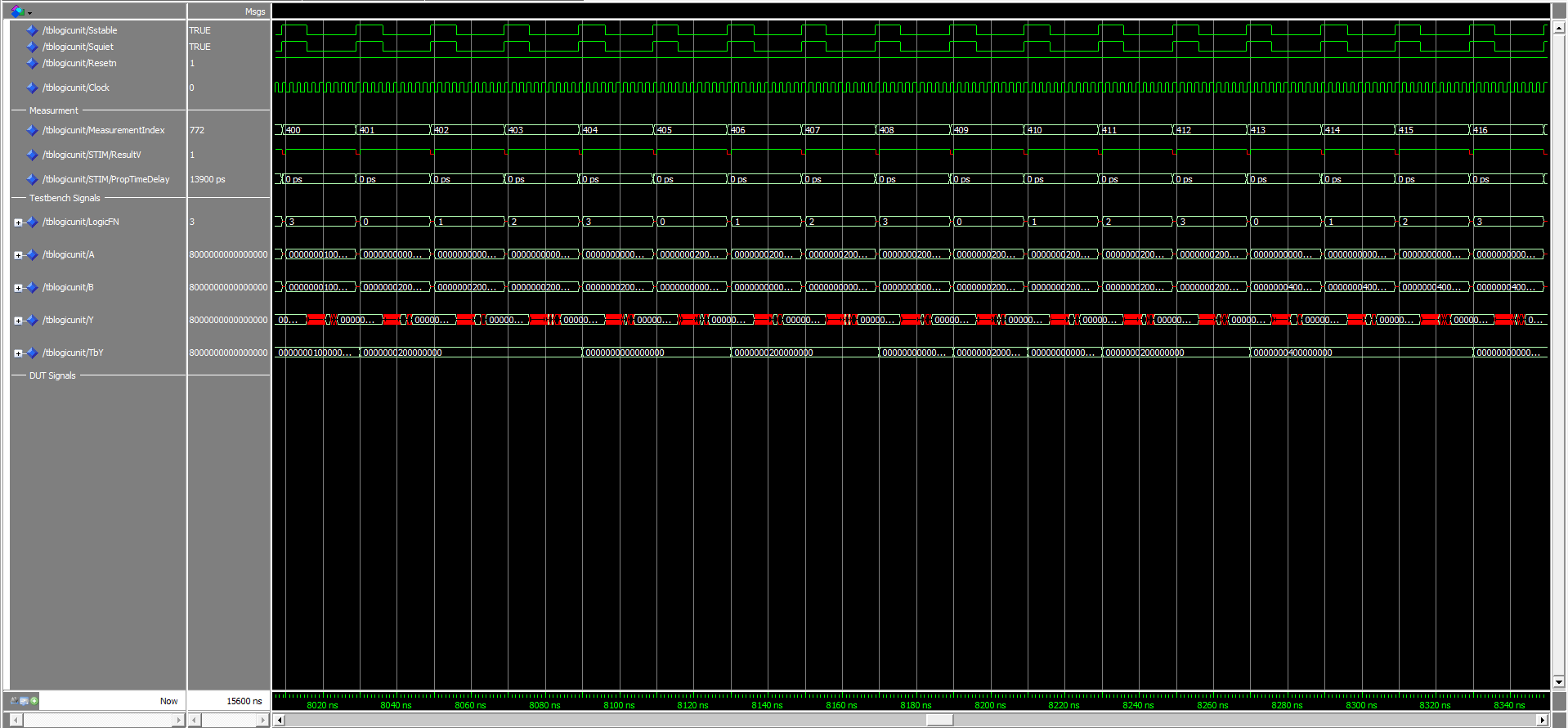


Figure 8: Timing Simulation for LogicUnit from measurement #400 to measurement #416

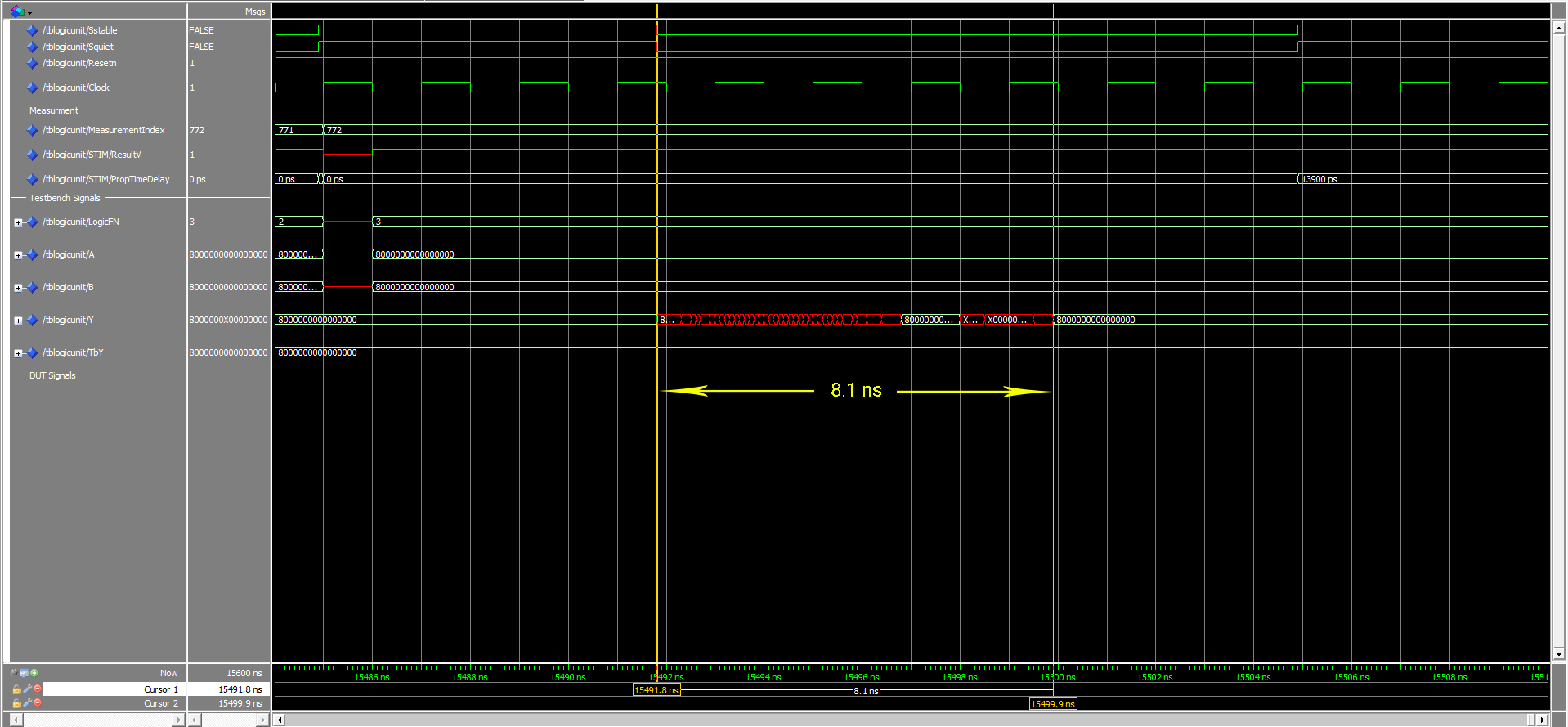


Figure 9: Timing Simulation for LogicUnit of Measurement #772

# Arithmetic Unit

# Conclusion

# Appendix

## Appendix A: Logic Gates

Inside the LogicUnit, the logic gates.

The operators *and*, *or* and *xor* are available in the IEEE standardised library. The logic gates entity interfaces and implementation for *AndGate*, *OrGate* and *XorGate* is represented in Figure 2, Figure 3 and Figure 4 respectively.

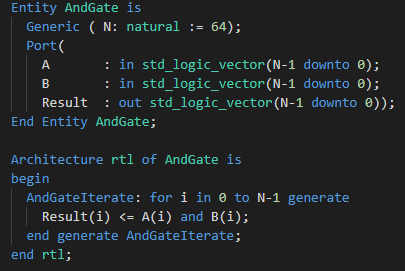


Figure 10: VHDL Interface and Implementation of AndGate

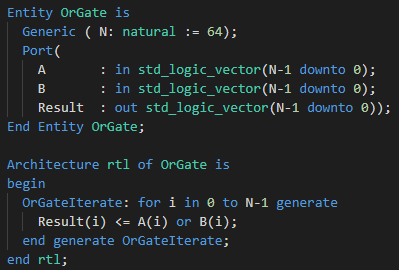


Figure 11: VHDL Interface and Implementation of OrGate

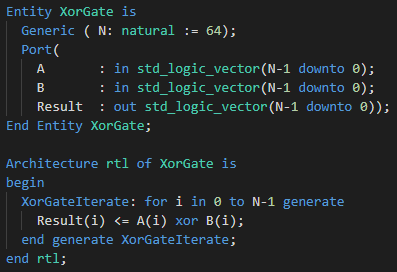


Figure 12: VHDL Interface and Implementation of XorGate

The synthesised circuits are represented in Figure 12.

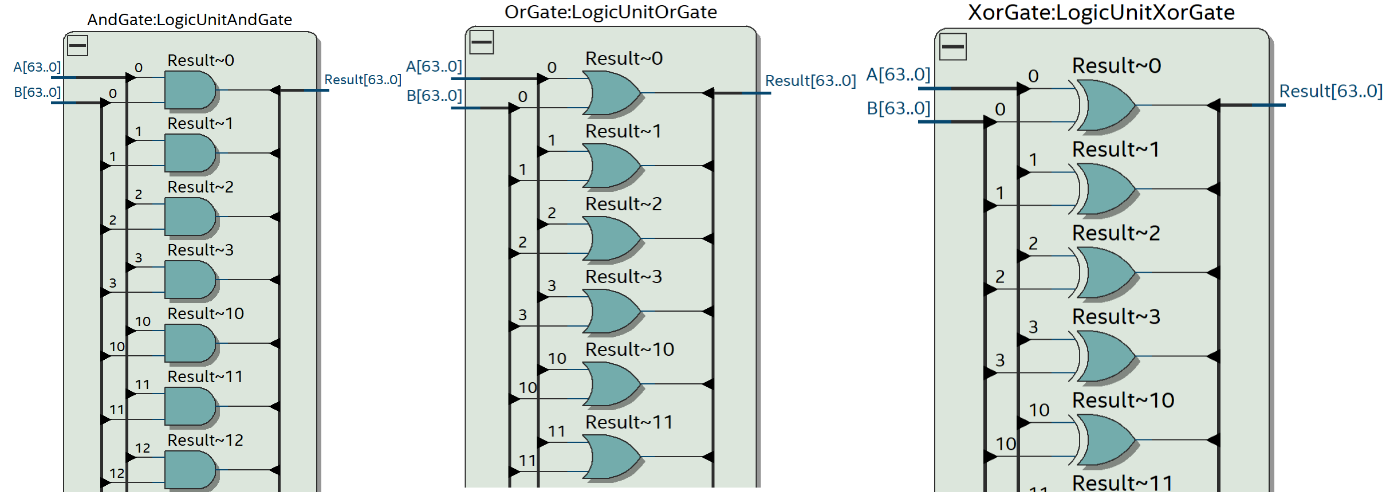


Figure 13: Synthesised Circuits of AndGates, OrGates and XorGates respectively

# Table of Tables

[Table 1: Truth Table of LogicUnit 2](#_Toc36938680)

# Table of Figures

[Figure 1: Block Diagram of LogicUnit Circuit 2](#_Toc36950651)

[Figure 2: VHDL Interface of LogicUnit 3](#_Toc36950652)

[Figure 3: Functional Simulation for LogicUnit from t=0 to t=70ns 3](#_Toc36950653)

[Figure 4: Functional Simulation for LogicUnit from measurement #458 to measurement #464 3](#_Toc36950654)

[Figure 5: Functional Simulation for LogicUnit from measurement #770 to measurement #772 4](#_Toc36950655)

[Figure 6: Timing Simulation for LogicUnit of Measurement #1 4](#_Toc36950656)

[Figure 7: Timing Simulation for LogicUnit from measurement #400 to measurement #416 5](#_Toc36950657)

[Figure 8: Timing Simulation for LogicUnit of Measurement #772 5](#_Toc36950658)

[Figure 9: VHDL Interface and Implementation of AndGate 6](#_Toc36950659)

[Figure 10: VHDL Interface and Implementation of OrGate 6](#_Toc36950660)

[Figure 11: VHDL Interface and Implementation of XorGate 7](#_Toc36950661)

[Figure 12: Synthesised Circuits of AndGates, OrGates and XorGates respectively 7](#_Toc36950662)