CARTER NESBITT

Computer Engineering

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EDUCATION

Bachelor's of Science - GPA: 3.99

Rochester Institute of Technology

Graduating June 2022

EXPERIENCE

Firmware Engineering Intern

Positive Science

Feb 2019 – Aug 2019 Rochester, NY

- Research, development and integration of various sensors and components onto an embedded system.
- Worked on a small team to diagnose and resolve issues in both software and hardware that cause device failures.
- Leading firmware development, device diagnostics and research of system during internship.
- Experience with internal and wireless communications, operating systems, and constraints associated with embedded systems.

Orientation Programming Assistant

Rochester Institute of Technology

Mar 2019 – Aug 2019 Rochester, NY

- Organized and maintained a welcoming campus for new students arriving at RIT.
- Setup and supervised many events that took place during RIT's orientation week.
- Collaborated with a close team to maintain a reputable New Student Orientation program at RIT.

Orientation Leader

Rochester Institute of Technology

August 2018 Rochester, NY

- Provided guidance to a group of new students during their first weeks at university.
- Gave advice with respect to college life and critical habits to new students to aid in their personal development at RIT.
- Functioned as part of the public view of RIT under the New Student Orientation program.

ACHIEVEMENTS

- Maintained Dean's List at RIT every semester, beginning Fall 2017.
- Computer Engineering Department GPA of 4.0

OBJECTIVE

Secure a computer engineering internship from Spring 2020 through Summer 2020.

PROJECTS

MIPS-I VHDL Implementation

Feb 2019 - Present

- Continued implementation of the MIPS ISA, previously started as an in-lab project.
- Developed in VHDL to be programmed onto an FPGA development board.
- Hazard detection, forwarding, interrupts, instruction programming and I/O actively being developed.

NES Emulator

Dec 2018 - Present

- Replication of Nintendo Entertainment System hardware in software.
- Proper emulation of the MOS 6502 CPU with a partially complete 2C02 PPU co-processor.
- Developed in the C language, including a reimagination of the picture display using the SDL2 library.

STRENGTHS

FPGA | Embedded System Applications | Hardware Testing and Verification | Digital System Design | Computer Architecture Design

LANGUAGES

C
Python
VHDL
ARM Assembly
MIPS
Verilog