











SN74HC595B

SCLS751 - MARCH 2016

SN74HC595B 8-Bit Shift Registers With 3-State Output Registers

Features

- 8-Bit Serial-In, Parallel-Out Shift Registers
- Available in Ultra Small Logic QFN package(0.5 mm max height)
- Over-Voltage Tolerant on Inputs Independent of
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Low Power Consumption: 80-µA (Maximum) I_{CC}
- $t_{pd} = 13 \text{ ns (Typical)}$
- ±6-mA Output Drive at 5 V
- Low Input Current: 1 µA (Maximum)
- Shift Register Has Direct Clear
- -55°C to 125°C Operating Temperature

Applications

- **Network Switches**
- **Factory Automation**
- Mobile Wearables
- Industrial Building Automation
- Power Infrastructure
- LED Displays
- Servers

3 Description

The SN74HC595B devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3state outputs. Separate clocks are provided for both the shift register and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (\overline{OE}) input is high, the all outputs are in the high-impedance state except Q_H.

Table 1. Device Information

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)		
SN74HC595BRWN	X1QFN (16)	2.50 mm x 2.50 mm		

(1) For available package, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

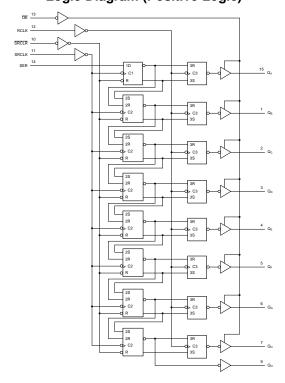




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4 Pin Configuration and Functions

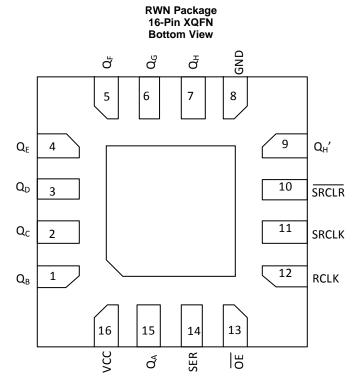


Table 2. Pin Functions

	PIN	1/0	DESCRIPTION		
NAME	RWN	I/O			
GND	8	_	Ground Pin		
ŌĒ	13	1	Output Enable; does not control Q _H		
Q _A	15	0	Q _A Output		
Q_B	1	0	Q _B Output		
Q_C	2	0	Q _C Output		
Q_D	3	0	Q _D Output		
Q _E	4	0	Q _E Output		
Q_{F}	5	0	Q _F Output		
Q_G	6	0	Q _G Output		
Q _H	7	0	Q _H Output		
Q _H '	9	0	Q _H Output		
RCLK	12	1	RCLK Input		
SER	14	I	SER Input		
SRCLK	11	I	SRCLK Input		
SRCLR	10	I	SRCLR Input		
V _{CC}	16	_	Power Pin		

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TEXAS INSTRUMENTS

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
V_{I}	Input voltage	-0.5	7	V	
I _{IK}	Input clamp current ⁽¹⁾	V _I < 0		-20	mA
lok	Output clamp current (2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V _{CC} or GND		±70	mA	
TJ	Junction temperature		150	°C	
T _{stg}	Storage temperature	-65	150	°C	

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000		
\	V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN	74HC595B		LINUT
		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage		2	5	6	V
		V _{CC} = 2 V	1.5			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			V
		V _{CC} = 6 V	4.2			
	Low-level input voltage	V _{CC} = 2 V			0.5	
V_{IL}		V _{CC} = 4.5 V			1.35	V
		V _{CC} = 6 V			1.8	
VI	Input voltage		0		V _{CC}	V
Vo	Output voltage		0		V_{CC}	V
		V _{CC} = 2 V			1000	
Δt/Δν	Input transition rise or fall time (2)	V _{CC} = 4.5 V			500	ns
		V _{CC} = 6 V			400	
T _A	Operating free-air temperature		-55		125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

⁽²⁾ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

⁽²⁾ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



5.4 Thermal Information

		SN74HC595B	
	THERMAL METRIC ⁽¹⁾	RWN (X1QFN)	UNIT
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112	
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	47.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.6	*C/VV
ΨЈВ	Junction-to-board characterization parameter	72.4	
R _{0JCbot}	Junction-to-case (bottom) thermal resistance	32.2	

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		T 001/01/01/0	V _{cc}	Т	_A = 25°C		T _A = -55°C t	o 125°C	T _A = -40°C to 85°C		
PARAMETER	IES	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
V _{OH}	$V_{I} = V_{IH} \text{ or } V_{IL}$	$Q_{H'}$, $I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		V
		$Q_A - Q_H$, $I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$Q_{H'}$, $I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
		$Q_A - Q_H$, $I_{OH} = -7.8 \text{ mA}$		5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
	$V_{I} = V_{IH}$ or V_{IL}	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
V_{OL}		$Q_{H'}$, $I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	V
		$Q_A - Q_H$, $I_{OL} = 6 \text{ mA}$			0.17	0.26		0.4		0.33	
		$Q_{H'}$, $I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
		$Q_A - Q_H$, $I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	$V_O = V_{CC}$ or 0, $Q_A - Q_H$		6 V		±0.01	±0.5		±10		±5	μΑ
Icc	$V_I = V_{CC}$ or 0, I_C) = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF



TEXAS INSTRUMENTS

5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			.,	T _A = 2	5°C	$T_A = -55^{\circ}C$ to	125°C	$T_A = -40^{\circ}C$ to	85°C	
			V _{CC}	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		6		4.2		5	
f _{clock}	Clock frequency		4.5 V		31		21		25	MHz
			6 V		36		25		29	
			2 V	80		120		100		
		SRCLK or RCLK high or low	4.5 V	16		24		20		
	Pulse		6 V	14		20		17		
t _w	duration	SRCLR low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		SER before SRCLK↑	2 V	100		150		125		
			4.5 V	20		30		25		
			6 V	17		25		21		
		SRCLK↑ before RCLK↑ ⁽¹⁾	2 V	75		113		94		
			4.5 V	15		23		19		
	0.1		6 V	13		19		16		
t _{su}	Set-up time		2 V	50		75		65		ns
		SRCLR low before RCLK↑	4.5 V	10		15		13		
			6 V	9		13		11		
			2 V	50		75		60		
		SRCLR high (inactive) before SRCLK↑	4.5 V	10		15		12		
			6 V	9		13		11		
			2 V	0		0		0		
t _h	Hold time, SI	ER after SRCLK↑	4.5 V	0		0		0		ns
			6 V	0		0		0		

⁽¹⁾ This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.



5.7 Switching Characteristics

Over recommended operating free-air temperature range.

PARAMETER	FROM	TO (OUTPUT)	LOAD CAPACITANCE	V _{cc}	T,	₄ = 25°	С	T _A = -55 125°	S°C to	T _A = -40 85°0	°C to	UNIT	
	(INPUT)	(001701)	CAPACITANCE		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
				2 V	6	26		4.2		5			
f _{max}			50 pF	4.5 V	31	38		21		25		MHz	
				6 V	36	42		25		29			
				2 V		50	160		240		200		
	SRCLK	$Q_{H'}$	50 pF	4.5 V		17	32		48		40		
				6 V		14	27		41		34		
t _{pd}				2 V		50	150		225		187	ns	
	RCLK	$Q_A - Q_H$	50 pF	4.5 V		17	30		45		37		
				6 V		14	26		38		32		
				2 V		51	175		261		219		
t _{PHL}	SRCLR	$Q_{H'}$	50 pF	4.5 V		18	35		52		44	ns	
				6 V		15	30		44		37		
					2 V		40	150		255		187	
t _{en}	ŌĒ	$Q_A - Q_H$	50 pF	4.5 V		15	30		45		37	ns	
				6 V		13	26		38		32		
				2 V		42	200		300		250		
t _{dis}	ŌE	$Q_A - Q_H$	50 pF	4.5 V		23	40		60		50	ns	
				6 V		20	34		51		43		
				2 V		28	60		90		75		
		$Q_A - Q_H$	50 pF	4.5 V		8	12		18		15		
				6 V		6	10		15		13		
t _t				2 V		28	75		110		95	ns	
		$Q_{H'}$	50 pF	4.5 V		8	15		22		19		
				6 V		6	13		19		16		
				2 V		60	200		300		250		
t _{pd}	RCLK	$Q_A - Q_H$	150 pf	4.5 V		22	40		60		50	ns	
				6 V		19	34		51		43		
				2 V		70	200		298		250		
t _{en}	ŌĒ	$Q_A - Q_H$	150 pf	4.5 V		23	40		60		50	ns	
				6 V		19	34		51		43		
				2 V		45	210		315		265		
t _t		$Q_A - Q_H$	150 pf	4.5 V		17	42		63		53	ns	
				6 V		13	36		53		45		

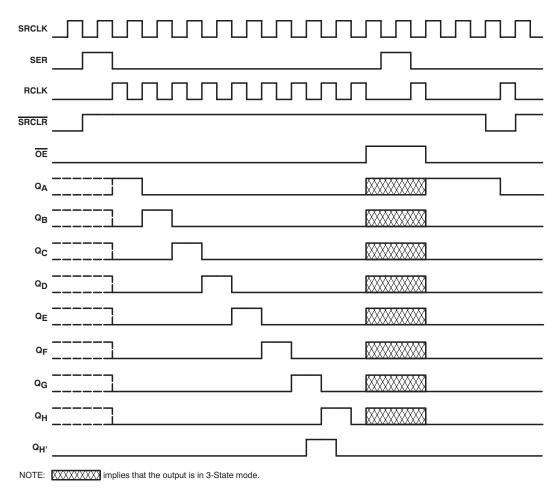


Figure 1. Timing Diagram

5.8 Operating Characteristics

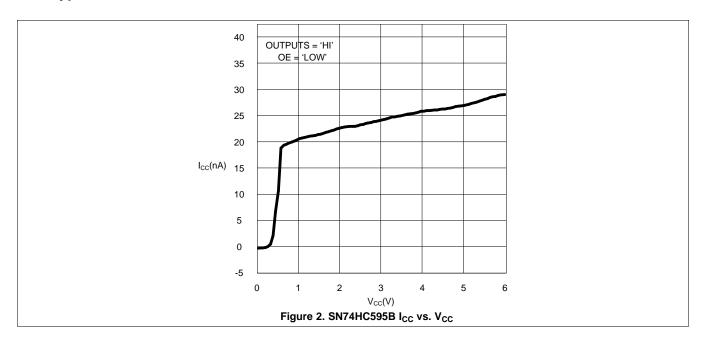
 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	400	pF

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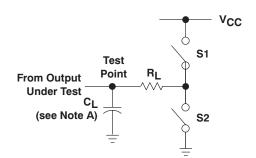


5.9 Typical Characteristics

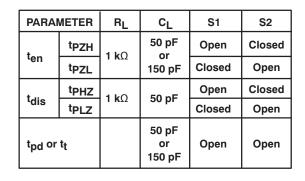


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6 Parameter Measurement Information



LOAD CIRCUIT



ISTRUMENTS

VCC

≈Vcc

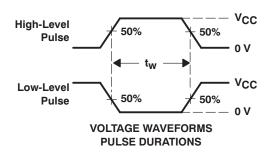
VOL

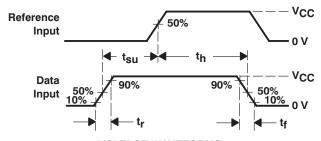
۷он

≈0 V

tpi 7

^tPHZ





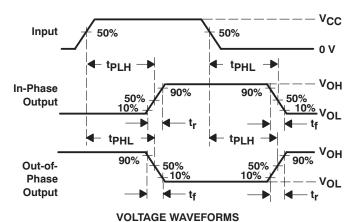
VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES

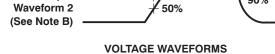
≈VCC

50%

ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

50%





PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 6 \ ns$, $t_f = 6 \ ns$.

Output

Control

Output

Output

tpzL

tp7H

(Low-Level Enabling)

Waveform 1

(See Note B)

- D. For clock inputs, $f_{\mbox{max}}$ is measured when the input duty cycle is 50%.
- E. The outputs are measured one at a time, with one input transition per measurement.
- F. tpLz and tpHz are the same as tdis.
- G. tpzI and tpzH are the same as ten.
- H. tpLH and tpHL are the same as tpd.

Figure 3. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

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The SN74HC595B is part of the HC family of logic devices intended for CMOS applications. The SN74HC595B device is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register. The Q_{H'} may be used for daisy chaining the device and will not go into high impedance when \overline{OE} is asserted.

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TEXAS INSTRUMENTS

7.2 Functional Block Diagram

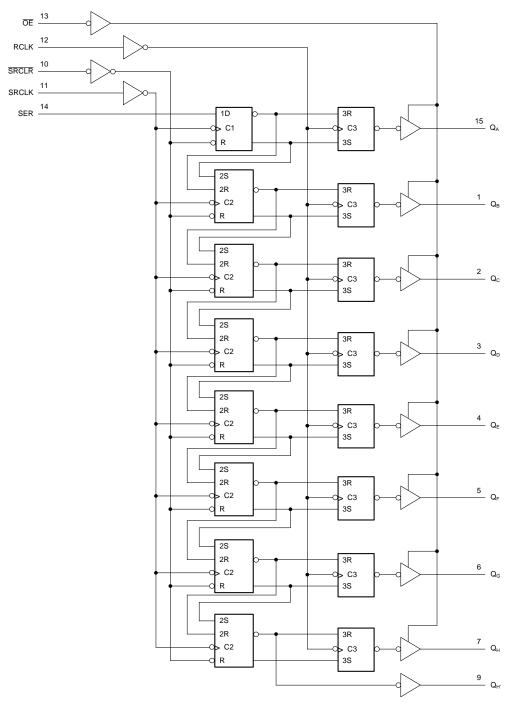


Figure 4. Logic Diagram (Positive Logic)

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7.3 Feature Description

The SN74HC595B device is an 8-bit Serial-In, Parallel-Out shift register. It has a wide operating voltage of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The device has a low power consumption of 80- μ A (Maximum) I_{CC}. Additionally, this device has a low input current of 1 μ A (Maximum) and a \pm 6-mA output drive at 5 V. The device is available currently in the smallest logic QFN package at 0.5 mm max height with 0.4 mm pitch. The inputs are over voltage tolerant independent of V_{cc}.

7.4 Device Functional Modes

Table 3 lists the functional modes of the SN74HC595B devices.

Table 3. Function Table

		INPUTS			FUNCTION
SER	SRCLK	SRCLR	RCLK	ŌĒ	FUNCTION
_	_	-	-	Н	Outputs $Q_A - Q_H$ are disabled. $Q_{H'}$ is active .
_	_	-	-	L	Outputs Q _A – Q _H are enabled.
_	-	L	_	_	Shift register is cleared.
L	1	Н	_	_	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
Н	1	Н	-	-	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
_	-	-	1	_	Shift-register data is stored in the storage register.

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NSTRUMENTS

Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74HC595B is a low-drive CMOS device that is used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. Q_H pin of the first register should be connected to the serial (SER) pin of the second register for daisy chaining.

8.2 Typical Application

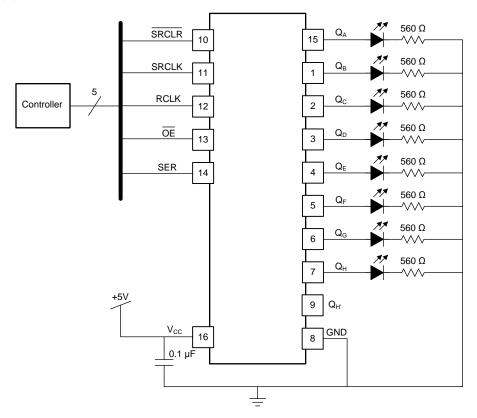


Figure 5. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has a balanced output drive. Take care to avoid bus contention because it can drive currents in excess of the maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended input conditions
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Specified high and low levels. See (V_{IH} and V_{II}) in the Recommended Operating Conditions table.

Product Folder Links: SN74HC595B

Inputs are over-voltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}

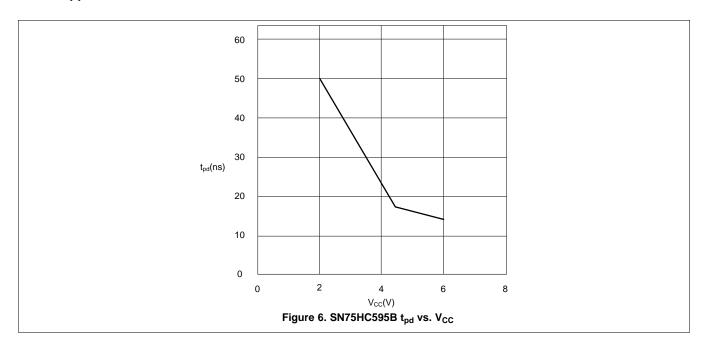
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Typical Application (continued)

- · Recommended output conditions
 - Load currents should not exceed 35 mA per output as per the *Absolute Maximum Ratings* table.
 - $-\,\,$ Outputs should not be pulled below Ground or above V_{CC}

8.2.3 Application Curves



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9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table. The total current through Ground or Vcc should not exceed 70 mA as per *Absolute Maximum Ratings* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ f is recommended; if there are multiple V_{CC} pins, then 0.01 μ f or 0.022 μ f is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ f and a 1 μ f are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

10 Layout

10.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 7 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or $V_{\rm CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

10.2 Layout Example

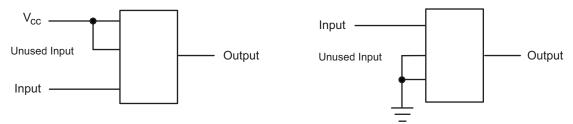


Figure 7. Layout Diagram



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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following: Implications of Slow or Floating CMOS Inputs, SCBA004

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.



PACKAGE OPTION ADDENDUM

11-Mar-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC595BRWNR	ACTIVE	X1QFN	RWN	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	13YI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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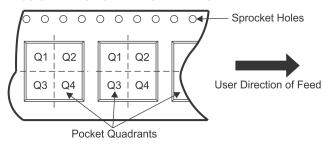
TAPE AND REEL INFORMATION





A0	
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC595BRWNR	X1QFN	RWN	16	2000	178.0	13.5	2.8	2.8	0.75	8.0	12.0	Q1

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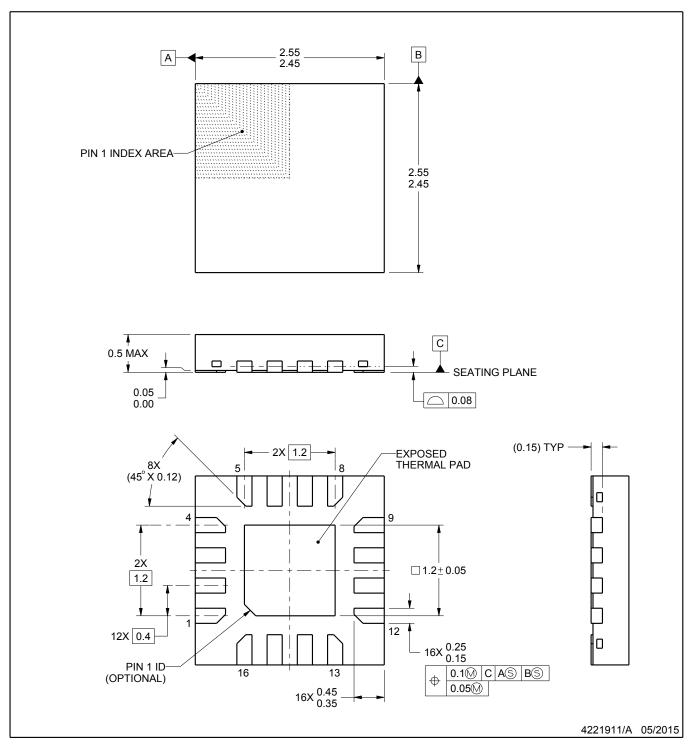


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74HC595BRWNR	X1QFN	RWN	16	2000	189.0	185.0	36.0	



PLASTIC QUAD FLATPACK - NO LEAD

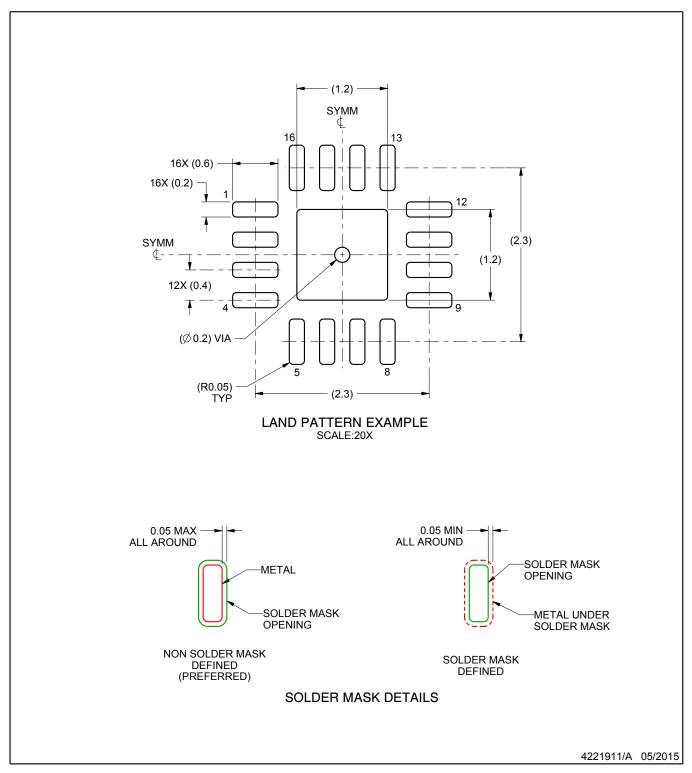


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

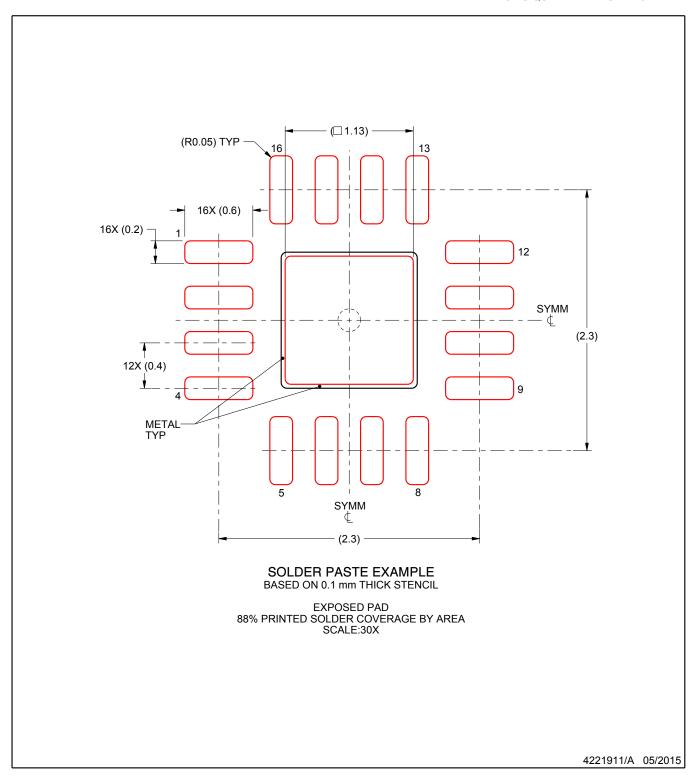


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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