

EinsyRetro 1.0a  
UltiMachine  
10/30/2017

0.3a Revision Summary (for detailed infomation goto: <https://github.com/ultimachine/Einsy-Rambo/tree/0.3a>)

- Added TVS and over-voltage protection to select nets
- Added and corrected testpoints
- Added "XTRA0" net between 32U2 and 2560
- Removed via tenting underneath QFNs and other flat solder lug/heatsink primitives
- Added teardrops to vias
- Standardized via sizes to 10/22 and 15/30 (mils)
- New footprint for 5V SMPS inductor (fits two inductors now)
- Added I2C pullup footprints (resistors are "DNI")
- Fan connectors now have a 3rd pin for reading the TACH signal
- Added 100R to the gate of each FET
- Adjusted the stackup to better reflect a standard 4-layer stack

0.4a Revision Summary

- Touchup diode polarity markings in silkscreen
- New footprint for P3
- Moved thermistor TPs to connector pin
- Increased GND stitching
- Increased copper pour coverage
- Updated paste mask apertures on QFNs
- Added nAC\_FAULT to pin\_6 of Atmega2560
- Added J7, power failure relay input.
- Added R73
- Removed RN4
- Stole RX1 and TX1 from P1, moved to J19
- Combined 2560 ICSP (X18) with pins\_9-14 of J19
- Removed J16-J18, X\_MAX, Y\_MAX, Z\_MAX
- Changed X\_MIN and Y\_MIN endstops to 2-pin headers
- Changed Z\_MIN endstop to Z\_PROBE, 4-pin header
- Combined DIAG\_0 and DIAG\_1 on TMC2130 drivers
- TP40 moved 0.1" to the left
- TP32 moved 0.1" to the left

0.5a Revision Summary

- Added ferrites to motor controller outputs.
- Removed fuse and input filter for VMOT
- Move MOSFET pulldown resistors to input side of AND gates
- Added ferrites to all P1 and P2 signals.
- Changed RN1 and RN2 from 10k to 5.6k (increases voltage on motor controller Vref pins)
- Changed motor controller low-side I-sense resistors from 0.1 to 0.22Ohm
- Voltage regulator U3 is now sourced from VMOT (was +12V2)
- Added power bypass capacitors to J7 and J15
- +12V2(Logic) and +12V3(Bed) now have micro-controller ADC based voltage monitoring.
- Added 2 internal layers (now 6 layers total)
- Added filtered internal island for micro-controller Vcc
- Most bottom layer routing (Layer 6) was moved to the new adjacent internal layer (Layer 5)
- Moved MOSFET pulldowns R43 and R57 upstream from FETs and placed at input of AND gate.
- New pinout for J19 header.
- Motor connectors are now flush with the bottom edge of the board.

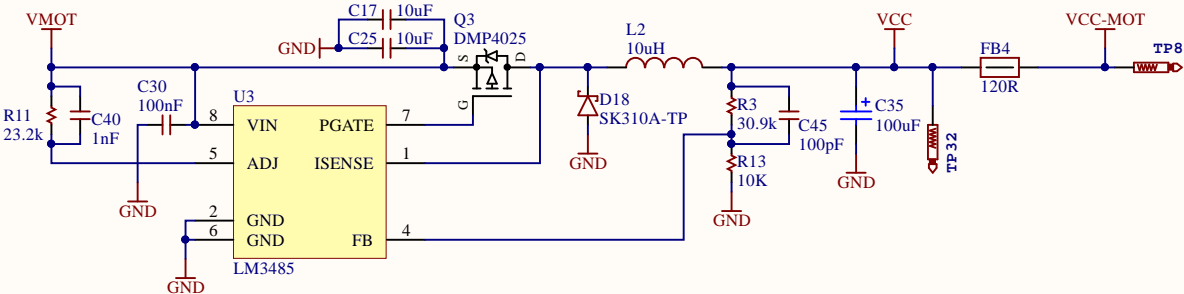
1.0a Revision Summary

- Populate FGND to GND resistor ties

Notes:  
DNI = Do Not Include = No Populate

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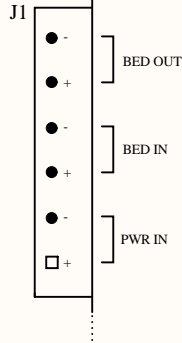
Voltage Regulator



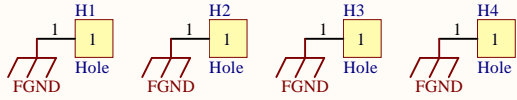
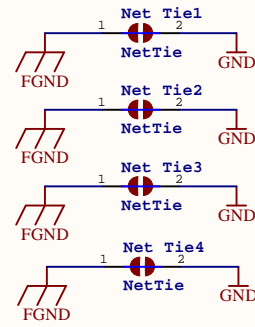
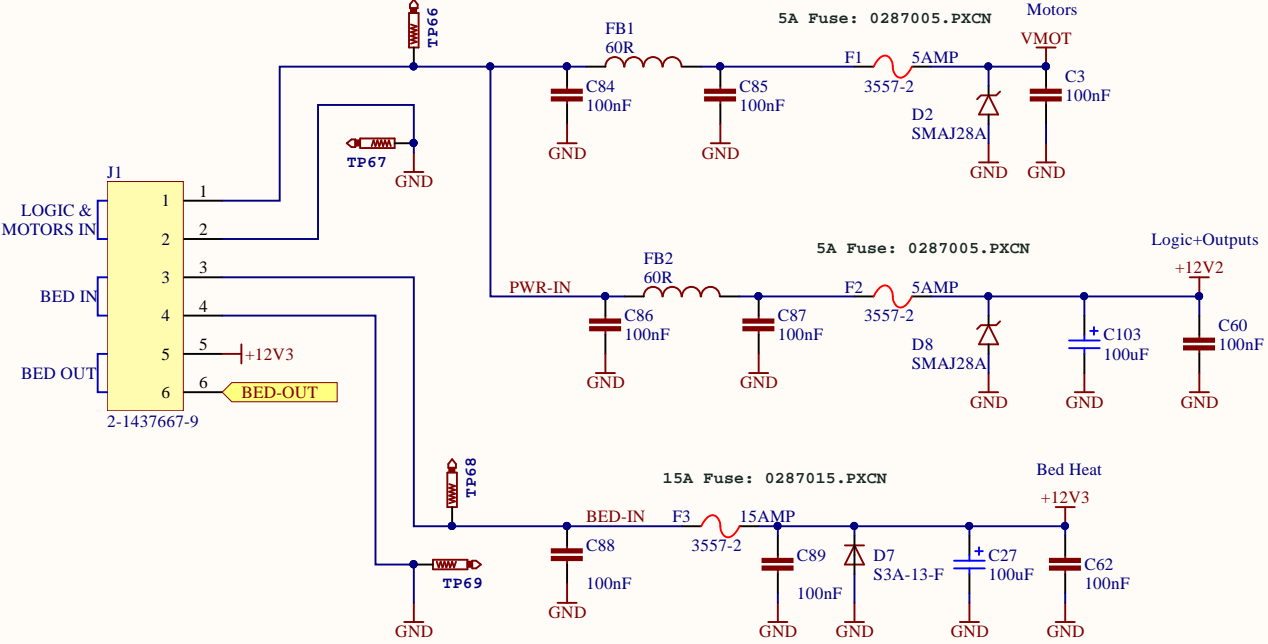
SRR1208-220ML 0.37 @ 400pcs  
SRR1280-220M 0.45 @ 1k  
ASPI-0630LR-150M-T15 0.42 @ 500pcs  
SRN8040TA-100M 0.32 @ 500pcs

TOP BOARD EDGE

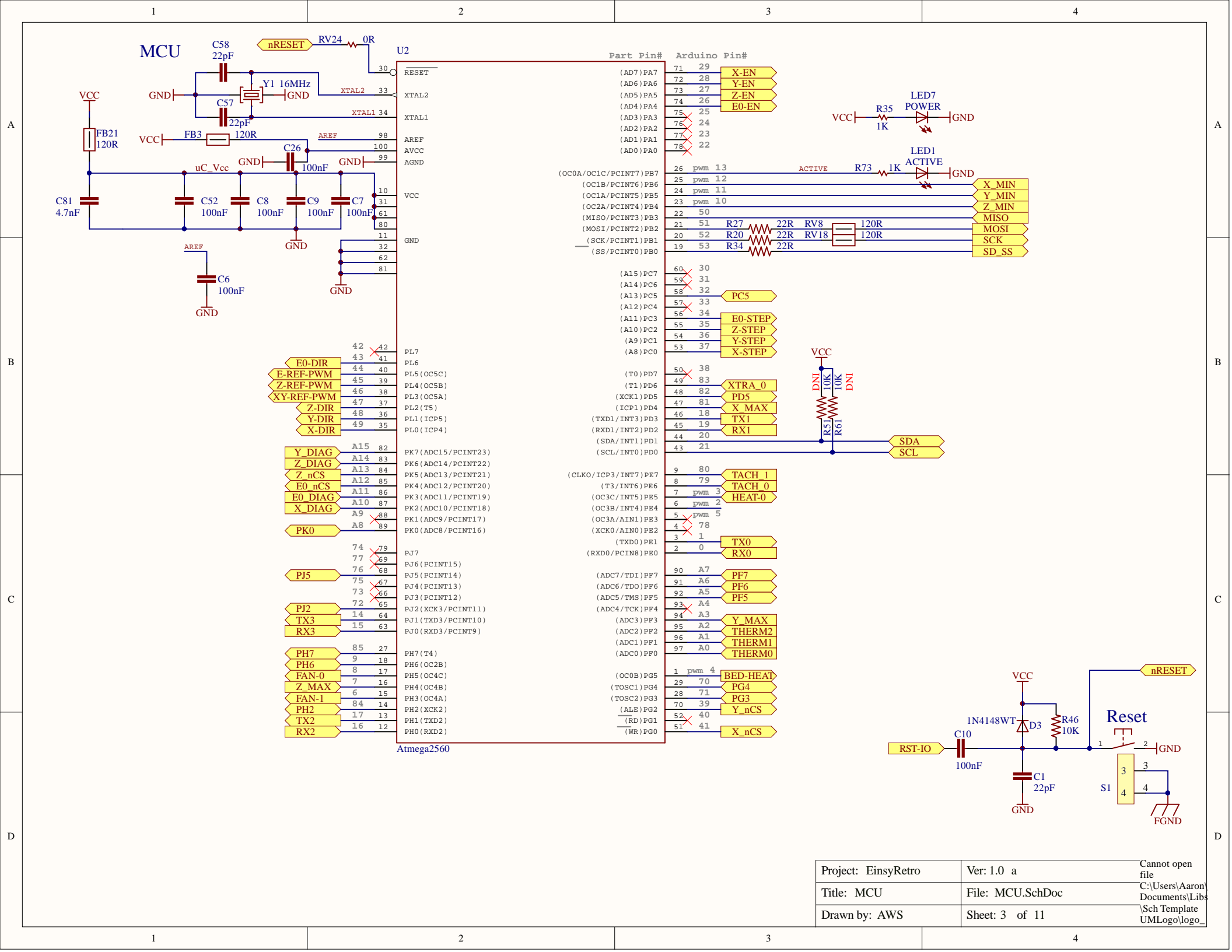
Connector Layout



Power Input

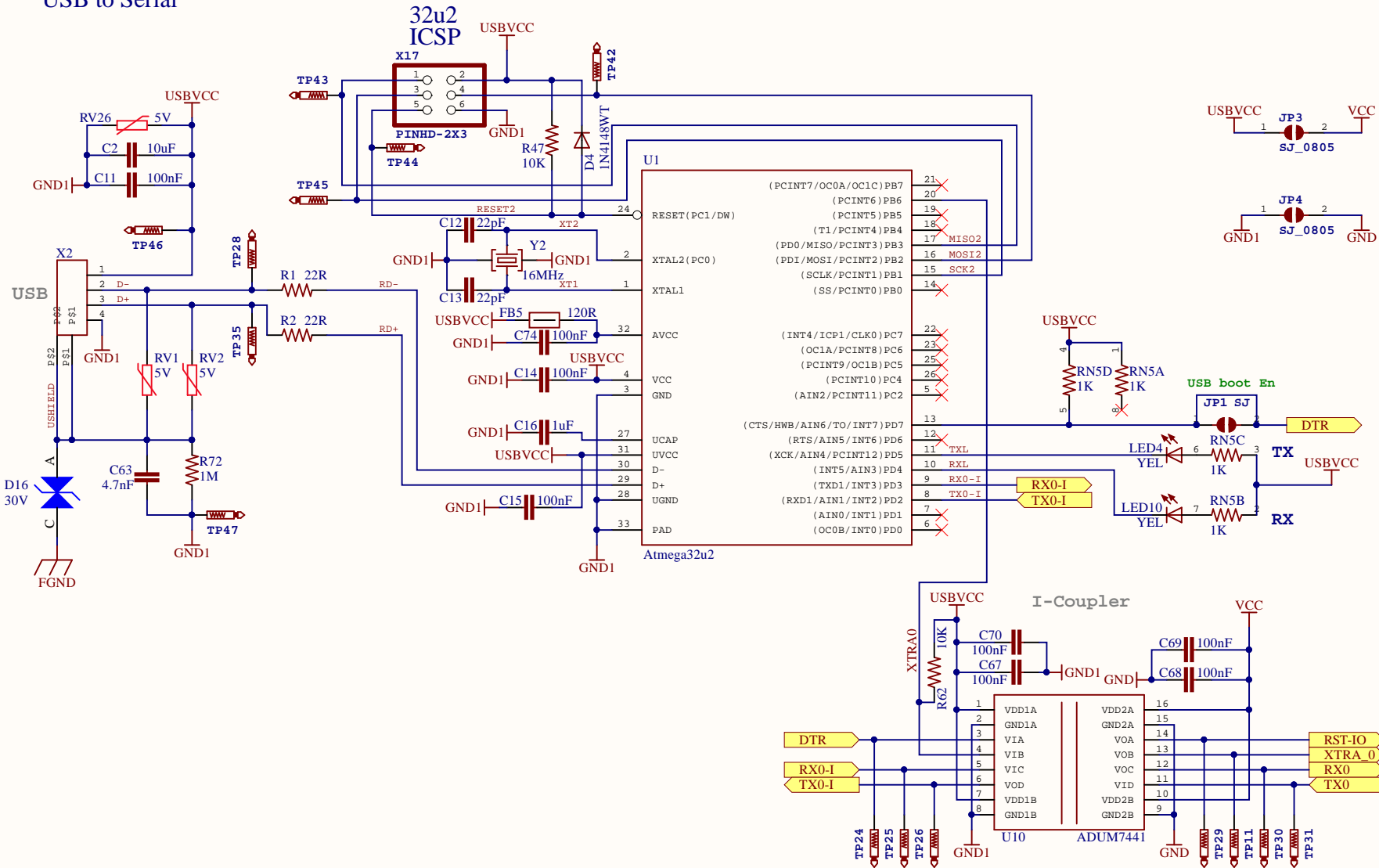


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# Atmega 32u2 USB

## USB to Serial



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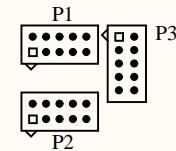
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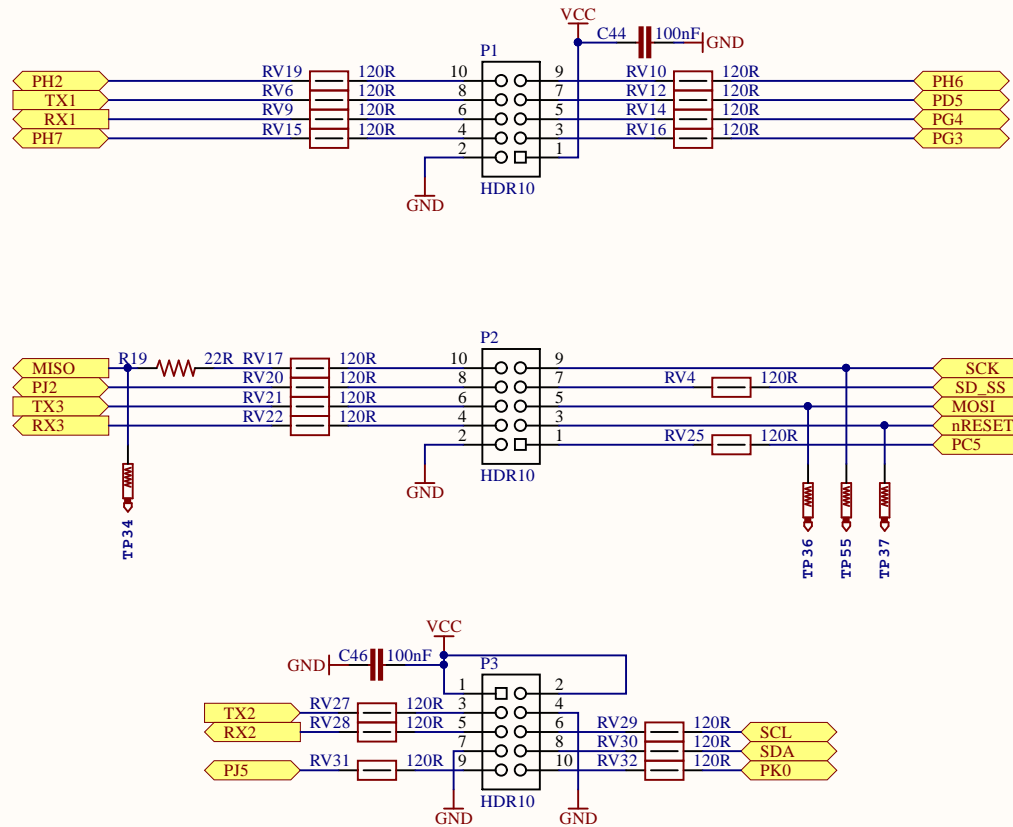
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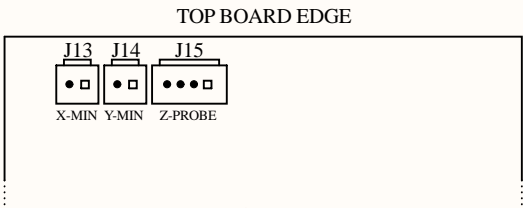


Connector Layout

### Expansion Connectors



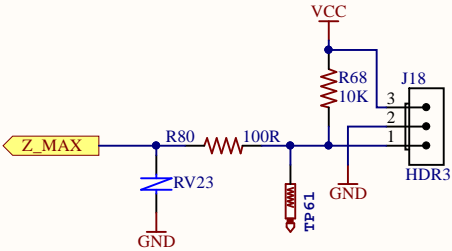
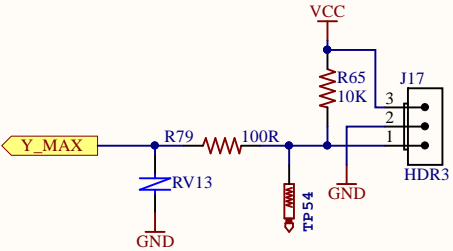
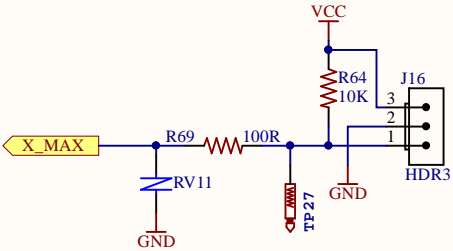
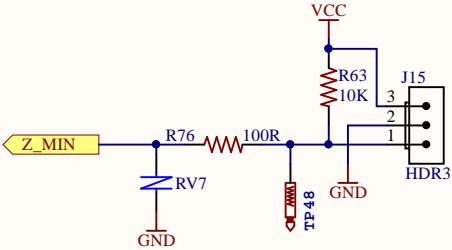
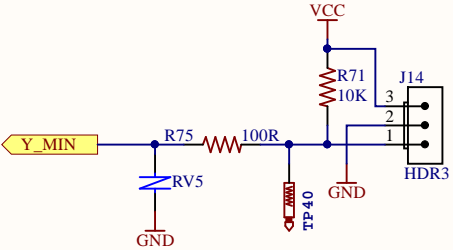
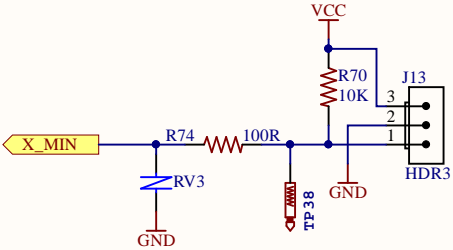
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REDO

Connector  
Layout

End Stops



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1



1

1

2

A

B

C

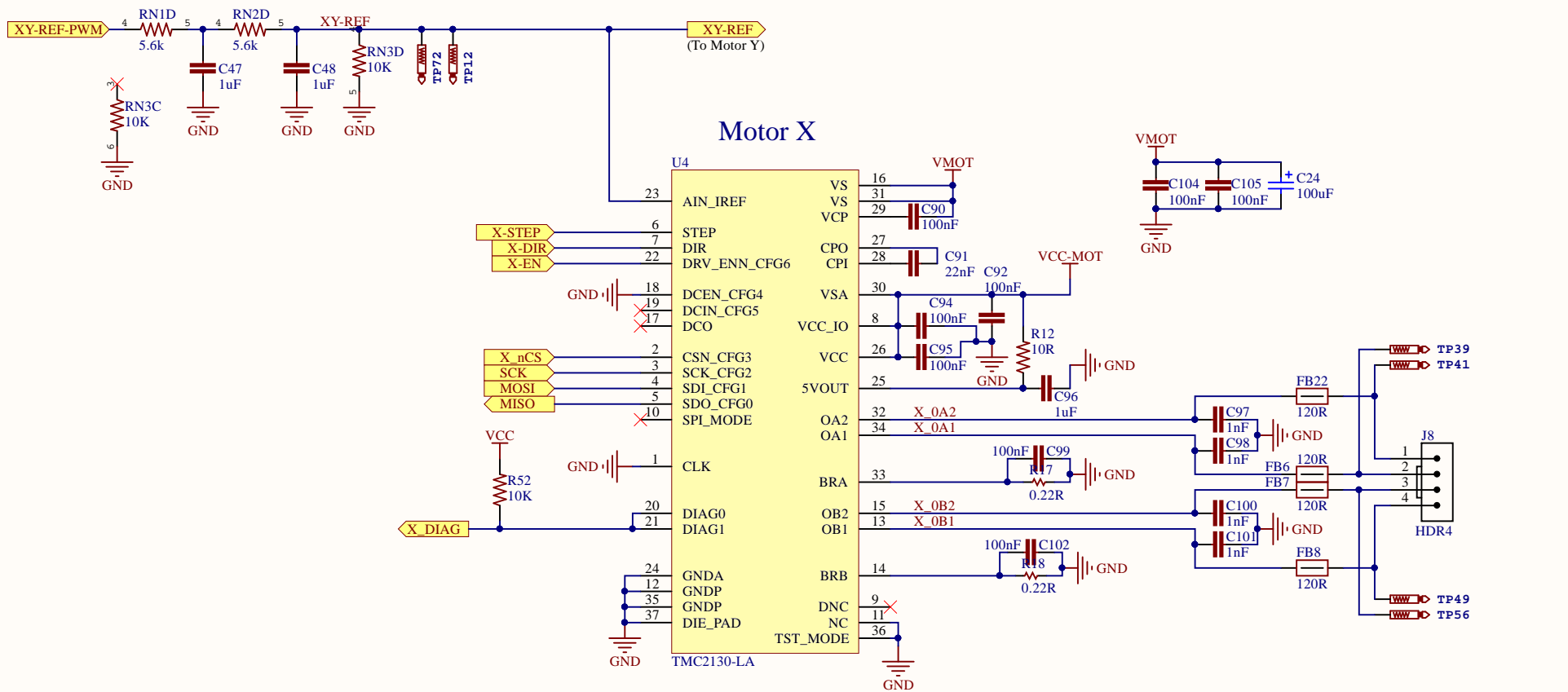
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A

B

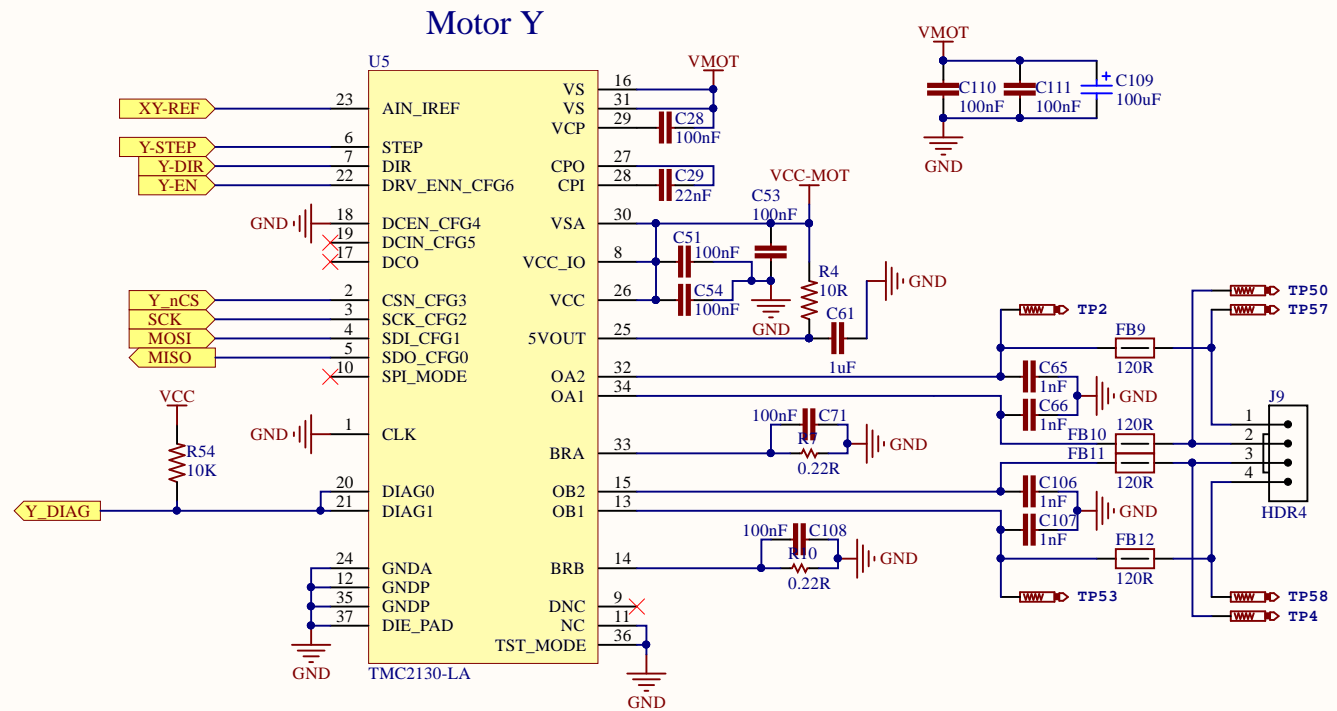
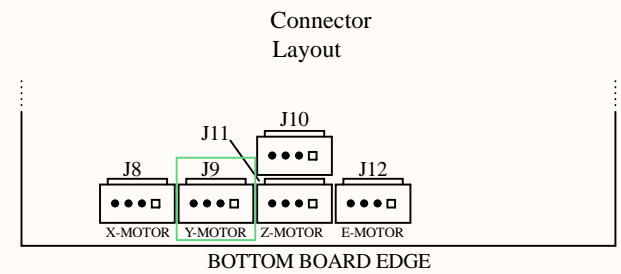
C

D

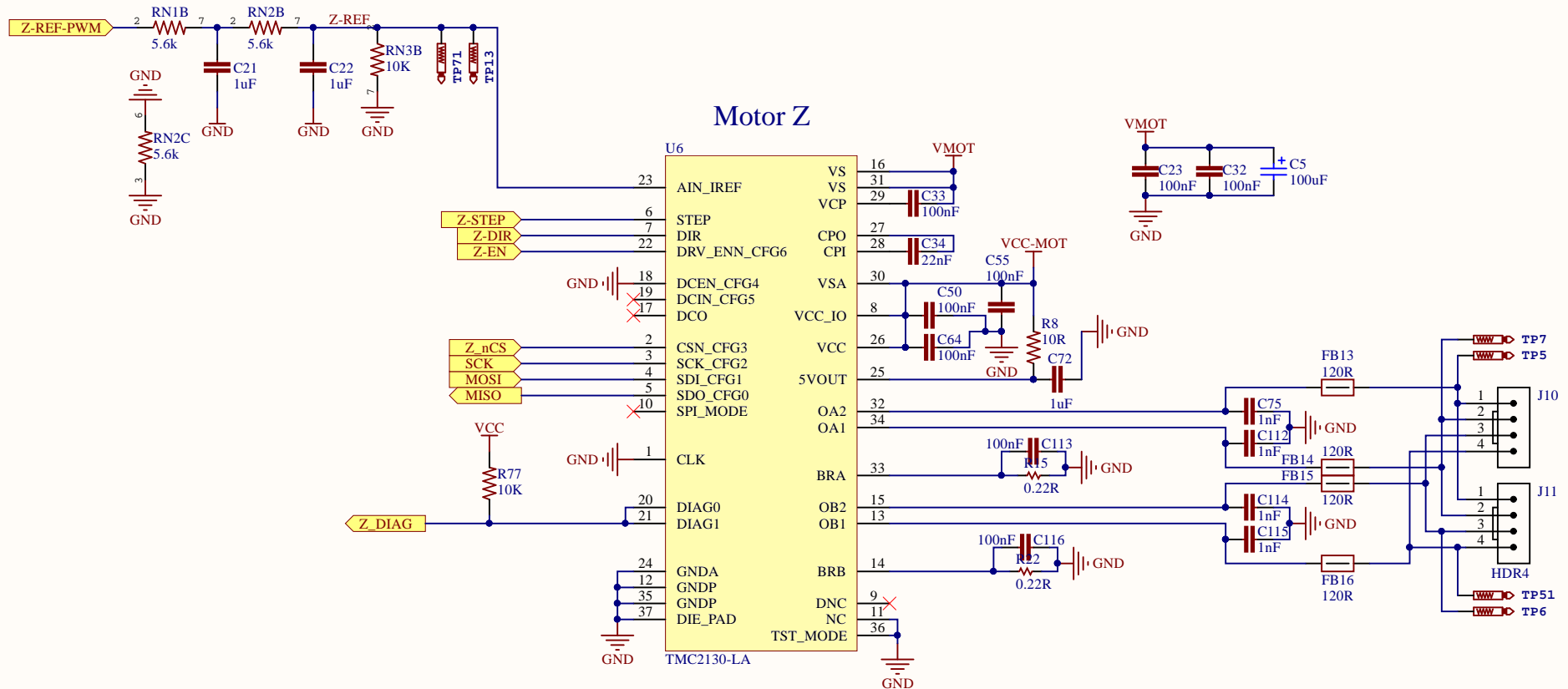
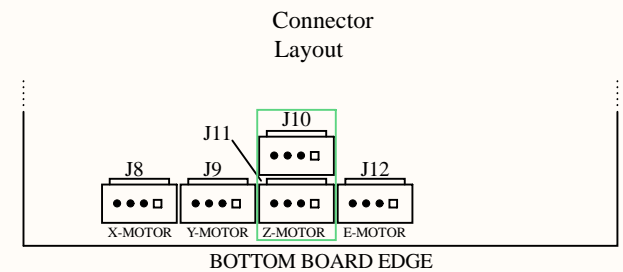


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