

EinsyRetro 1.0b

UltiMachine

11/08/2017

0.3a Revision Summary (for detailed infomation goto: <https://github.com/ultimachine/Einsy-Rambo/tree/0.3a>)

- Added TVS and over-voltage protection to select nets
- Added and corrected testpoints
- Added "XTRA0" net between 32U2 and 2560
- Removed via tenting underneath QFNs and other flat solder lug/heatsink primitives
- Added teardrops to vias
- Standardized via sizes to 10/22 and 15/30 (mils)
- New footprint for 5V SMPS inductor (fits two inductors now)
- Added I2C pullup footprints (resistors are "DNI")
- Fan connectors now have a 3rd pin for reading the TACH signal
- Added 100R to the gate of each FET
- Adjusted the stackup to better reflect a standard 4-layer stack

0.4a Revision Summary

- Touchup diode polarity markings in silkscreen
- New footprint for P3
- Moved thermistor TPs to connector pin
- Increased GND stitching
- Increased copper pour coverage
- Updated paste mask apertures on QFNs
- Added nAC_FAULT to pin_6 of Atmega2560
- Added J7, power failure relay input.
- Added R73
- Removed RN4
- Stole RX1 and TX1 from P1, moved to J19
- Combined 2560 ICSP (X18) with pins_9-14 of J19
- Removed J16-J18, X_MAX, Y_MAX, Z_MAX
- Changed X_MIN and Y_MIN endstops to 2-pin headers
- Changed Z_MIN endstop to Z_PROBE, 4-pin header
- Combined DIAG_0 and DIAG_1 on TMC2130 drivers
- TP40 moved 0.1" to the left
- TP32 moved 0.1" to the left

0.5a Revision Summary

- Added ferrites to motor controller outputs.
- Removed fuse and input filter for VMOT
- Move MOSFET pulldown resistors to input side of AND gates
- Added ferrites to all P1 and P2 signals.
- Changed RN1 and RN2 from 10k to 5.6k (increases voltage on motor controller Vref pins)
- Changed motor controller low-side I-sense resistors from 0.1 to 0.22Ohm
- Voltage regulator U3 is now sourced from VMOT (was +12V2)
- Added power bypass capacitors to J7 and J15
- +12V2(Logic) and +12V3(Bed) now have micro-controller ADC based voltage monitoring.
- Added 2 internal layers (now 6 layers total)
- Added filtered internal island for micro-controller Vcc
- Most bottom layer routing (Layer 6) was moved to the new adjacent internal layer (Layer 5)
- Moved MOSFET pulldowns R43 and R57 upstream from FETs and placed at input of AND gate.
- New pinout for J19 header.
- Motor connectors are now flush with the bottom edge of the board.

1.0a Revision Summary


- Populate FGND to GND resistor ties
- Changed motor drive sense resistors from 0.22R to 0.12R
- Added a 5V buck controller for more current and future flexibility
- Fan power is derived from 12V2 rail
- Hardware SPI nSS signal moved back to P2
- UART1 TX and RX moved back to P1

1.0b Revision Summary

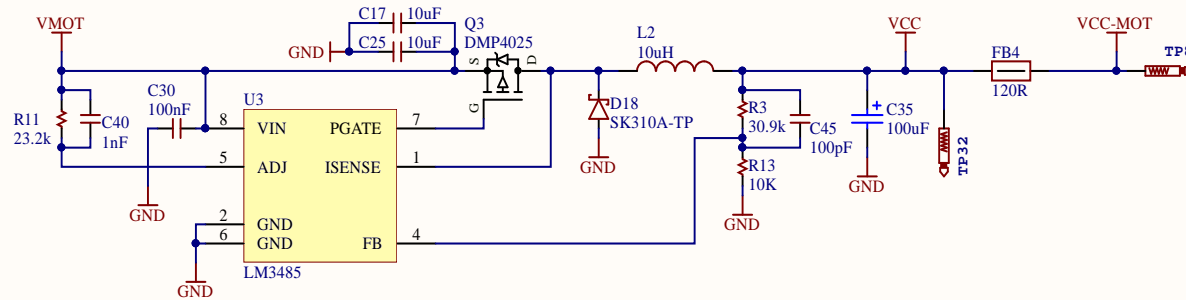
- Added 3-state buffer between SD_MISO_3V3 and MISO_5V0

Notes:

DNI = Do Not Include = No Populate

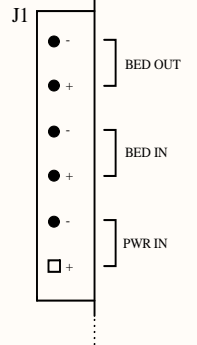
Project: EinsyRetro	Ver: 1.0 a	
Title: Title Page	File: Title.SchDoc	
Drawn by: AWS	Sheet: 1 of 11	

Voltage Regulator

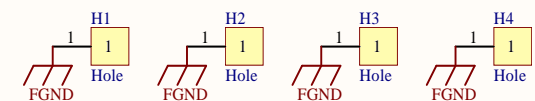
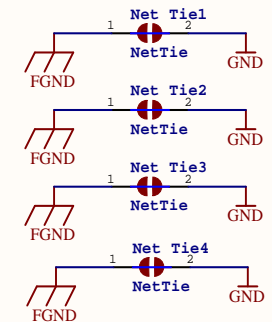
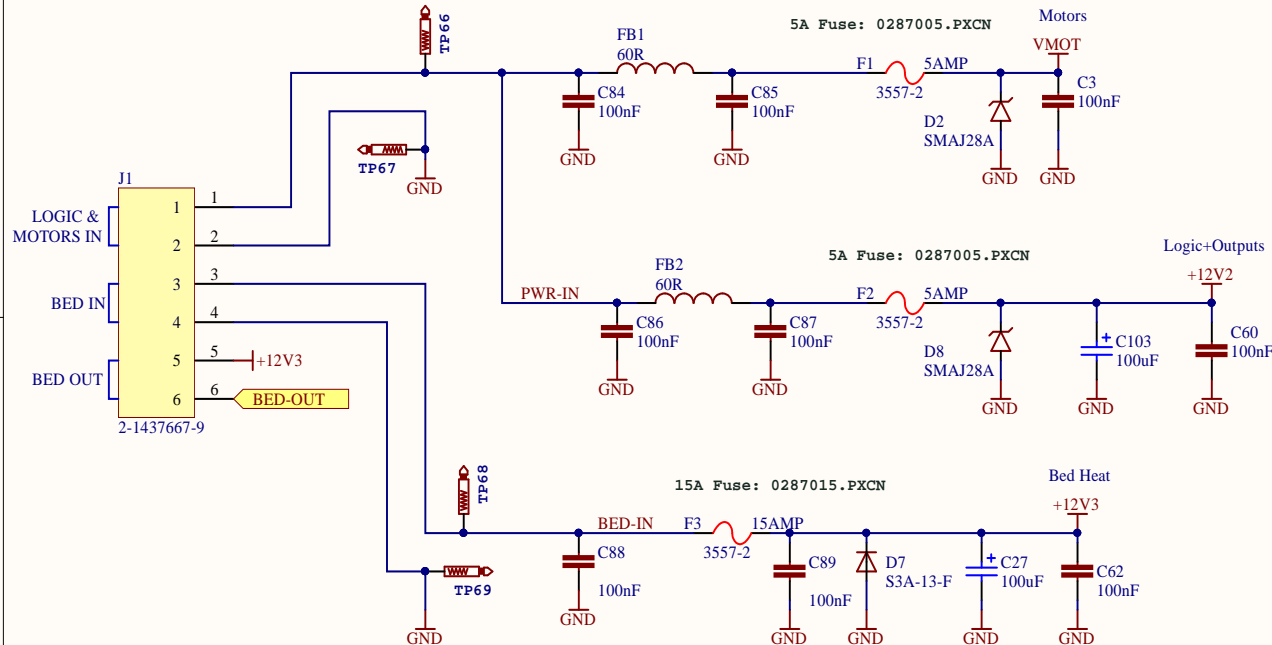



TOP BOARD EDGE

Connector Layout



Power Input



Project: EinsyRetro	Ver: 1.0 a	
Title: Power-SMPS	File: Power-SMPS.SchDoc	
Drawn by: AWS	Sheet: 2 of 11	

MCU

U2

Part Pin#

Arduino Pin#

Atmega2560

Project: EinsyRetro

Ver: 1.0 a

Title: MCU

File: MCU.SchDoc

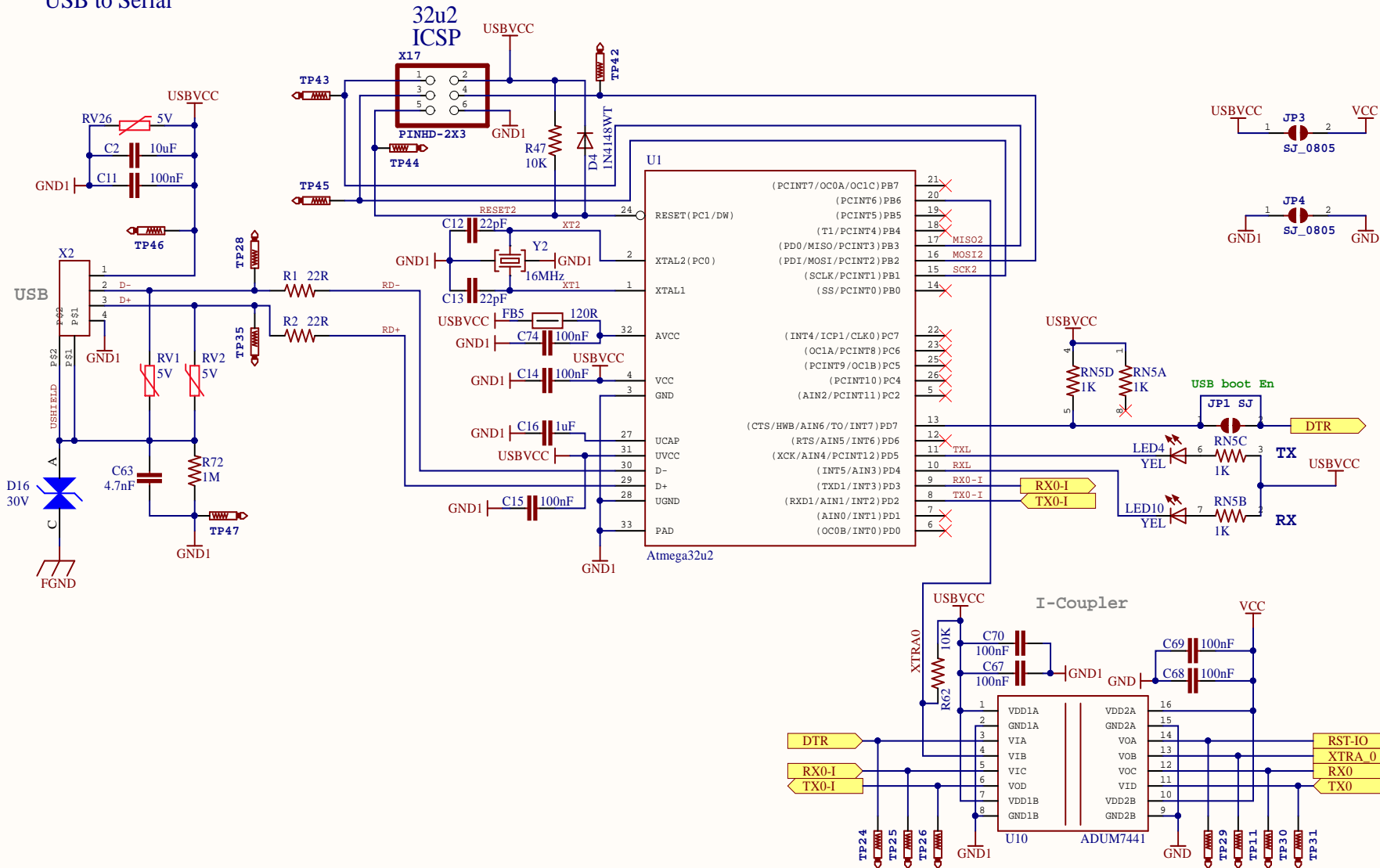
Drawn by: AWS

Sheet: 3 of 11



USB to Serial

Atmega 32u2 USB



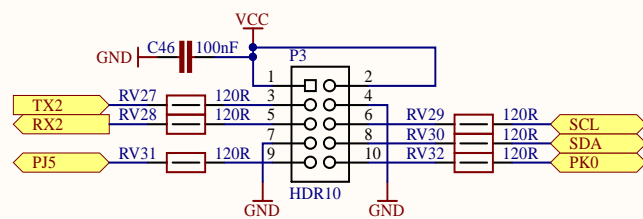
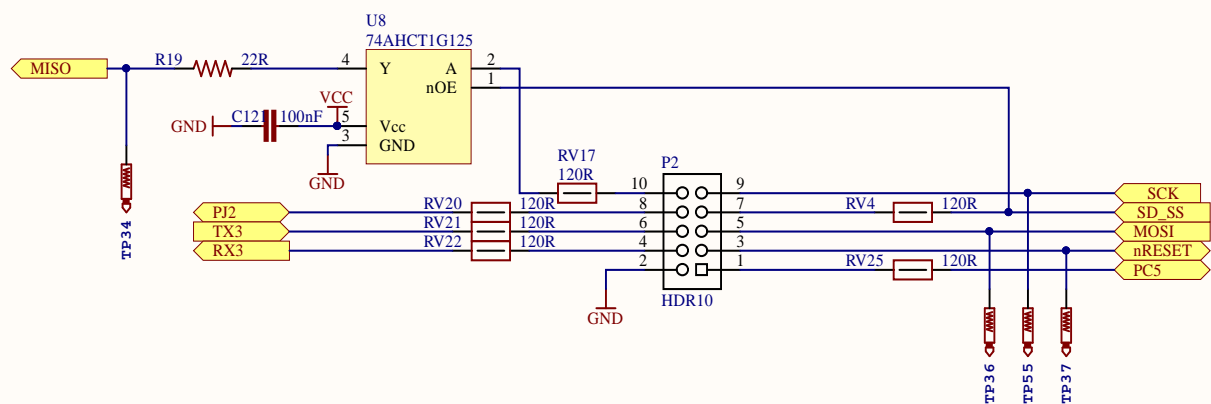
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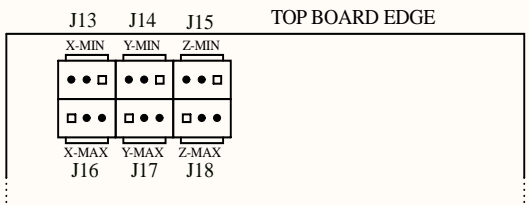
Project: EinsyRetro	Ver: 1.0 a	
Title: USB-Serial	File: USB-Serial.SchDoc	
Drawn by: AWS	Sheet: 4 of 11	



Connector Layout

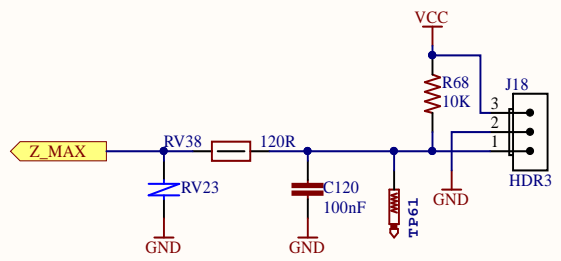
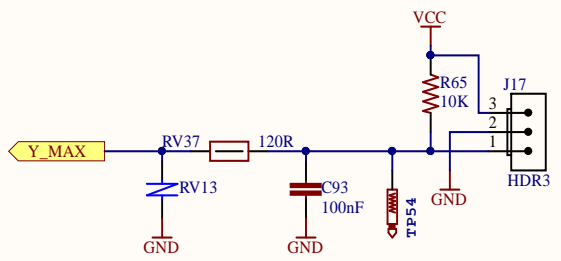
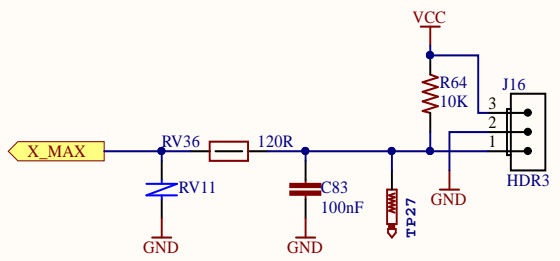
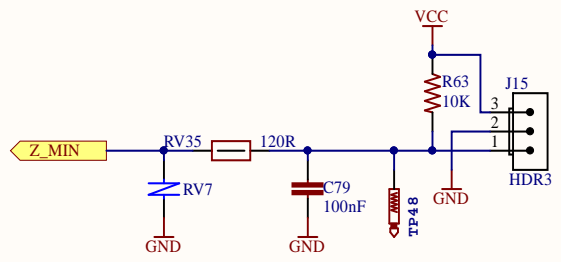
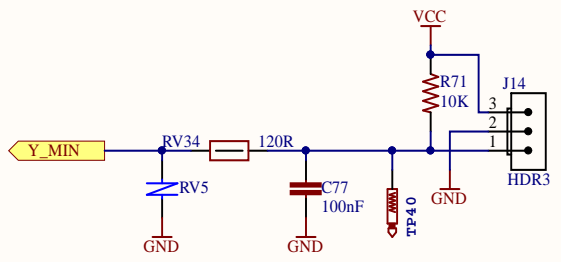
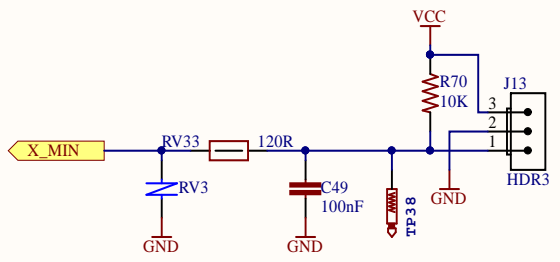
Project: EinsyRetro	Ver: 1.0 a	
Title: Connectors	File: Connectors.SchDoc	
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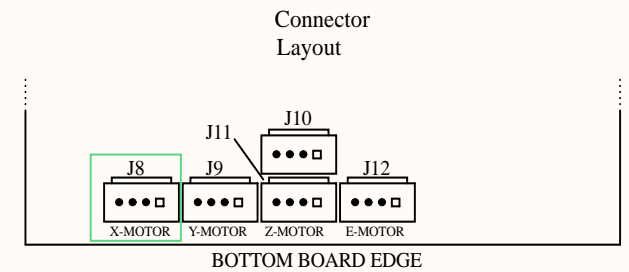
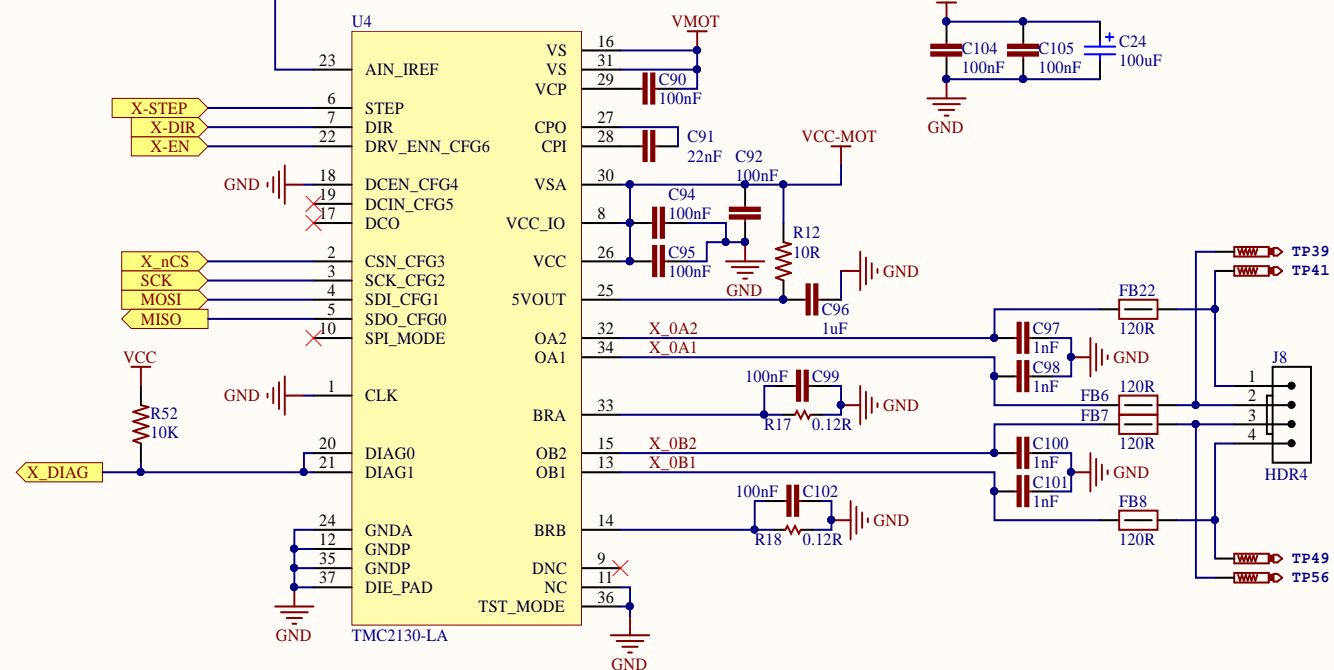
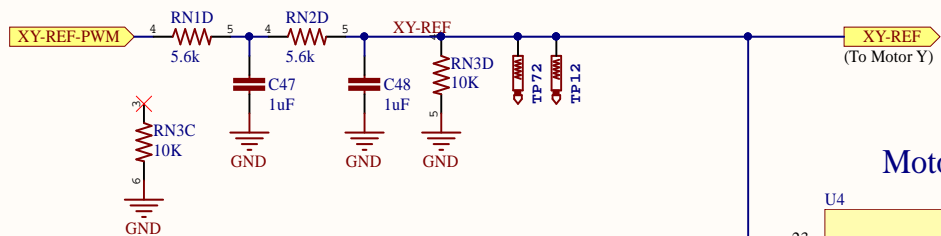
Connector Layout

End Stops







A



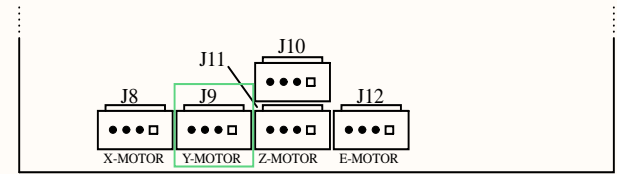


Deprecated Test Points

X_0A1		TP75
X_0A2		TP73
X_0B1		TP1
X_0B2		TP74

Project: EinsyRetro	Ver: 1.0 a
Title: Motor-X	File: Motor-X.SchDoc
Drawn by: AWS	Sheet: 8 of 11



Connector
Layout

BOTTOM BOARD EDGE

Motor Y

