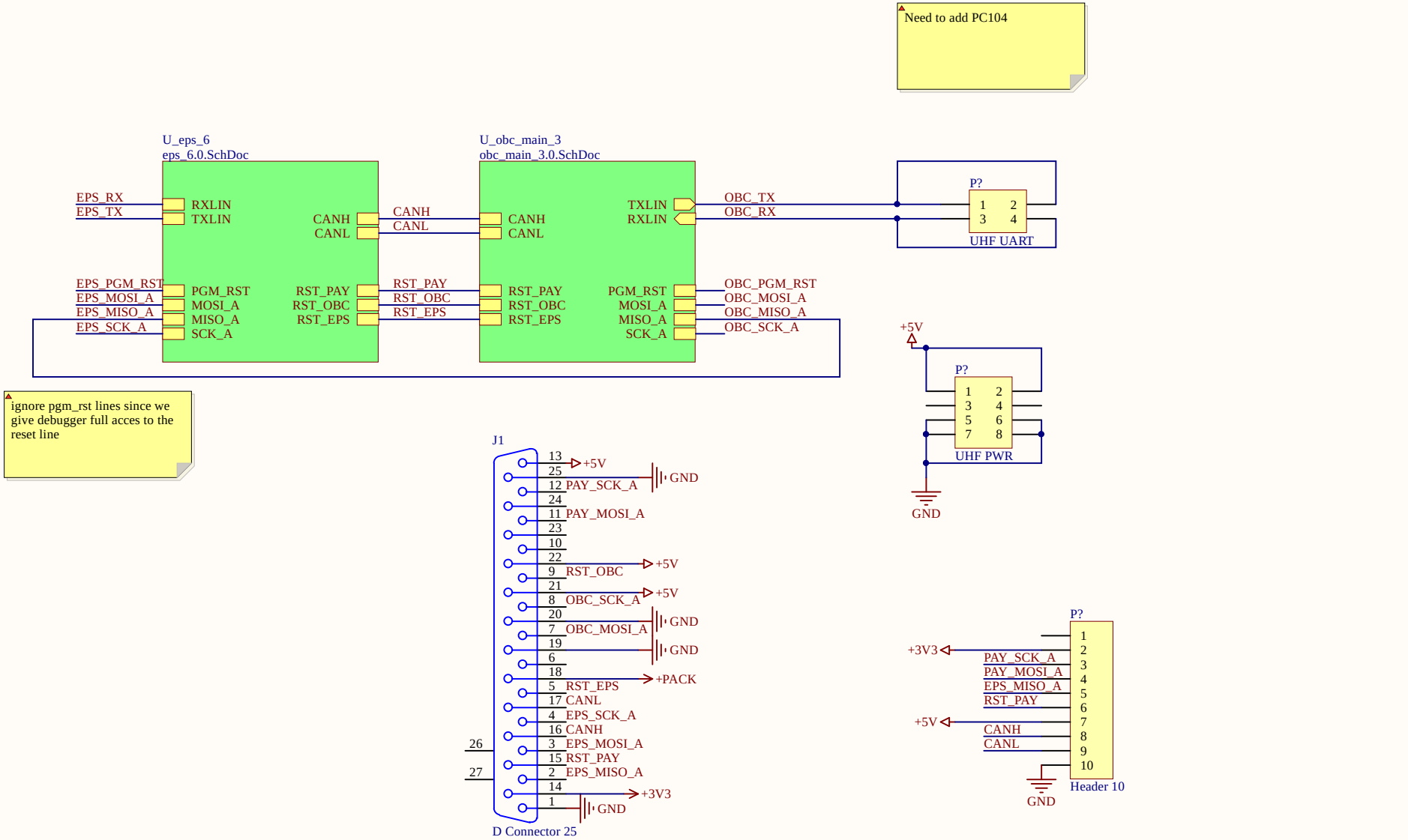

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Date: 2018-06-02	Sheet of	
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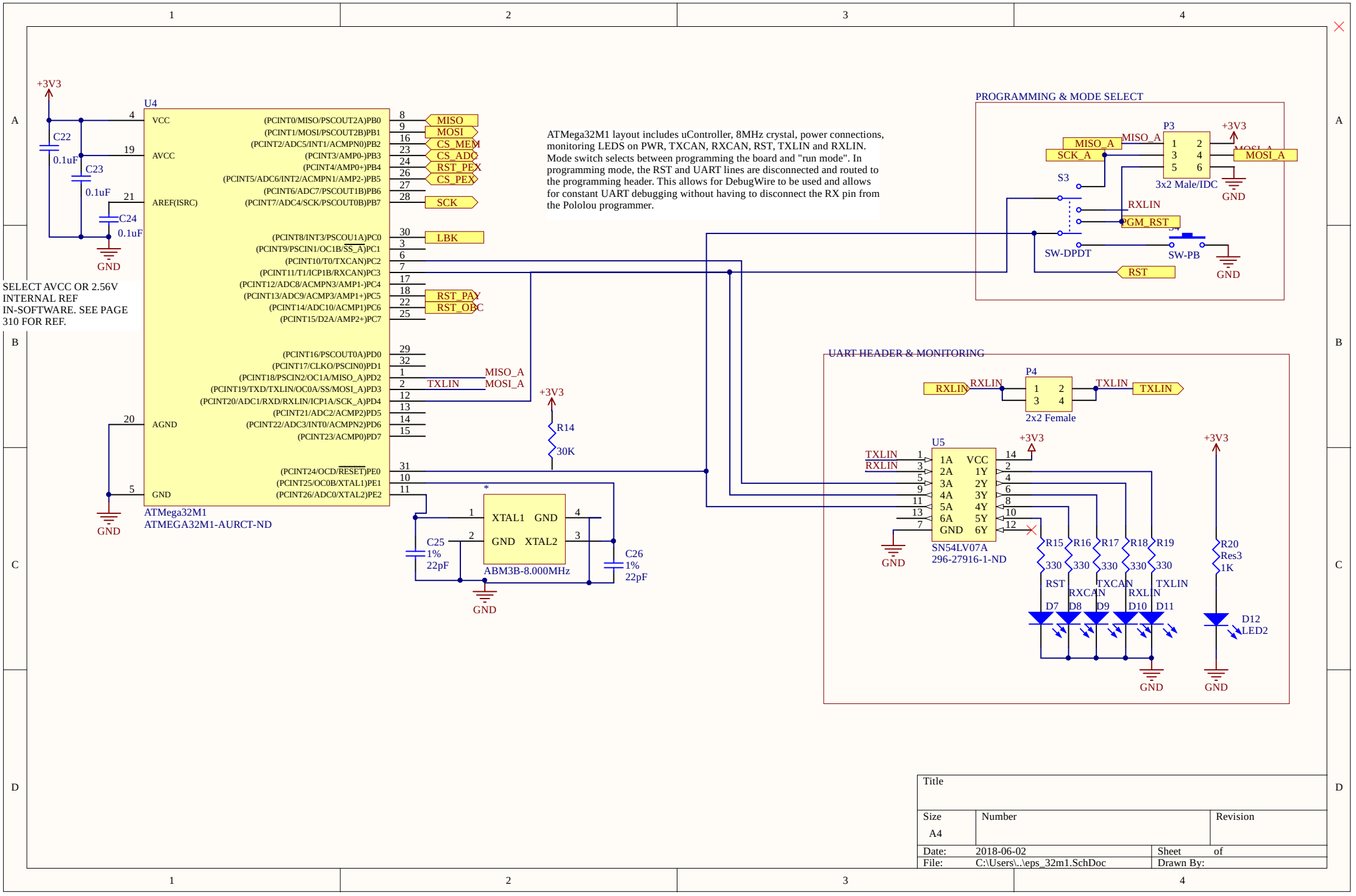
ATMega32M1 layout includes uController, 8MHz crystal, power connections, monitoring LEDS on PWR, TXCAN, RXCAN, RST, TXLIN and RXLIN. Mode switch selects between programming the board and "run mode". In programming mode, the RST and UART lines are disconnected and routed to the programming header. This allows for DebugWire to be used and allows for constant UART debugging without having to disconnect the RX pin from the Pololou programmer.
SELECT AVCC OR 2.56V INTERNAL REF IN-SOFTWARE. SEE PAGE 310 FOR REF.
U4
ATMega32M1
ATMEGA32M1-AURCT-ND
PROGRAMMING & MODE SELECT
P3
3x2 Male/IDC
S3
SW-DPDT
SW-PB
UART HEADER & MONITORING
P4
2x2 Female
U5
SN54LV07A
296-27916-1-ND
ABM3B-8.000MHz
Title
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Number
Revision
Date: 2018-06-02
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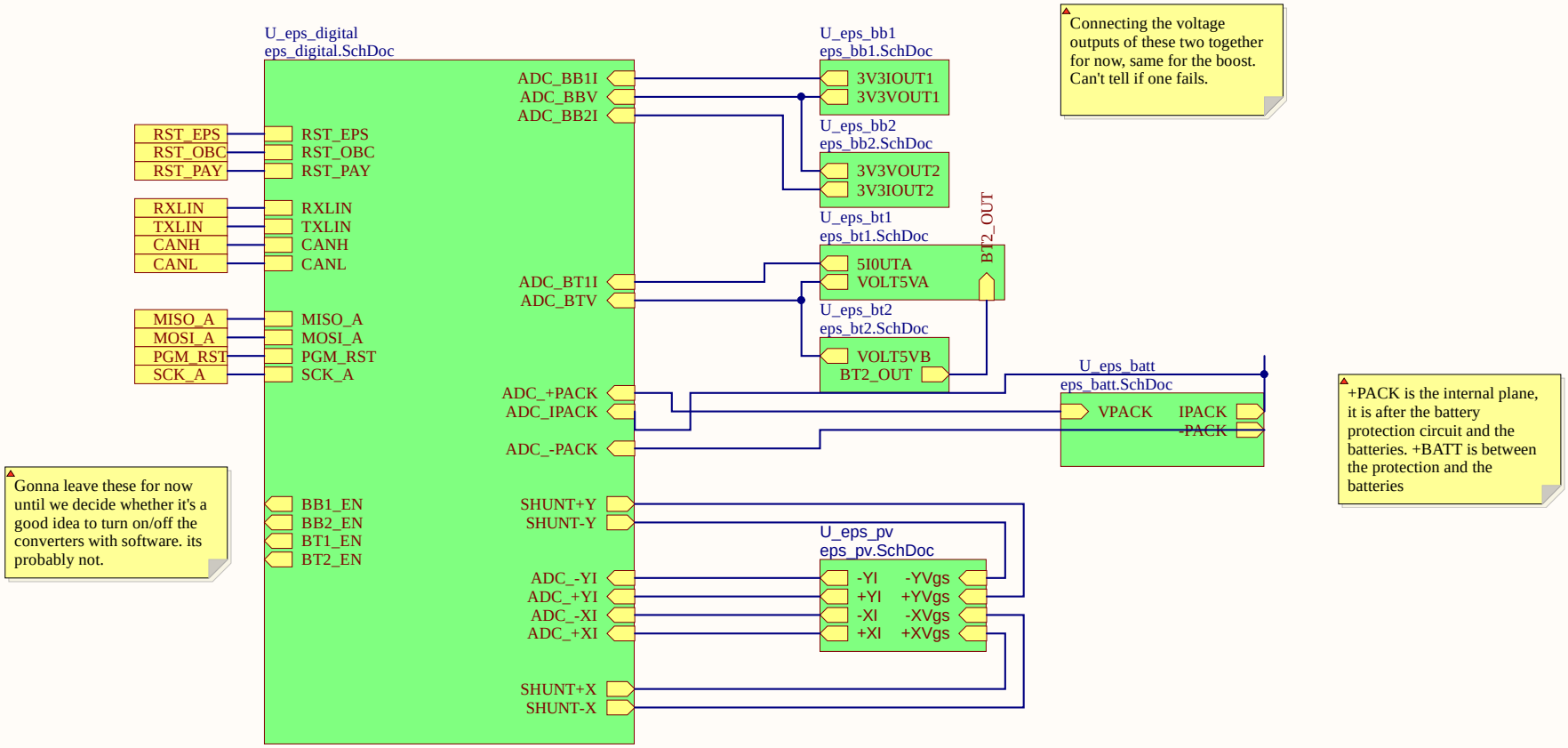

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Size A	Number	Revision
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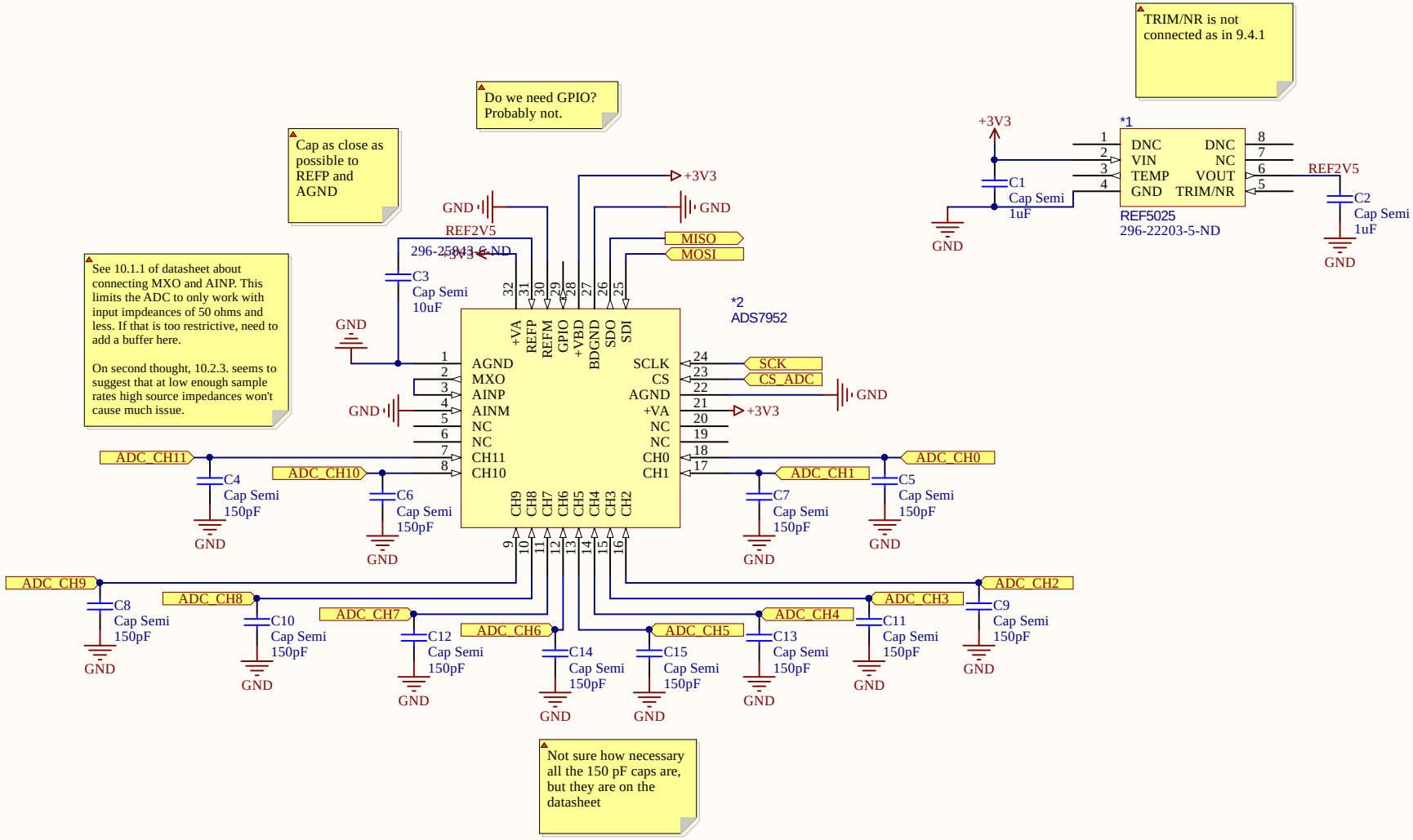

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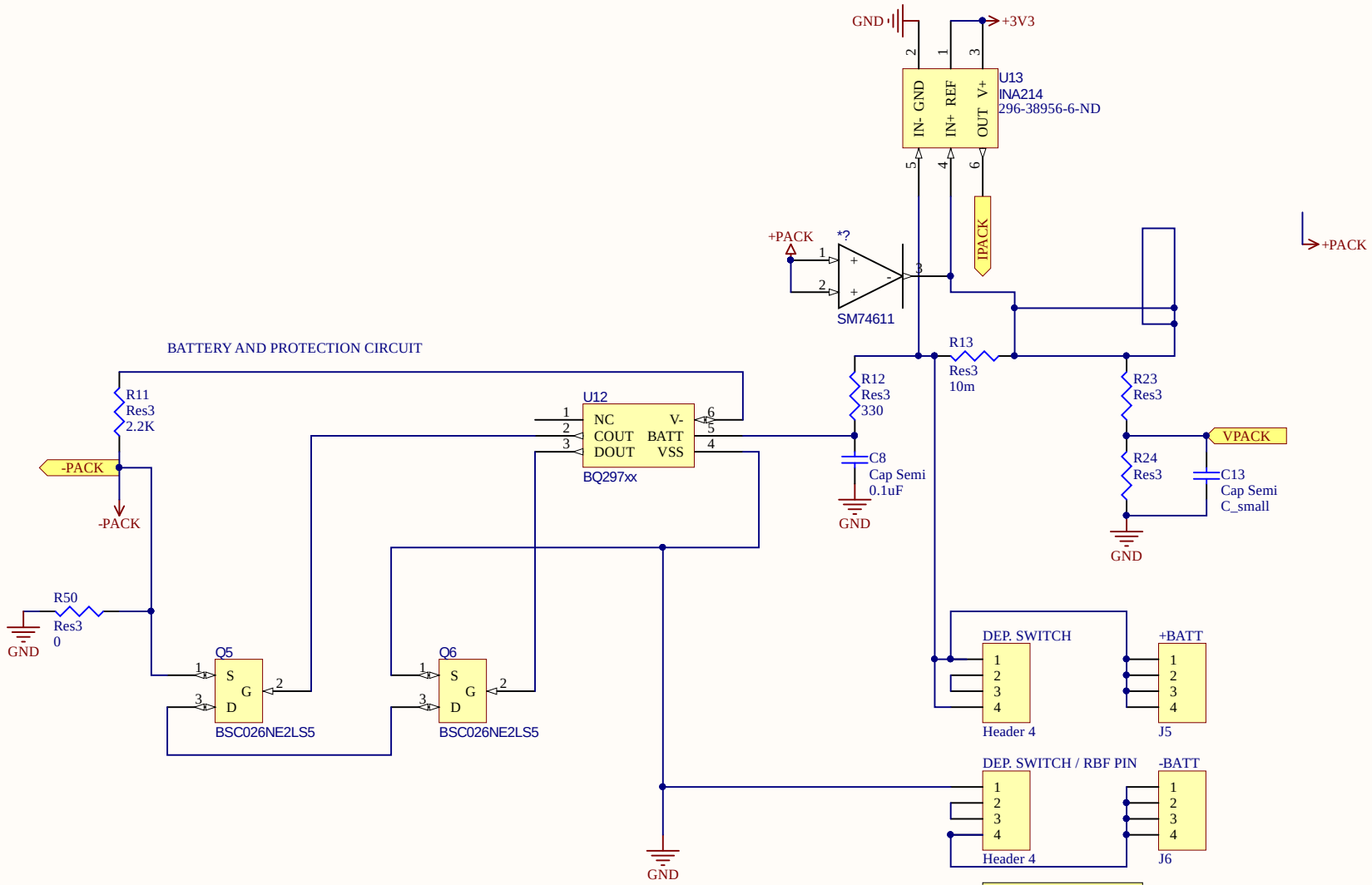

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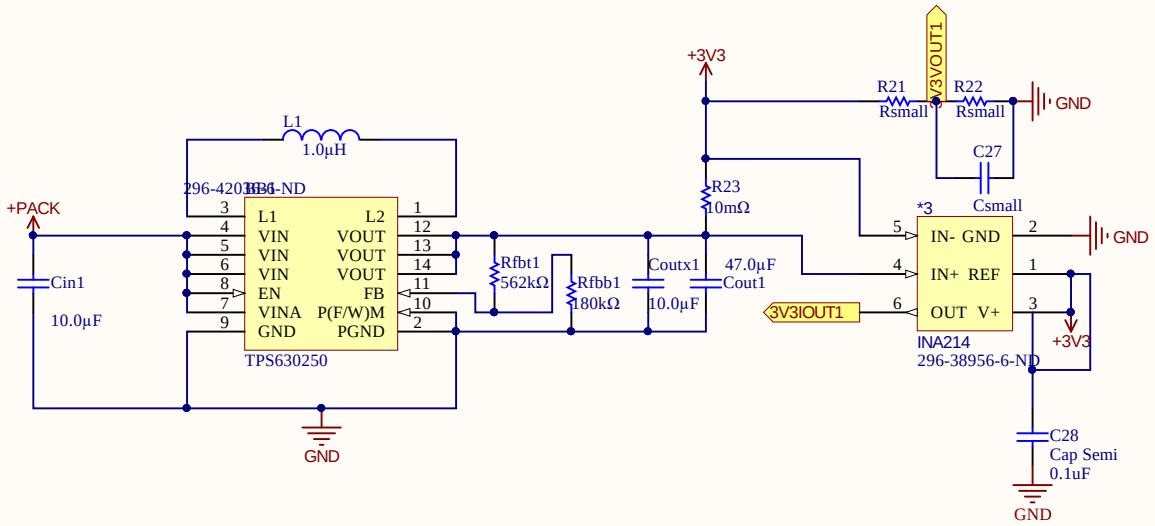

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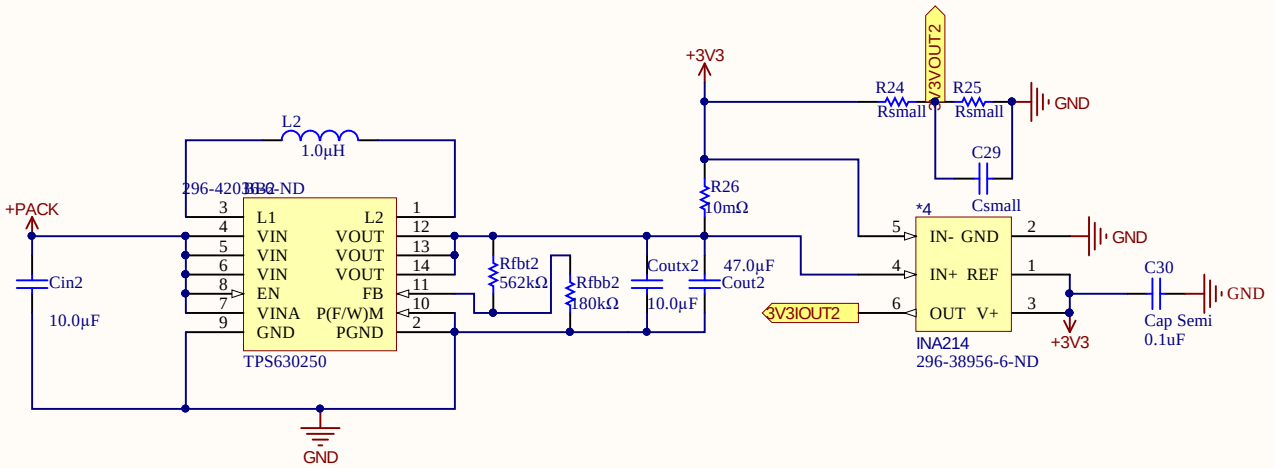

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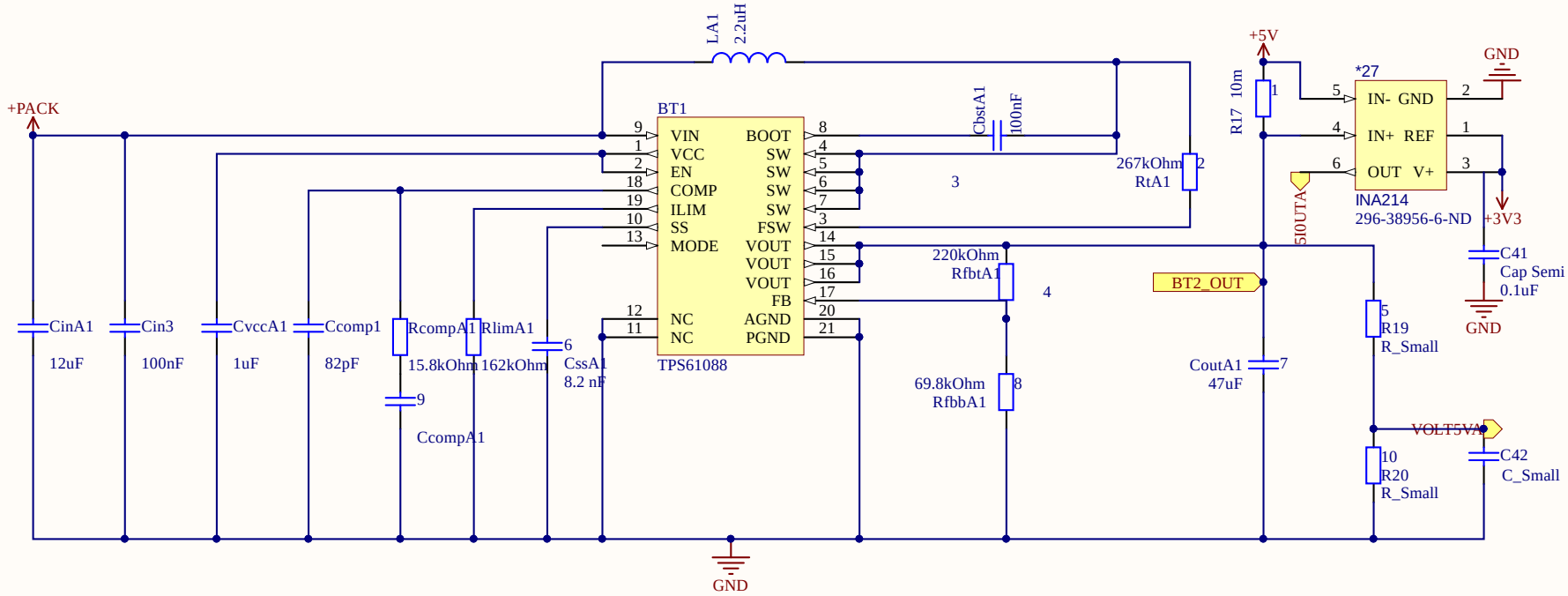

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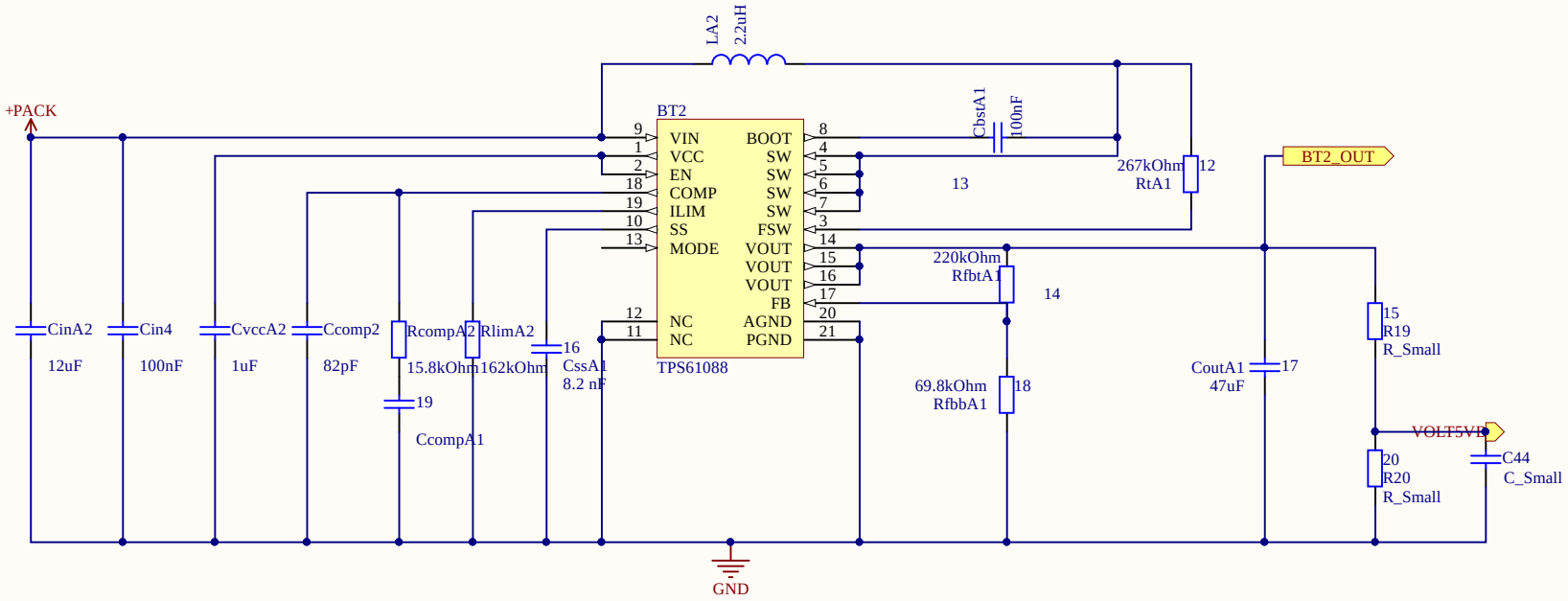

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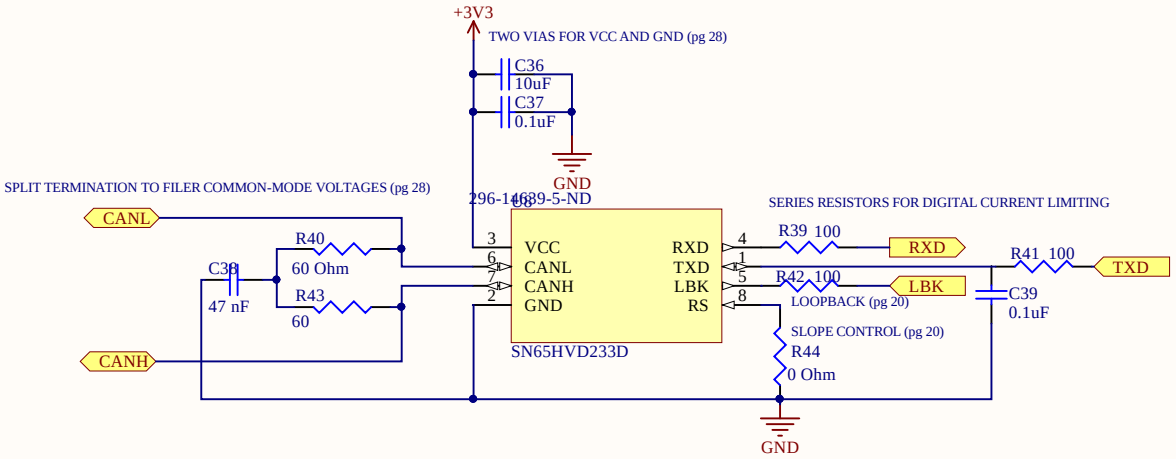

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Size: A4	Number	Revision
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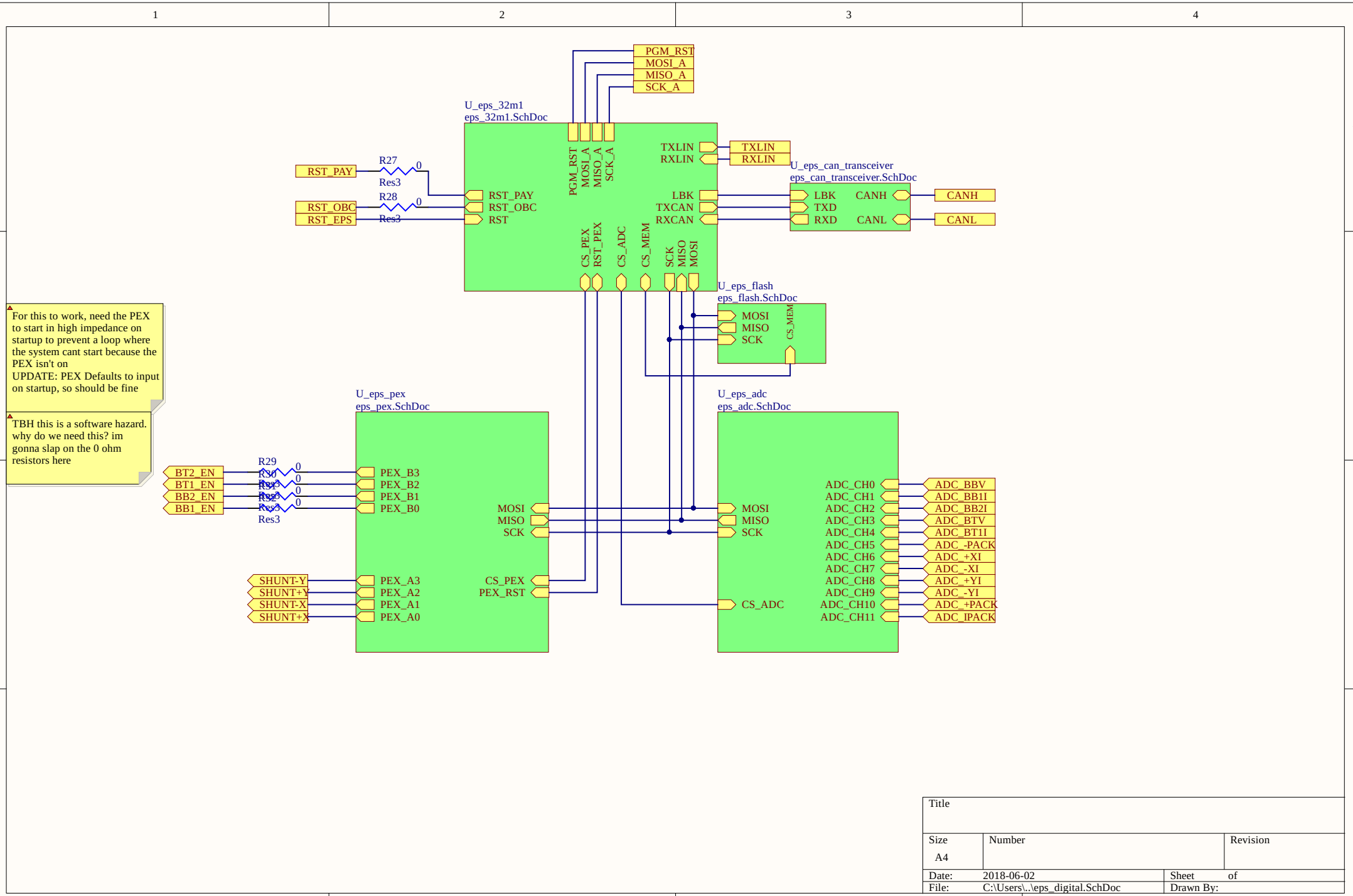
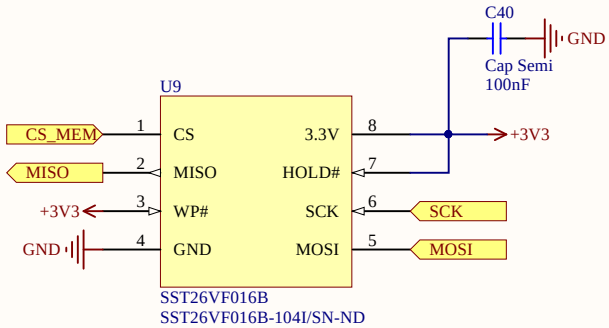

PGM_RST
MOSI_A
MISO_A
SCK_A
U_eps_32m1
eps_32m1.SchDoc
TXLIN
RXLIN
TXLIN
RXLIN
U_eps_can_transceiver
eps_can_transceiver.SchDoc
RST_PAY
R27
0
Res3
RST_OBC
R28
0
Res3
RST_EPS
RST_PAY
RST_OBC
RST
LBK
TXCAN
RXCAN
LBK
TXD
RXD
CANH
CANL
CANH
CANL
CS_PEX
RST_PEX
CS_ADC
CS_MEM
SCK
MISO
MOSI
U_eps_flash
eps_flash.SchDoc
MOSI
MISO
SCK
CS_MEM
For this to work, need the PEX to start in high impedance on startup to prevent a loop where the system cant start because the PEX isn't on
UPDATE: PEX Defaults to input on startup, so should be fine
TBH this is a software hazard. why do we need this? im gonna slap on the 0 ohm resistors here
U_eps_pex
eps_pex.SchDoc
U_eps_adc
eps_adc.SchDoc
BT2_EN
BT1_EN
BB2_EN
BB1_EN
R29
R30
R31
R32
0
Res3
PEX_B3
PEX_B2
PEX_B1
PEX_B0
MOSI
MISO
SCK
SHUNT-Y
SHUNT+Y
SHUNT-X
SHUNT+X
PEX_A3
PEX_A2
PEX_A1
PEX_A0
CS_PEX
PEX_RST
MOSI
MISO
SCK
CS_ADC
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
ADC_CH8
ADC_CH9
ADC_CH10
ADC_CH11
ADC_BBV
ADC_BB1I
ADC_BB2I
ADC_BTV
ADC_BT1I
ADC_-PACK
ADC_+XI
ADC_-XI
ADC_+YI
ADC_-YI
ADC_+PACK
ADC_IPACK
Title
Size
A4
Number
Revision
Date:
2018-06-02
Sheet
of
File:
C:\Users\..\eps_digital.SchDoc
Drawn By:



Title		
Size: A4	Number	Revision
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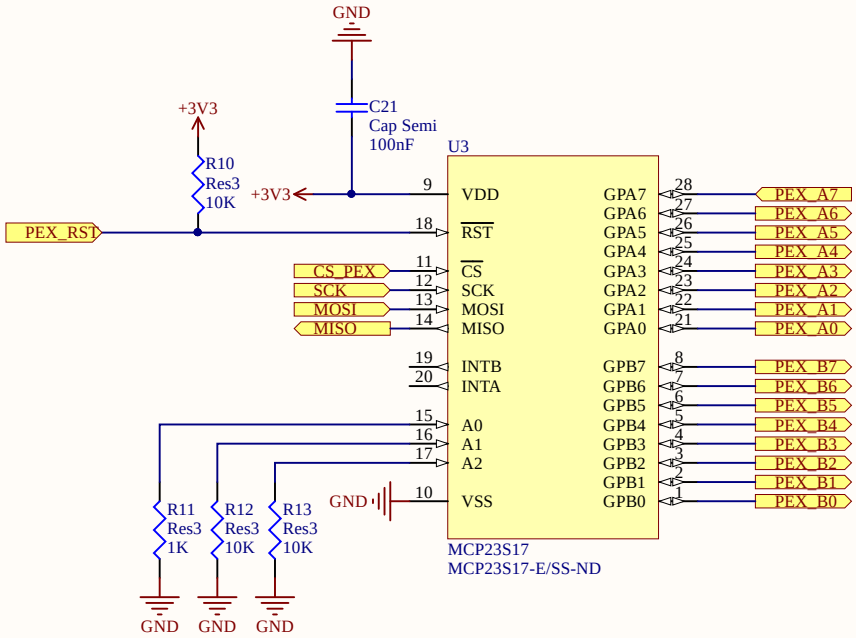
File: C:\Users\..\eps_flash.SchDoc		Drawn By:



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Size A4	Number	Revision
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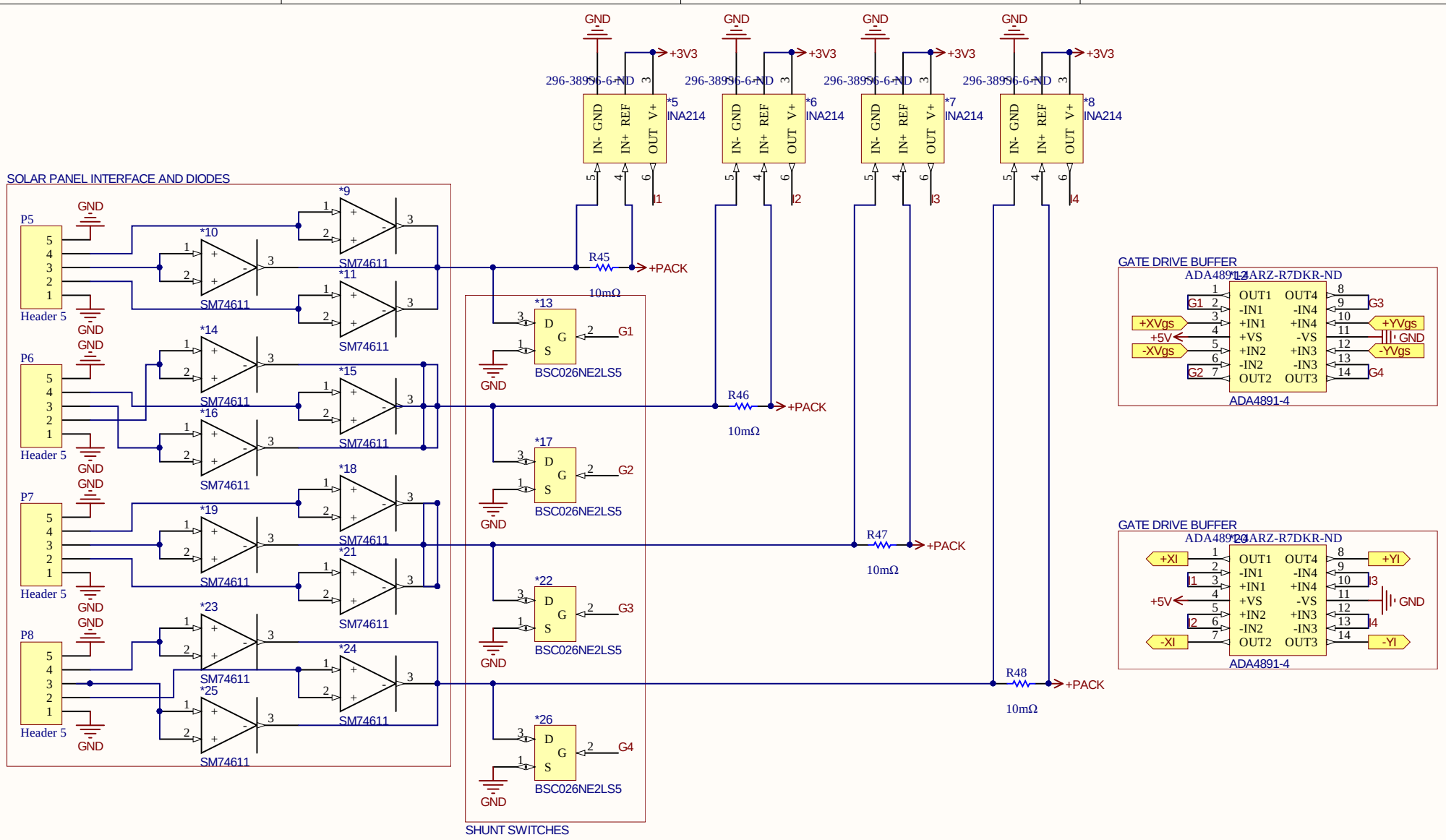
SOLAR PANEL INTERFACE AND DIODES
P5
P6
P7
P8
Header 5
GND
SM74611
*9
*10
*11
*14
*15
*16
*18
*19
*21
*23
*24
*25
SHUNT SWITCHES
*13
*17
*22
*26
BSC026NE2LS5
G1
G2
G3
G4
R45
R46
R47
R48
10mΩ
+PACK
+3V3
296-38956-6-ND
*5
*6
*7
*8
INA214
IN- GND REF IN+ OUT V+
I1
I2
I3
I4
GATE DRIVE BUFFER
ADA4891-4ARZ-R7DKR-ND
ADA4891-4
OUT1 OUT4
-IN1 -IN4
+IN1 +IN4
+VS -VS
+IN2 +IN3
-IN2 -IN3
OUT2 OUT3
+XVgs
-XVgs
+YVgs
-YVgs
+5V
+XI
-XI
+YI
-YI
Title
Size
A4
Number
Revision
Date: 2018-06-02
File: C:\Users\..\eps_pv.SchDoc
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Board S