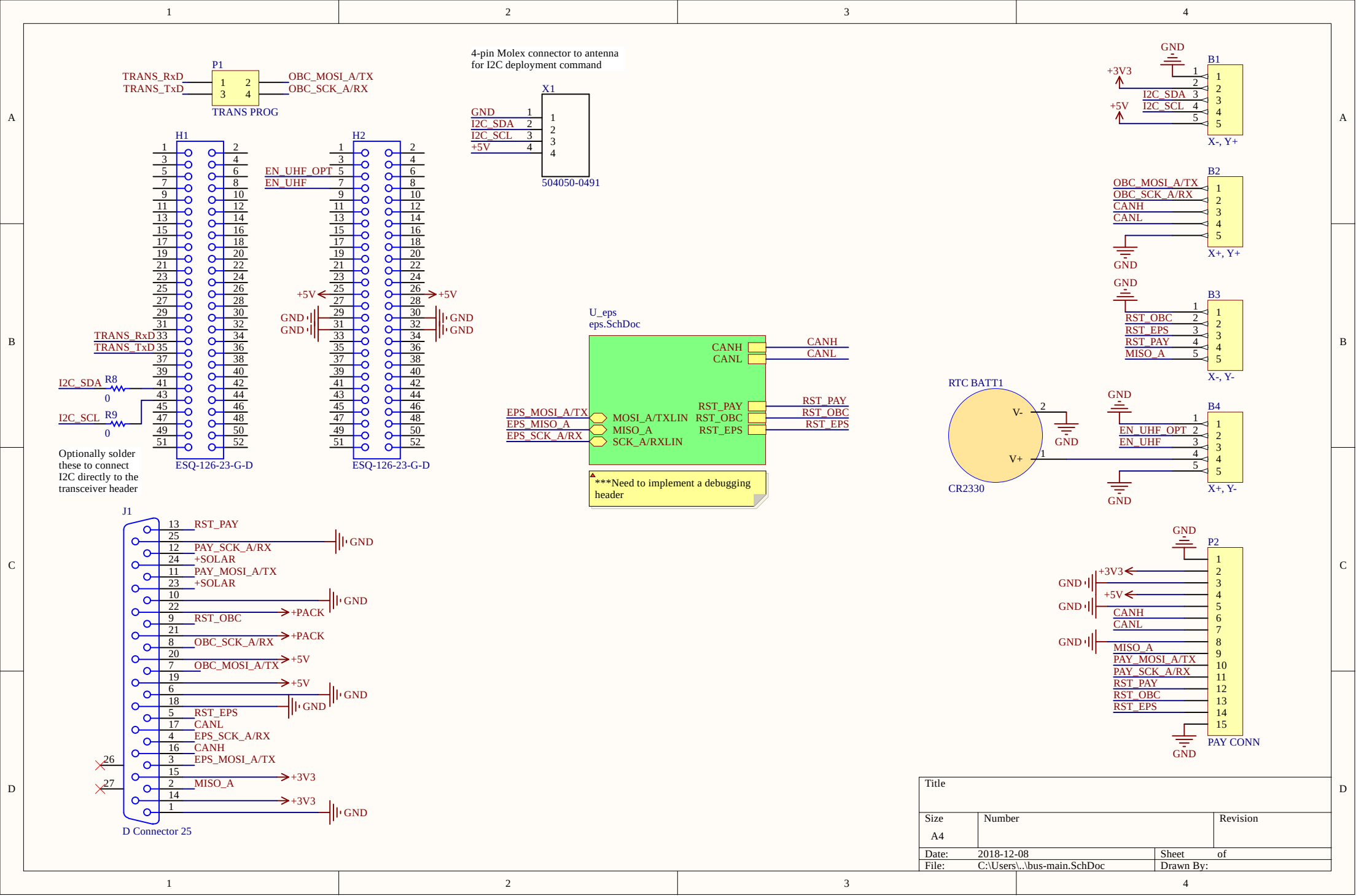
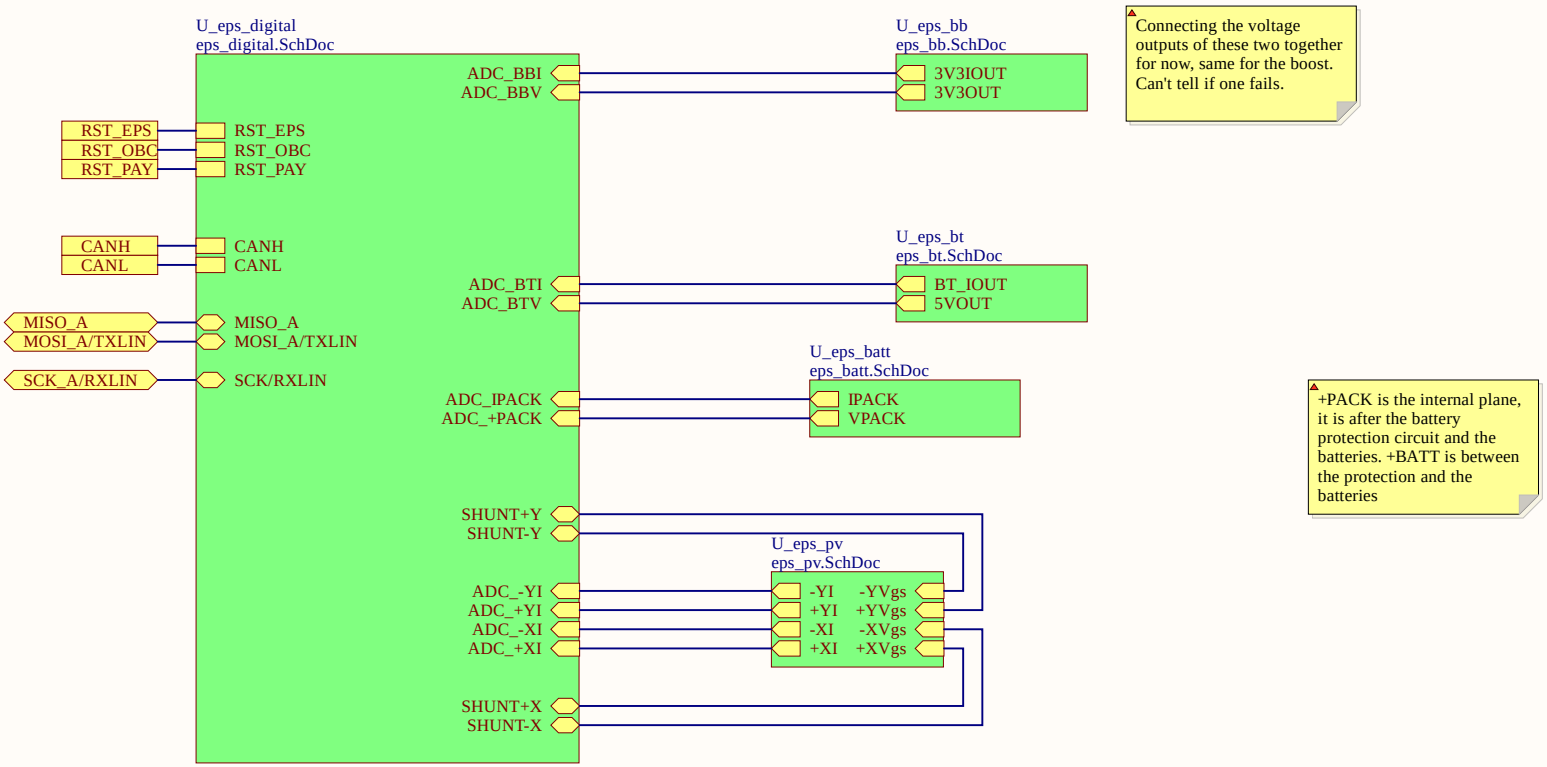
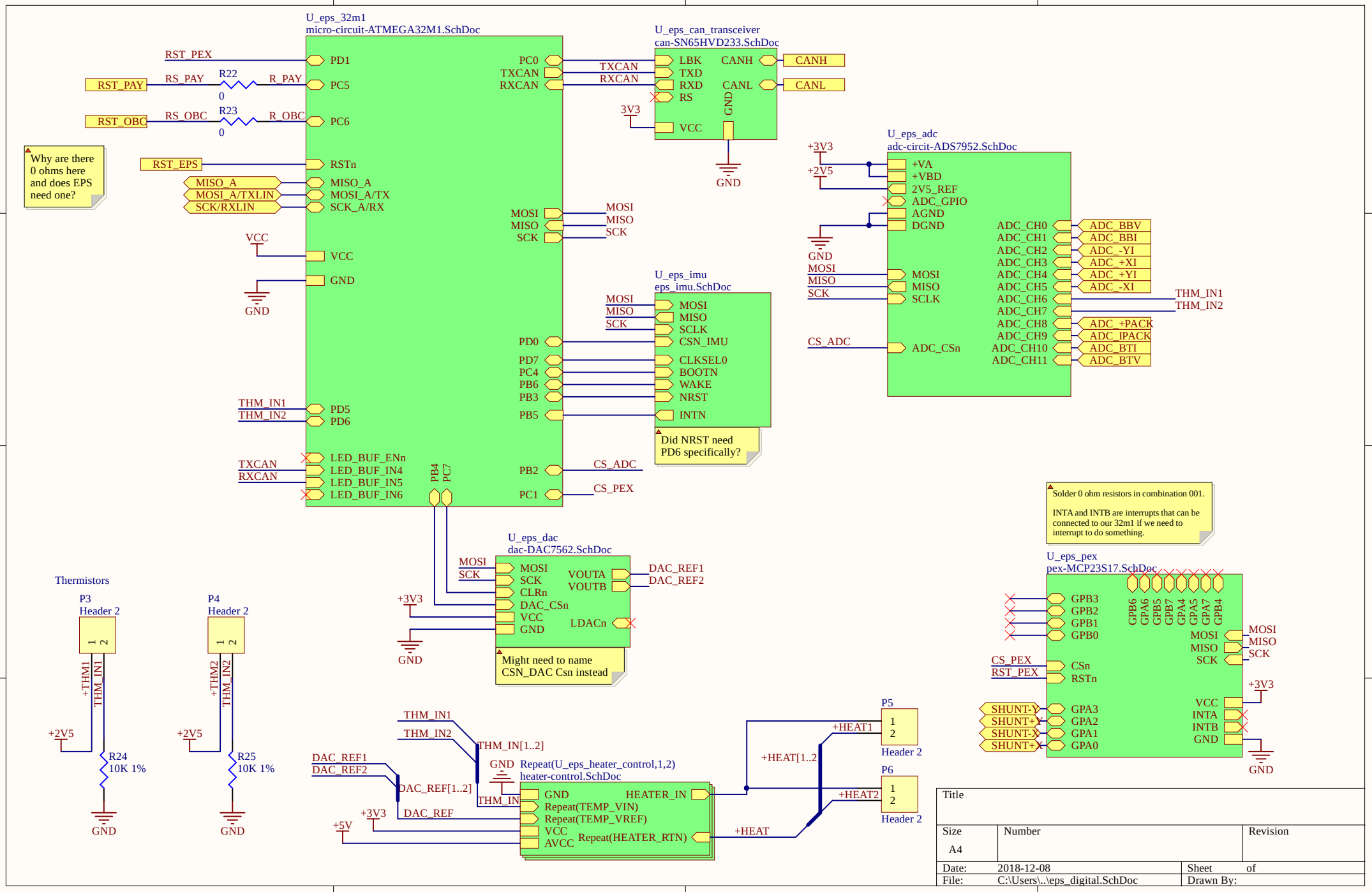
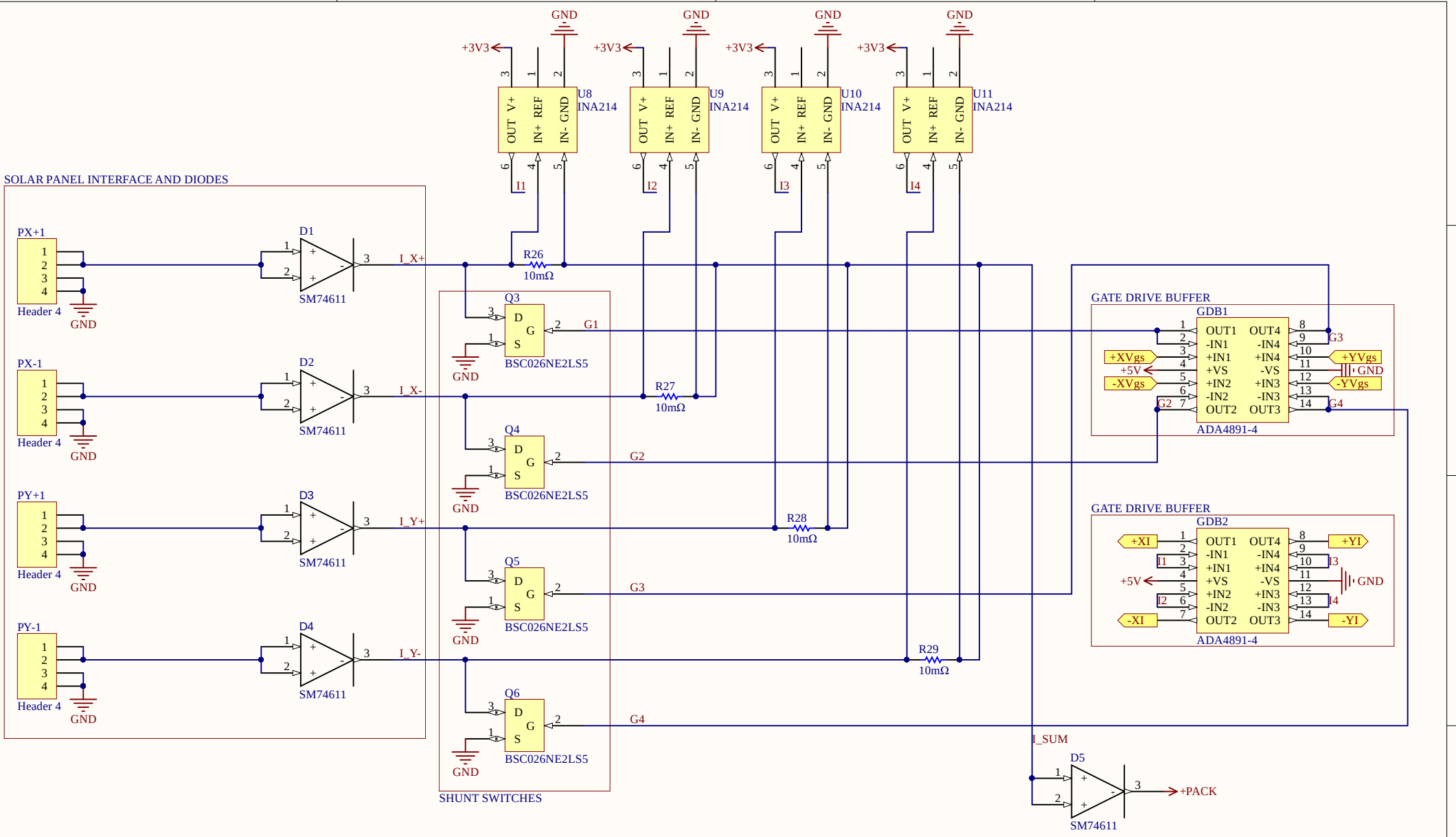

P1
TRANS_RxD
TRANS_TxD
OBC_MOSI_A/TX
OBC_SCK_A/RX
TRANS PROG
4-pin Molex connector to antenna for I2C deployment command
X1
GND
I2C_SDA
I2C_SCL
+5V
504050-0491
H1
H2
EN_UHF_OPT
EN_UHF
TRANS_RxD
TRANS_TxD
I2C_SDA
I2C_SCL
R8
R9
0
Optionally solder these to connect I2C directly to the transceiver header
ESQ-126-23-G-D
U_eps
eps.Schdoc
CANH
CANL
RST_PAY
RST_OBC
RST_EPS
EPS_MOSI_A/TX
EPS_MISO_A
EPS_SCK_A/RX
MOSI_A/TXLIN
MISO_A
SCK_A/RXLIN
***Need to implement a debugging header
B1
B2
B3
B4
X-, Y+
X+, Y+
X-, Y-
X+, Y-
RTC BATT1
CR2330
V-
V+
J1
D Connector 25
RST_PAY
PAY_SCK_A/RX
+SOLAR
PAY_MOSI_A/TX
+PACK
RST_OBC
OBC_SCK_A/RX
OBC_MOSI_A/TX
RST_EPS
CANL
EPS_SCK_A/RX
CANH
EPS_MOSI_A/TX
MISO_A
P2
PAY CONN
Title
Size
A4
Number
Revision
Date:
2018-12-08
Sheet
of
File:
C:\Users\..\bus-main.SchDoc
Drawn By:

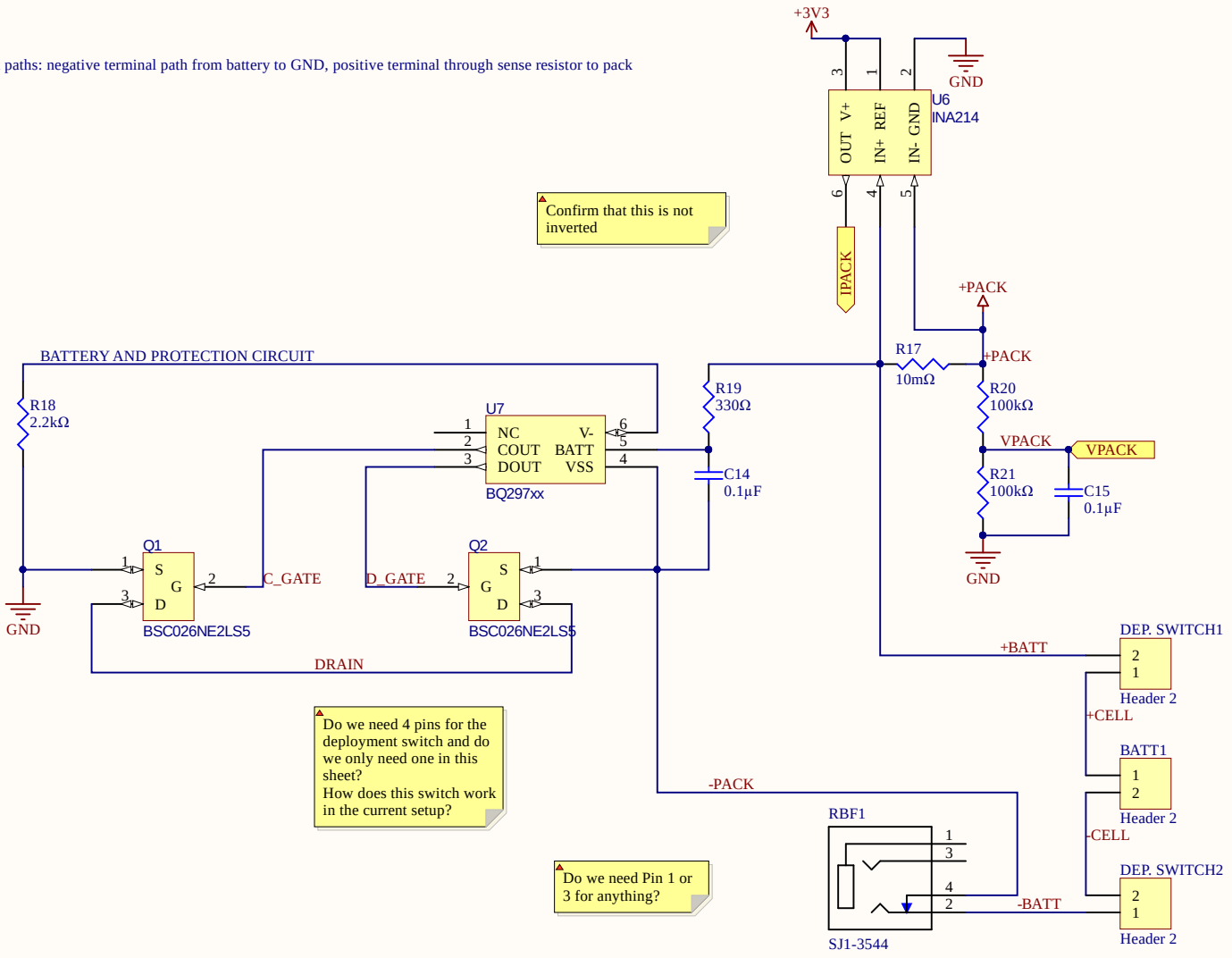


Title		
Size A	Number	Revision
Date: 2018-12-08		Sheet of
File: C:\Users\..\eps.SchDoc		Drawn By:

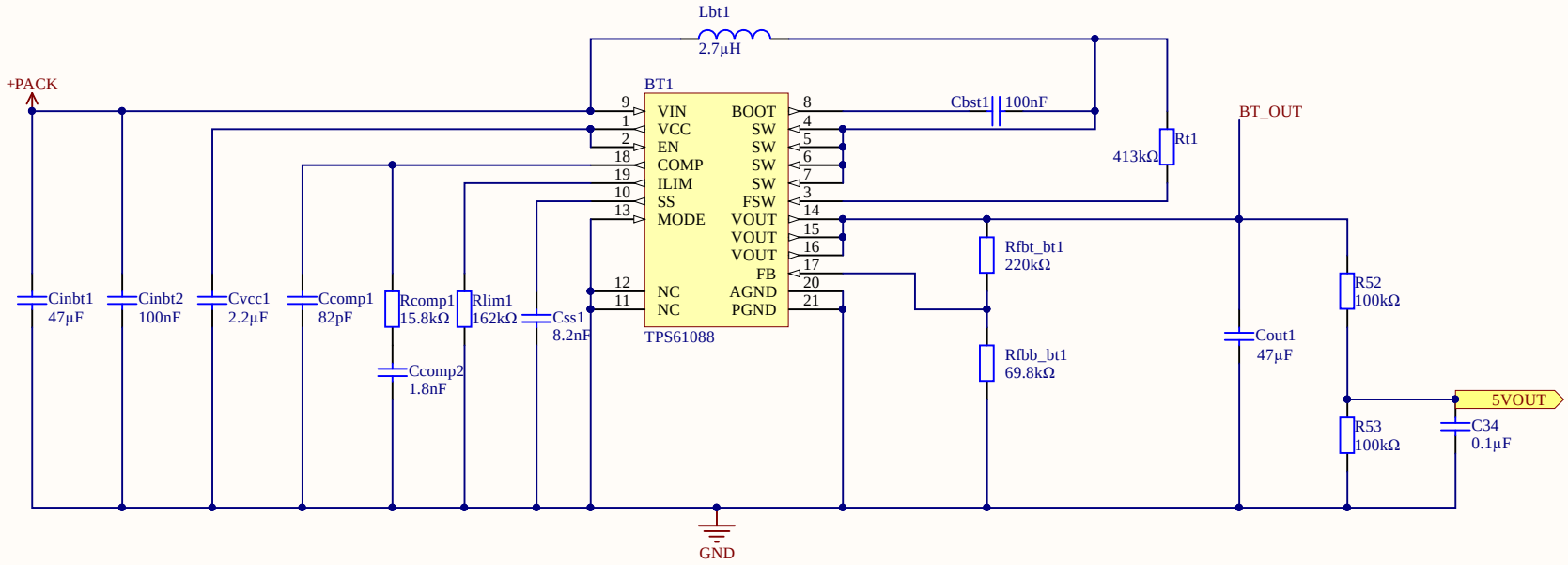

U_eps_32m1
micro-circuit-ATMEGA32M1.SchDoc
RST_PEX
RST_PAY
RS_PAY
R22
R_PAY
0
RST_OBC
RS_OBC
R23
R_OBC
0
Why are there 0 ohms here and does EPS need one?
RST_EPS
MISO_A
MOSI_A/TXLIN
SCK/RXLIN
VCC
GND
THM_IN1
THM_IN2
TXCAN
RXCAN
LED_BUF_ENn
LED_BUF_IN4
LED_BUF_IN5
LED_BUF_IN6
PB4
PC7
PD1
PC5
PC6
RSTn
MISO_A
MOSI_A/TX
SCK_A/RX
PD5
PD6
PC0
TXCAN
RXCAN
MOSI
MISO
SCK
PD0
PD7
PC4
PB6
PB3
PB5
PB2
PC1
CS_ADC
CS_PEX
U_eps_can_transceiver
can-SN65HVD233.SchDoc
LBK
TXD
RXD
RS
VCC
CANH
CANL
GND
3V3
U_eps_imu
eps_imu.SchDoc
MOSI
MISO
SCLK
CSN_IMU
CLKSEL0
BOOTN
WAKE
NRST
INTN
Did NRST need PD6 specifically?
U_eps_adc
adc-circit-ADS7952.SchDoc
+3V3
+2V5
+VA
+VBD
2V5_REF
ADC_GPIO
AGND
DGND
GND
MOSI
MISO
SCK
SCLK
CS_ADC
ADC_CSn
ADC_CH0
ADC_CH1
ADC_CH2
ADC_CH3
ADC_CH4
ADC_CH5
ADC_CH6
ADC_CH7
ADC_CH8
ADC_CH9
ADC_CH10
ADC_CH11
ADC_BBV
ADC_BBI
ADC_-YI
ADC_+XI
ADC_+YI
ADC_-XI
THM_IN1
THM_IN2
ADC_+PACK
ADC_IPACK
ADC_BTI
ADC_BTV
U_eps_dac
dac-DAC7562.SchDoc
MOSI
SCK
CLRn
DAC_CSn
VCC
GND
LDACn
VOUTA
VOUTB
DAC_REF1
DAC_REF2
+3V3
GND
Might need to name CSN_DAC Csn instead
Solder 0 ohm resistors in combination 001.
INTA and INTB are interrupts that can be connected to our 32m1 if we need to interrupt to do something.
U_eps_pex
pex-MCP23S17.SchDoc
GPB3
GPB2
GPB1
GPB0
GPB6
GPA6
GPB5
GPB7
GPA4
GPA5
GPA7
GPB4
MOSI
MISO
SCK
CS_PEX
RST_PEX
CSn
RSTn
+3V3
VCC
INTA
INTB
GND
SHUNT-Y
SHUNT+Y
SHUNT-X
SHUNT+X
GPA3
GPA2
GPA1
GPA0
Thermistors
P3
Header 2
P4
Header 2
+THM1
THM_IN1
+THM2
THM_IN2
+2V5
R24
10K 1%
R25
10K 1%
GND
THM_IN1
THM_IN2
THM_IN[1..2]
DAC_REF1
DAC_REF2
DAC_REF[1..2]
DAC_REF
THM_IN
+3V3
+5V
Repeat(U_eps_heater_control,1,2)
heater-control.SchDoc
GND
HEATER_IN
Repeat(TEMP_VIN)
Repeat(TEMP_VREF)
VCC
AVCC
Repeat(HEATER_RTN)
+HEAT
+HEAT[1..2]
+HEAT1
+HEAT2
P5
P6
Header 2
Title
Size
A4
Number
Revision
Date:
2018-12-08
Sheet
of
File:
C:\Users\..\eps_digital.SchDoc
Drawn By:

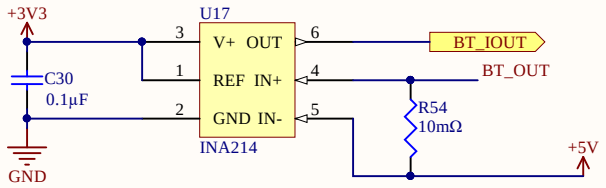

SOLAR PANEL INTERFACE AND DIODES
PX+1
PX-1
PY+1
PY-1
Header 4
GND
D1
D2
D3
D4
SM74611
I_X+
I_X-
I_Y+
I_Y-
+3V3
U8
U9
U10
U11
INA214
OUT V+ IN+ REF IN- GND
I1
I2
I3
I4
R26
R27
R28
R29
10mΩ
Q3
Q4
Q5
Q6
BSC026NE2LS5
G1
G2
G3
G4
SHUNT SWITCHES
GATE DRIVE BUFFER
GDB1
GDB2
ADA4891-4
+XVgs
-XVgs
+5V
+YVgs
-YVgs
+XI
-XI
+YI
-YI
I_SUM
D5
+PACK
Title
Size
A4
Number
Revision
Date: 2018-12-08
Sheet of
File: C:\Users\..\eps_pv.SchDoc
Drawn By:

High current paths: negative terminal path from battery to GND, positive terminal through sense resistor to pack

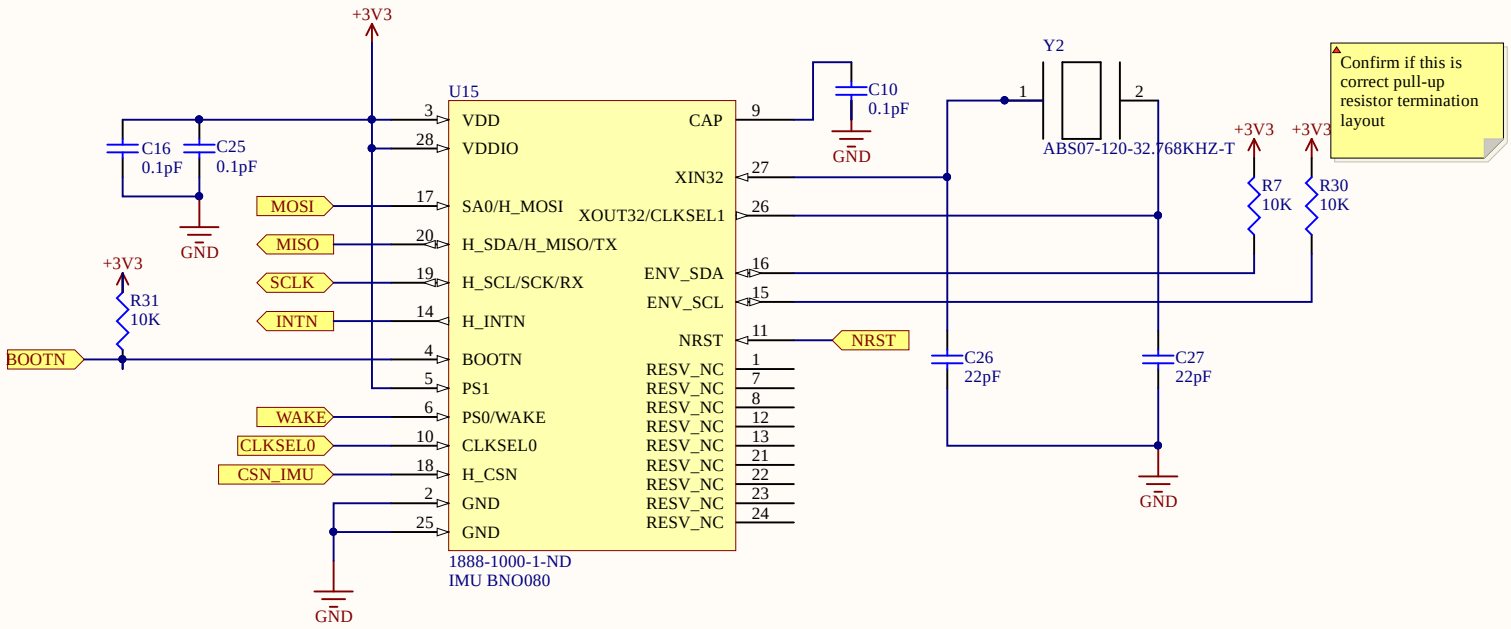


Title		
Size A4	Number	Revision
Date: 2018-12-08		Sheet of
File: C:\Users\..\eps_batt.SchDoc		Drawn By:





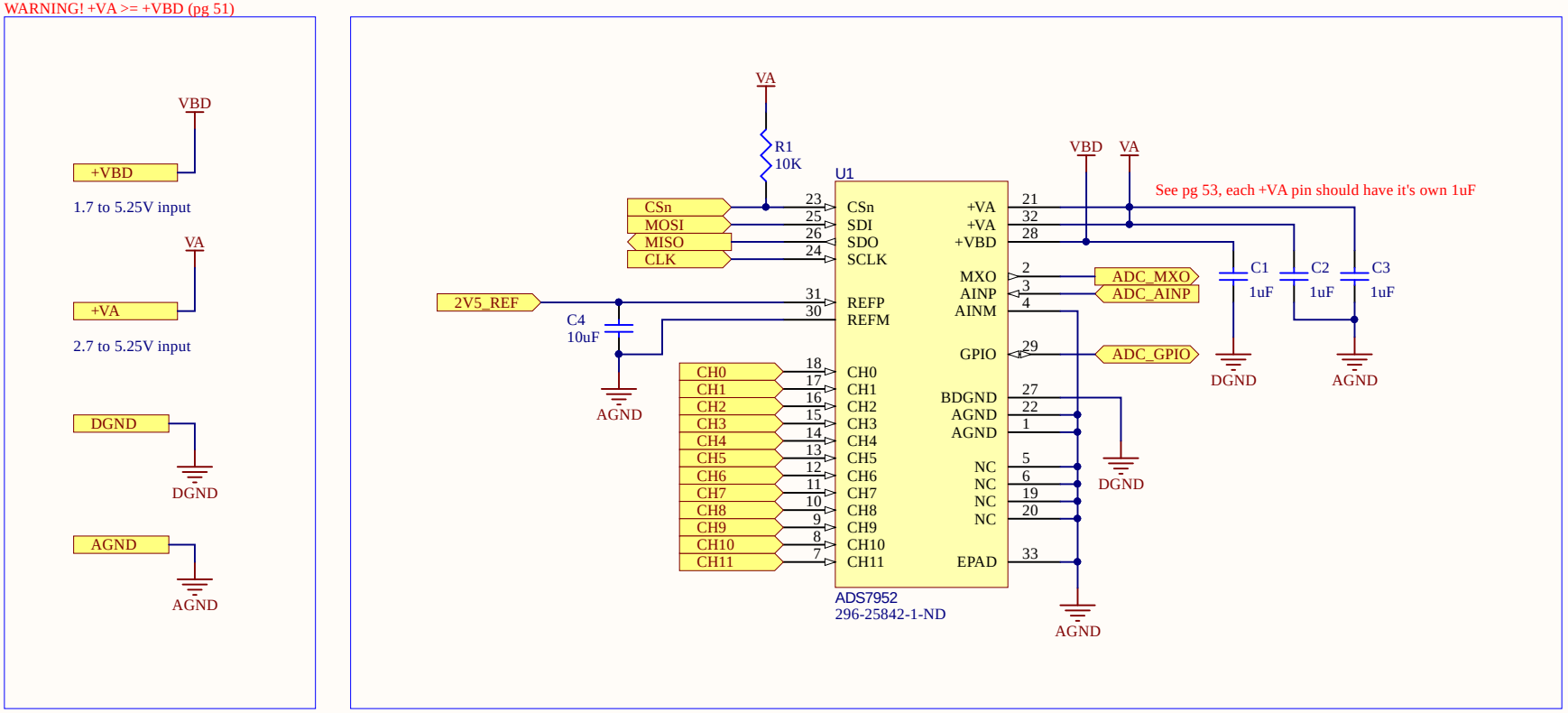
Title		
Size: A	Number	Revision
Date: 2018-12-08		Sheet of
File: C:\Users\..\eps_bt.SchDoc		Drawn By:



Title		
Size A	Number	Revision
Date: 2018-12-08		Sheet of
File: C:\Users\..\eps_imu.SchDoc		Drawn By:

POWER INPUTS

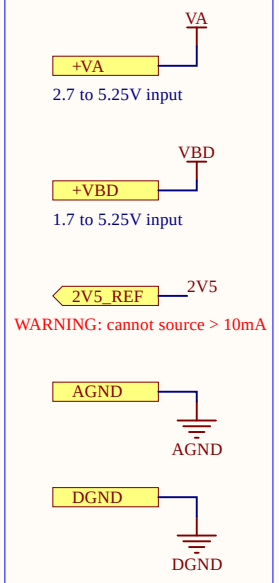
WARNING! +VA >= +VBD (pg 51)



Title	ADS7952	UTAT SS
Size	Number	Revision
A4	*	1.0
Date:	2018-12-08	Sheet * of *
File:	C:\Users\..\adc-ADS7952.SchDoc	Drawn By: Dylan Vogel

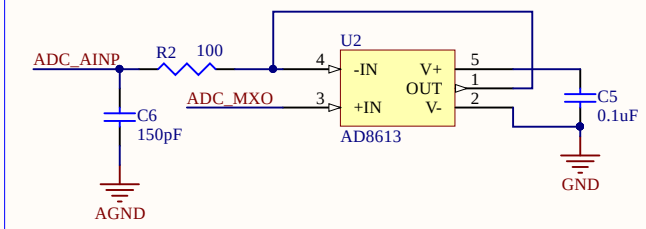
POWER PORTS

WARNING! +VA >= +VBD (pg 51)



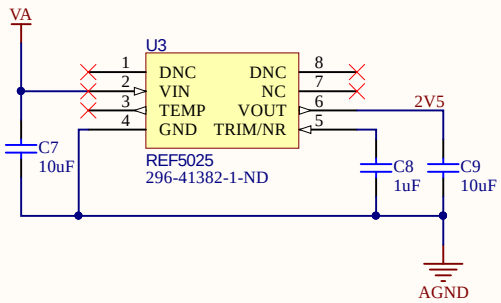
ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure

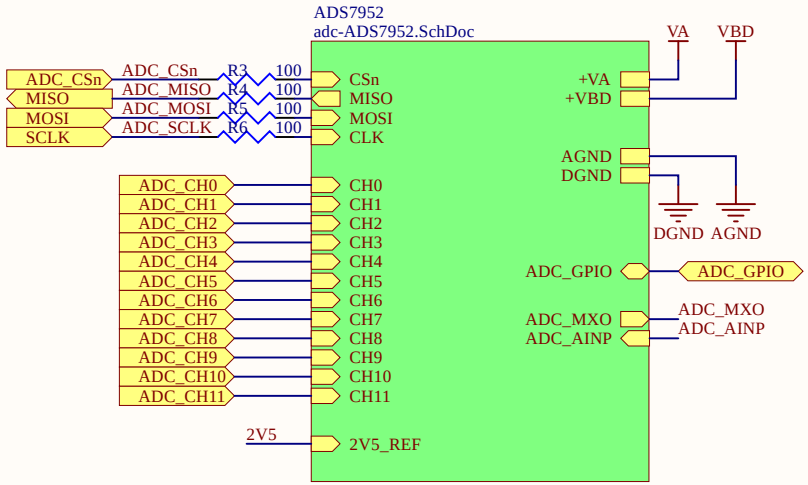


2V5 REFERENCE

Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)



ADC



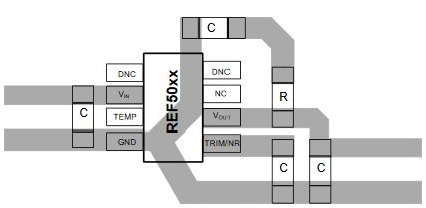


Figure 44. Layout Example

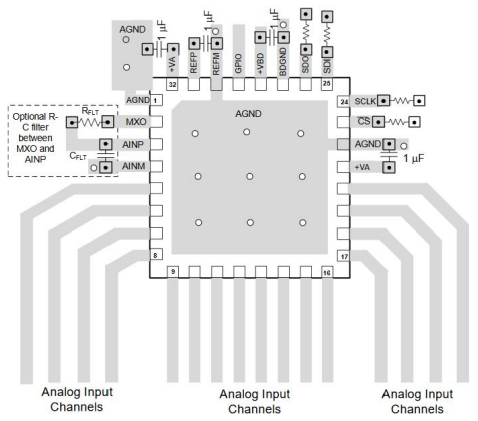
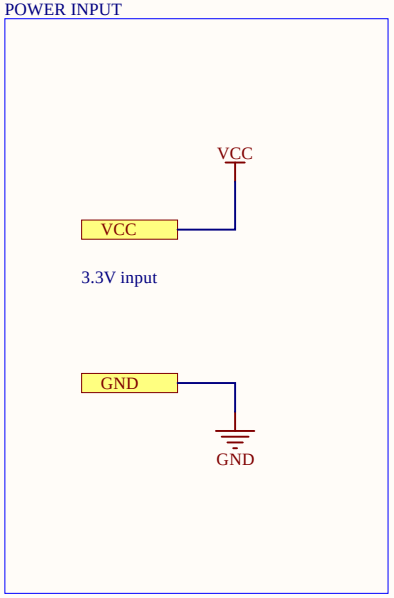


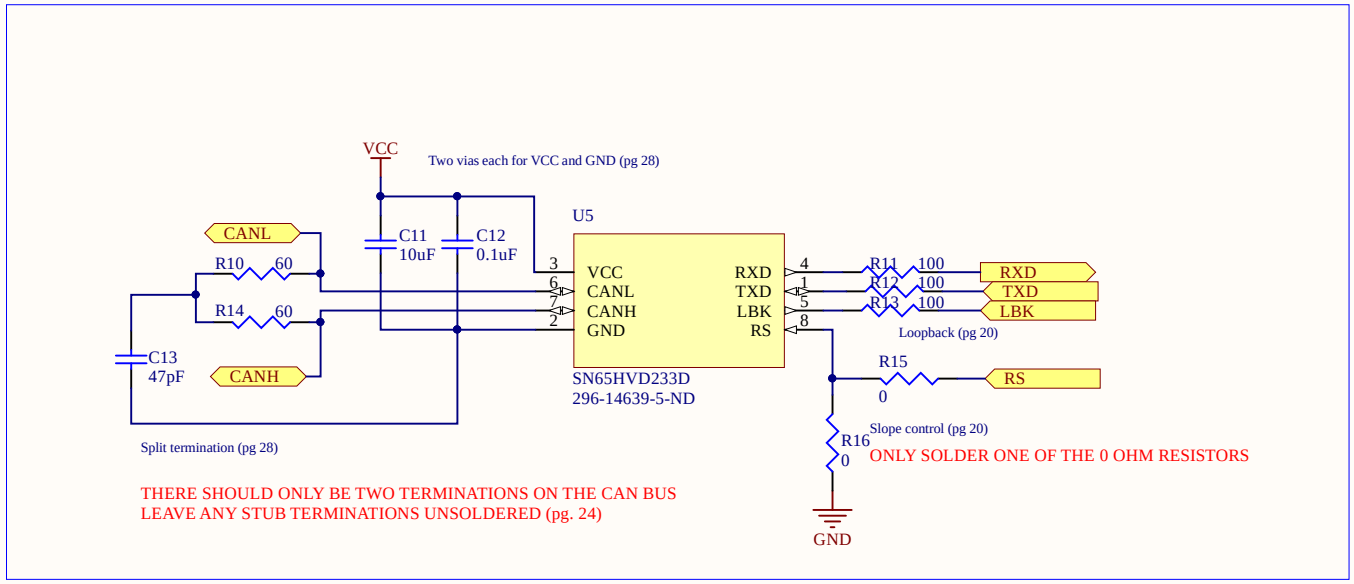
Figure 70. Recommended Layout for the VQFN Packaged Device

This schematic implements the ADS7952 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.
- Recommended input impedance should be < XX ohm. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7952 schematic
- In most low-performance applications, +VA and +VBD can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

Title: ADS7952 Circuit		UTAT SS
Size: A4	Number: *	Revision: 1.0
Date: 2018-12-08		Sheet * of *
File: C:\Users\..\adc-circit-ADS7952.SchDoc		Drawn By: Dylan Vogel

POWER INPUT





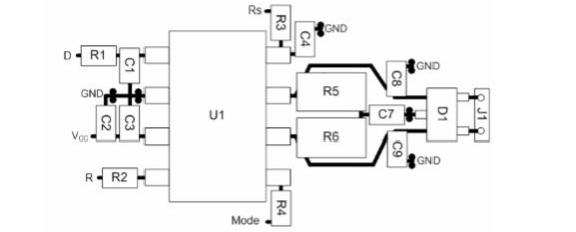


Figure 41. Layout Example Schematic

See pg. 28 of the datasheet for layout guidelines

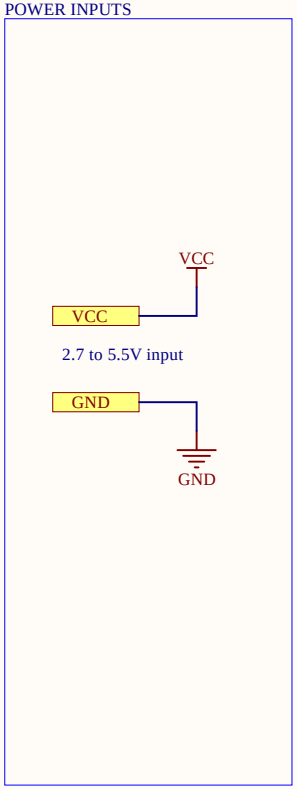
This schematic implements the SN65HVD233 CAN transciever with loopback control and two options for slope control.

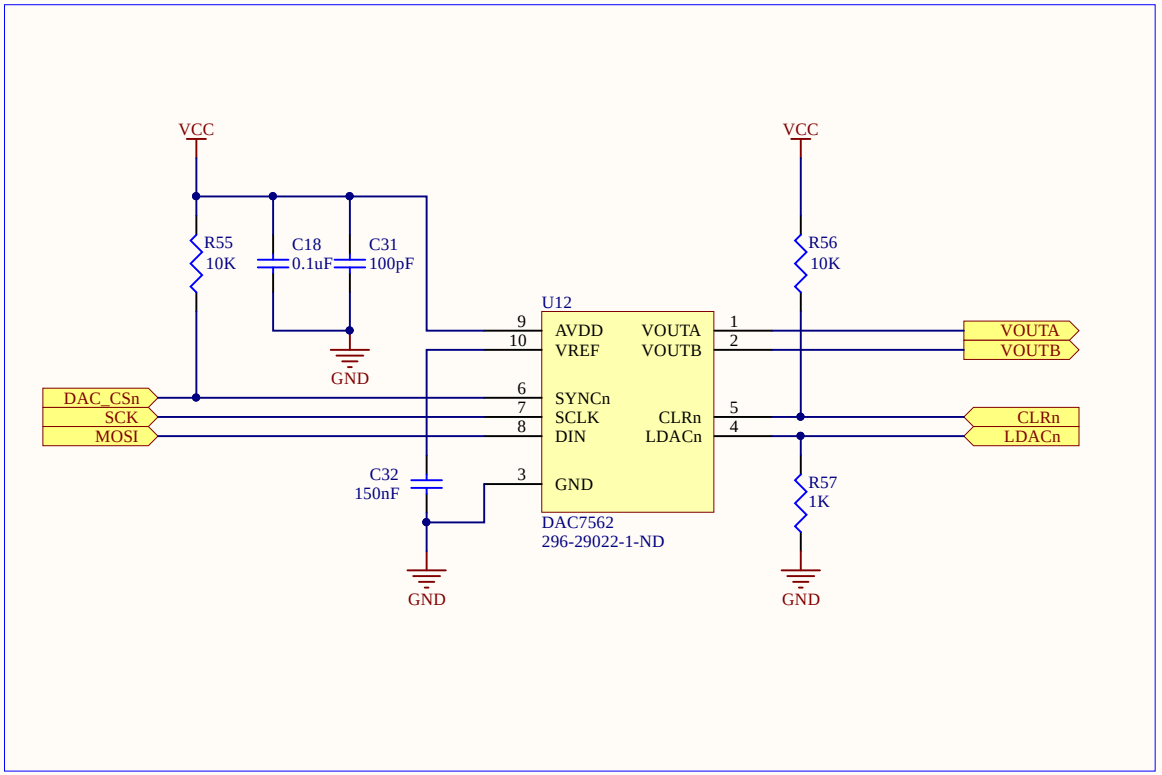
A 0 Ohm resistor can be soldered to GND to permanently put the device in High Speed mode (20 V / us slew), or a 0 Ohm resistor can be soldered to the RS port to control the device via an external uController. Connecting the RS pin to a uController allows the device to be put into low-power mode by setting a voltage high.

- Device is meant to be used in a 3.3 V system
- 100 Ohm current limiting resistors placed on the digital lines to minimize digital noise to the device
- Only two CAN transcievers on the bus should have 120 ohm terminations. Other devices should be placed on 'stub' networks where the terminations are left unsoldered

Title	SN65HVD233		UTAT SS
Size	Number		Revision
A4	*		1.0
Date:	2018-12-08	Sheet *	of *
File:	C:\Users\..\can-SN65HVD233.SchDoc	Drawn By:	Dylan Vogel

POWER INPUTS

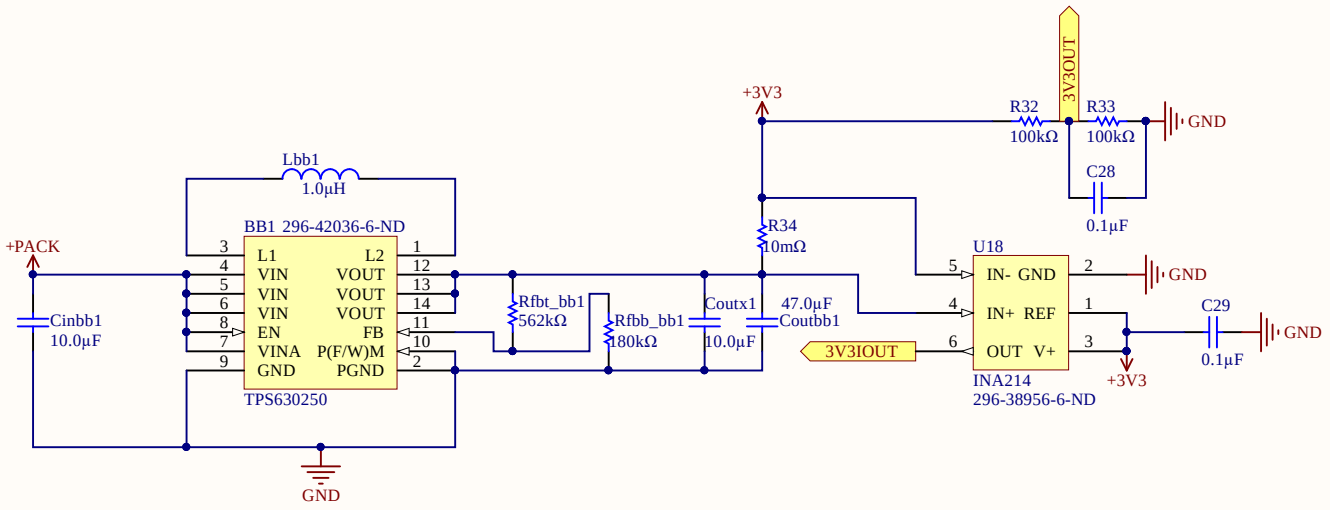




This schematic implements the DAC7562 16-bit digital-to-analog converter. The device has two configurable outputs, VOUTA and VOUTB, which can be digitally written through the 3-wire SPI interface. This particular device is set to zero scale (0V) both outputs upon power-on/reset. Toggling CLRn to LOW via an external GPIO will also zero both outputs.

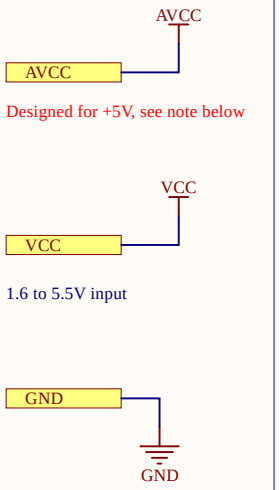
The device is connected in synchronous mode, where LDACn is connected to GND through a strong pull-down. This means that output VOUTA/VOUTB will be updated at the end of the SPI communication frame. The alternative would be to connect LDACn to a microcontroller GPIO and toggle it low manually to set all outputs at the same time. This is referred to as asynchronous mode in the datasheet.

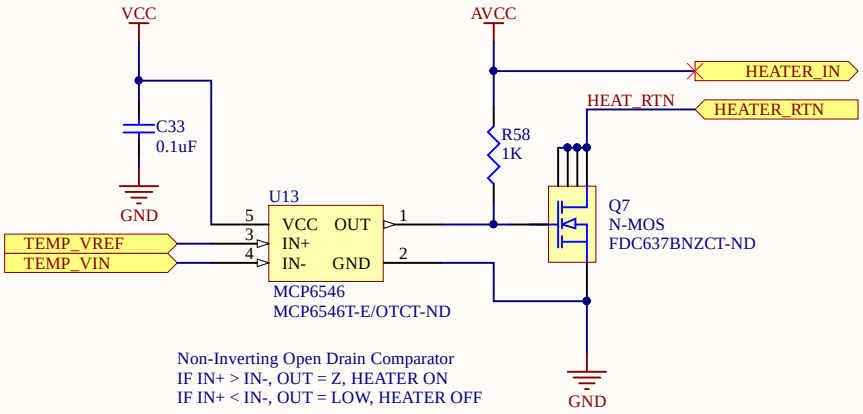
Title	DAC7562	UTAT SS
Size	Number	Revision
A4	*	1.1
Date:	2018-12-08	Sheet * of *
File:	C:\Users\..\dac-DAC7562.SchDoc	Drawn By: Dylan Vogel



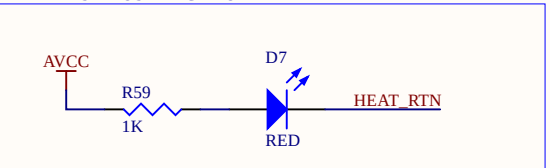
Title		
Size: A4	Number	Revision
Date: 2018-12-08		Sheet of
File: C:\Users\..\eps_bb.SchDoc		Drawn By:

POWER INPUTS





LED HEATER STATUS INDICATION



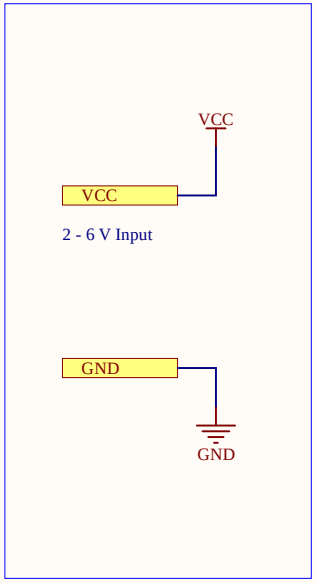
This schematic implements a single heater control circuit, relying on an open-drain comparator and NMOS switch for completely analog operation.

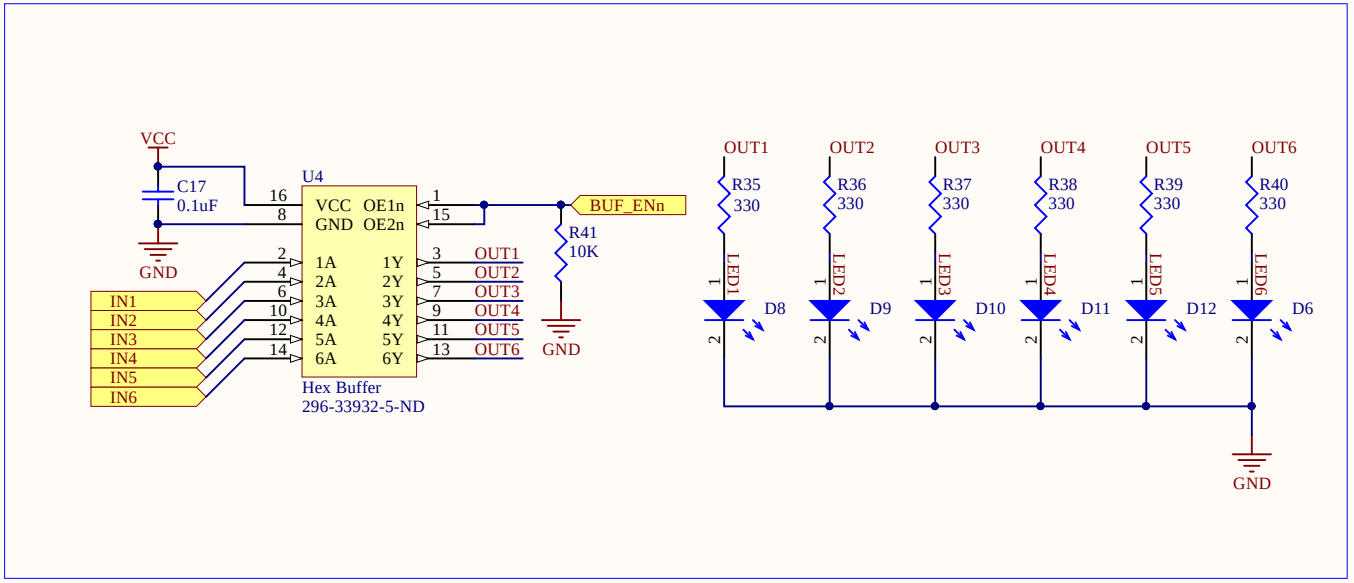
The temperature setpoint is set via the voltage on the TEMP_VREF pin, which is compared against the voltage on the TEMP_VIN pin. If the voltage on TEMP_VREF is higher, the output of the comparator will go high-impedance and drive the gate of the NMOS to 5V through the 1K pull-up resistor. This should be enough to switch the MOSFET in triode with a relitively low VDS at our target current (128mA).

Conversely, when TEMP_VIN is above TEMP_VREF, the output is switched to GND and the MOSFET turns off. How you decide to set TEMP_VREF and TEMP_VIN is entirely up to you.

The circuit is designed to work at 5V. To operate at different voltages, just be sure to check the relevant ratings on the different components.

Title: Heater Control *		
Size: A	Number: *	Revision: 1
Date: 2018-12-08		Sheet * of *
File: C:\Users\..\heater-control.SchDoc		Drawn By: B. Almeida, D. Vogel



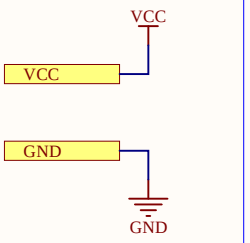


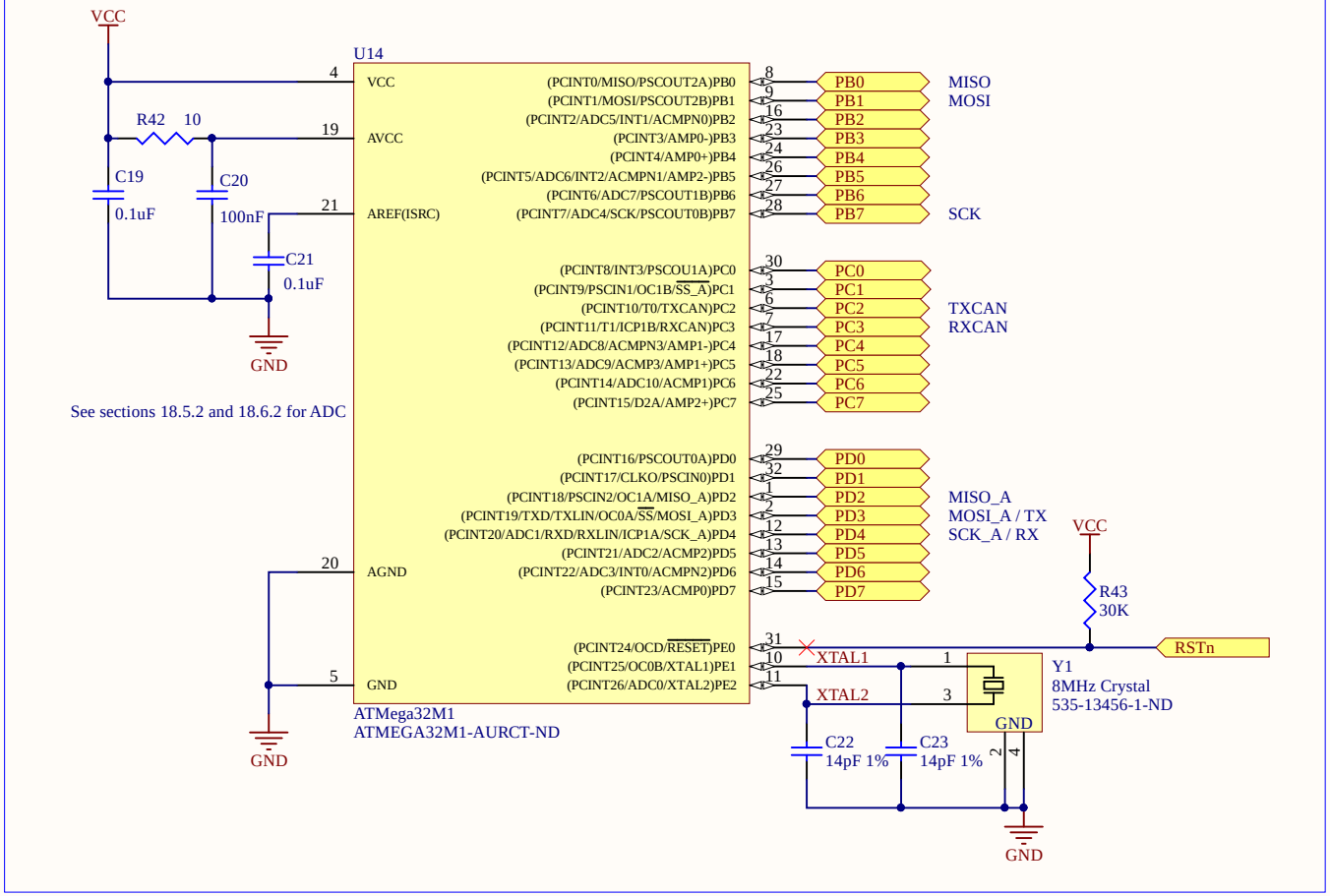
This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF_ENn input can be connected to a mircocontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

Title: SN74HC365PW LED Monitoring		UTAT SS
Size: A4	Number: *	Revision: 1.0
Date: 2018-12-08	Sheet * of *	
File: C:\Users\..\led-monitoring-SN74HC365PW.SchDoc	Drawn By: Dylan Vogel	

POWER INPUT



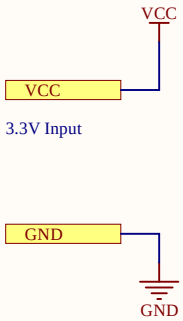


This schematic implements the ATMega32M1 microcontroller with a 8 MHz external crystal and necessary power connections.

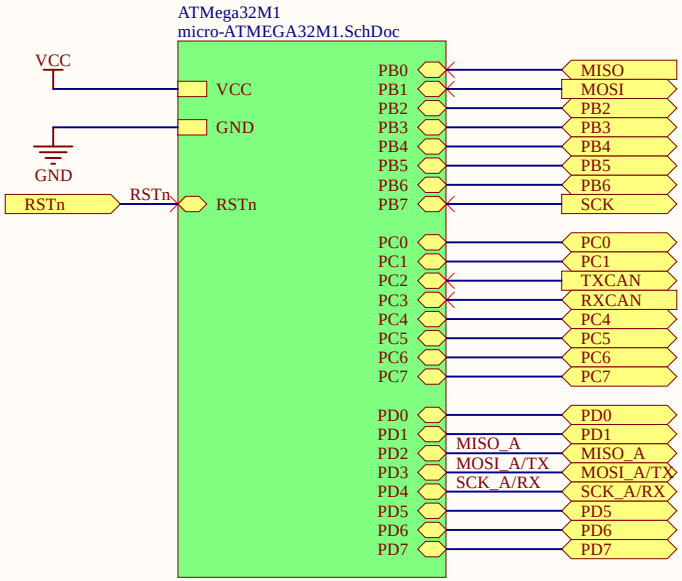
- Crystal is connected in a Pierce configuration, values of the capacitors were calculated based on the capacitance of the crystal and ESR.
- I would read through 18.5.2 and 18.6.2 of the complete 32M1 datasheet if you're interested in the motivation behind the ADC input connections. They recommend connecting AVCC through a RC lowpass network to minimize noise.
- If the ADC functionality of the device is used, either AVCC or the internal 2.56 V source can be seleted in software as the reference voltage.

Title: ATMega32M1		UTAT SS
Size: A4	Number: *	Revision: 1.0
Date: 2018-12-08	Sheet * of *	
File: C:\Users\..\micro-ATMEGA32M1.SchDoc	Drawn By: Dylan Vogel	

POWER INPUTS

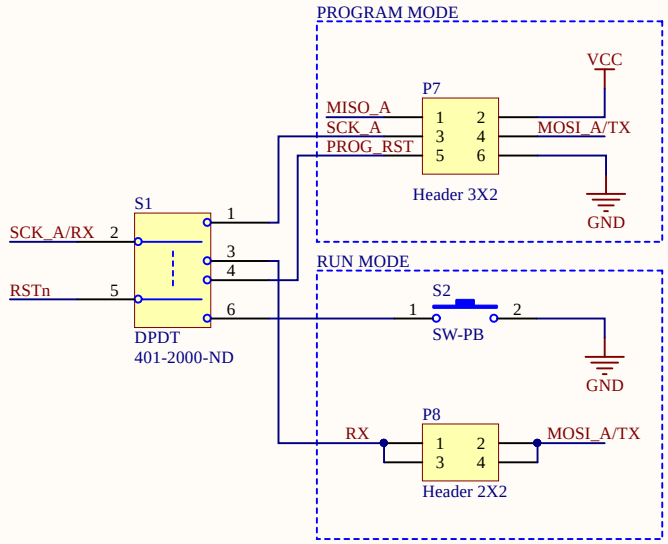


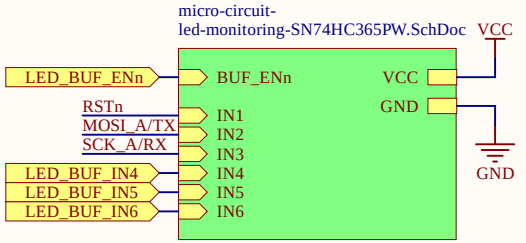
ATMEGA32M1



Specific No-ERCs placed for I/O Port and Bidirectional Sheet Entry

MODE SELECT CIRCUITRY

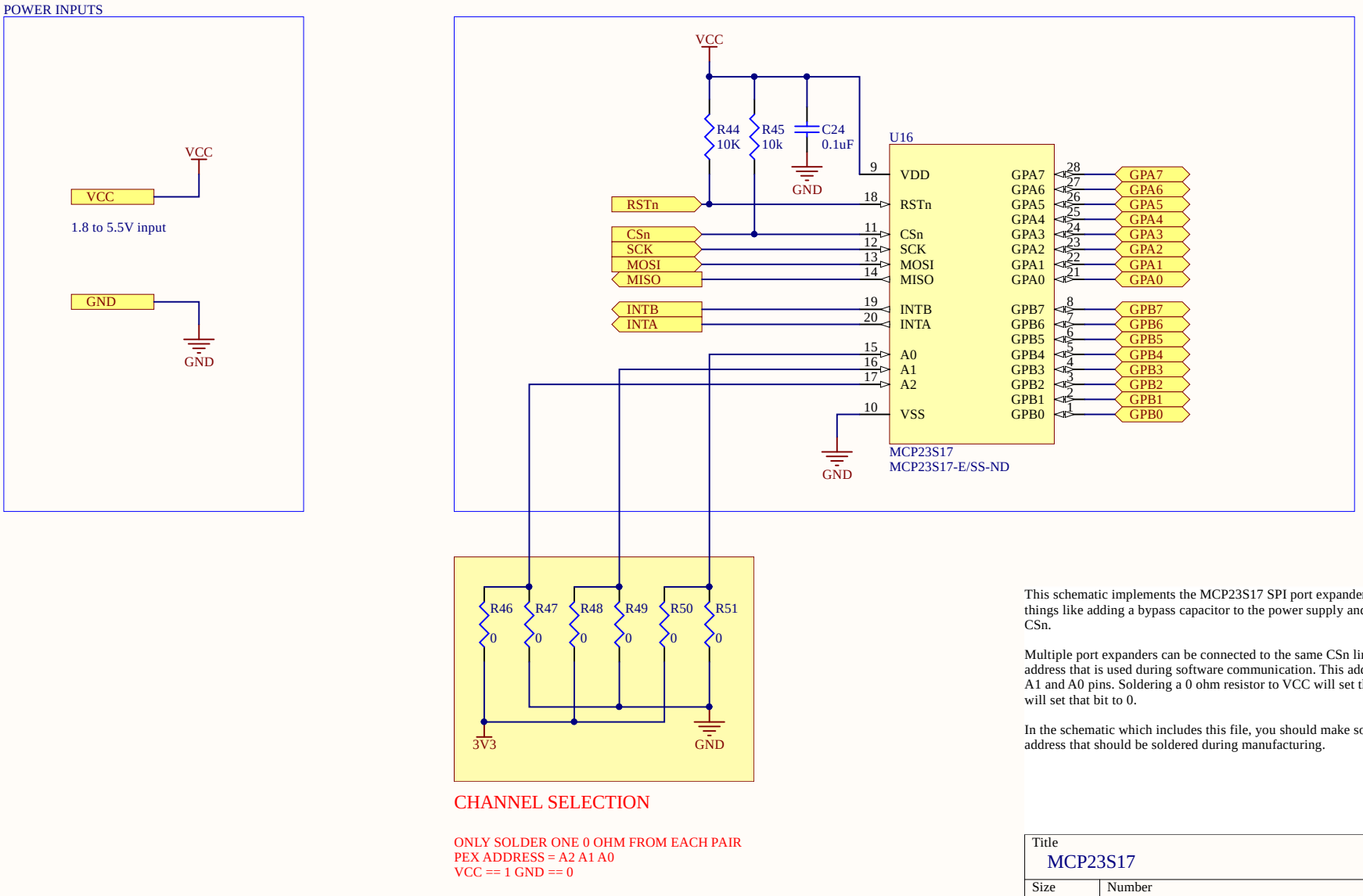




This schematic extends the functionality already included in the micro-ATMEGA32M1 schematc, adding a mode select switch, programming header, reset button and LED indication for TX, RX and RSTn.

- IN[4:6] of the LED buffer have been left unconnected, but are broken out on ports LED_BUF_IN[4:6]. They can be connected in the schematic which includes this sheet to monitor up to an additional 3 lines. Highly recommend more blinking lights.

Title: ATMega32M1 Circuit		UTAT SS
Size: A4	Number: *	Revision: 1.0
Date: 2018-12-08	Sheet * of *	
File: C:\Users\..\micro-circuit-ATMEGA32M1.SchDoc	Drawn By: Dylan Vogel	



This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RSTn and CSn.

Multiple port expanders can be connected to the same CSn line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

Title	MCP23S17	UTAT SS
Size	Number	Revision
A4	*	1.0
Date:	2018-12-08	Sheet * of *
File:	C:\Users\..\pex-MCP23S17.SchDoc	Drawn By: Dylan Vogel