

DUNE ColdADC ASIC Preliminary Testing Results

Authors go here

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DUNE Electronics Consortium

Abstract

The DUNE ColdADC is a 16-channel low-noise ADC ASIC designed to read out the LArASIC preamps in the DUNE Liquid Argon Far Detectors. The resolution of the ADC is 12-bits and it digitizes at a rate of 2MS/s/channel. The ADC accepts single-ended or differential inputs and outputs digitized data to COLDATA, the DUNE digital data aggregator/serializer chip.

In this document, we present the preliminary performance studies on the first version of the ColdADC ASIC. The prototype ColdADC has already achieved a performance that essentially meets the DUNE noise, linearity, and power requirements. We will also discuss some of the issues found during the functional tests and the plan to mitigate them in the next revision of the ASIC.

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1 Introduction [Grace/Lin]

The DUNE ColdADC is a digitizer ASIC intended for operation in the Deep Underground Neutrino Experiment (DUNE) Far Detectors. It will operate immersed in Liquid Argon (LAr) and will need to operate reliably, without any servicing or component replacement, for over 30 years at a temperature of 88 K.

The ColdADC was implemented in 65 nm CMOS by a team comprised of engineers from Fermilab (FNAL), Brookhaven National Laboratory (BNL), and Lawrence Berkeley National Laboratory (LBNL). The prototype was submitted for fabrication in late 2018 and received in early 2019. Evaluation is ongoing.

The first prototype meets essential requirements. The key performance specification, noise, is as expected. The prototype is currently being integrated into a new revision of the DUNE Far Detector Front-End Mother Board (FEMB). Preliminary results are good, and the DUNE Far Detector FEMB is displaying better noise performance than the SBND FEMB, which uses a Commercial Off-the-Shelf (COTS) ADC. This enables the use of a lower gain setting in LArASIC and thus larger dynamic range. The key specifications of the ColdADC compared to the measured results are presented in Table 1.

Specification	Value	Result	Note
Operation Temperature	Room Temp. (RT) and 88 K	Success	
Sampling Rate	2 MHz	2 MHz	
Noise	200 μ V-rms	189 μ V-rms	@ LN ₂ temp
Differential Non-linearity (DNL)	\pm 0.5 LSB (at 12-bit level)	+0.2 to -0.5 LSB	@LN ₂ ; typical values
Integral Non-Linearity (INL)	\pm 1 LSB (at 12-bit level)	+1.2 to -1.1 LSB	@LN ₂ , typical values
Effective-Number-of-Bits (ENOB)	11.0 bits	<mean>=10.6 bits rms=0.3 bits	@ LN ₂
No Missing Codes Across Dynamic Range	N/A	Success	@LN ₂ and RT
Crosstalk	No Specification	< 1%	

Table 1: Summary of Results

In order to mitigate the hot carrier effect (and ensure long operational lifetime at 88 K), the circuits in the ColdADC prototype are designed with a minimum transistor channel length 50% longer than the minimum length allowed by the process, and the power supplies are kept at 10% below their nominal values. To follow this rule, the synthesized digital circuits use a custom standard cell library with longer transistors than the foundry-supplied library. In addition, the architecture of the ADC was chosen as the Pipelined ADC, whose performance depends primarily on the matching of ratioed capacitors. Studies conducted by BNL showed capacitor performance degraded less than active devices under cold conditions.

2 Test Setup

The first prototype of the ColdADC ASIC has been undergoing evaluation at BNL, FNAL and LBNL since early 2019. In addition to validating the portion of the ASIC that they designed, the three labs also worked collaboratively to cross-check the key performance results and debug issues. In this section, we will describe the setup used for testing the ColdADC.

2.1 Cryogenic Test System (CTS) [Lin]

One of the cryogenic equipments used in ColdADC testing is the Cryogenic Test System (CTS), shown in Figure 1. The CTS is a cryogenic test chamber mounted on top of a commercial LN₂ dewar. The device-under-test (e.g. ColdADC chip) can be mounted inside the test chamber and immersed in LN₂. The CTS can also circulate either cold or warm gas to slowly cool down or warm up the ASIC before and

after testing. The CTS has been effective at minimizing water condensation on the ASIC from thermal cycling. Multiple CTS units were built by a group from Michigan State University and distributed to the various testing sites.



Figure 1: Cryogenic Test System.

2.2 BNL Test System [Gao]

The block diagram of the ColdADC test board at BNL is shown in the Figure 2. There are two types of ColdADC test board at BNL. The first type can have either ColdADC die directly wire-bonded on board or packaged chip populated on the board. The purpose of this board is for ColdADC performance characterization, as shown in Figure 3. The second type has an ASIC test socket mezzanine on the test motherboard, which is aimed for the QC test, as shown in Figure 4.

The test motherboard hosts a P1/P2 LArASIC chip, a ColdADC chip (or die, or ASIC socket mezzanine), a few cold regulators and some passive components (capacitors, resistors and connectors). There are two features different from Fermilab and LBNL test boards. First, this is a test board which can characterize ColdADC performance with the FE-ASIC chip, a full chain from analog detector signal input to digital output is implemented. By using signal generator, we can also characterize standalone ADC performance, including power consumption, INL/DNL, ENOB, DC noise, etc. Second, ColdADC can be powered either by on-board regulators or directly by external power supply, which is not shown in Figure 2. On-board regulators can provide extremely low noise power sources for the test board, which is suitable for noise-sensitive measurements, such as the full chain performance characterization test. Inputs of ColdADC chip can be connected either to FE-ASIC outputs or signal generator outputs.

To minimize the design effort, a ProtoDUNE FM (FPGA mezzanine board) is adopted to configure LArASIC/ColdADC and read data out. The FM communicates with computer through Gigabit Ethernet, and UDP protocol is used.

As shown in Figure 5 is the test setup for ADC performance characterization. Low noise power supply Keysight E36312A is used if ColdADC is powered directly by external power supply. There

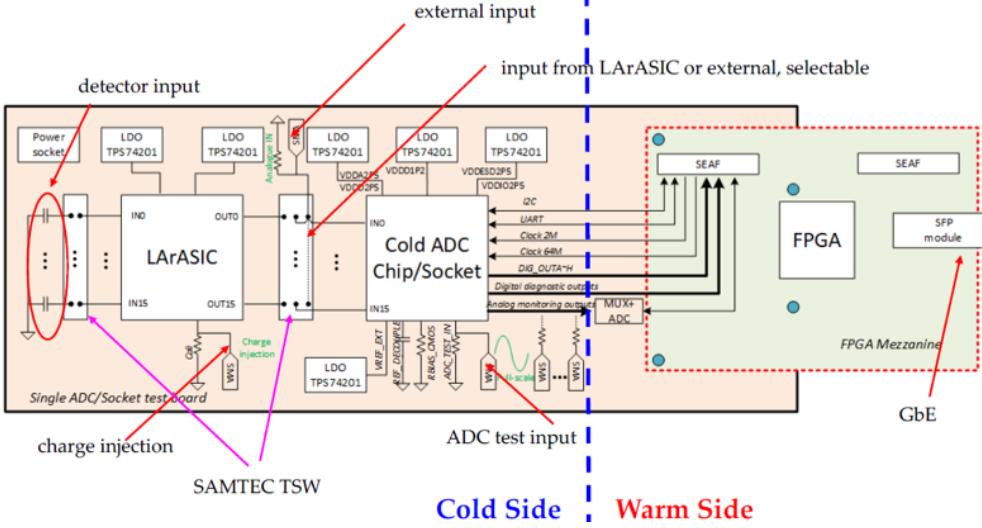


Figure 2: Block diagram of the BNL ColdADC test board

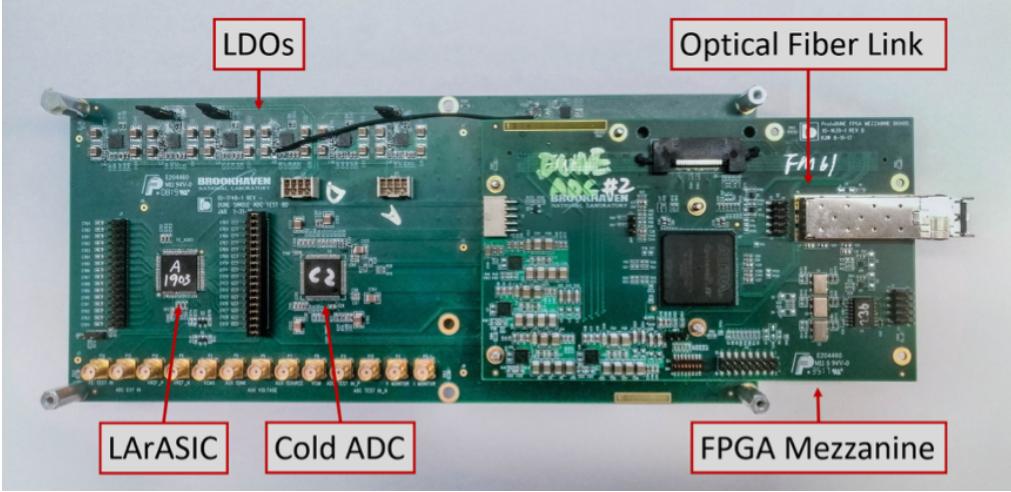


Figure 3: Test board with packaged ColdADC chip. To avoid unexpected noise from computer, a 1-port fiber to copper switch is inserted between FM and the computer.

are 3 different power rails for ColdADC, VDDA2P5/VDDD2P5 is set to 2.5V if CMOS reference is chosen and 2.7V if BJT reference is chosen, VDD1P2 is set to 2.1V, and VDDIO2P5 is set to 2.25V. The power consumption of ColdADC can be measured by power supply. E36312A provides a flexible way to adjust voltages for ColdADC but the noise is not as low as on-board regulators, so for precision measurements, on-board regulators should be used. Power supply Rigol DS832 provides two power rails (5.0V and 2.8V) for both ColdADC test motherboard and FPGA mezzanine. All on-board regulators are powered by DS832. SRS DS360 is an ultra-low distortion function generator with 20-bit resolution and THD lower than -100 dBc, which is sufficient to study ADC INL/DNL and ENOB performance. In addition, we also have a Keysight 33600A generator (14-bit resolution) to provide both ramp and sine waveforms for INL/DNL study if needed (actually in the beginning 33600A was used to characterize INL/DNL with ramp waveform). In order to study ADC dynamic performance such as ENOB, FM outputs 10MHz clock to synchronize SRS360. (Later in the QC test, instead of 100MHz oscillator on board, the CG635 synthesized clock generator is applied to provide a stable 100MHz clock source which is not affected by temperature change, and CG635 outputs a 10MHz clock to synchronize SRS360).

Python scripts are implemented to communicate with FPGA mezzanine via UDP protocol and analyze the data collected. A Python-based GUI interface was implemented to display real-time output.



Figure 4: Test board assembly with ColdADC socket mezzanine. The socket test motherboard can be treated as a minor revision of chip/die test motherboard. The socket test motherboard integrates MICA 150pF capacitors at the FE inputs to simulate the capacitance of 8m detector sense wire, which makes the full chain characterization close to the real experiment with the detector.

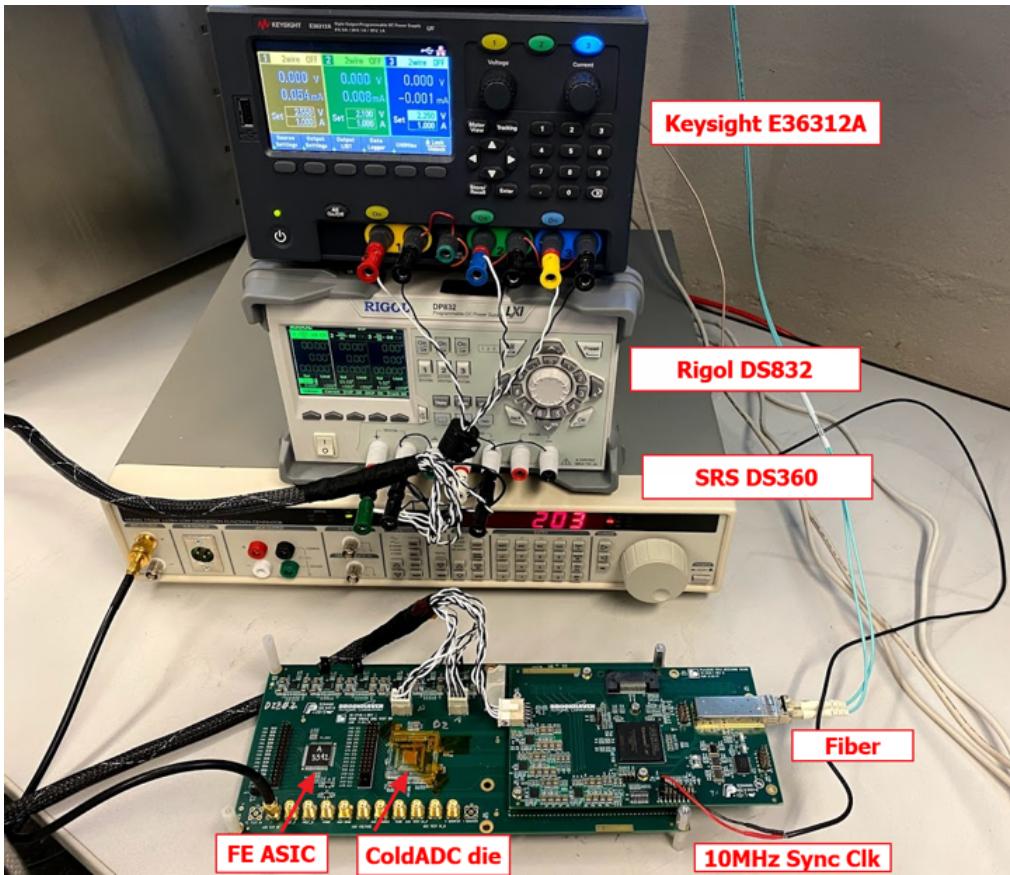


Figure 5: BNL ColdADC (die or chip) test setup.

A similar test setup is built for the QC procedure which is described in Section 6.1. The SFP module on FM cannot work in liquid nitrogen temperature, if cold test is conducted, half of the test board assembly, including FE-ASIC and ColdADC, is submerged in liquid nitrogen. The other half is above liquid nitrogen level, as shown in Figure 5.

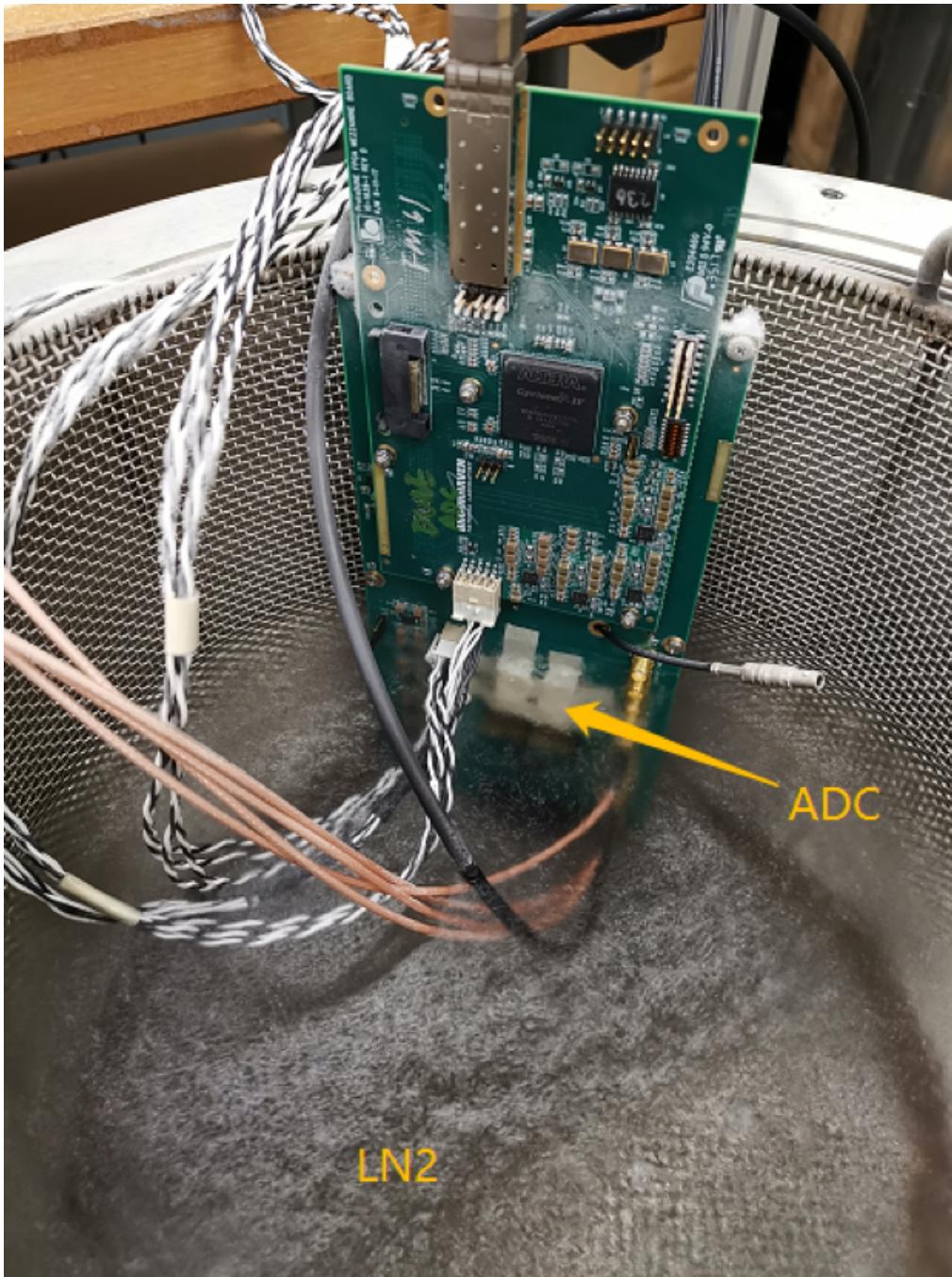


Figure 6: Cold test with ColdADC submerged in LN₂.

2.3 Fermilab Cryocooler Test System [Christian]

The Fermilab Cryocooler Test System consists of a vacuum vessel and a cryogenic refrigerator. The cryogenic refrigerator is a Cryomech PT-60. It is a closed-loop cryocooler consisting of a helium compressor (located next to the vacuum vessel) and a cold head (located on top of the vacuum vessel). The cryocooler cools a copper cold-plate inside the vacuum vessel to a minimum of 60 K. A 100 ohm platinum RTD and a 75 Watt heater are mounted on the cold-plate. A temperature controller cycles the heater on and off to achieve the set-point temperature. Any temperature between 60 and 250 K can be set. The vacuum vessel has 2 large penetrations and 12 small penetrations that can be used in device testing. Typically, one of the large penetrations is used as an inspection port and the other as a



Figure 7: Fermilab Cryocooler Test System.

feedthrough for ribbon cables. The small ports allow for a variety of other signal feedthroughs.

Two printed circuit boards are used in ASIC testing, a “cold board,” which is screwed onto the cold-plate and includes a large unmasked copper thermal contact area, and a “warm board” which is mounted as a mezzanine board on the cold-board. RTDs are placed on both the cold board and the warm board. The temperature on the warm board is typically 100 K higher than the temperature on the cold board. If the cryocooler is regulated to hold the cold-board at LN₂ temperature, then the temperature on the warm board is $\sim -96^{\circ}\text{C}$, which is warm enough for most COTS components to operate properly.

The cold board used in tests of COLDADC includes a single bare chip, wire bonded to the printed circuit board. An 80-pin header carries digital I/O and three of the four bias voltages (VDDIO and both digital voltages) between the cold board and the warm board. A 60 pin header carries the analog bias voltage and all analog signals with the exception of the analog inputs to the COLDADC. Jumpers allow the analog inputs to be grounded or connected to an external sources using cables. The only other parts on the cold board are bypass capacitors (selected for cryogenic use) and test points.

The warm board includes connectors that mate to the cold board connectors, a 52-pin header used for a cable connection to an National Instruments (NI) FPGA module, single ended to differential converters used for the 64 and 2 MHz clock signals, differential to single ended converters for the LVDS output signals, level shifters for the CMOS I/O signals, passive components, buffer amplifiers, and SMA connectors for the analog outputs, SMA connectors for the ADC test inputs, and 9-pin D connectors for cable connections to NI power supplies that provide source-measure functionality (used for chip power and for providing or measuring analog I/O signals such as reference voltages).

Test software was written using National Instruments LabView and run on a single-crate PXIe system consisting of a controller, an NI 6583 FPGA unit, and 5 power supply modules. A Keysight 33500B waveform generator was used to provide input signals. Analog measurements were made using an oscilloscope and a DVM as well as with the NI modules.

2.4 LBNL Test System [Prakash/Lin]

The ASIC testing at LBNL uses the CTS to cool the ColdADC to cryogenic temperature. A single board solution was developed by LBNL to test the ColdADC. The test board accommodates one ColdADC bare die, wire bonded to the board. The board is divided into cold and warm sections with an empty strip of PCB in between to clamp the board to CTS. The cold section of the PCB contains the ColdADC die and four low noise LDOs. Power supply distribution circuitry, Spartan 6 FPGA, 80MHz oscillator for clocking the FPGA, and the Raspberry PI are in the warm section of the test board. Analog inputs to the ColdADC are supplied by 16 edge-mount SMA connectors. There are two additional edge-mount SMA connectors to supply test inputs directly to the ADC-core. Eight-pin standard header connector is available if there is a need to bypass the ColdADC LDOs and supply external VDDs directly to the ASIC. The first version of the test board was used extensively to evaluate the ColdADC performance. However, due to the small block-RAM size of the FPGA, the ADC data cannot be streamed continuously to the Raspberry PI. Thus makes data collection a time consuming process. Another limitation is that the inputs to the ColdADC can only be single-ended due the space constraints for mounting the SMA connectors.

Recently, a version 2 of the test board was developed to improve data throughput and address some other limitations of the previous test board. The new design is a three-board solution, which consists of a motherboard, a daughter card and an FPGA mezzanine board. The daughter card can either have a bare die or a packaged chip. A modular approach was taken so the same test setup can be used for the next iteration of the ColdADC V2 chip just by minor re-designing the Chip-On-Board (COB) daughter card. The V2 LBNL test board is shown in Figure 8. This test board, similar to the previous version, has cold and warm sections. The COB daughter card and the LDOs are at the bottom, in the cold section of the board. The power distribution circuitry, FPGA mezzanine board, and the Raspberry PI are in the warm section of the board. Four 8-pin Samtec 5.00 mm 50 Ohm Ganged Micro-Miniature RF Jack connectors are used to drive external differential or single ended analog inputs to the ColdADC.

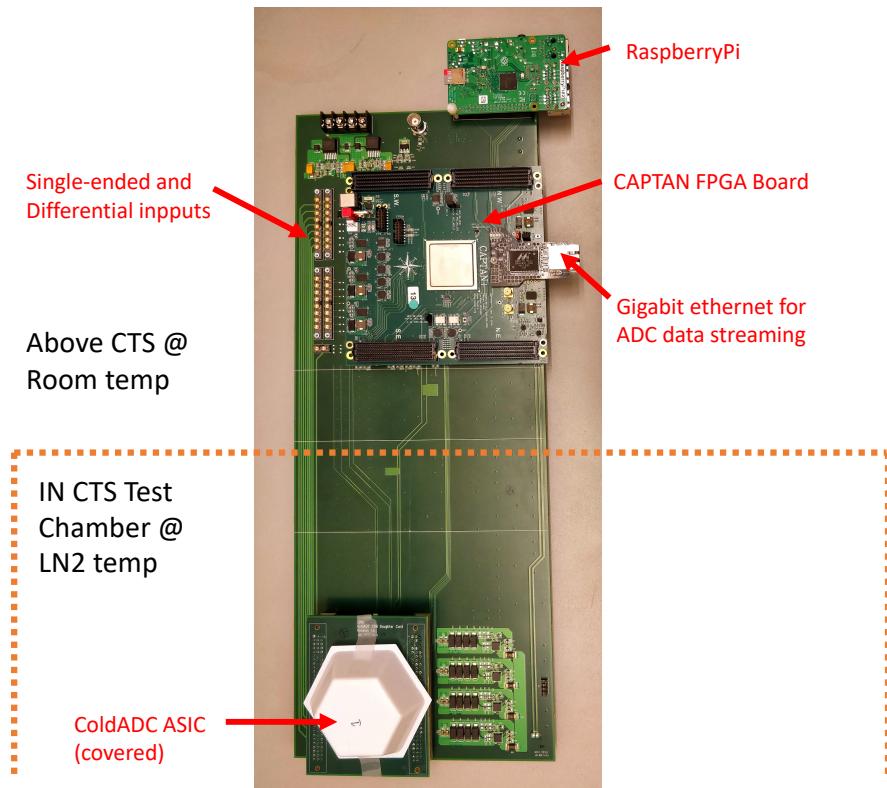


Figure 8: Version 2 LBNL ColdADC Testboard

3 Functional Testing [Christian]

ColdADC is highly programmable. Many circuit blocks can be bypassed and two versions of a number of circuit blocks are included to mitigate the risk that one might fail. Testing at Fermilab concentrated on verifying the functionality of all of the circuit blocks. Three design errors were revealed and a number of documentation errors were corrected. The table below summarizes the tests.

Test/Circuit	Result
Power on	No shorts
I2C	Works as designed (registers can be written and read)
Reset	Works as designed (registers are set to default values)
UART	Works as designed
LVDS I/O	Works as designed (output amplitude controlled as designed)
Clock Generation	16 MHz clock verified
Data Formatter	Works as designed
Band Gap Reference	Works ~as designed at room temperature, but fails when cold. Problem traced to a design error (inclusion of the wrong OP-Amp in the current source DAC); works as designed with elevated VDDA2P5 (needs 2.7V at 77K)
CMOS Reference	Works as designed
Automatic Calibration	Fails. Calibration can be done by using control registers to force the sequence of steps required and doing arithmetic off-chip. Eventually we noticed that when automatic calibration is attempted, the low order bytes of W0 and W2 for every “calibrated” stage are equal. Simulation verified that this is due to a timing error storing W0 and W2.
ADC Correction Logic	Works as designed (loaded fake comparator output values; resulting ADC output is as expected).
Pipeline ADC	Linear ramp yields close to linear output; deviation from linear at extremes of ramp; no significant deviation from linear when cold.
Input buffers	Significant non-linearity observed. Problem traced to circuit naming confusion that resulted in level shifters being omitted from input buffers. Buffers operate ~as designed with elevated VDDD1P2
Sample and Hold and MUX	Require elevated VDDD1P2 because inputs come through input buffers.

Table 2: Functional Testing.

4 Performance Results

The ColdADC is designed with many redundancies to mitigate single point of failure. During functional testing, a number of problems were identified. Fortunately, none of the problems prevented the ColdADC from achieving a performance that meets the key DUNE requirements. In this section we will show the performance results (already summarized in Table 1) with the ASIC in the nominal configuration, the same configuration that we will use for the system-level integration tests at CERN on APA#7 in the Coldbox and the ICEBERG teststand at FNAL.

4.1 Noise

4.1.1 ColdADC Only

4.1.2 LArASIC + ColdADC [Gao]

4.2 Static Linearity (DNL,INL)

To evaluate the Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) of the ColdADC, a sine wave is applied to the single-ended input of the ColdADC. The resulting ADC code density histograms are used to extract DNL and INL. Some representative distributions at LN₂ temperature are shown in Figure 9.

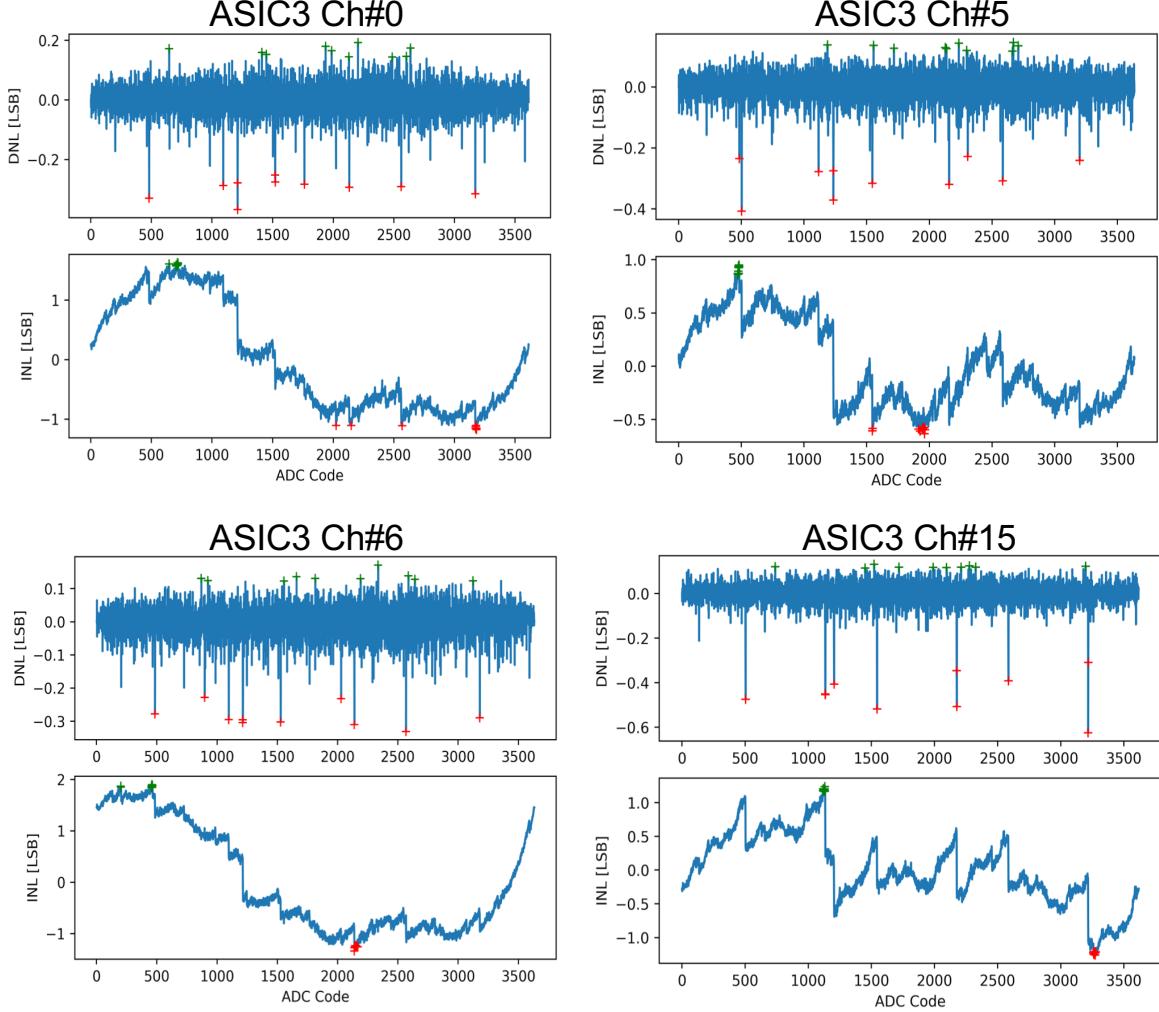


Figure 9: DNL and INL for a few representative channels on ColdADC ASIC#3 at LN₂ temperature.

The typical DNL vs. ADC code has a narrow band between ± 0.1 (12-bit) but exhibits large negative spikes. The source of the spikes are attributed to residual nonlinearity from the MUX-SHA stage (to be discussed in Section 5.4). The DNL extrema, dominated by the spikes, across all channels are typically between $+0.2$ to -0.5 LSB. The average INL extrema are from $+1.2$ to -1.1 LSB.

4.3 Dynamic Linearity (ENOB, SNDR)

The dynamic performance of an ADC is determined by the effective number of bits (ENOB). Figure 10 shows the Fast-Fourier Transform (FFT) from one of the ADC channels. The ENOB across ADC

channels at LN₂ temperature is generally fairly uniform with a mean value of 10.6 and an RMS of about 0.3 bits. Table 3 lists the measured ENOB for the 16 ADC channels from one of the ASICs tested.

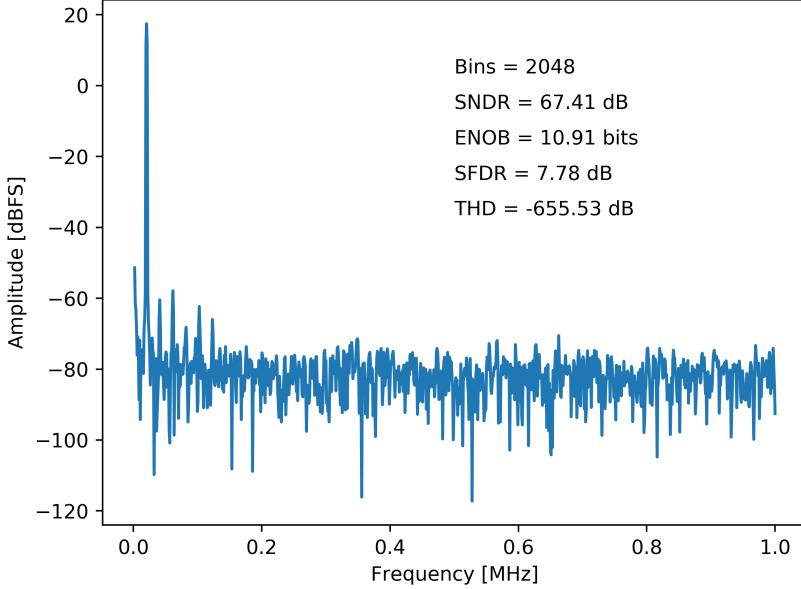


Figure 10: FFT.

Channel#	Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
ENOB	10.5	10.8	10.2	10.4	10.7	9.8	10.6	10.4
Channel#	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15
ENOB	10.2	10.5	10.6	10.5	10.7	10.3	9.8	9.7

Table 3: ColdADC ASIC# ENOB vs channel in LN₂.

4.4 Channel Crosstalk [Gao]

4.5 Power Consumption [Gao]

5 Issues Identified and Mitigations

As mentioned earlier, during functional testing of the ColdADC, a number of problems were identified. A series of studies were carried out at the three labs to understand the issues, and come up with solutions to mitigate the problems for the current ASIC, and also fixes for the next version of the design. In this section, we will go through the various issues in more details.

5.1 Auto Calibration [Grace]

The linearity of the ADC is primarily determined by the capacitor matching internal to the circuit, and to a lesser extent the performance of the internal amplifiers. To achieve the target specifications, the ADC requires calibration. The calibration in ColdADC can be carried out internally, in a fully automated way, or can be done externally. Unfortunately, while the chip can be fully calibrated externally, with calibration data loaded back onto the chip, the autocal function failed in the prototype. The ADC performance under autocal or external calibration does not differ in any way, so the main issue here is the loss of convenience that autocal promises.

When we developed the digital part of the ColdADC, we decided to partition the blocks such that the blocks that calibrate the ADC and compute the corrected digital output would be placed within the ADC cores, and the rest of the digital logic would be aggregated in a third core. This can be seen in Figure 11. The CAL_UNIT is the block that performs the calibration and also applies the calibration coefficients (or weights) to the data during normal operation. Each CAL_UNIT stores the calculated configuration weights to the register file in the CAL_CORE (which was synthesized separately).

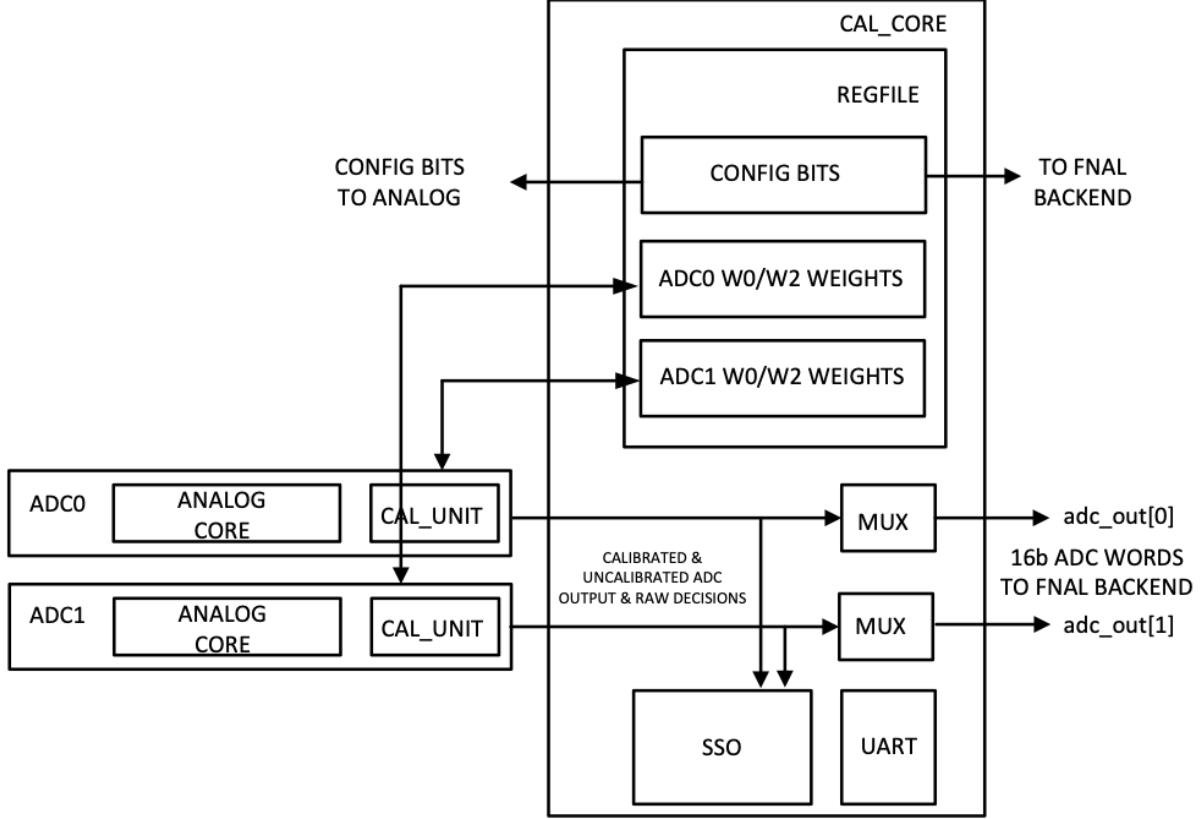


Figure 11: Partitioning of Digital Logic in the ColdADC.

This would have been an acceptable strategy but due to miscommunication the interface between the cores was not simulated with back-annotated timing. This means that the timing when a computed calibration coefficient is written back into the registers was not simulated properly. When the blocks were placed, there was a timing error between the CAL_UNIT and the CAL_CORE in the case when the CAL_UNIT was writing back computed calibration weights into storage in the CAL_CORE.

An example of the intended operation is shown in Figure 12. In this simulation the CAL_UNIT is back annotated with parasitics (but the interface with the CAL_CORE is not properly back annotated). In this simulation, the intended data is in the second row (the word 0x03FD) and is written to the w2_4 register that resides in the CAL_CORE correctly. Correct operation is assured by disabling the memory after the edge of clk.

When the interface between CAL_UNIT and CAL_CORE was properly annotated and simulated, the result was in Figure 13.

A gross error has been made, because the write signal is released too soon and therefore we have a race condition. What happens specifically here is that due to the race condition, the LSB byte of w0[4] is overwritten with the LSB byte of w2[4]. This is error and causes the entire calibration sequence to fail.

The fix here is to repartition the digital logic for the second version of the ColdADC ASIC. We will move the digital calibration and correction logic out of the ADCs and into a single, monolithic digital block as shown in Figure 14. This will ensure that the interfaces between the calculation engines and the

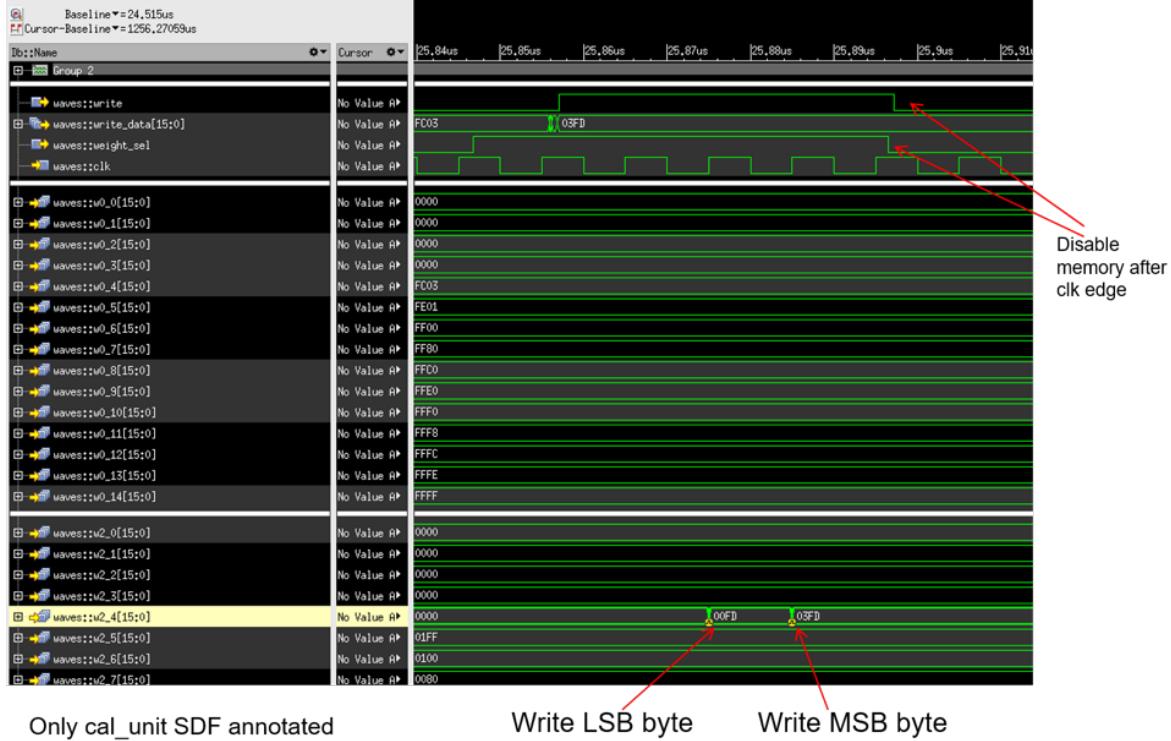


Figure 12: Correct writeback of calibration weights

memory are simulated correctly and the absence of race conditions will be verified using static timing analysis. The RTL code itself will also be made more robust by adjusting the internal state machine.

5.2 Level Shifter [Grace]

Because the digital core of the Cold ADC uses 1.2 V rails, but many of the analog circuits on the chip use 2.5 V rails, level shifters are required to translate control settings from the 1.2 V voltage domain to the 2.5 V voltage domain. Unfortunately, due to confusion during the design process, the required level shifters that were required for the front end single-ended-to-differential input buffer were not included. Therefore, in order to configure the block correctly, the 1.2 V digital supply must be elevated. While this allows the chip to be operated successfully, it is not compatible with long-term reliability.

The fix is to include the proper level shifters in the next version of Cold ADC. The fix has already been made in the layout.

5.3 ADC Core Linearity [Prakash]

The measured ADC INL of the Cold ADC is approximately 1 LSB at a 12-bit level. However, simulations suggest 0.5 LSB INL after calibration is possible. The key reasons for the discrepancy is the lack of corner models at cold and the Monte Carlo analysis done using the warm models was insufficient. Testing indicates the ADC linearity is limited primarily by insufficient op-amp gain in the stages. Since the calibration algorithm can only correct linear gain error, higher-order non-linearity beyond what was expected limited the performance. The op-amp becomes nonlinear as their swing increases because the output resistance of the devices connected to the output decreases when the voltage across them is reduced. This is a known issue and was mitigated in the design by increasing the open-loop gain. The main suspect in the reduced linearity is that the raw open-loop gain is lower than expected and therefore the closed-loop rejection of the non-linearity is not good enough. To verify the large closed-loop gain non-linearity in the stages, we adjusted the reference voltages to reduce the dynamic range of each stage and this improved the linearity, as it should if the nonlinearity steps from the output stages of the



Figure 13: Error in writeback of calibration weights

op-amps. This is demonstrated in Figure 15 and 16. In Figure 15, the differential reference is reduced 100 mV from nominal, and in Figure 16 the differential reference is reduced 200 mV from nominal. Comparing Figures 15 and 16, the DNL is improved and becomes more uniform as the reference is reduced.

To get evidence about what is the root cause of the increased linearity, we can use the programmability of the ColdADC to run various experiments to rule out potential causes. To rule out that the observed nonlinearity was caused by incomplete stage settling, we first operated the ADC with increased bias currents, to reduce settling time. This did not improve performance. We then slowed down the ADC by a factor of 16 and reduced the op-amp bias currents. Reducing the bias currents has the effect of increasing the op-loop gain, but also slows down the circuit, necessitating the reduced sampling rate. The results of this experiment is shown in Figure 17. The ColdADC demonstrates superior performance in this situation, strongly suggesting the increased open-loop gain mitigates the gain-drooping caused by the op-amp output resistance. Note that the references are nominal here, showing that the observed nonlinearity it reduced in this case by the negative feedback.

A schematic of the op-amp used in the ADC stages is shown in Figure 18. The circuit uses a standard folded-cascode topology with gain boosting amplifiers used to increase the open-loop gain. These gain boosting amplifiers work by regulating the voltage drop across the output transistors, increasing their output resistance. Simulations suggested that the gain boosting amplifiers increased the open-loop gain of the op-amp by approximately a factor of 5 (14 dB).

To narrow down what precisely in the op-amp was causing the lower-than-expected gain, we disabled the gain boosting amplifiers. This is possible to do through the configuration interface and was included for debugging purposes. When we disabled the gain boosting amplifiers, but held all other conditions constant, the linearity degraded as shown in Figure 19. In fact, the INL increased by over a factor of 2 and the DNL increased as well.

For further evidence, we modeled the ADC behaviorally using MATLAB. The simulated linearity obtained after setting the op-amp open-loop gain in the model to 80 dB is shown in Figure 20, which is a result similar to Figure 17. By reducing the open-loop gain to 74 dB, we obtained the result in Figure 21 which closely follows the linearity structure of Figure 19, this gives further evidence the issue is insufficient gain in the gain boosting amplifiers. Based on the behavioral modeling, we estimate the gain-boosting amplifiers are providing approximately 6 dB in additional gain, rather than the 14 dB

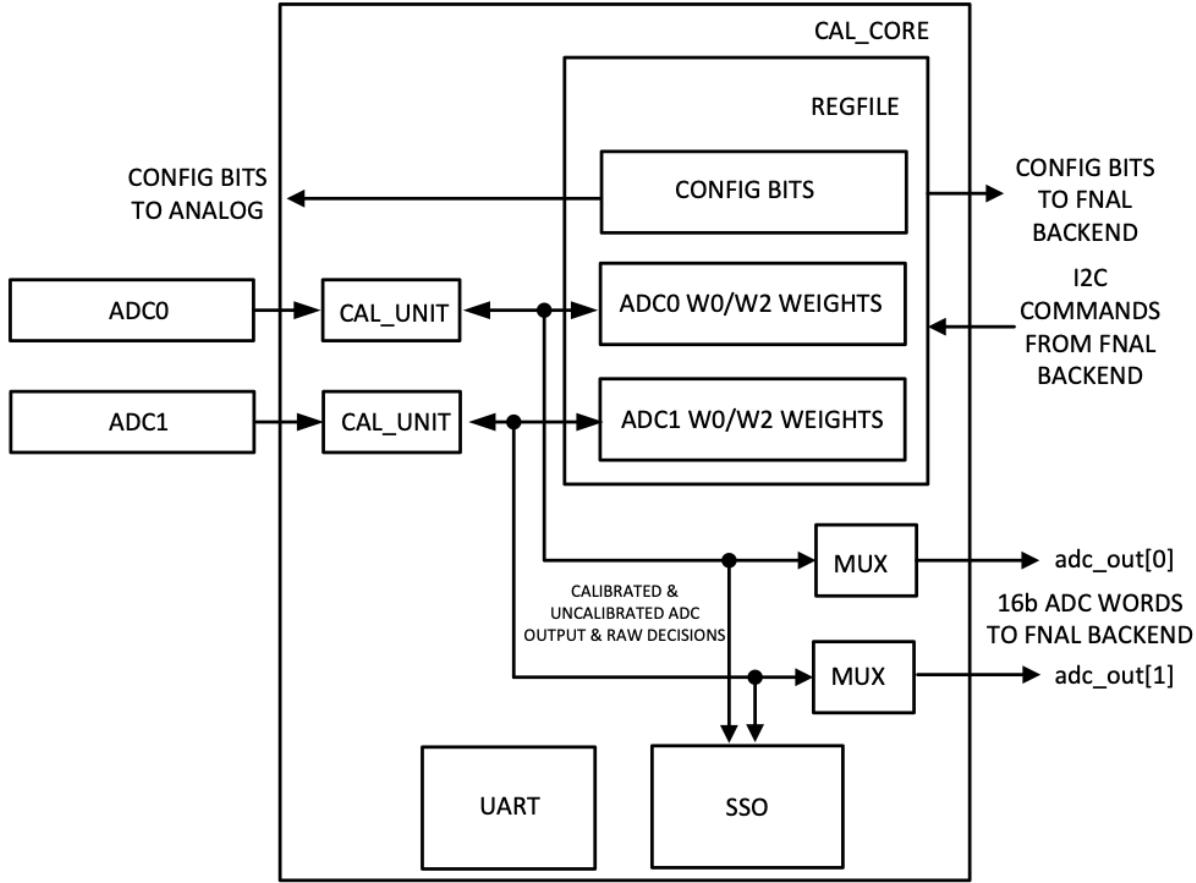


Figure 14: Proposed Calibration Digital Logic partitioning in revised prototype.

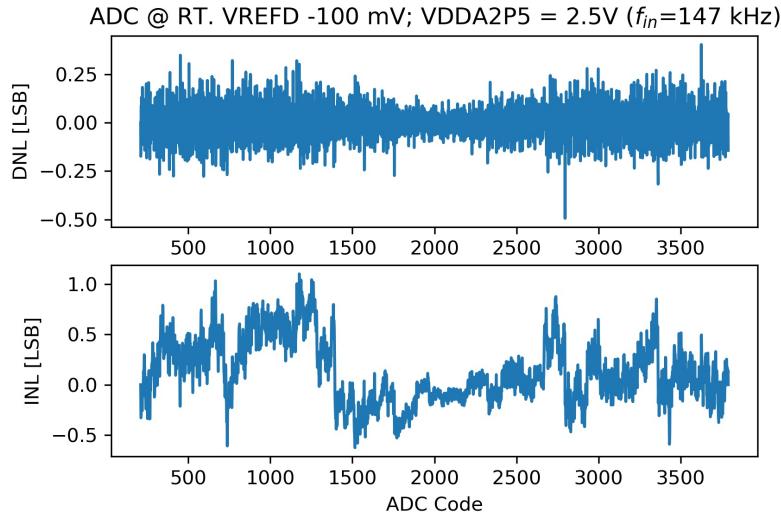


Figure 15: ADC linearity with VREFN/P +/- 100mV

that was expected.

Analysis of the circuits in the gain-boosting amplifiers indicates that they may have insufficient design margin in their biasing networks. The gain-boosting amplifiers and op-amp can be improved by

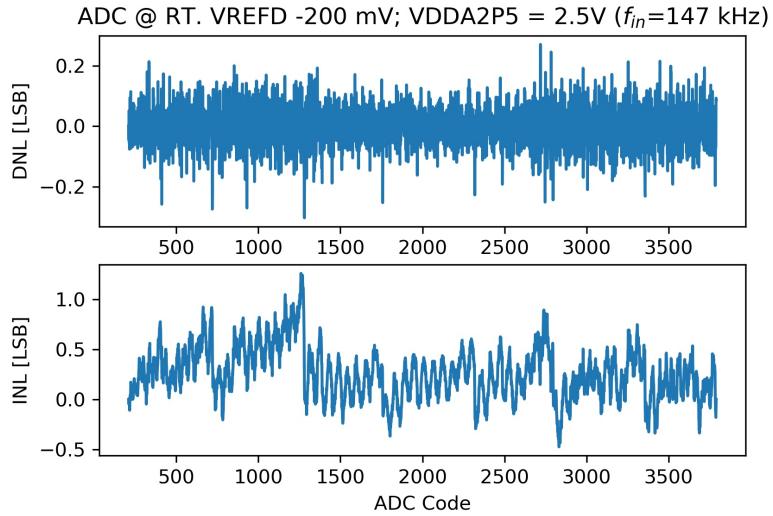


Figure 16: ADC linearity with VREFN/P +/- 200mV

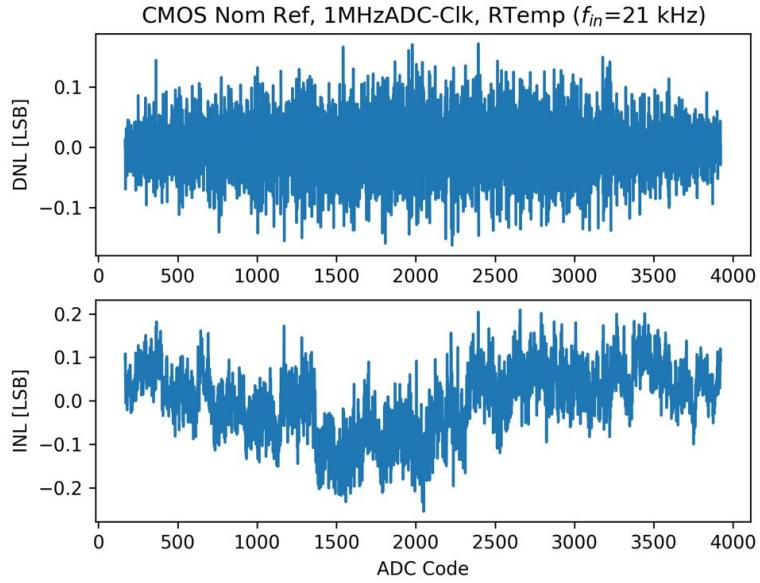


Figure 17: Linearity with Gain Boosters ON

redesigning them to better center their operating points across process and temperature.

Corner analysis of the complete op-amp before and after the gain-boosting redesign is shown in Figures 22 and 23, respectively. While the corners are only strictly valid at room temperature, the take away here is that the minimum open-loop gain across corners after the redesign is higher than the maximum open-loop gain before redesign. The design fix is being finalized and will soon be implemented in the layout.

5.4 SHA/MUX Linearity [Prakash]

The input signals are sampled at a rate of 2 MS/s, multiplexed by 8 and digitized by one of two calibrated 12-bit pipelined ADCs operating at 16 MS/s. The linearity of the ADC to a small extent depends on the linearity of the SHA/MUX circuit as well.

ColdADC can be calibrated to an amazing degree. The ability to configure and isolate the MUX's

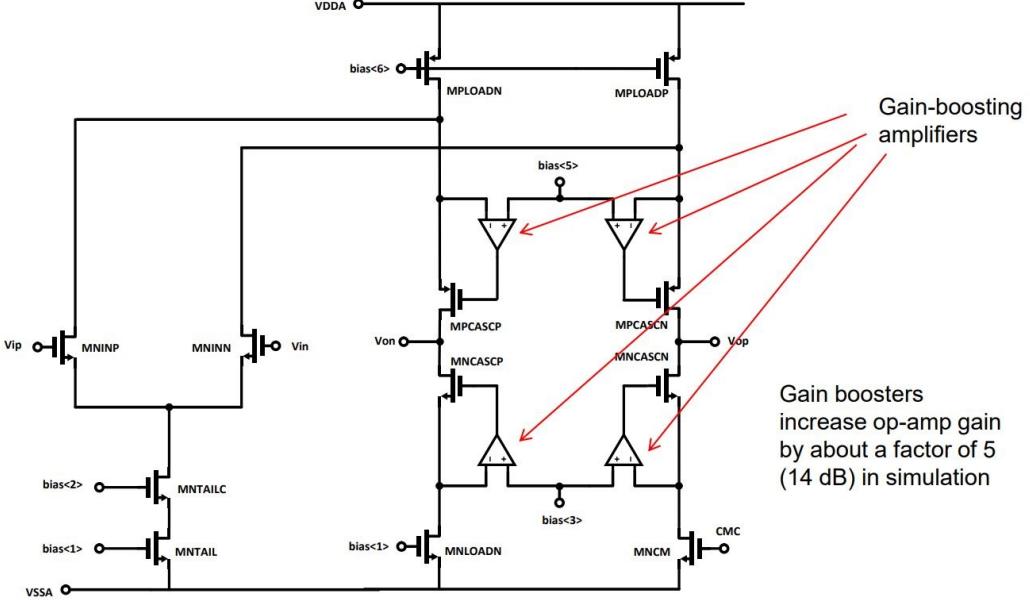


Figure 18: Op-Amp used in ColdADC stages.

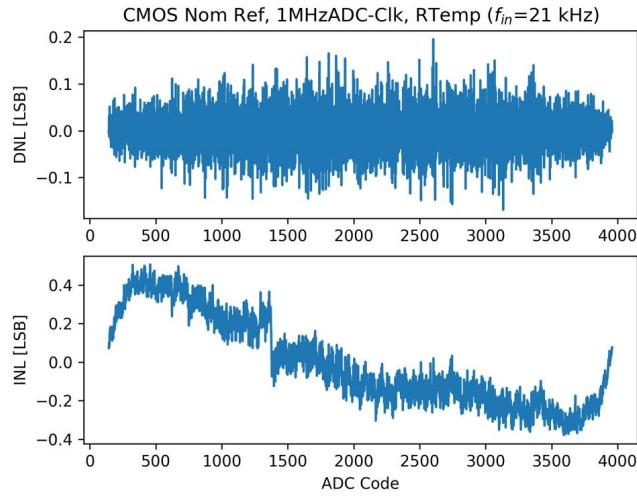


Figure 19: Linearity with Gain Boosters OFF.

turned out to be very helpful to debug the SHA/MUX linearity issue. The linearity of the ADC is approximately reduced by 0.3 LSB when SHA is in free running mode (MUX is operating).

During the Frozen SHA mode, the ADC will oversample the SHA output by a factor of 8 and the linearity of the ADC can be calculated by taking any of the samples. We observed that the overall linearity was different for different sample sets. Figure 24 shows ADC sampling with frozen SHA.

The non-linearity could be affected by SHA or MUX or a combination of both. To verify if the SHA op-amps are causing any non-linearity. Figures 25, 26 and 27 show the linearity of ADC measured by looking at the second sample of channel 7 at $40\mu\text{A}$, $50\mu\text{A}$ (default) and $60\mu\text{A}$ bias currents.

Varying the SHA bias currents did not affect the overall linearity of the ADC. To verify if the MUX's were causing the non-linearity, we reduced the sampling speed. Figures 28, 29 and 30 show the linearity at different sampling clocks.

Reducing the sampling frequency improves the linearity significantly. The MUX's seem to be causing the non-linearity and we believe the kickback is the main source of the problem. To fix this problem

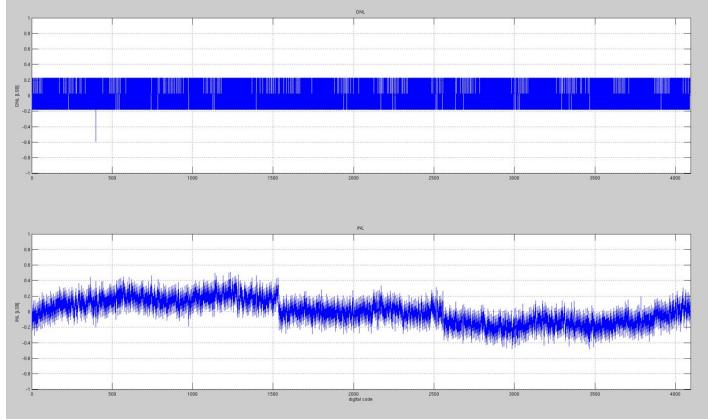


Figure 20: MATLAB model - gain boosters on \rightarrow 80 dB op-amp gain.

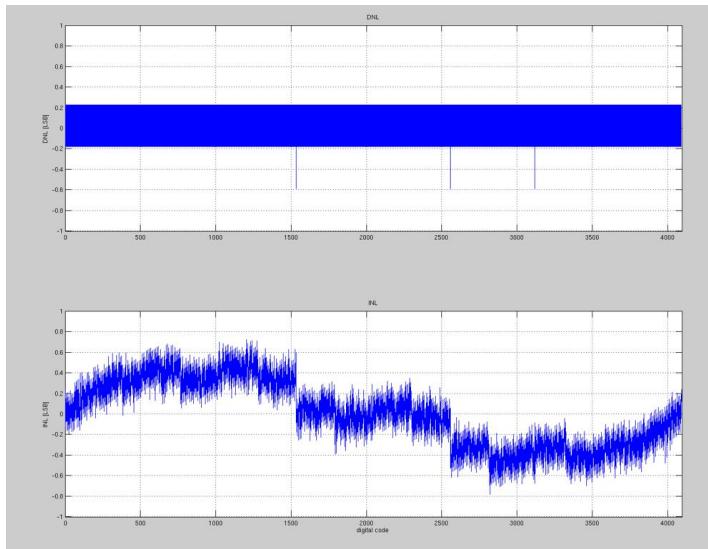


Figure 21: MATLAB model - gain boosters off \rightarrow 74 dB op-amp gain.

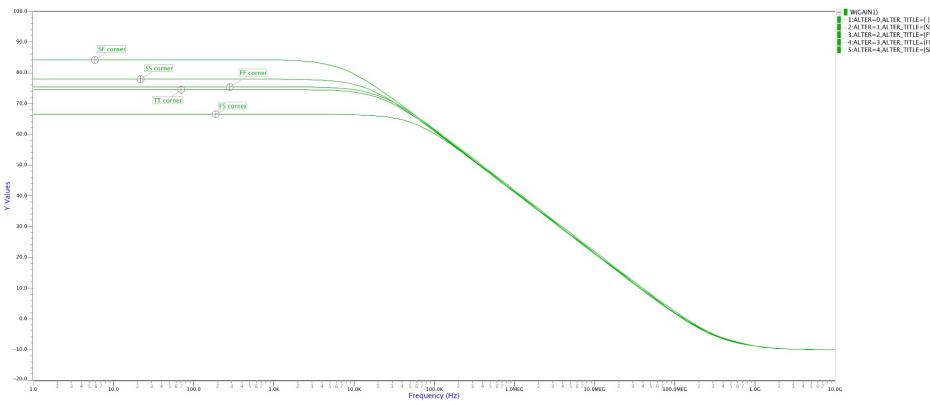


Figure 22: Corner analysis of the op-amp gain, with current gain booster circuit.

we have to redesign the MUX to be much faster.

We also observed spikes in the DNL plots while the ColdADC was configured to free running SHA mode. These spikes however reduced when the ColdADC was configured to frozen SHA mode. Figures

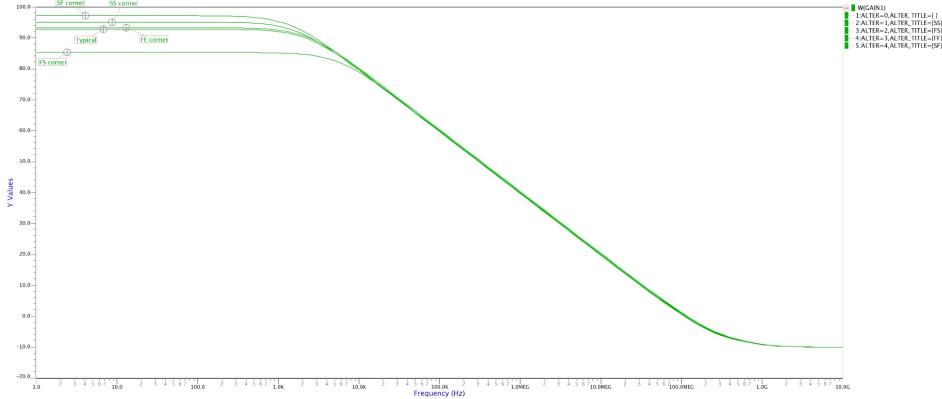


Figure 23: Corner analysis of the op-amp gain, with improved gain booster circuit.

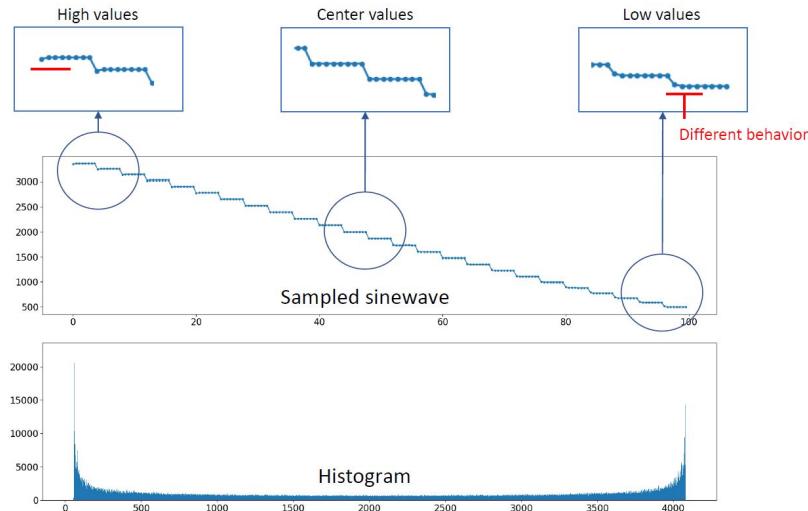


Figure 24: Histogram of ADC sampling in frozen SHA configuration

31 and 32 show the difference in linearity for free running and frozen SHA. These measurements were performed with nominal clocks and nominal reference voltages.

Another observation was that the DNL spikes were larger when the ASIC was cooled down, a possible explanation for this is the ON resistance of the switches (MUX) is significantly larger at cold than in warm. Redesigning the MUX to be faster will solve this problem aswell.

Evidence of linearity degradation only during the free running SHA mode indicate couple other possible issues: possible overlapping of the clocks for the MUX's and/or insufficient settling of MUX's. It is very difficult to simulate MUX's effects on ADC linearity. We are still in the process of understanding and proving the root cause for linearity degradation in simulations. To fix this, we will redesign the MUX's to be faster and improve the clocking scheme.

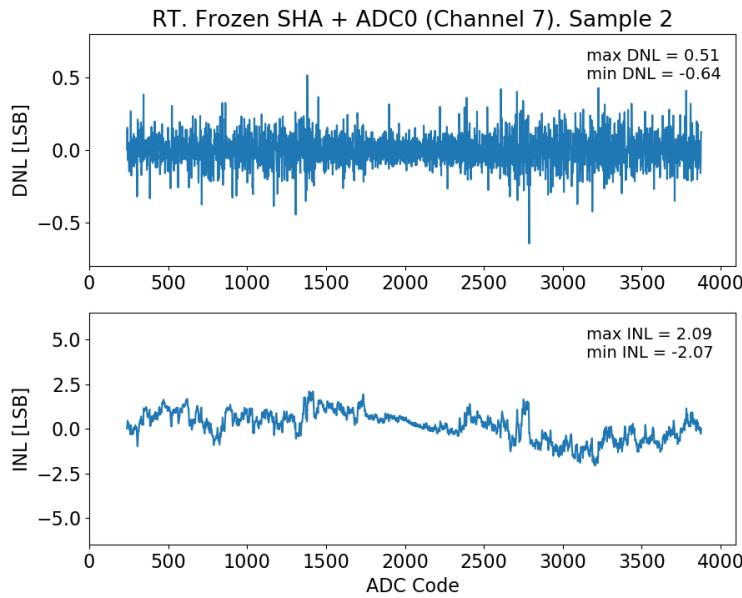


Figure 25: Linearity of ADC at room temperature with SHA bias current configured to $40\mu\text{A}$

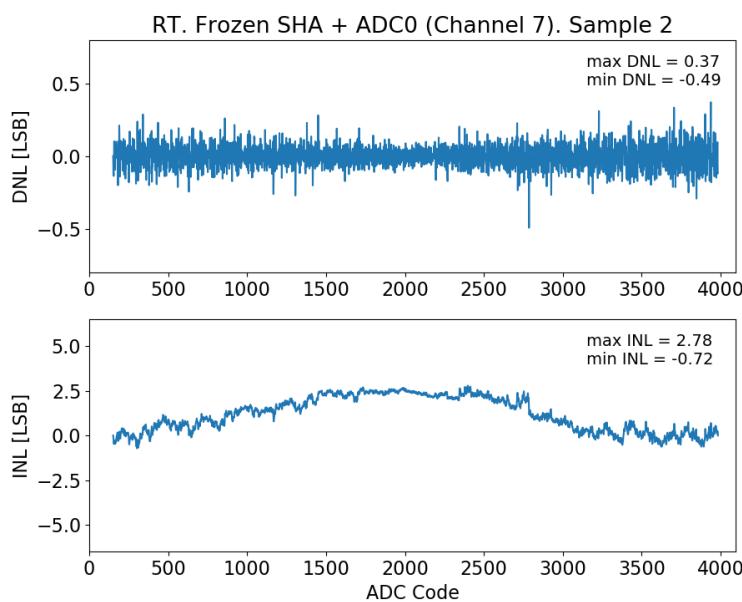


Figure 26: Linearity of ADC at room temperature with SHA bias current configured to $50\mu\text{A}$, this the nominal SHA bias current

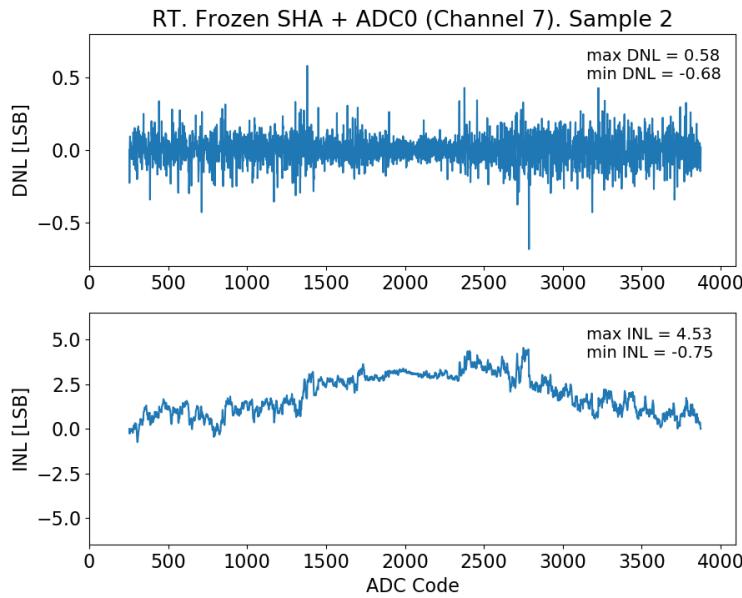


Figure 27: Linearity of ADC at room temperature with SHA bias current configured to $60\mu\text{A}$

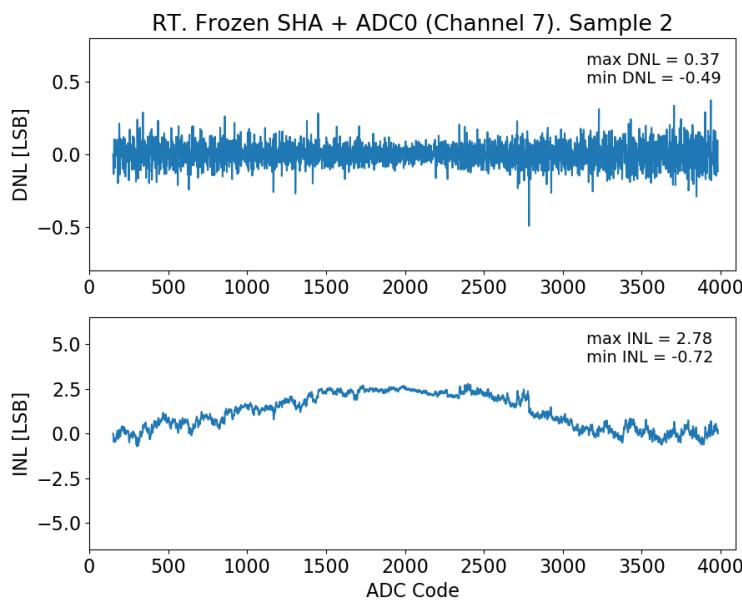


Figure 28: Linearity of ADC at room temperature with 2MHz sampling frequency (16MS/s ADC)

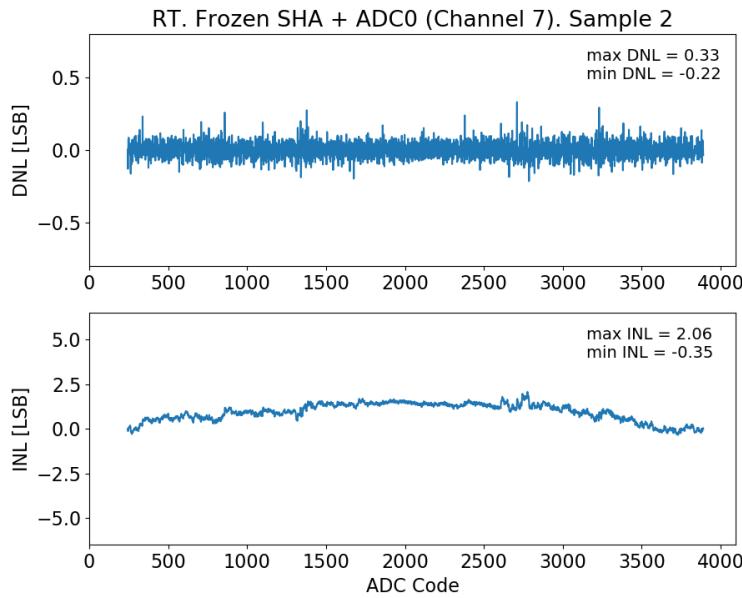


Figure 29: Linearity of ADC at room temperature with 1MHz sampling frequency (8MS/s ADC)

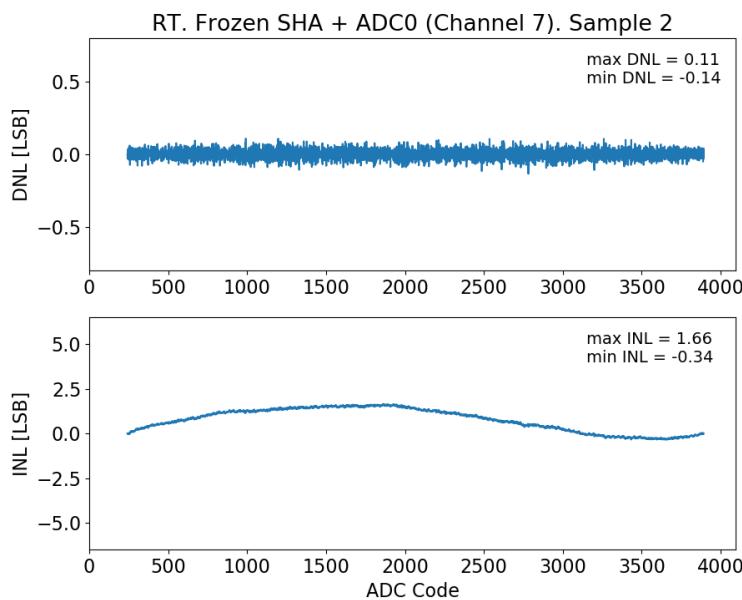


Figure 30: Linearity of ADC at room temperature with 500kHz sampling frequency (4MS/s ADC)

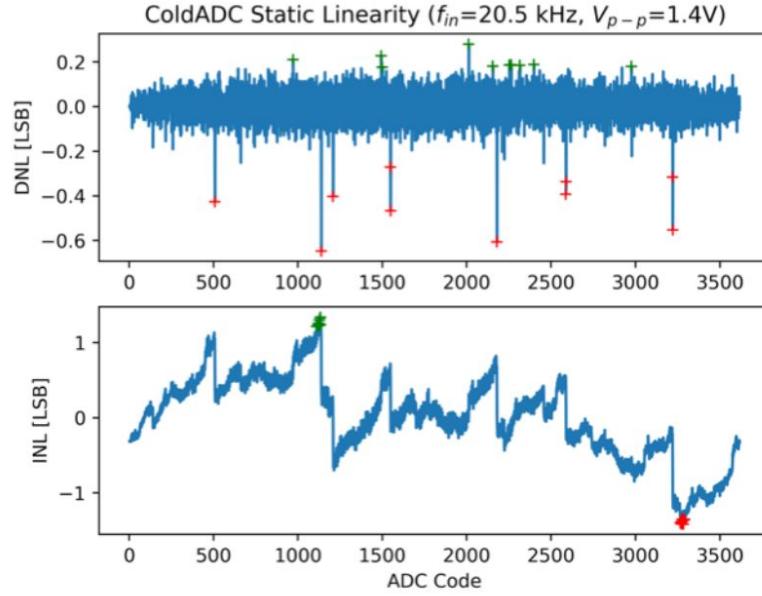


Figure 31: Linearity of the ADC with single ended input with free running SHA: These measurements were taken at LN2 temperature. During the free running SHA configuration, the MUX's introduces additional spikes in the DNL

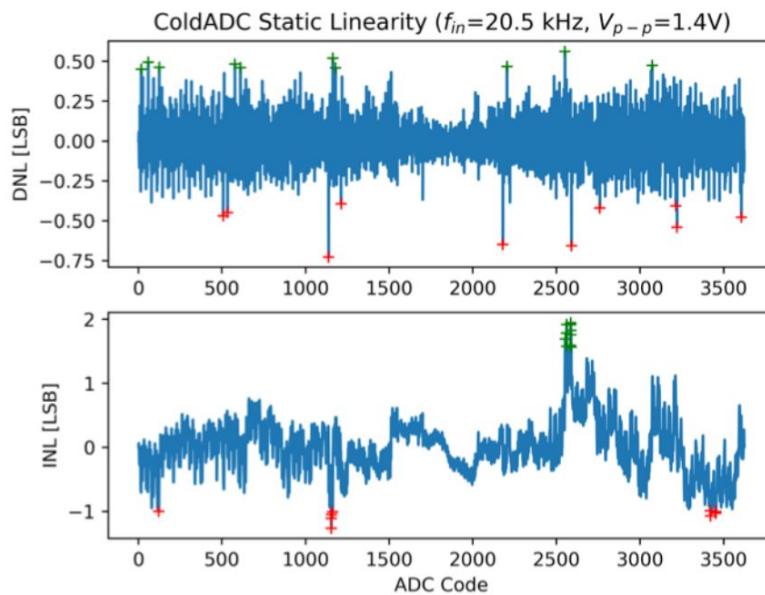


Figure 32: Linearity of the ADC with single ended input with frozen SHA: These measurements were taken at LN2 temperature

5.5 SDC Linearity [Dabrowski]

A single ColdADC input channel comprises of an Input Buffer block followed by a Sample-and-Hold (SHA) circuit, followed by a multiplexer that multiplexes outputs of 8 channels to a single fully-differential ADC core. ColdADC contains two cores, therefore, channels from 0 to 7 are multiplexed to the first core and channels from 8 to 15 to the second one.

Input Buffer contains two blocks - a Single-to-Differential Converter (SDC) and a Differential Buffer (DB). The former one accepts single-ended signals and converts them to fully-differential ones, has a low-capacitance input-impedance, and drives the capacitive switching load of the SHA. The latter one buffers differential input signals, has a static capacitive input impedance, and drives the switching load of the SHA. Each of these two blocks can be separately powered-down and bypassed.

LArASIC outputs single-ended waveforms; therefore, the performance of each ADC input channel when accepting single-ended signals is of high importance. Single-ended input signals to the ADC can be converted to fully-differential signals in either a SDC or SHA block. The performance merit of primary interest are input channel DNL and INL at room (RT) and cryogenic temperatures (Liquid Nitrogen - LN) when driven by a single-ended source, with and without the SDC block.

Figures 33 and 34 show measurements of maximum INL and maximum DNL across all ADC channels at room and cryogenic temperatures, respectively. These were derived from measurements presented in Figures 35, 36, 37 and 38. Figure 39 depicts ENOB across ADC channels with and without the SDC.

Measured results are insufficient in providing a conclusion as to whether the SDC block improves or deteriorates ADC's performance. However, measurements at LN temperature show slight improvement, on average, in DNL across channels with the SDC turned on. Measurements also indicate introduction of larger channel-to-channel variation in INL when the SDC is on. However, this might be related to bypass switches and/or other interfaces, not the SDC alone.

A standalone SDC circuit is currently being tested and a statistical analysis on a larger set of samples of standalone chips is also planned for. These results might help to answer some of the above questions/uncertainties.

Current recommendation is to remove the SDC block from the ADC input chain and implement it in the LArASIC channel.

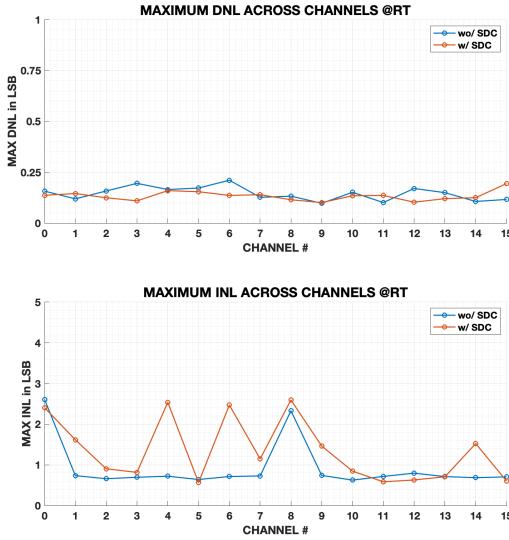


Figure 33: Maximum DNL and INL across ADC channels at room temperature.

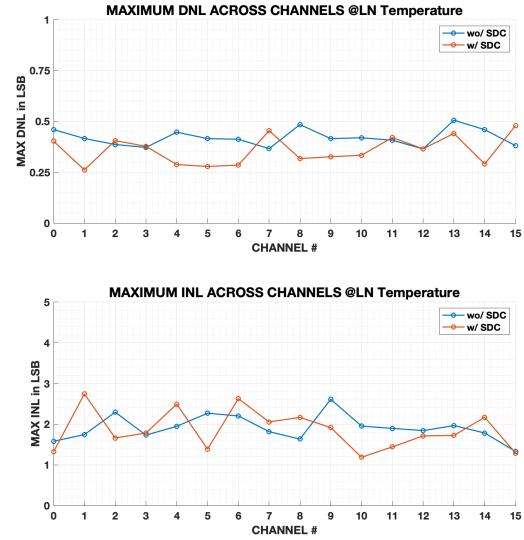


Figure 34: Maximum DNL and INL across ADC channels at liquid nitrogen temperature.

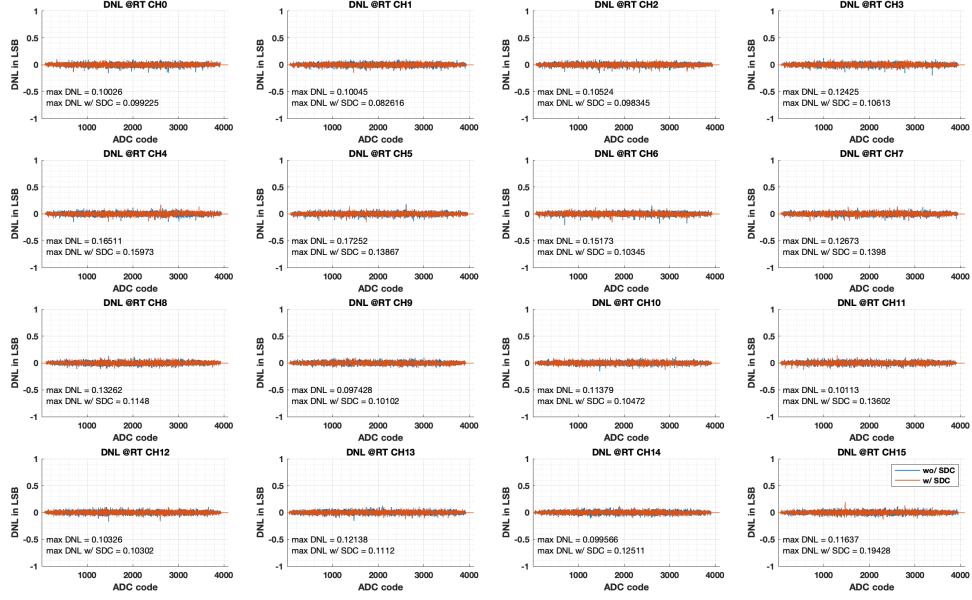


Figure 35: Measurement of DNL across all ADC channels at room temperature. Blue - SDC off, Orange - SDC on.

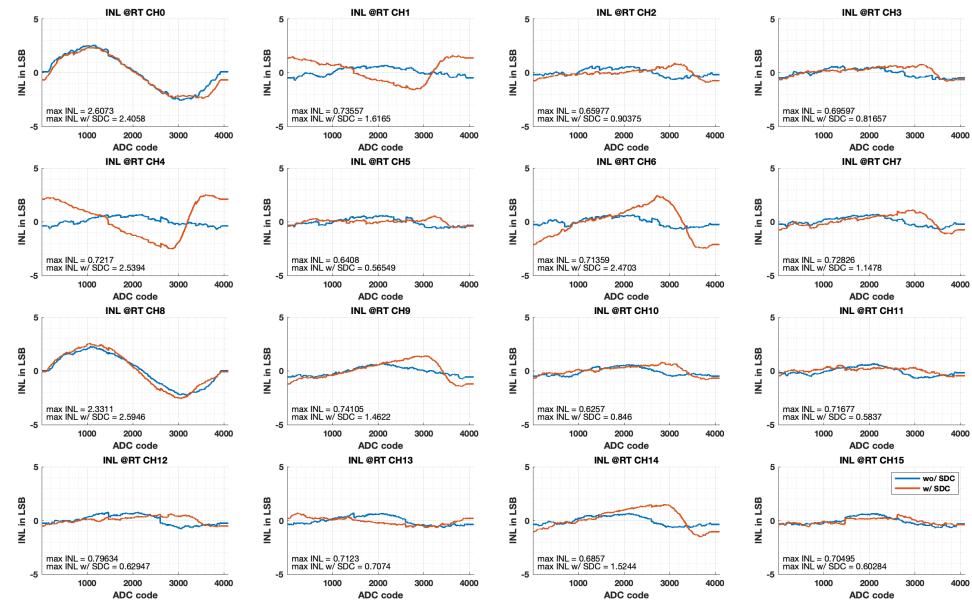


Figure 36: Measurement of INL across all ADC channels at room temperature. Blue - SDC off, Orange - SDC on.

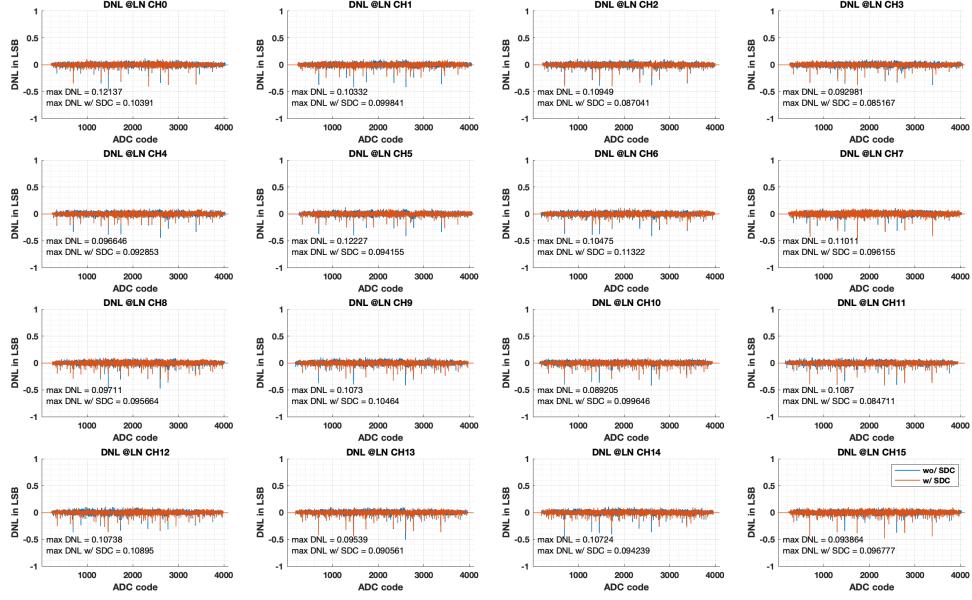


Figure 37: Measurement of DNL across all ADC channels at liquid nitrogen temperature. Blue - SDC off, Orange - SDC on.

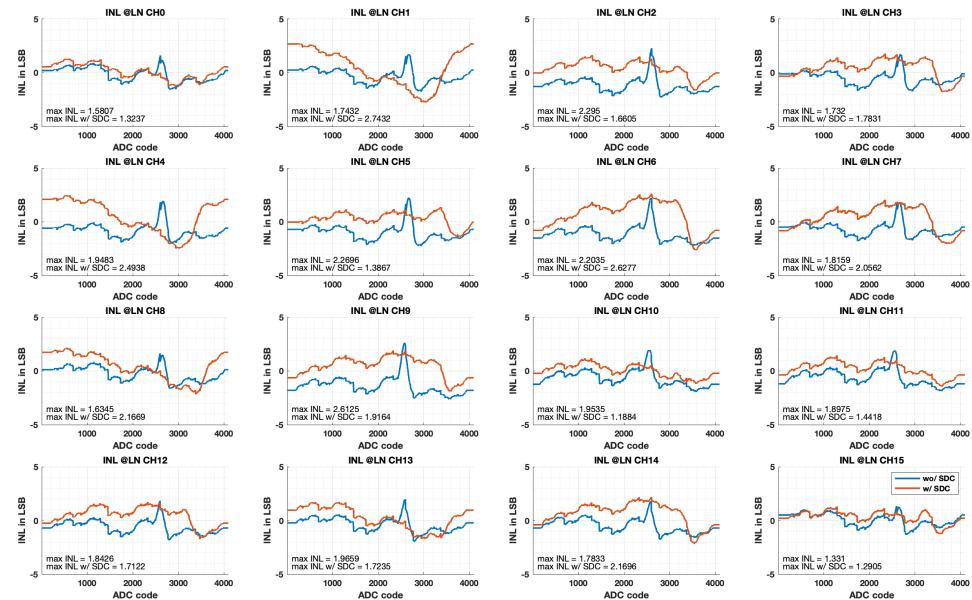


Figure 38: Measurement of INL across all ADC channels at liquid nitrogen temperature. Blue - SDC off, Orange - SDC on.

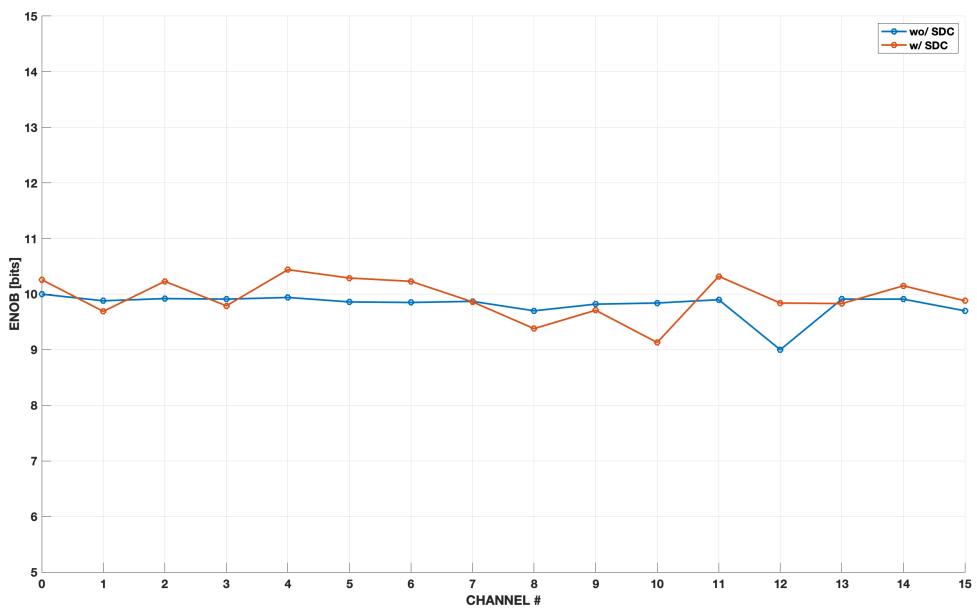


Figure 39: Measurement of ENOB across all ADC channels at room temperature.

5.6 IR Drop [Christian/Miryala]

At room temperature, when the test inputs are used to test the pipeline ADCs individually (bypassing the input buffers, Sample and Hold Amplifiers (SHAs), and the SHA multiplexer), significant non-linearity is observed for input signals near the voltage extremes of the ADC. At cryogenic temperature, no significant deviation from linearity is observed. We interpret this as evidence that there is an IR drop on the analog 2.25V power when the chip is operated at room temperature. The fact that the non-linearity is not observed at cryogenic temperature or elevated analog supply voltage (from 2.25 to 2.5V) at warm is consistent with the fact that the resistivity of the metal used to distribute the power is greatly reduced at cryogenic temperature. Metal layers M8 and M9 were used for power distribution. The redistribution layer (AP) was not used and could easily be added to the power mesh in the analog sections of ColdADC. We will make this change in the next submission.

5.7 SHA/MUX Crosstalk [Grace/Prakash/Lin]

While there is no formal specification regarding the channel crosstalk, we have measured crosstalk of approximately 1%. We have done a variety of measurements that suggest the crosstalk is due to kickback between the channels during the sampling phase that makes it so the SHAs are not completely settled between samples. When the channels are slowed down, the crosstalk is somewhat mitigated, which indicates that it is due to insufficient bandwidth in the SHA Mux. To improve this, we will lower the impedance of the Mux to allow faster settling.

5.8 BGR Op-amp [Dabrowski]

5.9 Overflow Wraparound [Grace]

The gains of each stage are weighted by the calibration. If the sum of the weights of the stages is greater than 2^{16} , then the digital correction logic can overflow, and a large input can lead to a small output code and vice versa. The stages were designed with an analog closed-loop gain slightly less than two. Based on supplied process data, we expected the closed-loop gain would be low enough to be free from overflow. In fact this was not the case and overflow was observed when the input voltage was close to one of the reference voltages. This can be seen in Figure 40, which shows the response of the two different ADCs on one of the ColdADC prototypes to the same input signal. The One the left portion of Figure 40 shows the ramp response of ADC0 and the prototype operates as expected. When the ADC is saturated, the digital output is pinned to its maximum value. On the right portion of Figure 40 overflow is observed as part of the ramp response of ADC1. In this case, the ADC input reaches its maximum value but instead of remaining pinned, the digital output jumps to a low value. This is due to higher-than-expected closed-loop gain in ADC1.

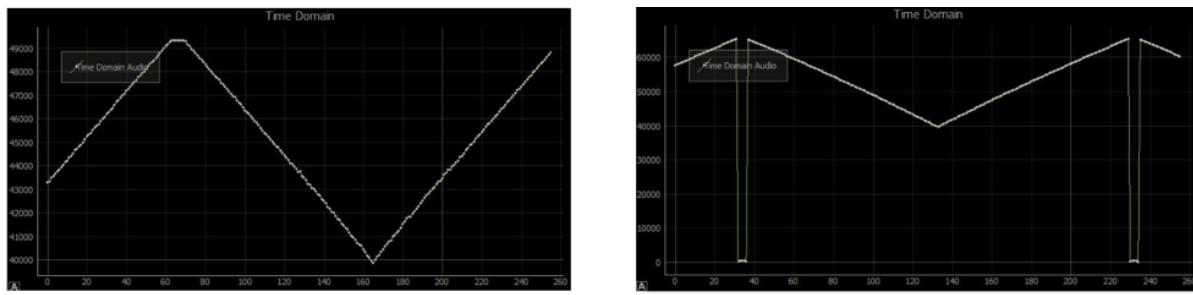


Figure 40: Digital overflow. The image on the left corresponds to ADC0 and the image on the right corresponds to ADC1.

We will fix this in two ways. First, we will further reduce the analog gain of the stages. Second, we will add to the next version of the prototype a digital overflow detection block that will sense over (or under) flow and pin the output code at a high or low level, respectively. It will do that by looking at

the sign bit of the running sum one stage prior to the last. Then the algorithm will know whether to pin to a high or low value.

6 Production Testing [Furic/Gao]

6.1 Test Setup

6.2 Results

7 Summary

References

- [1] "LBNF/DUNE Conceptual Design Report", <https://web.fnal.gov/project/LBNF/ReviewsAndAssessments/LBNF-DUNE%20CD-1-Refresh%20Directors%20Review/SitePages/Conceptual%20Design%20Report.aspx>
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- [3] "The GENIE Neutrino Monte Carlo Generator", C. Andreopoulos, et al., *Nucl. Instrum. Meth.* A614, 87 (2010).

Appendix