

# DUNE ColdADC ASIC Preliminary Testing Results

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## Abstract

The DUNE ColdADC is a 16-channel low-noise ADC ASIC designed to read out the LArASIC preamps in the DUNE Liquid Argon Far Detectors. The resolution of the ADC is 12-bits and it digitizes at a rate of 2MS/s/channel. The ADC accepts single-ended or differential inputs and outputs digitized data to COLDATA, the DUNE digital data aggregator/serializer chip.

In this document, we present the preliminary performance studies on the first version of the ColdADC ASIC. The prototype ColdADC has already achieved a performance that essentially meets the DUNE noise, linearity, and power requirements. We will also discuss some of the issues found during the functional tests and the plan to mitigate them in the next revision of the ASIC.

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# 1 Introduction

The DUNE ColdADC is a digitizer ASIC intended for operation in the Deep Underground Neutrino Experiment (DUNE) Far Detectors [1]. It will operate immersed in Liquid Argon (LAr) and will need to operate reliably, without any servicing or component replacement, for over 30 years at a temperature of 88 K.

The ColdADC was implemented in 65 nm CMOS by a team comprised of engineers from Fermilab (FNAL), Brookhaven National Laboratory (BNL), and Lawrence Berkeley National Laboratory (LBNL). The block diagram of the ColdADC is shown in Figure 1. Each ColdADC has 16 input channels that can either be single-ended or fully differential. The input signals go through a buffer block followed by a Sample-and-Hold (SHA) circuit. The buffer block contains a Single-to-Differential Converter (SDC) and a Differential Buffer (DB). The analog samples after the SHA are multiplexed by a MUX and then digitized by one of two pipelined ADCs. The digitized data is then processed by Correction Logic and Calibration Engine blocks. The data is then formatted and output via LVDS I/O. The configuration and debug interface includes an I<sup>2</sup>C port, a UART port, and a VMONITOR and IMONITOR.

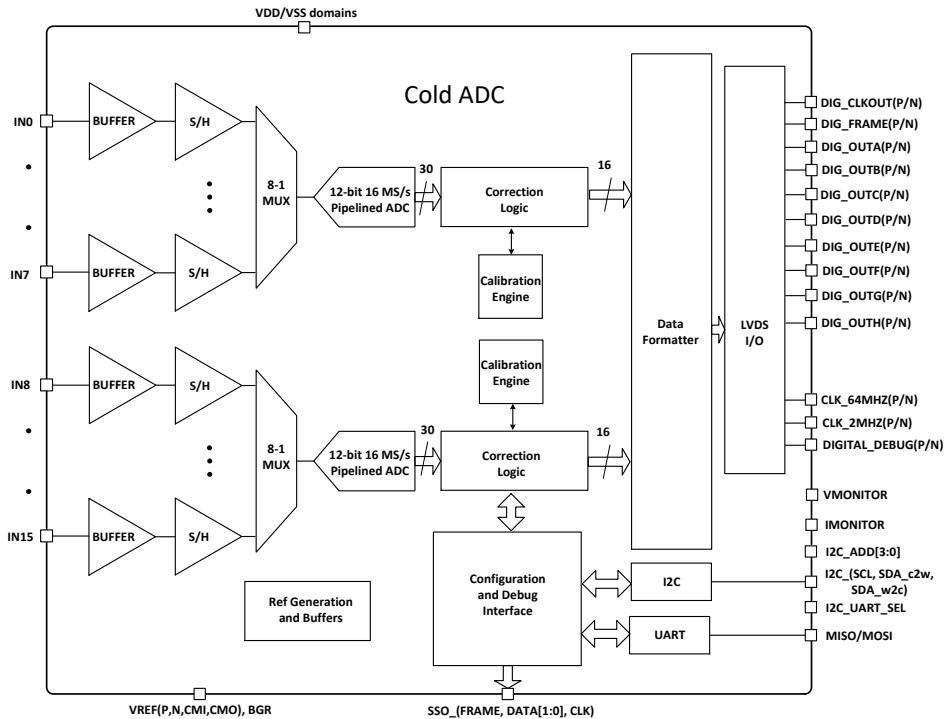


Figure 1: ColdADC block diagram.

In order to mitigate the hot carrier effect (and ensure long operational lifetime at 88 K), the circuits in the ColdADC prototype are designed with a minimum transistor channel length 50% longer than the minimum length allowed by the process, and the power supplies are kept at 10% below their nominal values. To follow this rule, the synthesized digital circuits use a custom standard cell library with longer transistors than the foundry-supplied library. In addition, the architecture of the ADC was chosen as the Pipelined ADC, whose performance depends primarily on the matching of ratioed capacitors. Studies conducted by BNL showed capacitor performance degraded less than active devices under cold conditions.

The prototype was submitted for fabrication in late 2018 and received in early 2019. Evaluation is ongoing. The first prototype meets essential requirements. The key performance specification, noise, is as expected. Recently the ColdADC has been integrated into a new revision of the DUNE Far Detector Front-End Mother Board (FEMB). Preliminary results are good, and the DUNE Far Detector FEMB is displaying better noise performance than the SBND FEMB, which uses a Commercial Off-the-Shelf (COTS) ADC. This enables the use of a lower gain setting in LArASIC and thus larger dynamic range. The key specifications of the ColdADC compared to the measured results are presented in Table 1.

Specification	Value	Result	Note
Operation Temperature	Room Temp. (RT) and 88 K	Success	
Sampling Rate	2 MHz	2 MHz	
Noise	200 $\mu$ V-rms —	189 $\mu$ V-rms (302 $\mu$ V-rms)	@ LN <sub>2</sub> temp (RT)
Differential Non-linearity (DNL)	$\pm$ 0.5 LSB (at 12-bit level)	+0.2 to -0.5 LSB	@LN <sub>2</sub> ; typical values
Integral Non-Linearity (INL)	$\pm$ 1 LSB (at 12-bit level)	+1.2 to -1.1 LSB	@LN <sub>2</sub> , typical values
Effective-Number-of-Bits (ENOB)	11.0 bits	<mean>=10.6 bits rms=0.3 bits	@ LN <sub>2</sub>
No Missing Codes Across Dynamic Range	N/A	Success	@LN <sub>2</sub> and RT
Crosstalk	No Specification	< 0.5% (< 1%)	@LN <sub>2</sub> (RT)

Table 1: Summary of ColdADC Performance.

## 2 Test Setup

The first prototype of the ColdADC ASIC has been undergoing evaluation at BNL, FNAL and LBNL since early 2019. In addition to validating the portion of the ASIC that they designed, the three labs also worked collaboratively to cross-check the key performance results and debug issues. In this section, we will describe the setup used for testing the ColdADC.

### 2.1 Cryogenic Test System (CTS)

One of the cryogenic equipments used in ColdADC testing is the Cryogenic Test System (CTS), shown in Figure 2. The CTS is a cryogenic test chamber mounted on top of a commercial LN<sub>2</sub> dewar. The device-under-test (e.g. ColdADC chip) can be mounted inside the test chamber and immersed in LN<sub>2</sub>. The CTS can also circulate either cold or warm gas to slowly cool down or warm up the ASIC before and after testing. The CTS has been effective at minimizing water condensation on the ASIC from thermal cycling. Multiple CTS units were built by a group from Michigan State University and distributed to the various testing sites.

### 2.2 BNL Test System

The block diagram of the ColdADC test board at BNL is shown in the Figure 3. There are two types of ColdADC test board at BNL. The first type can have either ColdADC die directly wire-bonded on board or packaged chip populated on the board. The purpose of this board is for ColdADC performance characterization, as shown in Figure 4. The second type has an ASIC test socket mezzanine on the test motherboard, which is aimed for the QC test, as shown in Figure 5.

The test motherboard hosts a P1/P2 LArASIC chip, a ColdADC chip (or die, or ASIC socket mezzanine), a few cold regulators and some passive components (capacitors, resistors and connectors). There are two features different from Fermilab and LBNL test boards. First, this is a test board which can characterize ColdADC performance with the FE-ASIC chip, a full chain from analog detector signal input to digital output is implemented. By using signal generator, we can also characterize standalone ADC performance, including power consumption, INL/DNL, ENOB, DC noise, etc. Second, ColdADC can be powered either by on-board regulators or directly by external power supply, which is not shown in Figure 3. On-board regulators can provide extremely low noise power sources for the test board, which is suitable for noise-sensitive measurements, such as the full chain performance characterization test. Inputs of ColdADC chip can be connected either to FE-ASIC outputs or signal generator outputs.

To minimize the design effort, a ProtoDUNE FM (FPGA mezzanine board) is adopted to configure LArASIC/ColdADC and read data out. The FM communicates with computer through Gigabit Ethernet, and UDP protocol is used. As shown in Figure 6 is the test setup for ADC performance



Figure 2: Cryogenic Test System.

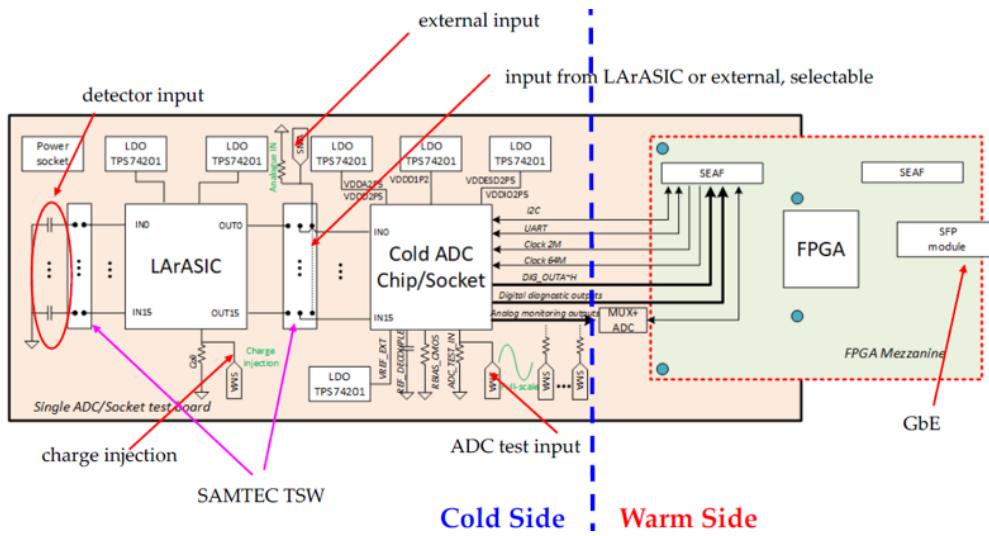


Figure 3: Block diagram of the BNL ColdADC test board

characterization. Low noise power supply Keysight E36312A is used if ColdADC is powered directly by external power supply. There are 3 different power rails for ColdADC, VDDA2P5/VDDD2P5 is set to 2.5V if CMOS reference is chosen and 2.7V if BJT reference is chosen, VDD1P2 is set to 2.1V, and VDDIO2P5 is set to 2.25V. The power consumption of ColdADC can be measured by power supply. E36312A provides a flexible way to adjust voltages for ColdADC but the noise is not as low as on-board regulators, so for precision measurements, on-board regulators should be used. Power supply

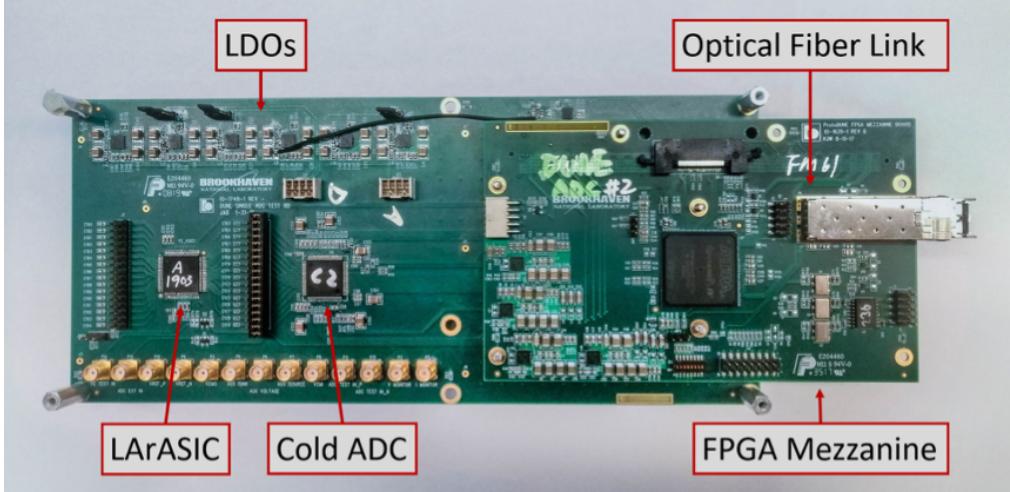


Figure 4: Test board with packaged ColdADC chip. To avoid unexpected noise from computer, a 1-port fiber to copper switch is inserted between FM and the computer.



Figure 5: Test board assembly with ColdADC socket mezzanine. The socket test motherboard can be treated as a minor revision of chip/die test motherboard. The socket test motherboard integrates MICA 150pF capacitors at the FE inputs to simulate the capacitance of 8m detector sense wire, which makes the full chain characterization close to the real experiment with the detector.

Rigol DS832 provides two power rails (5.0V and 2.8V) for both ColdADC test motherboard and FPGA mezzanine. All on-board regulators are powered by DS832. SRS DS360 is an ultra-low distortion function generator with 20-bit resolution and THD lower than -100 dBc, which is sufficient to study ADC INL/DNL and ENOB performance. In addition, we also have a Keysight 33600A generator (14-bit resolution) to provide both ramp and sine waveforms for INL/DNL study if needed (actually in the beginning 33600A was used to characterize INL/DNL with ramp waveform). In order to study ADC dynamic performance such as ENOB, FM outputs 10MHz clock to synchronize SRS360. (Later in the QC test, instead of 100MHz oscillator on board, the CG635 synthesized clock generator is applied to provide a stable 100MHz clock source which is not affected by temperature change, and CG635 outputs a 10MHz clock to synchronize SRS360). Python scripts are implemented to communicate with FPGA mezzanine via UDP protocol and analyze the data collected. A Python-based GUI interface was implemented to display real-time output. The SFP module on FM cannot work in liquid nitrogen temperature, if cold test is conducted, half of the test board assembly, including FE-ASIC and ColdADC, is submerged in liquid nitrogen. The other half is above liquid nitrogen level, as shown in Figure 7.

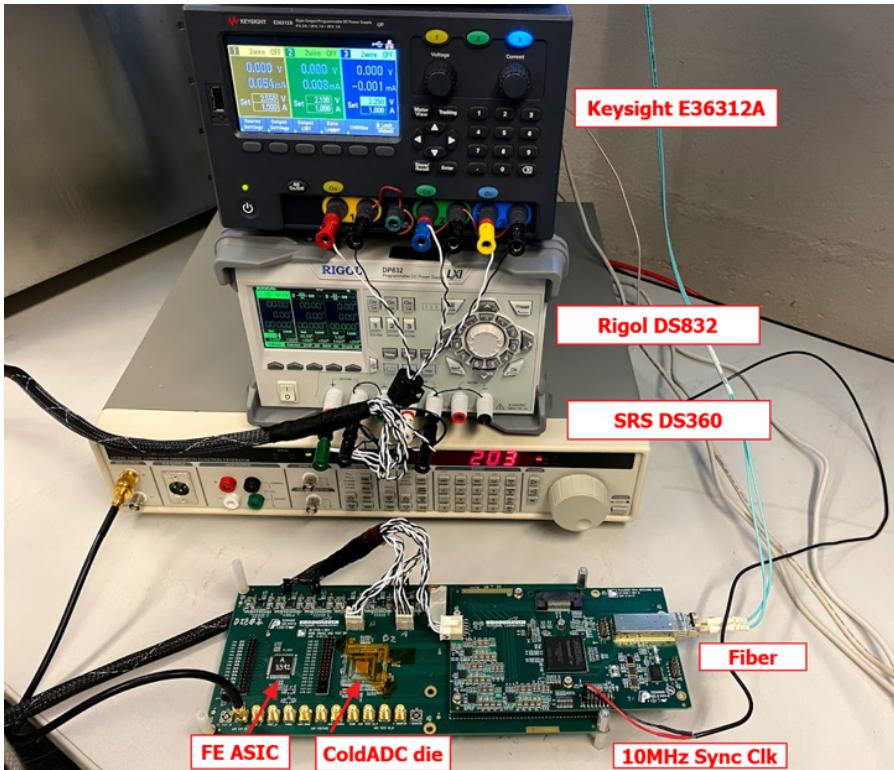


Figure 6: BNL ColdADC (die or chip) test setup.

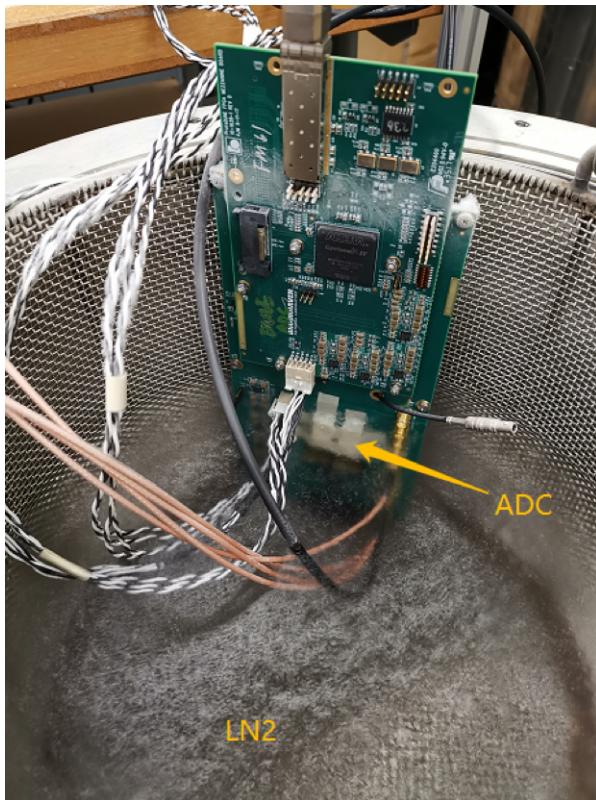


Figure 7: Cold test with ColdADC submerged in LN<sub>2</sub>.

## 2.3 Fermilab Cryocooler Test System



Figure 8: Fermilab Cryocooler Test System.

The Fermilab Cryocooler Test System, see Figure 8, consists of a vacuum vessel and a cryogenic refrigerator. The cryogenic refrigerator is a Cryomech PT-60. It is a closed-loop cryocooler consisting of a helium compressor (located next to the vacuum vessel) and a cold head (located on top of the vacuum vessel). The cryocooler cools a copper cold-plate inside the vacuum vessel to a minimum of 60 K. A 100 ohm platinum RTD and a 75 Watt heater are mounted on the cold-plate. A temperature controller cycles the heater on and off to achieve the set-point temperature. Any temperature between 60 and 250 K can be set. The vacuum vessel has 2 large penetrations and 12 small penetrations that can be used in device testing. Typically, one of the large penetrations is used as an inspection port and the other as a feedthrough for ribbon cables. The small ports allow for a variety of other signal feedthroughs.

Two printed circuit boards are used in ASIC testing, a “cold board,” which is screwed onto the cold-plate and includes a large unmasked copper thermal contact area, and a “warm board” which is mounted as a mezzanine board on the cold-board. RTDs are placed on both the cold board and the warm board. The temperature on the warm board is typically 100 K higher than than the temperature

on the cold board. If the cryocooler is regulated to hold the cold-board at LN<sub>2</sub> temperature, then the temperature on the warm board is  $\sim -96^{\circ}\text{C}$ , which is warm enough for most COTS components to operate properly.

The cold board used in tests of COLDADC includes a single bare chip, wire bonded to the printed circuit board. An 80-pin header carries digital I/O and three of the four bias voltages (VDDIO and both digital voltages) between the cold board and the warm board. A 60 pin header carries the analog bias voltage and all analog signals with the exception of the analog inputs to the COLDADC. Jumpers allow the analog inputs to be grounded or connected to an external sources using cables. The only other parts on the cold board are bypass capacitors (selected for cryogenic use) and test points.

The warm board includes connectors that mate to the cold board connectors, a 52-pin header used for a cable connection to an National Instruments (NI) FPGA module, single ended to differential converters used for the 64 and 2 MHz clock signals, differential to single ended converters for the LVDS output signals, level shifters for the CMOS I/O signals, passive components, buffer amplifiers, and SMA connectors for the analog outputs, SMA connectors for the ADC test inputs, and 9-pin D connectors for cable connections to NI power supplies that provide source-measure functionality (used for chip power and for providing or measuring analog I/O signals such as reference voltages).

Test software was written using National Instruments LabView and run on a single-crate PXIE system consisting of a controller, an NI 6583 FPGA unit, and 5 power supply modules. A Keysight 33500B waveform generator was used to provide input signals. Analog measurements were made using an oscilloscope and a DVM as well as with the NI modules.

## 2.4 LBNL Test System

The ASIC testing at LBNL uses the CTS to cool the ColdADC to cryogenic temperature. A single board solution was developed by LBNL to test the ColdADC. The test board accommodates one ColdADC bare die, wire bonded to the board. The board is divided into cold and warm sections with an empty strip of PCB in between to clamp the board to CTS. The cold section of the PCB contains the ColdADC die and four low noise LDOs. Power supply distribution circuitry, Spartan 6 FPGA, 80MHz oscillator for clocking the FPGA, and the Raspberry PI are in the warm section of the test board. Analog inputs to the ColdADC are supplied by 16 edge-mount SMA connectors. There are two additional edge-mount SMA connectors to supply test inputs directly to the ADC-core. Eight-pin standard header connector is available if there is a need to bypass the ColdADC LDOs and supply external VDDs directly to the ASIC. The first version of the test board was used extensively to evaluate the ColdADC performance. However, due to the small block-RAM size of the FPGA, the ADC data cannot be streamed continuously to the Raspberry PI. Thus makes data collection a time consuming process. Another limitation is that the inputs to the ColdADC can only be single-ended due the space constraints for mounting the SMA connectors.

Recently, a version 2 of the test board was developed to improve data throughput and address some other limitations of the previous test board. The new design is a three-board solution, which consists of a motherboard, a daughter card and an FPGA mezzanine board. The daughter card can either have a bare die or a packaged chip. A modular approach was taken so the same test setup can be used for the next iteration of the ColdADC V2 chip just by minor re-designing the Chip-On-Board (COB) daughter card. The V2 LBNL test board is shown in Figure 9. This test board, similar to the previous version, has cold and warm sections. The COB daughter card and the LDOs are at the bottom, in the cold section of the board. The power distribution circuitry, FPGA mezzanine board, and the Raspberry PI are in the warm section of the board. Four 8-pin Samtec 5.00 mm 50 Ohm Ganged Micro-Miniature RF Jack connectors are used to drive external differential or single ended analog inputs to the ColdADC. This test board will be used extensively to test the response of the ColdADC to differential inputs, which is the output format for the next version of LArASIC.

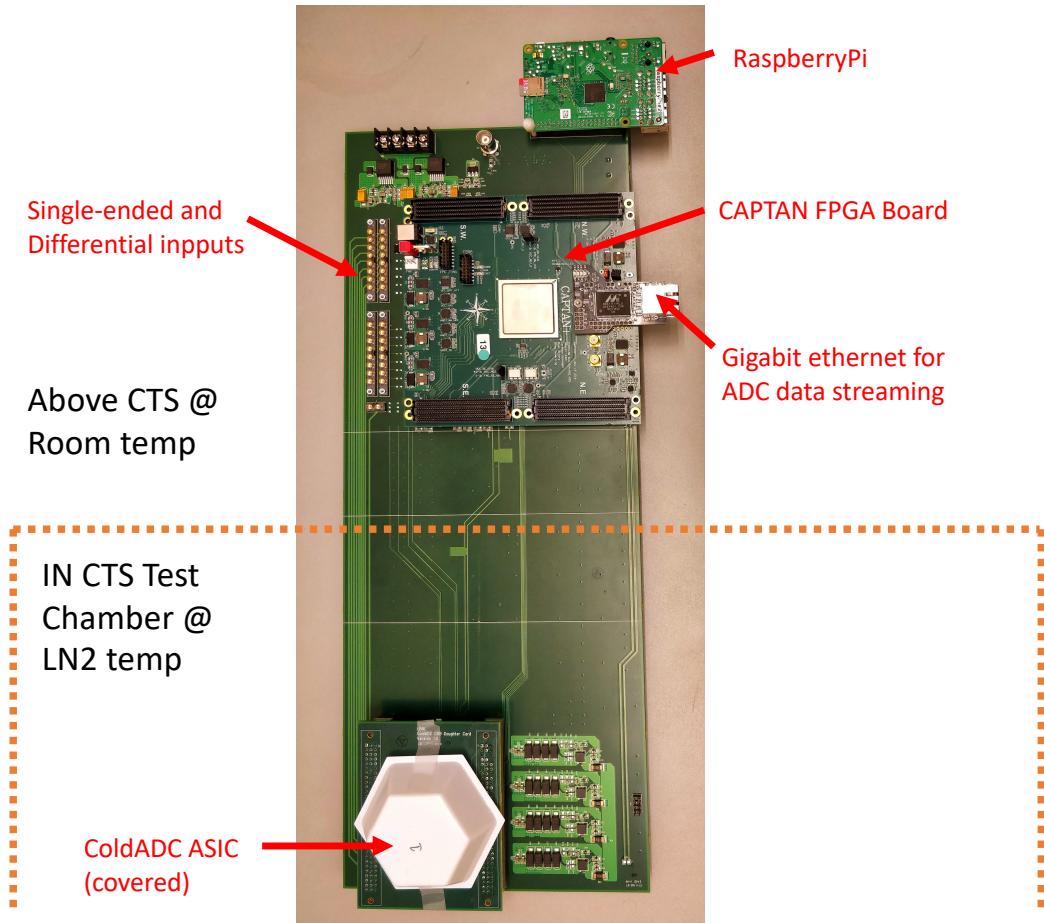


Figure 9: Version 2 LBNL ColdADC Testboard. The board has a cold and warm section. The cold part of the board is inside the CTS test chamber. The warm part of the board where the FPGA and Raspberry Pi board are mounted is outside of the CTS at room temperature.

### 3 Functional Testing

ColdADC is highly programmable. Many circuit blocks can be bypassed and two versions of a number of circuit blocks are included to mitigate the risk that one might fail. Testing at Fermilab concentrated on verifying the functionality of all of the circuit blocks. Three design errors were revealed and a number of documentation errors were corrected. The table below summarizes the tests.

Test/Circuit	Result
Power on	No shorts
I2C	Works as designed (registers can be written and read)
Reset	Works as designed (registers are set to default values)
UART	Works as designed
LVDS I/O	Works as designed (output amplitude controlled as designed)
Clock Generation	16 MHz clock verified
Data Formatter	Works as designed
Band Gap Reference	Works ~as designed at room temperature, but fails when cold. Problem traced to a design error (inclusion of the wrong OP-Amp in the current source DAC); works as designed with elevated VDDA2P5 (needs 2.7V at 77K)
CMOS Reference	Works as designed
Automatic Calibration	Fails. Calibration can be done by using control registers to force the sequence of steps required and doing arithmetic off-chip.  Eventually we noticed that when automatic calibration is attempted, the low order bytes of W0 and W2 for every “calibrated” stage are equal. Simulation verified that this is due to a timing error storing W0 and W2.
ADC Correction Logic	Works as designed (loaded fake comparator output values; resulting ADC output is as expected).
Pipeline ADC	Linear ramp yields close to linear output; deviation from linear at extremes of ramp; no significant deviation from linear when cold.
Input buffers (SDC,DB)	Significant non-linearity observed. Problem traced to circuit naming confusion that resulted in level shifters being omitted from input buffers. Buffers operate ~as designed with elevated VDDD1P2
Sample and Hold and MUX	Require elevated VDDD1P2 because inputs come through input buffers.

Table 2: Functional Testing.

## 4 Performance Results

The ColdADC is designed with many redundancies to mitigate single point of failure. During functional testing, a number of problems were identified. Fortunately, none of the problems prevented the ColdADC from achieving a performance that meets the key DUNE requirements. In this section we will show the performance results (already summarized in Table 1) with the ASIC in the nominal configuration, the same configuration that we will use for the system-level integration tests at CERN on APA#7 in the Coldbox and the ICEBERG teststand at FNAL.

### 4.1 Noise

The key performance metric for the ColdADC is its noise performance, as it directly impacts the sensitivity of the experiment. The design goal for the ColdADC was for its internal noise to be well below the noise of the LArASIC, so the LArASIC would dominate the overall noise of the system. This has been achieved as the ADC met its goal of 200  $\mu\text{V}$ -rms noise at LN<sub>2</sub> temperature. Detailed measurements of the ASIC and system noise in different conditions follow.

#### 4.1.1 ColdADC Only

The noise distribution for 16-channels from one ColdADC chip with the input floating are shown in Figure 10 (RT) and Figure 11 (LN<sub>2</sub>). The results are given in full 16-bit ADC output. The average noise is 6.7 LSB (302  $\mu\text{V}$ -rms) at warm and 4.2 LSB (189  $\mu\text{V}$ -rms) in LN<sub>2</sub>, in 16-bit. The measurement is done with ColdADC configured after calibration, VDDA2P5/VDDD2P5=2.5 V, VDDD1P2=2.0 V, VDDIO=2.25 V, SDC bypassed. Separate study has shown that SDC noise is negligible.

#### 4.1.2 LArASIC + ColdADC

To evaluate the combined noise of LArASIC and ColdADC, 150pF mica capacitor is added to the LArASIC input to simulate the capacitance of the detector sense wire. Noise characterization is made at both room and LN<sub>2</sub> temperatures, as shown in Figure 12. The quantization noise of 12-bit ADC is negligible when LArASIC gain is set to 7.8 mV/fC or higher. With a shaping time > 2  $\mu\text{s}$ , the ENC noise is below 630 e<sup>-</sup> at RT and < 500 e<sup>-</sup> at LN<sub>2</sub> temperature.

The noise dependence on the input capacitance is also studied. In this setup, each input LArASIC channel has a different capacitor with value that ranges from 22 pF to 150 pF. The input capacitance dependence result in LN<sub>2</sub> is shown in Figure 13 . The four different curves correspond to different values of LArASIC shaping time. The noise performance comparison between ColdADC BGR and CMOS reference, and comparison between SDC and bypassing SDC show no significant difference. The ENC noise performance for the LArASIC + ColdADC setup has better noise performance compared to MicroBooNE, ProtoDUNE, and SBND cold electronics (see results in the Appendix).

The DUNE requirement calls for a 12-bit ADC. The nominal plan is to truncate 16-bit ColdADC output down to 12-bit. Given the low noise of the ColdADC, we explore the feasibility of outputting more than 12-bit. Earlier Figure 12 demonstrates that when LArASIC gain is set to 7.8 mV/fC or higher, the quantization noise of 12-bit ADC is negligible. Figure 14 shows the ENC as a function of shaping time for 16, 14, and 12 bit ADC output with input LArASIC capacitance of 150 pF. Figure 15 shows the ENC with LArASIC input floating. With the current noise performance, the quantization noise is negligible at 14-bit output even with the lowest LArASIC gain setting of 4.7 mV/fC.

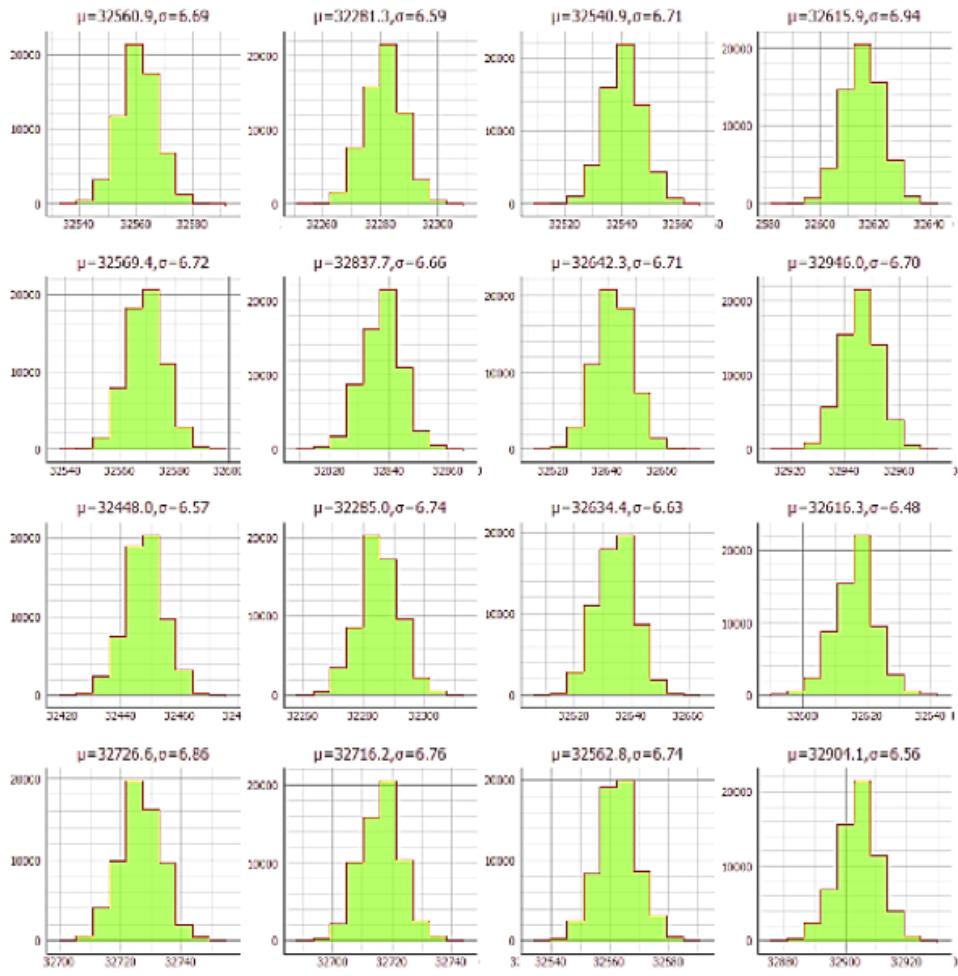


Figure 10: Noise distribution (16-bit) of 16 input channels at room temperature.

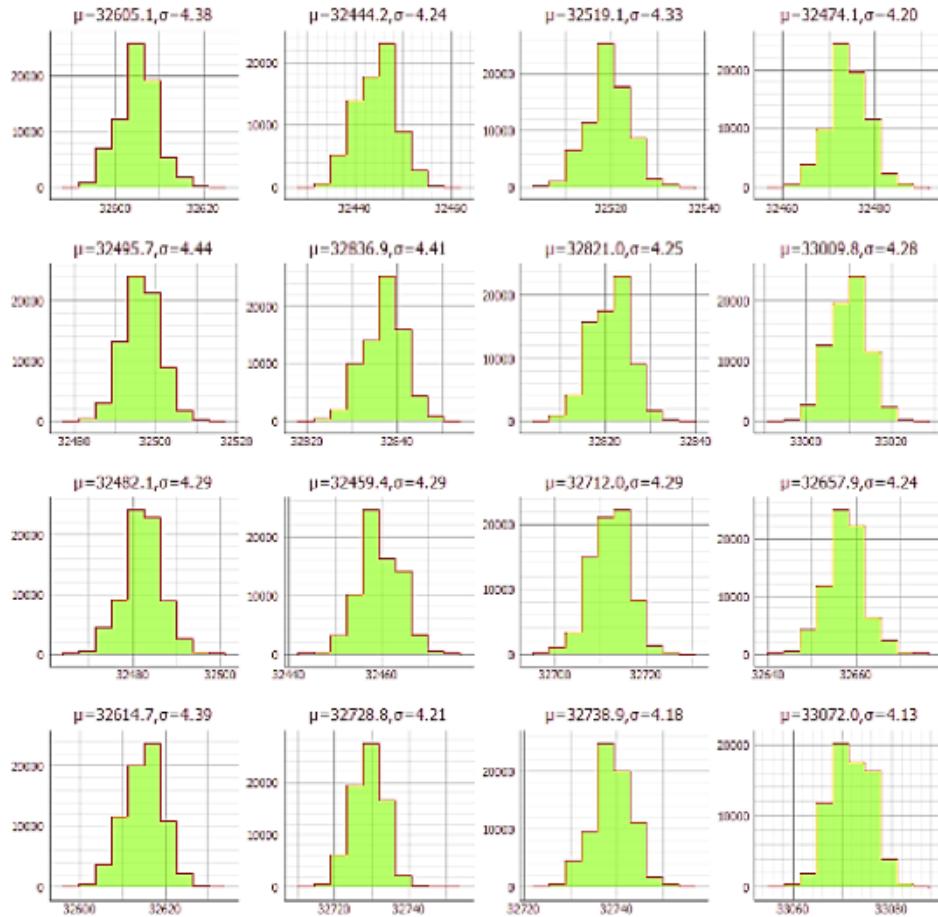


Figure 11: Noise distribution (16-bit) of 16 input channels at  $\text{LN}_2$  temperature.

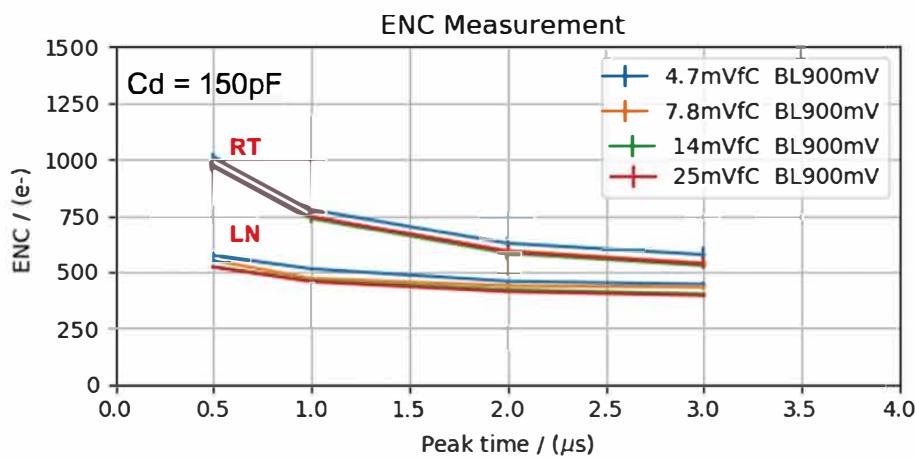


Figure 12: LArASIC + ColdADC (12-bit mode) noise as a function of shaping time at RT and  $\text{LN}_2$  temperatures.

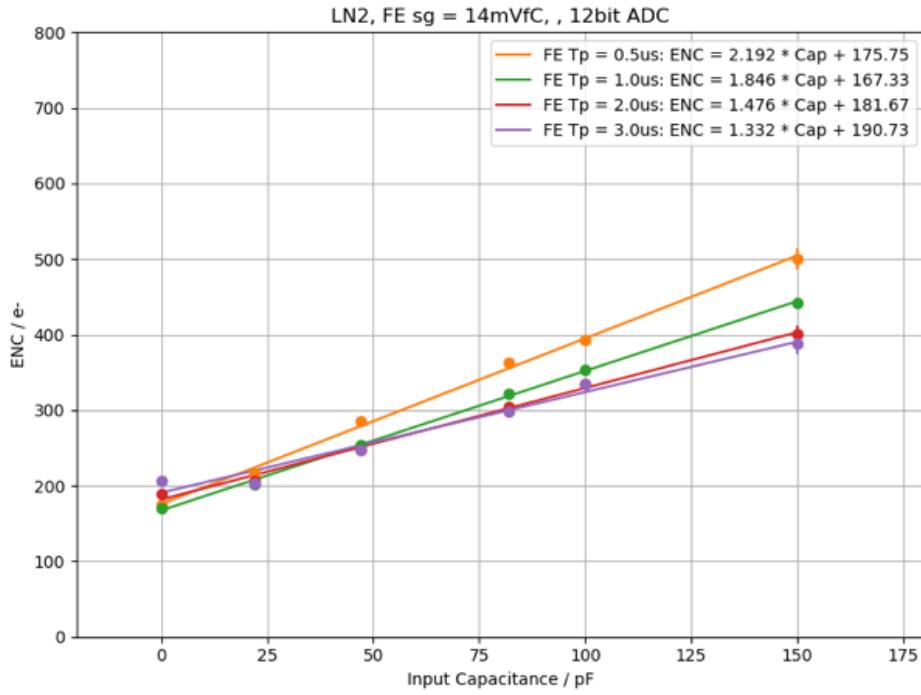


Figure 13: ENC vs. input capacitance at LN<sub>2</sub> temperature. LArASIC is configured with a gain setting of 14 mV/fC, ColdADC output is truncated to 12-bit. The four curves correspond to (from top to bottom) 0.5, 1.0, 2.0, and 3.0  $\mu$ s shaping time.

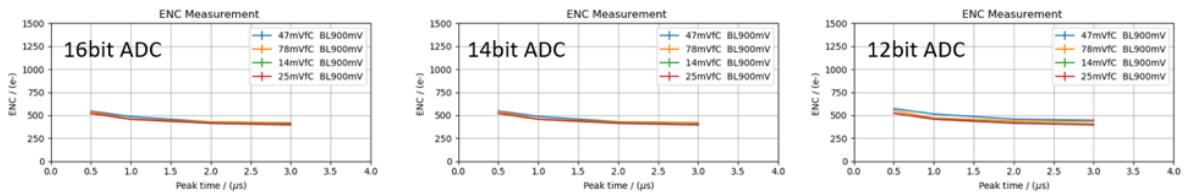


Figure 14: ENC vs. Shaping Time at LN<sub>2</sub> temperature. Input capacitance is 150 pF. Different curves correspond to gain setting of (top to bottom) 4.7, 7.8, 14, 25 mV/fC.

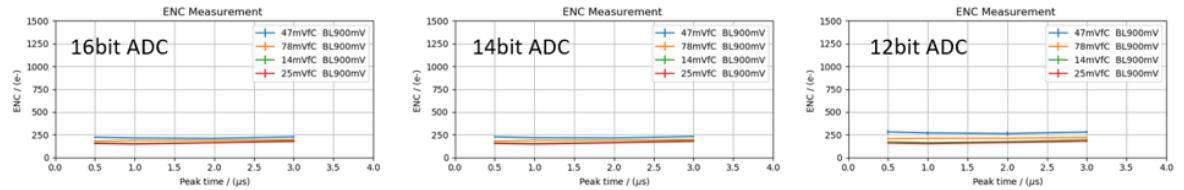


Figure 15: ENC vs. Shaping Time at LN<sub>2</sub> temperature. Input floating. Different curves correspond to gain settings of (top to bottom) 4.7, 7.8, 14, 25 mV/fC.

## 4.2 Static Linearity (DNL,INL)

To evaluate the Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) of the ColdADC, a sine wave is applied to the single-ended input of the ColdADC. The resulting ADC code density histograms are used to extract DNL and INL. Some representative distributions at LN<sub>2</sub> temperature are shown in Figure 16.

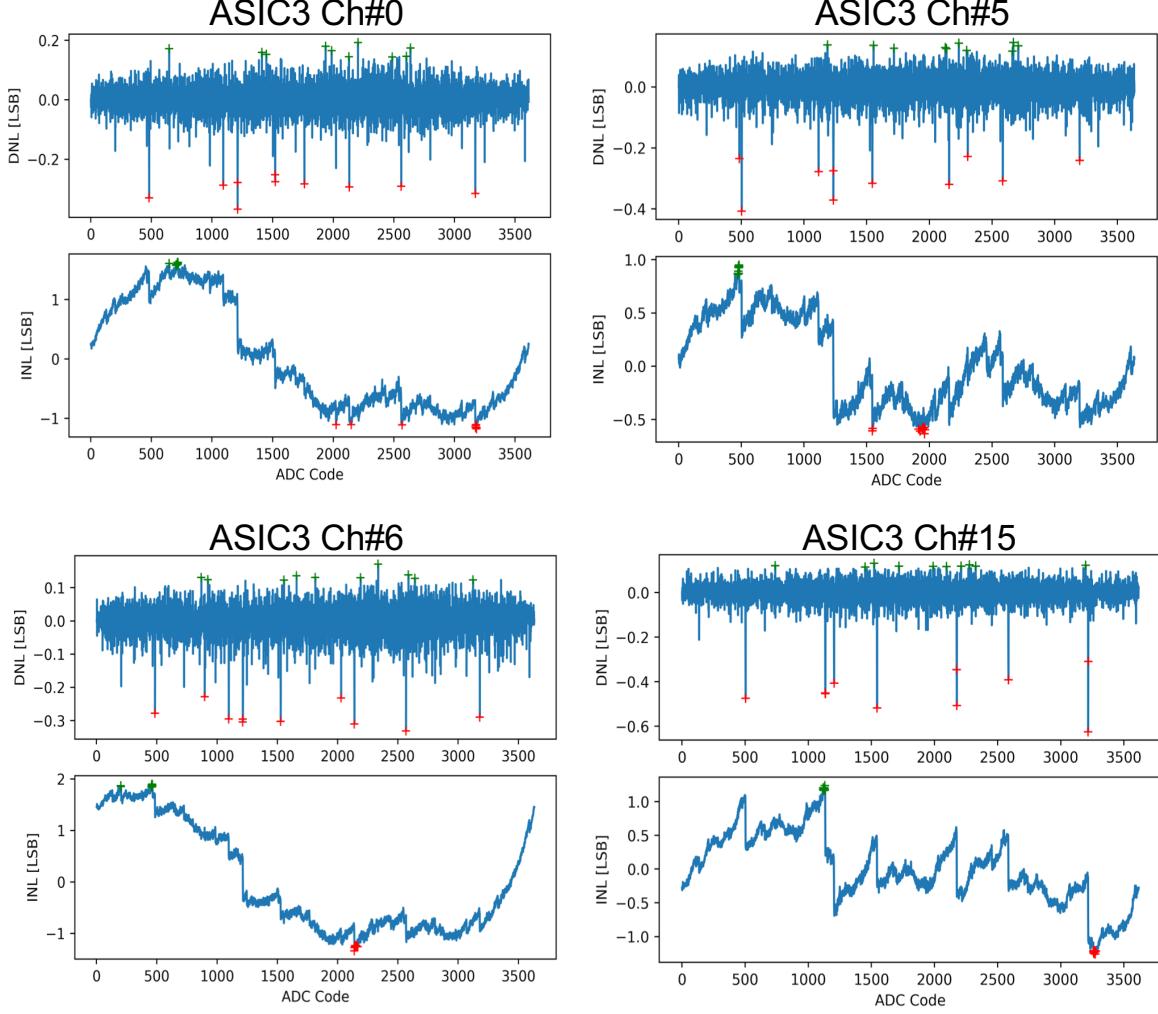


Figure 16: DNL and INL for a few representative channels on ColdADC ASIC#3 at LN<sub>2</sub> temperature.

The typical DNL vs. ADC code has a narrow band between  $\pm 0.1$  (12-bit) but exhibits large negative spikes. The source of the spikes are attributed to residual nonlinearity from the MUX-SHA stage (to be discussed in Section 5.4). The DNL extrema, dominated by the spikes, across all channels are typically between  $+0.2$  to  $-0.5$  LSB. The average INL extrema are from  $+1.2$  to  $-1.1$  LSB.

## 4.3 Dynamic Linearity (ENOB, SNDR)

The dynamic performance of an ADC is determined by the effective number of bits (ENOB). Figure 17 shows the Fast-Fourier Transform (FFT) from one of the ADC channels. The ENOB across ADC channels at LN<sub>2</sub> temperature is generally fairly uniform with a mean value of 10.6 and an RMS of about 0.3 bits. Table 3 lists the measured ENOB for the 16 ADC channels from one of the ASICs tested.

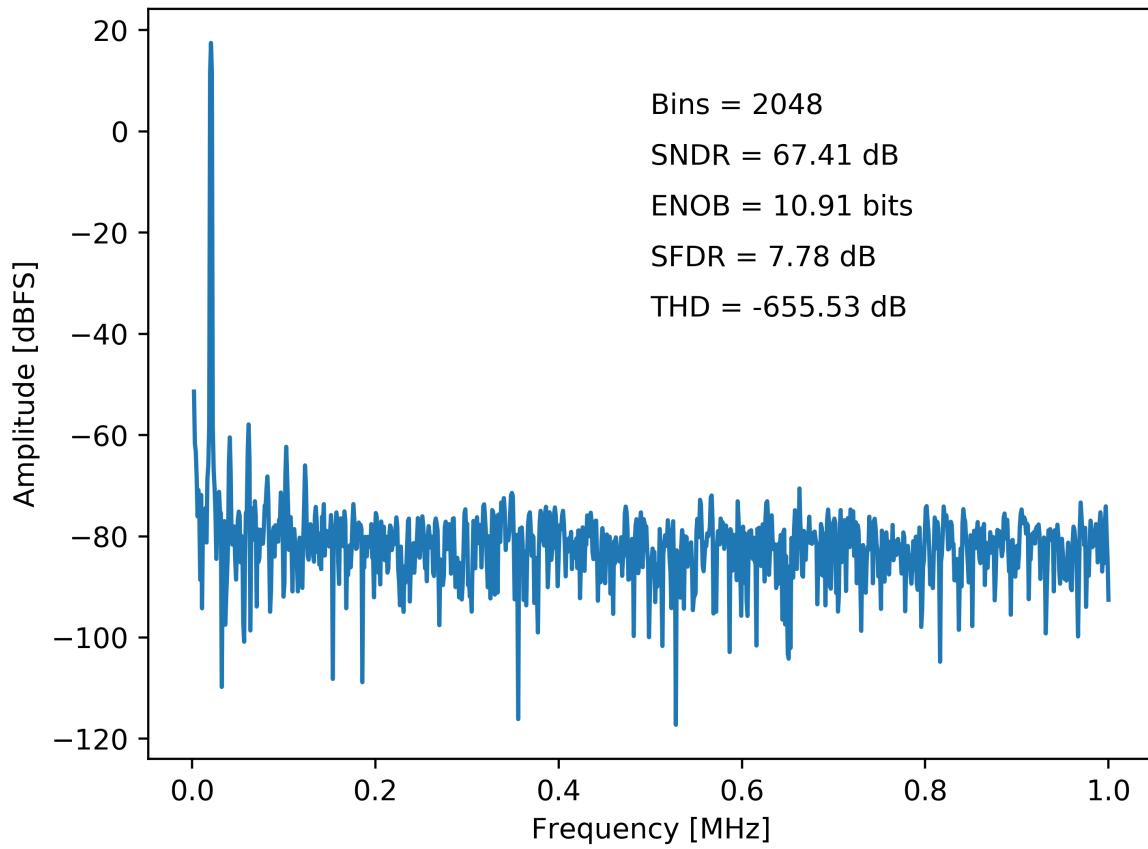


Figure 17: Fast-Fourier Transform of ADC output. Input signal is a 20.5 KHz sine wave.

Channel#	Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
ENOB	10.5	10.8	10.2	10.4	10.7	9.8	10.6	10.4
Channel#	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15
ENOB	10.2	10.5	10.6	10.5	10.7	10.3	9.8	9.7

Table 3: ColdADC ASIC# ENOB vs channel in LN<sub>2</sub>.

#### 4.4 Linearity Measurement using LArASIC Calibration Pulser

The LArASIC has an internal 6-bit DAC to generate a voltage step through a charge injection capacitor for calibration. Figure 18 shows the pulse response of channel 0 at room temperature. LArASIC is configured with 14 mV/fC gain, 2.0  $\mu$ s shaping time, 900mV baseline, output buffer off, DC coupling and 500pA leakage current. ColdADC is configured with single-ended input, BGR reference and 16-bit calibrated data. The observed non-linearity of 0.19ColdADC is expected to be less than 0.1%.

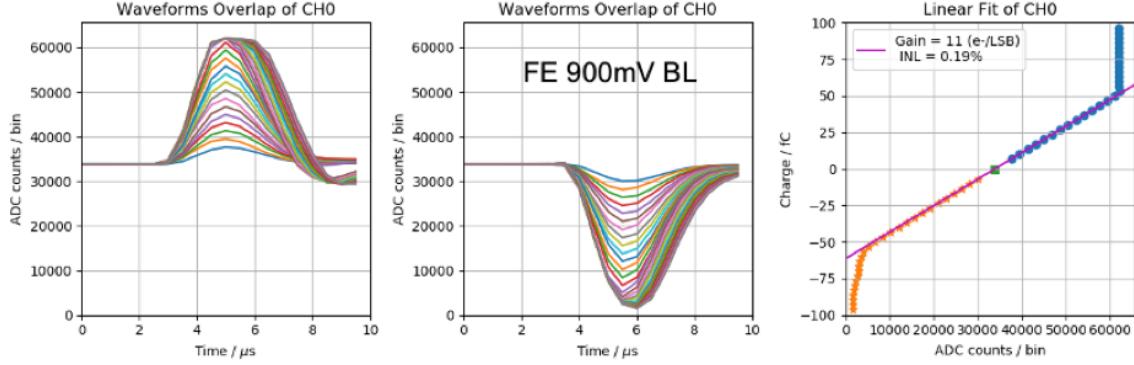


Figure 18: Response of LArASIC + ColdADC to the calibration pulse.

#### 4.5 Channel Crosstalk

The schematic diagram for the input channel crosstalk study is shown in Figure 19. The crosstalk on neighboring channels is related to the impedance of the channels. Instead of characterizing the crosstalk for the ColdADC alone, the crosstalk from both the LArASIC and ColdADC is measured together in this study. A large calibration charge pulse is injected into a specified LArASIC channel, and the responses of the neighboring channels are recorded. A sample crosstalk result at room temperature is presented in Figure 20. In this case the calibration pulse is injected into CHN0, and the largest crosstalk, close to 1%, is observed on CHN1. The crosstalk on the remaining channels is less than 0.5%. When the calibration pulse is injected into other channels one by one, it is observed that the next channel within the same ADC core has the largest crosstalk. This is an indication that the main contribution of the crosstalk is within the ColdADC itself. At cryogenic temperature, the magnitude of the crosstalk is significantly reduced to less than <0.5% across all channels. The results at LN<sub>2</sub> is shown in Figure 21 with LArASIC configured for 3 $\mu$ s shapping time and 14mV/fC gain setting. At 0.5% level, the crosstalk from LArASIC and ColdADC is negligible compared to the crosstalk contribution between sense wires.

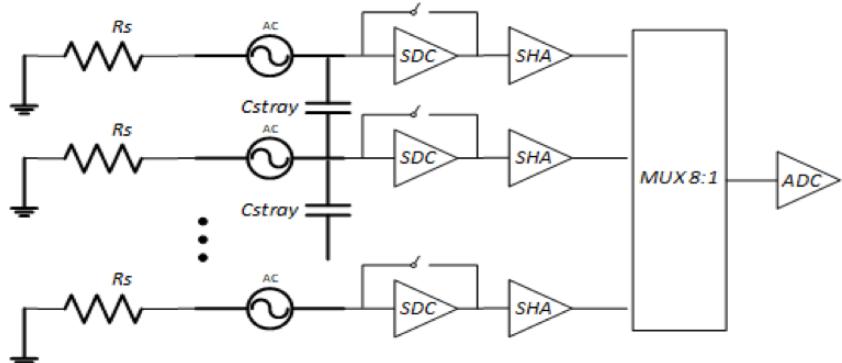


Figure 19: Schematic diagram of the crosstalk measurement.

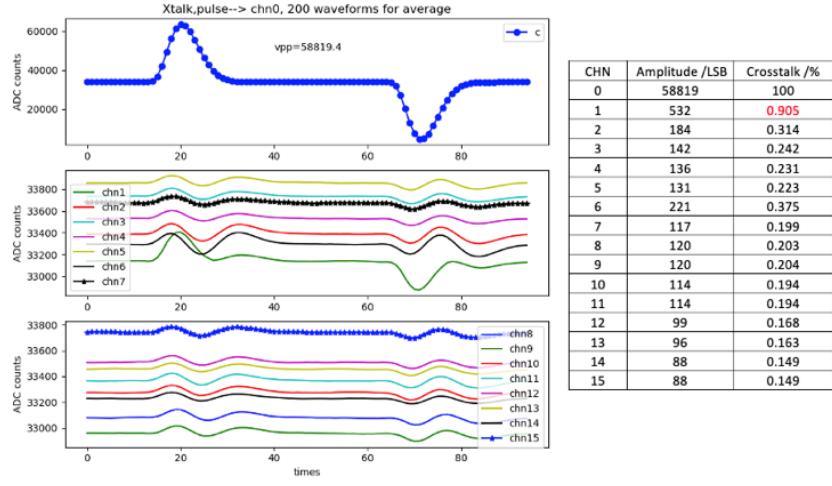


Figure 20: Crosstalk waveforms at room temperature. Calibration signal is injected in CHN0. The waveforms of the other 15 channels are shown in the bottom two plots. The amplitude of the cross talk is listed in the Table.

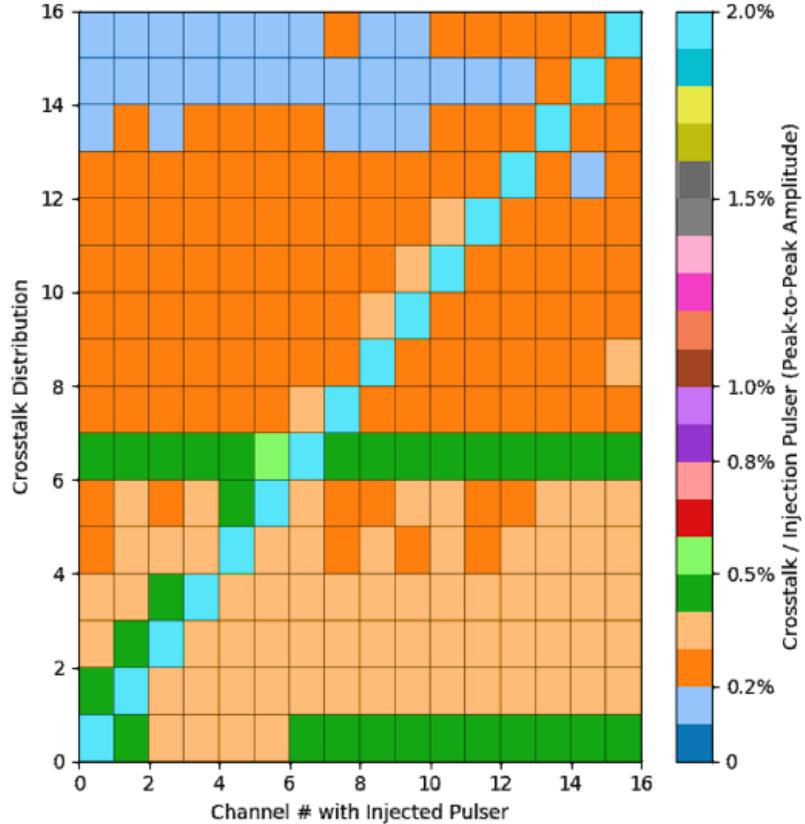


Figure 21: Cross talk distribution at  $\text{LN}_2$  temperature. The x-axis is the channel number with the injected pulse. The y-axis shows the amplitude of the crosstalk (in %) for the remaining 15 channels.

## 4.6 Power Consumption

The ColdADC is designed with several power rails with 3 different voltages: VDDA2P5/VDDD2P5 = 2.25 V, VDDIO = 2.25 V, and VDDD1P2 = 1.1 V. To achieve good ADC performance, the voltages are elevated to account for IR drop and other design issues. The VDDA2P5/VDDD2P5 voltage is raised to 2.5 V when using CMOS reference (2.7 V when using BGR), and VDDD1P2 to 2.1 V. Table 4 shows the measured power consumption under several operating configuration. If ColdADC is powered as the design expected, the power consumption is  $\approx$  20 mW per channel with SDC bypassed (powered down). If SDC is enabled, each channel will consume an extra  $\approx$  6 mW. When BGR reference is applied, with the elevated VDDA2P5/VDDD2P5 at 2.7 V, the measured power consumption is  $\approx$  30 mW per channel with SDC powered down. If CMOS reference is applied, VDDA2P5/VDDD2P5 can be set to 2.5 V to mitigate the power consumption, which is  $\approx$  26 mW per channel. The issue of raising VDDA2P5/VDDD2P5 to 2.7 V is related to the instantiation of an OTA with the wrong input pair polarity (to be discussed in Section 5.8). VDDD1P2 must be raised to 2.1 V due to the lack of DC voltage level shifters between 1.2 V and 2.5 V domains (to be discussed in Section 5.2). Both issues will be addressed in the next version of the ColdADC. We expect power consumption using BGR or CMOS references will be roughly the same, and the overall power consumption will be lowered with the new chip.

Temperature	RT	RT	RT	LN <sub>2</sub>	LN <sub>2</sub>	LN <sub>2</sub>
Reference	BGR	BGR	CMOS	BGR	BGR	CMOS
SDC	enable	bypassed	bypassed	enable	bypassed	bypassed
<b>VDDA2P5/VDDD2P5 / V</b>	2.5	2.5	2.5	2.5	2.5	2.5
<b>VDD1P2 / V</b>	2.1	2.1	2.1	2.1	2.1	2.1
<b>VDDIO / V</b>	2.25	2.25	2.25	2.25	2.25	2.25
<b>Total Power / mW</b>	515	418	418	563	513	425
<b>Power per Channel / mW</b>	32.2	26.1	26.1	35.2	32.1	26.6

Table 4: Power Consumption for ColdADC Chip#00067

## 5 Issues Identified and Mitigations

As mentioned earlier, during functional testing of the ColdADC, a number of problems were identified. A series of studies were carried out at the three labs to understand the issues, and come up with solutions to mitigate the problems for the current ASIC, and also fixes for the next version of the design. In this section, we will go through the various issues in more details.

### 5.1 Auto Calibration

The linearity of the ADC is primarily determined by the capacitor matching internal to the circuit, and to a lesser extent the performance of the internal amplifiers. To achieve the target specifications, the ADC requires calibration. The calibration in ColdADC can be carried out internally, in a fully automated way, or can be done externally. Unfortunately, while the chip can be fully calibrated externally, with calibration data loaded back onto the chip, the autocal function failed in the prototype. The ADC performance under autocal or external calibration does not differ in any way, so the main issue here is the loss of convenience that autocal promises.

When we developed the digital part of the ColdADC, we decided to partition the blocks such that the blocks that calibrate the ADC and compute the corrected digital output would be placed within the ADC cores, and the rest of the digital logic would be aggregated in a third core. This can be seen in Figure 22. The CAL\_UNIT is the block that performs the calibration and also applies the calibration coefficients (or weights) to the data during normal operation. Each CAL\_UNIT stores the calculated configuration weights to the register file in the CAL\_CORE (which was synthesized separately).

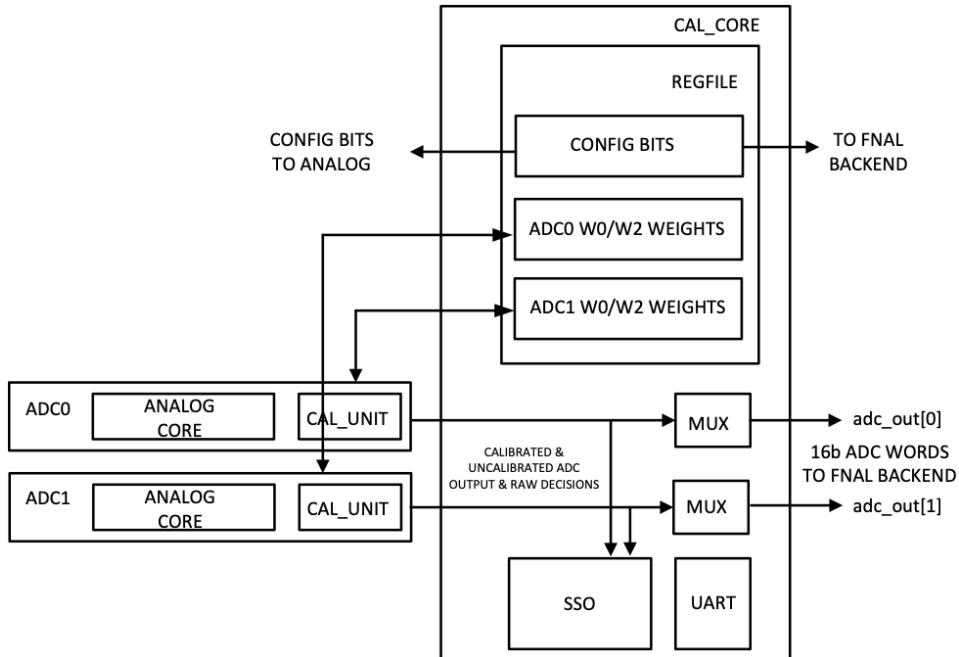


Figure 22: Partitioning of Digital Logic in the ColdADC.

This would have been an acceptable strategy but due to miscommunication the interface between the cores was not simulated with back-annotated timing. This means that the timing when a computed calibration coefficient is written back into the registers was not simulated properly. When the blocks were placed, there was a timing error between the CAL\_UNIT and the CAL\_CORE in the case when the CAL\_UNIT was writing back computed calibration weights into storage in the CAL\_CORE.

An example of the intended operation is shown in Figure 23. In this simulation the CAL\_UNIT is back annotated with parasitics (but the interface with the CAL\_CORE is not properly back annotated). In this simulation, the intended data is in the second row (the word 0x03FD) and is written to the w2\_4

register that resides in the CAL \_ CORE correctly. Correct operation is assured by disabling the memory after the edge of clk.

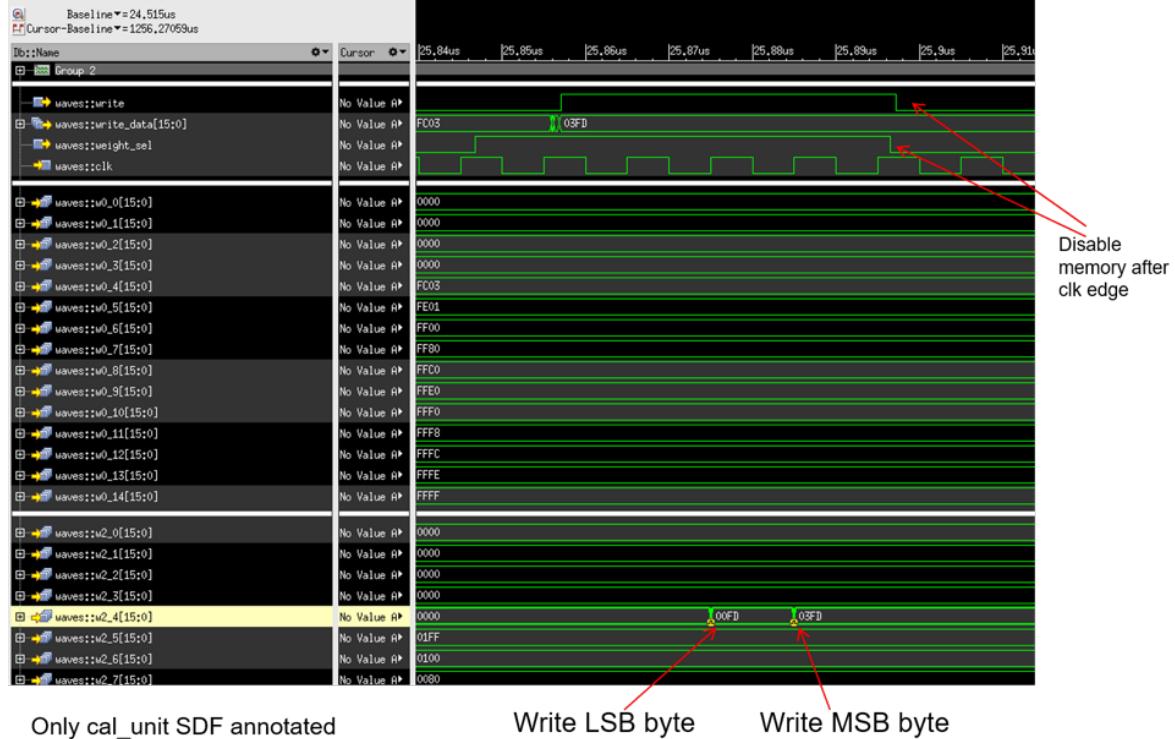


Figure 23: Correct writeback of calibration weights

When the interface between CAL \_ UNIT and CAL \_ CORE was properly annotated and simulated, the result was in Figure 24.

A gross error has been made, because the write signal is released too soon and therefore we have a race condition. What happens specifically here is that due to the race condition, the LSB byte of w0[4] is overwritten with the LSB byte of w2[4]. This is error and causes the entire calibration sequence to fail.

The fix here is to repartition the digital logic for the second version of the ColdADC ASIC. We will move the digital calibration and correction logic out of the ADCs and into a single, monolithic digital block as shown in Figure 25. This will ensure that the interfaces between the calculation engines and the memory are simulated correctly and the absence of race conditions will be verified using static timing analysis. The RTL code itself will also be made more robust by adjusting the internal state machine.

## 5.2 Level Shifter

Because the digital core of the Cold ADC uses 1.2 V rails, but many of the analog circuits on the chip use 2.5 V rails, level shifters are required to translate control settings from the 1.2 V voltage domain to the 2.5 V voltage domain. Unfortunately, due to confusion during the design process, the required level shifters that were required for the front end single-ended-to-differential input buffer were not included. Therefore, in order to configure the block correctly, the 1.2 V digital supply must be elevated. While this allows the chip to be operated successfully, it is not compatible with long-term reliability. The fix is to include the proper level shifters in the next version of Cold ADC. The fix has already been made in the layout.



Figure 24: Error in writeback of calibration weights

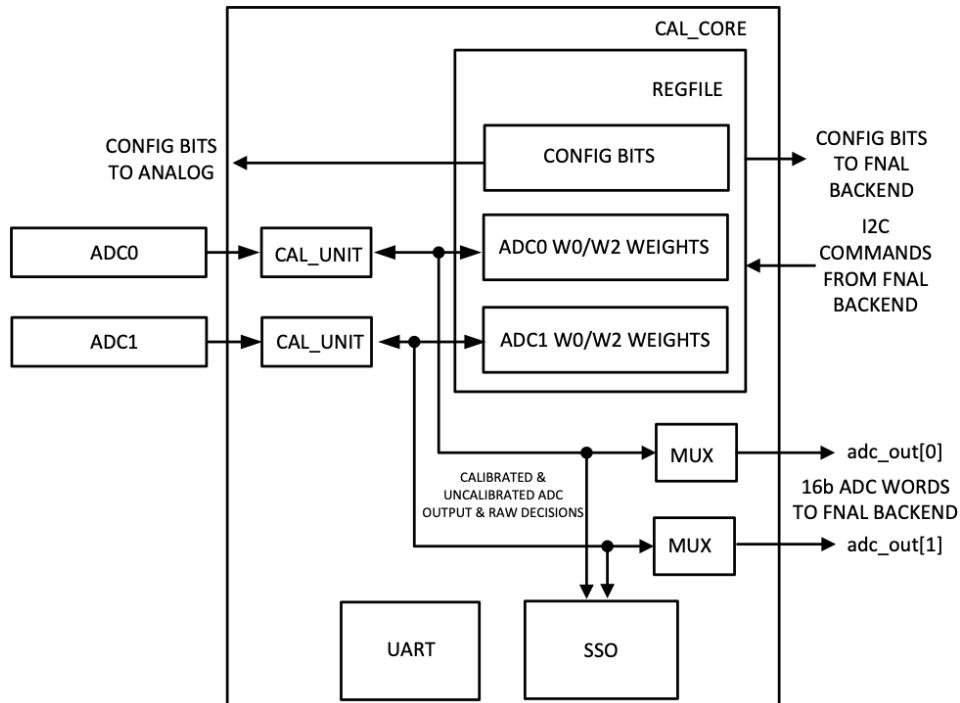


Figure 25: Proposed Calibration Digital Logic partitioning in revised prototype.

### 5.3 ADC Core Linearity

The measured ADC INL of the Cold ADC is approximately 1 LSB at a 12-bit level. However, simulations suggest 0.5 LSB INL after calibration is possible. The key reasons for the discrepancy is the lack of corner models at cold and the Monte Carlo analysis done using the warm models was insufficient. Testing indicates the ADC linearity is limited primarily by insufficient op-amp gain in the stages. Since the calibration algorithm can only correct linear gain error, higher-order non-linearity beyond what was expected limited the performance. The op-amp becomes nonlinear as their swing increases because the output resistance of the devices connected to the output decreases when the voltage across them is reduced. This is a known issue and was mitigated in the design by increasing the open-loop gain. The main suspect in the reduced linearity is that the raw open-loop gain is lower than expected and therefore the closed-loop rejection of the non-linearity is not good enough. To verify the large closed-loop gain non-linearity in the stages, we adjusted the reference voltages to reduce the dynamic range of each stage and this improved the linearity, as it should if the nonlinearity steps from the output stages of the op-amps. This is demonstrated in Figure 26 and 27. In Figure 26, the differential reference is reduced 100 mV from nominal, and in Figure 27 the differential reference is reduced 200 mV from nominal. Comparing Figures 26 and 27, the DNL is improved and becomes more uniform as the reference is reduced.

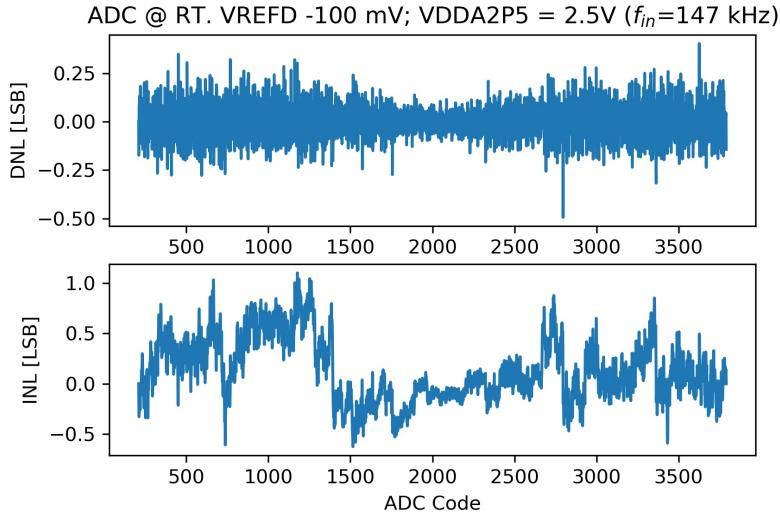


Figure 26: ADC linearity with VREFN/P +/- 100mV

To get evidence about what is the root cause of the increased linearity, we can use the programmability of the ColdADC to run various experiments to rule out potential causes. To rule out that the observed nonlinearity was caused by incomplete stage settling, we first operated the ADC with increased bias currents, to reduce settling time. This did not improve performance. We then slowed down the ADC by a factor of 16 and reduced the op-amp bias currents. Reducing the bias currents has the effect of increasing the op-loop gain, but also slows down the circuit, necessitating the reduced sampling rate. The results of this experiment is shown in Figure 28. The ColdADC demonstrates superior performance in this situation, strongly suggesting the increased open-loop gain mitigates the gain-drooping caused by the op-amp output resistance. Note that the references are nominal here, showing that the observed nonlinearity it reduced in this case by the negative feedback.

A schematic of the op-amp used in the ADC stages is shown in Figure 29. The circuit uses a standard folded-cascode topology with gain boosting amplifiers used to increase the open-loop gain. These gain boosting amplifiers work by regulating the voltage drop across the output transistors, increasing their output resistance. Simulations suggested that the gain boosting amplifiers increased the open-loop gain of the op-amp by approximately a factor of 5 (14 dB).

To narrow down what precisely in the op-amp was causing the lower-than-expected gain, we disabled the gain boosting amplifiers. This is possible to do through the configuration interface and was included

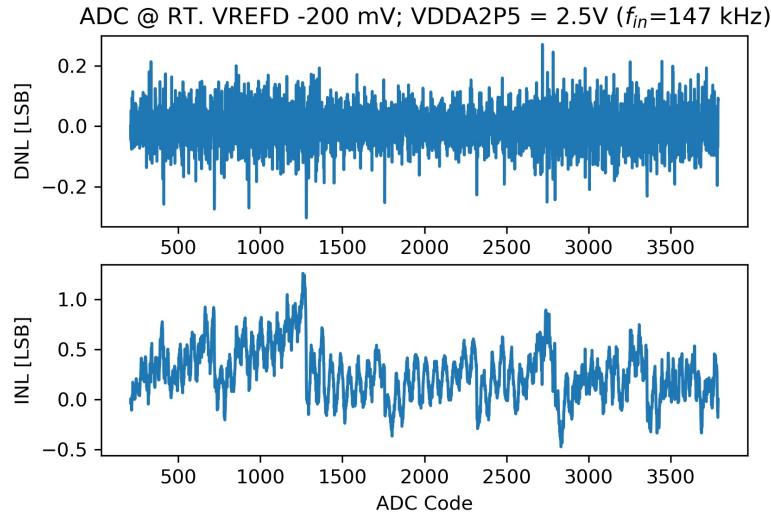


Figure 27: ADC linearity with VREFN/P +/- 200mV

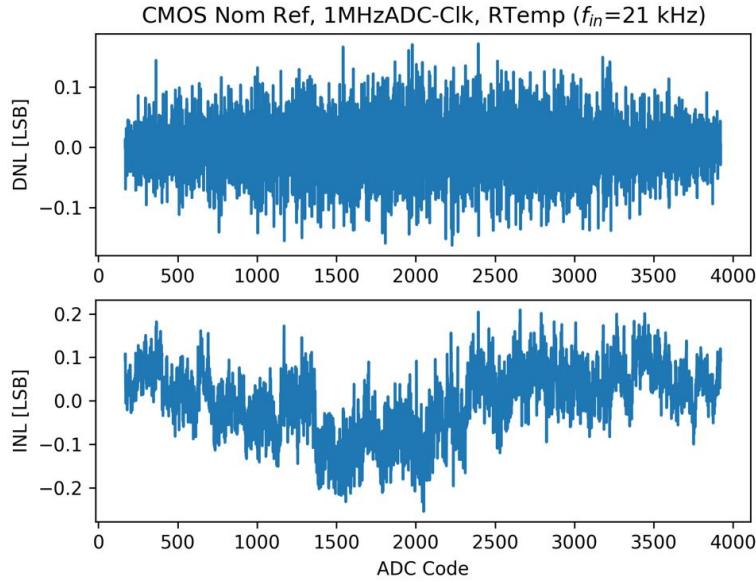


Figure 28: Linearity with Gain Boosters ON

for debugging purposes. When we disabled the gain boosting amplifiers, but held all other conditions constant, the linearity degraded as shown in Figure 30. In fact, the INL increased by over a factor of 2 and the DNL increased as well.

For further evidence, we modeled the ADC behaviorally using MATLAB. The simulated linearity obtained after setting the op-amp open-loop gain in the model to 80 dB is shown in Figure 31, which is a result similar to Figure 28. By reducing the open-loop gain to 74 dB, we obtained the result in Figure 32 which closely follows the linearity structure of Figure 30, this gives further evidence the issue is insufficient gain in the gain boosting amplifiers. Based on the behavioral modeling, we estimate the gain-boosting amplifiers are providing approximately 6 dB in additional gain, rather than the 14 dB that was expected.

Analysis of the circuits in the gain-boosting amplifiers indicates that they may have insufficient design margin in their biasing networks. The gain-boosting amplifiers and op-amp can be improved by

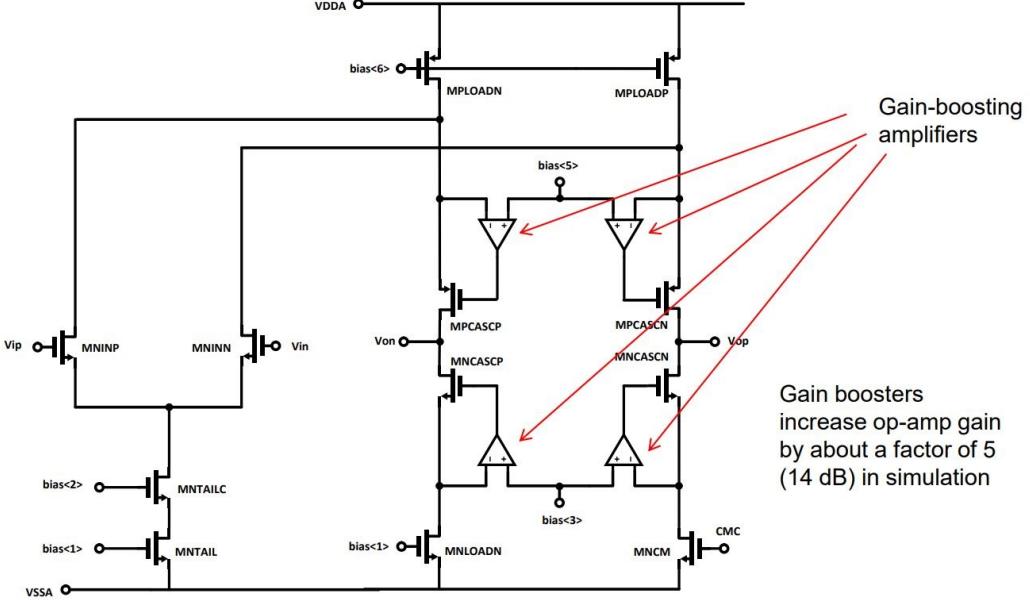


Figure 29: Op-Amp used in ColdADC stages.

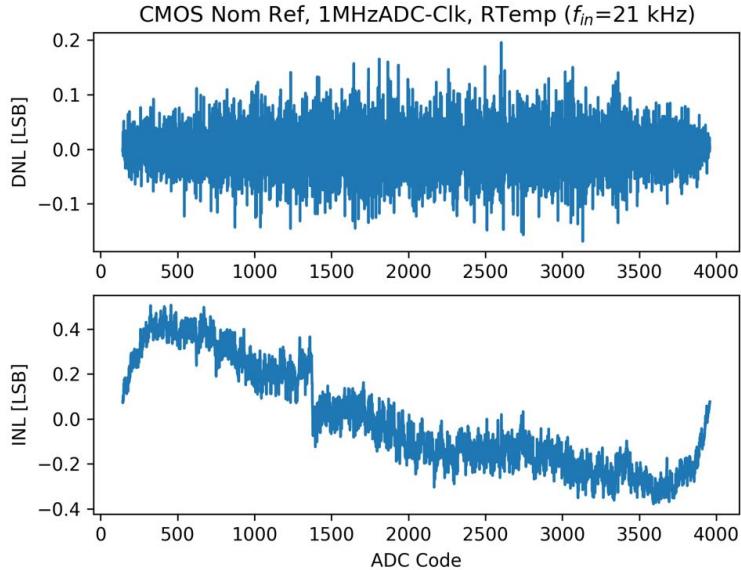


Figure 30: Linearity with Gain Boosters OFF.

redesigning them to better center their operating points across process and temperature.

Corner analysis of the complete op-amp before and after the gain-boosting redesign is shown in Figures 33 and 34, respectively. While the corners are only strictly valid at room temperature, the take away here is that the minimum open-loop gain across corners after the redesign is higher than the maximum open-loop gain before redesign. The design fix is being finalized and will soon be implemented in the layout.

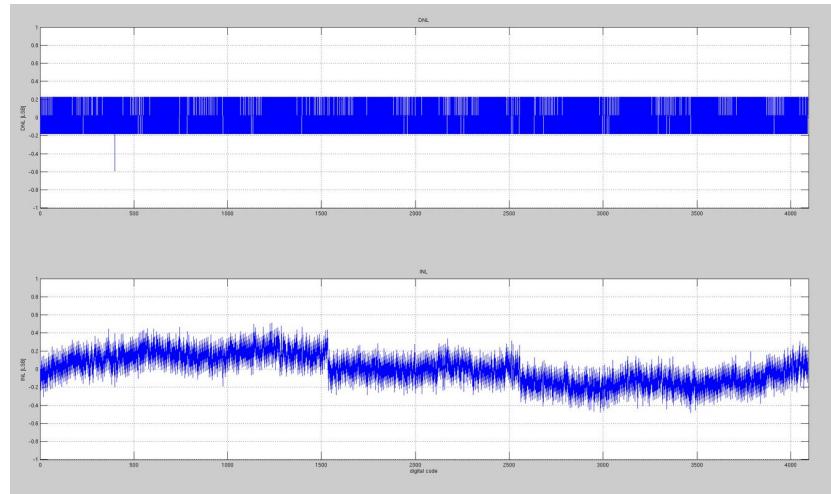


Figure 31: MATLAB model - gain boosters on  $\rightarrow$  80 dB op-amp gain.

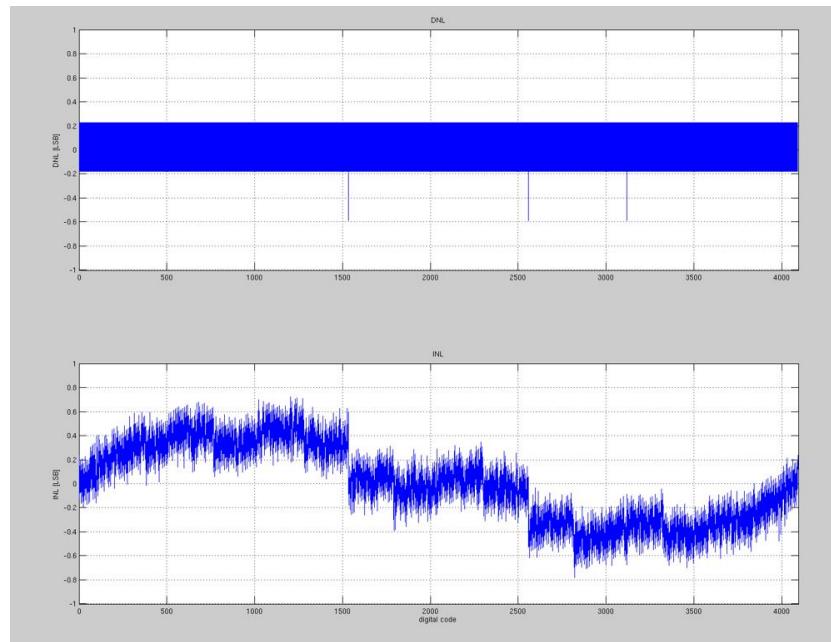


Figure 32: MATLAB model - gain boosters off  $\rightarrow$  74 dB op-amp gain.

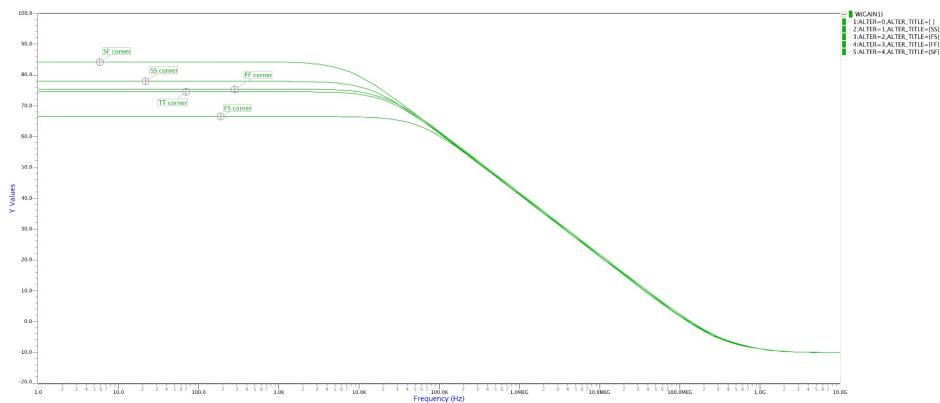


Figure 33: Corner analysis of the op-amp gain, with current gain booster circuit.

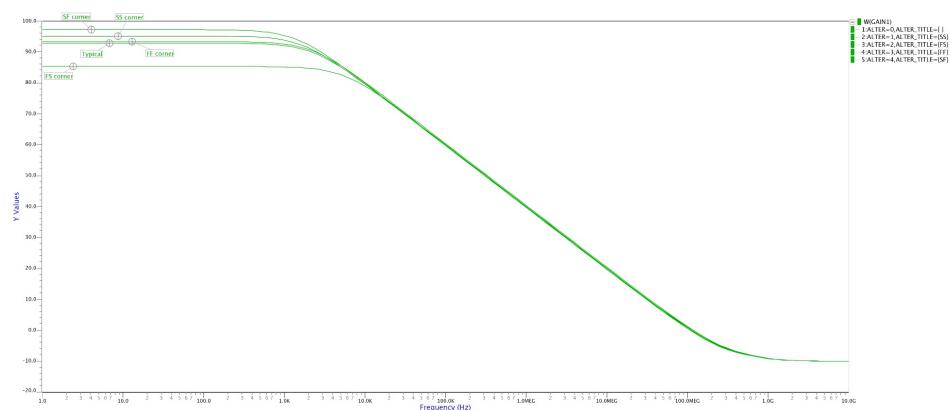


Figure 34: Corner analysis of the op-amp gain, with improved gain booster circuit.

## 5.4 SHA/MUX Linearity

The input signals are sampled at a rate of 2 MS/s, multiplexed by 8 and digitized by one of two calibrated 12-bit pipelined ADCs operating at 16 MS/s. The overall integral non-linearity of the ADC is due to the integral non-linearity of the front-end (SDC), SHA, MUX as well as the ADC transfer function. Programming the ColdADC in ADC only mode, frozen SHA mode and free running SHA mode, we were able to measure linearity for ADC only, ADC + SHA and ADC + SHA + MUX configurations.

In the frozen SHA mode (ADC + SHA) we observed the overall linearity is slightly different for different sample sets. In this mode, the ADC will oversample the SHA output by a factor of 8 and the linearity of the ADC can be calculated by taking any of the samples. Figure 35 shows that the samples are not consistent and non-linearity has been introduced by SHA/MUX combination. The main source of non-linearity could be SHA op-amps or the MUX.

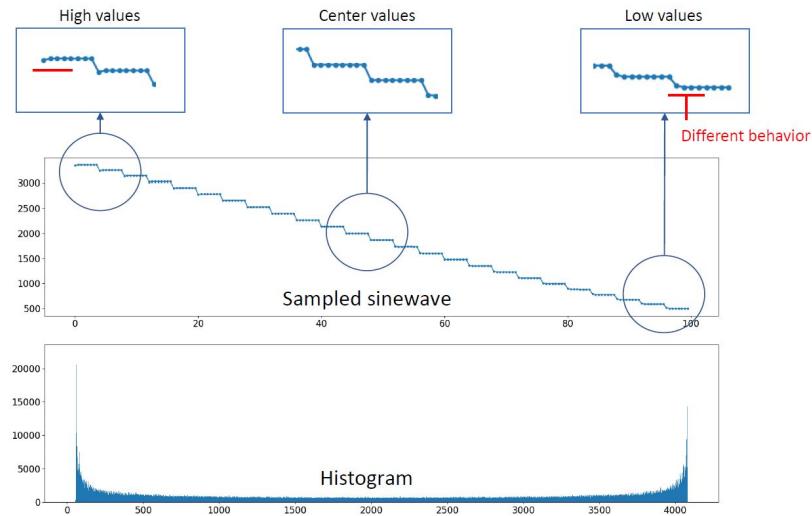


Figure 35: Histogram of ADC sampling in frozen SHA configuration

To narrow down if any of this non-linearity was causing by the SHA op-amps, we varied the SHA bias current. The change in the SHA bias current did not affect the overall linearity of the ADC. Figure 36 shows the linearity of ADC measured by looking at the second sample of channel 7 at  $40\mu\text{A}$ ,  $50\mu\text{A}$  (default) and  $60\mu\text{A}$  SHA bias currents. These measurements were taken at room temperature with nominal sample rate.

In the next study, we reduced the sampling speed of the ADC. With reduced sampling speed the MUX's will have more time to settle and be less sensitive to kickback effect, if any. Figure 37 shows the overall linearity at different sampling clocks. Reducing the sampling frequency improves the linearity significantly. Based on the results of the studies, the MUX's seem to be causing the non-linearity and kickback is likely the main source of the problem. To address this issue we plan to redesign the MUX to be faster.

Another observation when ColdADC is in free running SHA mode at LN2 temperature is that large spikes appear in the DNL plots. These spikes do not appear in frozen SHA configuration or at slower clock speed. Figure 38 shows the difference in linearity for free running SHA mode and frozen SHA mode at LN2 temperature and the 10 most extreme values are labeled in the plots. While the root cause of these spikes is still not fully understood, we believe that redesigning the MUX to be faster will likely resolve this issue as well.

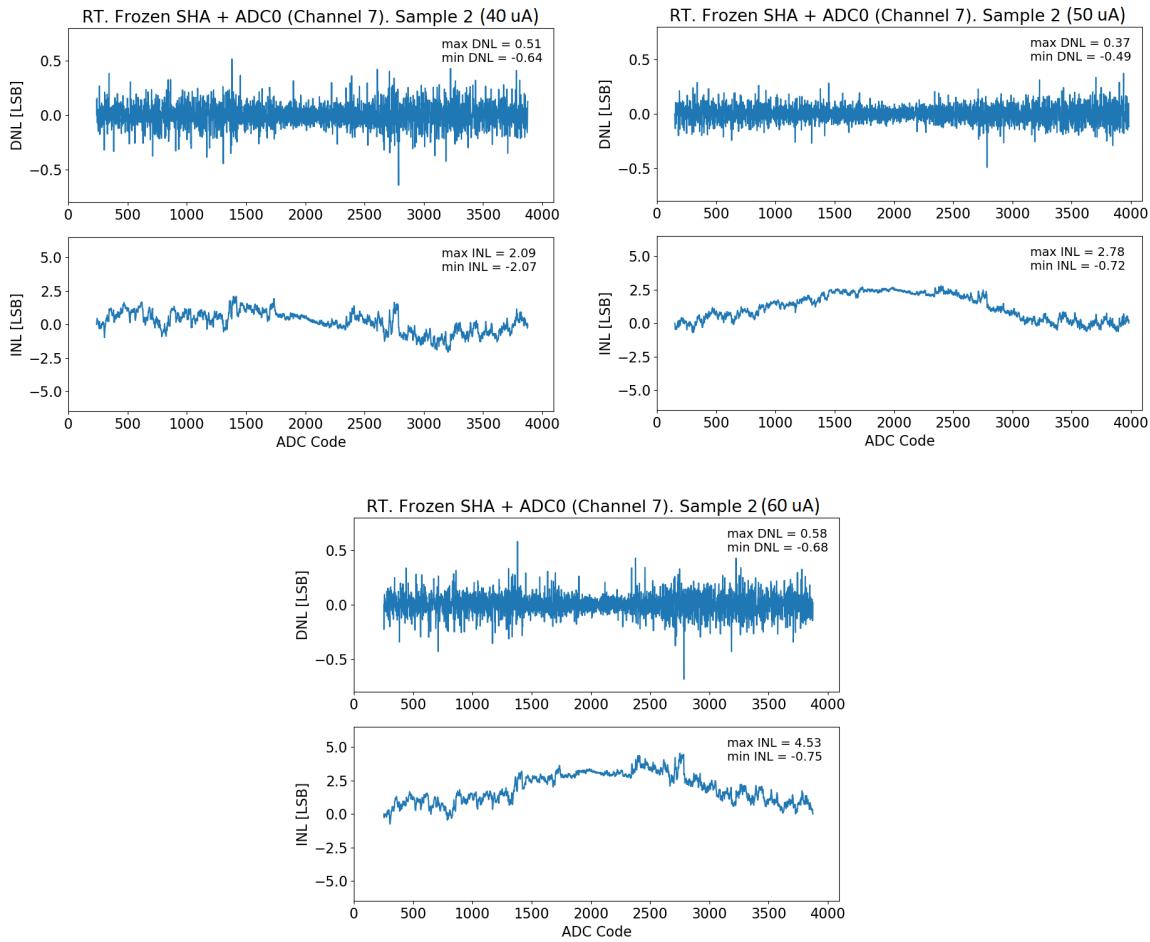


Figure 36: Linearity of ADC at room temperature with SHA bias current configured to 40, 50, and 60  $\mu$ A.

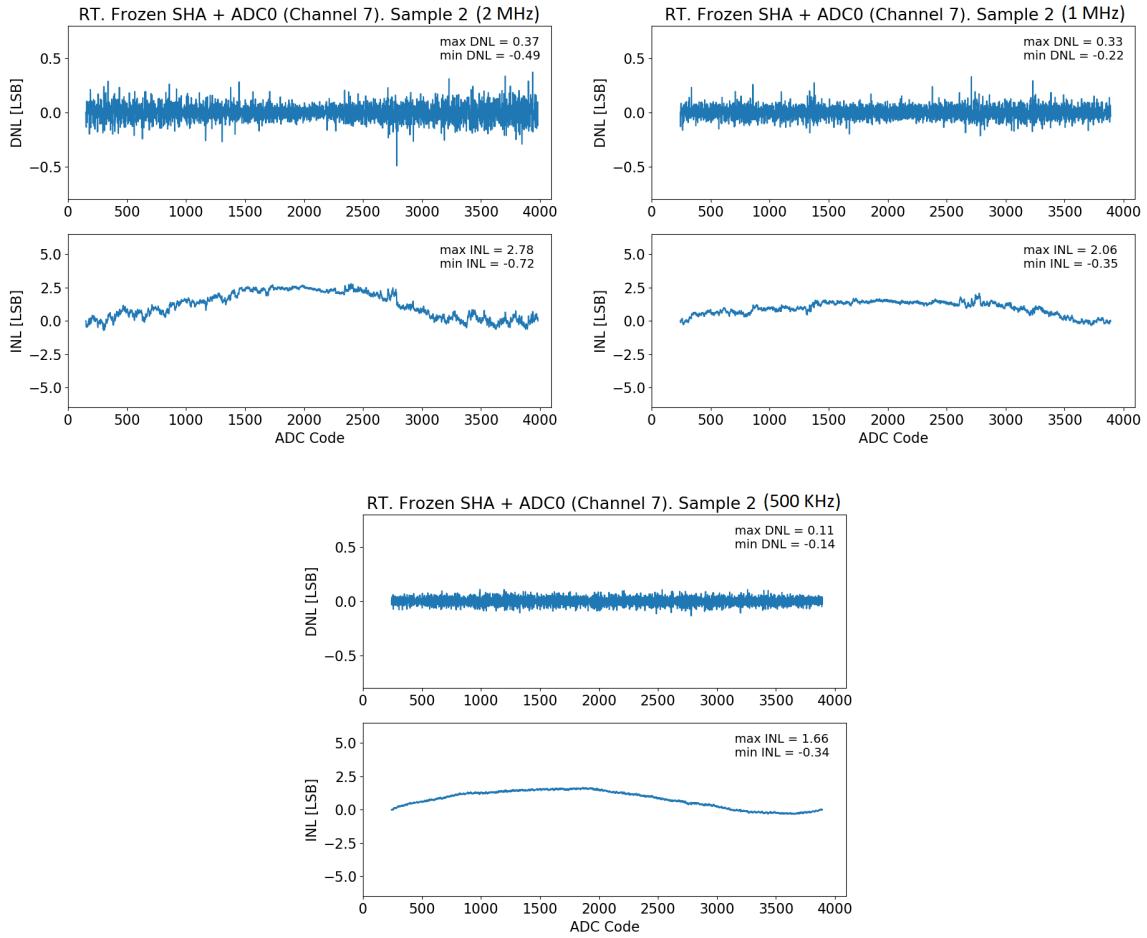


Figure 37: Linearity of ADC at room temperature with 2, 1, 0.5 MHz sampling frequencies.

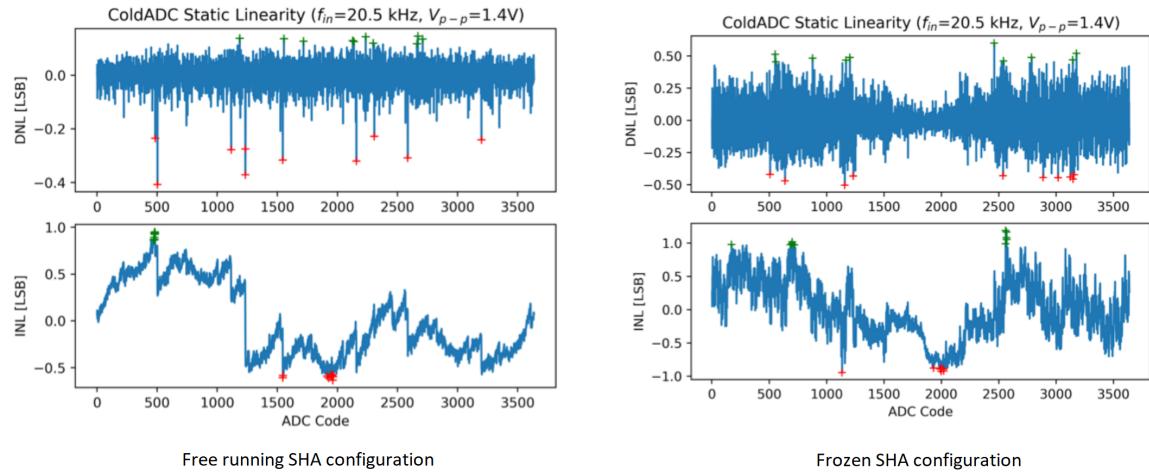


Figure 38: Linearity comparison of the ADC with single ended input in free running SHA and frozen SHA mode at LN2 temperature

## 5.5 SDC Linearity

The ColdADC Input Buffer contains two blocks - a Single-to-Differential Converter (SDC) and a Differential Buffer (DB). The former one accepts single-ended signals and converts them to fully-differential ones, has a low-capacitance input-impedance, and drives the capacitive switching load of the SHA. The latter one buffers differential input signals, has a static capacitive input impedance, and drives the switching load of the SHA. Each of these two blocks can be separately powered-down and bypassed.

LArASIC outputs single-ended waveforms; therefore, the performance of each ADC input channel when accepting single-ended signals is of high importance. Single-ended input signals to the ADC can be converted to fully-differential signals in either a SDC or SHA block. The performance merit of primary interest are input channel DNL and INL at room (RT) and cryogenic temperatures (Liquid Nitrogen - LN) when driven by a single-ended source, with and without the SDC block.

Figures 39 and 40 show measurements of maximum INL and maximum DNL across all ADC channels at room and cryogenic temperatures, respectively. These were derived from measurements presented in Figures 41, 42, 43 and 44. Figure 45 depicts ENOB across ADC channels with and without the SDC.

Measured results are insufficient in providing a conclusion as to whether the SDC block improves or deteriorates ADC's performance. However, measurements at LN temperature show slight improvement, on average, in DNL across channels with the SDC turned on. Measurements also indicate introduction of larger channel-to-channel variation in INL when the SDC is on. However, this might be related to bypass switches and/or other interfaces, not the SDC alone.

A standalone SDC circuit is currently being tested and a statistical analysis on a larger set of samples of standalone chips is also planned for. These results might help to answer some of the above questions/uncertainties.

Current recommendation is to remove the SDC block from the ADC input chain and implement it in the LArASIC channel.

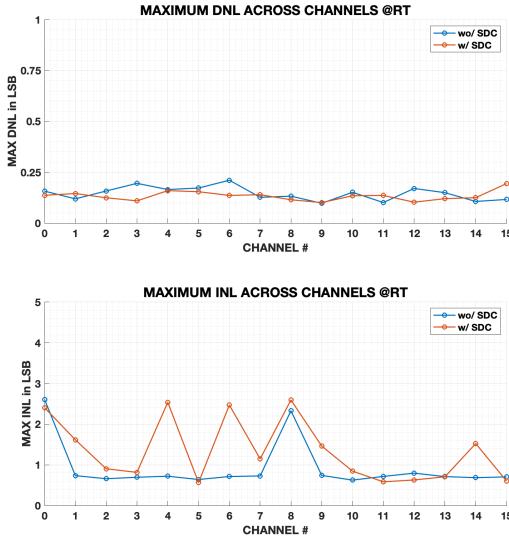


Figure 39: Maximum DNL and INL across ADC channels at room temperature.

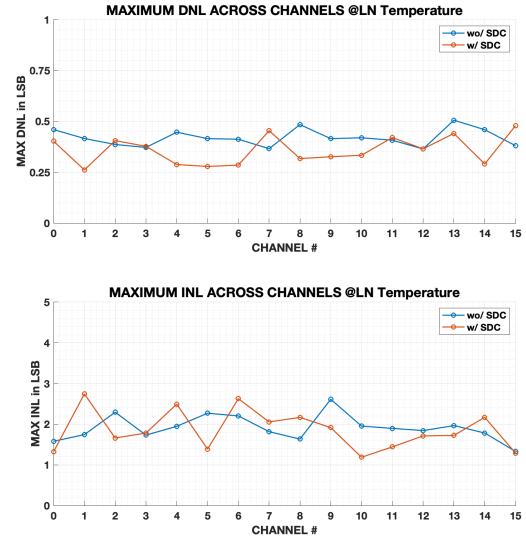


Figure 40: Maximum DNL and INL across ADC channels at liquid nitrogen temperature.

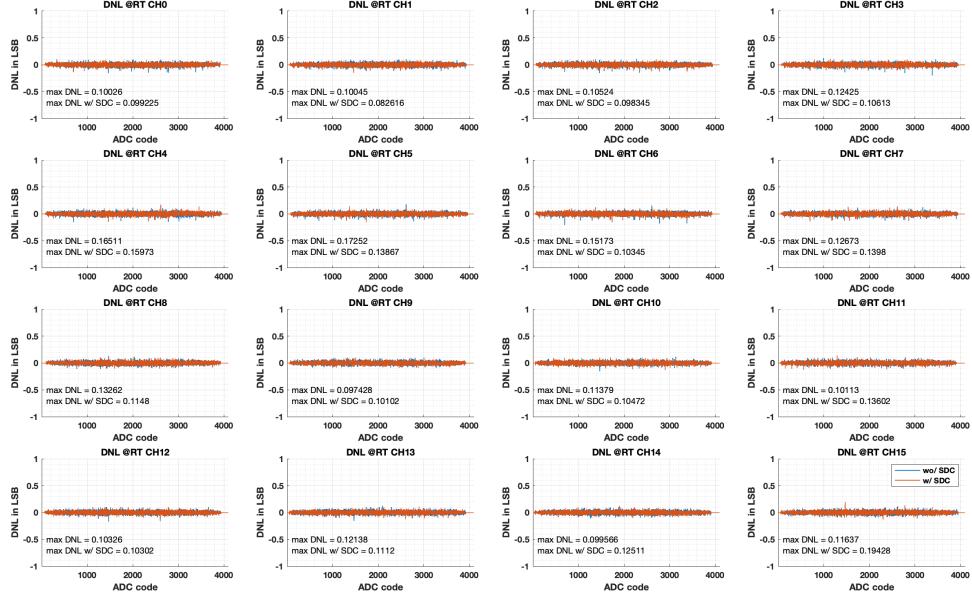


Figure 41: Measurement of DNL across all ADC channels at room temperature. Blue - SDC off, Orange - SDC on.

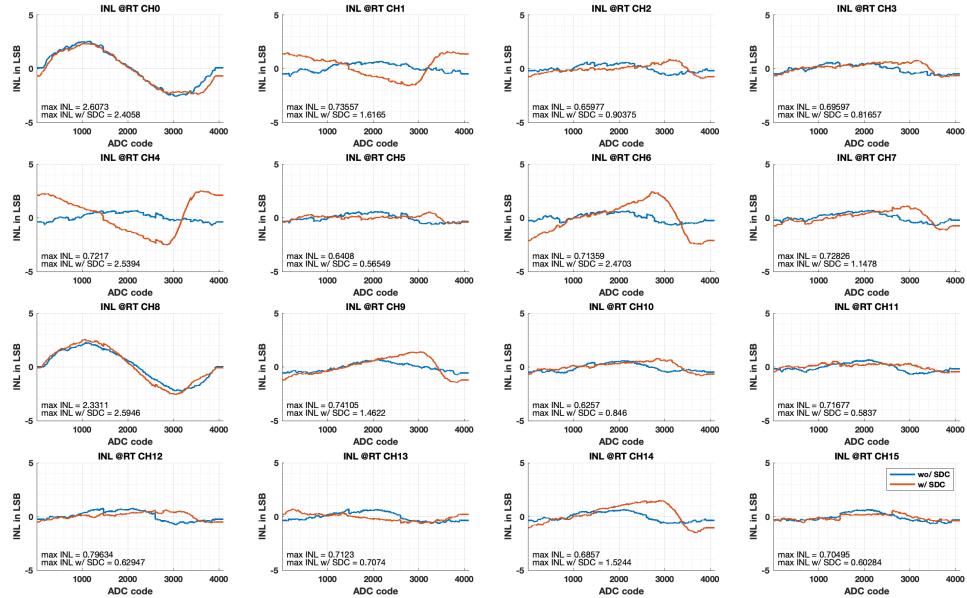


Figure 42: Measurement of INL across all ADC channels at room temperature. Blue - SDC off, Orange - SDC on.

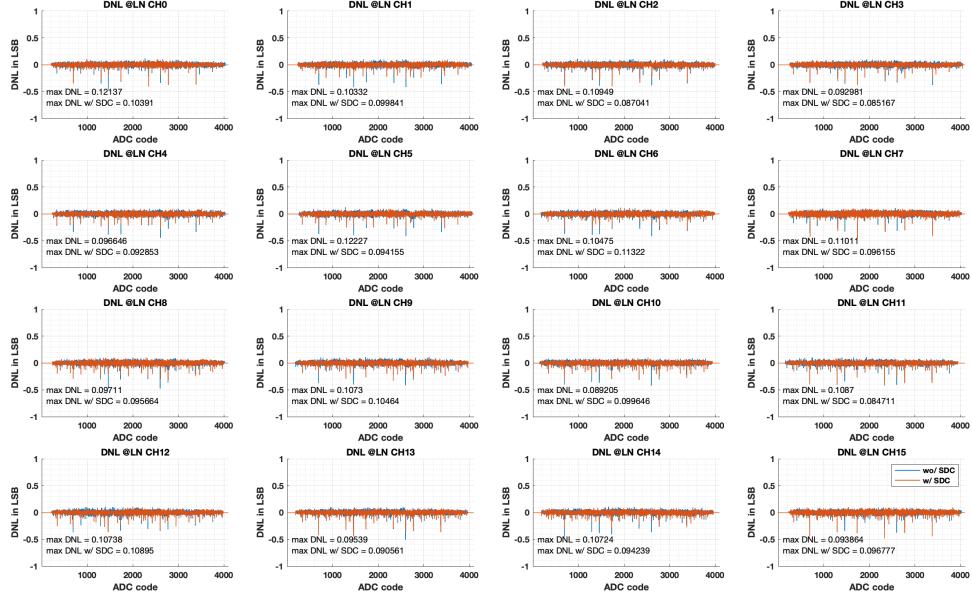


Figure 43: Measurement of DNL across all ADC channels at liquid nitrogen temperature. Blue - SDC off, Orange - SDC on.

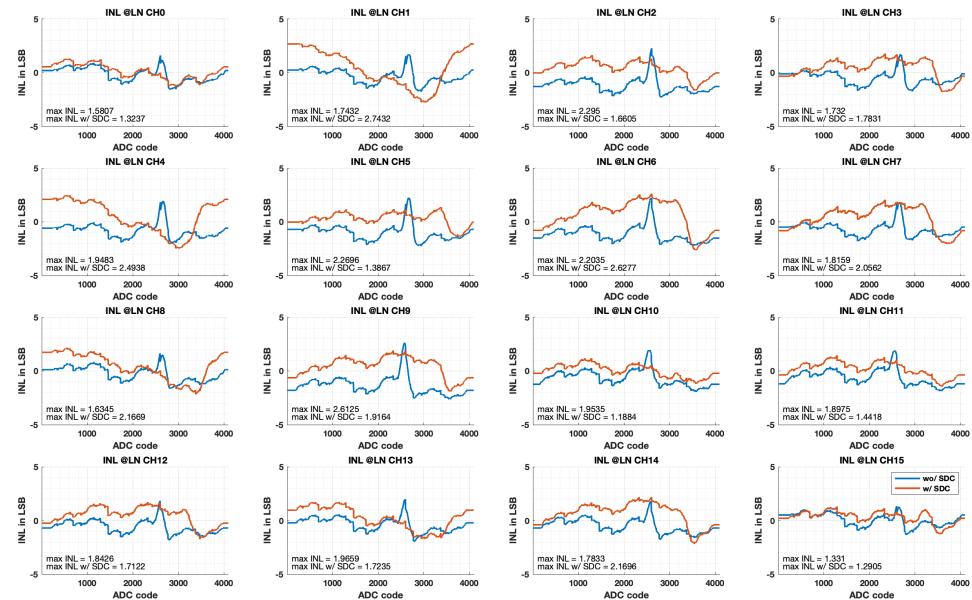


Figure 44: Measurement of INL across all ADC channels at liquid nitrogen temperature. Blue - SDC off, Orange - SDC on.

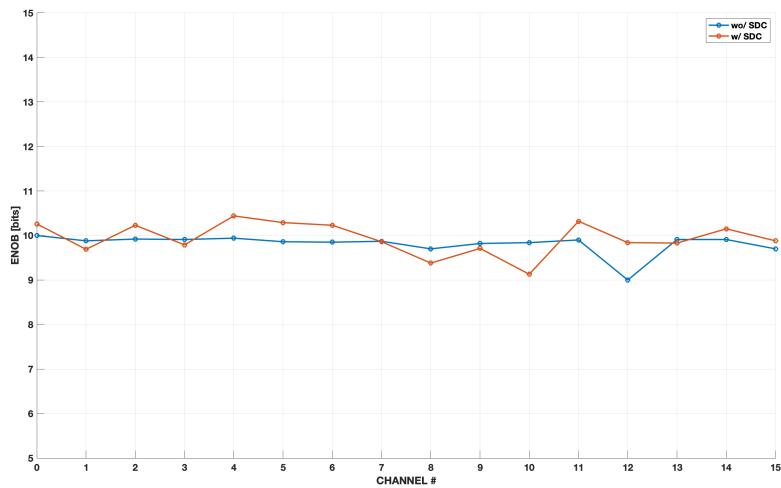


Figure 45: Measurement of ENOB across all ADC channels at room temperature.

## 5.6 IR Drop

At room temperature, when the test inputs are used to test the pipeline ADCs individually (bypassing the input buffers, Sample and Hold Amplifiers (SHAs), and the SHA multiplexer), significant non-linearity is observed for input signals near the voltage extremes of the ADC. At cryogenic temperature, no significant deviation from linearity is observed. We interpret this as evidence that there is an IR drop on the analog 2.25V power when the chip is operated at room temperature. The fact that the non-linearity is not observed at cryogenic temperature or elevated analog supply voltage (from 2.25 to 2.5V) at warm is consistent with the fact that the resistivity of the metal used to distribute the power is greatly reduced at cryogenic temperature. Metal layers M8 and M9 were used for power distribution. The redistribution layer (AP) was not used and could easily be added to the power mesh in the analog sections of ColdADC. We will make this change in the next submission.

## 5.7 SHA/MUX Crosstalk

While there is no formal specification regarding the channel crosstalk, we have measured crosstalk of  $< 0.5\%$  in LN<sub>2</sub> and  $< 1\%$  at RT. We have done a variety of measurements that suggest the crosstalk is due to kickback between the channels during the sampling phase that makes it so the SHAs are not completely settled between samples. When the channels are slowed down, the crosstalk is somewhat mitigated, which indicates that it is due to insufficient bandwidth in the SHA Mux. To improve this, we will lower the impedance of the Mux to allow faster settling.

## 5.8 Bandgap Voltage Reference (BGR) Op-Amp

To operate correctly, the ColdADC requires accurate voltage references for the ADC. In addition, the various analog circuits on the prototype require bias currents. To mitigate risk, the ColdADC includes two redundant reference generation blocks to supply these needed voltages and currents, one block based on a bandgap reference, and one based on a CMOS reference. Which reference to use can be selected by setting the appropriate bits in the control registers.

A voltage proportional to the bandgap of silicon is generated in the V-BGR core. This voltage is then converted to a current in the I-DAC block to generate bias currents. In addition, the bandgap voltage is scaled by the various V-DAC blocks. Because the reference voltages for the ADC span a significant portion available power supply voltage, two different versions of the V-DAC are required: one to generate voltages near the supply voltage, and one to generate voltages near ground. Unfortunately, the wrong version of the V-DAC was included to generate VREFP (a voltage near the supply is required, but the included V-DAC is the version intended for voltages near ground). The included V-DAC can still generate the required voltage for VREFP if it is given significant additional headroom, in other words if VDDA is elevated above nominal.

While the BJT-based reference is fully functional in this case, it is not appropriate for long-term reliability because the supply should be operated below nominal, not above. The fix for this design error is simple: replace the VDAC that generates VREFP with the appropriate version of the V-DAC.

## 5.9 Overflow Wraparound

The gains of each stage are weighted by the calibration. If the sum of the weights of the stages is greater than  $2^{16}$ , then the digital correction logic can overflow, and a large input can lead to a small output code and vice versa. The stages were designed with an analog closed-loop gain slightly less than two. Based on supplied process data, we expected the closed-loop gain would be low enough to be free from overflow. In fact this was not the case and overflow was observed when the input voltage was close to one of the reference voltages. This can be seen in Figure 46, which shows the response of the two different ADCs on one of the ColdADC prototypes to the same input signal. The left portion of Figure 46 shows the ramp response of ADC0 and the prototype operates as expected. When the ADC is saturated, the digital output is pinned to its maximum value. On the right portion of Figure 46 overflow is observed as part of the ramp response of ADC1. In this case, the ADC input reaches its maximum value but instead of remaining pinned, the digital output jumps to a low value. This is due to higher-than-expected closed-loop gain in ADC1.

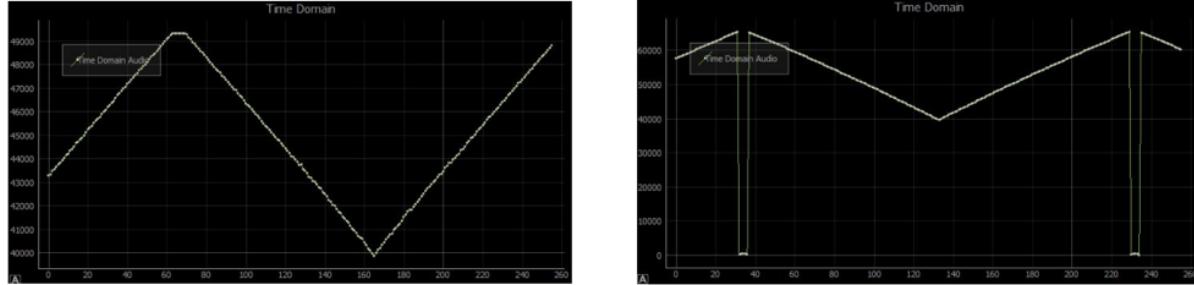


Figure 46: Digital overflow. The image on the left corresponds to ADC0 and the image on the right corresponds to ADC1.

We will fix this in two ways. First, we will further reduce the analog gain of the stages. Second, we will add to the next version of the prototype a digital overflow detection block that will sense over (or under) flow and pin the output code at a high or low level, respectively. It will do that by looking at the sign bit of the running sum one stage prior to the last. Then the algorithm will know whether to pin to a high or low value.

## 6 Production Testing

A Production Test Site is currently being assembled at the University of Florida to perform QC of all the packaged ColdADC ASIC. The production QC procedure was developed and tested on the first 33 packaged chips at BNL. In this section, we describe the production test system and the results from the first 33 chips.

### 6.1 Test Setup

The ColdADC QC teststand is a dedicated system to characterize the ColdADC performance with a low distortion signal generator SRS DS360, which is very similar to the test setup described in Section 2.2. Shown in Figure 47 is the block diagram of the setup. The testboard has an ASIC socket mezzanine card to avoid having to solder the ColdADC chips. This convenience, however, introduces additional capacitance from the ASIC socket which may slightly degrade the test results. Since the main purpose of the production testing is to distinguish good chips from bad chips, the performance degradation from the additional capacitance is not an issue. Instead of an on-board oscillator to provide 100MHz clock for FPGA Mezzanine, an external clock source SRS CG635 is used to provide a stable clock for both room temperature and liquid nitrogen operations. For ENOB/FFT measurements, clock synchronization between the board and the signal generator is required. Without an external clock source it can be difficult to obtain a stable synchronization between the testboard and the signal generator. Figure 48 shows the test setup at room temperature.

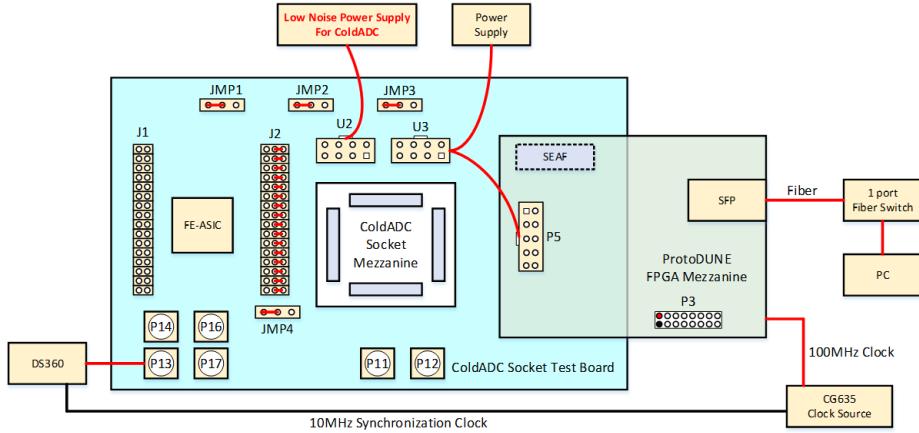


Figure 47: Block diagram of ColdADC Production Testing setup.

The flowchart of the QC process is shown Figure 49. The chart illustrates the sequence of steps for characterizing the functionality and performance of the chip. At every iteration, the measurements are done using BJT reference and then repeated again using the CMOS reference. The list below describes the QC steps in more detail:

1. Input configuration: ColdADC chip ID and test board ID are recorded, the path for data storage is specified.
2. Initialization checkout: mainly to check ColdADC functionality. It includes power consumption with different configurations, power cycles, I2C/UART communication check, pattern and register check, reference sweeping check, synchronization and calibration check. Any chip failed in any procedure in this checkout is treated as a bad chip.
3. Static linearity: INL/DNL results are obtained with a sine wave input from the DS360 generator. Data and plots are generated with the sine wave code-density method. Performances at both 2 MS/s/ch and 500 kS/s/ch are measured.
4. Dynamic Behavior: ENOB/SFDR/SINAD is calculated from the FFT plot obtained by using coherent sampling. Performances at both 2 MS/s/ch and 500 kS/s/ch are measured.

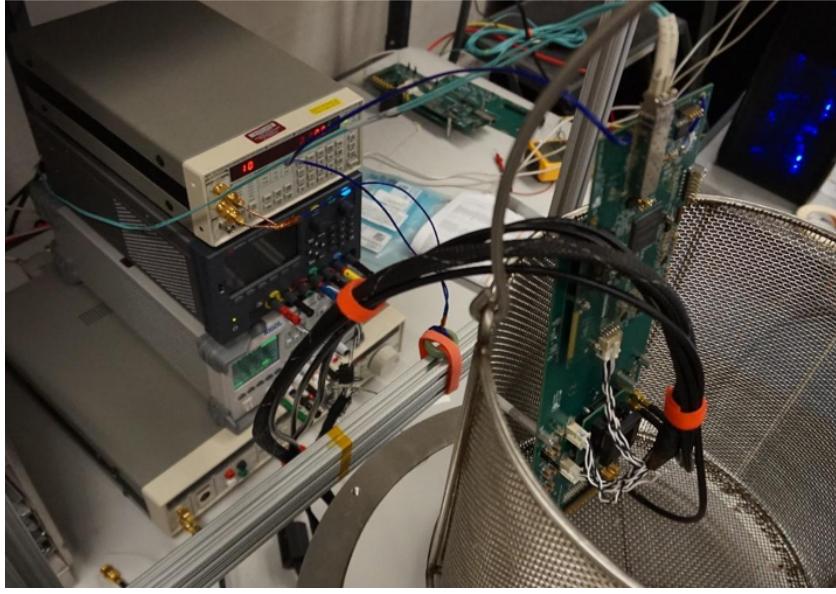


Figure 48: ColdADC QC test setup at room temperature.

5. DC noise: Two DC points, 200mV and 900mV are chosen.
6. ADC core characterization (optional): DNL/INL, FFT, and DC noise.

The test procedure is largely automated using Python scripts. The only step that requires manual intervention is to replace the ASIC chips at the end of the measurement. When the test is completed, the Python script automatically generates a detailed report in pdf format. The report includes:

1. Summary: date and time, temperature, chip and board IDs, power consumption and characterization results (CMOS reference only, can be changed to BJT);
2. Initialization checkout: ADC power consumption with both BJT and CMOS references, sweep plots of reference voltages and currents;
3. Calibration weights: recorded weights listed with respect to internal ADC stages;
4. Noise study: RMS noise for each channel and comparison between all channels. Four pages in total: 200 mV and 900 mV baselines for both BJT and CMOS references;
5. Channels characterization: noise, linearity and dynamic studies, with both BJT and CMOS references for comparison. Each page collects results for one channel;
6. ADC test input: internal ADC characterization for two sampling rates, 4 MS/s and 16 MS/s.

At the moment, the test data are stored in a local database at BNL. U. of Florida group is developing an online database for the ColdADC QC test that will be used for all future production tests. A sample of the QC test report can be found at [2].

## 6.2 Results

For the initial production QC test, a batch of 33 ColdADCs were tested. One of the chips (#00096) drew very high current ( $>1$  A) when it was first powered and was excluded from further QC testing. It was found that the bad chip had a resistance of  $< 5\Omega$  between VDDA2P5 and VSSA2P5, while the nominal resistance should be about 12 k $\Omega$ . The cause of the failure is not clear; may be due to manufacturing defect or handling issues. In addition to the 33 QC chips, 20 other chips were previously tested at BNL and passed functionality tests. Based on a sample of 53 chips (51 packaged and 2 bare dies), the functionality failure rate of ColdADC is less than 2%.

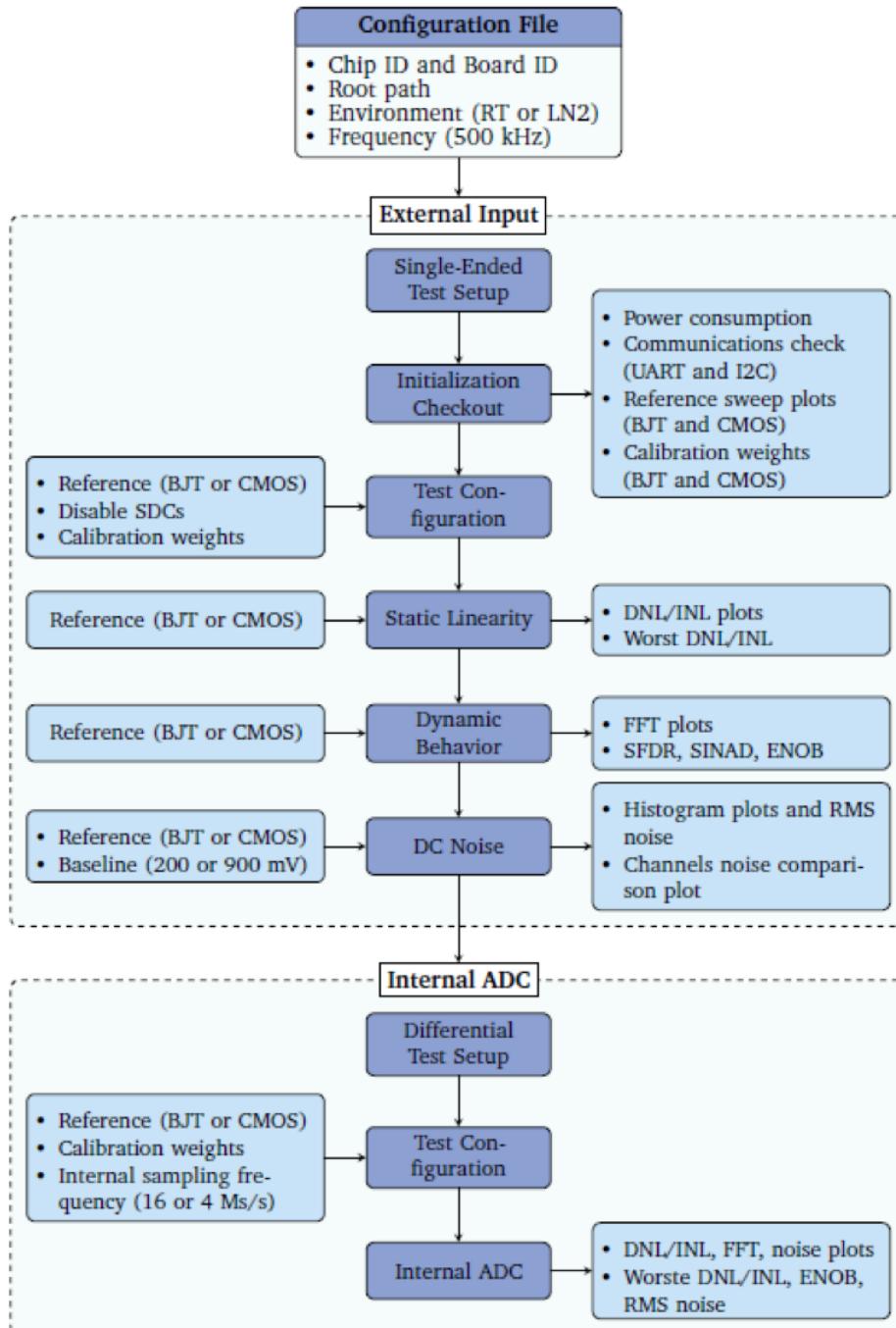


Figure 49: ColdADC QC Flowchart.

### 6.2.1 Power Consumption

The power consumption of ColdADC strongly depends on the chip configuration. The power consumption with VDDA2P5/VDDD2P5=2.5V, VDDD1P2=2.1V, VDDIO=2.25V, SDC&DB bypassed, CMOS reference, floating single-end input, and 2 MS/s sampling rate is summarized in in Figure 50. For this configuration, the average power consumption of ColdADC is about 413 mW at room and 450 mW at LN<sub>2</sub> temperature.

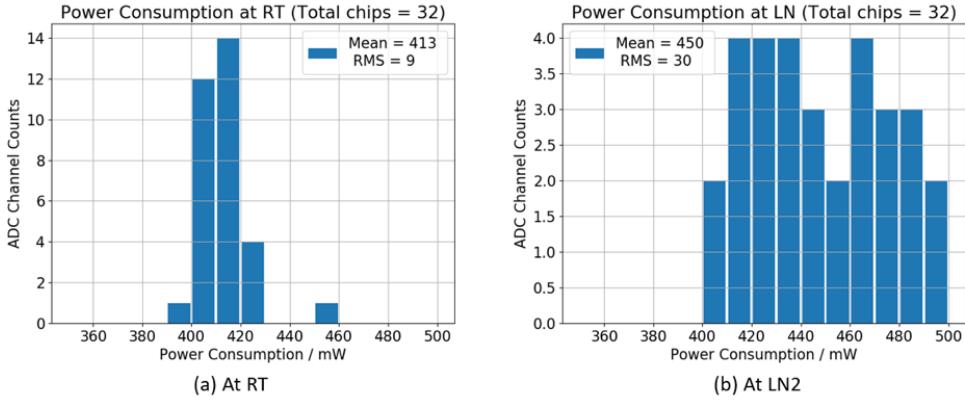


Figure 50: Power consumption distribution.

### 6.2.2 Linearity Results with 2 Ms/s/channel Sampling Rate

The results of the linearity and noise measurements at the nominal 2 Ms/s/channel sampling rate for the 32 chips are shown in Figures 51 (RT) and Figure 52 (LN<sub>2</sub>). Overall, the ColdADC performance is reasonably good, average of the worst DNL is 0.76 LSB, average of the worst INL is 2.6 LSB, average of ENOB is 10.0 bit and average of DC noise at 900mV is 0.68vLSB. In addition, the spread of these 4 key parameters among channels (or chips) is small. Cryogenic test is performed as well with the same configuration, Figure 7 shows the statistical result. By comparing Figure 6 and Figure 7, the linearity performance of DNL, INL and ENOB do not show significant temperature dependence but the DC noise at LN<sub>2</sub> is smaller than at RT due to the suppression of thermal noise at cryogenic temperature. The linearity results shown here are slightly worse than the ones shown in Section 4 due to the known SHA/MUX crosstalk issue. For the QC tests, all 16 input channels are simultaneously connected to the signal source.

### 6.2.3 Linearity Results with 0.5 Ms/s/channel Sampling Rate

The SHA/MUX crosstalk issue mentioned in the earlier section is expected to be fixed in the next revision of the ColdADC. For now we can estimate the optimized performance without the crosstalk issue by repeating the QC measurements with a slower sampling rate and still pulse all 16 channels simultaneously. Results at the sampling rate of 0.5 Ms/s per channel are shown in Figures 53 (RT) and Figure 54 (LN<sub>2</sub>). Compared to the result of 2MS/s per channel, the linearity is significantly better. Average of the worst INL/DNL is less than 1 LSB. Average of ENOB is nearly 11 bits at LN<sub>2</sub>. DC noise at room temperature is improved but no significant difference is observed at LN<sub>2</sub>.

## 7 Summary

We presented the preliminary performance of the ColdADC in this document. The performance for this first prototype has already exceeded the previous cold ADC design that are in use at ProtoDUNE and other LAr experiments. The noise is very low which enables the possibility of outputting 14-bit ADC code instead of the required 12-bit. The linearity is reasonable, but below the expectation from simulation. There were also a number of other issues identified during the testing program . A series of detailed studies have pin-point the areas of the ASIC that could be optimized to achieve the ultimate performance. Work in underway on the design of the second version of the ColdADC to address them.

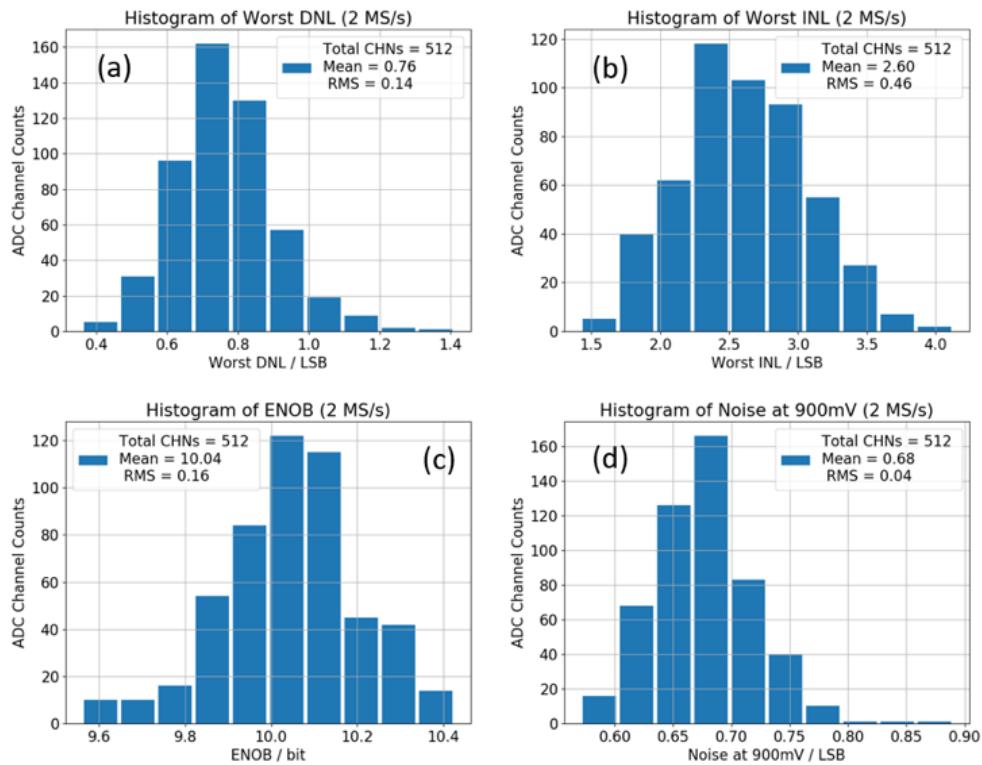


Figure 51: ColdADC QC Results at RT with 2 MS/s per channel sampling rate. ADC output is truncated to 12-bit.

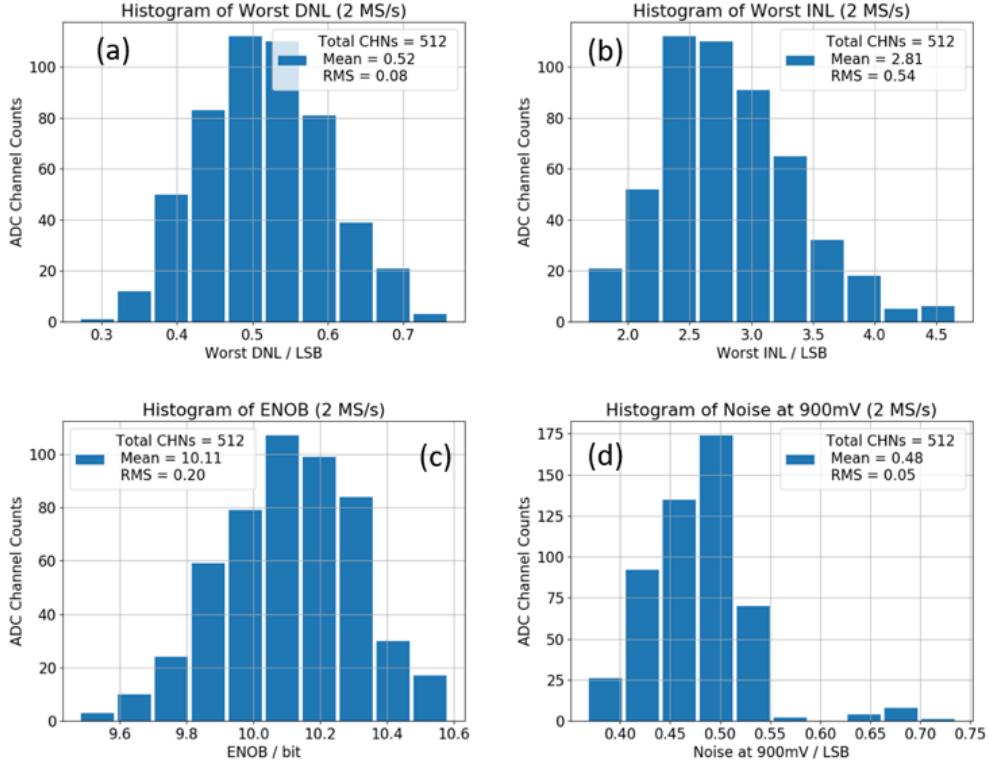


Figure 52: ColdADC QC Results at LN<sub>2</sub> temperature with 2 MS/s per channel sampling rate. ADC output is truncated to 12-bit.

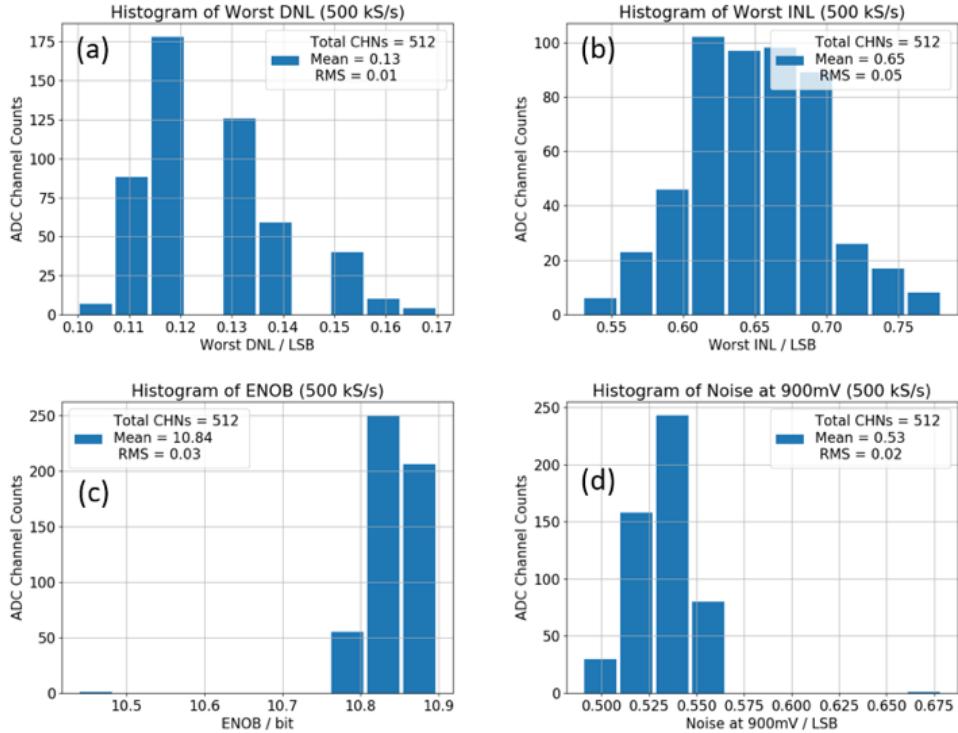


Figure 53: ColdADC QC Results at RT with 0.5 MS/s per channel sampling rate. ADC output is truncated to 12-bit.

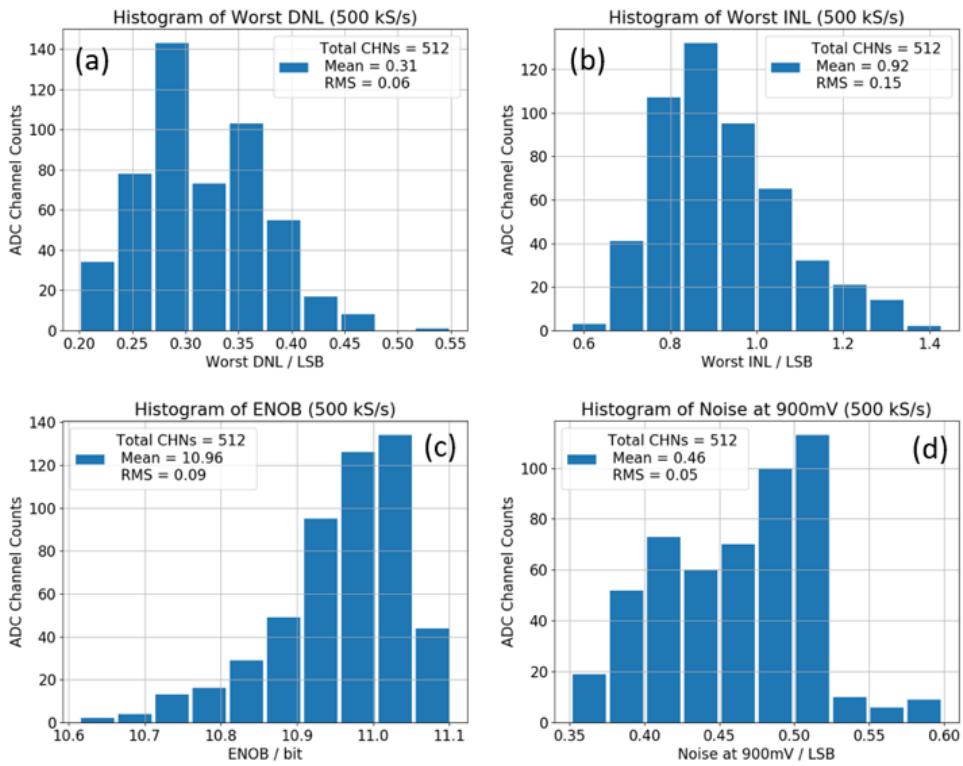


Figure 54: ColdADC QC Results at  $\text{LN}_2$  temperature with 0.5 MS/s per channel sampling rate. ADC output is truncated to 12-bit.

## References

- [1] "LBNF/DUNE Conceptual Design Report", <https://web.fnal.gov/project/LBNF/ReviewsAndAssessments/LBNF-DUNE%20CD-1-Refresh%20Directors%20Review/SitePages/Conceptual%20Design%20Report.aspx>
- [2] [https://brookhavenlab-my.sharepoint.com/:b/g/personal/sgao\\_bnl\\_gov/EVx\\_pSShd3F0tkym9sWL9xsBMKtv98etz8IlxkfAzDToqQ?e=YB51td](https://brookhavenlab-my.sharepoint.com/:b/g/personal/sgao_bnl_gov/EVx_pSShd3F0tkym9sWL9xsBMKtv98etz8IlxkfAzDToqQ?e=YB51td)

## 8 Appendix

Figure 55 shows the ENC project vs. detector wire length for MicroBooNE, ProtoDUNE, and SBND cold electronics.

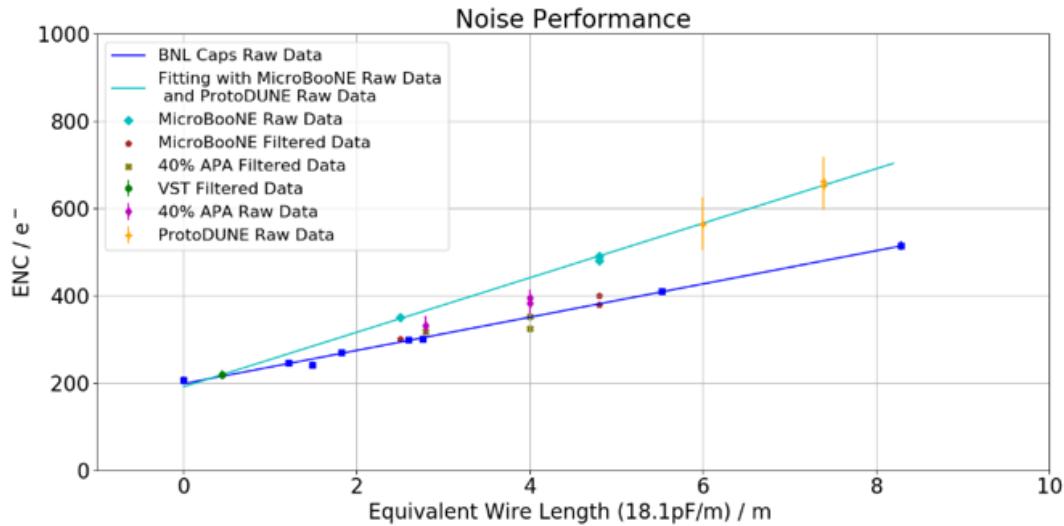


Figure 55: ENC project with MicroBooNE, ProtoDUNE, and SBND cold electronics at cryogenic temperature.