DUNE ColdADC ASIC Preliminary Testing Results

Authors go here

January 13, 2020

DUNE Electronics Consortium

Abstract

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1 Introduction [Grace/Lin]

Note to authors: executive summary of the testing plan and status. Include specs table.

The DUNE ColdADC is a digitizer ASIC intended for operation in the Deep Underground Neutrino Experiment (DUNE) Far Detectors. It will operated immersed in Liquid Argon (LAr) and will need to operate reliably, without any servicing or component replacement, for over 30 years at a temperature of approximately 88 K.

The ColdADC was implemented in 65 nm CMOS by a team comprised of engineers from Fermilab (FNAL), Brookhaven National Laboratory (BNL), and Lawrence Berkeley National Laboratory (LBNL). The prototype was submitted for fabrication in late 2018 and received in early 2019. Evaluation is ongoing.

The first prototype meets essential requirements (except suitability for long-term reliable operation at 88 K). The key performance specification, noise, is as expected. The prototype is currently being integrated into a new revision of the DUNE Far Detector Front-End Mother Board (FEMB). Preliminary results are good, and the DUNE Far Detector FEMB is displaying better noise performance than the SBND FEMB, which uses a Commercial Off-the-Shelf (COTS) ADC. This enables the use of a lower gain setting in LArASIC.

The key specifications of the ColdADC compared to the measured results are presented in Table 1.

Specification	Value	Result	Note
Operation Temperature	RT and 88 K	Success	
Sampling Rate	2 MHz	2 MHz	
Noise	200 μV-rms	202 μV-rms	At 88 K
Differential Nonlinearity (DNL)	0.5 LSB (at 12-bit level)	$0.18/-0.5$ LSB	At 2 MHz and 88 K, worst case across channels
Integral Nonlinearity (INL)	1 LSB (at 12-bit level)	$1.56/-1.8$ LSB	At 2 MHz and 88 K, worst case across channels
Effective-Number-of-Bits (ENOB)	11.0 bits		At 2 MHz and 88 K
No Missing Codes Across Dynamic Range	N/A	Success	
Crosstalk	No Specification	$< 1\%$	
Power Dissipation	No Specification	420 mW	290 K

Table 1: Summary of Results

2 Test Setup

2.1 Cryogenic Test System (CTS) [Lin]

2.2 BNL Test System [Gao]

Describe BNL test setup including the test boards.

2.3 Fermilab Cryo Cooler Test System [Christian]

Describe Fermilab test setup including the test boards.

2.4 LBNL Test Board [Lin]

3 Functional Testing [Christian]

Note to author: Discuss functional testing including reading/writing registers with I2C and UART, verifying the data I/O, including LVDS current control, and verifying clock generation.

4 Performance Results

Note to authors: discuss in this section the high level performance results. The main message here is to convey to the readers that the ASIC functions well overall. The details of the known issues will be discussed in the next section.

4.1 Noise

4.1.1 ColdADC Only

4.1.2 LArASIC + ColdADC [Gao]

4.2 Static Linearity (INL,DNL)

4.3 Dynamic Linearity (ENOB, SNDR)

4.4 Channel Crosstalk [Gao]

4.5 Power Consumption [Gao]

5 Issues Identified and Mitigations

Note to authors: describe studies that have been done to identify the issues and possible mitigations.

5.1 Auto Calibration [Grace]

The linearity of the ADC is primarily determined by the capacitor matching internal to the circuit, and to a lesser extent the performance of the internal amplifiers. To achieve the target specifications, the ADC requires calibration. The calibration in Cold ADC can be carried out internal, in a fully automated way, or can be done externally. Unfortunately, while the chip could be fully calibrated externally, with calibration data loaded back onto the chip, the autocal function failed in the prototype. The ADC performance under autocal or external calibration does not differ in any way, so the main issue here is the loss of convenience that autocal promises.

When we developed the digital part of the Cold ADC, we decided to partition the blocks such that the blocks calibrate the ADC and compute the corrected digital output would be placed within the ADC cores, and the rest of the digital logic would be aggregated in a third core. This can be seen in Figure 1. The CAL_UNIT is the block that performs the calibration and also applies the calibration coefficients (or weights) to the data during normal operation. Each CAL_UNIT stores the calculated configuration weights to the register file in the CAL_CORE (which was synthesized separately).

This would have been an acceptable strategy but due to miscommunication the interface between the cores was not simulated with back-annotated timing. This means that the timing when a computed calibration coefficient is written back into the registers was not simulated properly. When the blocks were placed, there was a timing error between the CAL_UNIT and the CAL_CORE in the case when the CAL_UNIT was writing back computed calibration weights into storage in the CAL_CORE.

An example of the intended operation is shown in Figure 2. In this simulation the CAL_UNIT is back annotated with parasitics (but the interface with the CAL_CORE is not properly back annotated). In this simulation, the intended data is in the second row (the word 0x03FD) and is written to the w2_4 registerthat resides in the CAL_CORE correctly. Correct operation is assured by disabling the memory after the edge of clk.

When the interface between CAL_UNIT and CAL_CORE was properly annotated and simulated, the result was in Figure 3.

A gross error has been made, because the write signal is released too soon and therefore we have a race condition. What happens specifically here is that due to the race condition, the LSB byte of w0[4] is overwritten with the LSB byte of w2[4]. This is error and causes the entire calibration sequence to fail.

The fix here is to repartition the digital logic for the second version of the Cold ADC ASIC. We will move the digital calibration and correction logic out of the ADCs and into a single, monolithic digital block. This will ensure that the interfaces between the calculation engines and the memory are

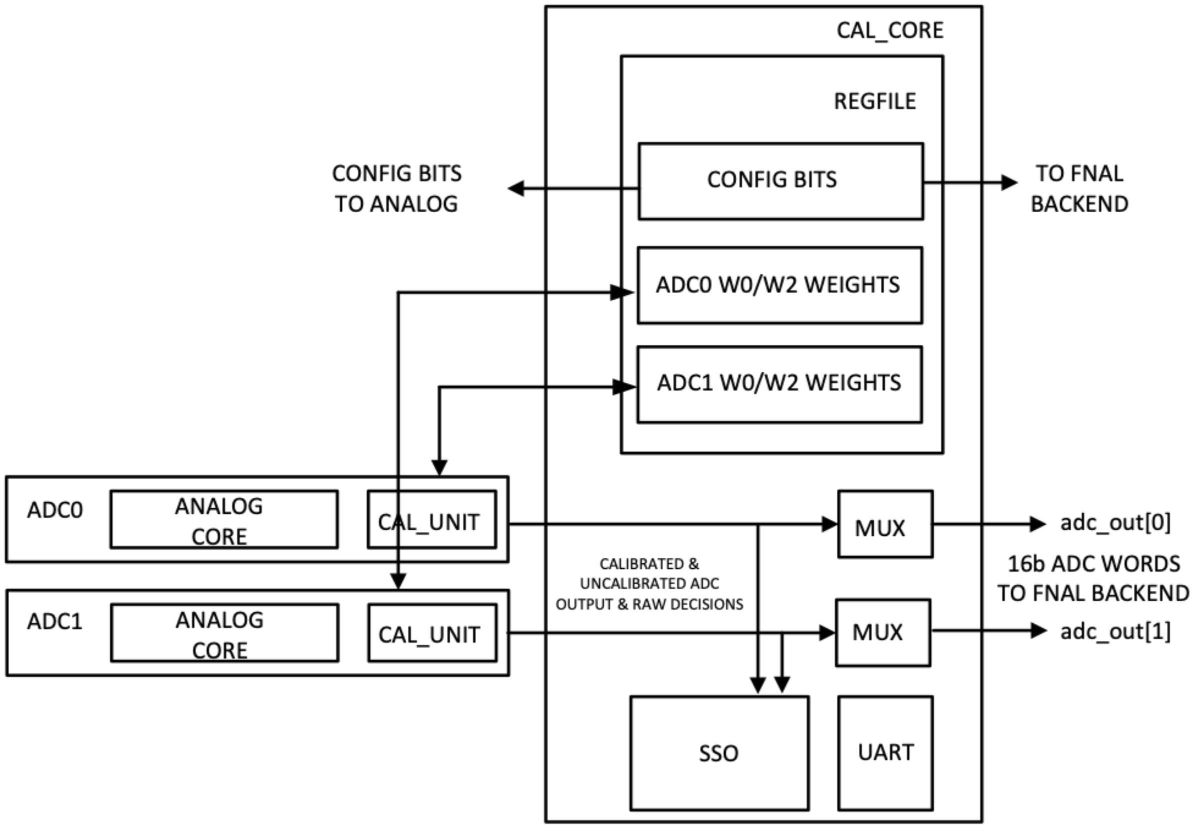

Figure 1: Partitioning of Digital Logic in the ColdADC.

simulated correctly and the absence of race conditions will be verified using static timing analysis. The RTL code itself will also be made more robust by adjusting the internal state machine.

5.2 Level Shifter [Grace]

Because the digital core of the Cold ADC uses 1.2 V rails, but many of the analog circuits on the chip use 2.5 V rails, level shifters are required to translate control settings from the 1.2 V voltage domain to the 2.5 V voltage domain. Unfortunately, due to confusion during the design process, the required level shifters that were required for the front end single-ended-to-differential input buffer were not included. Therefore, in order to configure the block correctly, the 1.2 V digital supply must be elevated. While this allows the chip to be operated successfully, it is not compatible with long-term reliability.

The fix is to include the proper level shifters in the next version of Cold ADC. The fix has already been made in the layout.

5.3 ADC Core Linearity [Prakash]

5.4 SHA/MUX Linearity [Prakash]

5.5 SDC Linearity [Dabrowski]

5.6 IR Drop * [Christian/Miryala]

5.7 SHA/MUX Crosstalk [Grace/Prakash/Lin]

While there is no formal specification regarding the channel crosstalk, we have measured crosstalk of approximately 1%. We have done a variety of measurements that suggest the crosstalk is due to kickback between the channels during the sampling phase that makes it so the SHAs are not completely

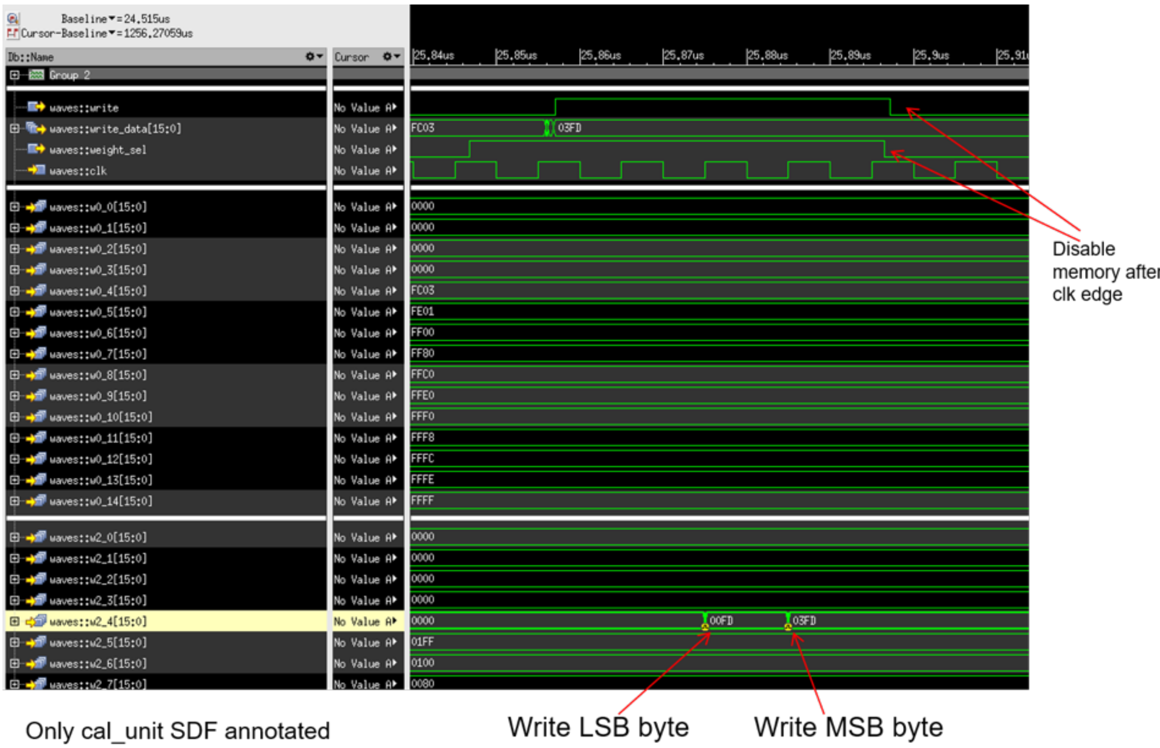

Figure 2: Correct writeback of calibration weights

settled between samples. When the channels are slowed down, the crosstalk is somewhat mitigated, which indicates that it is due to insufficient bandwidth in the SHA Mux. To improve this, we will lower the impedance of the Mux to allow faster settling.

5.8 BGR Op-amp [Dabrowski]

5.9 Overflow Wraparound [Grace]

The gains of each stage are weighted by the calibration. If the sum of the weights of the stages is greater than 2^{16}, then the digital correction logic can overflow, and a large input can lead to a small output code and vice versa. The stages were designed with an analog closed-loop gain slightly less than two. Based on supplied process data, we expected the closed-loop gain would be low enough to be free from overflow. In fact this was not the case and overflow was observed when the input voltage was close to one of the reference voltages. This can be seen in Figure 4, which shows the response of the two different ADCs on one of the Cold ADC prototypes to the same input signal. The One the left portion of Figure 4 shows the ramp response of ADC0 and the prototype operates as expected. When the ADC is saturated, the digital output is pinned to its maximum value. On the right portion of Figure 4 overflow is observed as part of the ramp response of ADC1. In this case, the ADC input reaches its maximum value but instead of remaining pinned, the digital output jumps to a low value. This is due to higher-than-expected closed-loop gain in ADC1.

We will fix this in two ways. First, we will further reduce the analog gain of the stages. Second, we will add to the next version of the prototype a digital overflow detection block that will sense over (or under) flow and pin the output code at a high or low level, respectively. It will do that by looking at the sign bit of the running sum one stage prior to the last. Then the algorithm will know whether to pin to a high or low value.

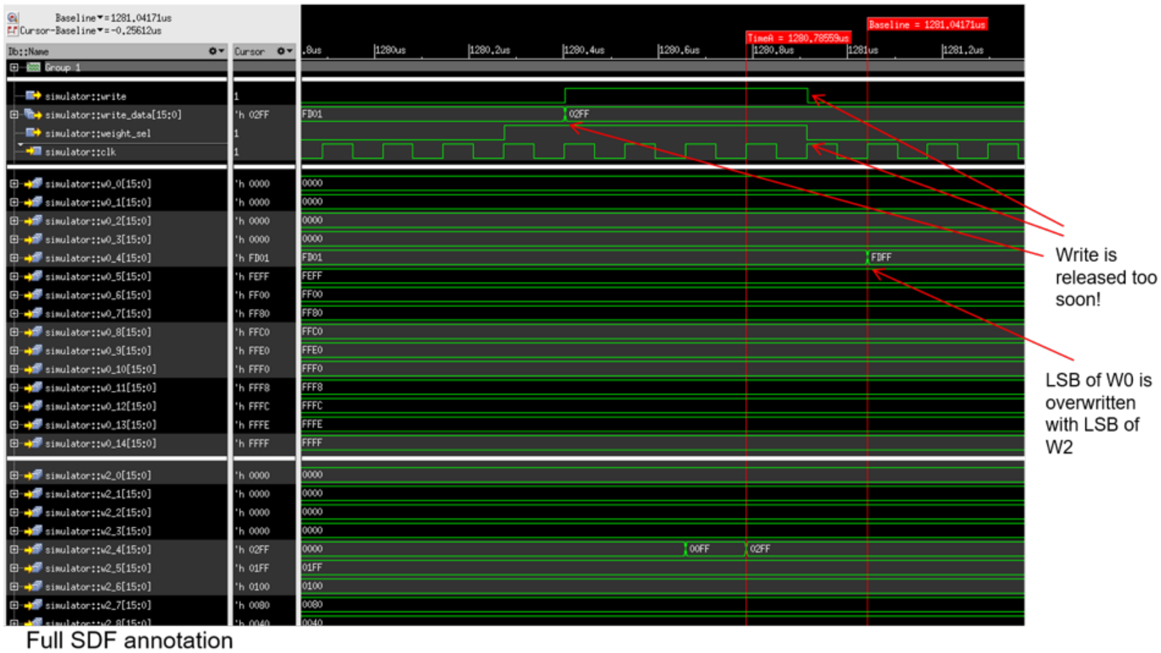

Figure 3: Error in writeback of calibration weights

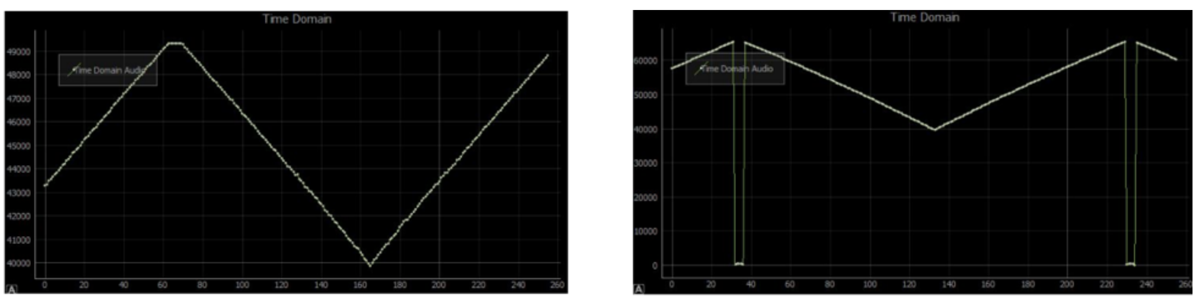

Figure 4: Digital overflow. The image on the left corresponds to ADC0 and the image on the right corresponds to ADC1.

6 Production Testing [Furic/Gao]

6.1 Test Setup

6.2 Results

7 Summary

References

[1] "LBNF/DUNE Conceptual Design Report", https://web.fnal.gov/project/LBNF/ReviewsAndAssessments/LBNF-DUNE%20CD-1-Refresh%20Directors%20Review/SitePages/Conceptual%20Design%20Report.aspx

[2] First scientific application of the membrane cryostat technology, D.Montanari et al, *AIP Proceedings 1573, 1664 (2014)* http://scitation.aip.org/content/aip/proceeding/aipcp/10.1063/1.4860907

[3] "The GENIE Neutrino Monte Carlo Generator", C. Andreopoulos, et al., Nucl. Instrum. Meth. A614, 87 (2010).

Appendix

Example for citing references. References [1–3] should be entered in bibliography.tex file under your section.

```
Example for citing references. References~\cite{dunecdr,montanari_35ton,genie}.
```

Here is an example of how to insert Fig. 5. Figures should be saved in ./figures directory.

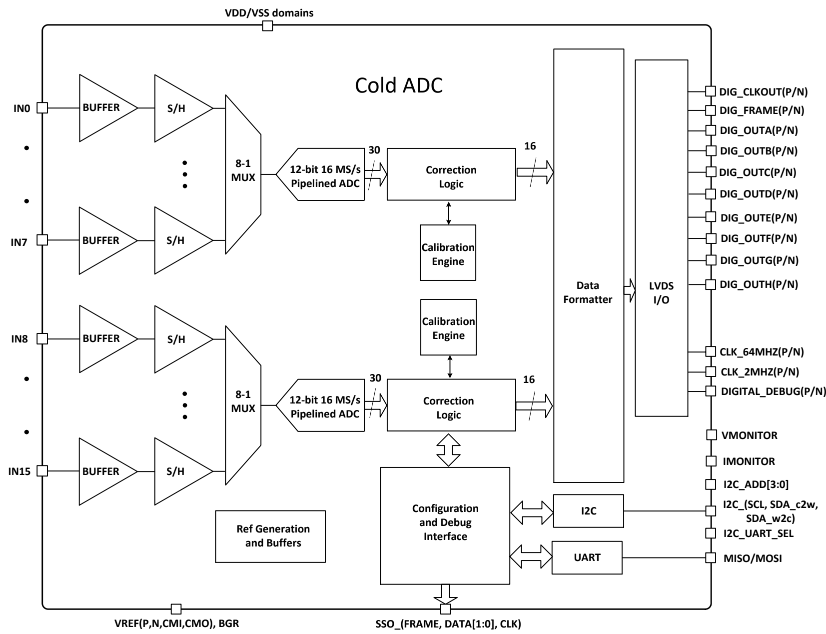

Figure 5: ColdADC Block Diagram.

```
\begin{figure}[htb]
\centering
\begin{center}
\includegraphics[width=0.7\textwidth]{figures/coldadc_blockdiagram.pdf}
\end{center}
\caption{ColdADC Block Diagram.}
\label{fig:adc_blockdiagram}
\end{figure}
```

Here is an example of how to create Table 2.

Component	dimensions [m]
APA (active)	$2.29(wide) \times 5.9(high)$
APA (external)	$2.32(wide) \times 6.2(high)$
TPC (active)	$7.0(long) \times 7.2(wide) \times 5.9(high)$
TPC (external)	$7.3(long) \times 7.4(wide) \times 6.2(high)$
cryostat (internal)	$8.9(long) \times 7.8(wide) \times 8.1(high)$

Table 2: Dimensions of DUNE-PT.

```
\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
\textbf{ Component } & dimensions [m]  \\ \hline \hline
APA  (active) &  $2.29 (wide) \times 5.9 (high)$ \\ \hline
APA  (external) &  $2.32 (wide) \times 6.2 (high)$ \\ \hline
TPC (active)       & $7.0 (long) \times 7.2 (wide) \times 5.9 (high)$  \\ \hline
TPC (external)       & $7.3 (long) \times 7.4 (wide) \times 6.2 (high)$  \\ \hline
cryostat (internal) &  $8.9 (long) \times 7.8 (wide) \times 8.1 (high)$  \\ \hline
\end{tabular}
\caption{Dimensions of DUNE-PT.}
\label{tab:TPC-dim}
\end{table}
```