DUNE ColdADC ASIC Preliminary Testing Results

Authors go here

January 16, 2020

DUNE Electronics Consortium

Abstract

The DUNE ColdADC is a 16-channel low-noise ADC ASIC designed to read out the LArASIC preamps in the DUNE Liquid Argon Far Detectors. The resolution of the ADC is 12-bits and it digitizes at a rate of 2MS/s/channel. The ADC accepts single-ended or differential inputs and outputs a serial data stream to COLDATA, the DUNE digital data aggregator/serializer chip.

In this document, we present the preliminary performance studies on the first version of the ColdADC ASIC. The prototype ColdADC has already achieved a performance that essentially met the DUNE requirements. We will discuss some of the issues found during the functional tests and the plan to mitigate them in the next revision of the ASIC.

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1 Introduction [Grace/Lin]

The DUNE ColdADC is a digitizer ASIC intended for operation in the Deep Underground Neutrino Experiment (DUNE) Far Detectors. It will operated immersed in Liquid Argon (LAr) and will need to operate reliably, without any servicing or component replacement, for over 30 years at a temperature of 88 K.

The ColdADC was implemented in 65 nm CMOS by a team comprised of engineers from Fermilab (FNAL), Brookhaven National Laboratory (BNL), and Lawrence Berkeley National Laboratory (LBNL). The prototype was submitted for fabrication in late 2018 and received in early 2019. Evaluation is ongoing.

The first prototype meets essential requirements. The key performance specification, noise, is as expected. The prototype is currently being integrated into a new revision of the DUNE Far Detector Front-End Mother Board (FEMB). Preliminary results are good, and the DUNE Far Detector FEMB is displaying better noise performance than the SBND FEMB, which uses a Commercial Off-the-Shelf (COTS) ADC. This enables the use of a lower gain setting in LArASIC and thus larger dynamic range. The key specifications of the ColdADC compared to the measured results are presented in Table 1.

Specification	**Value**	**Result**	**Note**
Operation Temperature	Room Temp. (RT) and 88 K	Success	
Sampling Rate	2 MHz	2 MHz	
Noise	200 μV-rms	189 μV-rms	@ LN_2 temp
Differential Non-linearity (DNL)	$\pm$0.5 LSB (at 12-bit level)	+0.2 to $-$0.5 LSB	@LN_2 ; typical values
Integral Non-Linearity (INL)	$\pm$1 LSB (at 12-bit level)	+1.2 to $-$1.1 LSB	@LN_2, typical values
Effective-Number-of-Bits (ENOB)	11.0 bits	<mean>=10.6 bits rms=0.3 bits	@ LN_2
No Missing Codes Across Dynamic Range	N/A	Success	@LN_2 and RT
Crosstalk	No Specification	$< 1\%$	
Power Consumption	<50 mW/channel(??)	24 mW/channel	

Table 1: Summary of Results

In order to mitigate the hot carrier effect (and ensure long operational lifetime at 88 K), the circuits in the ColdADC prototype are designed with a minimum transistor channel length 50% longer than the minimum length allowed by the process, and the power supplies are kept at 10% below their nominal values. To follow this rule, the synthesized digital circuits use a custom standard cell library with longer transistors than the foundry-supplied library. In addition, the architecture of the ADC was chosen as the Pipelined ADC, whose performance depends primarily on the matching of ratioed capacitors. Studies conducted by BNL showed capacitor performance degraded less than active devices under cold conditions.

2 Test Setup

The first prototype of the ColdADC ASIC has been undergoing evaluation at BNL, FNAL and LBNL since early 2019. In addition to validating the portion of the ASIC that they designed, the three labs also worked collaboratively to cross-check the key performance results and debug issues. In this section, we will describe the setup used for testing the ColdADC.

2.1 Cryogenic Test System (CTS) [Lin]

One of the cryogenic equipments used in ColdADC testing is the Cryogenic Test System (CTS), shown in Figure 1. The CTS is a cryogenic test chamber mounted on top of a commerical LN_2 dewar. The device-under-test (e.g. ColdADC chip) can be mounted inside the test chamber and immersed in LN_2.

The CTS can also circulate either cold or warm gas to slowly cool down or warm up the ASIC before and after testing. The CTS has been effective at minimizing water condensation on the ASIC from thermal cycling. Multiple CTS units were built by a group from Michigan State University and distributed to the various testing sites.

Figure 1: Cryogenic Test System.

2.2 BNL Test System [Gao]

Describe BNL test setup including the test boards.

2.3 Fermilab Cryocooler Test System [Christian]

The Fermilab Cryocooler Test System consists of a vacuum vessel and a cryogenic refrigerator. The cryogenic refrigerator is a Cryomech PT-60. It is a closed-loop cryocooler consisting of a helium compressor (located next to the vacuum vessel) and a cold head (located on top of the vacuum vessel). The cryocooler cools a copper cold-plate inside the vacuum vessel to a minimum of 60 K. A 100 ohm platinum RTD and a 75 Watt heater are mounted on the cold-plate. A temperature controller cycles the heater on and off to achieve the set-point temperature. Any temperature between 60 and 250 K can be set. The vacuum vessel has 2 large penetrations and 12 small penetrations that can be used in device testing. Typically, one of the large penetrations is used as an inspection port and the other as a feedthrough for ribbon cables. The small ports allow for a variety of other signal feedthroughs.

Two printed circuit boards are used in ASIC testing, a "cold board," which is screwed onto the cold-plate and includes a large unmasked copper thermal contact area, and a "warm board" which is mounted as a mezzanine board on the cold-board. RTDs are placed on both the cold board and the warm board. The temperature on the warm board is typically 100 K higher than than the temperature on the cold board. If the cryocooler is regulated to hold the cold-board at LN_2 temperature, then the

Figure 2: Fermilab Cryocooler Test System.

temperature on the warm board is $\sim -96°C$, which is warm enough for most COTS components to operate properly.

The cold board used in tests of COLDADC includes a single bare chip, wire bonded to the printed circuit board. An 80-pin header carries digital I/O and three of the four bias voltages (VDDIO and both digital voltages) between the cold board and the warm board. A 60 pin header carries the analog bias voltage and all analog signals with the exception of the analog inputs to the COLDADC. Jumpers allow the analog inputs to be grounded or connected to an external sources using cables. The only other parts on the cold board are bypass capacitors (selected for cryogenic use) and test points.

The warm board includes connectors that mate to the cold board connectors, a 52-pin header used for a cable connection to an National Instruments (NI) FPGA module, single ended to differential converters used for the 64 and 2 MHz clock signals, differential to single ended converters for the LVDS output signals, level shifters for the CMOS I/O signals, passive components, buffer amplifiers, and SMA connectors for the analog outputs, SMA connectors for the ADC test inputs, and 9-pin D connectors for cable connections to NI power supplies that provide source-measure functionality (used for chip power and for providing or measuring analog I/O signals such as reference voltages).

Test software was written using National Instruments LabView and run on a single-crate PXIe system consisting of a controller, an NI 6583 FPGA unit, and 5 power supply modules. A Keysight 33500B waveform generator was used to provide input signals. Analog measurements were made using an oscilloscope and a DVM as well as with the NI modules.

2.4 LBNL Test Board [Lin]

3 Functional Testing [Christian]

COLDADC is highly programmable. Many circuit blocks can be bypassed and two versions of a number of circuit blocks are included to mitigate the risk that one might fail. Testing at Fermilab concentrated on verifying the functionality of all of the circuit blocks. Three design errors were revealed and a number of documentation errors were corrected. The table below summarizes the tests.

Test/Circuit	Result
Power on	No shorts
I2C	Works as designed (registers can be written and read)
Reset	Works as designed (registers are set to default values)
UART	Works as designed
LVDS I/O	Works as designed (output amplitude controlled as designed)
Clock Generation	16 MHz clock verified
Data Formatter	Works as designed
Band Gap Reference	Works ∼as designed at room temperature, but fails when cold. Problem traced to a design error (inclusion of the wrong OP Amp in the current source DAC); works as designed with elevated VDDA2P5 (needs 2.7V at 77K)
CMOS Reference	Works as designed
Automatic Calibration	Fails. Calibration can be done by using control registers to force the sequence of steps required and doing arithmetic off-chip. Eventually we noticed that when automatic calibration is attempted, the low order bytes of W0 and W2 for every "calibrated" stage are equal. Simulation verified that this is due to a timing error storing W0 and W2.
ADC Correction Logic	Works as designed (loaded fake comparator output values; resulting ADC output is as expected).
Pipeline ADC	Linear ramp yields close to linear output; deviation from linear at extremes of ramp; no significant deviation from linear when cold.
Input buffers	Significant non-linearity observed. Problem traced to circuit naming confusion that resulted in level shifters being omitted from input buffers. Buffers operate ∼as designed with elevated VDDD1P2
Sample and Hold and MUX	Require elevated VDDD1P2 because inputs come through input buffers.

Table 2: Functional Testing.

4 Performance Results

The ColdADC is designed with many redundancies to mitigate single point of failure. During functional testing, a number of problems were identified. Forunately, none of the problems prevented the ColdADC from achieving a performance that essentially meet the DUNE requirements. In this section we will show the performance results (already summarized in Table 1) with the ASIC in the nominal configuration, the same configuration that we will use for the system-level integration tests at CERN on APA#7 in the Coldbox and the ICEBERG teststand at Fermilab.

4.1 Noise

4.1.1 ColdADC Only

4.1.2 LArASIC + ColdADC [Gao]

4.2 Static Linearity (INL,DNL)

4.3 Dynamic Linearity (ENOB, SNDR)

4.4 Channel Crosstalk [Gao]

4.5 Power Consumption [Gao]

5 Issues Identified and Mitigations

Note to authors: describe studies that have been done to identify the issues and possible mitigations.

5.1 Auto Calibration [Grace]

The linearity of the ADC is primarily determined by the capacitor matching internal to the circuit, and to a lesser extent the performance of the internal amplifiers. To achieve the target specifications, the ADC requires calibration. The calibration in ColdADC can be carried out internal, in a fully automated way, or can be done externally. Unfortunately, while the chip could be fully calibrated externally, with calibration data loaded back onto the chip, the autocal function failed in the prototype. The ADC performance under autocal or external calibration does not differ in any way, so the main issue here is the loss of convenience that autocal promises.

The cause of the auto calibration issue is understood and is mainly due to a miscommunication between ASIC designers. When we developed the digital part of the ColdADC, we decided to partition the blocks such that the blocks calibrate the ADC and compute the corrected digital output would be placed within the ADC cores, and the rest of the digital logic would be aggregated in a third core. This can be seen in Figure 3. The CAL_UNIT is the block that performs the calibration and also applies the calibration coefficients (or weights) to the data during normal operation. Each CAL_UNIT stores the calculated configuration weights to the register file in the CAL_CORE (which was synthesized separately).

This would have been an acceptable strategy but due to miscommunication the interface between the cores was not simulated with back-annotated timing. This means that the timing when a computed calibration coefficient is written back into the registers was not simulated properly. When the blocks were placed, there was a timing error between the CAL_UNIT and the CAL_CORE in the case when the CAL_UNIT was writing back computed calibration weights into storage in the CAL_CORE.

An example of the intended operation is shown in Figure 4. In this simulation the CAL_UNIT is back annotated with parasitics (but the interface with the CAL_CORE is not properly back annotated). In this simulation, the intended data is in the second row (the word 0x03FD) and is written to the w2_4 registerthat resides in the CAL_CORE correctly. Correct operation is assured by disabling the memory after the edge of clk.

When the interface between CAL_UNIT and CAL_CORE was properly annotated and simulated, the result was in Figure 5. A gross error has been made, because the write signal is released too soon and therefore we have a race condition. What happens specifically here is that due to the race condition, the LSB byte of w0[4] is overwritten with the LSB byte of w2[4]. This is error and causes the entire calibration sequence to fail.

The fix here is to repartition the digital logic for the second version of the ColdADC ASIC. We will move the digital calibration and correction logic out of the ADCs and into a single, monolithic digital block. This will ensure that the interfaces between the calculation engines and the memory are simulated correctly and the absence of race conditions will be verified using static timing analysis. The RTL code itself will also be made more robust by adjusting the internal state machine.

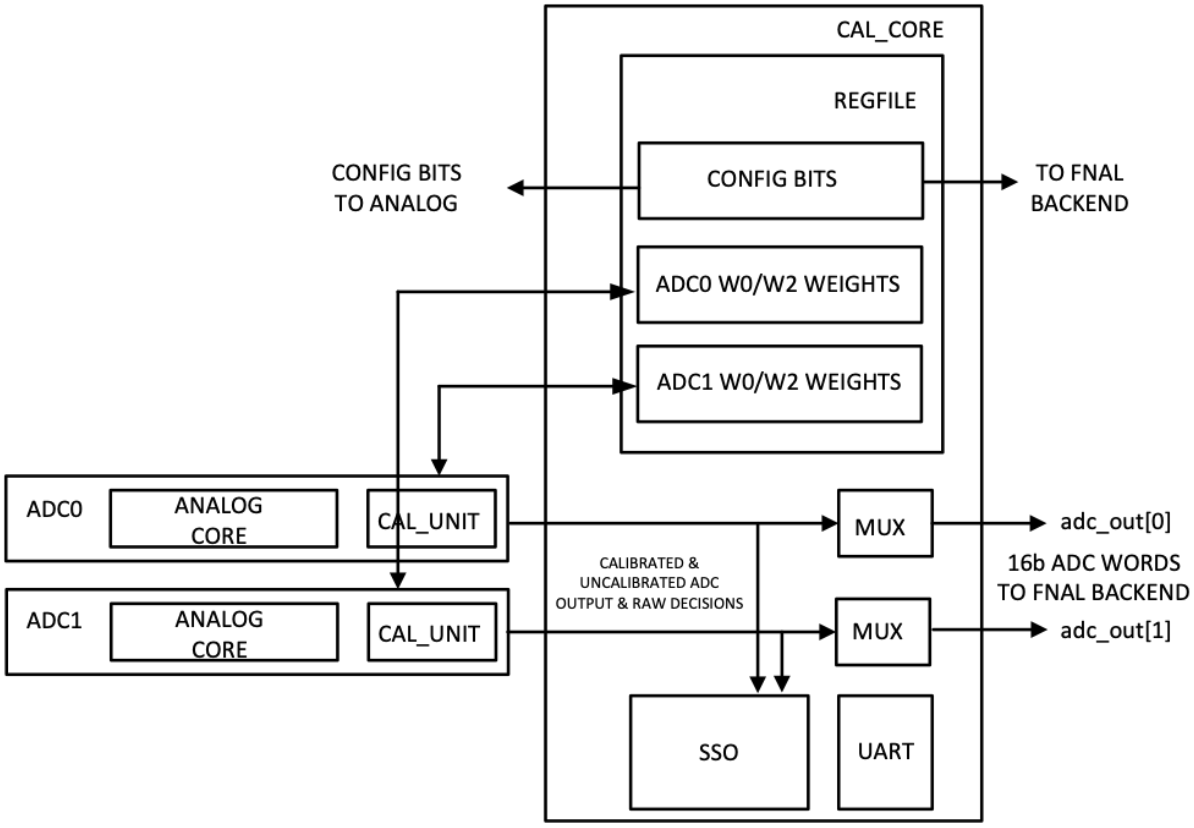

Figure 3: Partitioning of Digital Logic in the ColdADC.

5.2 Level Shifter [Grace]

Because the digital core of the Cold ADC uses 1.2 V rails, but many of the analog circuits on the chip use 2.5 V rails, level shifters are required to translate control settings from the 1.2 V voltage domain to the 2.5 V voltage domain. Unfortunately, due to confusion during the design process, the required level shifters that were required for the front end single-ended-to-differential input buffer were not included. Therefore, in order to configure the block correctly, the 1.2 V digital supply must be elevated. While this allows the chip to be operated successfully, it is not compatible with long-term reliability.

The fix is to include the proper level shifters in the next version of Cold ADC. The fix has already been made in the layout.

5.3 ADC Core Linearity [Prakash]

Measured ADC INL is approximately 1 LSB at 12-bit level, however simulations suggest 0.5 LSB INL is possible. The main drawback is lack of corner models at cold and the the Monte Carlo analysis at warm was insufficient.

The ADC linearity is limited by insufficient op-amp gain in the stages. Since the calibration algorithm can only correct linear gain errors, non-linearity beyond the expectation could and will limit the performance. The op-amp becomes nonlinear as their swing increases because the output resistance of the devices connected to the output decreases when the voltage across them is reduced. The main suspect is the raw open-loop gain is lower than expected and the closed-loop rejection of the non-linearity is not good enough. To verify the large closed-loop gain non-linearity in the stages, references were clamped down and the evidence of op-amps becoming less and less non-linear when we reduce the swing become apparent. Figures 6 through 8 demonstrate this.

Slowing down ADC by 16X and reducing bias currents to increase op-amp gain improves linearity, while increasing bias currents at full speed doesn't help, this is a key evidence to rule out other issues

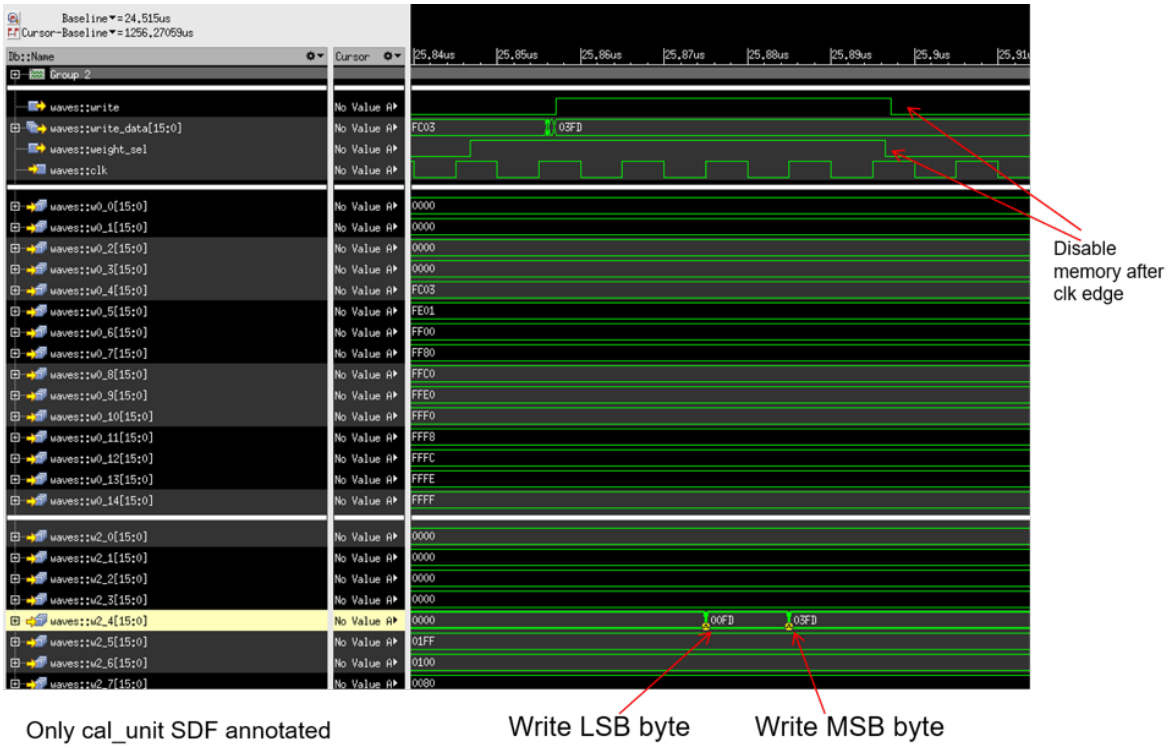

Figure 4: Correct writeback of calibration weights

like settling issues.

The calibration algorithm is linear, and does little to improve performance in presence of non-constant stage gain. Negative feedback rejects non-linearity in the stage via high open-loop gain. In other words, high op-amp gain is needed to keep the stages linear so the calibration algorithm can work.

Each op-amp includes a gain-boosting circuit to increase the open-loop gain. The gain boosting amplifiers increase the op-amp gain by a factor of 5 in simulation.

The gain-boosters can be controlled externally by the configuration bits, figures 10 and 11 show the measured linearity of the ADC with gain-boosters ON and OFF. All the measurements were taken by clocking the ADC at 1MHz (nominal 16MHz) and nominal reference voltages.

Behavioral modeling was performed to verify the open loop gain of the op-amp with gain boosters ON and OFF.

Figures 10, 12 and figures 11, 13 have roughly similar performances. The gain boosters improve the open loop gain by 6 dB instead of 14dB, i.e, the gain boosters are adding 2X gain and not 5X gain as expected.

Analysis indicates not a lot of margin on the gain booster design for biasing. Also, the fact linearity doesn't improve at cold as much as we thought it would, also points to a biasing issue. The op-amp can be improved by centering the gain booster biasing for more margin.

Corner analysis on the op-amp was performed to understand the issues better and the gain booster circuit was modified to improve the overall gain of the op-amp. Figures 14 and 15 show the corner analysis of the op-amp circuit at room temperature.

With the modified gain booster circuit, the overall gain of the op-amp at the FS-corner(worst case) is increased from 67dB to 86dB. Analysis of this fix is being done and will be implemented in the layout.

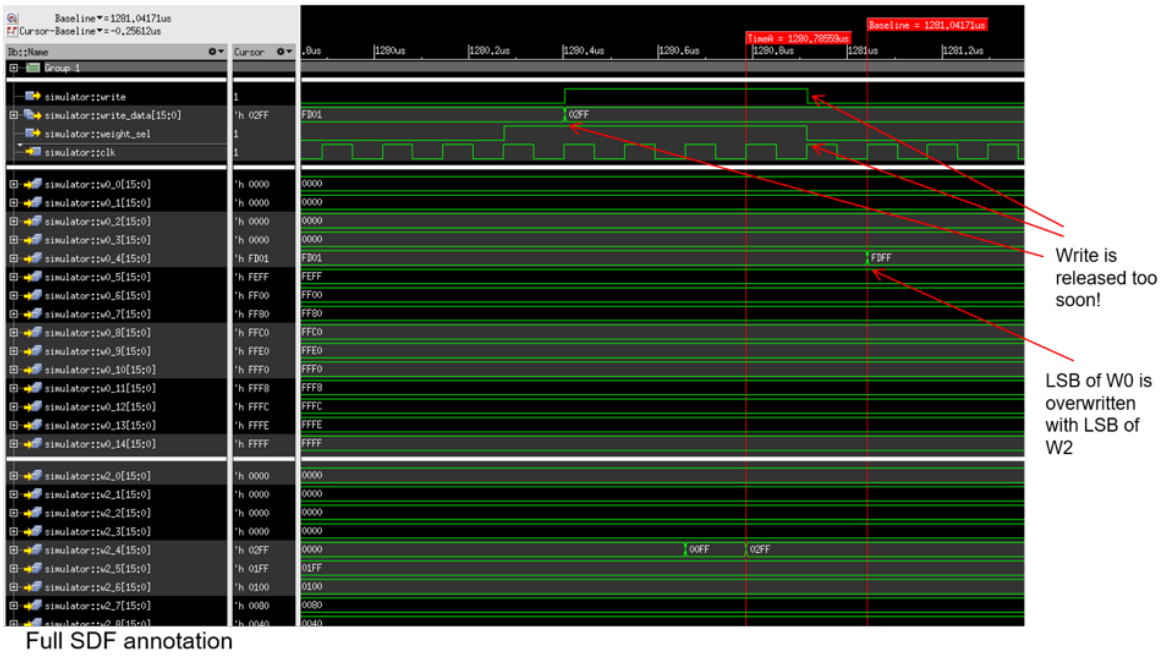

Figure 5: Error in writeback of calibration weights

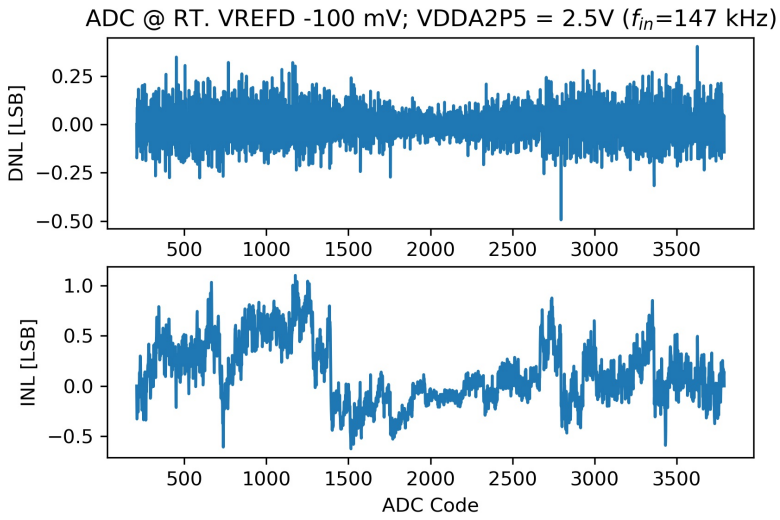

Figure 6: ADC linearity with VREFN/P +/- 100mV

5.4 SHA/MUX Linearity [Prakash]

5.5 SDC Linearity [Dabrowski]

5.6 IR Drop [Christian/Miryala]

At room temperature, when the test inputs are used to test the pipeline ADCs individually (bypassing the input buffers, Sample and Hold Amplifiers (SHAs), and the SHA multiplexer), significant non-linearity is observed for input signals near the voltage extremes of the ADC. At cryogenic temperature, no significant deviation from linearity is observed. We interpret this as evidence that there is an IR drop on the analog 2.25V power when the chip is operated at room temperature. The fact that the

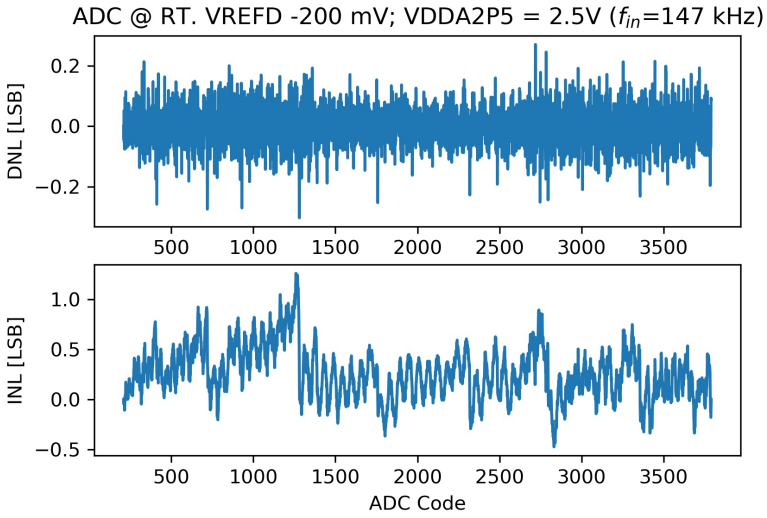

Figure 7: ADC linearity with VREFN/P +/- 200mV

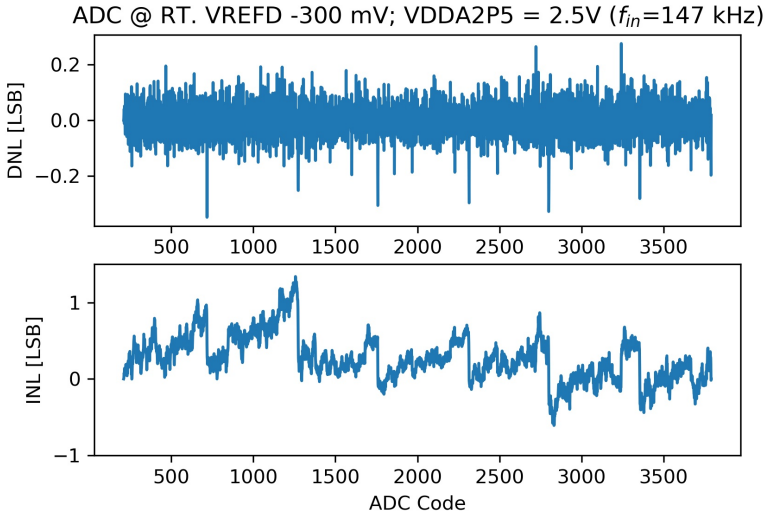

Figure 8: ADC linearity with VREFN/P +/- 300mV

non-linearity is not observed at cryogenic temperature or elevated analog supply voltage (from 2.25 to 2.5V) at warm is consistent with the fact that the resistivity of the metal used to distribute the power is greatly reduced at cryogenic temperature. Metal layers M8 and M9 were used for power distribution. The redistribution layer (AP) was not used and could easily be added to the power mesh in the analog sections of COLDADC. We will make this change in the next submission.

5.7 SHA/MUX Crosstalk [Grace/Prakash/Lin]

While there is no formal specification regarding the channel crosstalk, we have measured crosstalk of approximately 1%. We have done a variety of measurements that suggest the crosstalk is due to kickback between the channels during the sampling phase that makes it so the SHAs are not completely settled between samples. When the channels are slowed down, the crosstalk is somewhat mitigated, which indicates that it is due to insufficient bandwidth in the SHA Mux. To improve this, we will lower the impedance of the Mux to allow faster settling.

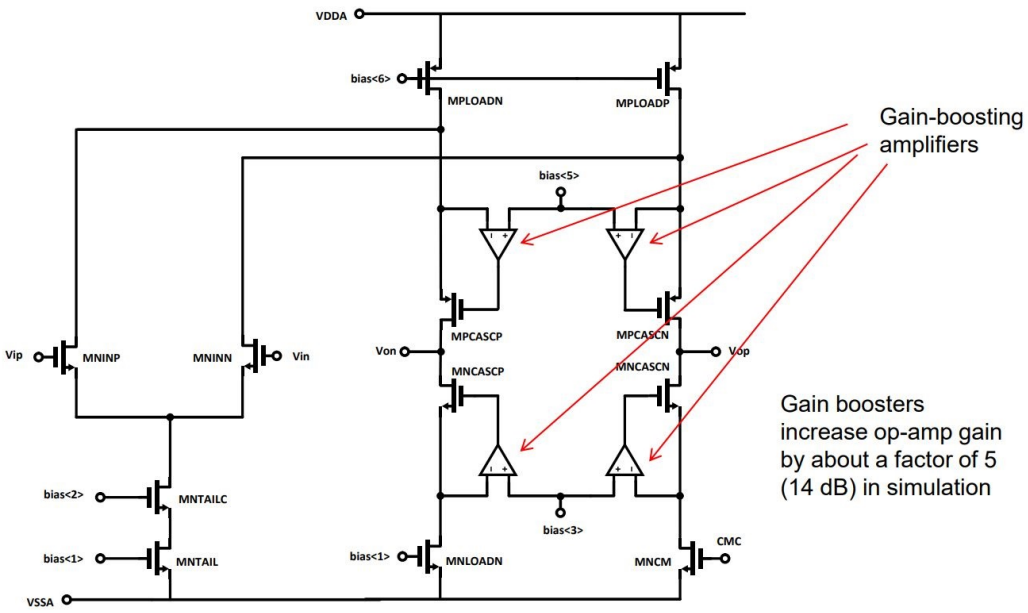

Figure 9: Op Amp

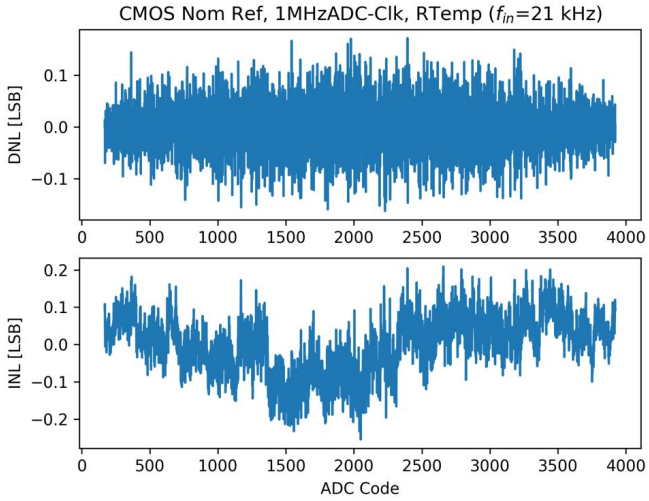

Figure 10: Linearity with Gain Boosters ON

5.8 BGR Op-amp [Dabrowski]

5.9 Overflow Wraparound [Grace]

The gains of each stage are weighted by the calibration. If the sum of the weights of the stages is greater than 2^{16}, then the digital correction logic can overflow, and a large input can lead to a small output code and vice versa. The stages were designed with an analog closed-loop gain slightly less than two. Based on supplied process data, we expected the closed-loop gain would be low enough to be free from overflow. In fact this was not the case and overflow was observed when the input voltage was close to one of the reference voltages. This can be seen in Figure 16, which shows the response of the two different ADCs on one of the Cold ADC prototypes to the same input signal. The One the left portion of Figure 16 shows the ramp response of ADC0 and the prototype operates as expected. When the ADC is saturated, the digital output is pinned to its maximum value. On the right portion of Figure 16 overflow is observed as part of the ramp response of ADC1. In this case, the ADC input reaches its

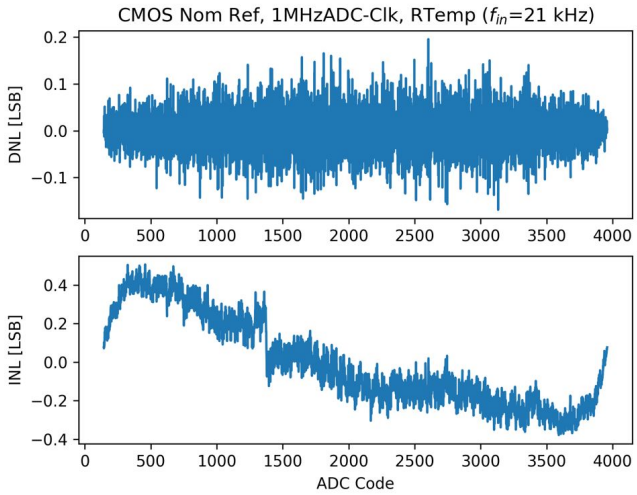

Figure 11: Linearity with Gain Boosters OFF

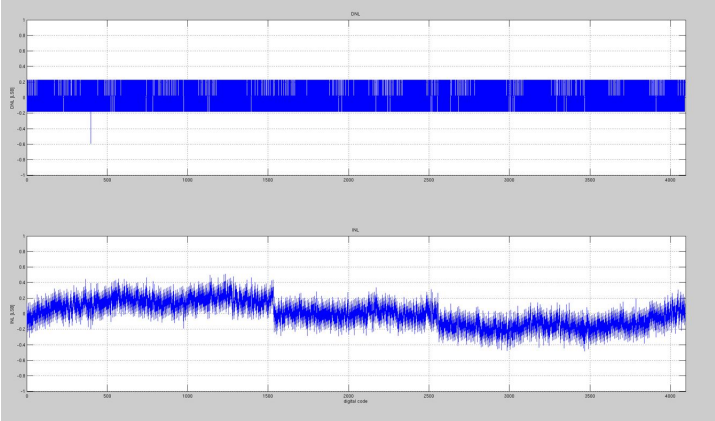

Figure 12: MATLAB model - gain boosters on -> 80 dB op-amp gain

maximum value but instead of remaining pinned, the digital output jumps to a low value. This is due to higher-than-expected closed-loop gain in ADC1.

We will fix this in two ways. First, we will further reduce the analog gain of the stages. Second, we will add to the next version of the prototype a digital overflow detection block that will sense over (or under) flow and pin the output code at a high or low level, respectively. It will do that by looking at the sign bit of the running sum one stage prior to the last. Then the algorithm will know whether to pin to a high or low value.

6 Production Testing [Furic/Gao]

6.1 Test Setup

6.2 Results

7 Summary

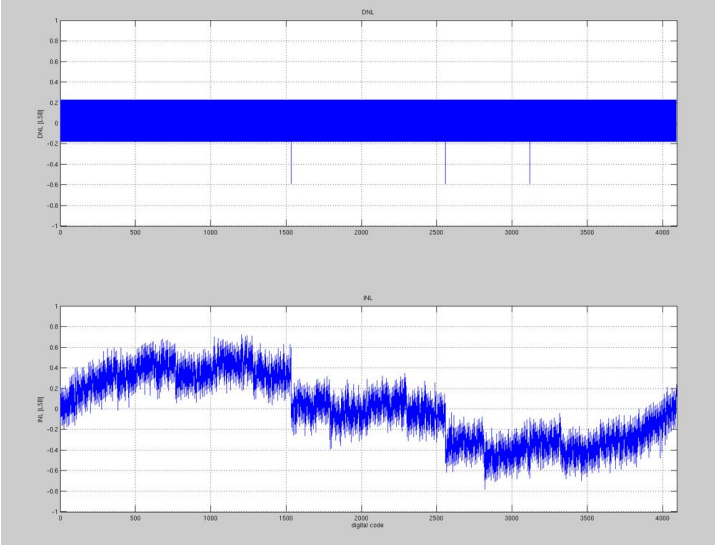

Figure 13: MATLAB model - gain boosters off -> 74 dB op-amp gain

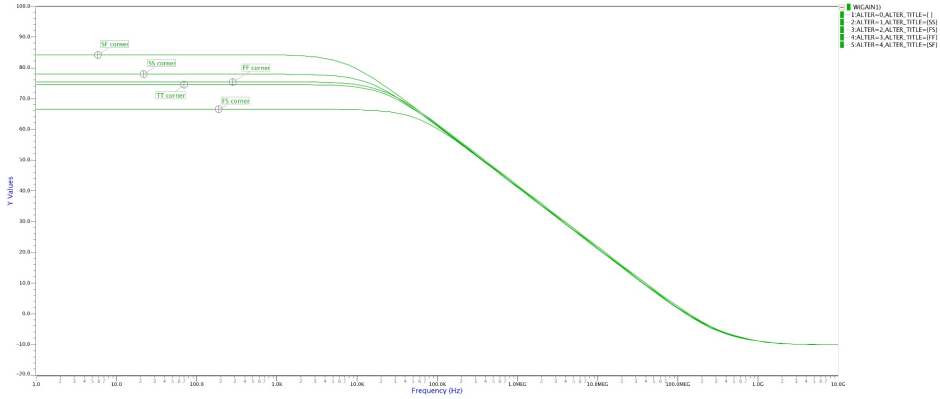

Figure 14: Corner analysis of the op-amp gain, with current gain booster circuit

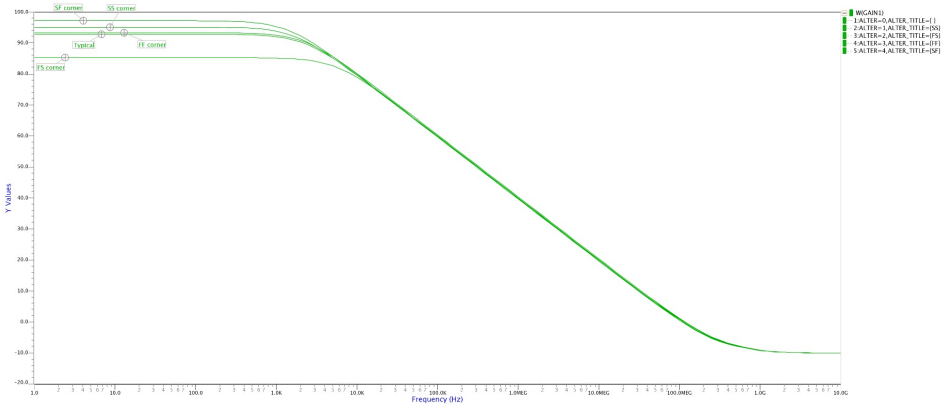

Figure 15: Corner analysis of the op-amp gain, with improved gain booster circuit

References

[1] "LBNF/DUNE Conceptual Design Report", https://web.fnal.gov/project/LBNF/ReviewsAndAssessments/LBNF-DUNE%20CD-1-Refresh%20Directors%20Review/SitePages/

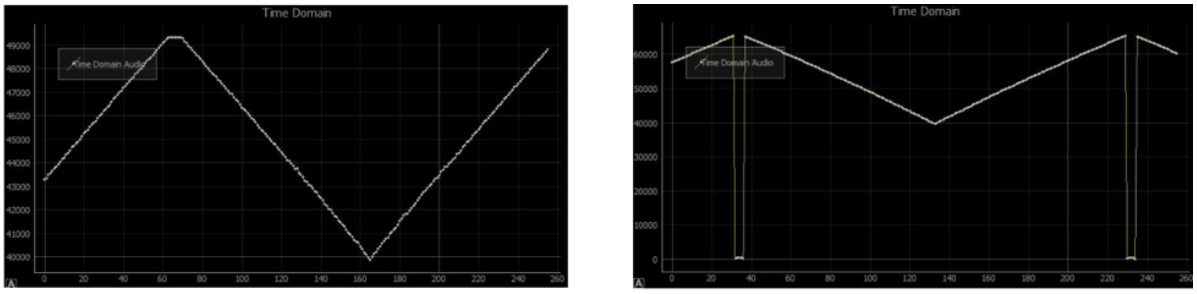

Figure 16: Digital overflow. The image on the left corresponds to ADC0 and the image on the right corresponds to ADC1.

Conceptual%20Design%20Report.aspx

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[3] "The GENIE Neutrino Monte Carlo Generator", C. Andreopoulos, et al., Nucl. Instrum. Meth. A614, 87 (2010).

Appendix

Example for citing references. References [1–3] should be entered in bibliography.tex file under your section.

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Example for citing references. References~\cite{dunecdr,montanari_35ton,genie}.
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Here is an example of how to insert Fig. 17. Figures should be saved in ./figures directory.

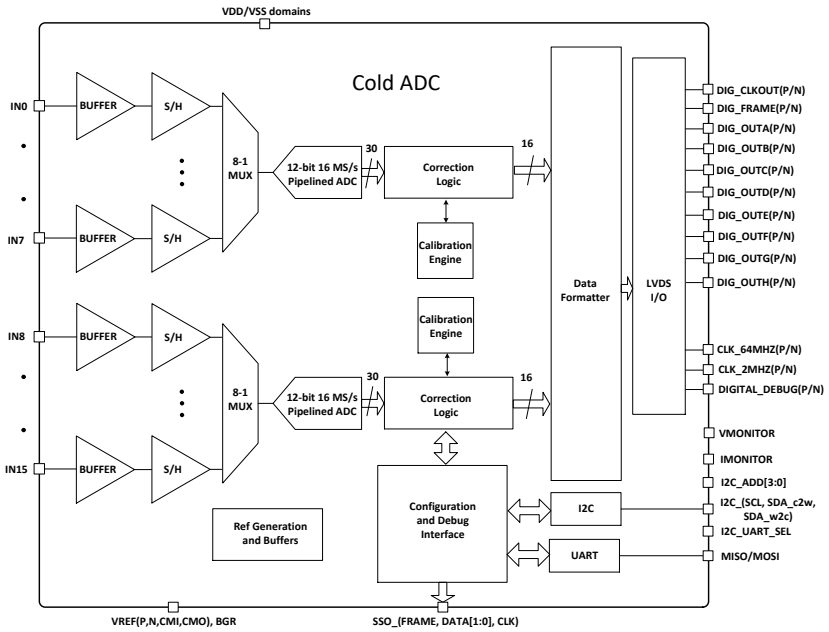

Figure 17: ColdADC Block Diagram.

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\end{center}
\caption{ColdADC Block Diagram.}
\label{fig:adc_blockdiagram}
\end{figure}
```

Here is an example of how to create Table 3.

Component	dimensions [m]
APA (active)	$2.29(wide) \times 5.9(high)$
APA (external)	$2.32(wide) \times 6.2(high)$
TPC (active)	$7.0(long) \times 7.2(wide) \times 5.9(high)$
TPC (external)	$7.3(long) \times 7.4(wide) \times 6.2(high)$
cryostat (internal)	$8.9(long) \times 7.8(wide) \times 8.1(high)$

Table 3: Dimensions of DUNE-PT.

```
\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
\textbf{ Component } & dimensions [m]  \\ \hline \hline
APA  (active) &  $2.29 (wide) \times 5.9 (high)$ \\ \hline
APA  (external) &  $2.32 (wide) \times 6.2 (high)$ \\ \hline
TPC (active)       & $7.0 (long) \times 7.2 (wide) \times 5.9 (high)$  \\ \hline
TPC (external)       & $7.3 (long) \times 7.4 (wide) \times 6.2 (high)$  \\ \hline
cryostat (internal) &  $8.9 (long) \times 7.8 (wide) \times 8.1 (high)$  \\ \hline
\end{tabular}
\caption{Dimensions of DUNE-PT.}
\label{tab:TPC-dim}
\end{table}
```