Common Design Rules

The following are a list of common design rules used for generic PCB design. Design rules are usually dictated by the manufacturing limitations of the PCB manufacturer and it is recommended to check with the PCB manufacturer before finalising a circuit board design.

It is recommended to use the following rules for hole sizes:

- Holes between 0.3mm to 3.5mm increase in 0.05mm increments. Over 3.5mm drill holes increase in 0.5mm increments.
- Holes larger than 6mm will be routed out

Common Altium Design Rules:

Electrical

- Clearance
    - Minimum Clearance = 0.3mm (10mil)

Routing

- Width
    - Min Track Width (both top and bottom layers) = 0.3mm (10 mil)
    - Preferred Track Size (both top and bottom layers) = 0.5mm (20 mil)
    - Max Track Width (both top and bottom layers) = 2mm (80 mil)

- Routing Via Style
    - Min Via Diameter = 1.3mm (50 mil)
    - Max Via Diameter = 3mm (120 mil)
    - Preferred Via Diameter = 1.3mm (50 mil)
    - Min Hole Size = 0.7mm (30 mil)
    - Max Hole Size = 1.5mm (60 mil)
    - Preferred Hole Size = 0.7mm (30 mil)

Plane

- Polygon Connect Style
    - Conductor Width = 0.5mm (20 mil)
    - Air Gap Width = 0.3mm (10 mil)

Manufacturing

- Hole Size
    - Min Hole Size = 0.7mm (30 mil)
    - Max Hole Size = 4mm (160 mil)
- Hole to Hole Clearance
    - Hole to hole clearance = 0.15mm (6 mil) (maybe less if datasheet of component dictates)
- Minimum Solder Mask Sliver
    - Minimum Solder Mask Sliver = 0.01mm (0.4 mil)
- Silkscreen Over Component Pads
    - Silkscreen over component pads = 0.01mm (0.4 mil)
- Silk to Silk Clearance

    - Silk to silk clearance = 0.01mm (0.4 mil)

Placement

- Component Clearance
    - Min Vertical Clearance = 0.3mm (10 mil)
    - Min Horizontal Clearance = 0.3mm (10 mil)