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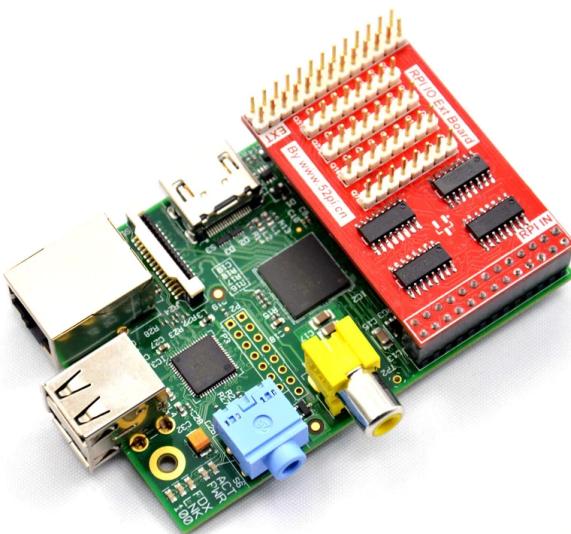
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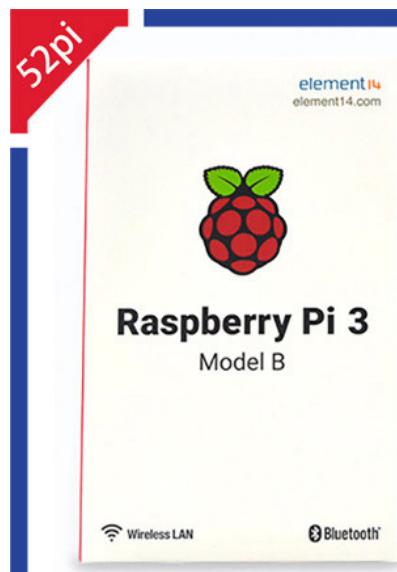
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### PRESSENTATION

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### Raspberry Pi Infinity Cascade RPI GPIO IO Expansion Board Extend Adapter Module

This module is designed specifically for the Raspberry Pi IO Expansion Modules, which can effectively solve the raspberry portinsufficient. Module uses four 74HC595 chips to expand 32 IO ports. As stated above, the top of the module will expand Raspberry Pi IO again which can be cascaded for the most IO expansion modules can theoretically unlimited expansion.

[5 inch Poster](#)[7 inch Poster](#)[10.1 Inch Poster](#)**› Banana Pi**[Banana Pi-Poster](#)[Banana Pi-Extend Modules](#)**› Launchpad****› BeagleBone Black****› Others****• expanded 32 GPIO**

- Infinity connection for the same module
- use PI API wiring, sample code

**Package Include:**

- 1pcs \* Infinity Cascade Module

**Harbor:**

- Raspberry Pi 2 \* 13 port
- Raspberry Pi 2 \* 13 waterfall port
- Q0-Q31 expanded IO port

**Product Parameters:**

- working voltage: 2.4v-5v
- IO voltage: 3.3v
- extended 32 unidirectional IO
- connection via SPI
- 100 MHz (typical) move off frequency
- 8-bit serial input
- 8-bit serial or parallel output
- specified from -40C to + 85C and from -40C to + 125C

**Typical application:**

- drive screen trellis
- pilot digital display
- LED matrix reader

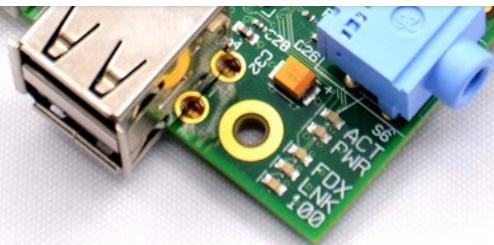
**Technological support:**

- [wiki.52pi.com/index.php/RPI\\_Infinity\\_cascade\\_IO\\_expand\\_Module\\_SKU:EP-0028](http://wiki.52pi.com/index.php/RPI_Infinity_cascade_IO_expand_Module_SKU:EP-0028)

**how to use:**

insert the module that the silk screen says 'RPI IN'. be careful not to do the reverse direction! the correct direction to insert above the Raspberry Pi of PCB; The 8 \* 4 header in the module are Q0-Q31 expanded GPIO, they can connect to the dev Dupont Line. the header which near silk screen write 'EXT' expand GPIO of Raspberry Pi, user can cascade the other mod same module.





You can also use Infinity Cascade RPI GPIO Expansion Board to connect with an RPI-RGB-LED-matrix Module, it is so co

#### more information:

The 74HC595, 74HCT595 are high-speed si-gate and devices are pin-to-pin compatible with Low-power Schottky TTL (LS) are specified in accordance with the JEDEC No standard. 7A.

The 74HC595, 74HCT595 are 8-stage serial shift registers with a storage register and 3-state outputs. the registers have 8 clocks.

Data is shifted on the rising edge of input clock shift register transitions (SHCP).

The data in each register is transferred to the storage register on a positive transition from the input clock storage register the two clocks are linked together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a standard serial output (Q7) for cascading. it is also supplied with asynchronous (active BAS) for all 8 step shift register. The storage register has 8 parallel 3-state bus driver outputs. data in the storage register appears at the exit whenever the output allow input (OE) is LOW.

#### table function

control			Entrance	exit	function	
PSSS	STCP	OE	Mr.	DS	Q7 Qn	
X	X	L	L	X	L NC	a LOW-level on MRonly affects the shift registers
X	& uarr;	L	L	X	L L	empty shift register loaded into storage register
X	X	H	L	X	L Z	clear shift register; parallel outputs in high-impedance OFF-state
& uarr;	X	L	H	H	Q6S NC	High Level logic shifted in shift register step 0. content of all shift register steps moved through, p. ex. previous stage 6 condition (internal Q6S) appears on the serial output (Q7).
X	& uarr;	L	H	X	NC QnS	contents of shift register steps (internal QnS) are transferred to the storage register andparallel output stages
& uarr;	& uarr;	L	H	X	Q6S QnS	shift register contents moved through; previous page table of contents of shift register is transferred to the storage register and the parallel output stages

H = HIGH voltage state;

L = LOW voltage state;

& uarr; = DOWN-on transition;

X = do not care;

NC = no change;

Z = high impedance in the OFF state.

#### chronogram

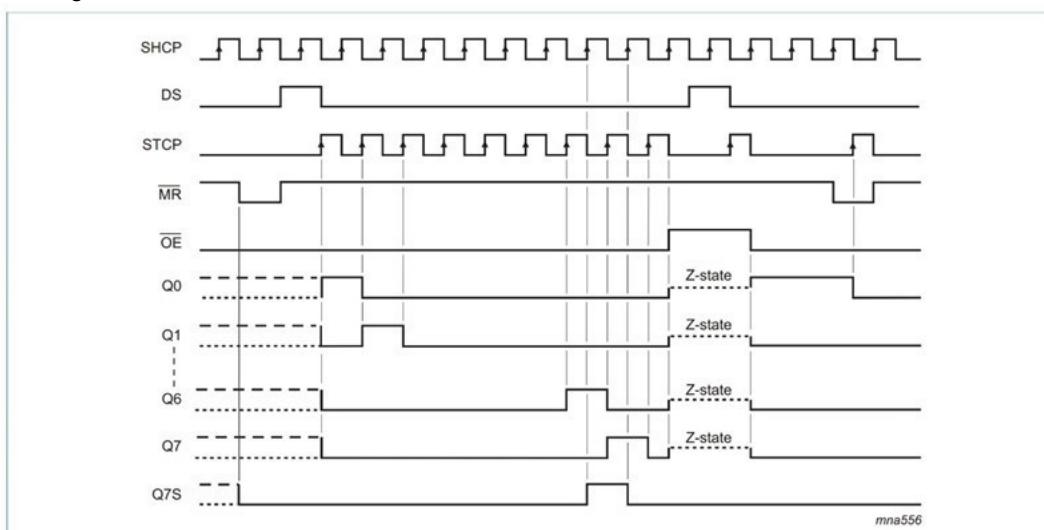
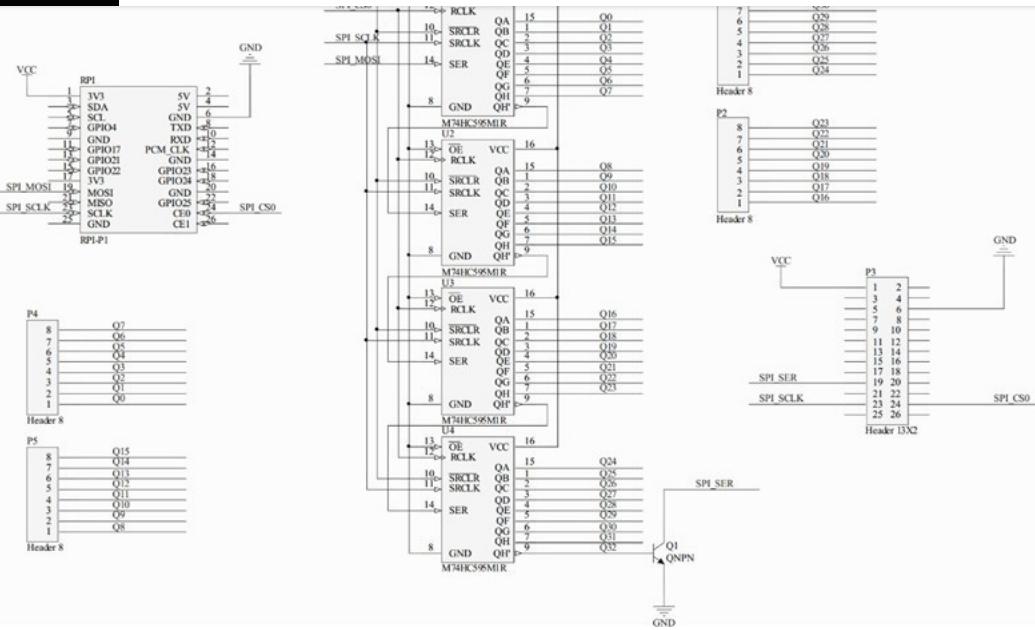


Fig 8. Timing diagram

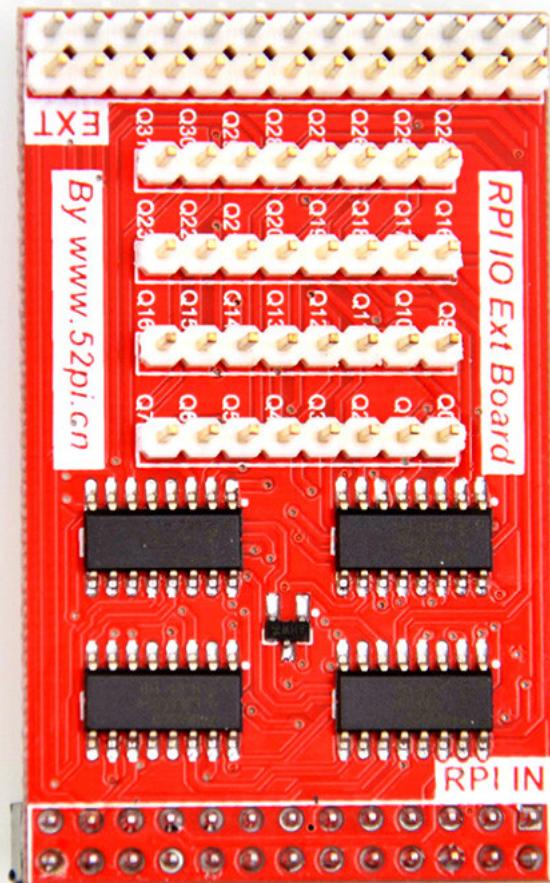
Diagram:

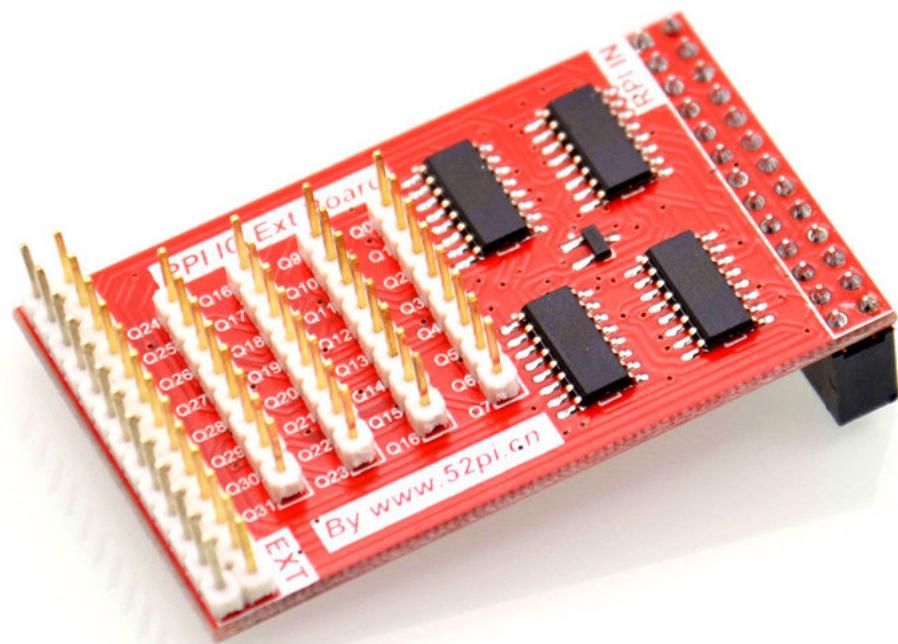
**example and test code:**

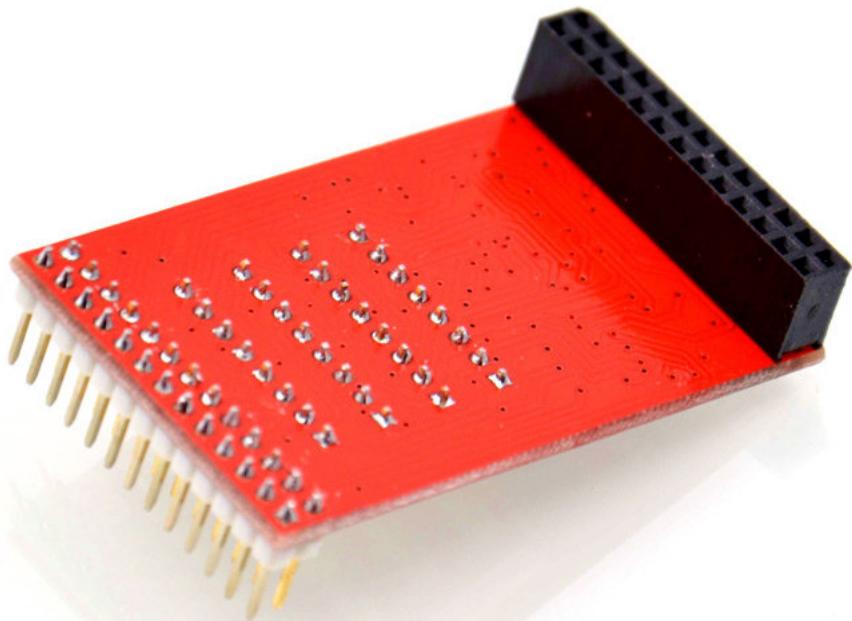
```
#include <wiringPi.h>
#include <stdio.h>
int SER = 12;
int RCLK = 10;
int SRCLK = 14;
unsigned char LED [8] = {0x01, 0x02, 0x04, 0x08, 0x10, 0x20, 0x40, 0x80};
empty SIPO (unsigned char byte);
pulse vacuum (int pins);
void init () {
pinMode (SER, OUTPUT);
pinMode (RCLK, OUTPUT);
pinMode (SRCLK, OUTPUT);
digitalWrite (SER, 0);
digitalWrite (SRCLK, 0);
digitalWrite (RCLK, 0);
}
void delayMS (int x) {
usleep (x * 1000);
}
int main (empty)
{
if (-1 == wiringPiSetup ()) {
printf ("WiringPi configuration failed!");
return 1;
}
init ();
int i;
int i;
while (1) {
for (i = 0; i < 8; i++)
{
SIPO (LED [i]);
pulse (RCLK);
delayMS (50);
printf ("i =% d", i);
}
printf ("\n");
delayMS (500); // 500 MS
for (i = 7; i >= 0; i-)
{
SIPO (LED [i]);
pulse (RCLK);
delayMS (50);
printf ("i =% d", i);
}
}
```

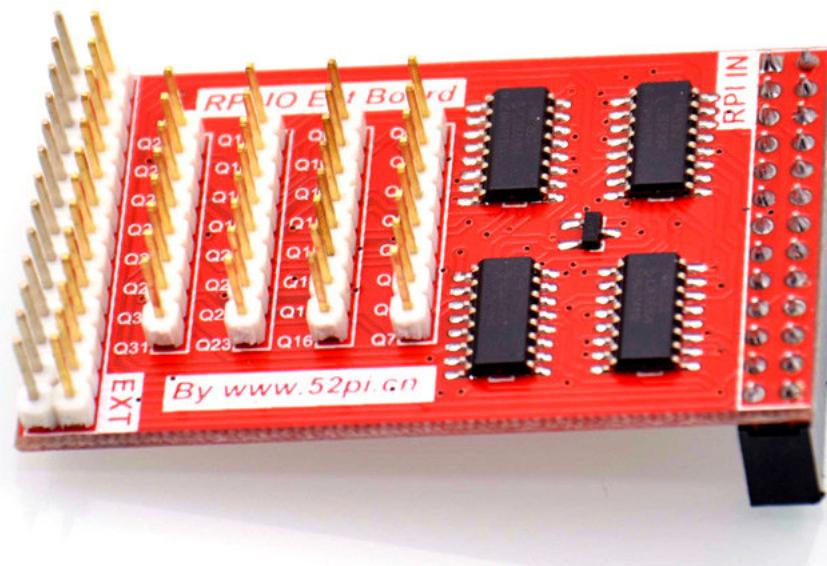
```
usleep (1000);
digitalWrite (RCLK, 1);
}
empty SIPO (unsigned char byte)
{
int i;
for (i = 0; i <8; i + +)
{
digitalWrite (SER, ((byte and (0x80>> i))> 0));
pulse (SRCLK);
}
}
pulse vacuum (int pins)
{
digitalWrite (pin, 1);
digitalWrite (pin, 0);
}
```

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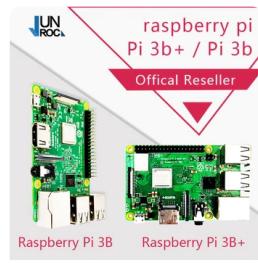
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