EE517 ANALOG IC DESIGN LAB
Course Project

Design a 2-stage Op-amp in 180 nm technology with Low power(power optimization)

Submitted by,
KARTALI CHANUKYA
Roll No-234102410
April 8, 2024

Contents

1 Experiment

Design and analysis of a 2-stage op-amp

2 Objective

Design and analyze a 2-stage op-amp with the Design specification mentioned below.

2.1 General Specifications

- Supply voltage V_{DD} is 1.8.
- Reference current source I_{ref} is 20µA.
- Slew rate is 1V/µs .
- Phase margin $\geq$ 60 .
- Load Capacitance C_L is 10pF.
- ICMR is 0.6- 1.4 V

2.2 design Specifications - Low Power (Power should be minimum)

- Gain $\geq$ 40dB
- GBW$\geq$10MHz
- Pdiss$\leq$0.25mW
- Lmax $\leq$ 2µm

2.3 Observations

2.3.1 DC analysis

- Report the schematic of the diff pair with DC OP point annotated: Id, Vgs, Vds, Vth, Vdsat, gm, gds, gmb, region.
- Check that all transistors operate in saturation.

2.3.2 AC analysis

- Observe pole-zero analysis of your circuit.
- Frequency response of your circuit.
- Find Av, PM, Bandwidth, CMRR, PSRR.
- Give a proper reason for selecting any value of any parameter.

2.3.3 Transient Analysis

- slew rate.
- ICMR, OCMR.

3 Theory

3.1 Some Definitions:

3.1.1 Transconductance($\mathbf{g_m}$)

It show us how productively a device converts voltage variation in input to current variation in output.In Mosfet input voltage applied at gate to source and output current si drain current .so It is the rate of change of drain current with respect to change in Gate-Source voltage.

$$g_m = \frac{dI_{ds}}{dV_{gs}} \tag{1}$$

3.1.2 voltage Gain $\mathbf{A_v}$:

Voltage gain is the one of the important parameter in AC analysis.It tells how much input amplifies by the circuit.generally we find out voltage gain by divide the small signal volatge output by the small signal voltage input.so maximum value of gain in the bode plot of gain treated as the voltage gain of the circuit.

$$A_v = \frac{v_{out}}{v_{in}} \tag{2}$$

3.1.3 Cut off frequency $\mathbf{f_c}$:

cut off frequency is up to which we have the half power .because to get proper gain we need atleast half power. It is also called the 3db frequency ,because half power means we need to have the 70 percentage of Voltage .we are going to plot the gain versus frequency graph which is the bode plot. so it will be frequency at which gain will the 3db less tahn the maximum value of gain.

cutt off frequency= $\text{frequency}_{\text{at 3db less than maximum gain}}$

$$Bandwidth = \frac{1}{2\pi R_{out} C_{OUT}} \tag{3}$$

3.1.4 Source Drain resistance($\mathbf{R_{ds}}$)

In a MOSFET output resistance is one of the important parameter.It is used for analysis the gain of the circuit and also useful to design the current source.To find out the output resistance we can use the Channel length modulation parameter(λ) and I_d at VGS-V_{th}.

$$r_{ds} = \frac{V_A}{I_{ds}} \tag{4}$$

3.1.5 Output Resistance resistance($\mathbf{R_{out}}$)

In a MOSFET output resistance is one of the important parameter.we need to have proper ouput resistance , because depends on that out put resistance amount of output will be reached to the Load circuit.To find out the output resistance of a circuit.we need to connect one test ac current souce at output

and done the ac analysis find the output voltage .then fraction of test voltage to test current will be the output resistance.

$$R_{out} = \frac{v_{test}}{I_{test}} \tag{5}$$

3.1.6 Slew Rate

Maximum Rate of change of output per micro second ,we treated as the slew rate.but in differential amplifiers we got maximum output when whole tail current is passing through one side.
General formula for slew rate is

$$slewrate = (\frac{dV_{out}}{dt})_{max} \tag{6}$$

3.1.7 ICMR

ICMR nothing but Input common mode Range .generally it is defined as range of common mode input we can applied to that circuit then all transistors in saturation.Maximum ICMR means Maximum values of common mode input we can apply.

3.1.8 GBWP

Gain Band Width Product ,of an amplifier nothing but ,product of Open Loop gain times frequency range at which amplifier gain attenuated to -20dB.

3.2 2 stage OP AMP

General differential amplifier also do same amplification as the op amp,but due heavy stack of Nmos at the bottom it have a less swing.so we are going to 2 stage for the op amp design. one is for amplification purpose which is general differential amplifier which is cascaded to next stage which have only one NMOs at the bottom ,so it have minimum value ,because it have only one vds sat value.

Given circuit diagram is

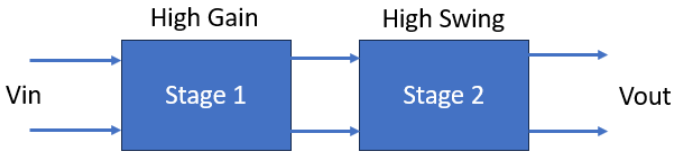

Figure 1: stages of Op amp

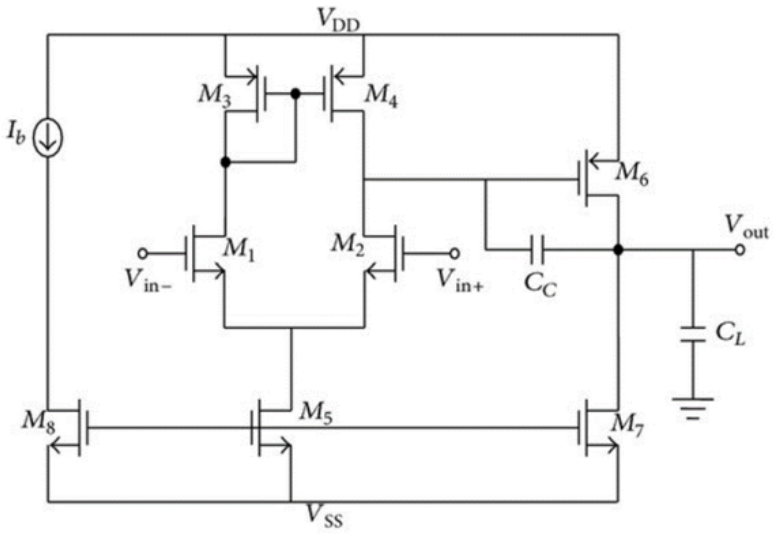

Figure 2: 2 stage OP AMP

Even though we just connected the two stage we have the issue with stability ,because after cascading the two stages ,we three high impedance nodes .so we have 2 poles which will fall under the unit gain cross over frequency , which will lead to un-stability.so we need to connected one capacitor which will make the dominant compared to the remaining poles .such that only one pole will fall under the gain cross over frequency.as we know that pole is inversely proportional to the capacitance .so to make dominant pole we need to connect the high capacitance .so simply we use the one capacitance by miller theorem.so it will provided large capacitance with small.which is Cc in above circuit.

4 2 stage OP -AMP design

4.1 Design procedure

4.1.1 Step 1

we have assumed phase margin will be 60 degrees and zero frequency at greater that 5 times Gain Band width product.so by solving the equation of one zero and two pole system , with above Assumptions we got equation.

$$(millercapacitance)C_c > 0.23C_L \tag{7}$$

They given C_L is 10 pF.so we got miller capacitance is

$$C_c > 2.3pF \tag{8}$$

4.1.2 Step 2

We have to design two stage OP AMP for low power they have given power should be less than or equal to 0.25milli watts and reference current current is 20µA. .

$$power \leq 0.25 * 10^{-3}$$
$$1.8 * (I_{ref} + I_5 + I_7) \leq 0.2510^{-3}$$
$$(I_{ref} + I_5 + I_7) \leq 138.8810^{-6}$$
$$I_5 + I_7 \leq 118.8810^{-6}$$

i have taken I_5 is 10µA and I_7 is 100µA.

$$I_5 = 10\mu A$$
$$I_{ref} = 20\mu A$$
$$I_7 = 100\mu A$$

4.1.3 Step 3

Slew rate is given in the design specification is 1 volt per micro sec.in above circuit we got maximum value of output when M1 is off and M2 is On, then M3 and M1 are series ,so M1 current also in zero. M3 and M4 connected in current mirror manner then M4 current also zero.then whole VDD will be at the drain of M2 and ,current in M2 which is M5 current flowing through Cc capacitance.then slew rate for above circuit will be.

$$slewrate = \frac{I_5}{C_c} \tag{9}$$

we have assumed I_5 is 10µA and given slew rate minimum 1v/um.so i have taken the 3.2.

$$C_c = 3.2pf \tag{10}$$

4.1.4 Step 4

we have the gain band width product will be the voltage unit gain frequency .because we have dominent pole ,so we have 20 db decay will happens at unit gain frequency.

$$gm_1 = GBW * 2\pi C_c \tag{11}$$

we have the GBW ,cc values so we got gm_1

$$gm_1 = 628.318\mu\mho \tag{12}$$

we have the gm equation

$$gm_1 = \sqrt{2I_d\mu_n C_{ox}\frac{W}{L}_1} \tag{13}$$

if you substitute the values in above equation we got

$$\frac{W}{L}_1 = 115.373 \tag{14}$$

as we know M1 and M2 are need to be symmetric so we have taken

$$\frac{W}{L}_1 = \frac{W}{L}_2 = 115.373 \tag{15}$$

4.1.5 Step 5

They given maximum ICMR value 1.4.so from above circuit we for M1 in saturation

$$V_{d1} > V_g - V_{th1} \tag{16}$$

$$V_g < V_{d1} + V_{th1} \tag{17}$$

$$V_g < (V_{dd} - V_{sg3}) + V_{th1} \tag{18}$$

$$V_g < (V_{dd} - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} \frac{W}{L}_3}}) + V_{th1} \tag{19}$$

here gate voltage is the maximum ICMR voltage .so if you you substitute the all values you got the (WŁ) of M3

$$ICMR_{max} > (V_{dd} - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} \frac{W}{L}_3}}) + V_{th1} \tag{20}$$

$$\frac{W}{L}_3 > 0.455 \tag{21}$$

as we know M3 and M4 are need to be symmetric so we have taken

$$\frac{W}{L}_3 = \frac{W}{L}_4 > 0.455 \tag{22}$$

4.1.6 Step 6

we know the ICMR minimum value which is 0.6.it will be taken from minimum gate voltage so all transistor are in saturation.so

$$V_{dsat} = ICMR_{min} - \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}_1}} - V_{thn} \tag{23}$$

if you substitute all the values you got the Vdsat value.

$$V_{dast} = 0.034 \tag{24}$$

so i have taken 100 milli volts ,then if you substitute the value on the current equation you got the

$$\frac{W}{L}_5 = 5.844 \tag{25}$$

4.1.7 Step 7

as we taken the assumption zero frequency is 5 times of the GBW. we got the

$$gm_6 > 5 * gm_1 \tag{26}$$

we know the gm_1 from the eqution 12

$$gm_6 > 628.318\mu\Omega \tag{27}$$

we know M6 and M4 are in current mirror so .

$$\frac{(W/l)_6}{(W/l)_4} = \frac{I_6}{I_4} = \frac{gm_6}{gm_4} \tag{28}$$

so we know the $(w/l)_4$ and I_4 so from gm equation we got the, i have taken the W/L of M4 such that I6 current should be 100µA ,so it is 11.7.

$$gm_4 = 126.688\mu\mho \tag{29}$$

from equation 29, we got

$$(w/l)_6 = 235 \tag{30}$$

from equation 29 we can calculate the

$$Id_6 = 100\mu A \tag{31}$$

4.1.8 Step 7

$$\frac{(W/l)_7}{(W/l)_5} = \frac{I_7}{I_5} \tag{32}$$

M6 and M7 are in series so both currents are equal.so we got

$$(w/l)_7 = 58.8 \tag{33}$$

we got the all the (wł) ratios ,we need to calculate the lengths.we know gain of two stage op amp is

$$gain = gm_1gm_2(r01||r04)(ro6||ro7) \tag{34}$$

so we know the gm1 and gm2 and gain.so if you substitute the values you got

$$(r01||r04)(ro6||ro7) = 405k\Omega \tag{35}$$

4.2 DC ANALYSIS

4.2.1 schematic

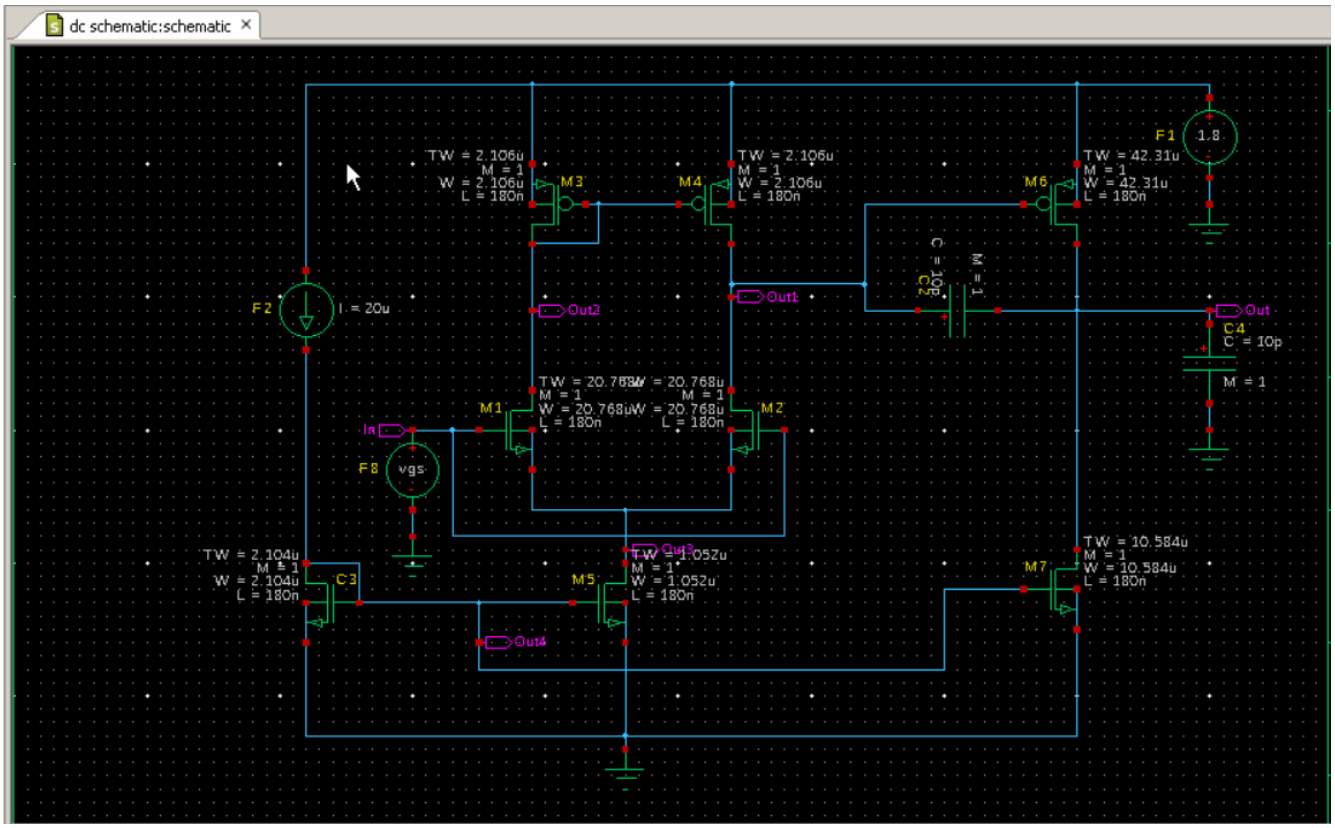

Figure 3: DC schematic of 2 stage op amp

we got the dc value at Vin 0.73710 v all the transistors are in saturation.

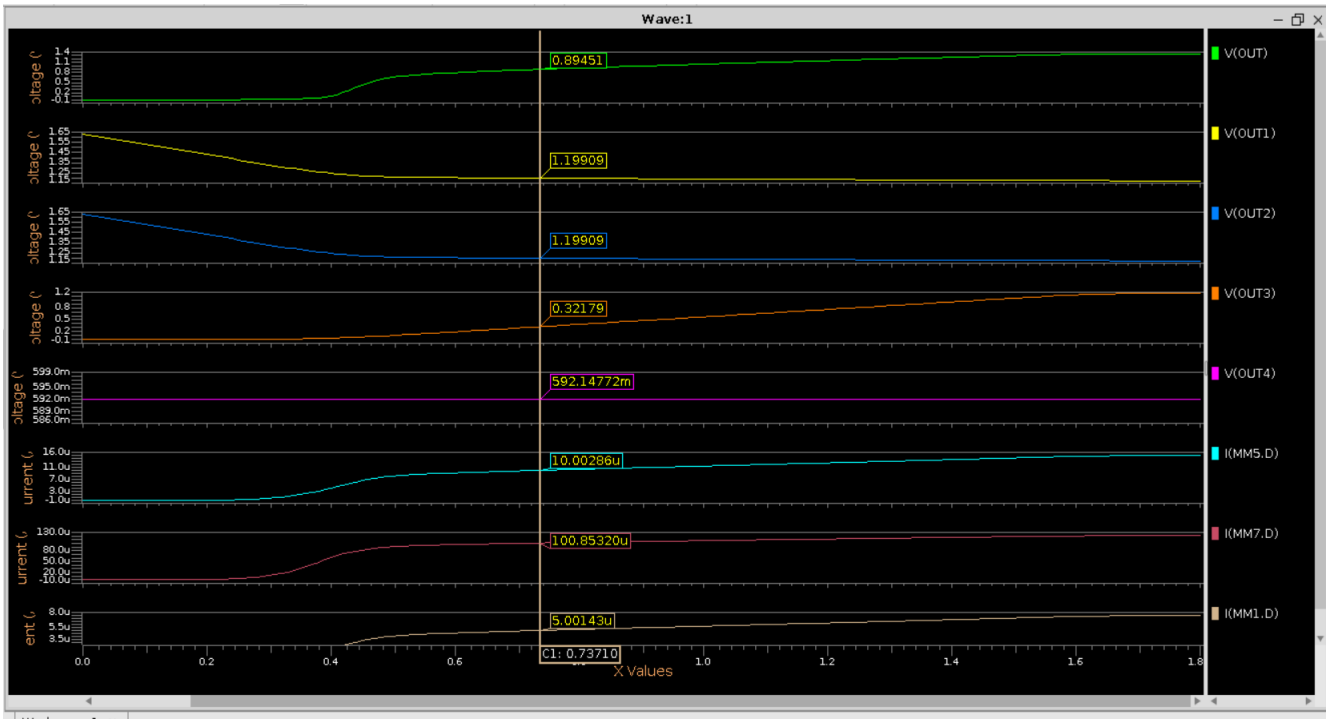

Figure 4: ID and VGs values of all transistors

4.2.2 DC observations

we are going to check the transistors are saturation are not
M1 and M2 :

$$V_D > V_G - V_{th}$$
$$out_2 > in - 0.55$$
$$1.19 > 0.737 - 0.55$$

So it is saturation.
M3 and M4: for M4

$$V_{SD} > V_{sG} - V_{th}$$
$$1.8 - out_2 > 1.8 - out_1 - 0.55$$
$$0.61 > 1.8 - 1.19 - 0.55$$

So it is saturation.
for M3 it is diode connected so always saturation.
M5:

$$V_D > V_G - V_{th}$$
$$out_3 > out_4 - 0.55$$
$$0.321 > 0.592 - 0.55$$

So it is saturation.
M6:

$$V_{SD} > V_{sG} - V_{th}$$
$$1.8 - out > 1.8 - out_1 - 0.55$$
$$1.8 - 0.894 > 0.61 - 0.55$$

So it is saturation.
M7:

$$V_D > V_G - V_{th}$$
$$out > out_4 - 0.55$$
$$0.894 > 0.592 - 0.55$$

So it is saturation.

4.3 power analysis analysis

4.3.1 Schematic

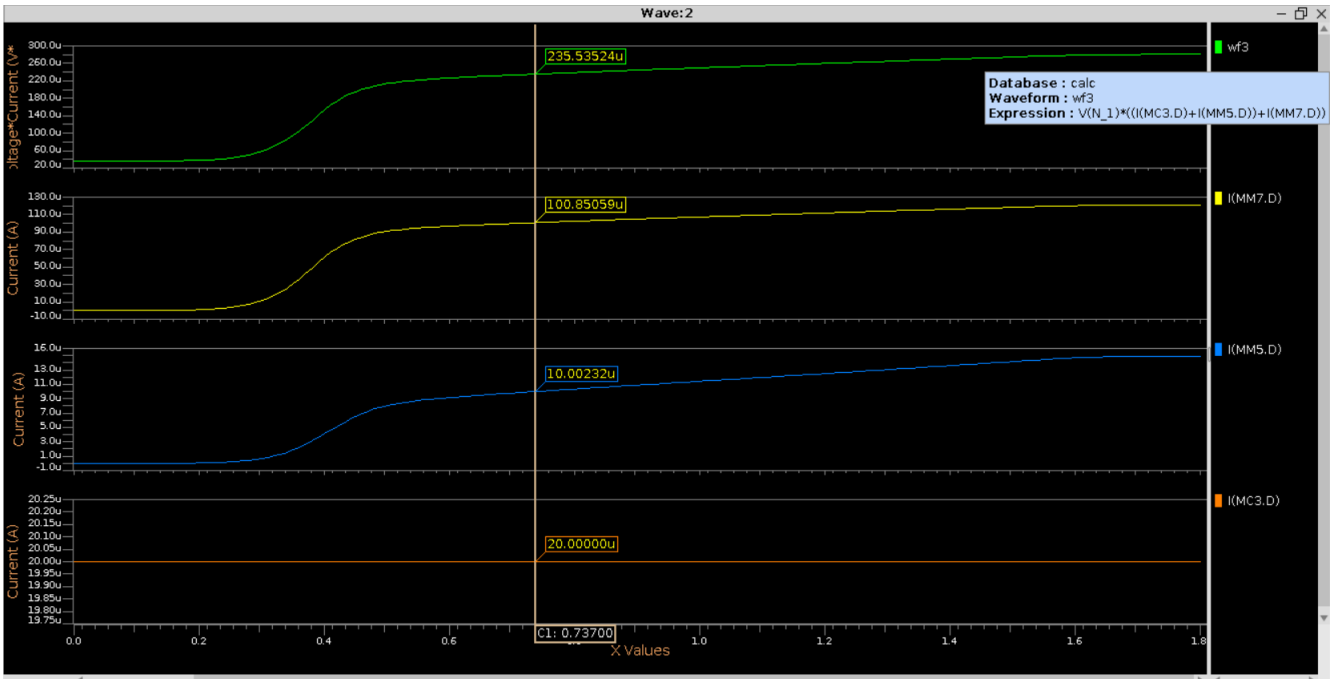

Figure 5: power of 2 stage op amp

we got power at DC voltage where we have all the transistors are in saturation.

$$power = 1.8(I_{C3} + I_{M5} + I_{M7})$$
$$power = 235.35\mu Watts$$

it is **satisfied the power specification**.

variable	specification	practical value
power	$\leq 250\ \mu$	$235.35\ \mu$

4.4 AC analysis

4.4.1 Schematic

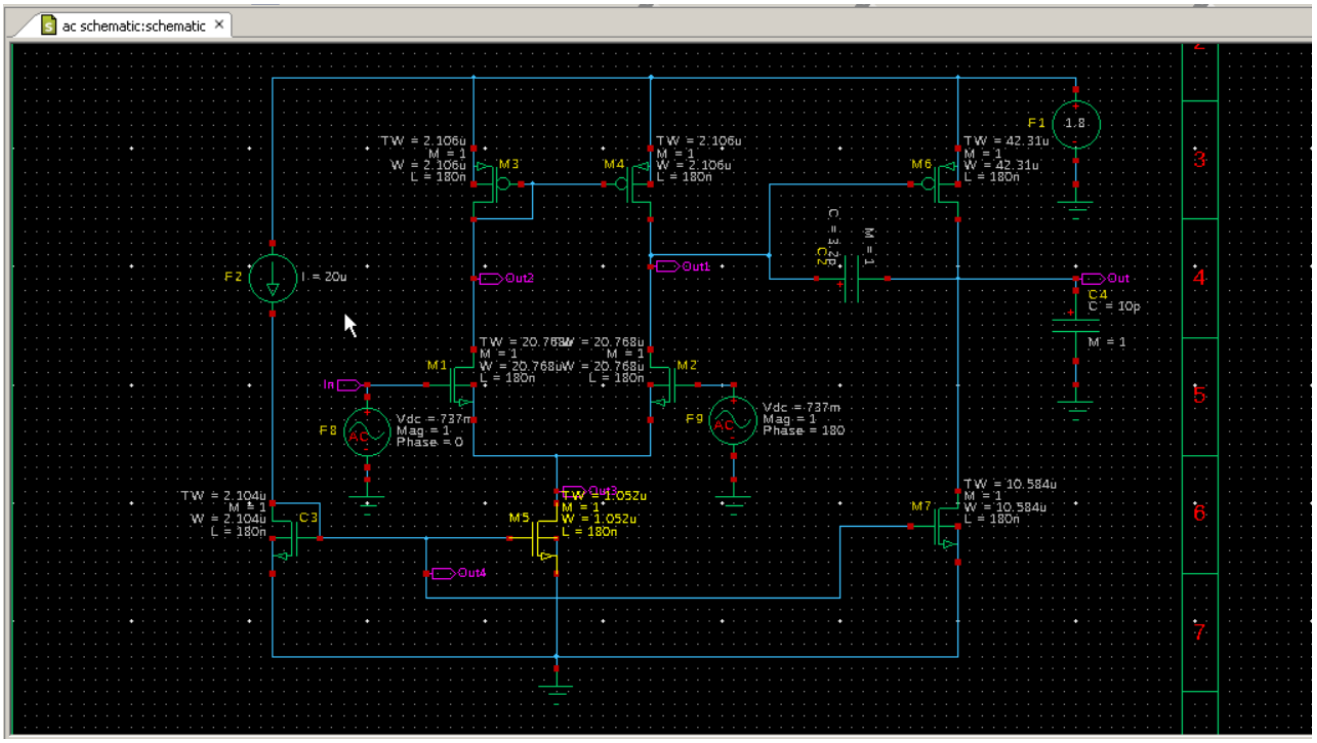

Figure 6: AC schematic of 2 stage op amp

4.4.2 AC results

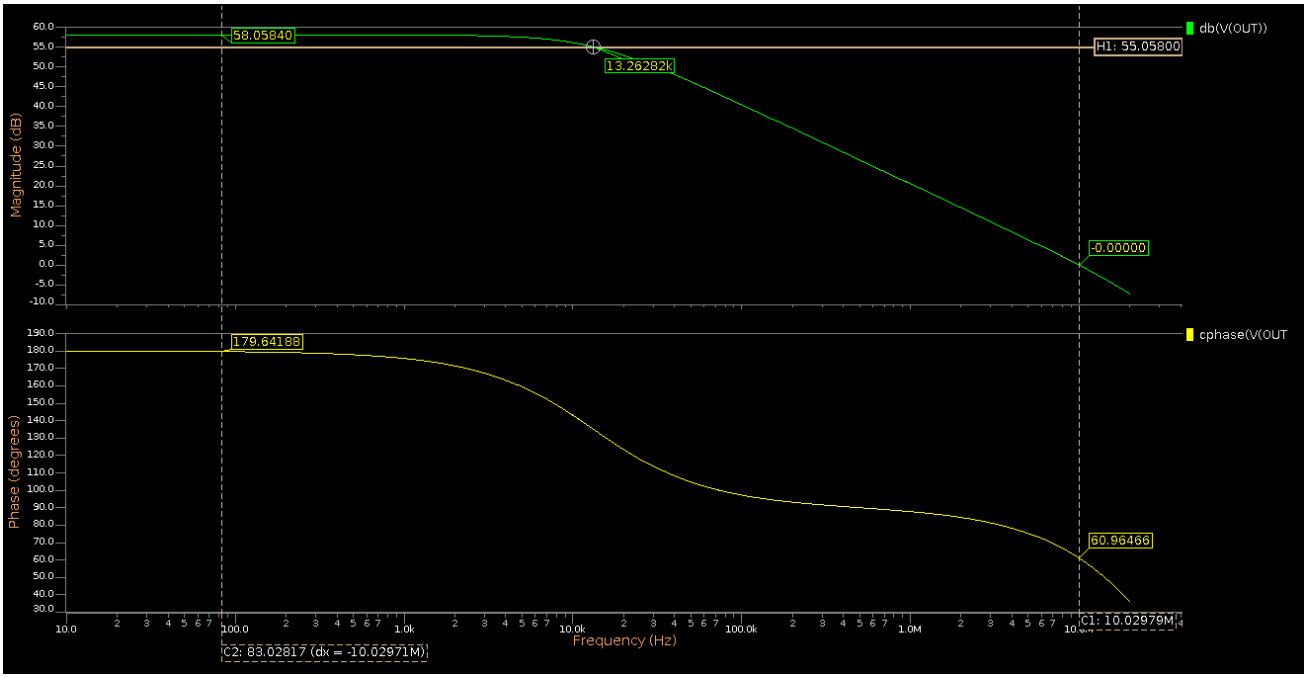

Figure 7: AC analysis of 2 stage op -amp

we got the ac parameters

$$gain = 58.058dB$$
$$bandwidth = 13.26kHz$$
$$GBW = 10.029Mhz$$
$$PM = 60.964$$

4.4.3 CMRR

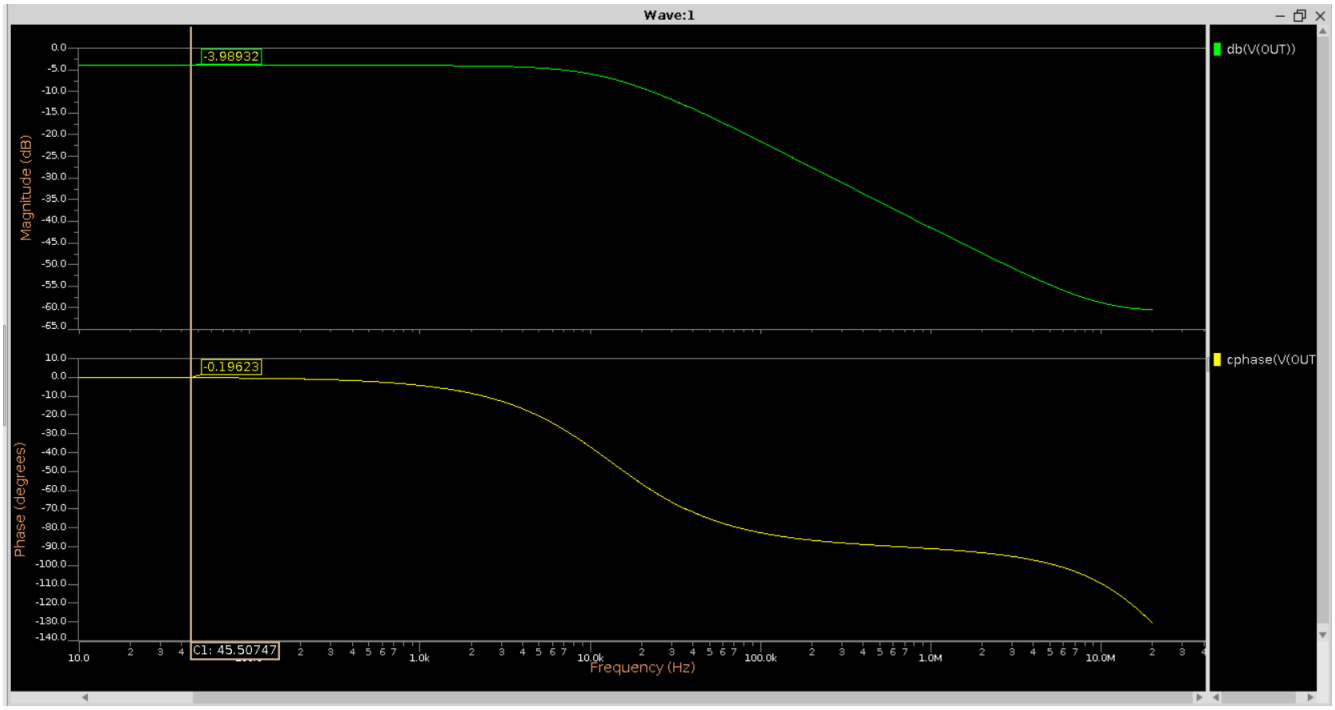

Figure 8: CMRR of 2 stage op -amp

we got the CMRR

$$A_{CM} = -3.98dB$$
$$CMRR = 62.038dB$$

4.4.4 PSRR

To calculate PSRR ,we have taken the unity feed back and at inverting terminal .we applied the dc bias voltage at non inverting terminal .which make NMOS on.Then we have to apply the ac source at the VDD and taken output will give the PSRR

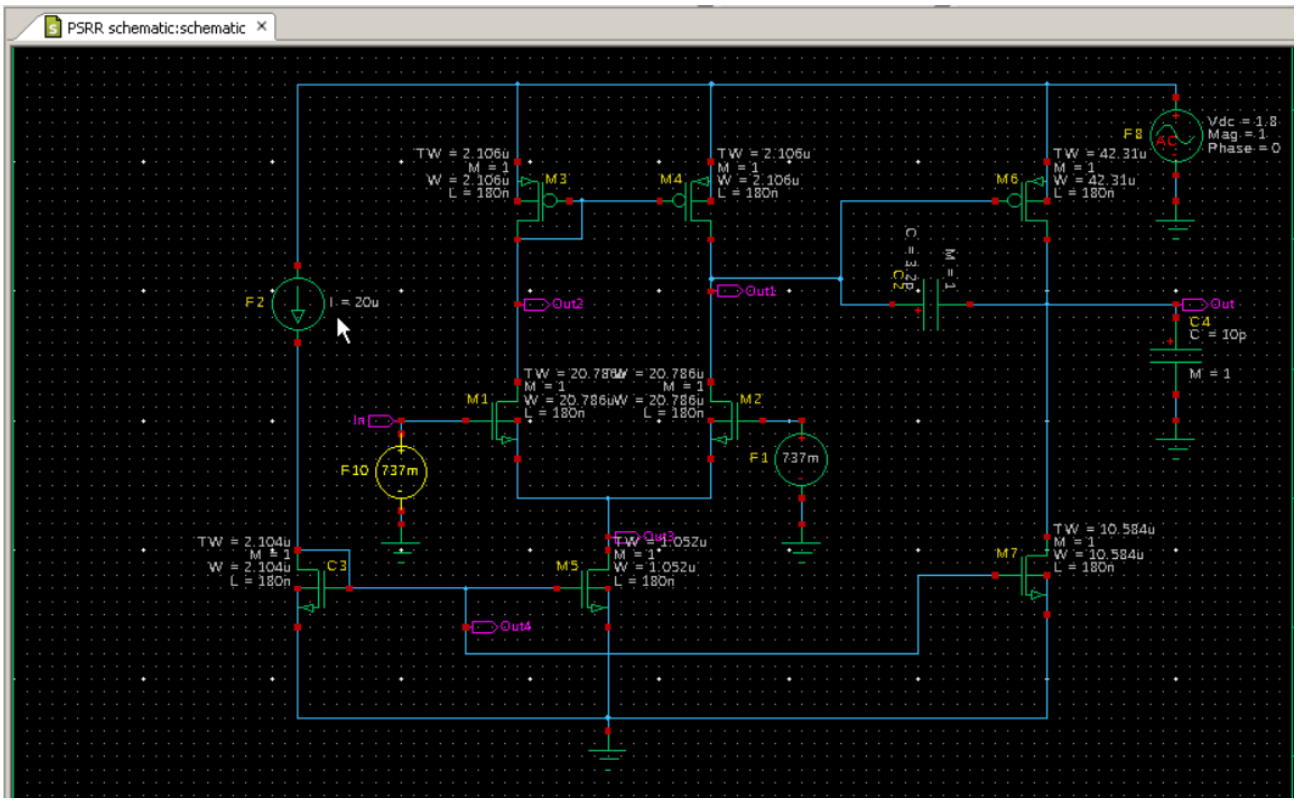

Figure 9: schematic of PSRR analysis of 2 stage OP AMP

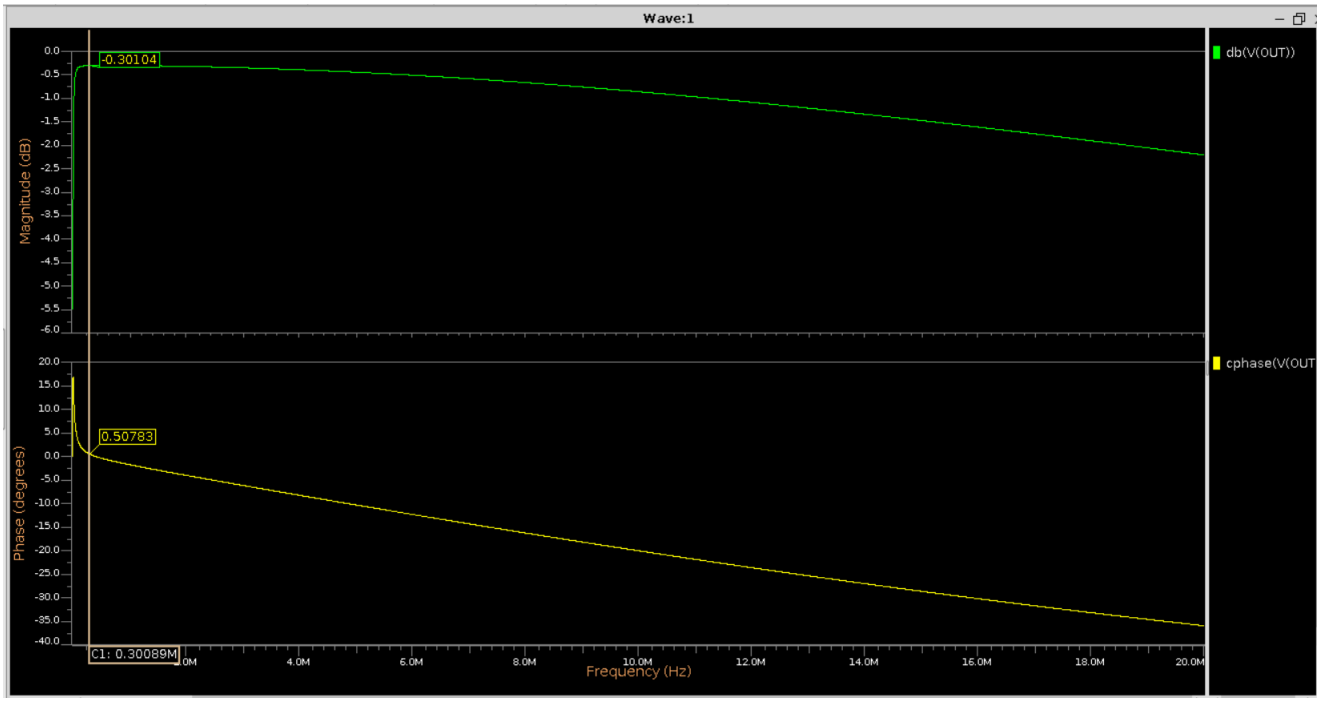

Figure 10: PSRR of 2 stage OP AMP

we got the CMRR

PSRR = -0.3014 dB

4.5 Transient Analysis

4.5.1 SLEW rate

we know slew rate will be ,when whole current passing through one side.so i have given one side input zero volts .so now whole current passing through one side .we got maximum current.

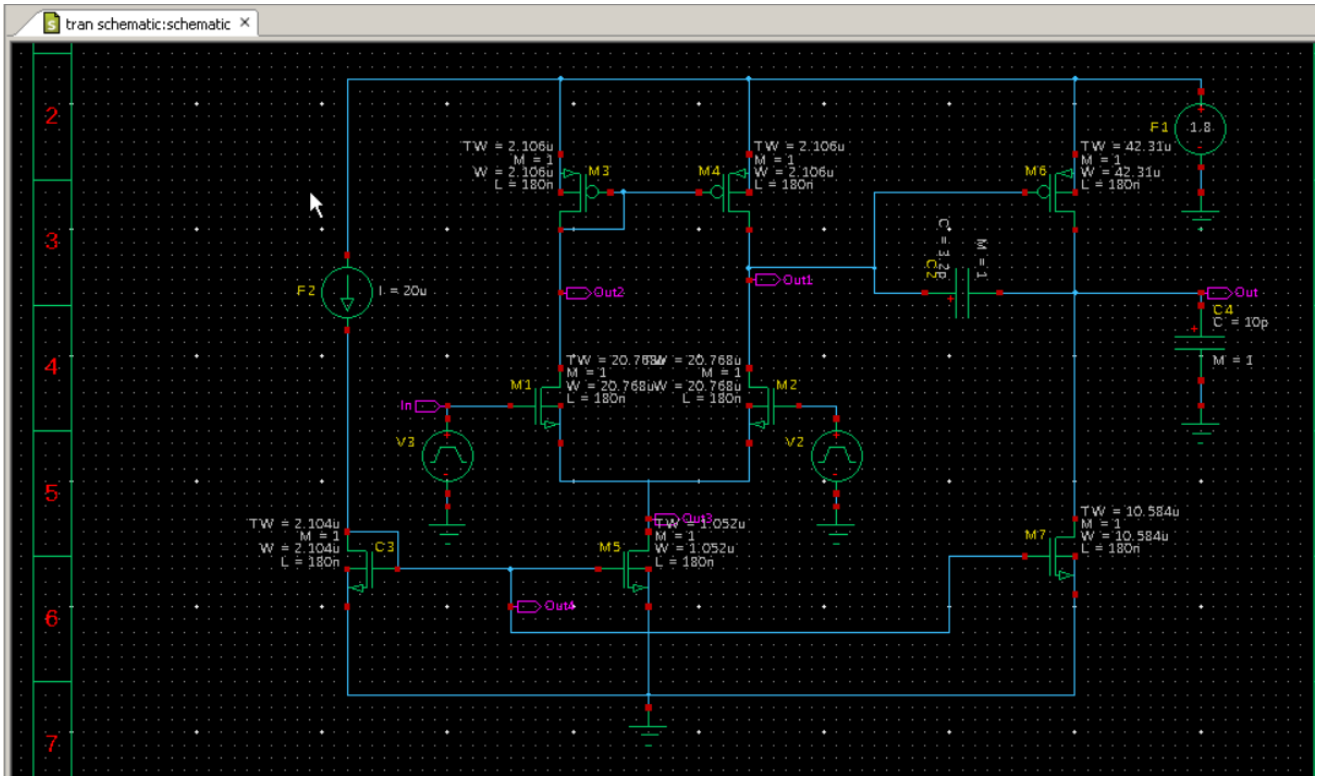

Figure 11: schematic for slew rate of 2 stage OP AMP

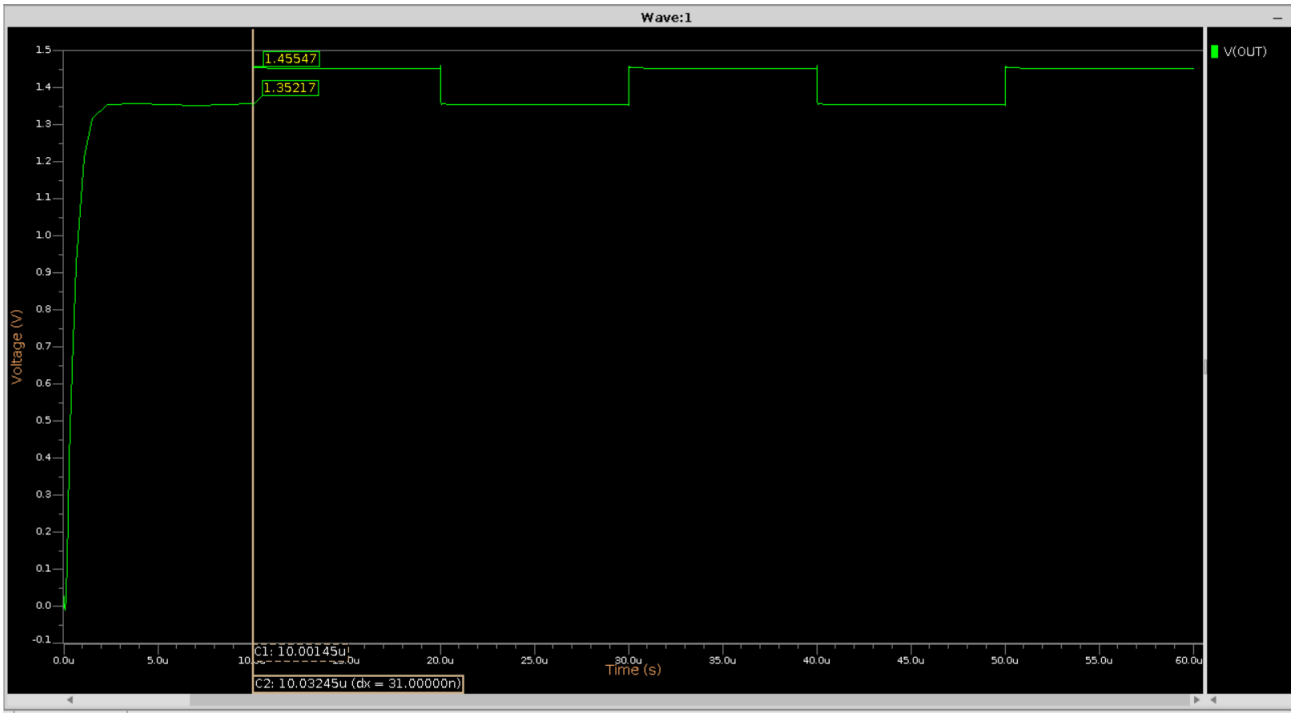

Figure 12: slew rate of 2 stage OP AMP

we got slew rate

$$slewrate = 3.32\frac{V}{\mu s} \tag{36}$$

4.5.2 ICMR and OCMR

we are taken the unit gain amplifier model ,so ICMR Aand OCMR same .so we have given the negative feed back and apply the DC sweep at the non inverting terminal.then we need to check the output .upto some input range it is in linear those range given as ICMR and saturation output will be the OCMR.

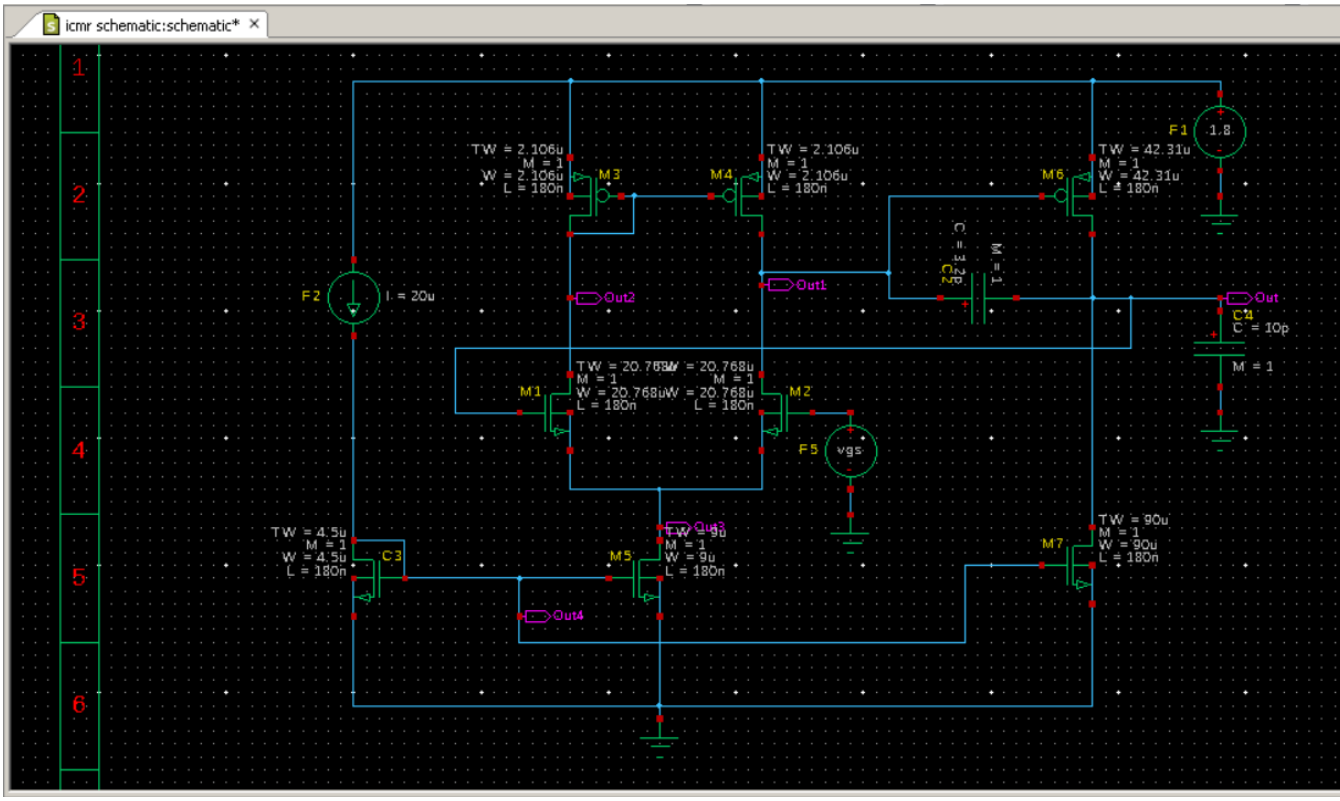

Figure 13: schematic for ICMR/OCMR of 2 stage OP AMP

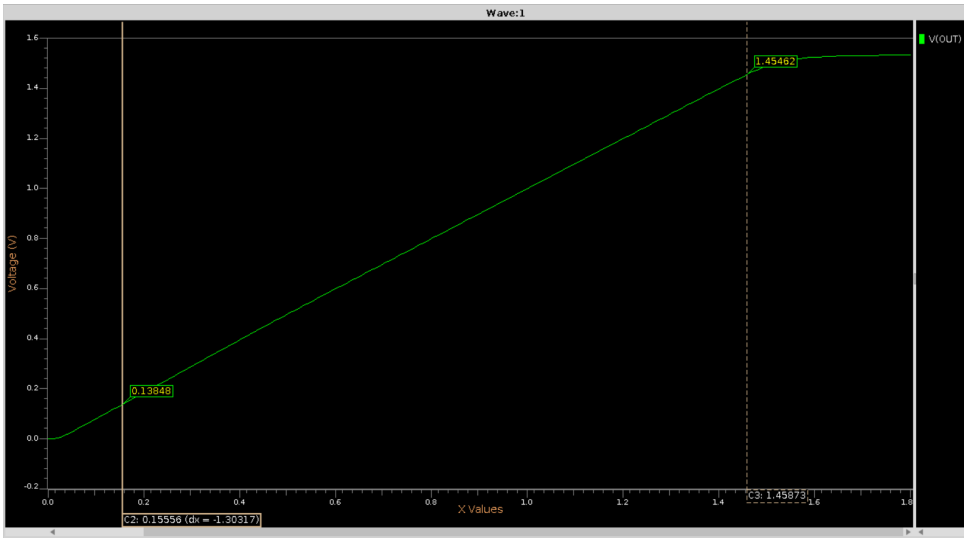

Figure 14: ICMR/OCMR of 2 stage OP AMP

From above graph we get ICMR

$$ICMR_{max} = 1.4$$
$$ICMR_{min} = 0.155$$

From above graph we get OCMR

$$OCMR_{max} = 1.45$$
$$OCMR_{min} = 0.138$$

5 Results

5.1 (W/l) of all transistors

transistor	width	length
M1	20.768um	180 nm
M2	20.768um	180 nm
M3	2.106um	180 nm
M4	2.106um	180 nm
M5	1.052um	180 nm
M6	42.31um	180 nm
M7	10.584um	180 nm
C3	2.104um	180 nm

5.2 capacitors

capacitor	values (pF)
C_c	3.2
C_L	10

5.3 design specifications

variable	Theoretical	practical
gain	$\geq$ 40dB	58.058 dB
GBW	$\geq$ 10Mhz	10.029Mhz
PM	$\geq$ 60	60.964
slew rate	$\geq$ 1	3.32
power	$\leq$ 250 μW	235.35 μW
ICMR	0.6 -1.4	0.16 - 1.4
OCMR	—-	0.133 - 1.45
Bandwidth	—-	13.26Khz
CMRR	—-	62.038dB
PSRR	—-	-0.3014dB

6 CONCLUSION

- designed and implemented 2 stage OP amp for low power consumption.
- To make system more stable , we have used the dominant pole concept.
- we have used the miller capacitance theory to realize the dominent pole concept.
- toatl current used in circuit is 130 μA which is less than the 138.88 μA to meet power specification.
- consumed very less power than given specification.so the design is optimized for power.
- Phase margin assumption and practical value which is 60 degrees satisfied.
- all the results which are given satisfied compared to given specification.
- All the results obtained practically and theoretically matched