# EE517 ANALOG IC DESIGN LAB
## Experiment 8

## Design a fully differential folded cascode single-stage opamp

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March 23, 2024

# Contents

# 1 Experiment

Design a fully differential folded cascode single-stage opamp

# 2 Objective

To find W/L, gain bandwidth product, output swing, ICMR, and compare the practical and theoretical results.

## 2.1 Design Specification

- Target gain is =2000
- Differential output swing 1.8.
- Power dissipation $\leq 0.12\ \mu$W
- CL = 10pF
- Technology=180 nm
- VDD= 1.8V

## 2.2 Observations

### 2.2.1 DC analysis

- Report the schematic of the diff pair with DC OP point annotated: Id, Vgs, Vds, Vth, Vdsat, gm, gds, gmb, region.
- Check that all transistors operate in saturation.

### 2.2.2 AC analysis

- Observe pole-zero analysis of your circuit.
- Frequency response of your circuit.
- Find Av, PM, Bandwidth, CMRR, PSRR.
- Give a proper reason for selecting any value of any parameter.

#### 2.2.3 Transient Analysis

- slew rate.
- ICMR, OCMR.

# 3 Theory

## 3.1 Some Definitions:

### 3.1.1 Transconductance($\mathbf{g_m}$)

It show us how productively a device converts voltage variation in input to current variation in output.In Mosfet input voltage applied at gate to source and output current si drain current .so It is the rate of change of drain current with respect to change in Gate-Source voltage.

$$g_m = \frac{dI_{ds}}{dV_{gs}} \tag{1}$$

### 3.1.2 voltage Gain $\mathbf{A_v}$:

Voltage gain is the one of the important parameter in AC analysis.It tells how much input amplifies by the circuit.generally we find out voltage gain by divide the small signal volatge output by the small signal voltage input.so maximum value of gain in the bode plot of gain treated as the voltage gain of the circuit.

$$A_v = \frac{v_{out}}{v_{in}} \tag{2}$$

### 3.1.3 Cut off frequency $\mathbf{f_c}$:

cut off frequency is up to which we have the half power .because to get proper gain we need atleast half power. It is also called the 3db frequency ,because half power means we need to have the 70 percentage of Voltage .we are going to plot the gain versus frequency graph which is the bode plot. so it will be frequency at which gain will the 3db less tahn the maximum value of gain.

cutt off frequency= $\text{frequency}_{\text{at 3db less than maximum gain}}$

$$Bandwidth = \frac{1}{2\pi R_{out} C_{OUT}} \tag{3}$$

### 3.1.4 Source Drain resistance($\mathbf{R_{ds}}$)

In a MOSFET output resistance is one of the important parameter.It is used for analysis the gain of the circuit and also useful to design the current source.To find out the output resistance we can use the Channel length modulation parameter($\lambda$) and $I_d$ at VGS-$V_{th}$.

$$r_{ds} = \frac{V_A}{I_{ds}} \tag{4}$$

### 3.1.5 Output Resistance resistance($\mathbf{R_{out}}$)

In a MOSFET output resistance is one of the important parameter.we need to have proper ouput resistance , because depends on that out put resistance amount of output will be reached to the Load circuit.To find out the output resistance of a circuit.we need to connect one test ac current souce at output and done the ac analysis find the output voltage .then fraction of test voltage to test current will be the output resistance.

$$R_{out} = \frac{v_{test}}{I_{test}} \tag{5}$$

### 3.1.6 Slew Rate

Maximum Rate of change of output per micro second ,we treated as the slew rate.but in differential amplifiers we got maximum output when whole tail current is passing through one side.
General formula for slew rate is

$$slewrate = (\frac{dV_{out}}{dt})_{max} \tag{6}$$

### 3.1.7 ICMR

ICMR nothing but Input common mode Range .generally it is defined as range of common mode input we can applied to that circuit then all transistors in saturation.Maximum ICMR means Maximum values of common mode input we can apply.

### 3.1.8 GBWP

Gain Band Width Product ,of an amplifier nothing but ,product of Open Loop gain times frequency range at which amplifier gain attenuated to -20dB.

### 3.1.9 PSRR

CMRR nothing but power supply rejection ratio. It tell ability to maintain same output voltage by varying the supply voltage.it should be very high in case of op amp. because we need less change in output as small change in vcc

$$PSRR = \frac{\Delta V_{cc}}{\Delta V_{out}} = inifite|_{idealcase} \tag{7}$$

### 3.1.10 PSRR

CMRR nothing but common mode rejection ratio. It tell how much common mode gain less with respect to the differential gain. so we need as much of as high CMRR means we need high differential gain and minimum common mode gain.

$$CMRR = \frac{A_{diff}}{A_{comm}} = inifite|_{idealcase} \tag{8}$$

## 3.2 Fully differential folded cascode single-stage opamp

First we need to know full differential and differential amplifier difference.full differential amplifier means double ended output ,where as differential amplifier is single ended output.For gain stage we go for the telescope op amp but ,we have some issues in that ,one is have very less output swing and second is we have difficulties use for the unit gain op amp configuration. So we are going to the use the Folded cascode structure In structure is same as telescope ,but connected two transistors as parallel to the top PMOS and we use give tail current to parallel connected transistors .By using this structure ,we are going to reduce the one mosfet in the stack,so we have little bit more OCMR compared to the telescope.Due to this we can use it for unit gain configuration.

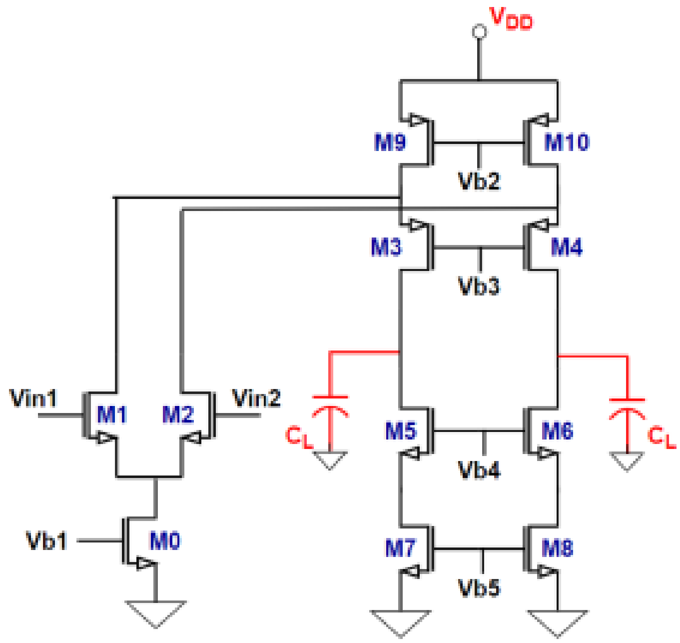


Figure 1: fully differential folded cascode single stage OPAMP

But in this experiment we have used only one reference source which is used for the biasing the circuit .so we have used one current mirror of PMOS to bias the top pmos.we called this structure as folded because ,here current will folded to stack and input transistors.

$$A_V = -gm_1(gm_5rds_5rds_3||gm_7rds_7(rds_9||rds_1)) \tag{9}$$

# 4 Telescope OP -AMP design

## 4.1 Design procedure

### 4.1.1 Step 1

Given in the question power dissipation is $\leq 0.12\ \mu$ W.from above circuit total we draw the current into two branches .which is current through Mb1 and M9.

$$(I_{mb1} + I_{M9})1.8 \leq 0.12\mu A \tag{10}$$

$$(I_{M9} + I_{M10}) \leq 66.66\mu A \tag{11}$$

so we have taken only 60 $\mu$A .

$$(I_{M9} + I_{M10}) = 60\mu A \tag{12}$$

we segregate the current

$$I_{\mathrm{M9}} + I_{\mathrm{M10}} = 60\mu A$$
$$I_{\mathrm{M9}} = 30\mu A$$
$$I_{\mathrm{M10}} = 30\mu A$$

so i am going to assign 10$\mu$ A to cascode branch and remaining 10$\mu$ A to input branch.

$$I_{M3,M4,M5,M6,M7,M8} = 10\mu A$$
$$I_{M9,M10} = 30\mu A$$
$$I_{M1,M2} = 20\mu A$$
$$I_{M0} = 40\mu A$$

#### 4.1.2 Step 2

In this experiment they given swing of Differential output swing is 1.8V.so

$$2(v_{DD} - (V_{OD9} + V_{OD5} + V_{OD3} + V_{OD7})) = 1.8$$
$$((V_{OD9} + V_{OD5} + V_{OD3} + V_{OD7}) = 0.9$$

As M9 holds more current we going to assign more over drive voltage as 0.3v. In remaining voltage 0.6 we have equally segregate to remaining mosfets in a stack.

$$V_{0D9} = 0.3$$
$$V_{0D7} = 0.2$$
$$V_{0D5} = 0.2$$
$$V_{0D3} = 0.2$$

We know we are using this amplifier mostly for unit gain configuration.so we treated ICMR as OCMR.so we know OCMR range is.

$$OCMR_{max} = V_{DD} - (VOD9 + VOD3) = 1.3v$$
$$OCMR_{min} = (VOD5 + VOD7) = 0.4v$$
$$OCMR_{Avg} = 0.85$$

now OCMR average we taken as input voltage and i am going to assign 0.2 v as over drive voltage for M0 mosfet.which means

$$V_{gs2} + V_{OD0} = 0.85$$
$$V_{OD0} = 0.2$$
$$V_{gs2} = 0.65$$
$$V_{OD2} = V_{gs2} - V_{th} = 0.65 - 0.55 = 0.1$$

So we got

$$V_{OD1,OD2} = 0.2$$
$$V_{OD0} = 0.1$$

#### 4.1.3 Step 3

so we have the all the over drive voltages , now we are going to find the aspect ration of all the transistors.as we assumed that all M5,M6,M7,M8 are identical , M3 and M4 identical , M9 and M10 identical and M1 and M2 identical.

**ASPECT RATIO**

**M9 and M10**

we know the current and overdrive voltage so we will get the aspect ratio.

$$30 * 10^{-6} = 0.5 * 137.12 * 10^{-6} * \frac{W}{L} * 0.3^2 \tag{13}$$

$$\frac{W}{L}_{M9,M10} = 4.859 \tag{14}$$

**M3 and M4**

$$10 * 10^{-6} = 0.5 * 137.12 * 10^{-6} * \frac{W}{L} * 0.2^2$$
$$\frac{W}{L}_{M3,M4} = 3.644$$

**M5,M6,M7 and M8**

$$10 * 10^{-6} = 0.5 * 342.18 * 10^{-6} * \frac{W}{L} * 0.2^2$$
$$\frac{W}{L}_{M5,M6,M7,M8} = 1.461$$

**M1 and M2**

$$20 * 10^{-6} = 0.5 * 342.18 * 10^{-6} * \frac{W}{L} * 0.1^2$$
$$\frac{W}{L}_{M1,M2} = 11.696$$

**M0**

$$40 * 10^{-6} = 0.5 * 342.18 * 10^{-6} * \frac{W}{L} * 0.2^2$$
$$\frac{W}{L}_{M0} = 5.84$$

so we got the all aspect ratios .so now we are going to find out the dc values of all the mosfets.

**BIAS VOLATGES**

**M0:**

we know the over drive voltage of M0 ,so

$$V_{OD0} = 0.2$$
$$V_{Gs0} - V_{th0} = 0.2$$
$$V_{G1} - 0.55 = 0.2$$
$$V_{G1} = 0.75$$

**M1 and M2:**
we now source voltage of M1 ,is nothing but drain voltage of M0 .which is 0.2.and we know overdrive voltage of 0.1.

$$V_{0D1} = 0.1$$
$$V_{Gs1} - V_{th1} = 0.1$$
$$V_{G1} - V_{S1} - V_{th1} = 0.1$$
$$V_{G1} - 0.2 - 0.55 = 0.1$$
$$V_{G1} = V_{G2} = 0.85$$

**M9 and M10**
we now source voltage of M9 ,is nothing but Vdd. and we know overdrive voltage of 0.3.

$$V_{OD9} = 0.3$$
$$V_{SG9} - V_{th9} = 0.3$$
$$V_{S9} - V_{G9} - V_{th9} = 0.3$$
$$1.8 - V_{G9} - 0.55 = 0.3$$
$$V_{G9} = V_{G10} = 0.95$$

**M3 and M4:**
we now source voltage of M3 ,is nothing but drain voltage of M9 which is 1.5 and we know overdrive voltage of 0.2.

$$V_{OD3} = 0.2$$
$$V_{SG3} - V_{th3} = 0.2$$
$$V_{S3} - V_{G3} - V_{th3} = 0.2$$
$$1.5 - V_{G3} - 0.55 = 0.2$$
$$V_{G3} = V_{G4} = 0.75$$

**M7and M8**

we know the over drive voltage of M7 which is 0.2v ,so

$$V_{OD7} = 0.2$$
$$V_{Gs7} - V_{th7} = 0.2$$
$$V_{G7} - 0.55 = 0.2$$
$$V_{G7} = V_{G8} = 0.75$$

**M5 and M6**

we now source voltage of M5 ,which is nothing but drain voltage of M7 which is 0.2. and we know overdrive voltage of 0.2.

$$V_{0D5} = 0.2$$
$$V_{Gs5} - V_{th5} = 0.2$$
$$V_{G5} - V_{S5} - V_{th5} = 0.2$$
$$V_{G5} - 0.2 - 0.55 = 0.2$$
$$V_{G1} = V_{G2} = 0.95$$

we know the all the dc voltage at gate we need to apply now we are going to find the gain.

#### 4.1.4 Step 4-

so if you take minimum length of mosfet 180nm ,then early voltage is 0.9.so then $\mathrm{r_{ds}}$

$$r_{ds} = \frac{V_A}{I_D}$$
$$r_{ds5,ds7,ds3} = 90K\Omega$$
$$r_{ds9} = 30K\Omega$$
$$r_{ds1} = 45K\Omega$$

and trans conductance will be

$$gm_1 = \frac{2I_{D1}}{V_{OD1}} = 400\mu\mho$$
$$gm_5 = \frac{2I_{D5}}{V_{OD5}} = 100\mu\mho$$
$$gm_3 = \frac{2I_{D3}}{V_{OD3}} = 100\mu\mho$$

if you substitute the above values in gain equation 9.

$$A_V = 53.6 \tag{15}$$

to increase the gain ,we are going to increase the $\mathrm{r_{ds}}$ .so we increase the length of M0,M3,M4,M5,M6,M7 and M8 1440nm and M1,M2,M9 and M10 to 1800nm.gain will be .

$$A_V = 4147 \tag{16}$$

## 4.2 DC Analysis

### 4.2.1 schematic

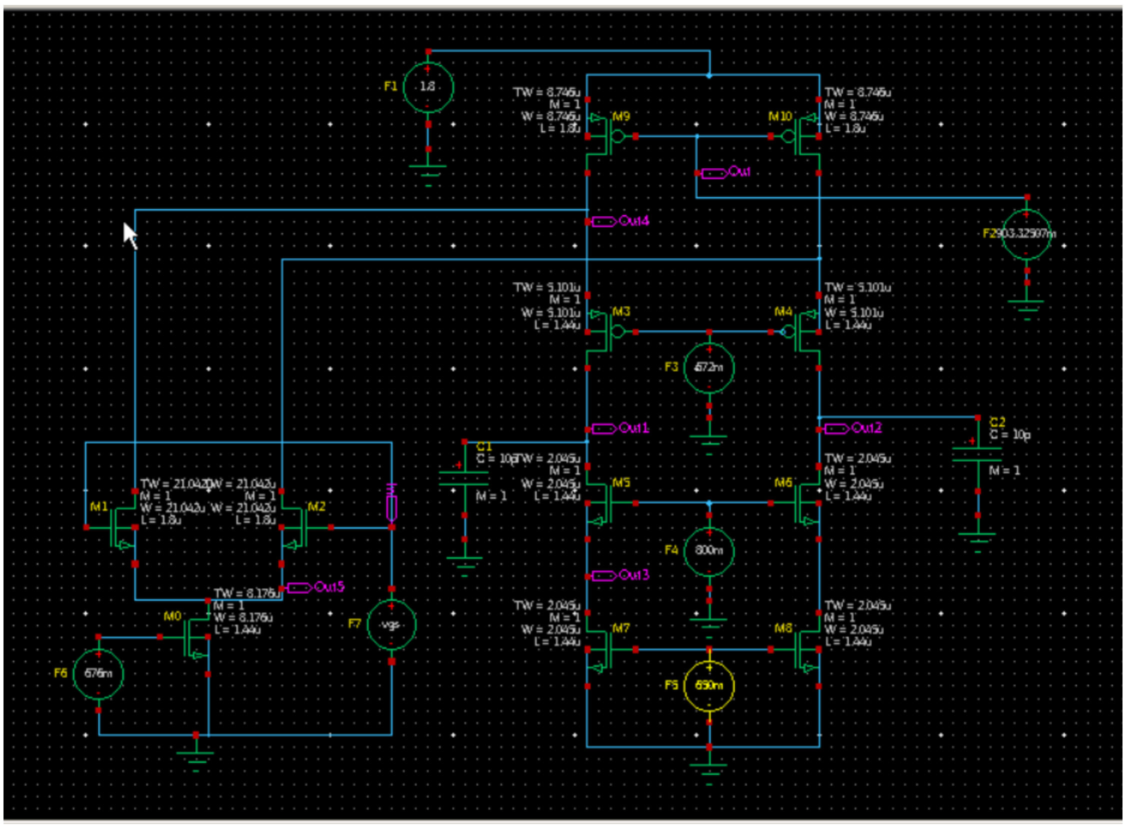

Figure 2: schematic of DC analysis of folded cascode amplifier

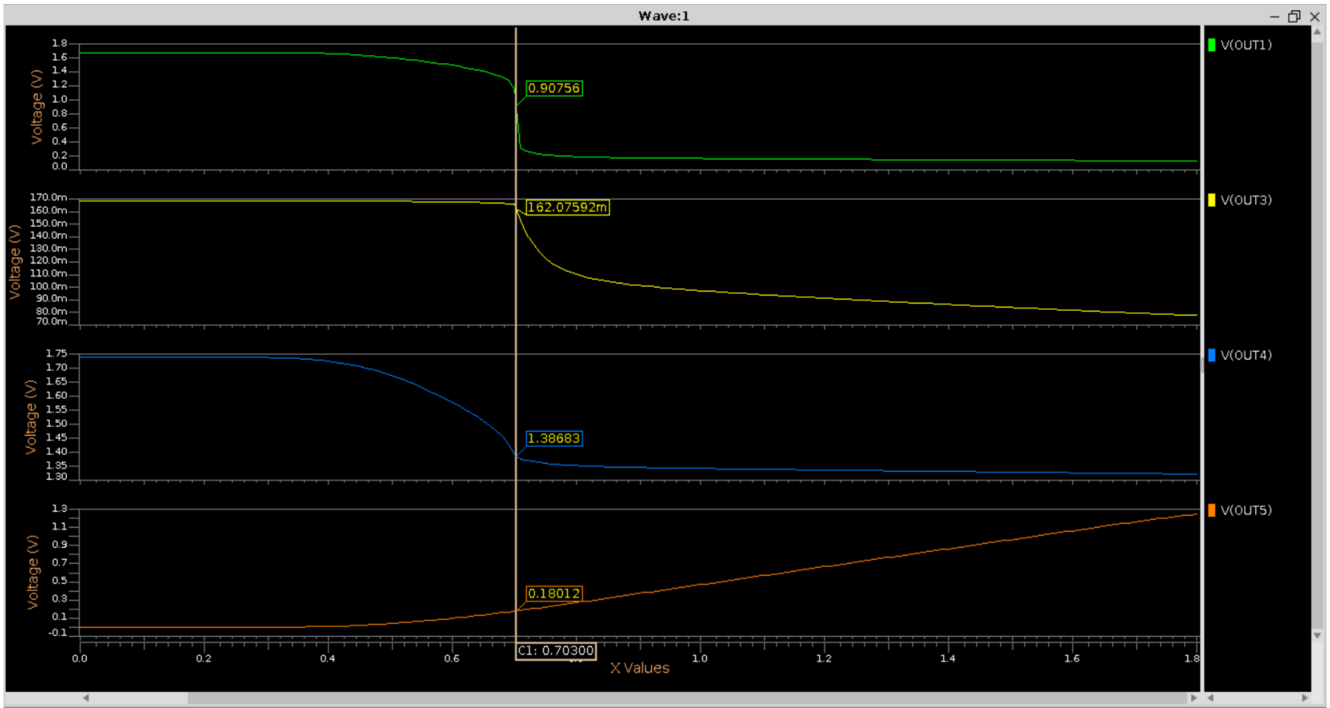


Figure 3: DC analysis of voltages folded cascode amplifier

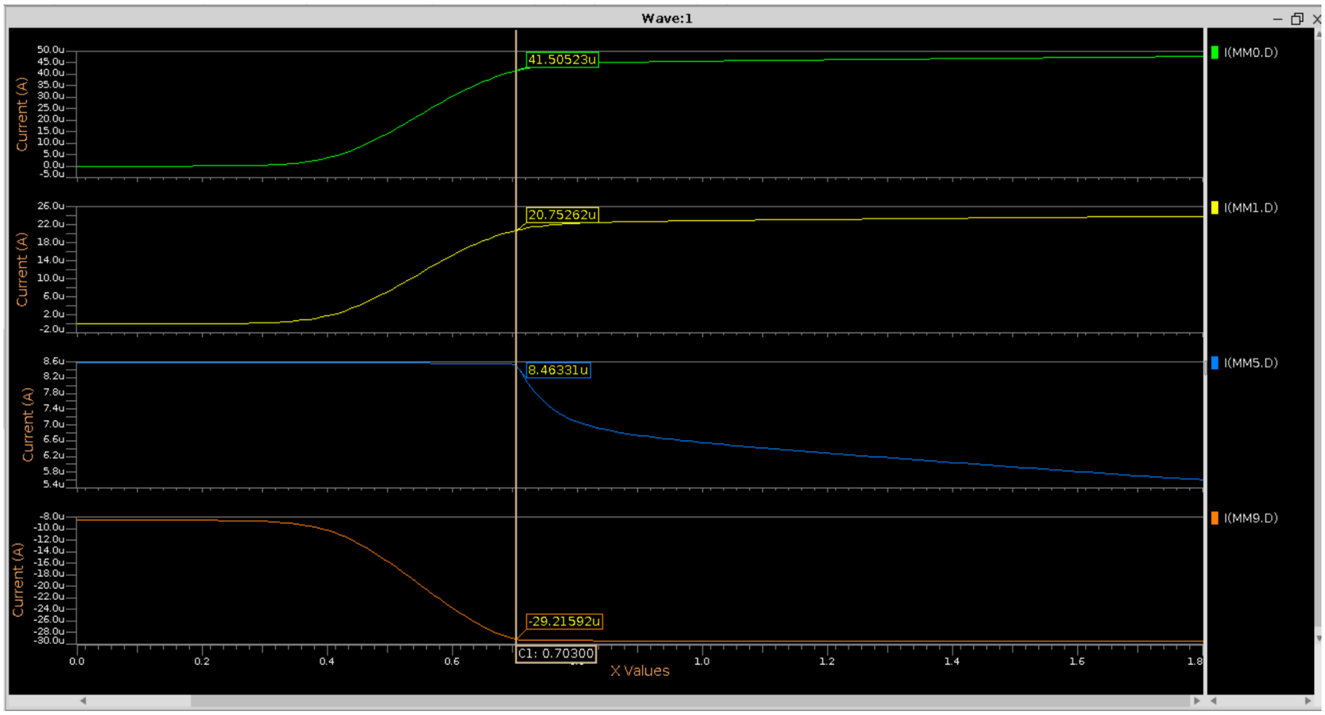


Figure 4: DC analysis of currents folded cascode amplifier

### 4.2.2 DC observations

we are going to check the transistors are saturation are not
**M0:**

$$V_D > V_G - V_{th}$$
$$0.180 > 0.676 - 0.55$$

So it is saturation.
**M1 and M2:**

$$V_D > V_G - V_{th}$$
$$1.386 > 0.703 - 0.55$$

So it is saturation.
**M7 and M8:**

$$V_D > V_G - V_{th}$$
$$0.162 > 0.650 - 0.55$$

So it is saturation.
**M5 and M6:**

$$V_D > V_G - V_{th}$$
$$0.9 > 0.8 - 0.55$$

So it is saturation.
**M3 and M4:**

$$V_{SD} > V_{sG} - V_{th}$$
$$1.386 - 0.9 > 1.386 - 0.672 - 0.55$$
$$0.479 > 0.161$$

So it is saturation.
**M9 and M10:**

$$V_{SD} > V_{sG} - V_{th}$$
$$1.8 - 1.386 > 1.8 - 0.903 - 0.55$$
$$0.414 > 0.347$$

So it is saturation.

## 4.3 AC Analysis

### 4.3.1 schematic

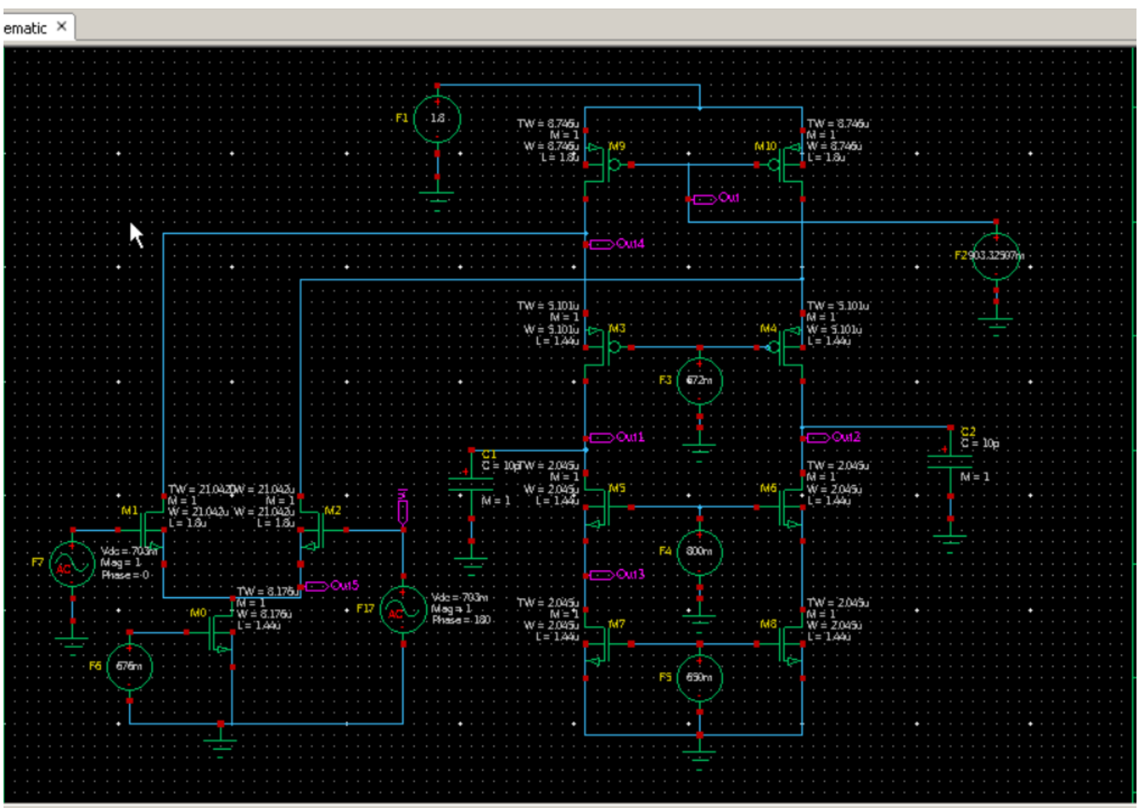


Figure 5: schematic of AC analysis of folded cascode amplifier

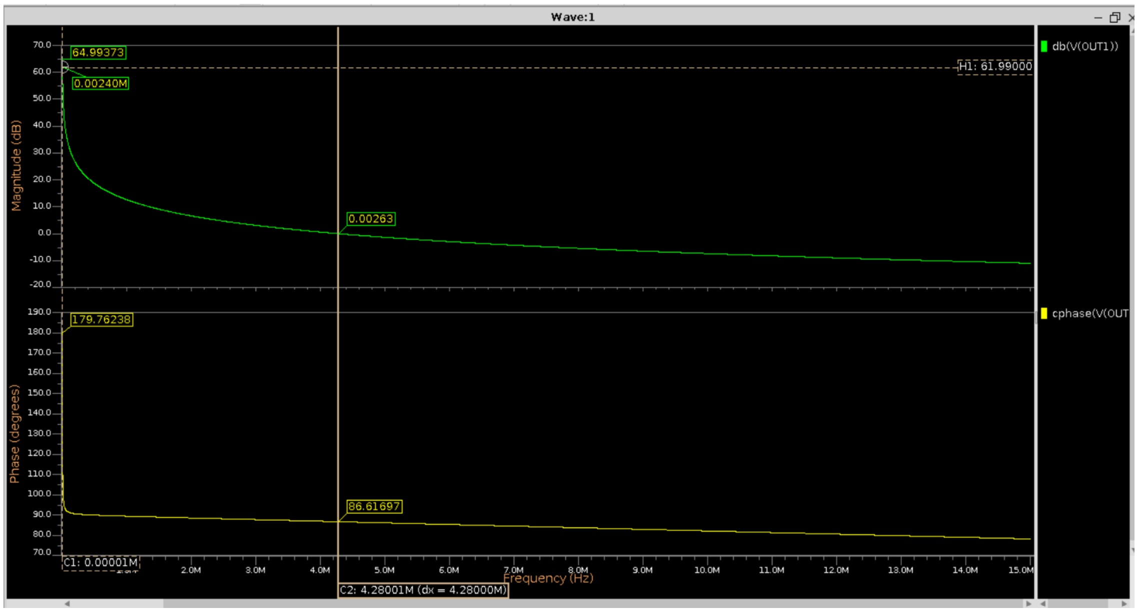


Figure 6: AC analysis of folded cascode amplifier

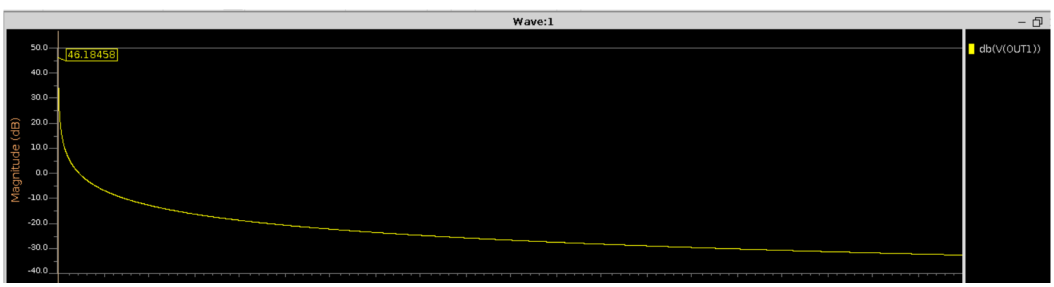


Figure 7: Common Mode gain of folded cascode amplifier

### 4.3.2 PSRR

To calculate PSRR ,we have taken the unity feed back and at inverting terminal .we applied the dc bias voltage at non inverting terminal .which make NMOS on.Then we have to apply the ac source at the VDD and taken output will give the PSRR

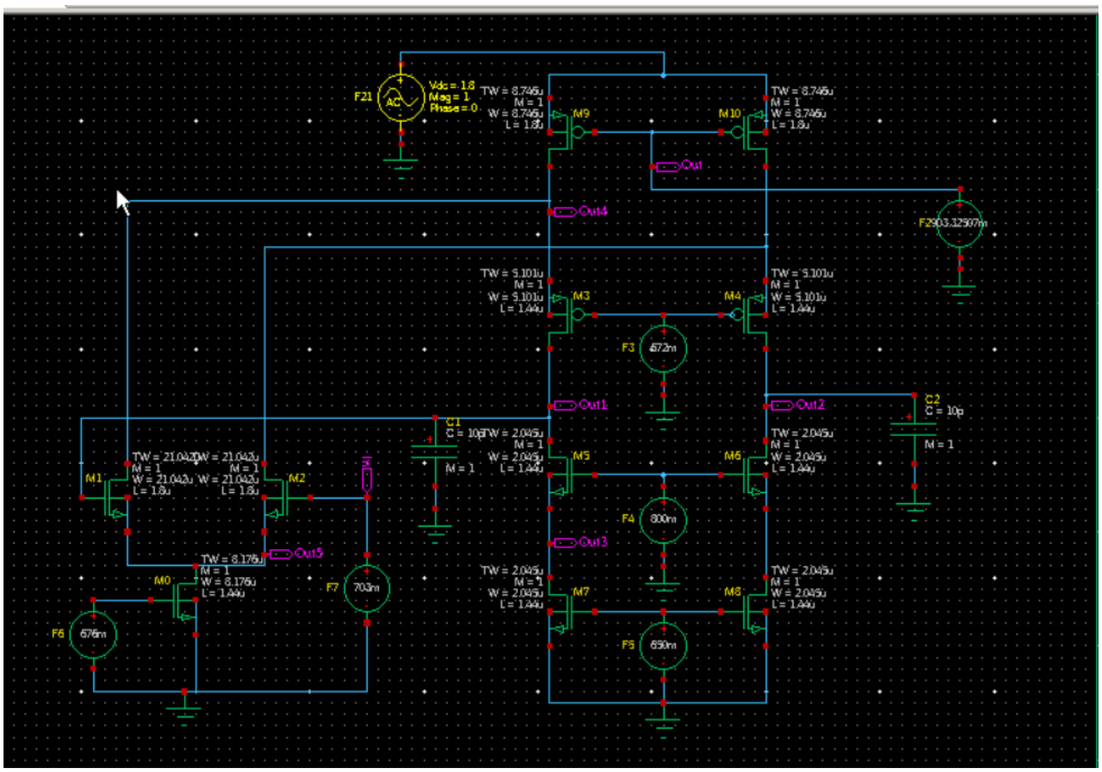

Figure 8: schematic of PSRR analysis of folded cascode amplifier

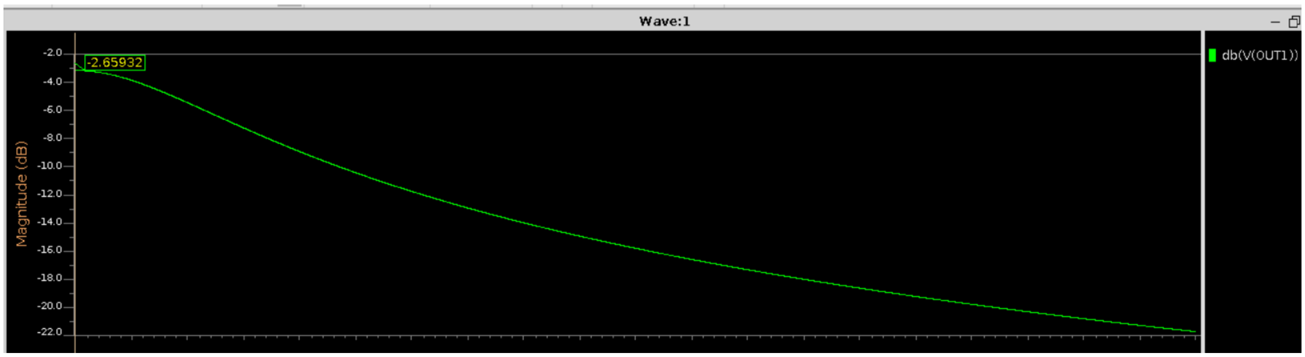


Figure 9: PSRR of folded cascode amplifier

### 4.3.3 AC observations

we got gain of the designed folded cascode amplifier.

$$A_V = 64.99dB \tag{17}$$

we got the 3 db frequency

$$bandwidth = 0.0024Mhz \tag{18}$$

we got the gain bandwidth product

$$GBW = 4.28Mhz \tag{19}$$

we got phase margin

$$PM = 86.61 \tag{20}$$

we got common mode gain little bit high ,beacuse of less tail current resistance ,we passing high current in whole circuit.

$$A_{CM} = 46dB \tag{21}$$

we got PSRR

$$PSRR = -2.65dB \tag{22}$$

## 4.4 Transient Analysis

### 4.4.1 SLEW rate

we know slew rate will be ,maximum rate of change of output.so we have applied the pulse signal at the input and checked the output.

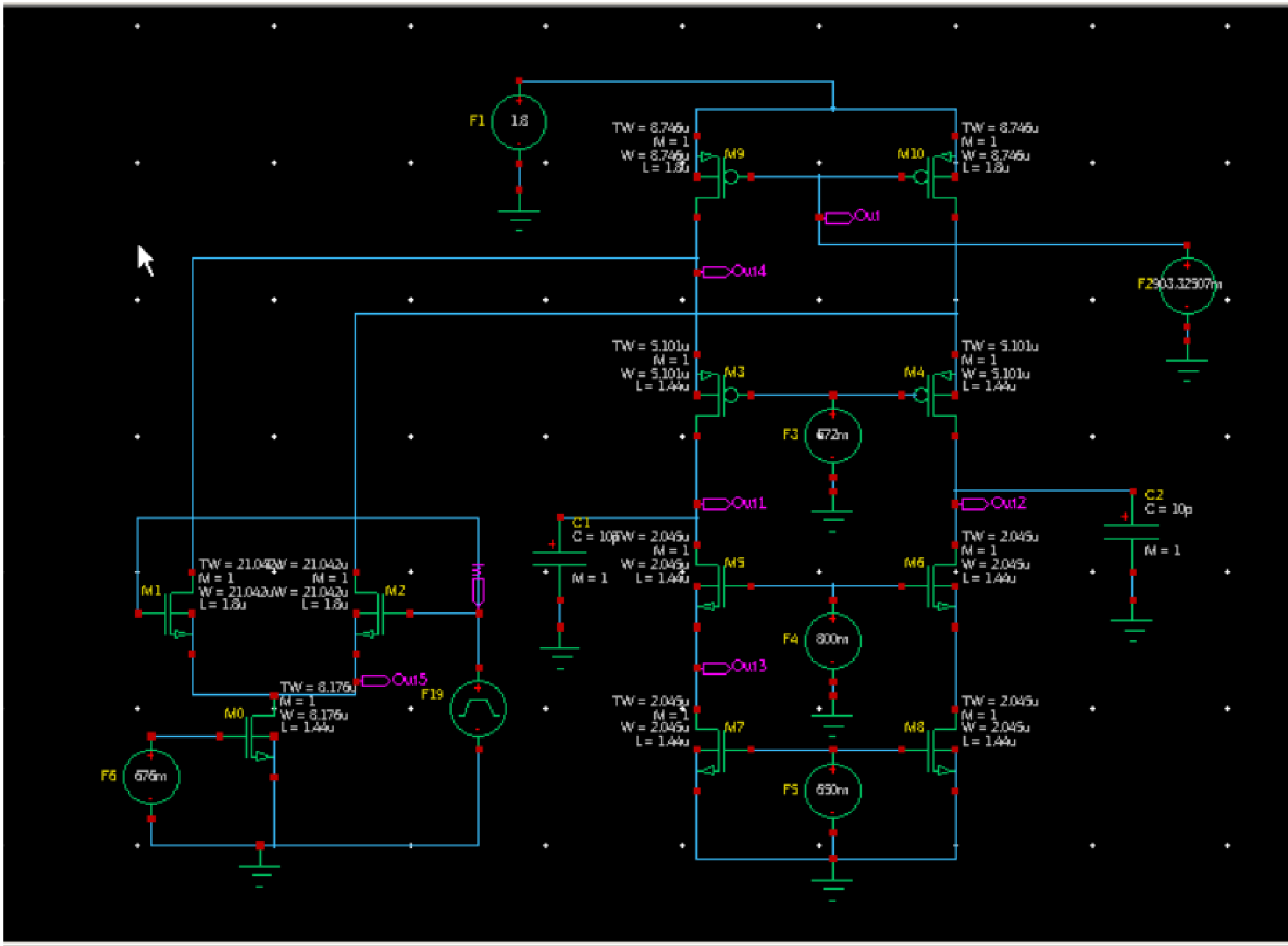


Figure 10: schematic for slew rate of folded cascode amplifier

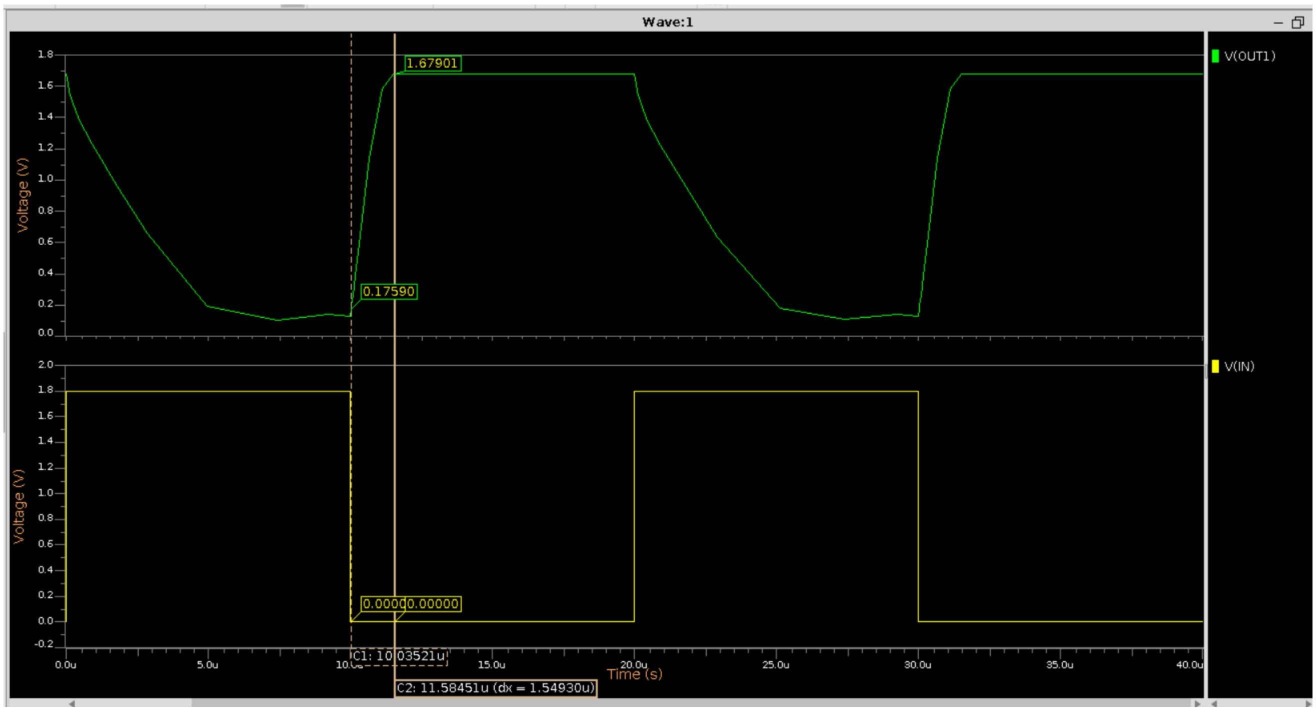


Figure 11: slew rate of folded cascode amplifier

we got slew rate

$$slewrate = 0.970\frac{V}{\mu s} \tag{23}$$

### 4.4.2 ICMR and OCMR

we are taken the unit gain amplifier model ,so ICMR Aand OCMR same .so we have given the negative feed back and apply the DC sweep at the non inverting terminal.then we need to check the output .upto some input range it is in linear those range given as ICMR and saturation output will be the OCMR.

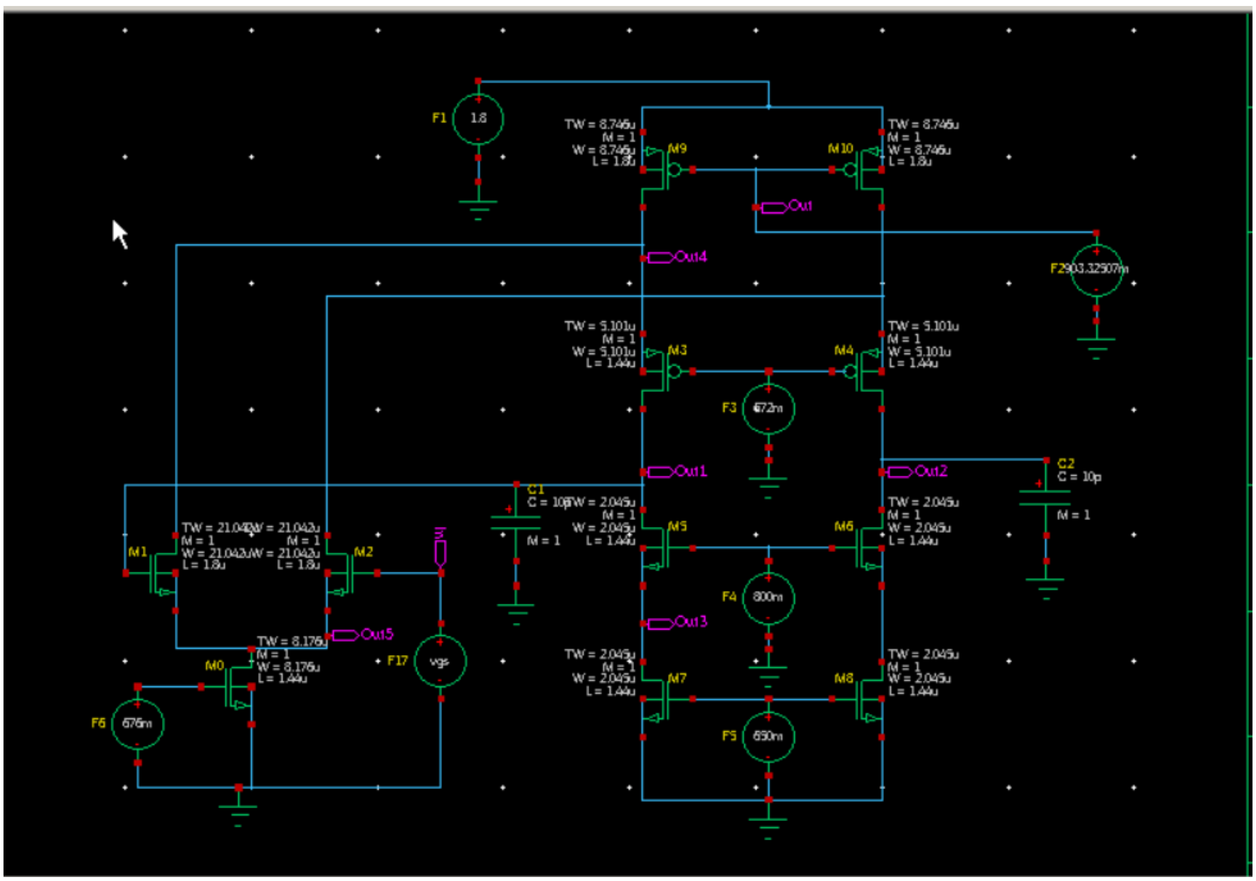


Figure 12: schematic for ICMR/OCMR of folded cascode amplifier

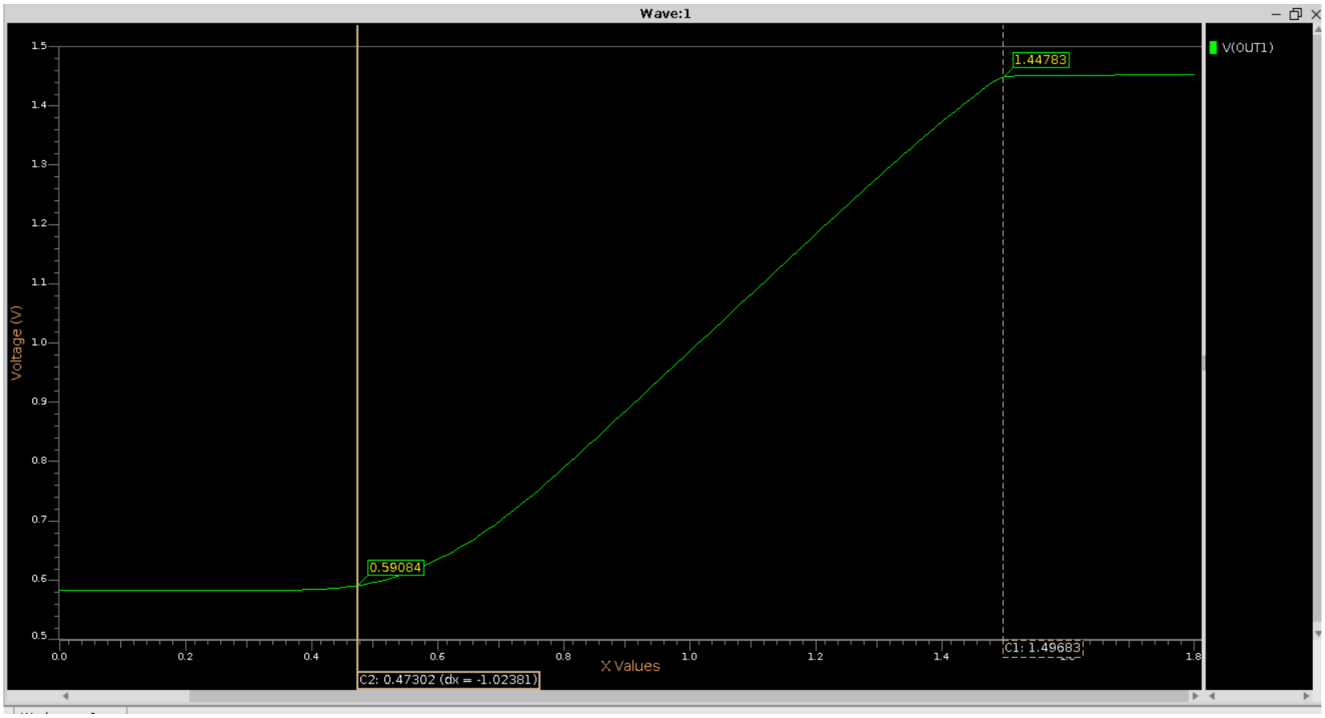


Figure 13: ICMR/OCMR of folded cascode amplifier

From above graph we get ICMR

$$ICMR_{max} = 1.496$$
$$ICMR_{min} = 0.473$$

From above graph we get OCMR

$$OCMR_{max} = 1.447$$
$$OCMR_{min} = 0.590$$

# 5 Results

## 5.1 (W/l) of all transistors

| transistor | aspect ration | width | length $\mu$ |
|---|---|---|---|
| M0 | 5.84 | 1440 nm | 8176 nm |
| M1 | 11.690 | 1800 nm | 21042 nm |
| M2 | 11.690 | 1800 nm | 21042 nm |
| M3 | 3.644 | 1440 nm | 5241 nm |
| M4 | 3.644 | 1440 nm | 5241 nm |
| M5 | 1.461 | 1440um | 2103nm |
| M6 | 1.461 | 1440um | 2103nm |
| M7 | 1.461 | 1440um | 2103nm |
| M8 | 1.461 | 1440um | 2103nm |
| M9 | 4.859 | 1800 nm | 8745 nm |
| M10 | 4.859 | 1800 nm | 8745 nm |

## 5.2 Bias voltages of transistors

| transistor | Theoretical $V_G$ | practical $V_G$ | $V_{GS}$ | $V_{DS}$ | $I_D$ |
|---|---|---|---|---|---|
| M0 | 0.75 | 0.676v | 0.676 | 0.18 | 41.502 $\mu$A |
| M1 | 0.85v | 0.703v | 0.523v | 1.206 | 20.752 $\mu$A |
| M1 | 0.85v | 0.703v | 0.523v | 1.206 | 20.752 $\mu$A |
| M3 | 0.75v | 0.672v | -0.714v | -0.479 | -8.463 $\mu$A |
| M4 | 0.75v | 0.672v | -0.714v | -0.479 | -8.463 $\mu$A |
| M5 | 0.95 | 0.8 | 0.638 | 0.745 | 8.463 $\mu$A |
| M6 | 0.95 | 0.8 | 0.638 | 0.745 | 8.463 $\mu$A |
| M7 | 0.75 | 0.65 | 0.65 | 0.162 | 8.463 $\mu$A |
| M8 | 0.75 | 0.65 | 0.65 | 0.162 | 8.463 $\mu$A |
| M9 | 0.95 | 0.903 | -0.897 | -0.414 | -29.215$\mu$A |
| M10 | 0.95 | 0.903 | -0.897 | -0.414 | -29.215$\mu$A |

### 5.3 AC results

| Variable | practicalvalue |
|---|---|
| gain | 64.99 dB |
| bandwidth | 0.0024Mhz |
| GBW | 4.28 Mhz |
| PM | 86.61 |
| CMRR | 20dB |
| PSRR | -2.65dB |

### 5.4 Transient results

| Variable | theoretical value | practicalvalue |
|---|---|---|
| slew rate | 1 | 0.97 |

| variable | max | min |
|---|---|---|
| ICMR | 1.496 | 0.473 |
| OCMR | 1.447 | 0.59 |

## 6 CONCLUSION

- designed and implemented folded cascode amplifier for high swing and high gain.
- we have good ICMR and OCMR compared to telescope amplifier
- so we can use it as unit gain amplifier
- if you connect it as the unit gain configuration ,we got high capacitance compared to the telescope.so we got dominant pole here so we got very less bandwidth.
- All the results obtained practically and theoretically matched