

REVIEW OF THE IBM DEEP BLUE PAPER

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INTRODUCTION:

The Deep Blue paper describes the design and architecture of the Deep Blue II system, and the rationale behind some of the architectural decisions.

There are two distinct versions of Deep Blue; one developed during 1996, and another during 1997. The 1996 version (Deep Blue I) lost 4-2 to Garry Kasparov, while the 1997 version (Deep Blue II) is the famous one that defeated Kasparov 3.5-2.5.

IMPROVEMENTS:

After the initial loss in 1996, several improvements were made (as can be seen in Table 1). The chess chips were redesigned for efficiency, while adding hardware repetition detection, and specialized move generation modes (e.g. generate all moves that attack). The team also concluded that the searching ability of Deep Blue I was good enough, and focused their efforts on debugging, match preparation, and feature tuning.

TABLE 1

	Deep Blue I	Deep Blue II
Single chess chips	216	480
Nodes (processors)	36	30
Feature groups	32	38
Features	6400	8000
Positions/second/chip	1.6 – 2 million	2 – 2.5 million
Positions/second	50 – 100 million	100 – 200 million

NO-PROGRESS PRUNING:

A novel idea used was a pruning mechanism called "no progress". The assumption was that if a move is good for a given side, it is best to play it early rather than late. This was implemented by detecting if the current position could have been reached by playing an alternate move at an earlier position in the search path; if so, the search is terminated with a fail low. The authors note that this has limited effect in most positions, but that there are noticeable benefits when there are few pieces left (during end-games).

HARDWARE DESIGN:

At a hardware level, Deep Blue II had a master node, and 29 worker nodes. Each node controls 16 chess chips, and have access to 1GB RAM and a 4GB disk.

The master node searches the top-level of the game tree, and distributes leaf positions to the workers. Workers carry out a few levels of additional search, and distribute their leaf positions to their chips which search the last few levels.

Multiple game books were also used during the design of the chess chips (the chip ROMs had stored patterns). The endgame books were replicated on disks of the individual nodes, and all the game books were stored on two 20GB raid disk arrays that were available to all the nodes.

SUCCESS FACTORS:

The major factors that contributed to the success of Deep Blue II can be summarized as:

- ◆ Single-chip chess search engine:
The chip generates moves via a 8x8 array of combinatorial logic, and uses a combination of a slow and a fast evaluation function to pick a move.
- ◆ Massively (multi-level) parallelism:
Over 500 processing units are available for searching; for early iteration, the master node can search using its 16 chess chips, and distribute the workload for later iterations.
- ◆ Search improvements:
A combination of hardware and software search was used. Hardware search used null-window alpha-beta search (with quiescence) for simple, but fast searches. This was limited to 4-5 plies until endgame. Software search used depth-limited alpha-beta search with negamax.
- ◆ Complex evaluation function:
The evaluation function is implemented in hardware. Therefore, time to execute this function is always constant. There were 8000 features to tune, and this allowed fine-grained control over the function. However being hardware-based, adding new features was not possible.
- ◆ Effective use of game databases:
There were three game databases; an opening book, an extended book, and an endgame book.
 - The opening book was created by hand (in collaboration with multiple grandmasters), and had about 4000 positions.
 - The extended book summarized all the information available at each position of a 700,000 game database.
 - The endgame book included all chess positions with five or fewer pieces, and selected positions with six pieces.

CONCLUSION:

The authors conclude that success was not dependent on any one factor. All the aforementioned reasons combined to edge Deep Blue over Kasparov. They also note several avenues of improvement; namely improved parallelism, hardware search and evaluation could be more efficient/flexible with FPGAs, and improved performance via pruning mechanisms.