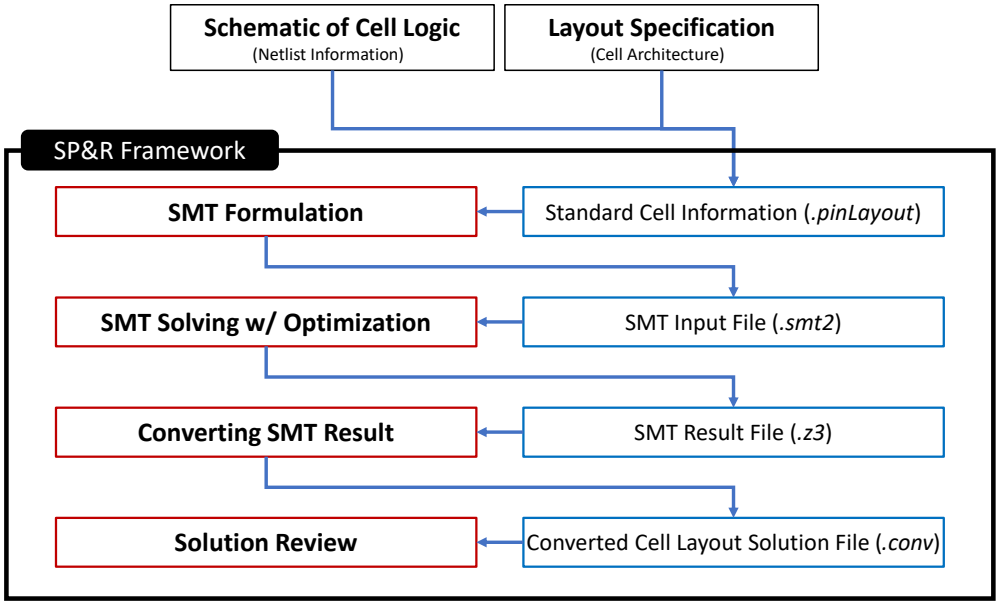
SMT-based Simultaneous Standard Cell Place-&-Route (SP&R) for PROBE 2.0

CK Research Group in UC San Diego
Email: ckcheng@ucsd.edu

1. Overview

This manual briefly summarizes the following flows to generate (i) SMT formulation file (*.smt2* file) and (ii) solution files to review the cell layout result. With the given standard cell information inputs (*.pinLayout* file) which are extracted from the ASAP7 PDK library[1], our flow generates the SMT formulation. We provide a solution viewer to validate the transistor placement and in-cell routing result of the SMT formulation. We employ Z3 (*Ver. 4.8.5*) [2] as our SMT solver. Please find more details from our papers [3][4].

(1) Flow Chart for Our Proposed Framework



(2) Contents in the TAR ball

```
(Current Path) ─┬─ /PNR_2F_4T/cmd_gen_smt
                │           /cmd_conv_solution
                │           /pinLayouts/AND2_X1.pinLayout … XOR2_X1.pinLayout
                │           /inputsSMT
                │           /RUN
                │           /scripts/convSMTResult_Ver1.0.pl
                │                   /genSMTInput_Ver1.0.pl
                │           /solutionsSMT/AND2_X1_2F_4T_EL_MPO2.conv … XOR2_X1_2F_4T_ET_MPO3.conv
                ├─ /PNR_3F_5T/cmd_gen_smt
                │           /cmd_conv_solution
                │           /pinLayouts/AND2_X1.pinLayout … XOR2_X1.pinLayout
                │           /inputsSMT
                │           /RUN
                │           /scripts/convSMTResult_Ver1.0.pl
                │                   /genSMTInput_Ver1.0.pl
                │           /solutionsSMT/AND2_X1_2F_4T_EL_MPO2.conv … XOR2_X1_2F_4T_ET_MPO3.conv
                └─ /PNR_3F_6T/cmd_gen_smt
                            /cmd_conv_solution
                            /pinLayouts/AND2_X1.pinLayout … XOR2_X1.pinLayout
                            /inputsSMT
                            /RUN
                            /scripts/convSMTResult_Ver1.0.pl
                                    /genSMTInput_Ver1.0.pl
                            /solutionsSMT/AND2_X1_2F_4T_EL_MPO2.conv … XOR2_X1_2F_4T_ET_MPO3.conv
```

2. Our Tool-Chain Scripts and Commands with User-Specified Options

Our tool-chain scripts are written in *Perl*. SMT solver is Z3 (*Ver. 4.8.5*). For the information of the Z3 solver, please visit the following link: https://github.com/Z3Prover/z3

** Z3 Solver has been frequently updated. We recommend to use the specific version V4.8.5*

(1) Input Standard Cell Information (`.pinlayout`)

We provide 39 typical standard cell information which are extracted from the ASAP7 PDK library. Based on the ASAP7's cell architecture (3 Fin / 6 Track), the number of routing tracks and the width of FETs have been scaled according to the target cell architecture of PROBE 2.0. The list of standard cells is as follows.

AND2_X1	AND2_X2	AND3_X1	AND3_X2	AOI21_X1
AOI21_X2	AOI22_X1	AOI22_X2	BUF_X1	BUF_X2
BUF_X4	BUF_X8	DFFHQNx1	INV_X1	INV_X2
INV_X4	INV_X8	MUX2_X1	NAND2_X1	NAND2_X2
NAND3_X1	NAND3_X2	NAND4_X1	NAND4_X2	NOR2_X1
NOR2_X2	NOR3_X1	NOR3_X2	NOR4_X1	NOR4_X2
OAI21_X1	OAI21_X2	OAI22_X1	OAI22_X2	OR2_X1
OR2_X2	OR3_X1	OR3_X2	XOR2_X1	

(2) SMT Formulation Generation (`genSMTinput_Ver1.0.pl`)

[Usage]

```
$ ./scripts/genSMTInput_Ver1.0.pl ./pinLayouts/DFFHQNx1.pinLayout [DesignRuleType Parameter (ET/EL)] [MPO Parameter (2/3)]
```

* DesignRuleType Parameter refers to the type of the design rule set. “ET” / “EL” are available parameters. “ET” denotes the “EUV-tight” case and “EL” denotes the “EUV-loose” case in PROBE 2.0. MPO Parameter sets the minimum pin opening of each standard cell (2/3 are valid).

* This package’s design rule parameters are simplified for the specific usage in PROBE 2.0. Please refer our papers [3][4] for further detailed information of a whole set of design rule parameters.

[Example]

Generating the SMT formulation file (*.smt2*) for the AND2_X1 standard cell “`AND2_X1.pinLayout`” with the design rule type “EUV-tight” and the minimum pin opening of 3.

```
$ ./scripts/genSMTInput_Ver1.0.pl ./pinLayouts/AND2_X1.pinLayout ET 3
```

This will create “`AND2_X1_2F_4T_EL_MPO3.smt2`” file in the `inputsSMT` directory. For the .smt2 file format, please visit the following link: https://rise4fun.com/z3/tutorialcontent/guide

(3) RUN SMT Solver (`Z3`)

[Usage]

```
SMT Solving & Storing solution
$ z3 inputsSMT/[inputFile(.smt2)] > RUN/[solutionName(.z3)]
```

[Example]

Running “`AND2_X1_2F_4T_EL_MPO3.smt2`” file and storing the result “`AND2_X1_2F_4T_EL_MPO3.z3`” to the output directory

```
$ z3 inputsSMT/AND2_X1_2F_4T_EL_MPO3.smt2 > RUN/AND2_X1_2F_4T_EL_MPO3.z3
```

(4) Solution Converter (`convSMTResult_Ver1.0.pl`)

[Usage]

```
$ ./scripts/convILPResult_Ver1.0.pl [solPath/solutionName]"
```

[Example]

Converting "AND2_X1_2F_4T_EL_MPO3.z3" output file to the solution output directory

```
$ ./scripts/convSMTResult_Ver1.0.pl RUN/AND2_X1_2F_4T_ET_MPO3.z3
```

This will create "[solutionName].conv" file in the solutionsSMT directory.

The converted solution files (*.conv*) can be reviewed using an excel-based solution viewer. The right solution viewer needs to be selected for each cell architecture type. (SolutionViewer_2F_4T.xlsm / SolutionViewer_3F_5T.xlsm / SolutionViewer_3F_6T.xlsm)

(5) Pre-described Command Lists

In each cell architecture directory (/PNR_2F_4T, /PNR_3F_5T, /PNR_3F_6T), there are "cmd_conv_solution", "cmd_gen_smt" files which consist of command lists to generate and convert the whole standard cells provided in this package. You can refer to the command file to execute each cell generation or sourcing the list file to execute all cases.

(6) Pre-generated Solution Results

In each cell architecture's solution directory (/PNR_2F_4T/solutionsSMT, /PNR_3F_5T/solutionsSMT, /PNR_3F_6T/solutionsSMT), there are pre-generated solution files (*.conv*) for all standard cells. Each solution file can be reviewed using the corresponding solution viewer.

3. References

[1] V. Vashishtha, M. Vangala, and L. T. Clark, "ASAP7 predictive design kit development and cell design technology co-optimization," in 2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 992–998, IEEE, 2017

[2] *Z3*, SMT Solver, https://github.com/Z3Prover/z3.

[3] D. Park, D. Lee, I. Kang, S. Gao, B. Lin, and C.-K. Cheng. "SP&R: Simultaneous Placement and Routing framework for standard cell synthesis in sub-7nm." In *2020 25th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 345-350. IEEE, 2020.

[4] C.-K. Cheng, D. Lee, and D. Park, "Standard-Cell Scaling Framework with Guaranteed Pin-Accessibility", *IEEE International Symposium on circuits and systems (ISCAS)*, October 2020 (to appear)