Quiz 04 - Requires Respondus LockDown Browser + Webcam

Due Dec 7 at 11:59pm **Points** 5 **Questions** 20
Available Dec 6 at 6am - Dec 7 at 11:59pm 1 day **Time Limit** 45 Minutes
Allowed Attempts 2 Requires Respondus LockDown Browser

Instructions

1. Lecture 19-23.
2. Open book / note quiz.
3. You can use your own blank scratch paper to solve problems.
4. You can use calculator.
5. You have total 45 minutes per attempt to complete this quiz.

[For respondus monitor system ID check, you can use tower card, library card, driving license or any other valid ID card]

This quiz was locked Dec 7 at 11:59pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	44 minutes	5 out of 5

ⓘ Correct answers are hidden.

Score for this attempt: **5** out of 5
Submitted Dec 7 at 5:50pm
This attempt took 44 minutes.

Question 1 — 0.25 / 0.25 pts

Arrange type of memory / data storage in descending order of their access time. Rank-1 is the slowest.

Rank Device Type

==========

1	[Select]
2	Memory Cards
3	Main Memory
4	[Select]
5	[Select]

Answer 1:

Magnetic Tape

Answer 2:

Memory Cards

Answer 3:

Main Memory

Answer 4:

Cache Memory

Answer 5:

Register Files

Question 2

0.25 / 0.25 pts

Regarding storage / memory select true statement(s)

- [ ] Magnetic tape storage is part of on-board storage in modern computers.
- [x] Cache memory is a type of associative memory
- [x] DRAM memory needs refresh cycle to regenerate data stored inside it.
- [x] Concept of access time is different in random vs. non random access memory.

- [ ] Cache memory is slower than main memory

Question 3

0.25 / 0.25 pts

What do(es) keep hit rate high in cache memory?

- [ ] Smaller block size
- [x] Temporal Locality
- [x] Bigger size cache memory, especially with full associative cache memory
- [ ] Higher clock speed for cache memory
- [x] Spatial Locality

Question 4

0.25 / 0.25 pts

A cache memory has 2ns access time with 450ns per miss. If 5000 memory access has 0.75 hit rate, what will be total memory access time in milli-second unit (write exact value - no unit)?

0.5725

Question 5

0.25 / 0.25 pts

A 4GB byte addressable main memory (32-bit system) is divided into block of size 1024 bytes. Processor wants to access a memory location 0xFC347004. Corresponding block is found in cache. Which index, within this block, will be accessed? [Answer in decimal number]

4

Question 6

0.25 / 0.25 pts

Assume a 24-bit computing system has a cache system with 256 cache lines. A block address of 0xA2CF5B is being accessed. Cache line 0x 5B will be accessed in this case with tag 0x A2CF

Answer 1:

5B

Answer 2:

A2CF

Question 7

0.25 / 0.25 pts

A cache system has 1024 cache line with block size of 1024 bytes. It uses 22-bits TAG and 10-bits 'Ctrl' bits. What is the total size of cache memory in KB unit?

1,028

Question 8

0.25 / 0.25 pts

Regarding cache memory, select true statement(s).

- [ ] Cache memory always needs quotient and remainder generation circuit (a.k.a. division circuit) to translate block address into cache line index and tag.

- [x] Control bits in cache memory is used for cache memory book keeping purpose.
- [ ] Cache line is replaced upon cache hit.
- [ ] For any cache system, memory address to cache line mapping is always many-to-one mapping.
- [x] For 1-way associative cache, memory addresses to cache lines mapping is many-to-one mapping.

Question 9

0.25 / 0.25 pts

Match write cache write policy characteristics.

Date inconsistency among hierarchy of memory is resolved at write time	Write through
Date inconsistency among hierarchy of memory is resolved at block replacement time	Write back

Question 10

0.25 / 0.25 pts

Related to cache miss handling select true statement(s)

- [x] Write operation is faster in a cache deploying write back policy.
- [ ] Only cache miss during write operation needs to write back dirty block into lower level memory in cache implementing write back policy.

- [ ] Cache miss is handled only by control unit of the processor.
- [ ] Write back policy is easier to implement in hardware than write through policy.
- [x] Write buffer in MMU helps to avoid controller stall upon cache miss during write using write through policy.

Question 11

0.25 / 0.25 pts

How many cache line a fully associative cache has?

1

Question 12

0.25 / 0.25 pts

What would be mapping type between main memory addresses and cache lines in a set associative cache?

- ( ) One to one
- (•) Many to many
- ( ) One to many
- ( ) Many to one

Question 13

0.25 / 0.25 pts

What is limit of virtual memory size in a computing system?

- Limited by number of bits in address bus.
- [x] Limited by swap space defined during OS installation.
- Same as main memory used in system.
- Unlimited
- None of these

Question 14

0.25 / 0.25 pts

What is the purpose of virtual memory system?

- It is an illusive memory to confuse programmers.
- To increase memory in virtual systems.
- [x] To enable usage of bigger memory space than system's main memory.
- To enable programs to use memory from virtual systems.
- [x] To permit single programs to use entire address space of the system.

Question 15

0.25 / 0.25 pts

Among the following list of page replacement strategies, which one is the most effective in virtual memory system?

- Random
- Most recently used
- [x] Least recently used
- Last in first out

Question 16

0.25 / 0.25 pts

What is the associativity of page table?

- None of these
- Set associative
- One way associative
- Fully associative

Question 17

0.25 / 0.25 pts

In a computing system deploying virtual memory, there are 1M (2^{20}) page table entries per process. Each entry has 48 bits. At one time, all the page tables for all active processes are consuming total 6GB space in main memory. How many active processes are there at this time?

1,024

Question 18

0.25 / 0.25 pts

Which register in processor holds address to page table for a process?

- Global pointer register
- Translation look-aside buffer
- None of these
- Stack pointer register
- Page table register

Question 19

0.25 / 0.25 pts

What is the associativity of a TLB?

- ○ Set associative
- ◉ Fully associative
- ○ None of these
- ○ One way associative

Question 20

0.25 / 0.25 pts

Regarding virtual memory system, select true statement(s) from the following.

- ☑ TLB is a cache for page table.
- ☐ Systems using virtual memory does not use cache system.
- ☐ Write through is the most effective strategy to sync content across hierarchy in virtual memory system.
- ☑ 'Cache miss' in context of cache is same as 'page fault' in context of virtual memory.
- ☐ Page faults are handled by hardware.

Quiz Score: **5** out of 5