Quiz 02 (Lecture 6-11) - Requires Respondus LockDown Browser + Webcam

- Due Oct 12 at 11:59pm
- Points 50
- Questions 20
- Available Oct 11 at 12am - Oct 13 at 5:30am
- Time Limit 45 Minutes
- Allowed Attempts 2
- Requires Respondus LockDown Browser

Instructions

1. Lecture 6-11.
2. Open book / note quiz.
3. You can use your own blank scratch paper to solve problems.
4. You can use calculator.
5. You have total 45 minutes per attempt to complete this quiz.

[For respondus monitor system ID check, you can use tower card, library card, driving license or any other valid ID card]

Attempt History

	Attempt	Time	Score
KEPT	Attempt 2	8 minutes	50 out of 50
LATEST	Attempt 2	8 minutes	50 out of 50
	Attempt 1	20 minutes	21.25 out of 50

⚠ Correct answers will be available Oct 13 at 6am - Oct 17 at 7:15pm.

Score for this attempt: 50 out of 50
Submitted Oct 12 at 4:20pm
This attempt took 8 minutes.

Question 1
2.5 / 2.5 pts

What are basic logic gates (may not be implemented by combining other basic gates) that can be implemented using CMOS technology?

- [x] NOT
- [ ] AND
- [ ] OR
- [x] NOR
- [x] NAND

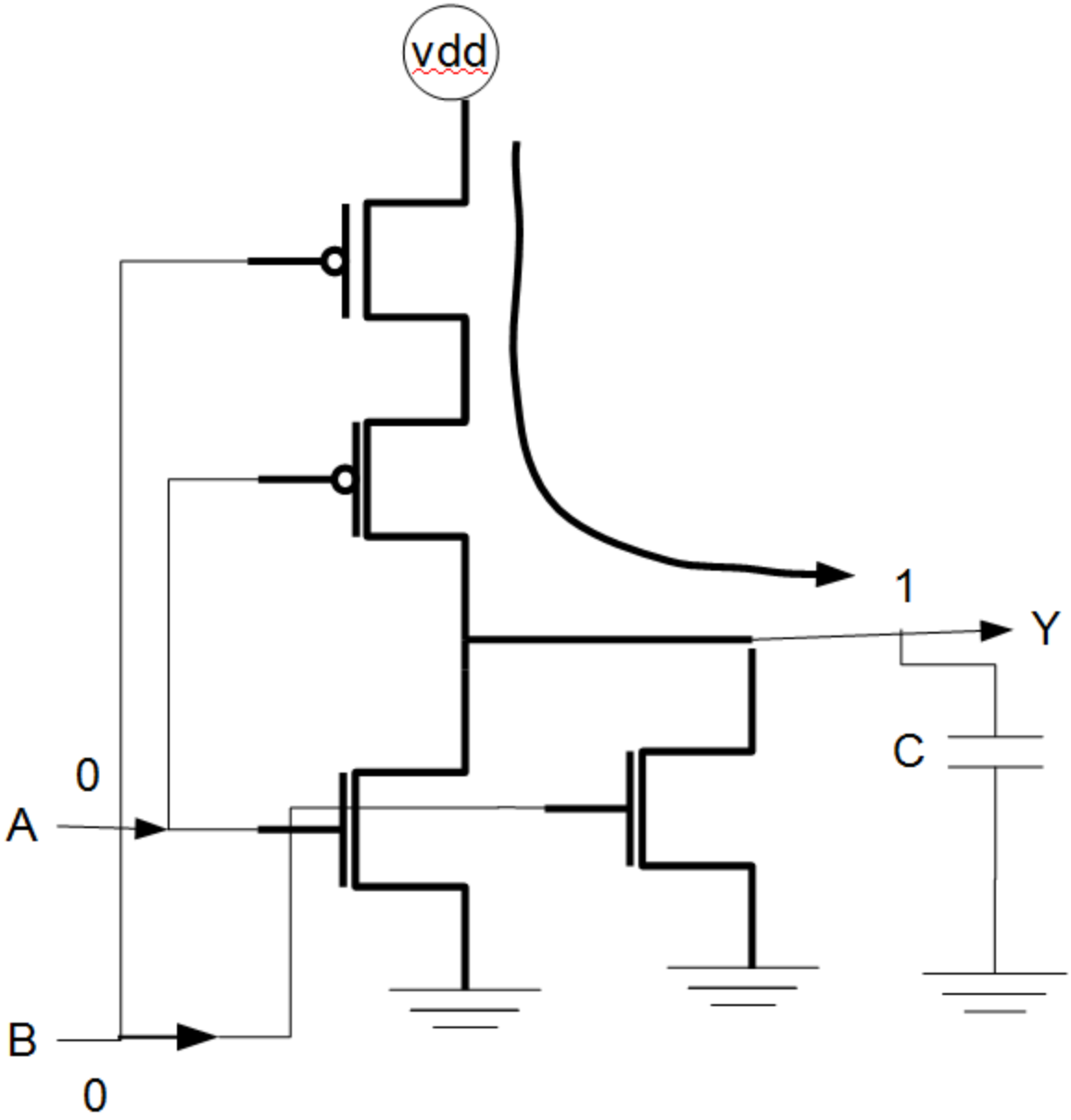
Question 2
2.5 / 2.5 pts

Which are the universal logic gates?

- [ ] INVERTER
- [x] NAND
- [ ] AND
- [x] NOR
- [ ] OR

Question 3
2.5 / 2.5 pts

This is a CMOS transistor level schematic for a logic gate. What is this logic gate?



- and
- or
- inv
- nor
- nand

To complete pull down path either NMOSs, driven by A and B has to be open (i.e. logic 1). Thus this is a NOR logic gate.

Question 4

2.5 / 2.5 pts

What are the steps for combination logic circuit design (i.e. no state table).

Step 1

Write Specification

Step 2

Construct Truth Table

Step 3

Optimize Boolean function

Step 4

Map Boolean functions to a

Step 5

Verify logic circuit

Correct !!! There is dependencies between steps. For example you can not make a truth table unless the problem specification is written down first. This is the correct sequence which resolves all such dependencies between steps.

Question 5
2.5 / 2.5 pts
Match characteristics of logic circuit types.
Combination Logic

Logic is always forward pro

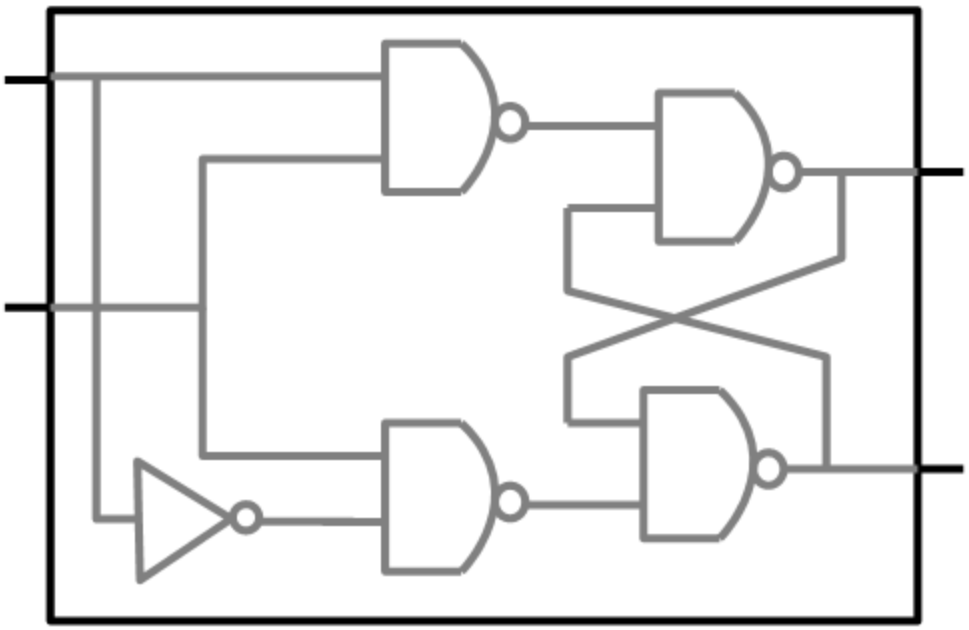
Sequential Logic

Logic is both forward and b

Combination logic circuit always push logic forward. Sequential logic circuit stores previous result (or part of it) and push back into current iteration of logic evaluation.

Question 6
2.5 / 2.5 pts

What type of sequential gate is this following?



- None of these
- S'R' Latch
- SR Latch
- SR Latch with control
- D Latch

Storage element in this circuit is an SR latch with control. The control logic gates are controlled by single control input (one with its true for and other with its complementary form). There is only one input for data. This is a D-latch with control.

Question 7

2.5 / 2.5 pts

How many latches are there in a master-slave flip-flop?

2

A master-slave flipflop has one master D-latch and one slave SR latch.

Question 8

2.5 / 2.5 pts

You are designing a sequential digital circuit with 12 states and 4 primary inputs. How many minimum number of rows do you need in corresponding truth table?

192

Correct !!!

12 states needs ceiling(log2(12)) = 4 bits to be encoded. With another 4 primary input, corresponding truth table will have 8 inputs. This means the truth table will have 2^8 = 256 rows. However, there are 12 states. This means 4 values of state encoding will be 'do not care' (X) state. This will give (4 * 2^4) = 64 'do not care' (X) terms in truth table. Therefore, truth table will have (256-64) = 192 rows minimum.

Question 9
2.5 / 2.5 pts
Match logic circuit type of logic circuit component.
Decoder

Combination Logic

Multiplexer

Combination Logic

Shift Register

Sequential Logic

Barrel Shifter

Combination Logic

Correct !!! Only shift register uses 'register' component in it thus it is sequential logic type.

Question 10
2.5 / 2.5 pts
How many XOR logic gate are there in a 64-bit ripple carry adder circuit?

128

Correct !!!

Each 1-bit full adder has 2 XOR gates. 64-bit ripple carry adder circuit will have 64 1-bit full adder circuit. This means, 64 bit ripple carry adder circuit will have (64*2) = 128 XOR gates.

Question 11

2.5 / 2.5 pts

What value combination(s) of input operands can cause overflow in a ripple carry adder/subtraction logic circuit? Assume input operands are represented in 2's compliment format.

- [x] Both positive
- [x] Both negative
- [ ] Any combination
- [ ] One positive and another negative

Only both positive or both negative addition will push result away from 0 on a number line which may cause overflow. Value with opposite sign will result a value ranging within those two operands. Hence, in this case, if the operands can be represented in binary, result will certainly be represented in binary using same number of bits.

Question 12

2.5 / 2.5 pts

What is the minimum size (in byte units) of total storage (register storage) needed in a 32-bit multiplier logic circuit data path?

- ( ) None of these
- ( ) 12
- (•) 0
- ( ) 20

Multiplier can be implemented with pure combination logic. That implementation does not need any storage.

Question 13

2.5 / 2.5 pts

What is the minimum size (in byte units) of total storage (register storage) needed in a 32-bit division logic circuit data path?

- ( ) 0
- ( ) None of these
- (•) 12
- ( ) 20

In the modified division circuit, that has been discussed in class, has one 32-bit register to hold divisor and 2 32-bit registers (specially connected for continuous shift operation and intermediate subtraction

result roll back) to hold dividend (quotient) and remainder. Therefore minimum register storage is needed is 12 bytes.

Question 14

2.5 / 2.5 pts

How many 32-bit 2x1 multiplexer is needed to implement signed division using unsigned division logic circuit as a basic component (i.e. no need to consider if there is a multiplexer inside this given division logic circuit)?

4

All these dividend, divisor, quotient and remainder need to have potential sign change depending on dividend's and quotient's original value. Therefore 4 32-bit 2x1 multiplexers are needed in this circuit.

Question 15

2.5 / 2.5 pts

Suppose you are designing a 32-bit sequential ALU as described in lecture 11. ALU output (HI & LO) is 0 for NoOP operation code. How many 1-bit 11x1 multiplexers do you need to implement 'result' and 'done' selection for the output of this ALU?

65

Correct !!!

For all the operation result is 32 bit, hence 32 1-bit 11x1 multiplexer is needed. There is one more 1-bit 11x1 multiplexer is needed for DONE signal. On top of this, MUL and DIV produces 64-bit result. There for we need another 32 1-bit 11x1 multiplexer. Here total of (32+32+1) = 65 1-bit 11x1 multiplexer is needed.

Question 16

2.5 / 2.5 pts

At which processor state, PC is updated with next Instruction's address?

- Memory Access (MEM)
- Write Back (WB)
- Instruction Fetch (IF)
- Execute (EXE)
- Instruction Decode / Register Fetch (ID/RF)

Question 17

2.5 / 2.5 pts

Which instruction in CS147DV has least number of components in its data path?

lui

Question 18

2.5 / 2.5 pts

Which of the following components are included in instruction fetch data path?

- [x] Memory
- [x] IR
- [ ] ALU
- [ ] Register File
- [x] PC

Question 19

2.5 / 2.5 pts

Which of this following transforms (processes) data in a micro-processor?

- ( ) Both of them
- ( ) Control Path
- (•) Data Path
- ( ) None of them

Question 20

2.5 / 2.5 pts

For CS147DV implementation, which are states where we should hold ALU operation codes for 'add r10, r2, r3' instruction execution?

- [ ] IF
- [x] MEM
- [x] WB
- [x] EXE
- [ ] ID/RF

Quiz Score: 50 out of 50