Quiz 03 - Requires Respondus LockDown Browser + Webcam

Due Nov 16 at 11:59pm **Points** 5 **Questions** 20
Available Nov 15 at 6am - Nov 16 at 11:59pm 1 day **Time Limit** 45 Minutes
Allowed Attempts 2 Requires Respondus LockDown Browser

Instructions

1. Lecture 12-18.
2. Open book / note quiz.
3. You can use your own blank scratch paper to solve problems.
4. You can use calculator.
5. You have total 45 minutes per attempt to complete this quiz.

[For respondus monitor system ID check, you can use tower card, library card, driving license or any other valid ID card]

Attempt History

	Attempt	Time	Score
KEPT	Attempt 2	3 minutes	5 out of 5
LATEST	Attempt 2	3 minutes	5 out of 5
	Attempt 1	17 minutes	4.63 out of 5

ⓘ Correct answers are hidden.

Score for this attempt: **5** out of 5
Submitted Nov 16 at 11:38am
This attempt took 3 minutes.

Question 1 — 0.25 / 0.25 pts

Which of the following component(s) do(es) determine that ALU must be designed sequential?

- ☐ bit shifter
- ☑ divider

- [ ] multiplier
- [ ] adder / subtractor

Question 2

0.25 / 0.25 pts

Select statement(s) which is (are) true.

- [ ] Instruction register is a component in control path
- [x] Control signal is Boolean function of processor state.
- [ ] Control signals are generated by data path.
- [x] Data path carries information to be processed though various data processing / storage elements.

Question 3

0.25 / 0.25 pts

How many states does our Project II processor have?

5

Question 4

0.25 / 0.25 pts

Assume our project II is using ALU as described in lecture 11. This processor is going execute 'sll r10, r5, 10' next. How many cycle will this processor take to complete this instruction?

14

Question 5

0.25 / 0.25 pts

Which component is used to resolve data path conflict?

- Line Decoder
- Shifter
- Multiplexer
- XOR Logic Gate

Question 6

0.25 / 0.25 pts

Select statement(s) which is (are) true.

- [x] It is sufficient to include only logic operations in ALU to build a processor.
- [ ] Processor supporting divide operation can be designed using single clock per state transition.
- [x] Frequency of clock used in processor with one cycle per state tends to be slower.
- [ ] Processor architecture is independent on ISA

Question 7

0.25 / 0.25 pts

A byte addressable memory contains 0x24 0x4A 0x3E 0x87 0x2A 0x5A 0xA5 0x71 from address 0x10010024. A processor following little endian system, is accessing an word from address 0x10010026. The value of the word is 0x

5A2A873E

Answer 1:

5A2A873E

Make sure to use UPPER CASE for hex digit.

Question 8

0.25 / 0.25 pts

For a processor, a single store word (sw) operation is accessing memory twice. What is the addressing mode corresponding to this instruction?

- ○ Displacement
- ◉ Indirect
- ○ Register
- ○ Register Indirect

Question 9

0.25 / 0.25 pts

Which of these addressing modes do not involve memory access?

- ☑ Immediate
- ☑ Register
- ☐ Displacement
- ☐ Stack

Question 10

0.25 / 0.25 pts

Select statement(s) which is (are) true.

- [ ] CISC needs more memory for program storage compare to RISC.
- [ ] RISC Supports variable length instruction format
- [x] Substantially large number of addressing mode is available in CISC compare to RISC.
- [x] RISC contains elementary operation sets only

Question 11

0.25 / 0.25 pts

What is the type of primary performance gain if a system is upgraded with faster processor?

- ( ) None
- (•) Response Time
- ( ) Both response time and throughput
- ( ) Throughput

Question 12

0.25 / 0.25 pts

What is the type of primary performance gain if a system is added with couple of extra faster processor?

- (•) Both response time and throughput
- ( ) Response Time
- ( ) None

- Throughput

Question 13

0.25 / 0.25 pts

A system is running benchmark program to measure performance of its processor. Which metric should we measure in this run?

- System CPU time
- User + System CPU time
- (•) User CPU time
- Elapsed time from start to finish

Question 14

0.25 / 0.25 pts

Determine impact on processor performance (+ve / -ve / neutral) of these following metrics.

Increase in clock frequency	+ve
Increase in CPI	-ve
Increase in number of instructions	-ve
More number of pipeline stages	+ve

Question 15

0.25 / 0.25 pts

Which of the followings do impact only instruction count and CPI?

- [x] Algorithm
- [ ] ISA
- [x] Programming Language
- [x] Compiler

Question 16

0.25 / 0.25 pts

What is the amount of performance improvement of a n-stage pipelined processor compare to its non-pipelined implementation?

- ( ) n
- ( ) Little more than n
- ( ) 2n
- (•) Almost n

Question 17

0.25 / 0.25 pts

Harvard architecture is used to resolve which of the following hazard in pipeline?

- ( ) Data Hazard
- (•) Structural hazard of accessing memory
- ( ) Structural hazard of accessing register file
- ( ) Control Hazard

Question 18

0.25 / 0.25 pts

Review following piece of code to be executed in a 5-stage pipe lined processor (as discussed in class) [ISA is CS147DV]

lw r1, r2, 0

lw r3, r2, 16

add r4, r1, r3

sw r1, r2, 20

Select strategies to avoid data hazard, if any, which will have minimum impact on performance.

- [ ] There is no data hazard
- [x] Data forward
- [ ] Pipeline stall
- [x] Instruction re-order

Question 19

0.25 / 0.25 pts

The following two pieces of code are executed on a 5 stage pipelined processor.

Code-A : Counting sum of 1 to 100 using a for loop .

Code-B : Looping through 100 values and printing if values are +ve or -ve. There is 50-50 chance of value being +ve or -ve.

Assume this processor always predicts 'branch is taken'. Which code does suffer more from purging / aborting instruction on fly?

- ( ) Insufficient informaiton
- (•) Code B

- Code A
- Both will suffer equal

Question 20

0.25 / 0.25 pts

Select statement(s) which is (are) true.

- [ ] Cluster computing does not provide high availability to users
- [x] Multi core systems are special type of SMP system
- [ ] SPARC T1 is an example of SMP system using shared bus architecture.
- [x] NUMA architecture is hybrid of SMP and Distributed System

Quiz Score: **5** out of 5