Quiz 01 (Lecture 1-5) - Requires Respondus LockDown Browser + Webcam

- Due Sep 14 at 11:59pm
- Points 50
- Questions 20
- Available Sep 13 at 12am - Sep 20 at 11:59pm
- Time Limit 45 Minutes
- Allowed Attempts 2
- Requires Respondus LockDown Browser

Instructions

1. Lecture 1-5.
2. Open book / note quiz.
3. You can use your own blank scratch paper to solve problems.
4. You can use calculator.
5. You have total 45 minutes per attempt to complete this quiz.

[For respondus monitor system ID check, you can use tower card, library card, driving license or any other valid ID card]

Attempt History

	Attempt	Time	Score
KEPT	**Attempt 2**	9 minutes	50 out of 50
LATEST	**Attempt 2**	9 minutes	50 out of 50
	Attempt 1	24 minutes	33.75 out of 50

ⓘ Correct answers will be available Sep 21 at 6am - Oct 15 at 7:15pm.

Score for this attempt: 50 out of 50
Submitted Sep 13 at 11:35pm
This attempt took 9 minutes.

⠿

Question 1
2.5 / 2.5 pts
An ALU implements 13 different operations. What is the minimum number of electrical signal lines needed for encoding 'operation' code (a.k.a. bus / bit width of 'operation' signal)?

> 4

Correct !!!

13 different operations needs ceiling ($\log_2$ (13)) = 4 bits for encoding. Thus, this ALU will have minimum 4 electrical signal lines for 'operation'.

⠿

Question 2

2.5 / 2.5 pts

Match power up values of these following registers in CS147DV ISA.

$PC

0x00001000	⌄

$GP

0x01008000	⌄

$SP

0x03FFFFFF	⌄

$R10

0x00000000	⌄

Correct !!!

⠿

Question 3

2.5 / 2.5 pts

Convert '**slti r15, r10, 0x26**' of CS147DV ISA into machine code in hexadecimal format. Answer is 0x

294F0026

.

Answer 1:

294F0026

Correct !!!

For assembly code 'slti r15, r10, 0x26' following are the parts of machine code.

OpCode : 0x0a => 001010

RS : 10 => 01010

RT: 15 => 01111

Immediate: 0x26 => 0x0026 => 0000000000100110

Hence machine code is 00101001010011110000000000100110

Thus hexadecimal is

0010 | 1001 | 0100 | 1111 | 0000 | 0000 | 0010 | 0110

0x294F0026

⋮

Question 4

2.5 / 2.5 pts

Your laptop's processor is running with 2.5GHz clock with 35% duty ratio. How much time in nano-second unit is spent in logic 'low' (0) state by clock signal during one clock period time? Assume ideal rise-fall and fall-rise transition, i.e. signal transition time in 0.

Just put numerical value. e.g. if your answer is 2.0ns then put 2.0 in answer space.

| 0.26 |

Correct !!!

Duty ratio = ((T_H / T) * 100) %

T_H : Signal at high state

T : Time period

In this case

Time period T = 1/2.5GHz = 0.4ns

35 = (T_H / 0.4) * 100

=> T_H = 0.35 * 0.4ns = 0.14ns

Therefore T_L = T - T_H = 0.4ns - 0.14ns = 0.26ns

⋮

Question 5

2.5 / 2.5 pts

A memory system has total 256GB storage space. This memory system has 35 address pins which are all used to access all parts of the memory. What can you infer about it's addressability?

○ Half Word Addressable

○ Byte Addressable

○ None of these

○ Word Addessable

◉ Double Word Addressable

Correct !!!

Let's say there are b number of bits per buckets. Since there are 35 address pins, there are 2^{35} buckets. Therefore :

b * 2^{35} bits = 256GB

=> b * 2^{35} bits = 2^8 * 2^{30} * 2^3 bits

=> b * 2^{35} = 2^{41}

=> b = 2^6 = 64 => Double word addressable memory

Question 6

2.5 / 2.5 pts

In a memory with 'INOUT' type data bus, which of the following operation sequence is not possible in two successive clock cycle.

○ Write after a write.

○ Read after a write.

○ Read after a read.

◉ Write after a read.

Correct !!!

Since memory is using same set of electrical signal wires for both read and write operation, a write after a read must wait at least one clock cycle so that memory can produce the read data onto data bus.

Question 7

2.5 / 2.5 pts

MIPS (and similar processors) uses 5 cycles to complete action for an instruction of program. Sequence them correctly.

Cycle 1

Instruction Fetch (IF)   ∨

Cycle 2

| Instruction Decode / Regis ⌄ |

Cycle 3

| Execution (EXE) ⌄ |

Cycle 5

| Memory Access (MEM) ⌄ |

Cycle 6

| Write Back (WB) ⌄ |

Correct !!!

⁞

Question 8

2.5 / 2.5 pts

What are the differences between Von-Neumaan architecture and Harvard Architecture?

☐ Von Neumaan architecture has PC and IR registers in controller, but Harvard architecture does not have it.

☐ Von Neumaan architecture separates 'input' and 'output' but Harvard architecture does not.

☐ All of these

☑
Von Neumaan architecture has unified memory for data and instruction, where as Hardvard Architecture separates data and instruction memory.

☐ None of these

☐ Von Neumaan architecture has accumulator in ALU, but Harvard architecture does not have it.

Correct !!!.

Von Neumaan and Harvard architecture differs from each other on how data and instructions are stored / access. Von Neumaan proposes to have same, unified memory to store data and instructions alike. Harvard architecture separates data and instructions memory to boost performance.

⁞

Question 9

2.5 / 2.5 pts

What is unsigned value of binary bit pattern 1001101001010110?

- ☑ 0x9A56
- ☐ 0x65A9
- ☐ 621511
- ☑ 115126 in octal

Correct !!!

For Hexadecimal make 4-bit groups from RHS.

1001 1010 0101 0110 == 0x9A56

For Octal make 3-bit groups from RHS and add '00' to LHS to make last group.

001 001 101 001 010 110 = 115126

Value is concept which is represented by number. Use bit grouping and encoding to translate into another representation.

::::
Question 10
2.5 / 2.5 pts
A number system uses symbols Do, Re, Mi, Fa, So, La, Te with decimal values 0, 1, 2, 3, 4, 5, and 6 respectively. What is the base of this number system?

- ○ None of these
- ○ 14
- ◉ 7
- ○ 6

Correct !!!

A base is the number of symbols used to write values in that number system.

::::
Question 11
2.5 / 2.5 pts

Write down base of the following number system. If it is unknown / undefined as in single base system, put a '0'.

Binary	2

Octal	8
Decimal	10
Hexadecimal	16
Roman	0

Answer 1:

2

Answer 2:

8

Answer 3:

10

Answer 4:

16

Answer 5:

0

Correct !!!

Since 'roman' number system does not follow single base system we put a '0' there. In fact, roman following something called 'biquinary' system. More interesting reading in https://en.wikipedia.org/wiki/Quinary

Question 12

2.5 / 2.5 pts

What is the lowest value represented in a 10-bit 2's complement binary number system?

-512

Correct !!!

Range of n-bit 2's complement representation is $[-2^{n-1}, 2^{n-1} - 1]$

Therefore with 10-bit 2's complement number system lowest value represented is $-2^{10-1} = -2^9 = -512$

Question 13

2.5 / 2.5 pts

A Boolean function $F(X,Y,Z) = X'.Y'+Z$. Construct truth table as following assuming bit sequences are X,Y,Z in LHS of this matching table.

000

1	⌄

001

1	⌄

010

0	⌄

011

1	⌄

100

0	⌄

101

1	⌄

110

0	⌄

111

1	⌄

Correct !!!

We have to evaluate the expression in RHS of the equation and fill out the table. Where X and Y has 00 combination or Z has 1 function will be evaluated to 1, 0 otherwise.

Question 14

2.5 / 2.5 pts

Which type of transformation on Boolean function involves complementing function variables.

○ None of these

◉ Complement of function

○ Dual of function

Correct !!!

Dual and Complement transformation only differs from each other on complementing variables. Dual does not need variable complement.

⋮⋮

Question 15

2.5 / 2.5 pts

Which rule / theorem / relation in Boolean algebra makes it directly reduce (X+Y)(X'+Z)(Y+Z) into (X+Y)(X'+Z)?

○ Dual

○ DeMorgan

◉ Consensus

○ Complement

Correct !!!

Consensus theorem states that if two variable individually goes with another 3rd variable in its complemented form respectively, then their own pairing can be omitted from final expression.

⋮⋮

Question 16

2.5 / 2.5 pts

Identify rule types for following cases.

X.Y = Y.X

Commutative ⌄

X+Y.Z = (X+Y).(X+Z)

Distributive ⌄

X+(Y+Z) = (X+Y)+Z

Associative ⌄

(X+Y)' = X'.Y'

> DeMorgan ⌄

Correct !!!

⋮

Question 17

2.5 / 2.5 pts

Select all the minterms for a function F(W,X,Y,Z).

- ☐ W'XYZW
- ☑ W'X'Y'Z
- ☐ WXY
- ☑ WX'Y'Z
- ☐ XYZ

Correct !!!

⋮

Question 18

2.5 / 2.5 pts

What are the standard forms of these following Boolean function F(X,Y,Z)?

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

- ☐ ΠM(0,1,4,5)
- ☑ ΠM(2,3,6,7)
- ☐ None of these
- ☐ Σm(2,3,6,7)
- ☑ Σm(0,1,4,5)

Correct !!!

This function in truth table can be written as both SOP and POS.

- Σm(0,1,4,5)
- ΠM(2,3,6,7)

⋮⋮

Question 19

2.5 / 2.5 pts

Simplify this Boolean function - F(W,X,Y,Z) = Σm(4,6,9,11,12,13,14,15)

○ W'X' + WX'Z + W'XZ'

○ W'Z' + X'Z

○ WX + W'XZ' + WX'Z

◉ WZ + XZ'

Correct !!!

Using K-map Primary implicants are

- Σm(4,6,12,14)
- Σm(9,11,13,15)
- Σm(12,13,14,15)

Essential prime implicants are

- Σm(4,6,12,14) = XZ'
- Σm(9,11,13,15) = WZ

⋮⋮

Question 20

2.5 / 2.5 pts

Choose true statement(s) in the following.

☐ One may make a prime implicant group in a K-map using all don't care terms (X)

☑ We can use K-map technique on paper pencil for 2 to 4 variable functions only.

☑ Column and row indices follow gray code sequence in K-Map

☑ In K-map reduction process, treat don't care term (X) as 1 if and only if it helps to reduce Boolean expression,

☐ All the prime implicants needs to selected for Boolean expression reduction using K-map.

Correct !!!

Quiz Score: 50 out of 50