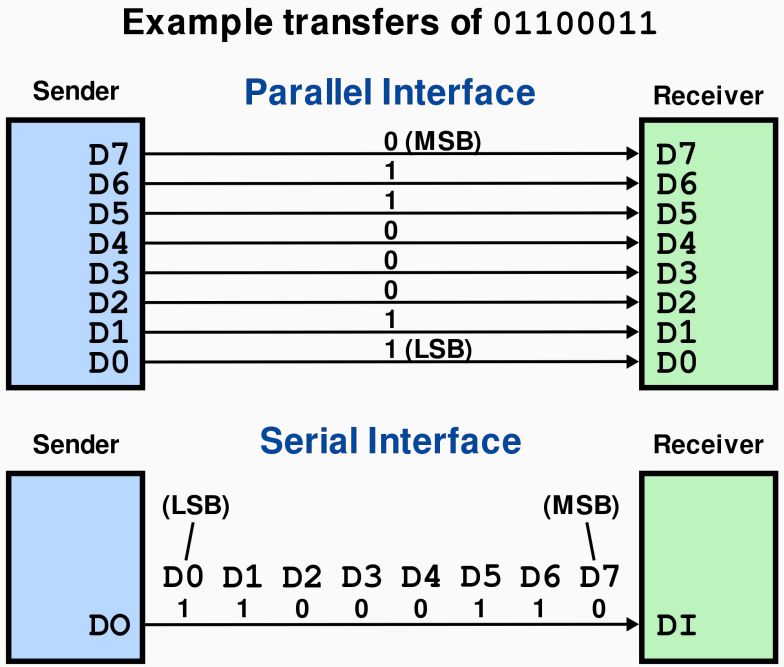
Advanced Projects

Lecture 1: Communication Protocols

Communication Protocols

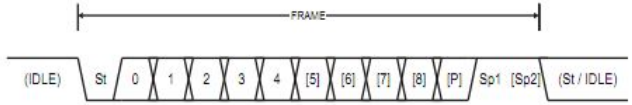
- Communication between different hardware devices
- Voltage used to represent 1s and 0s
- **Serial**
  - One bit at a time
  - UART, SPI, I^2C
- Parallel
  - Multiple bits sent simultaneously



UART - Universal Asynchronous Receiver/Transmitter

- Uses 2 wires per pair of devices
  - TX transmits data
  - RX receives data
  - TX connects to RX
- Message is 5 - 9 bits long
- Optional parity bit for error detection
- 1 start bit and 1 or more stop bits
- Line held high when not in use
- Data usually transmitted at 9600 - 115200 baud (bits per second)

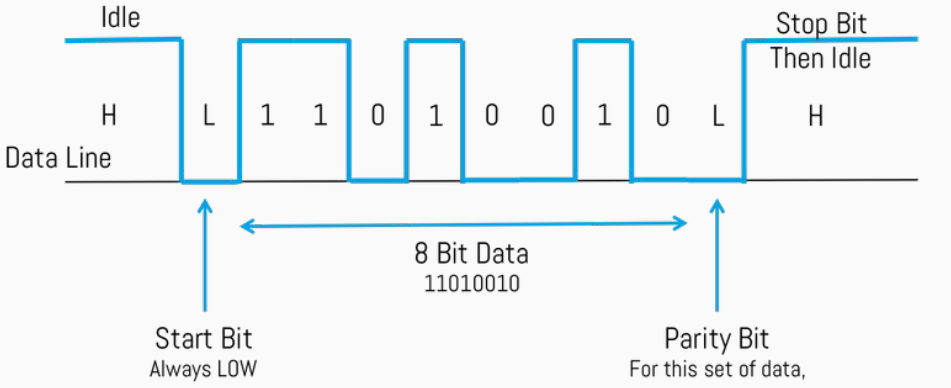
Figure 19-4. Frame Formats



St	Start bit, always low.
(n)	Data bits (0 to 8).
P	Parity bit. Can be odd or even.
Sp	Stop bit, always high.
IDLE	No transfers on the communication line (RxDn or TxDn). An IDLE line must be high.

Asynchronous Communication

- No explicit marking of each bit's start/end
- Each bit lasts a constant amount of time on the line
- Each device has its own clock, which drift over time
- Transitions from 0 -> 1 and 1 -> 0 can be used to resync clocks
- Low baud rate necessary to keep devices synchronized



Asynchronous Data Transfer Timing Diagram

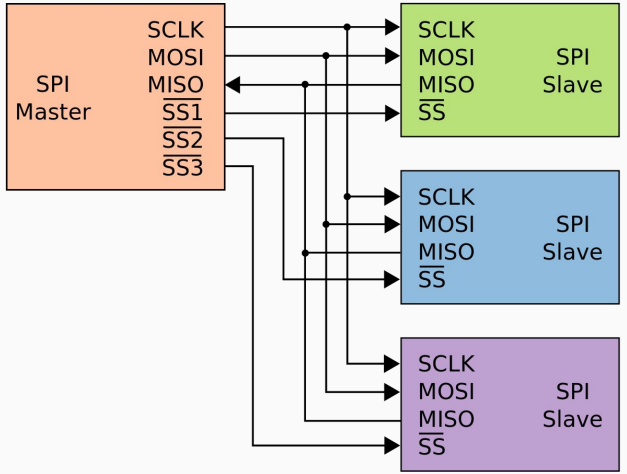
mE maxEmbedded.com

Drawbacks of UART

- Requires 2 wires per pair of devices
- Transmit speed must be configured beforehand
- Asynchronous communication greatly limits speed

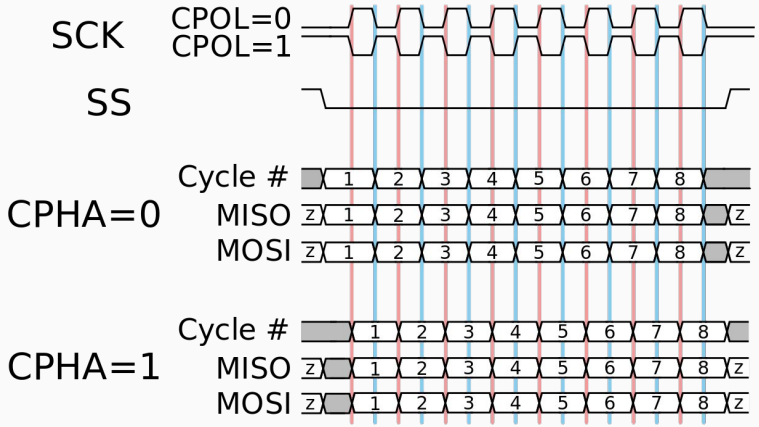
SPI - Serial Peripheral Interface

- Uses 3 + n wires
  - Data lines for master-out slave-in (MOSI) and master-in slave-out (MISO)
    - Master device controls clock and begins each synchronized transmission
  - Separate clock line (SCLK)
    - Transitions twice for each bit: reading and writing
  - Slave select (SS)
    - Unique to each slave to initiate transaction
    - Active low
- Message is usually multiple of 8 bits
- Data usually transmitted on order of MHz



Polarity and Phase

- Polarity is the idle state of SCLK
  - Represented by configuration variable CPOL
- Phase decides when data is read or transmitted
  - Represented by variable CPHA
  - 0 means read data on the leading edge, change data on the trailing edge, 1 is reverse
- Different devices have different polarity and phase

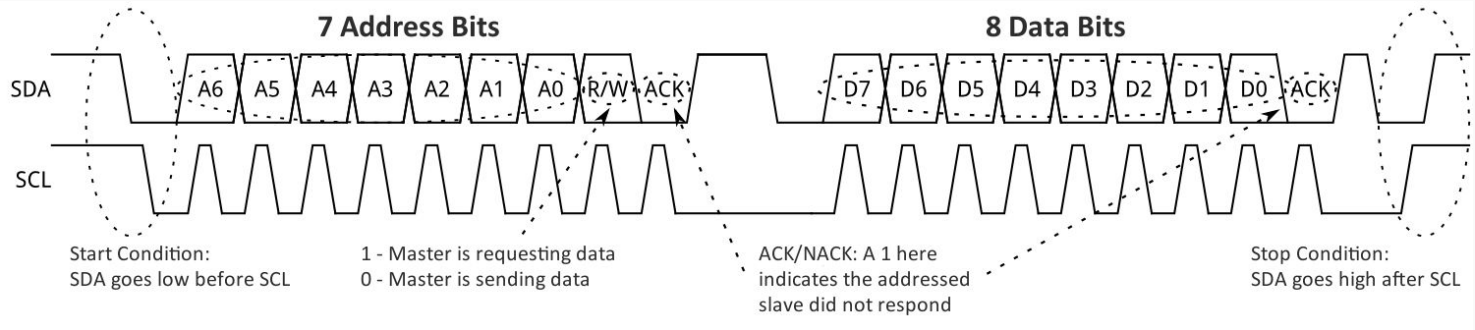


Drawbacks of SPI

- Still many wires
- No error detection (e.g. parity bit)
- Only one master per SPI bus

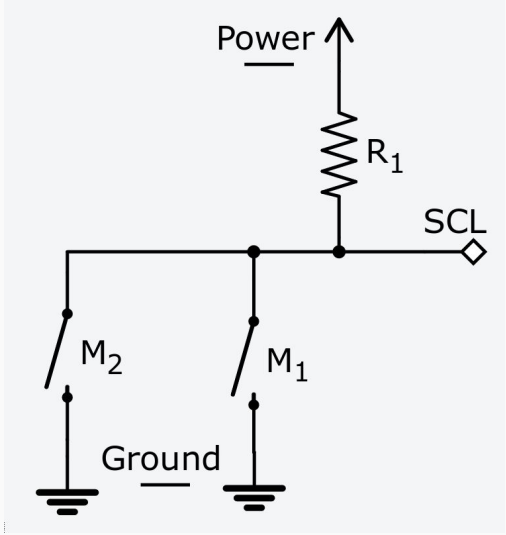
I²C - Inter-Integrated Circuit

- Multiple masters and multiple slaves on a single bus
- Only 2 wires
  - Data line (SDA), Clock line (SCL)
  - Both wires are idle high and SDA only changes when SCL is low (polarity = 1, phase = 1)
- Message begins with 7 bit address and either a 1 (read) or 0 (write)
- Start bit (low) and stop bit (high) transition when SCL is high
- Second start bit can be sent instead of a stop bit if two consecutive transactions are needed
- ACK (low) or NACK (high) follows every byte



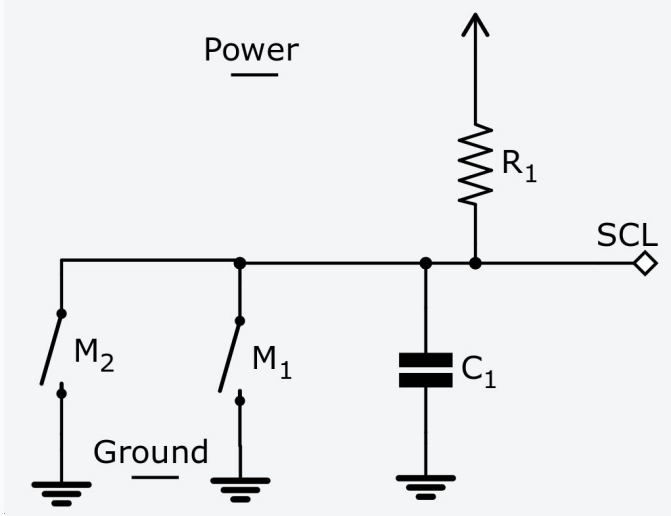
Multi-Master Bus with Open Drain Output

- SCL and SDA are both open-drain output, so masters writing low override masters writing high
- If bus voltage does not match output, master knows it is being overridden and stops sending data (bus arbitration)
- Slaves can also pull clock low to give extra data processing time (clock stretching)



Line Capacitance

- Common Ground is needed for reading voltages
- Communication wires run in parallel to ground, forming a (very small) capacitor
- Line capacitance combined with pullup resistor causes open drain to have significant switching time
- Limits speeds to 100KHz - 400KHz
- Max bus capacitance is 400pF



Comparison

	UART	SPI	I^2C
Wires	2n	3 + n	2
Normal Speeds	9600 - 115200 Hz	Several MHz	100 - 400 KHz
Synchronous	No	Yes	Yes
Multi-master	N/A	No	Yes
Data Direction	Duplex	Duplex	Half-Duplex
Frame Size	5 - 9 bits	Multiple of 8 bits	Multiple of 8 bits

Lab

- Wireless Space Team
  - Sending data wirelessly via radio modules
  - 3 LEDs on receiving end, 3 push buttons on transmitting end
    - LEDs should blink in random order, sequences of increasing length
    - User must push corresponding buttons in correct order to move on to next phase
    - Debouncing
- Full details will be in the lab schematic.