RZ/T2M, RZ/N2L Group

Quick Start Guide: EtherNet/IP OpENer Sample Program

Introduction

This document describes the setup procedure of the sample program for RZ/T2M, RZ/N2L port of EtherNet/IP™ “OpENer”.

Target Device

RZ/T2M, RZ/N2L Group

Contents

1. Overview

This document describes the setup procedure of the sample program for RZ/T2M, RZ/N2L port of EtherNet/IP “OpENer” and explains the procedure for connecting the CODESYS software programmable logic controller (PLC).

In this sample program, these open-source software are used.

- EtherNet/IP OpENer
- FreeRTOS
- lwIP

For demonstration, the application of this sample program has an Exclusive Connection and an Input Only Connection. This document also explains how to connect to the CODESYS software prepared in package.

1.1 Abbreviations / Definitions

Table 1-1 Abbreviations/Definitions

Index	Abbreviations/Definitions	Description
1	IP	Internet Protocol
2	TCP	Transmission Control Protocol
3	USB	Universal Serial Bus
4	PC	Personal Computer
5	SW	Switch
6	EWARM	Embedded Workbench® for ARM
7	lwIP	lightweight IP
8	CIP	Common Industrial Protocol
9	OSS	Open-Source Software
10	QoS	Quality of Service
11	DLR	Device Level Ring

1.2 Reference

Technical information about RZ/T2M and RZ/N2L is available via Renesas.

Table 1-2 Technical Inputs for RZ/T2M

Index	Technical Inputs
1	r20ut4939egxxxx-rskplus-rzt2m-v1-um.pdf
2	r01uh0916ejxxxx-rzt2m.pdf
3	r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf

Table 1-3 Technical Inputs for RZ/N2L

Index	Technical Inputs
1	r20ut4984egxxxx-rskplus-rzn2l-v1-um.pdf
2	r01uh0955ejxxxx-rzn2l.pdf
3	r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf

1.3 Limitations and Restrictions / Known Issues

- Software driver
  - For the implementation of DLR object, a version under development (r_ethsw_extend) is used for r_ethsw. It will be officially implemented in FSP in the future, but the API names and features may be changed.
- EtherNet/IP OpENer
  - The OpENer RZ/N2L port does not support the LLDP Management object and the LLDP Data Table object.
- CIP Protocol Conformance Test Suite CT19
  - The status of conformance to CT19 is as follows. We plan to remove errors conduct tests and in future version updates.

Table 1-4 Conformance status to CT19

Category 1	Category 2	Description	Status
Conformance Test	Conformance-mode	Tests that require a specified device profile and implemented optional objects.	2 errors detected*
Behavior Test	ACD Behavior Test	Test scripts for behaviors of each function.	N/A (ACD not implemented)
	QoS Behavior Test		Fail*
	TTL & MCast Test		Pass
Manual Test	-	Tests that include a lot of manual operations, provided by ODVA in Excel file format	Not conducted*

*: Plan to remove errors conduct tests and in future version updates.

2. Features

The "OpENer" is an open-source software for I/O communication adapters of EtherNet/IP. It supports multiple I/O and explicit connections and includes objects and services for making EtherNet/IP-compliant products as defined in the ODVA specification.

This package is the RZ/T2M, RZ/N2L port of OpENer and includes OpENer source codes. Regarding the open-source license of OpENer, please see the following file.

```
common\oss\OpENer\license.txt
```

The Class Objects implemented in this sample software are as follows. For details, please see Chapter 7 Appendix C Table 7-3 ~ Table 7-10.

Table 2-1 CIP Object Classes supported on this sample software

Object Class #	Object Class Name
0x01	Identity
0x02	Massage Router
0x04	Assembly
0x06	Connection Manager
0x47	Device Level Ring
0xF5	TCP/IP Interface
0xF6	Ethernet Link
0x48	QoS

3. Hardware Setup

3.1 Requirements

This RZ/T2M, RZ/N2L project has been developed and tested on these environments using the following boards and tools.

Table 3-1 RZ/T2M Requirements

Item	Vender	Description
Board	Renesas Electronics	RZ/T2M RSK Board
IDE	IAR Systems	Embedded Workbench® for ARM Version 9.30.1
	Renesas Electronics	e² studio 2022-10 FSP Smart Configurator 2022-10 RZ/T2M Flexible Software Package (FSP) v1.1.0 Please download from the link below. https://github.com/renesas/rzt-fsp/releases/tag/v1.1.0
Emulator	IAR Systems	I-jet
	SEGGER	J-Link
Evaluation Software	CODESYS GmbH	CODESYS v3.5.15.10 32-bit *

*: Please use 32bit version, the 3.5.15.10 64-bit version and other versions may not work.

Table 3-2 RZ/N2L Requirements

Item	Vender	Description
Board	Renesas Electronics	RZ/N2L RSK Board
IDE	IAR Systems	Embedded Workbench® for ARM Version 9.30.1 Please apply the patch (EWARM_Patch_for_RZN2L_rev1.0.zip) which is available in http://www.renesas.com/rzn2l. Regarding how to apply the patch, please read the readme file in the patch file.
	Renesas Electronics	e² studio 2022-07 FSP Smart Configurator 2022-07 RZ/N2L Flexible Software Package (FSP) v1.0.0 Please download from the link below. https://github.com/renesas/rzn-fsp/releases/tag/v1.0.0
Emulator	IAR Systems	I-jet
	SEGGER	J-Link
Evaluation Software	CODESYS GmbH	CODESYS v3.5.15.10 32-bit *

*: Please use 32bit version, the 3.5.15.10 64-bit version and other versions may not work.

3.2 Hardware Settings

3.2.1 RZ/T2M RSK board

This document describes the major hardware. Refer to Renesas Stater Kit+ for RZ/T2M user's manual and schematic for more board details.

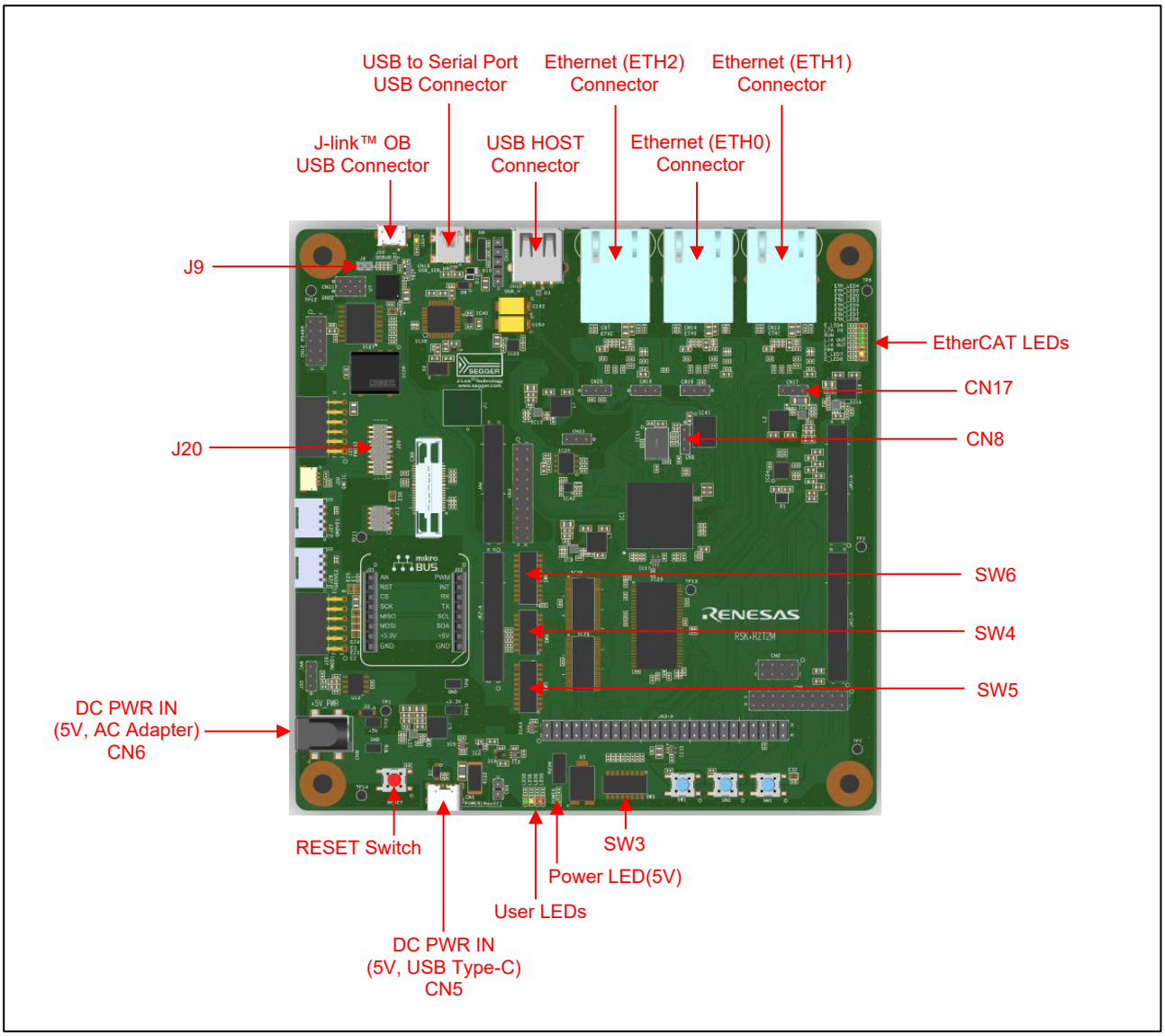


Figure 3-1 RZ/T2M RSK board layout

Table 3-3 Jumper pin settings

Reference	Jumper Position	Description
CN8	Shorted Pin 2-3	Enable QSPI (IC21).
CN17	Shorted Pin 2-3	Connect 1.8V Power rail to VCC1833_2. (When using Ethernet)
J9	Open	Enable the J-Link® OB.

Table 3-4 SW4 Settings

SW4	Setting	Description
SW4-1	ON	16-bit bus boot mode (NOR flash)
SW4-2	OFF	
SW4-3	ON	
SW4-4	ON	JTAG Authentication by Hash is disabled.
SW4-5	OFF	ATCM 1 wait

Table 3-5 SW5 Settings

SW5	Setting	Description
SW5-3	ON	Enable SCI_RTS
SW5-4	OFF	
SW5-5	ON	Enable SCI_RXD
SW5-6	OFF	
SW5-7	OFF	
SW5-8	OFF	Enable SCK3
SW5-9	ON	
SW5-10	OFF	

Table 3-6 SW6 Settings

SW6	Setting	Description
SW6-1	OFF	Enables signals other than the external bus. (CAN, Emulator, I2C, etc.)
SW6-3	ON	Enable TRACE_CTL
SW6-4	OFF	
SW6-5	OFF	Enable SCI_TXD
SW6-6	ON	
SW6-7	OFF	Enable MB_RST
SW6-8	ON	
SW6-9	OFF	Enable CAN_RX_OB
SW6-10	ON	

Other SW settings refer to r20ut4939egxxxx-rskplus-rzt2m-v1-um.pdf.

3.2.2 RZ/N2L RSK Board

This document describes the major hardware. Refer to Renesas Stater Kit+ for RZ/N2L user's manual and schematic for more board details.

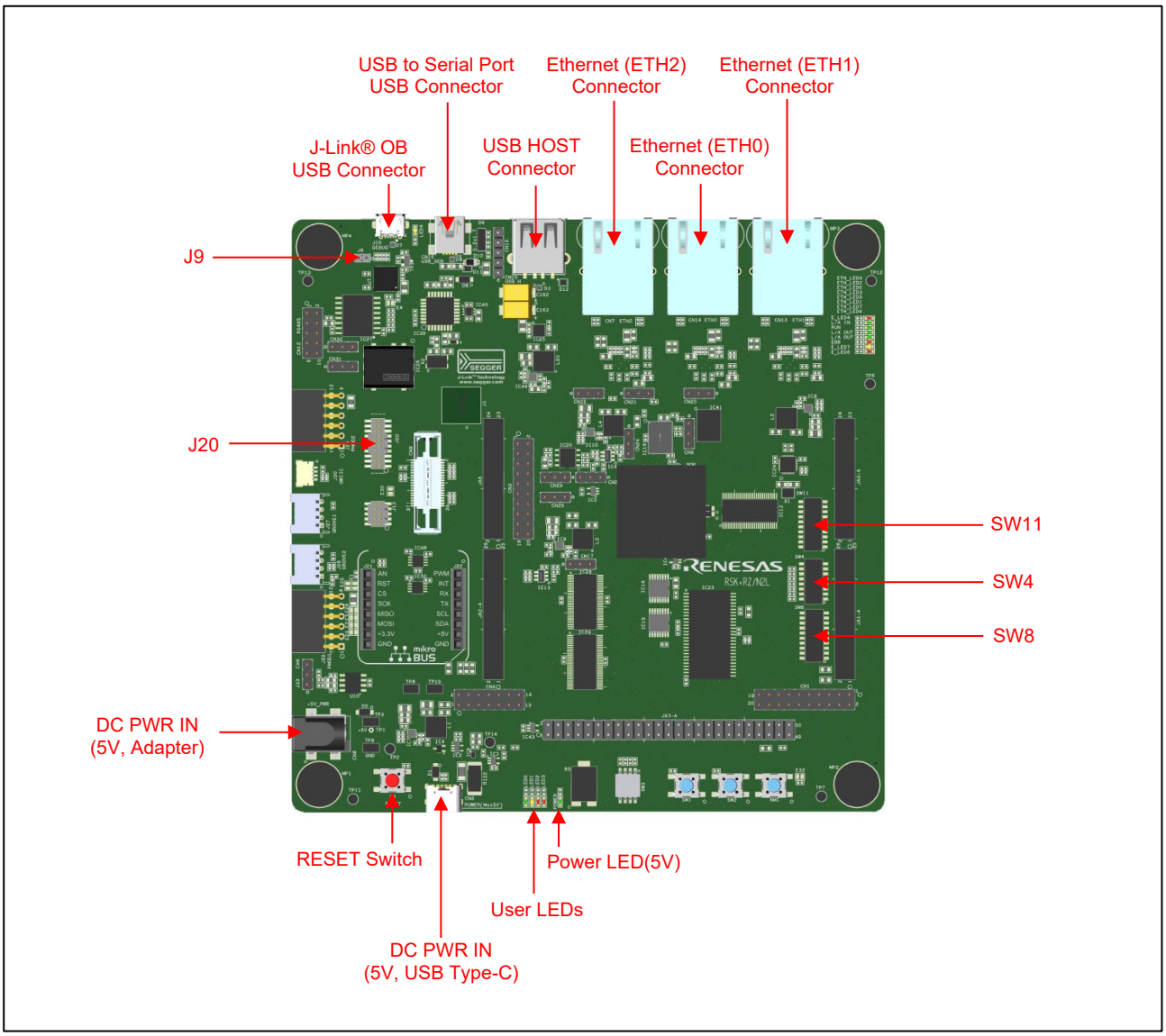


Figure 3-2 RZ/N2L RSK board layout

Table 3-7 Jumper pin settings

Reference	Jumper Position	Description
CN8	Shorted Pin 2-3	Enable QSPI (IC21).
CN17	Shorted Pin 2-3	Connect 1.8V Power rail to VCC1833_2. (When using Ethernet)
J9	Open	Enable the J-Link® OB.

Table 3-8 SW4 Settings

SW4	Setting	Description
SW4-1	ON	16-bit bus boot mode (NOR flash)
SW4-2	OFF	
SW4-3	ON	
SW4-4	ON	JTAG Authentication by Hash is disabled.
SW4-6	OFF	Enables signals other than the trace signal. (Motor, RS485, etc.)
SW4-7	ON	Enables signals other than the external bus. (CAN, Emulator, I2C, etc.)
SW4-8	OFF	Enable SW3.

Table 3-9 SW8 Settings

SW5	Setting	Description
SW8-1	OFF	Enable the "LED_GREEN" signal.
SW8-2	ON	
SW8-3	OFF	
SW8-4	ON	Enable the "LED5" signal.
SW8-5	OFF	

Table 3-10 SW11 Settings

SW6	Setting	Description
SW11-1	ON	Enable the " LED_RED2" signal.
SW11-2	OFF	
SW11-3	OFF	

Other SW settings refer to r20ut4984egxxxx-rskplus-rzn2l-v1-um.pdf.

3.3 Setup the Board

3.3.1 Setup RZ/T2M RSK Board

Setting the board for running sample program is shown below.

1. Connect an emulator.
   - When you use I-jet or J-Link emulator, connect it to J20 on RZ/T2M RSK board.
   - When you use J-Link On-Board emulator, connect USB micro-B to J10 on on RZ/T2M RSK board. (Please disconnect J9 for powering up J-Link OB.)

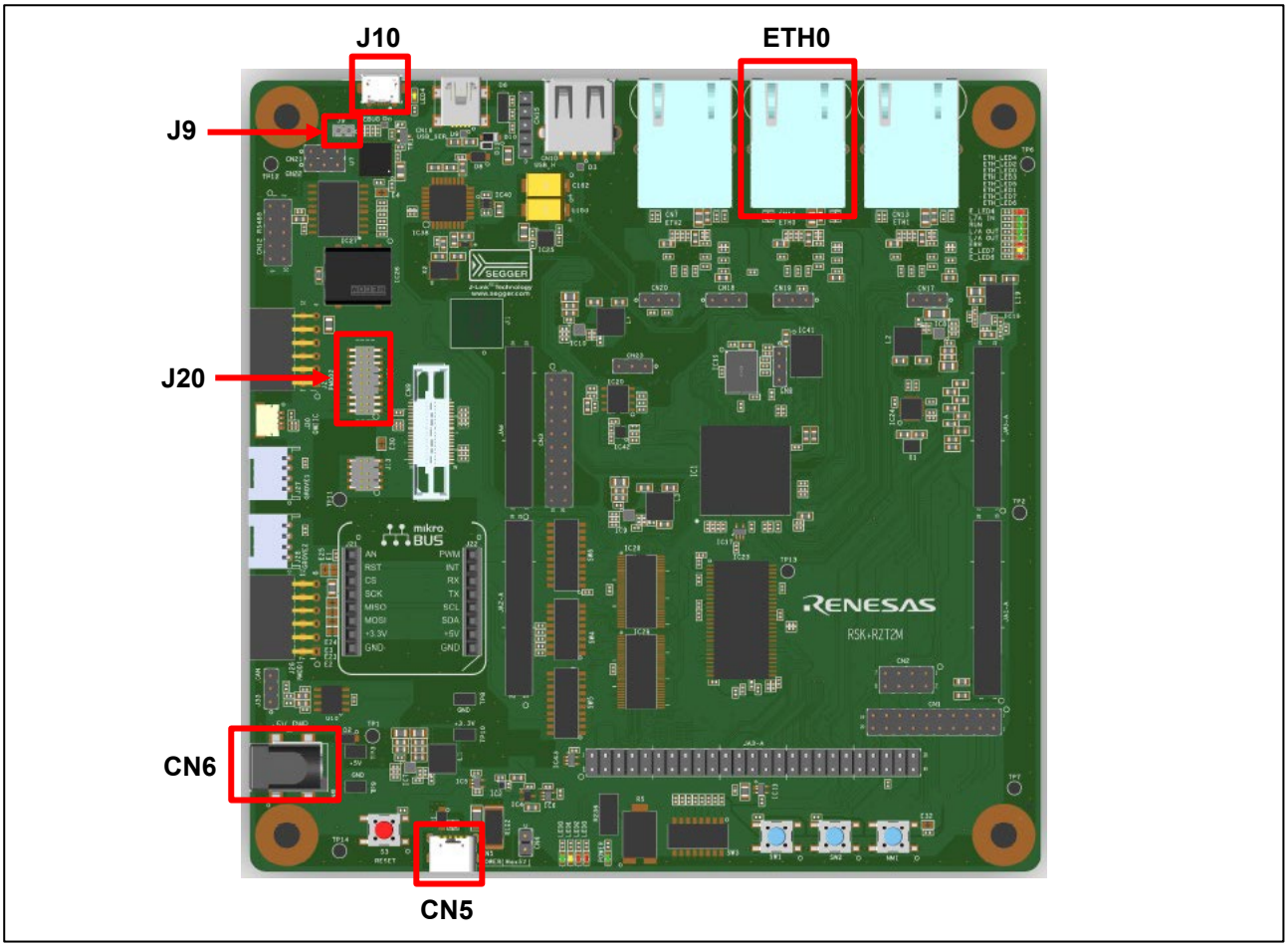


Figure 3-3 Setup RZ/T2M RSK board

2. Power is supplied using USB cable (Type-C) or AC / DC adapter.
   - When using USB cable (Type-C), connect it to the USB connector “CN5” on the RZ/T2M RSK board.
   - When using AC/DC adapter, connect it to the connector “CN6” on the RZ/T2M RSK board.
3. Connect Ethernet Cable to the Ethernet Connector “ETH0”.

3.3.2 Setup RZ/N2L RSK Board

Setting the board for running sample program is shown below.

1. Connect an emulator.
   - When you use I-jet or J-Link emulator, connect it to J20 on RZ/N2L RSK board.
   - When you use J-Link On-Board emulator, connect USB micro-B to J10 on on RZ/N2L RSK board. (Please disconnect J9 for powering up J-Link OB.)

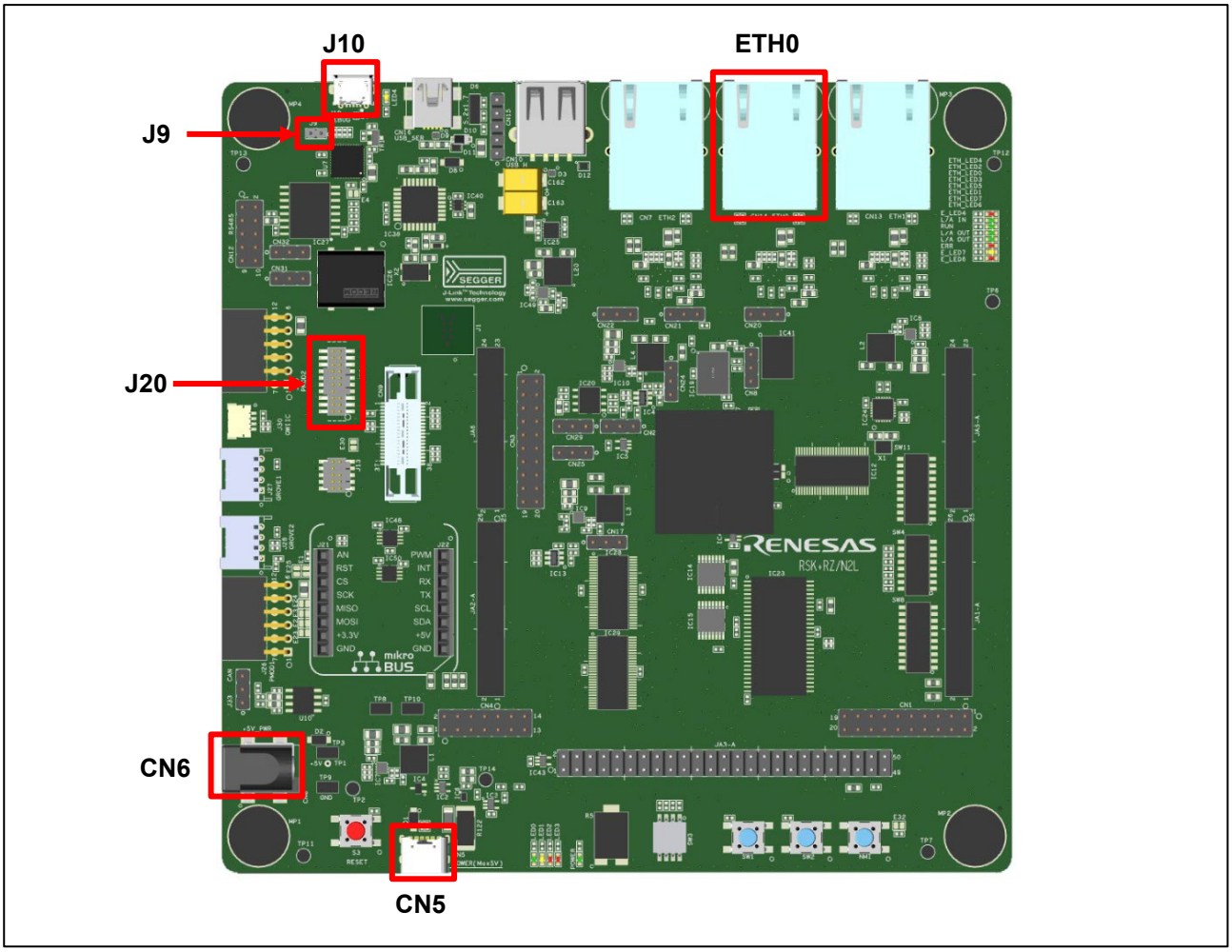


Figure 3-4 Setup RZ/N2L RSK board

2. Power is supplied using USB cable (Type-C) or AC / DC adapter.
   - When using USB cable (Type-C), connect it to the USB connector “CN5” on the RZ/N2L RSK board.
   - When using AC/DC adapter, connect it to the connector “CN6” on the RZ/N2L RSK board.
3. Connect Ethernet Cable to the Ethernet Connector “ETH0”.

4. Setup the Host Device

4.1 Configuration the Host IP Address

Set an IP address that can communicate with the device in the Ethernet adapter settings on the PC side.

This sample software sets the IP address 192.168.1.170 and subnet mask 255.255.255.0 for the device by default. Therefore, for example, set as follows on the PC side.

- IP address: 192.168.1.100
- Subnet mask: 255.255.255.0

4.2 Setup the CODESYS Software

This chapter describes the setup of the CODESYS software.

4.2.1 How to get CODESYS

CODESYS Development system is available from the following web sites. Please get version 3.5.15.10 32-bit*.

*: Please note that the 3.5.15.10 64-bit version or other versions may not work.

- CODESYS Store
  - ➢ To create your account and login is required to download the CODESYS tools.
    - ✧ When you create the account as a business customer, you need:
      - VAT Number if you are European VAT registered Customers.
      - Certificate of Registration as Taxpayer (entrepreneur) if you are non-EU customers.
  - ➢ Clicks "All versions" tab to get the specified version.

- CODESYS Store North America
  - ➢ To create your account and login is required to download the CODESYS tools.
    - ✧ United States, Canada and Mexico only can be registered in the "Country" form of the "Address Information".
  - ➢ Clicks "Versions" tab to get the specified version.

- LINX (Distributer in Japan)
  - ➢ To create your account and login is required to download the CODESYS tools.
    - ✧ Only Japanese companies can create the account.
  - ➢ The latest version only is available.
    - ✧ If you use the latest version, please try updating the CODESYS project included in this package by referring the section Appendix A: How to update CODESYS project.

4.2.2 Startup CODESYS Tools

After install the CODESYS, please launch the CODESYS tools shown below.

Table 4-1 CODESYS tools

Name	Description	Note
CODESYS V3	IDE	-
CODESYS Gateway V3	Software Gateway	This may be already started by Windows Start Up Process.
CODESYS Control Win V3	Software PLC	This may be already started by Windows Start Up Process.

If the CODESYS is launched properly, the following window is shown.

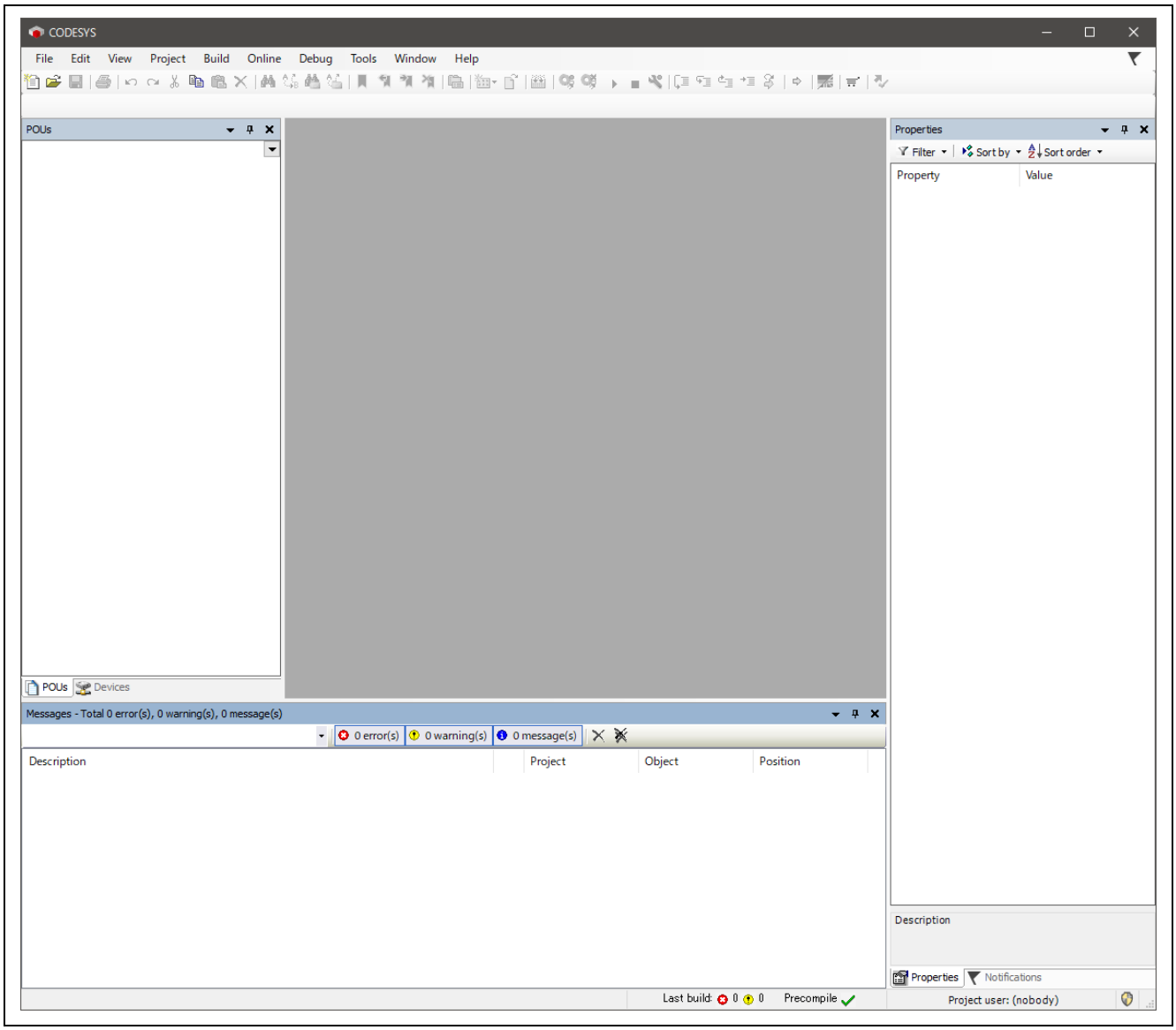


Figure 4-1 CODESYS Initial Window

If the CODESYS Gateway and Control Win SysTray is launched properly, the following icons are shown in notification area of Windows Tool Bar. (The left icon is of the CODESYS Gateway, and the right one is of the CODESYS Control Win SysTray)

Figure 4-2 CODESYS Icons

Please click each icon and click “Start Gateway” and “Start PLC”.

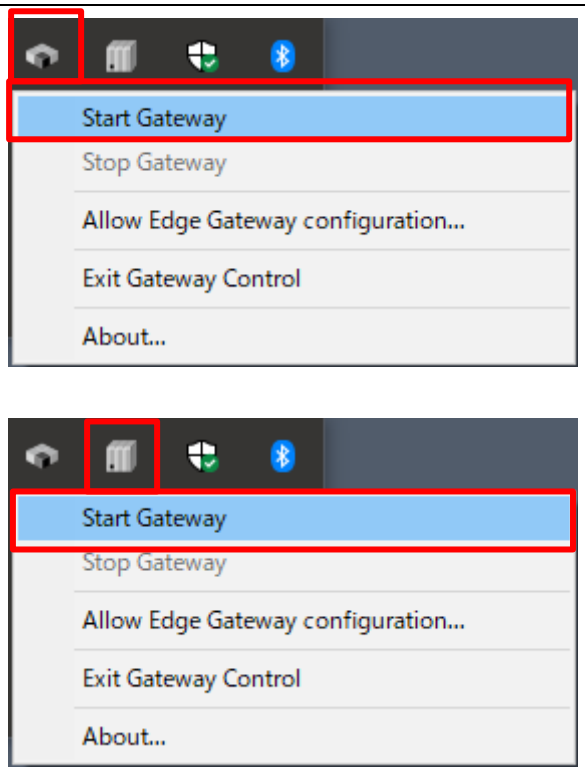


Figure 4-3 Start Gateway and PLC

If the Gateway and PLC is started properly, the icons pigment like the following image.

Figure 4-4 Icons with A and B successfully started

4.2.3 Install EDS File into CODESYS

In the CODESYS, please open “tools” > “Device Repository” in tool bar.

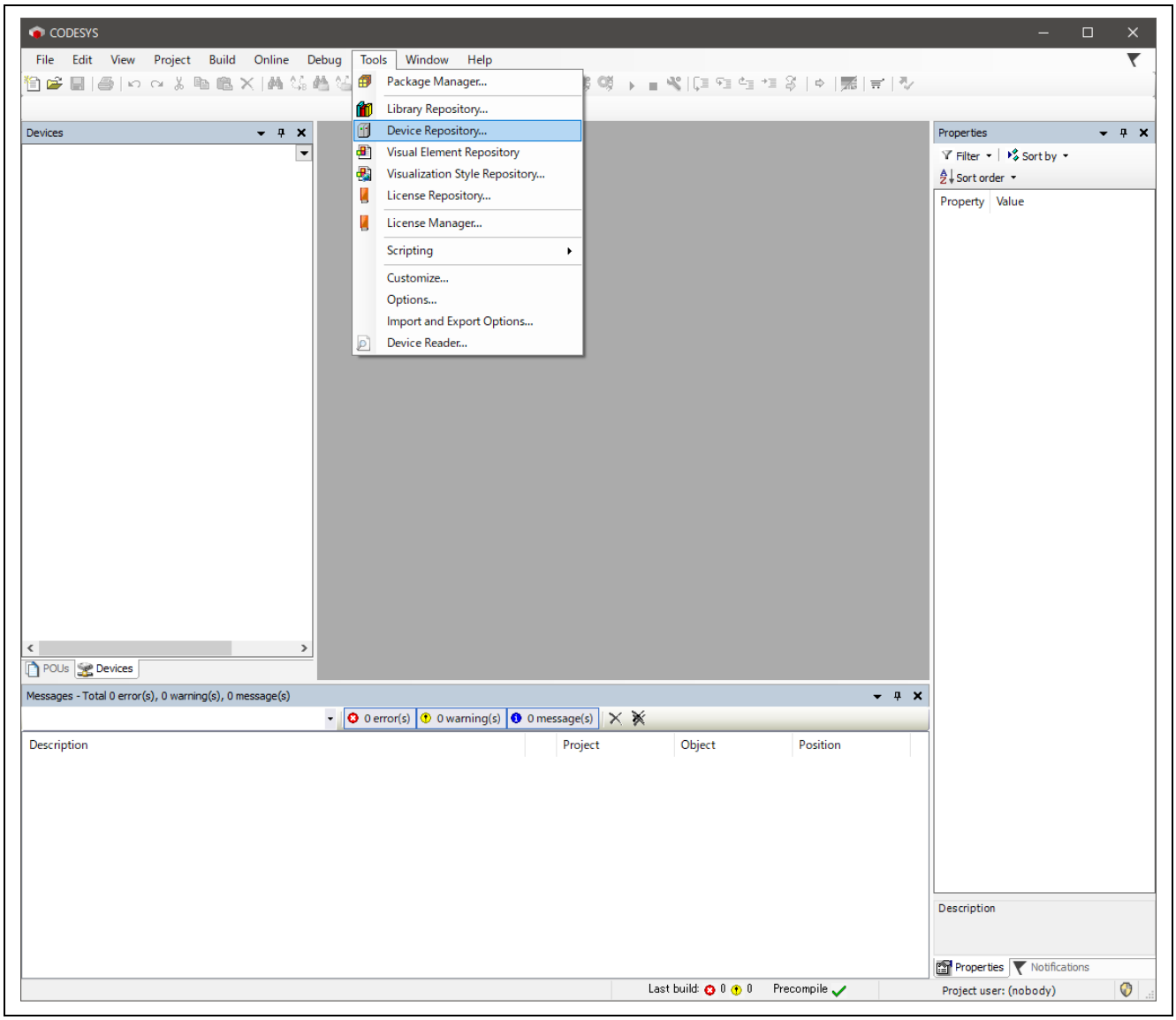


Figure 4-5 Device Repository in CODESYS

Please click the “Install” to open dialog to select EDS file, and select the EDS file “renesas_opener_sample_app.eds” in “scanner” directory.

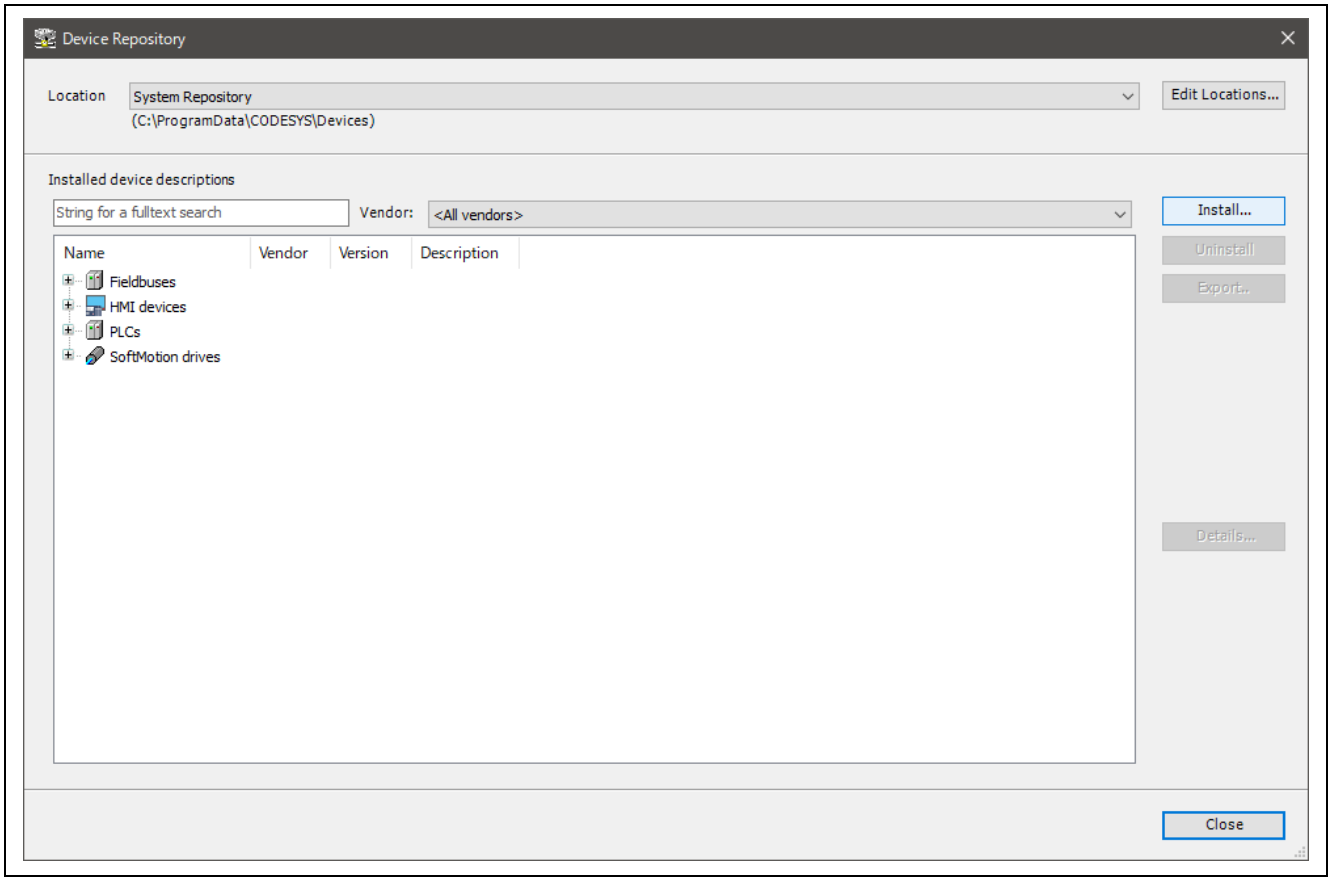


Figure 4-6 Click "Install" in Device Repository Window

If the Renesas OpENer Device is shown in the blue line as EtherNet/IP Remote Adapter, please click “close” to close this window.

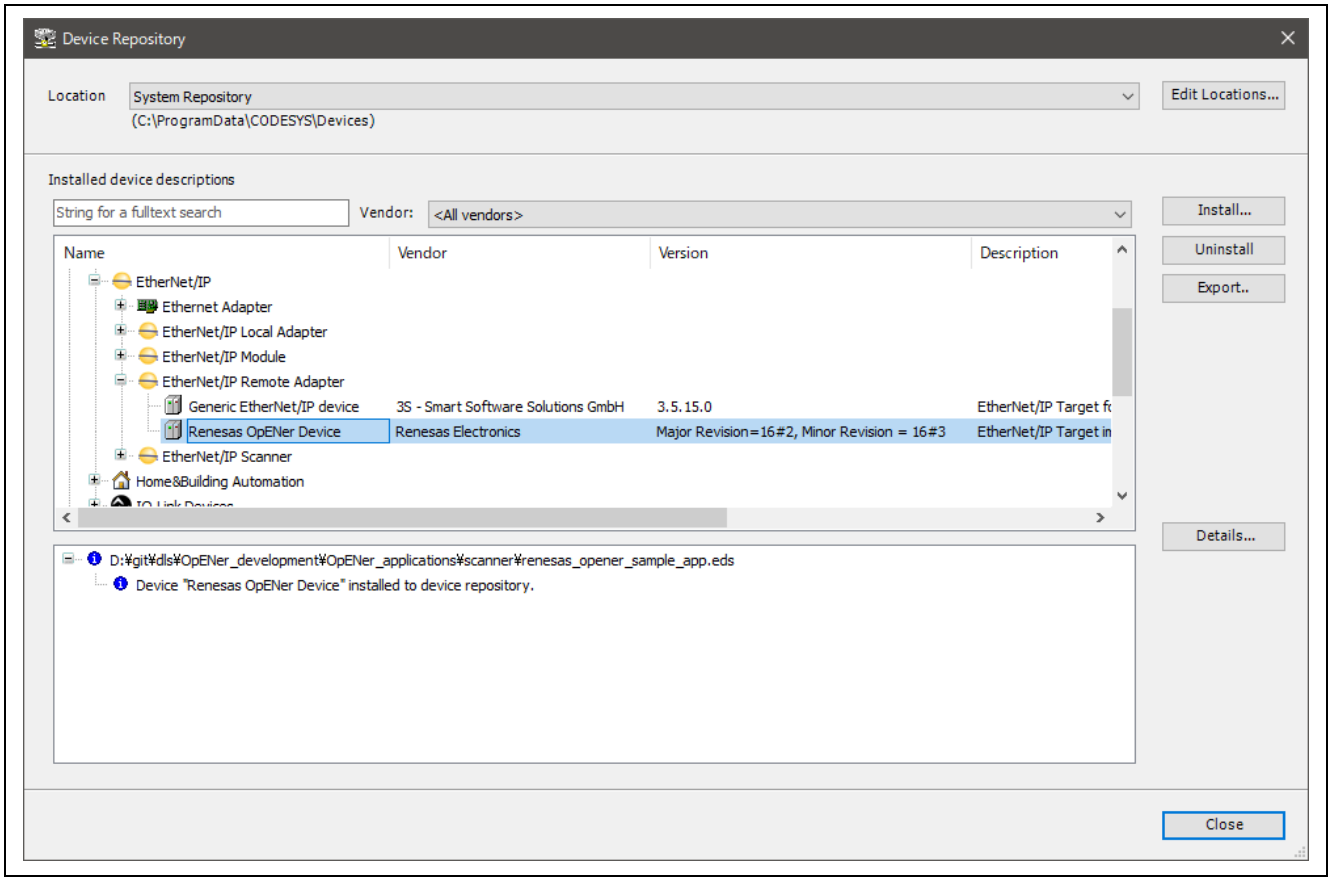


Figure 4-7 EtherNet/IP Remote Adapter

Preparation for using CODESYS is now complete. Continue with the program operation in Chapter 5 and then operate CODESYS again in Chapter 6.

5. Running the Sample Application

Before following this chapter, please look at Section 0 and 3.3 for board setup.

The setup differs depending on the IDE.

- When using e² studio, refer to section 5.1.
- When using EWARM, refer to section 5.2.

5.1 Setup sample project for e² studio

5.1.1 Startup e² studio

1. Open the e² studio and select a directory as workspace.
2. Click “Open Projects from File System…” in File tab.

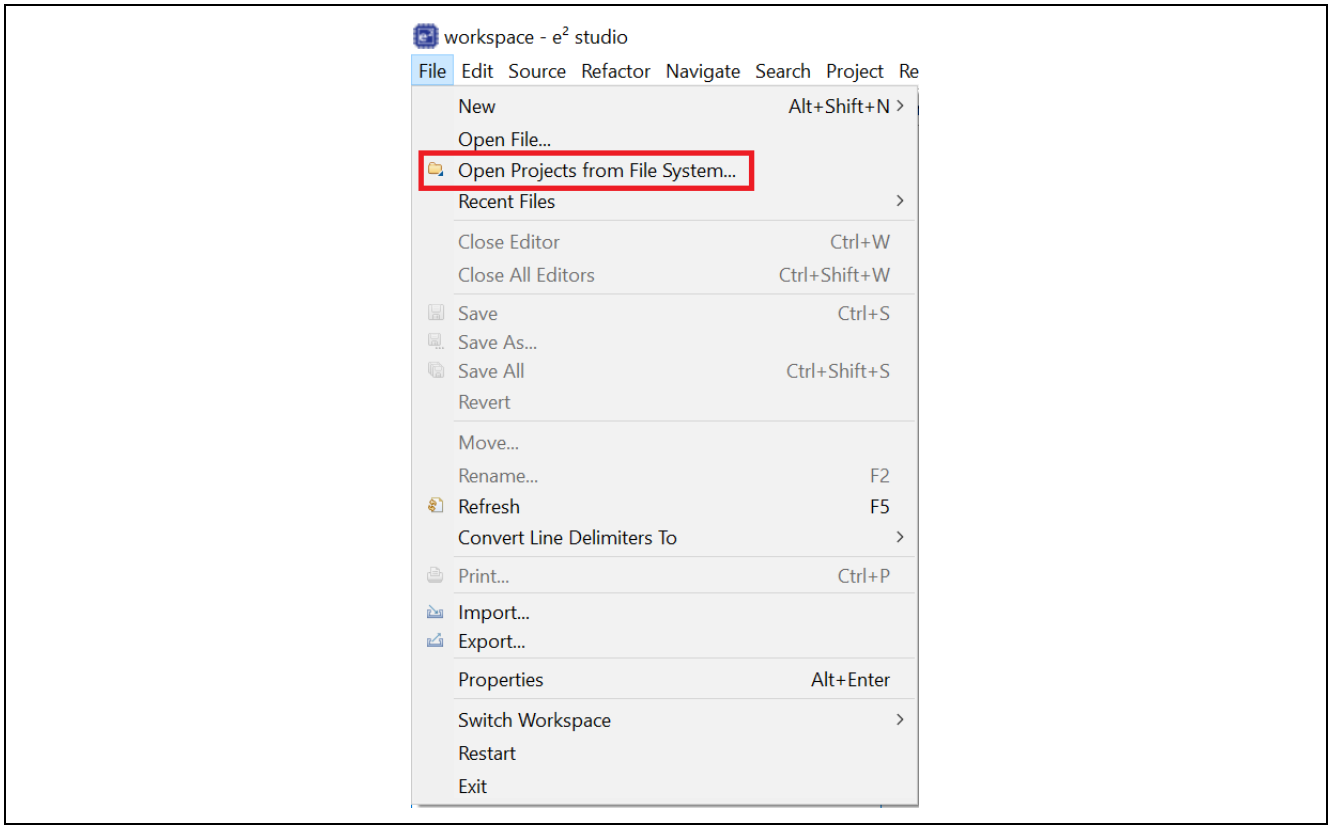


Figure 5-1 e² studio File tab

3. Import the project folder.

   For RZ/T2M, import “\project\rzt2m_rsk\opener_single\e2studio”.

   For RZ/N2L, import “\project\rzn2l_rsk\opener_single\e2studio”.

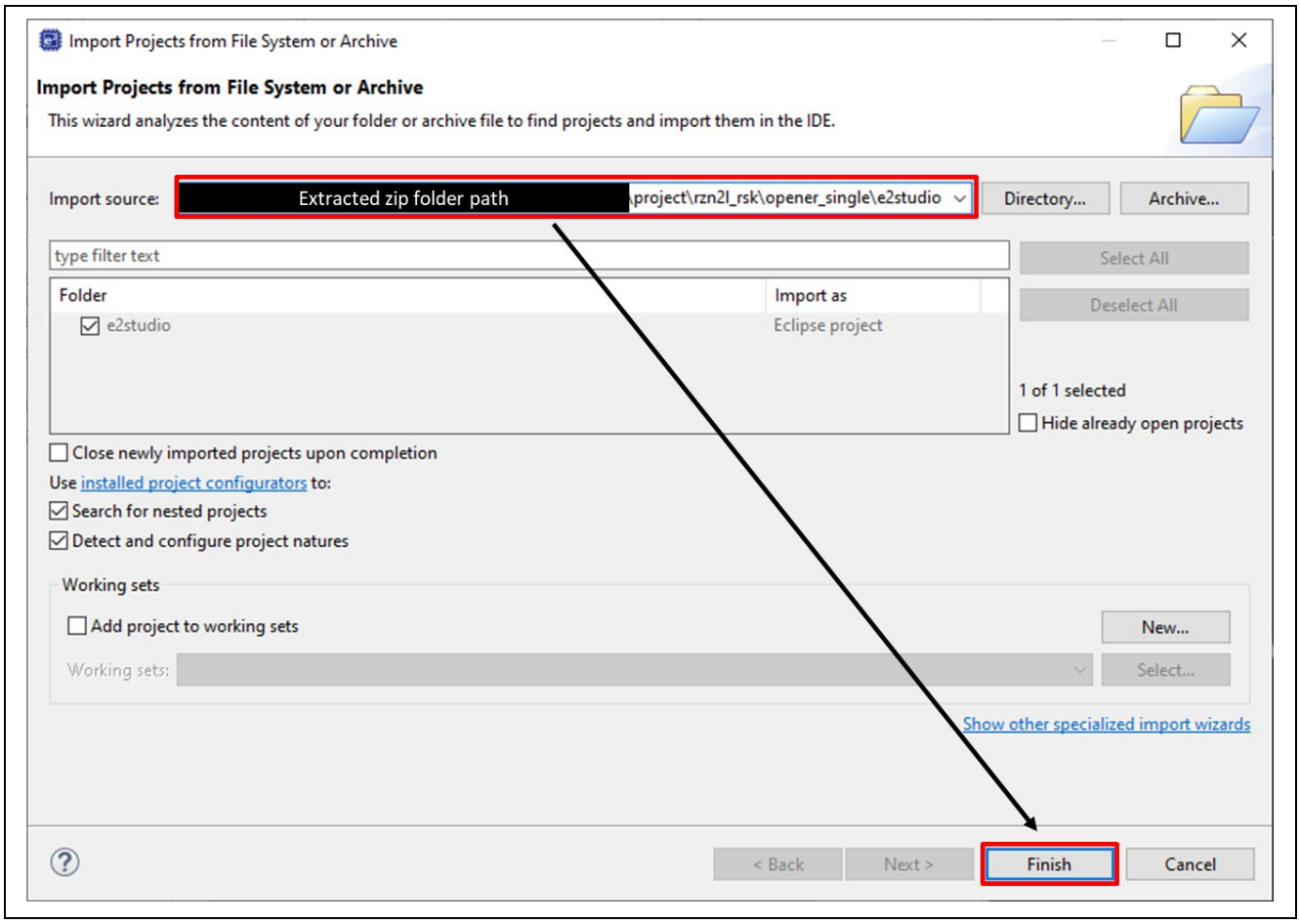


Figure 5-2 Import project on e² studio

5.1.2 Board IP Address Setting

The IP address is set in src/renesas/application/opener_port_instance.c.

The following addresses are used in the example:

IP address : 192.168.1.170

Subnet mask : 255.255.255.0

Default gateway : 192.168.1.1

Host Name : OPENER_NETIF0

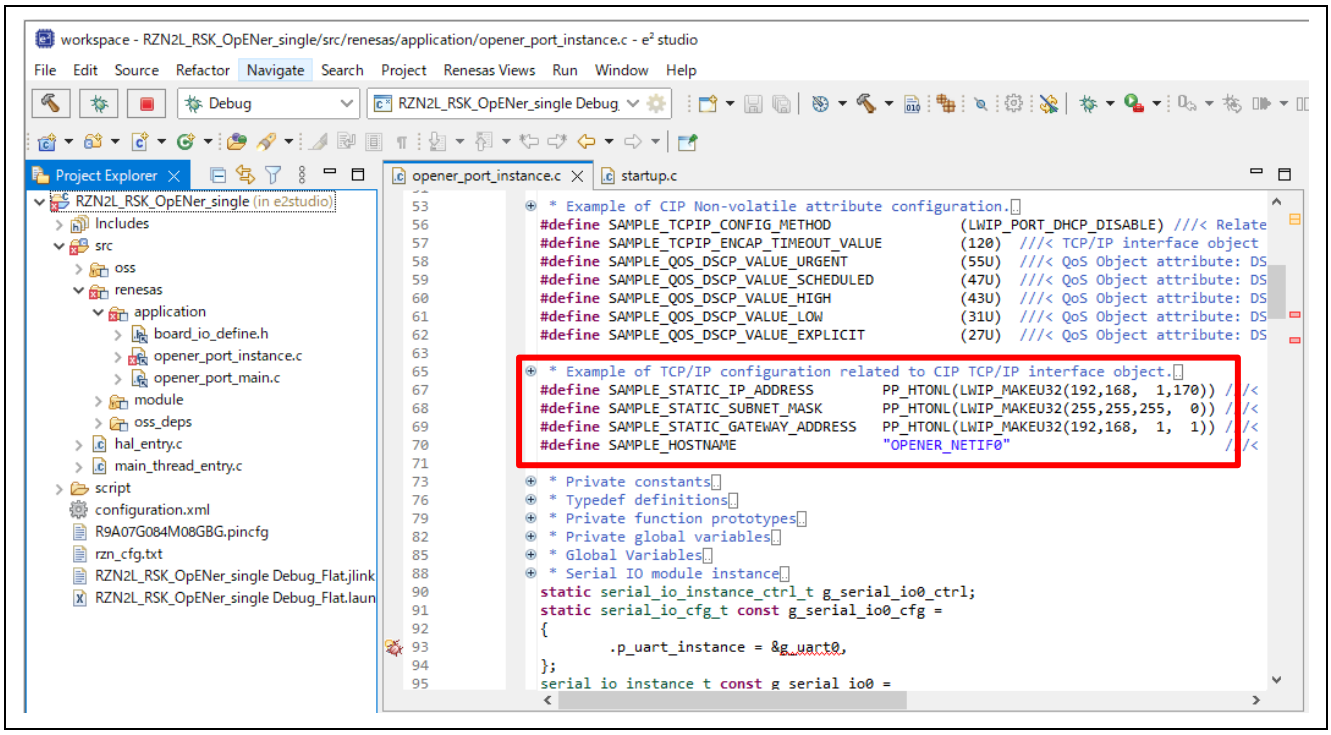


Figure 5-3 Static IP address

5.1.3 How to generate source code and how to build

1. Click the Configuration.xml.

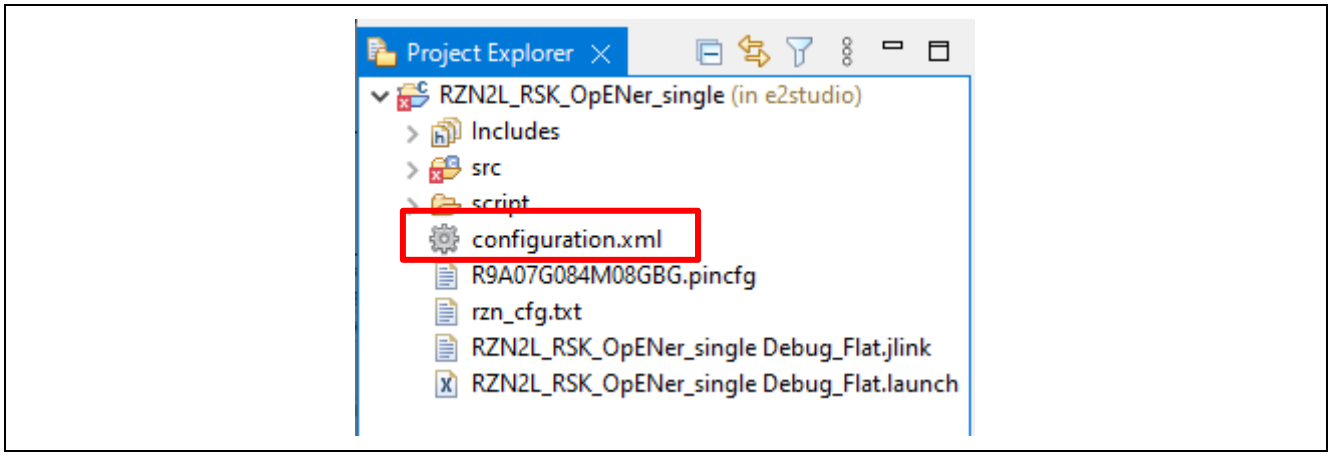


Figure 5-4 Configuration

2. Click ‘Generate Project Content’ button then generate rzt, rzt_gen, rzt_cfg (rzn, rzn_gen, rzn_cfg) folder.

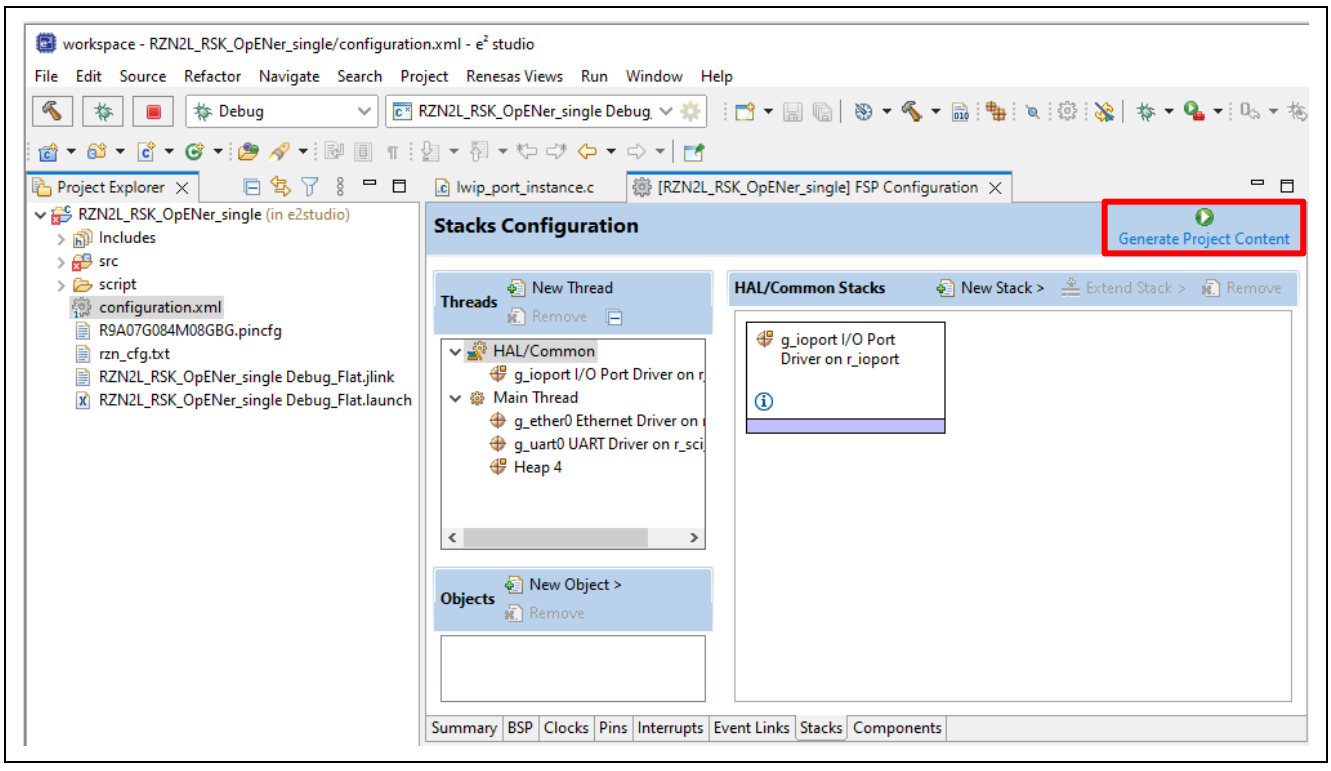


Figure 5-5 Generate Project Content

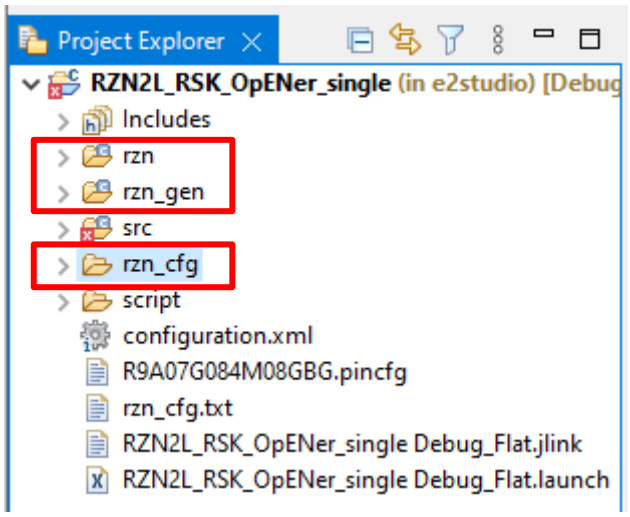


Figure 5-6 Generate project folder

3. Click the Build button in tool bar to build the project and confirm that there is no error message in build message log.

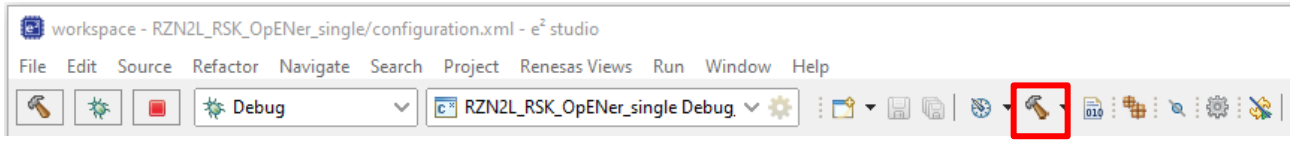


Figure 5-7 Build button

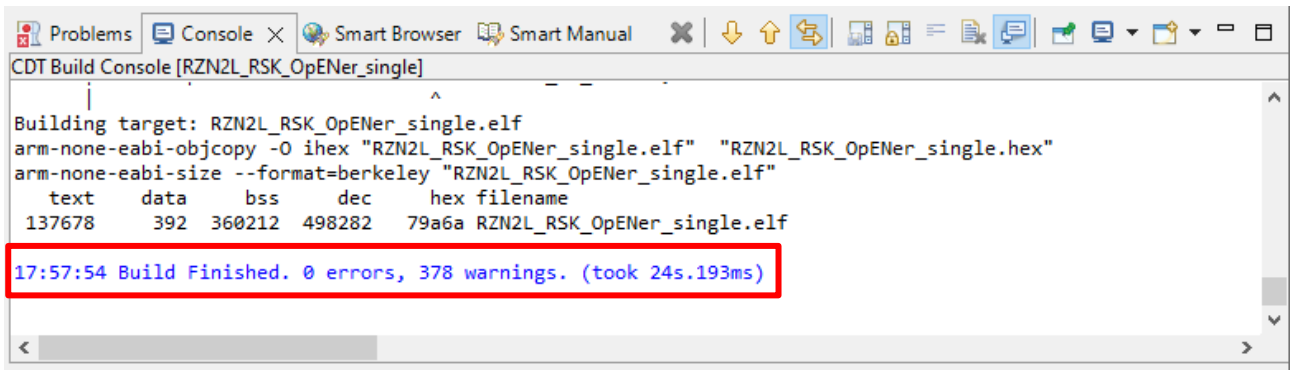


Figure 5-8 Build message

5.1.4 Download application and run debugger

1. Click the Debug button in tool bar to download the built application program and launch the debugger.

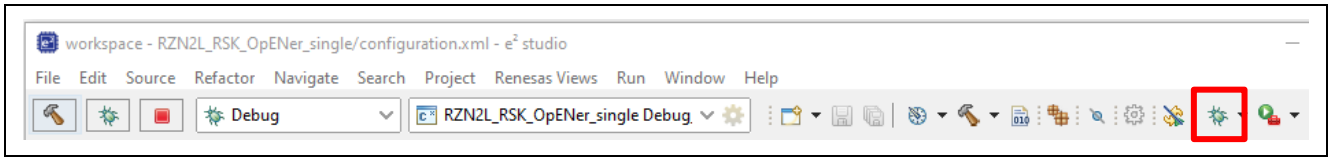


Figure 5-9 Debug button

2. Click to “Switch” button.

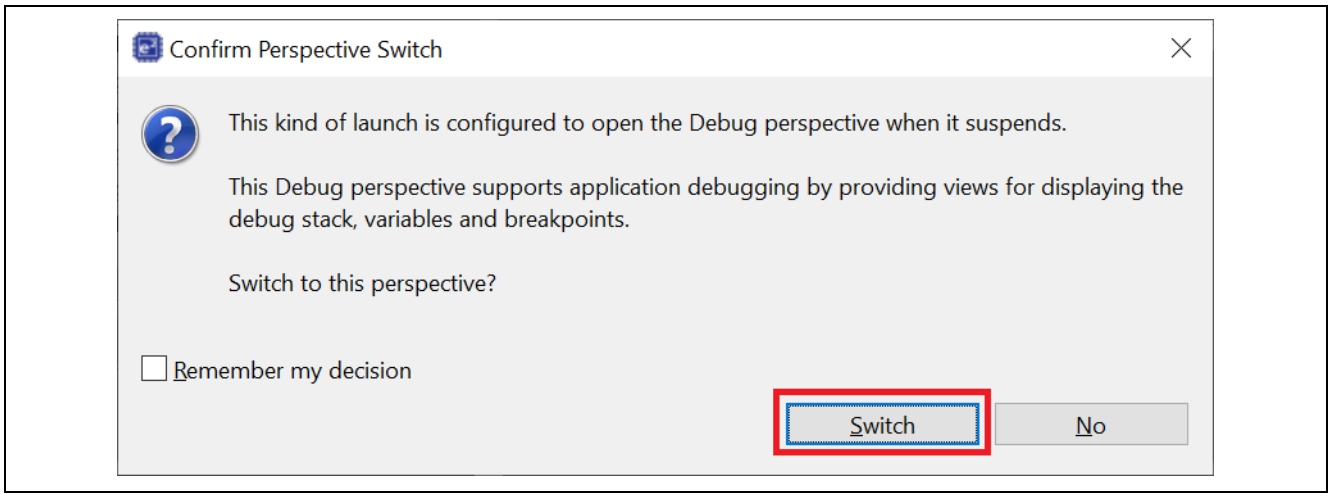


Figure 5-10 Confirm Perspective Switch

3. The program will break at “system_init” for startup.

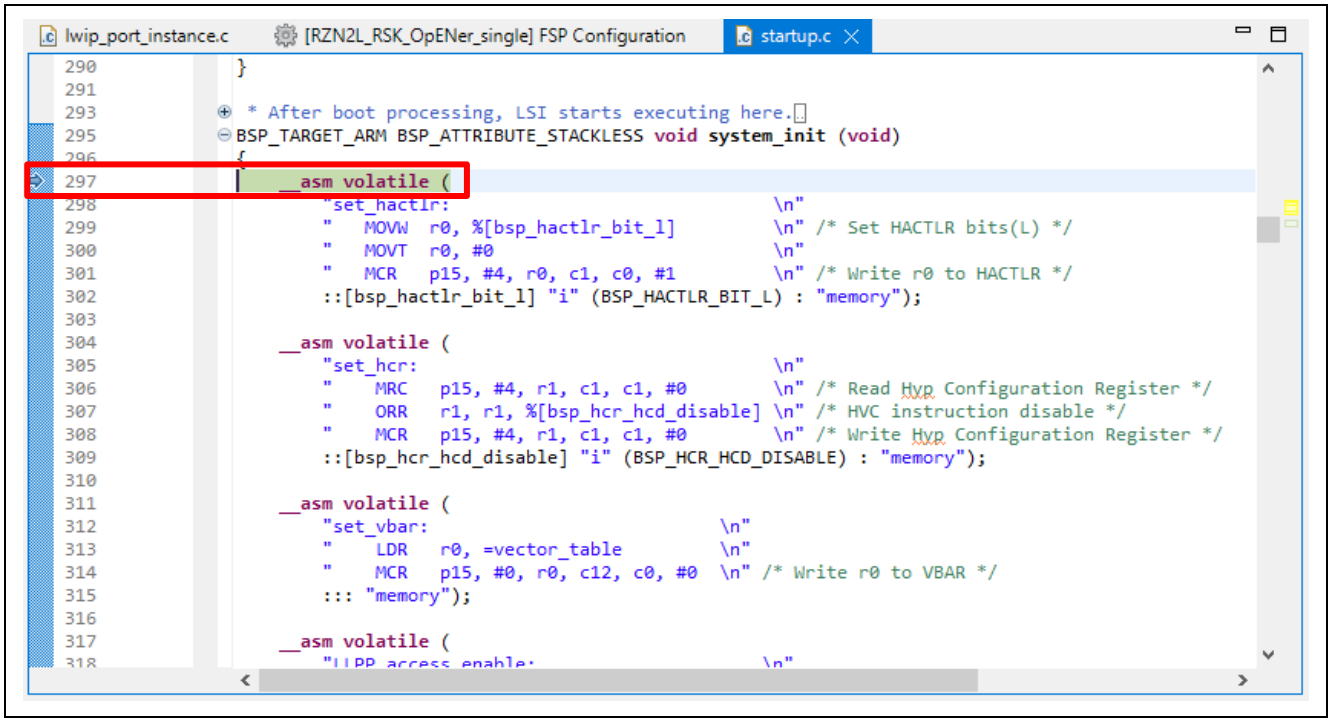


Figure 5-11 Break point 1

4. Before running the loaded program, please change the CPSR register of CR52 general register on Registers tabs.

- Change the “T” register bit (bit 5 in CPSR register), which is Thumb execution state bit, from “1” to “0” to switch the instruction mode from “Thumb” to “Arm”.

  ➢ When the register value is “0x000001**f**a”, set it to “0x000001**d**a”.

If the value of “T” bit in CPSR register is not changed, please note that the program does not work properly when running.

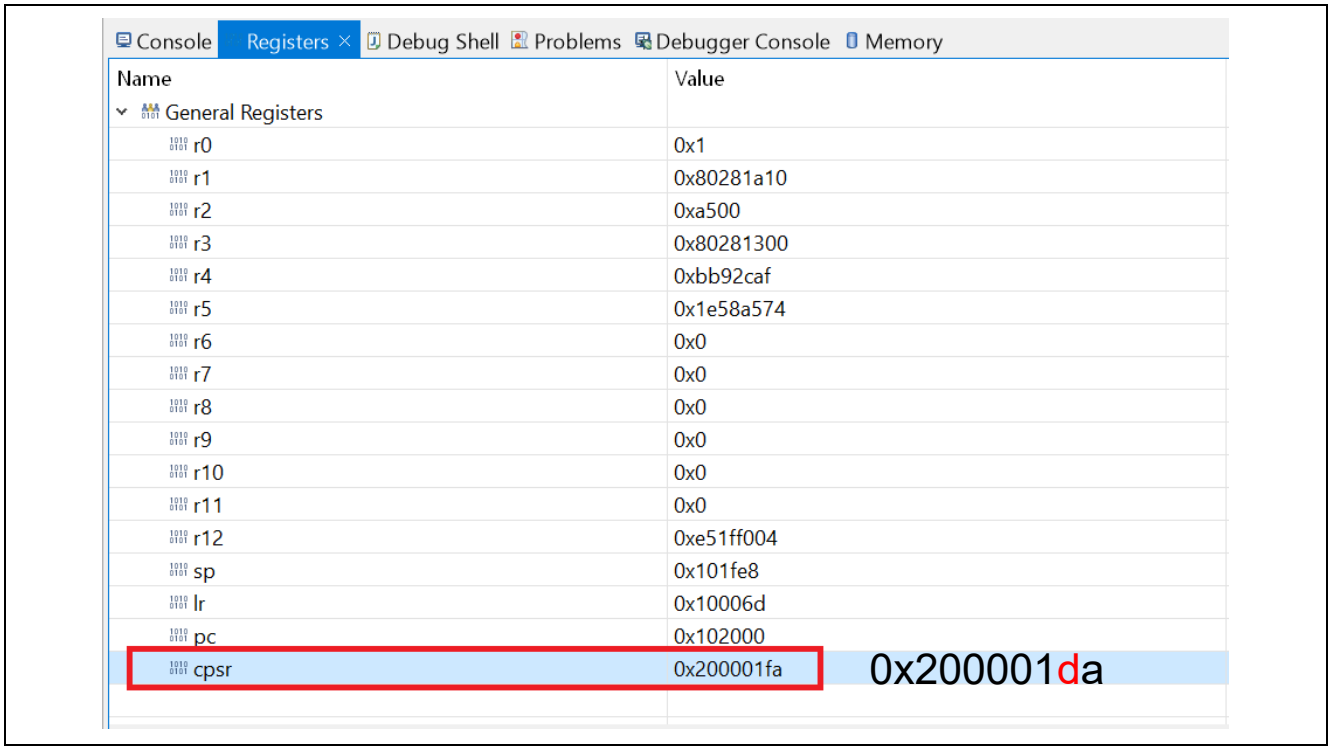


Figure 5-12 CPSR register of CR52 generic register on Registers tab

5. Click the Resume button. The program will break at the first of main function.

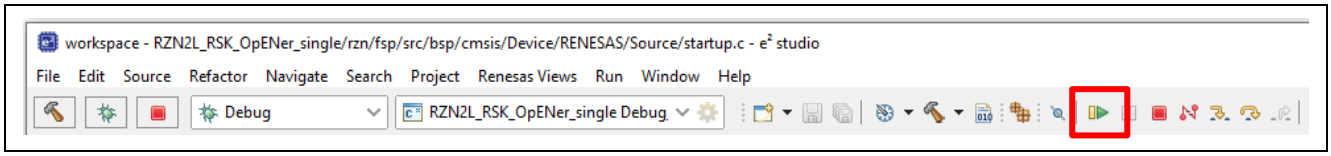


Figure 5-13 Resume button

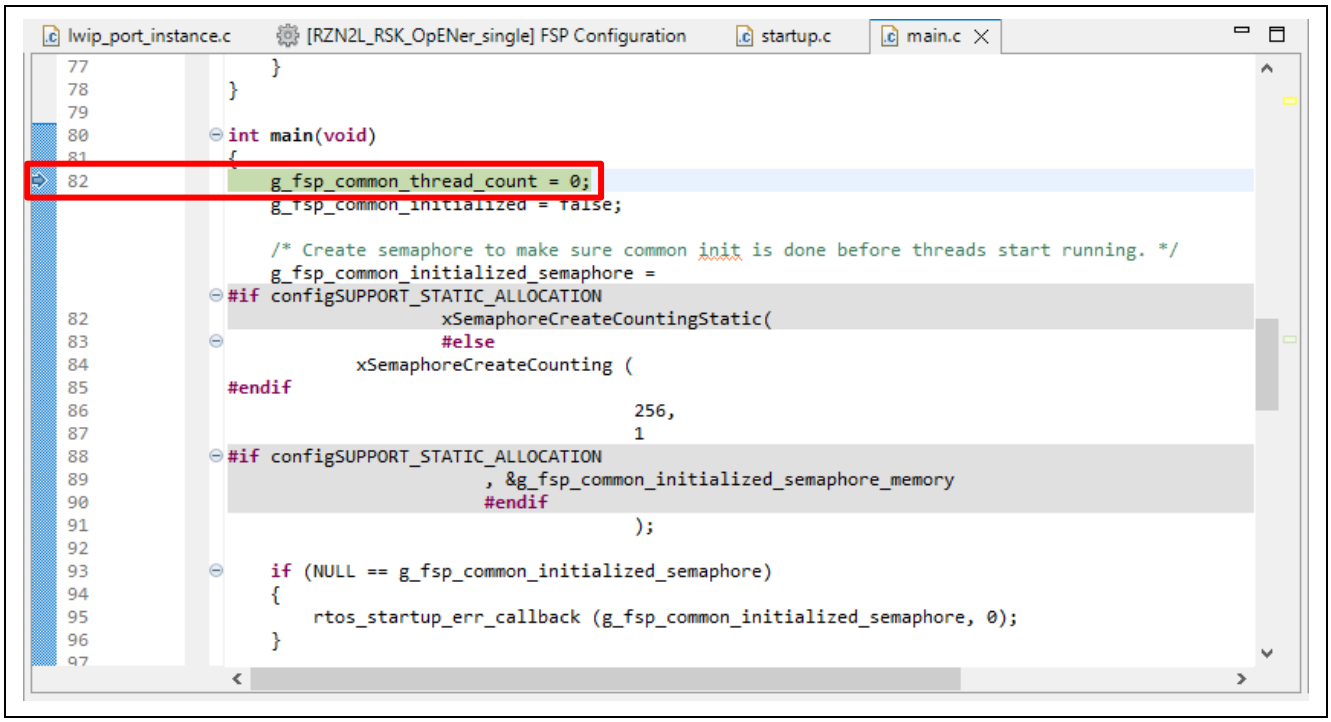


Figure 5-14 Break point 2

6. Click the Resume button again to execute the program.

5.2 Setup sample project for EWARM

5.2.1 Startup EWARM

1. Open the EWARM.
2. Click “Open Workspace…” in the File tab.

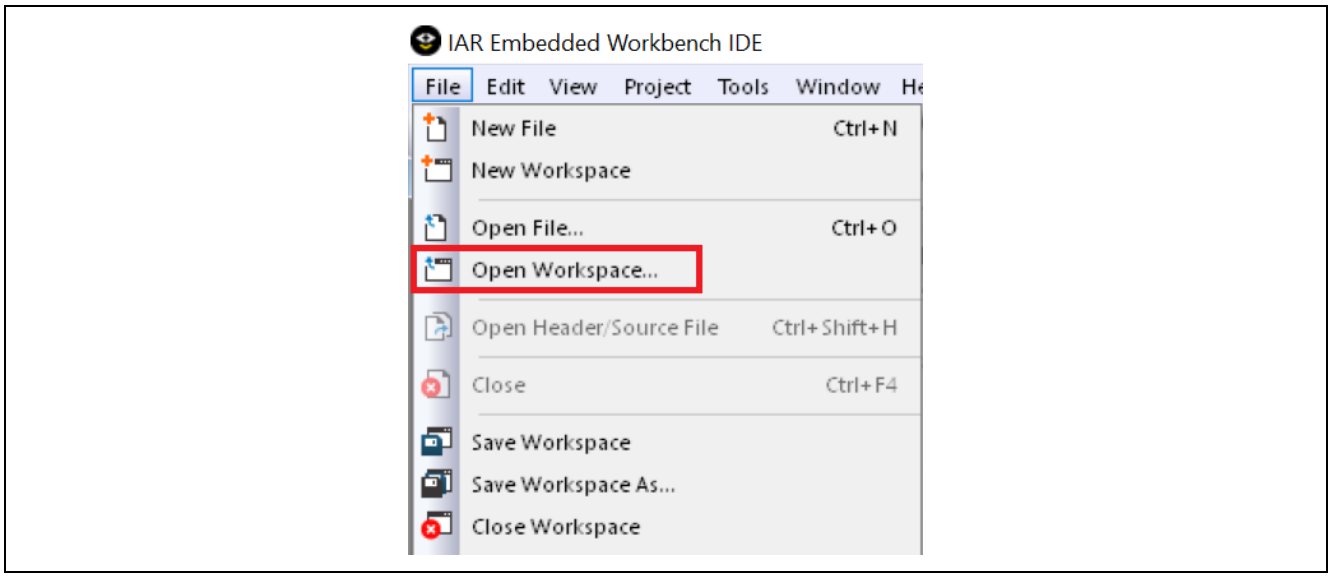


Figure 5-15 EWARM file tab

3. Select the Workspace File(.eww) and click the Open button.
   For RZ/T2M, select “\project\rzt2m_rsk\opener_single\ewarm\RZT2M_RSK_OpENer_single.eww”
   For RZ/N2L, select “\project\rzn2l_rsk\opener_single\ewarm\RZN2L_RSK_OpENer_single.eww”

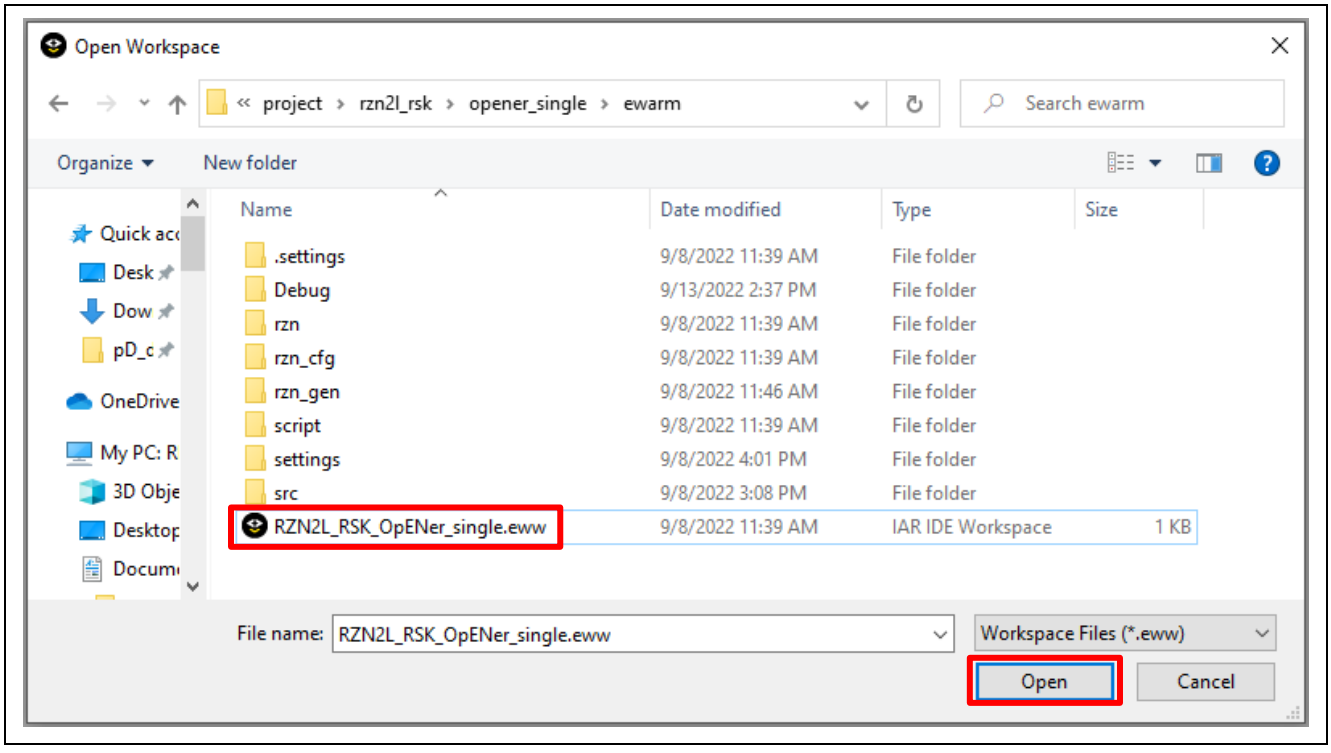


Figure 5-16 Open project file

5.2.2 Board IP Address Setting

The IP address is set in \common\renesas\application\opener_port_instance.c.

The following addresses are used in the example:

IP address : 192.168.1.170

Subnet mask : 255.255.255.0

Default gateway : 192.168.1.1

Host Name : OPENER_NETIF0

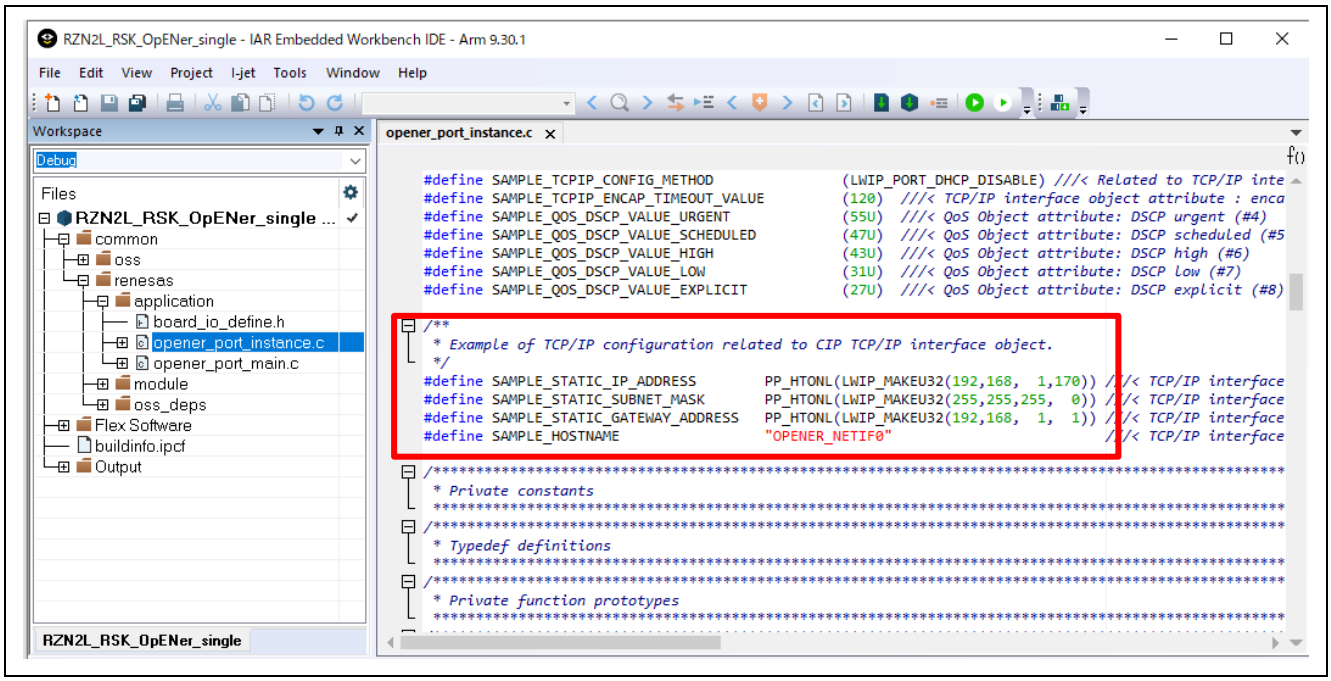


Figure 5-17 Static IP address

5.2.3 How to generate source code and how to build

1. Click the “Tool” -> “FSP Smart Configurator” on tool bar. If you have not set up FSP Smart Configurator yet on EWARM, refer to r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf in which section 5.4 describes how to set up it.

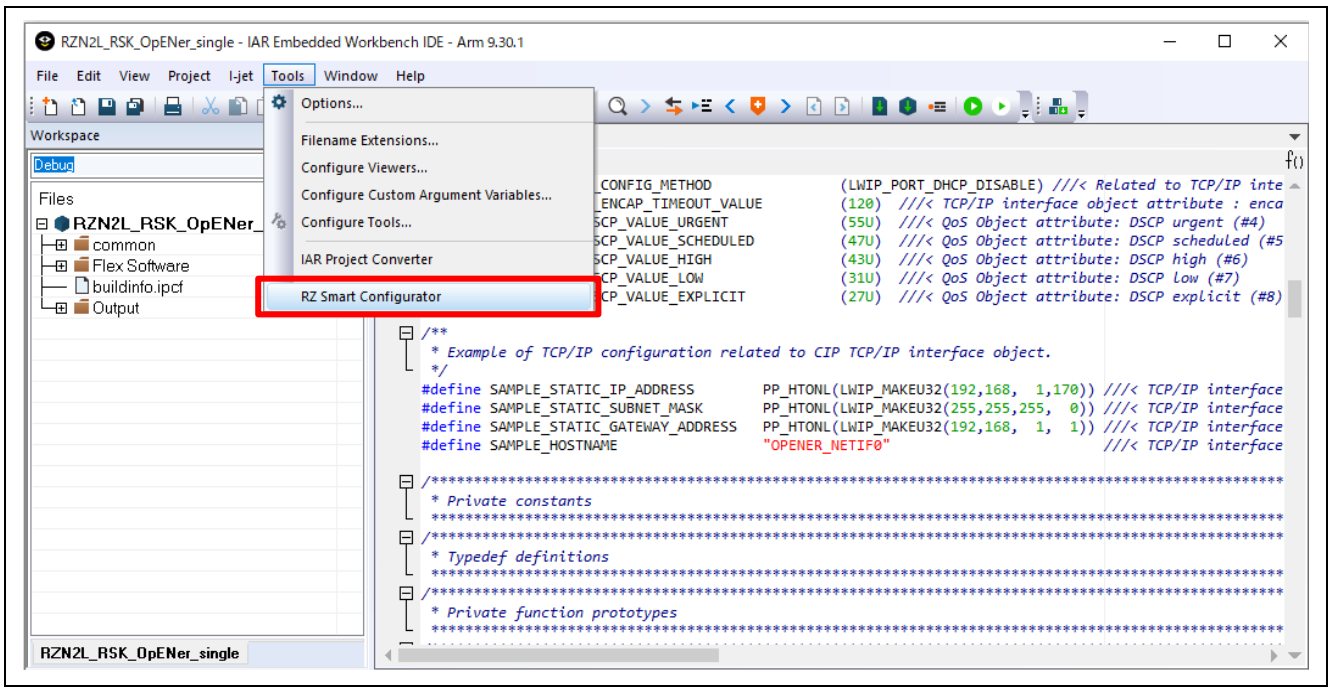


Figure 5-18 Tools tab

2. Click ‘Generate Project Content’ button then will be generate rzt, rzt_gen, rzt_cfg (rzn, rzn_gen, rzn_cfg) folder.

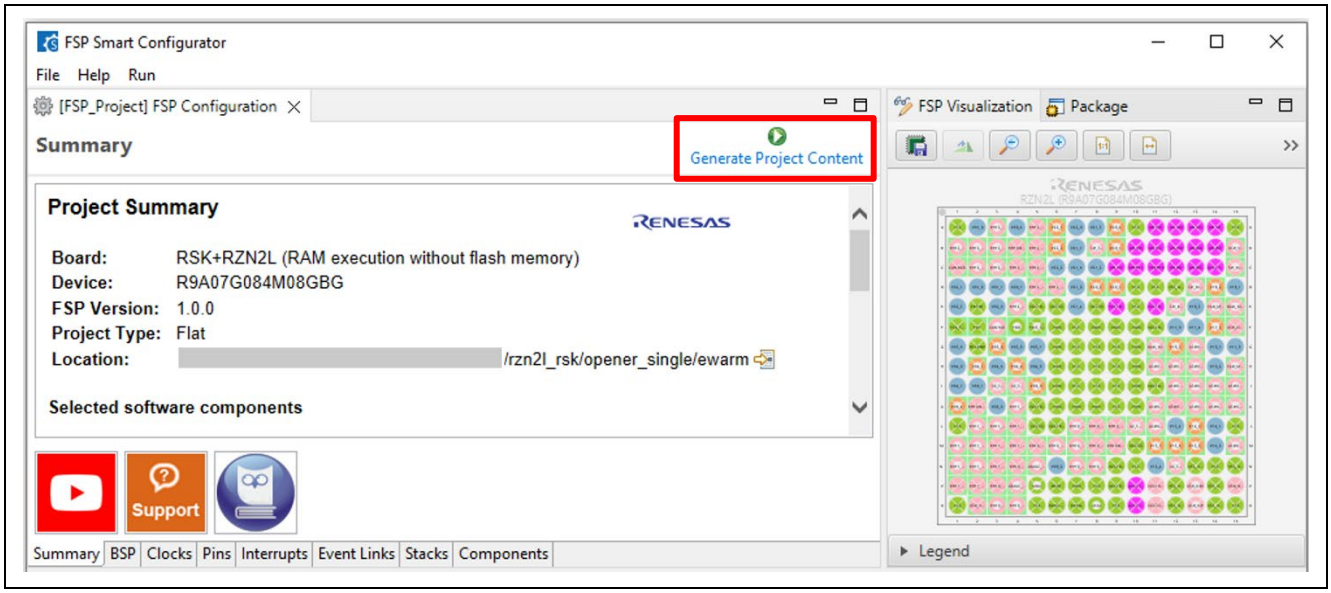


Figure 5-19 FSP SC Smart Configurator

3. Click the Make button on tool bar to build. Once the build is completed, the build message is displayed in the Build Console window that displays compilation target files and the number of error/warnings.

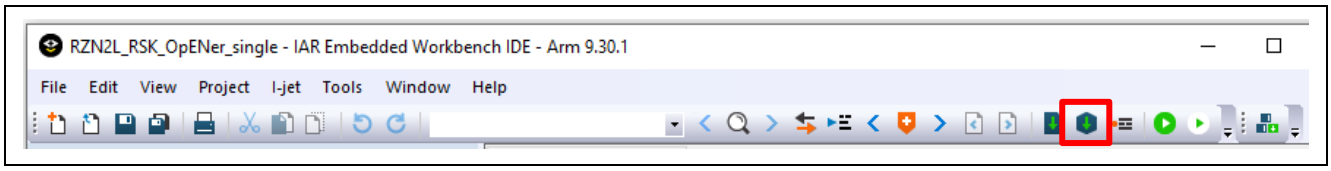


Figure 5-20 Make button 1

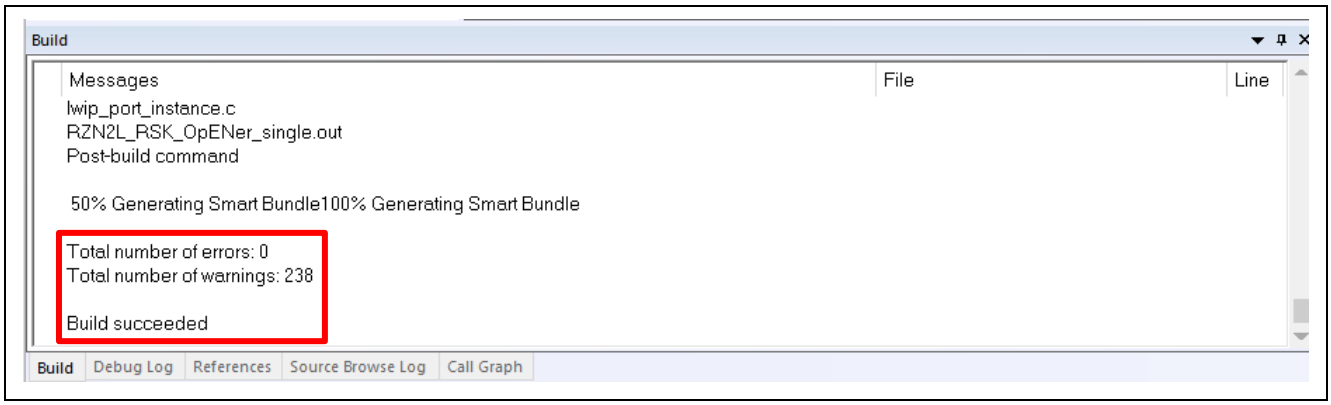


Figure 5-21 Make button 2 and Build console

5.2.4 Download application and run debugger

1. Click the Debug button in tool bar to download the built application program and launch the debugger. The program will break at the first code in main function.

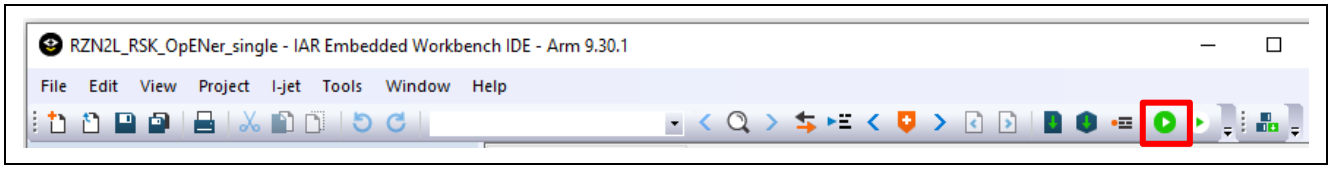


Figure 5-22 Debug button

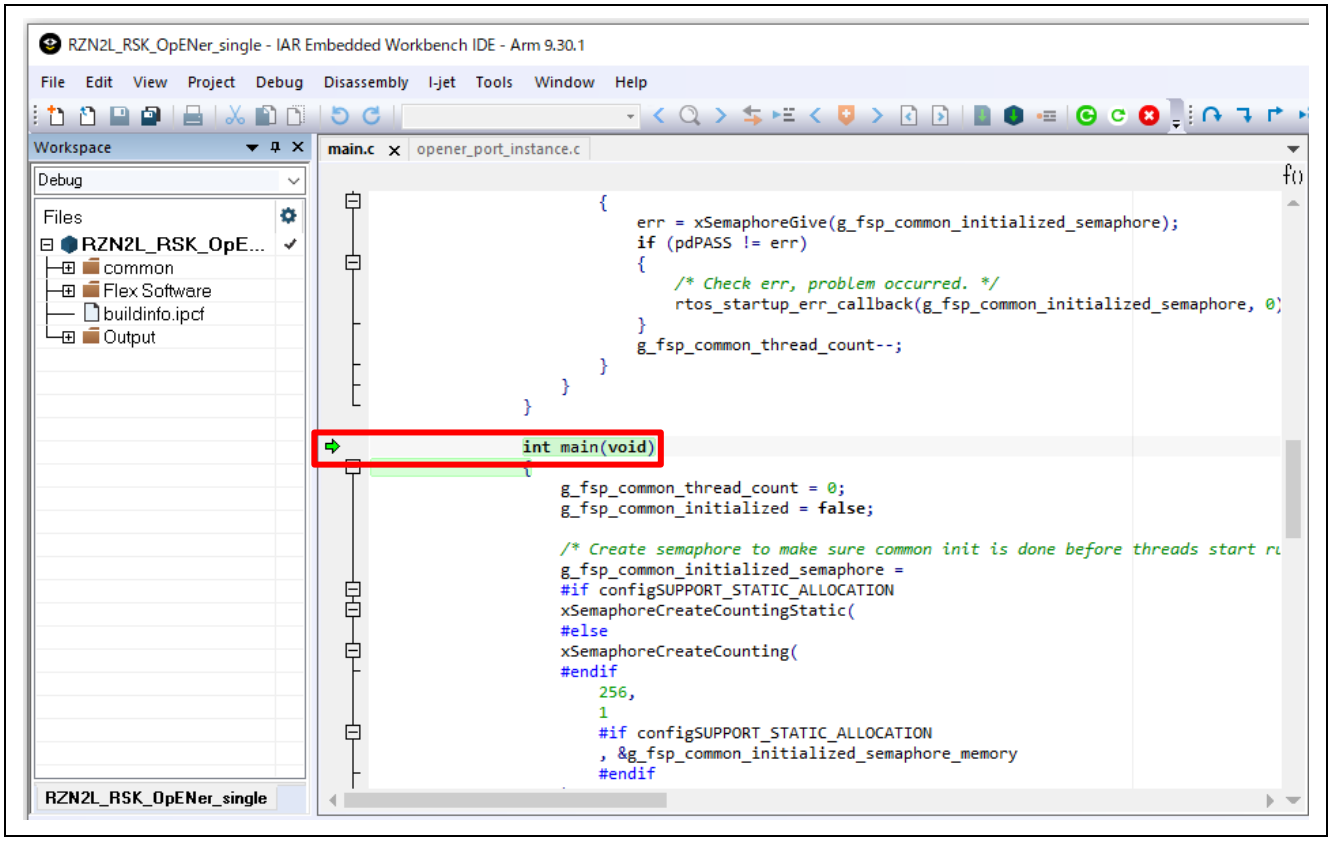


Figure 5-23 Break point

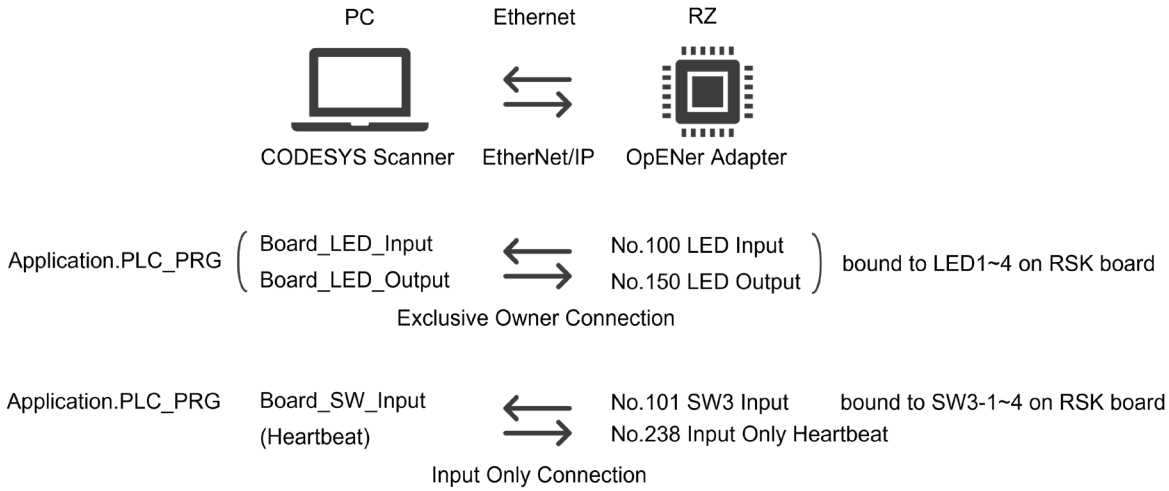
2. Click the Go button.

Figure 5-24 Go button

6. Demonstration of the application with the CODESYS

6.1 Application Behavior

For demonstration, the application of OpENer RZ/T2M, RZ/N2L port has an Exclusive Connection and an Input Only Connection. The connections between the RZ/T2M, RZ/N2L application and the CODESYS project application is shown below.



The PLC program of CODESYS project is shown below. The PLC program is described by ST (Structured Text) language.

```
CycleCounter := CycleCounter+Board_SW_Input;
IF CycleCounter > CyclePerTick THEN
   CycleCounter := CycleCounter-CyclePerTick;
   IF 0 < Board_LED_Input AND Board_LED_Input < 8 THEN
      Board_LED_Output := Board_LED_Input * 2;
   ELSE
      Board_LED_Output := 1;
   END_IF
END_IF
```

- The Exclusive Owner Connection is bound to LED on RSK board.
  - The PLC program make the LEDs light by shifting every CyclePerTick.
- The Input Only Connection is bound to SW3-1 ~ SW3-4 on RSK board.
  - The PLC program read the SW values and change the incrementation value of CycleCounter for controlling the frequency of LED light shifting.

CODESYS application can be shown page.

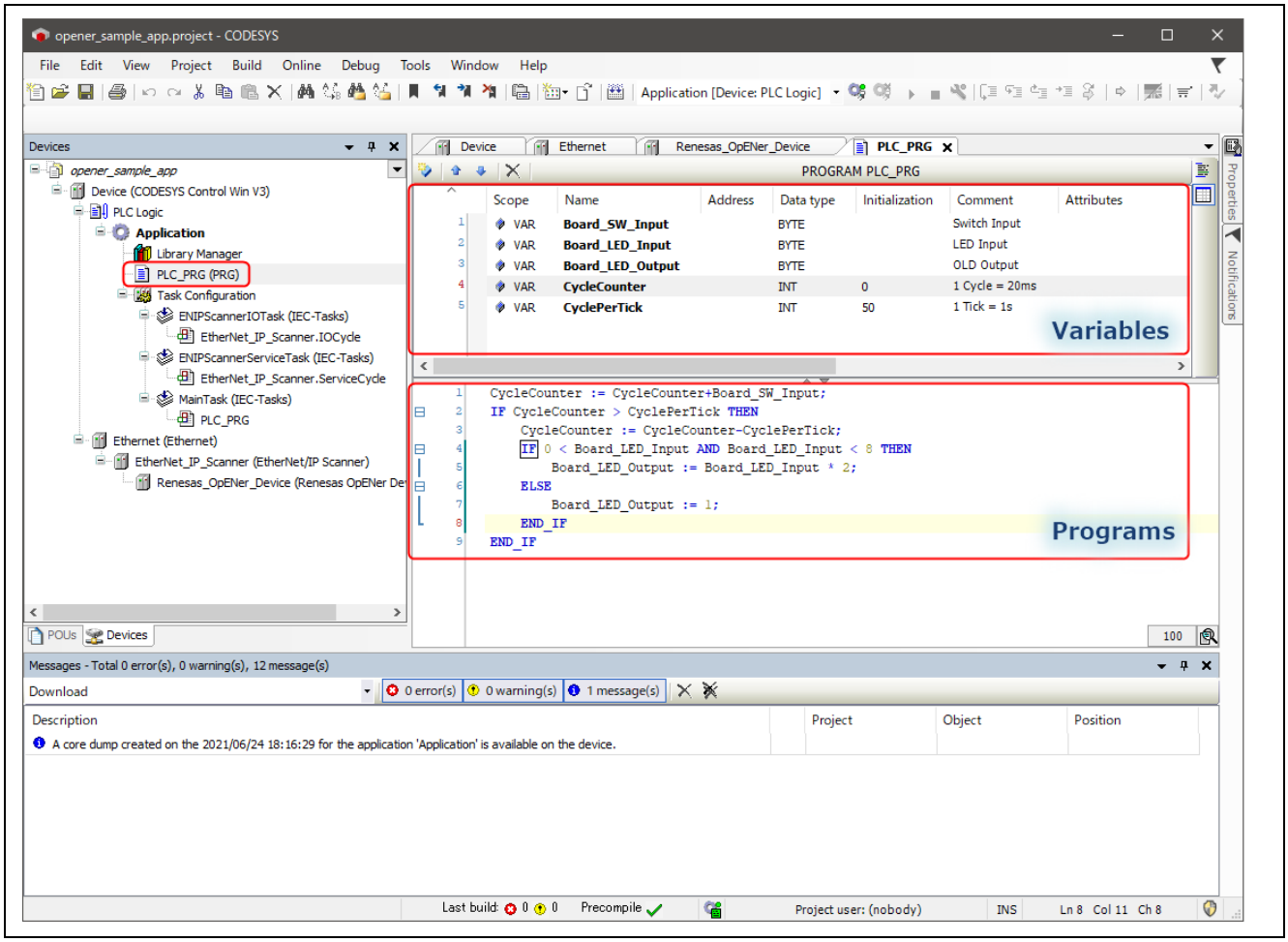


Figure 6-1 CODESYS Project included in this sample program

6.2 IP and MAC Address Configuration

6.2.1 IP Configuration

This program sets own IP and related parameters to the following values defined statically by “g_lwip_port0_netif_cfg” variable in “common\renesas\opener_port_instance.c”.

If changing the IP configuration, please change the following parameters.

Table 6-1 IP Configuration

Item	Value	Variable
IP Address	192.168.1.170	g_lwip_port0_netif_cfg.ip_address
Net Mask	255.255.255.0	g_lwip_port0_netif_cfg.subnet_mask
Gateway Address	192.168.1.1	g_lwip_port0_netif_cfg.gateway_address
Host Name	OPENER_NETIF0	g_lwip_port0_netif_cfg.p_host_name
DHCP	LWIP_PORT_DHCP_DISABLE	g_lwip_port0_netif_cfg.dhcp

If using DHCP, please set “g_lwip_port0_netif_cfg.dhcp” to “LWIP_PORT_DHCP_ENABLE”. After the program starts, DHCP process is executed to get an IP address dynamically. If the program gets an IP address, EtherNet/IP communication starts.

6.2.2 MAC Address Configuration

The MAC address is set to the following values defined statically by FSP Configurator.

Table 6-2 MAC Address Configuration

Item	Value (Decimal)
MAC Address	00:11:22:33:44:55

If changing the MAC address, please change the value on FSP configuration.

Regarding FSP configuration, please see the "RZ/T2M, RZ/N2L Getting Started with Flexible Software Package" (r01an6434ejxxxx-rzt2-rzn2-fsp-getting-started.pdf) document.

6.3 Startup Software PLC

6.3.1 Open CODESYS project

Please select “File” > “Open project...” in CODESYS tool bar and open “opener_sample_app.project” in “scanner/codesys”.

If the project is opened properly, the opened project is shown in “Device” section located at left in the following window.

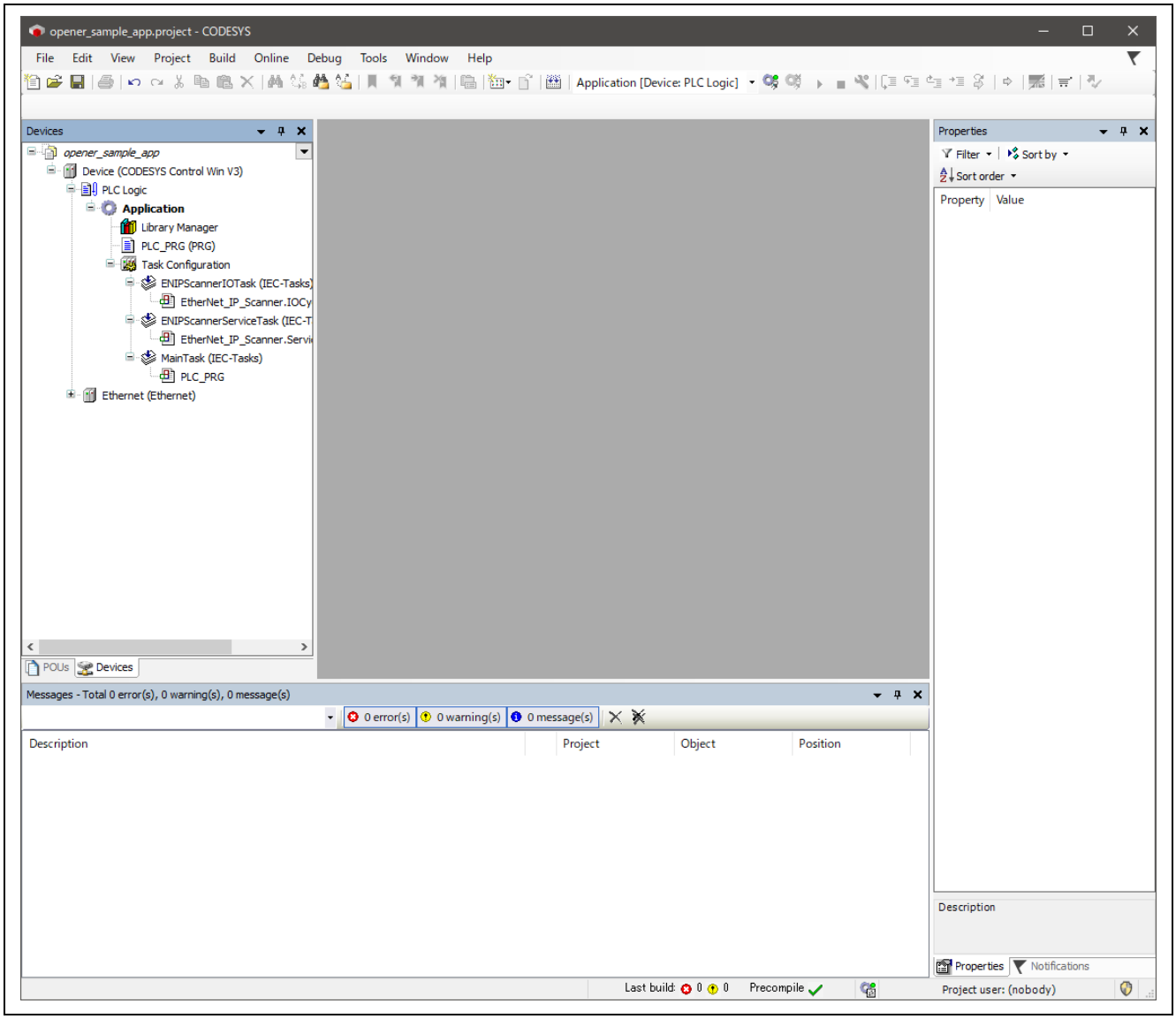


Figure 6-2 Open a CODESYS Project

6.3.2 Network Configuration

Please double-click “Device (CODESYS Control Win V3)” to open “Communication Settings” at center section, and please click “Scan Network...” to open “Select Device” window.

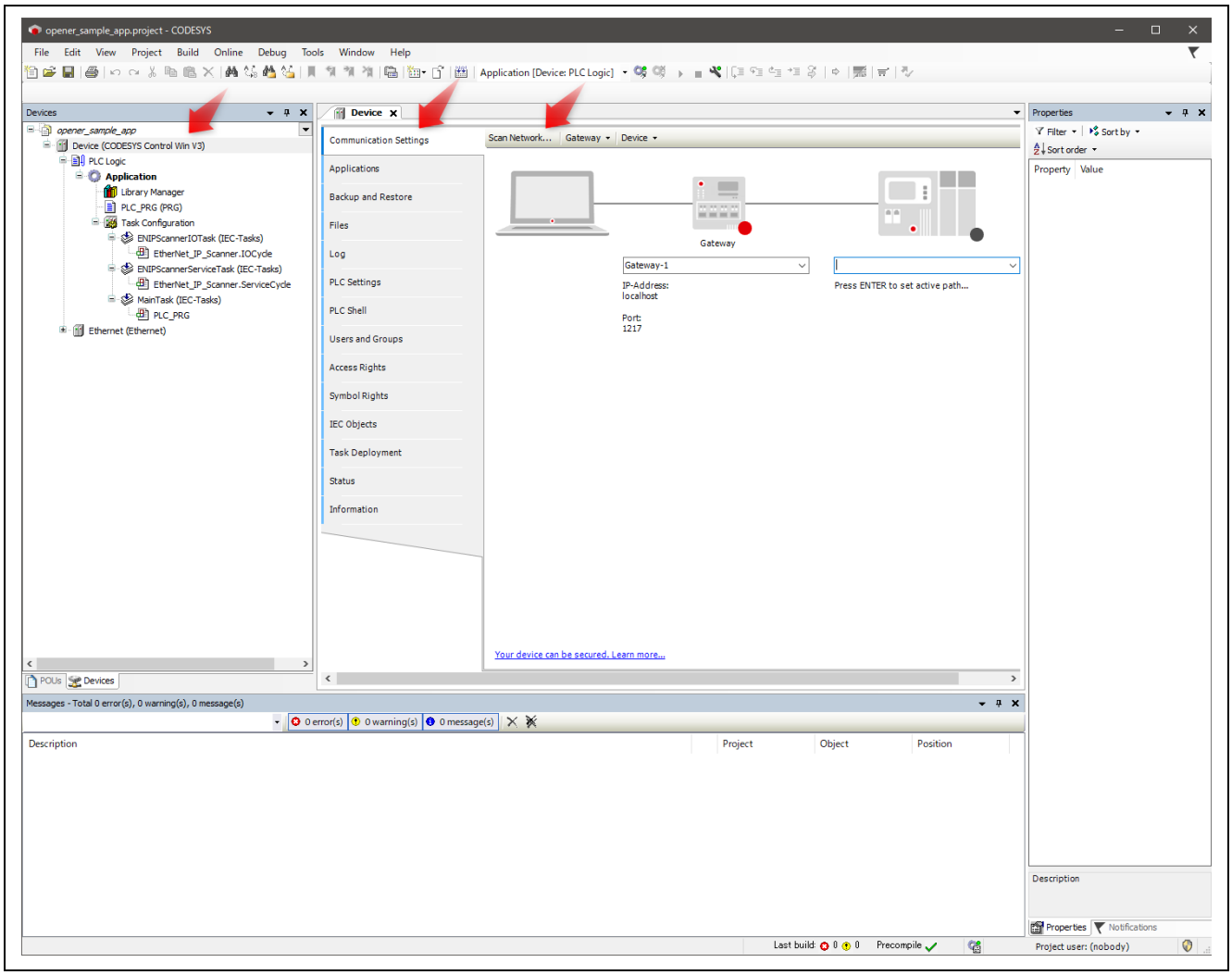


Figure 6-3 Communication Settings

If the software PLC is found after scanning network, the device name (here, PC name) is shown under Gateway tree. Please double-click this device name (in blue portion).

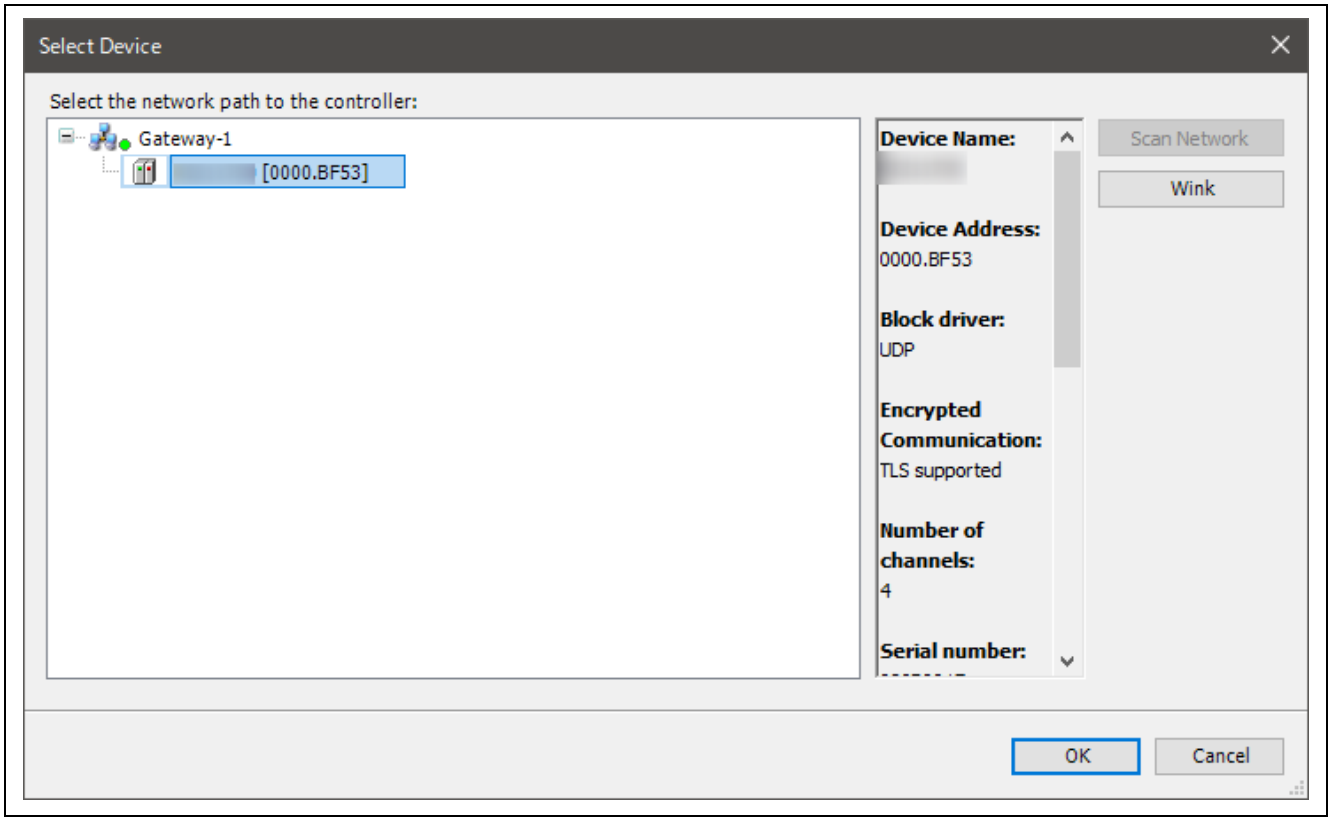


Figure 6-4 Select Device

If the network is configured properly, its configuration is shown in “Communication Settings” tab, and there are the green marks at gateway and device portions.

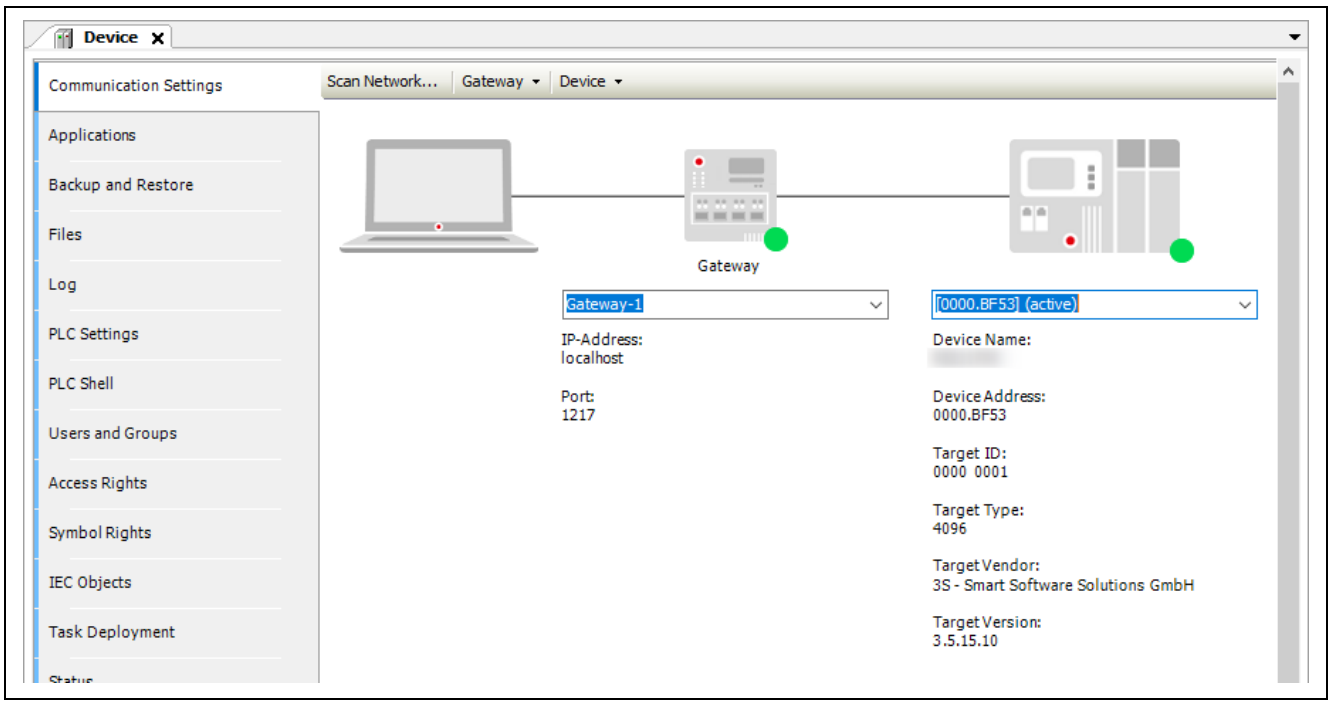


Figure 6-5 Green Marks at Gateway and Device Portions

6.3.3 Interface and IP address configuration

Please click “Ethernet (Ethernet)” in left section to open “Ethernet” tab in center section.

After that, please select “...” button to select network interface ethernet which is connected with RSK board, and please configure the IP address and related address values of the ethernet network interface.

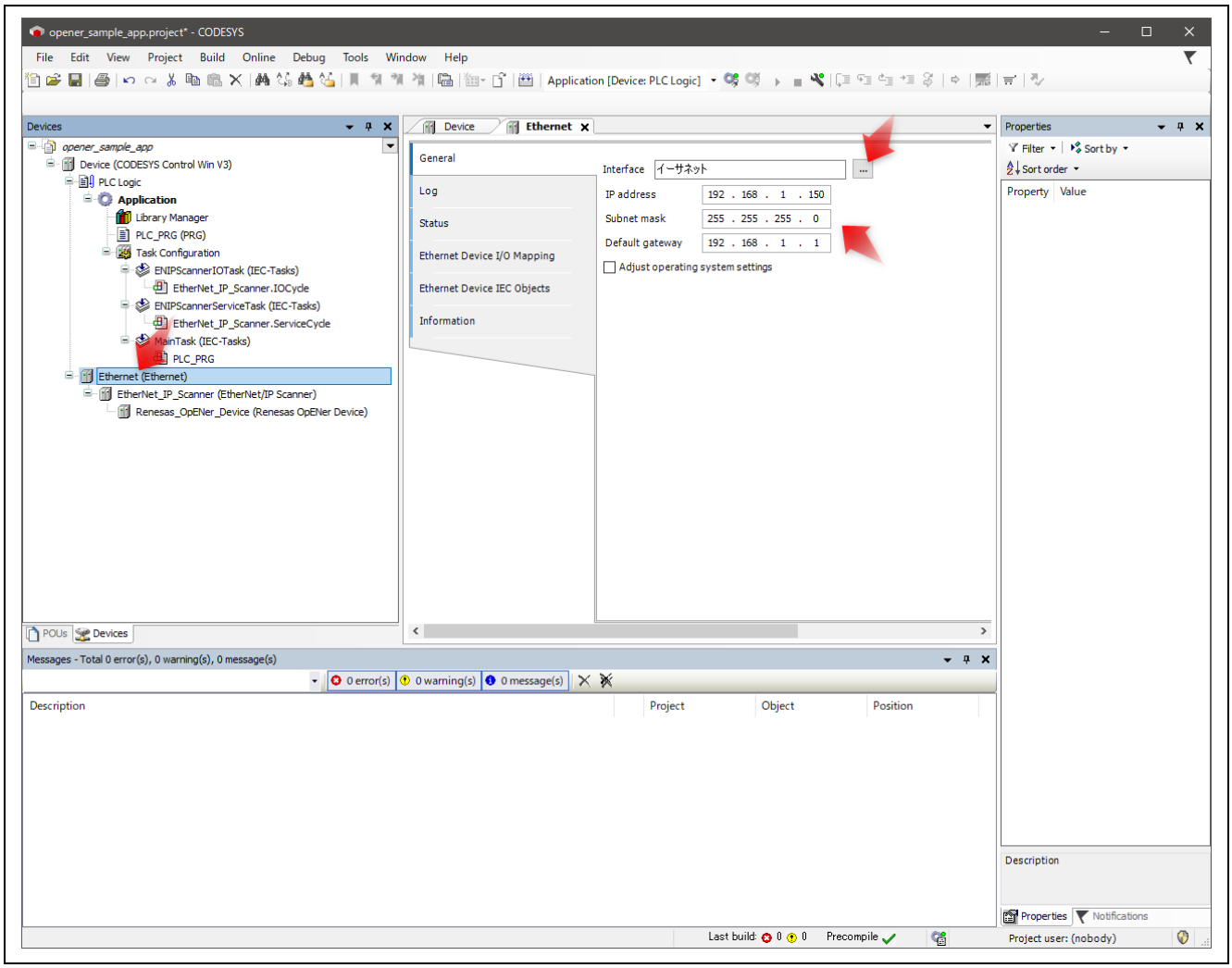


Figure 6-6 Open Ethernet tab

Next, please double-click “Renesas_OpENer_Device (Renesas OpENer Device)” in the left section to open “Renesas_OpENer_Device” tab in center section.

Enter the IP address of the sample code in the IP Address form. (Default setting is 192.168.1.170)

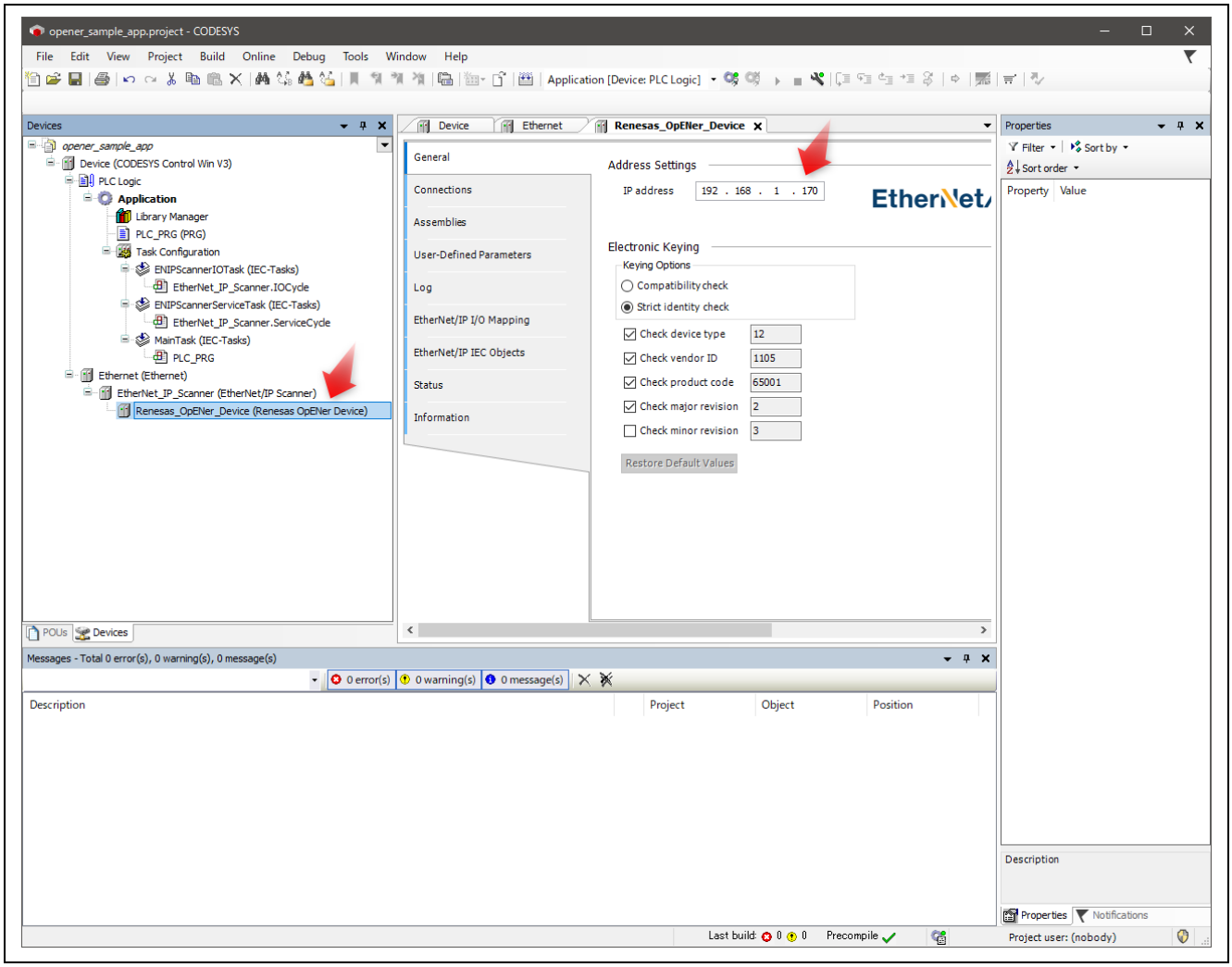


Figure 6-7 Renesas_OpENer_Device (Renesas OpENer Device)

6.4 Operation Check

6.4.1 Build Project and Start Application

Follow the following steps and figure to build the project and start the application.

1. Click “Build” button in the tool bar to build the CODESYS project.
2. Click “Login” button in the tool bar to login the network.
3. Click “Start” button in the tool bar to run network and application.

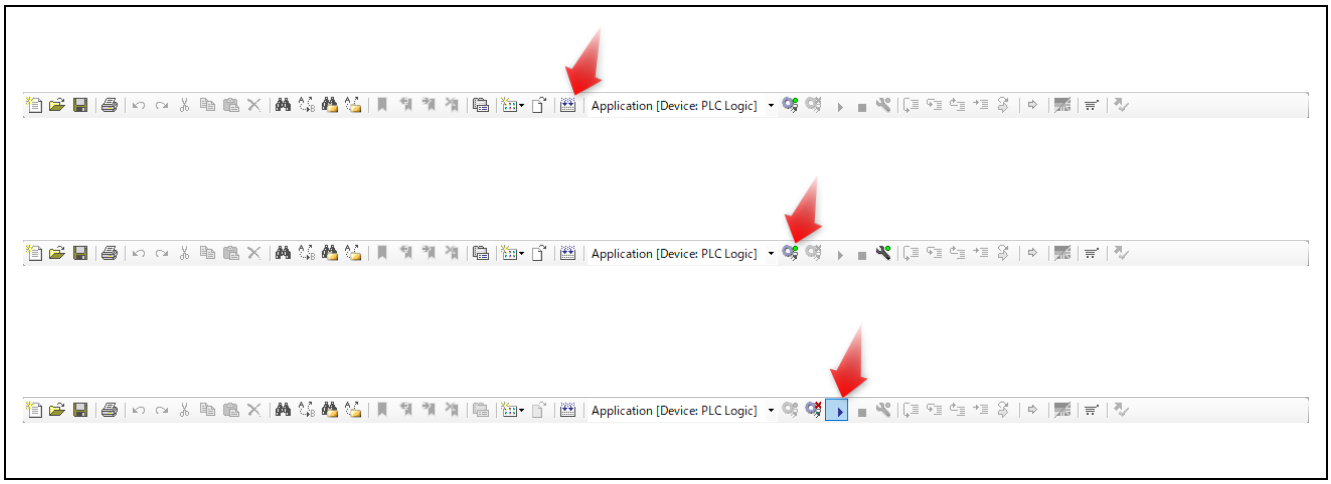


Figure 6-8 Build Project and Start Application

6.4.2 Check Network Connection

If the CODESYS application on PC connects with OpENer application on RZ/T2M(RZ/N2L) properly, “Device”, “Ethernet”, “EtherNet_IP_Scanner”, and “Renesas_OpENer_Device” in left section are marked with green cycle mark.

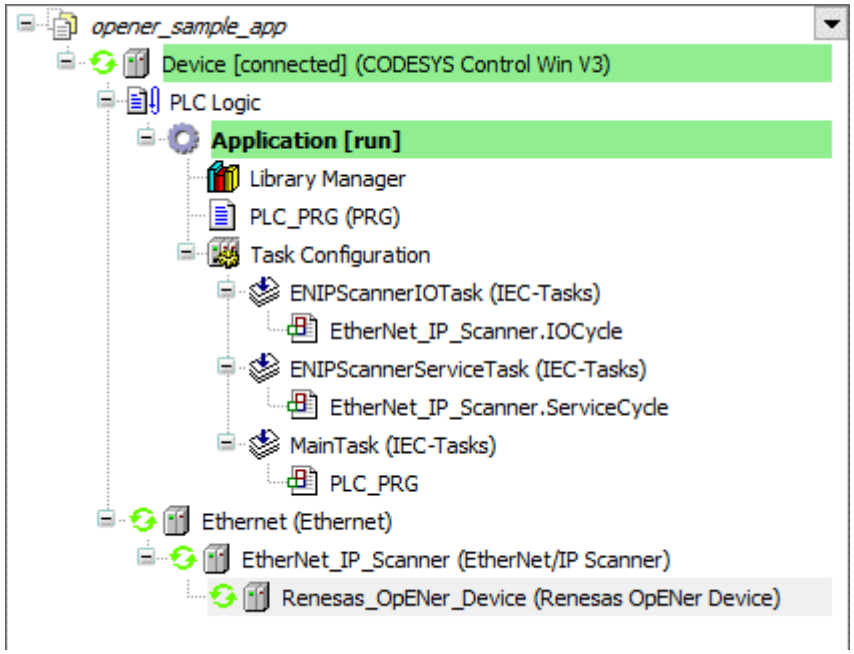


Figure 6-9 Check Network Connection

6.4.3 Check Application Behavior

Please open “EtherNet/IP I/O Mapping” page in “Renesas_OpENer_Device” tab.

This page shows the Exclusive Owner Connection and Input Only Connection mapping which indicates the connections between the CODESYS PLC application and the Assembly objects on OpENer application. The “Current Value” column indicates the LED and SW3 values.

- The Exclusive Owner Connection is bound to LED on RSK board.
  - The LEDs lights by shifting with [SW Value] Hz.
- The Input Only Connection is bound to SW3-1 ~ SW3-4 on RSK board.
  - The SW values indicates the frequency of LED light shifting.

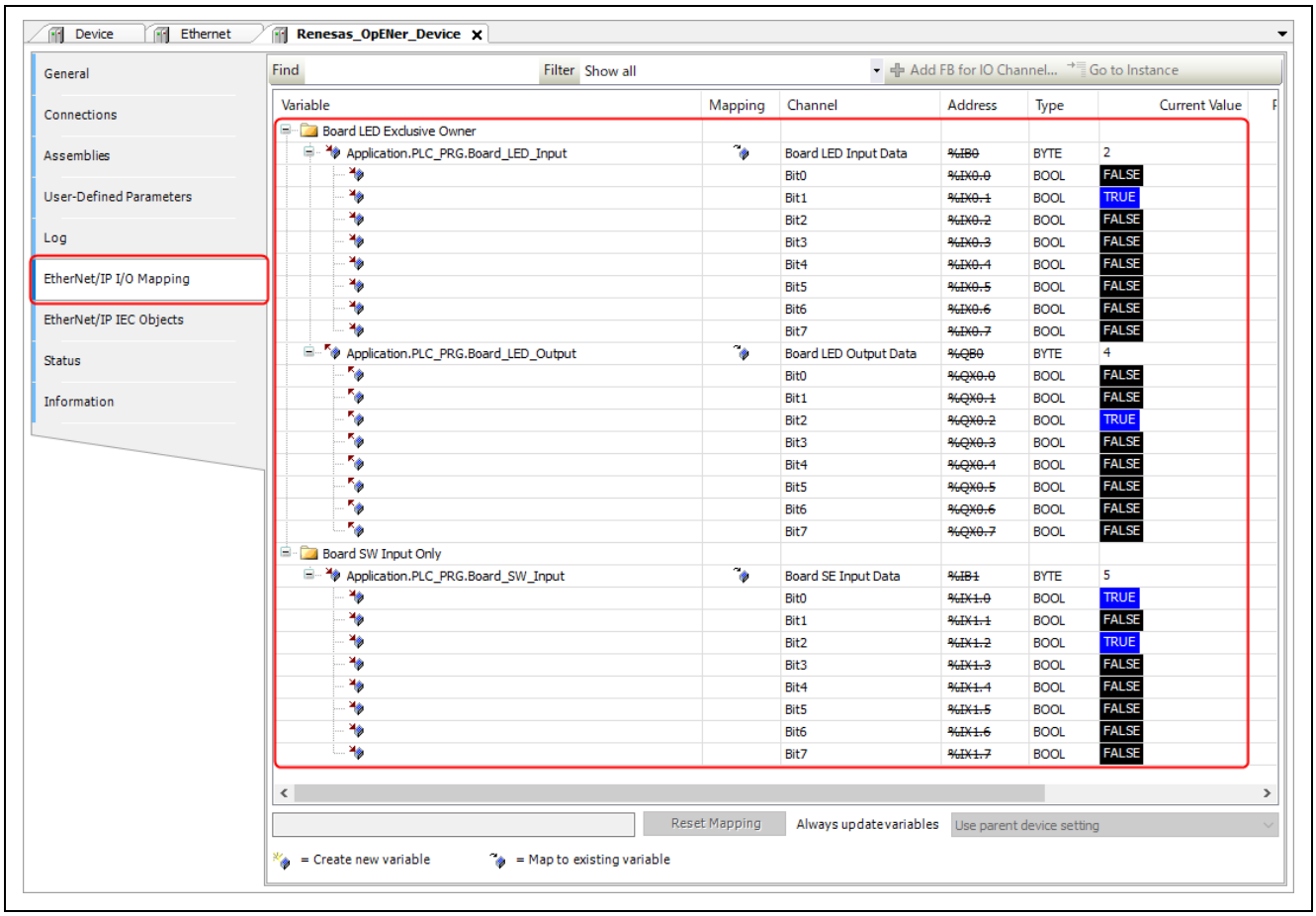


Figure 6-10 Check Application Behavior

7. Appendix

Appendix A: OSS implemented in the sample code

The following three OSS are used in the sample code.

OpENer

The "OpENer" is an open-source software for I/O communication adapters of EtherNet/IP. Please refer the following link for the detail.

https://github.com/EIPStackGroup/OpENer

- Git comment ID used in this sample software: 05cdd03

This package is the RZ/T2M, RZ/N2L port of OpENer and includes OpENer source codes. Regarding the open-source license of OpENer, please see the following file.

```
common\oss\OpENer\license.txt
```

FreeRTOS

The FreeRTOS is an open-source software for real-time operating system (RTOS) for microcontrollers. Please refer the following link for the details.

https://aws.amazon.com/freertos/

https://github.com/aws/amazon-freertos

- Git comment ID used in this sample software: a038063

The RZ/T2M, RZ/N2L port of OpENer includes FreeRTOS source codes as a RTOS kernel. Regarding the open-source license of OpENer, please see the following file.

```
common\oss\amazon-freertos\LICENSE
```

lwIP

The lwIP is an open-source software for a small independent implementation of the TCP/IP protocol suite. Please refer the following link for the details.

https://savannah.nongnu.org/projects/lwip/

https://github.com/lwip-tcpip/lwip

- Git comment ID used in this sample software: 79cd89f

The RZ/T2M, RZ/N2L port of OpENer includes lwIP source codes as a TCP/IP stack. Regarding the open-source license of lwIP, please see the following file.

```
common\oss\lwip\COPYING
```

Appendix B: Assembly Objects and I/O Connections

This sample application has the 7 instances of Assembly object. 5 of these instances are bound to the following array variables.

Table 7-1 Assembly Objects and I/O Connections

Instance No.	Type	Description	Bound variables
100 (0x64)	Static Input	Input of Exclusive Owner I/O Connection bound to LED	`g_assembly_data_led_input[1]`
101 (0x65)	Static Input	Input of Input Only I/O Connection bound to SW3	`g_assembly_data_sw_input[1]`
150 (0x96)	Static Output	Input of Exclusive Owner I/O Connection bound to LED	`g_assembly_data_led_output[1]`
151 (0x97)	Static Configuration	Configuration of I/O Connections	`g_assembly_data_config[4]`
154 (0x9A)	Static I/O	Accessing by explicit message connection only	`g_assembly_data_explicit[4]`
238 (0xEE)	Static Output	Heartbeat output of Input only I/O Connection bound to SW3	-
237 (0xED)	Static Output	Heartbeat output of listen only I/O Connection.	-

Appendix C: Support CIP Object Classes

The CIP object classes on OpENer RZ/T2M, RZ/N2L port are shown below.

Table 7-2 CIP Object Class on OpENer RZ/T2M, RZ/N2L port

Object Class #	Object Class Name
0x01	Identity
0x02	Massage Router
0x04	Assembly
0x06	Connection Manager
0x47	Device Level Ring
0xF5	TCP/IP Interface
0xF6	Ethernet Link
0x48	QoS

Table 7-3 0x01: Identity

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
2	Max Instance	○	-
3	Number of Instance	○	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	○	-
7	Max Number Instance Attributes	○	-
Class Services			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
1	Vendor ID	○	-
2	Device Type	○	-
3	Product Code	○	-
4	Revision	○	-
5	Status	○	-
6	Serial Number	○	-
7	Product Name	○	-
Instance Service			
#	**Service Name**		
0x01	Get_Attributes_All		
0x05	Reset		
0x0E	Get_Attribute_Single		

*: The values of instance attributes #1~#4, #6, and #7 are configured by macros in “deveicedata.h" in “common\renesas\oss_deps\opener” directory.

Table 7-4 0x02: Massage Router

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
2	Max Instance	○	-
3	Number of Instance	○	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	○	-
7	Max Number Instance Attributes	○	-
Class Services			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
No instance attributes are implemented.			
Instance Service			
#	**Service Name**		
0x0E	Get_Attribute_Single		

Table 7-5 0x04: Assembly

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
2	Max Instance	○	-
3	Number of Instance	○	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	○	-
7	Max Number Instance Attributes	○	-
Class Services			
#	**Service Name**		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
3	Data	○	○
4	Size	○	-
Instance Service			
#	**Service Name**		
0x0E	Get_Attribute_Single		
0x10	Set_Attribute_Single		

Table 7-6 0x06: Connection Manager

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
2	Max Instance	○	-
3	Number of Instance	○	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	○	-
7	Max Number Instance Attributes	○	-
Class Services			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
No instance attributes are implemented.			
Instance Service			
#	**Service Name**		
0x0E	Get_Attribute_Single		
0x4E	Forward_Close		
0x54	Forward_Open		
0x5a	Get_Connection_Owner		
0x5b	Large_Forward_Open		

Table 7-7 0x47: Device Level Ring

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
Class Services			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
1	Network Topology	○	-
2	Network Status	○	-
10	Active Supervisor Address	○	-
12	Capability Flags	○	-
Instance Service			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		

Table 7-8 0xF5: TCP/IP Interface

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
2	Max Instance	○	-
3	Number of Instance	○	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	○	-
7	Max Number Instance Attributes	○	-
Class Services			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
1	Status	○	-
2	Configuration Capacity	○	-
3	Configuration Control	○	○
4	Physical Link Object	○	-
5	Interface Configuration	○	-
6	Host name	○	-
8	TTL Value	○	-
9	Mcast Config	○	-
13	Encapsulation Inactivity Timeout	○	○
Instance Service			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
0x10	Set_Attribute_Single		

Table 7-9 0xF6: Ethernet Link

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
2	Max Instance	○	-
3	Number of Instance	○	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	○	-
7	Max Number Instance Attributes	○	-
Class Services			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
1	Interface Speed	○	-
2	Interface Flag	○	-
3	Physical Address	○	-
7	Interface Type	○	-
11	Interface Capability	○	-
Instance Service			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		

Table 7-10 0x48: QoS

Class Attributes			
#	**Attribute Name**	**Get**	**Set**
1	Revision	○	-
2	Max Instance	○	-
3	Number of Instance	○	-
4	Optional Attribute List	-	-
5	Optional Service List	-	-
6	Max Number Class Attributes	○	-
7	Max Number Instance Attributes	○	-
Class Services			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		
Instance Attributes*			
#	**Attribute Name**	**Get**	**Set**
1	802.1Q Tag Enable	○	-
2	DSCP PTP Event	○	-
3	DSCP PTP General	○	-
4	DSCP Urgent	○	○
5	DSCP Scheduled	○	○
6	DSCP High	○	○
7	DSCP Low	○	○
8	DSCP Explicit	○	○
Instance Service			
#	**Service Name**		
0x01	Get_Attributes_All		
0x0E	Get_Attribute_Single		

Appendix D: DLR Operation Check

This section describes how to check DLR operation.

The sample code implements the function as a DLR node only (not Supervisor or Redundant Gateway). Refer to Table 7-7 for supported Attributes and Services.

Check Procedure

1. Prepare Table 7-11 devices and Table 7-12 software tools.
2. Establish the Figure 7-1 topology and power up.
3. Download the program to the RSK board and run it on e^{2}studio or EWARM. (Please refer to Chapter 5)
4. Monitor DLR Instance Attribute values and DLR operation with software tools.

Table 7-11 Used Devices

Product Name	Catalog #:	Vendor	Comment
Allen Bradley Compact Logic 384KB DI/O Controller	1769-L16ER-BB1B	Rockwell Automation	Used as a DLR Supervisor
Allen Bradley 3 port Ethernet Tap	1783-ETAP	Rockwell Automation	Used as a DLR node (Sub-supervisor)

Table 7-12 Used Software Tools

Software Name	Released by
EIP Tools	Molex
RSLinx	Rockwell Automation
DLR Tool	Rockwell Automation

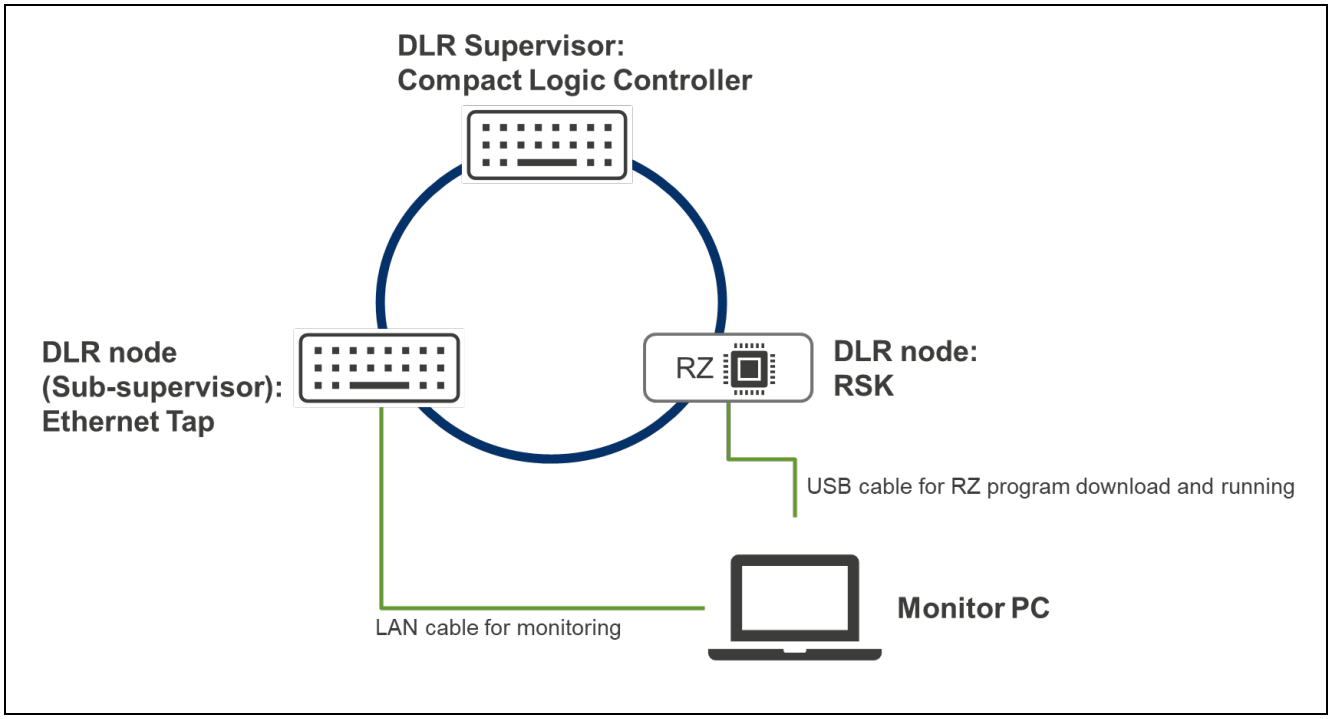


Figure 7-1 Topology for check

Check DLR Instance Attribute values by EIP Tools

The Instance Attribute value can be checked using the EIP Tools. The procedure is described below.

Open EIP Tools and enter the IP address of the target device. The default setting for the IP address written in the sample code is 192.168.1.170.

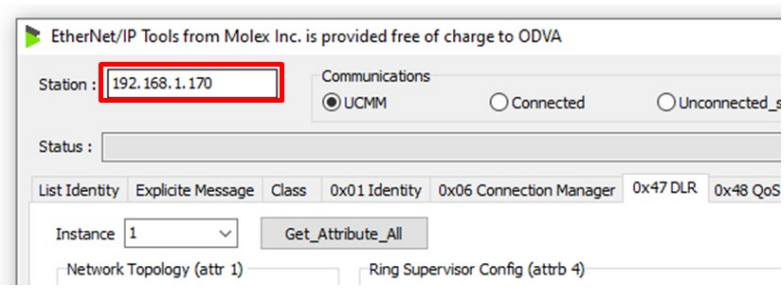
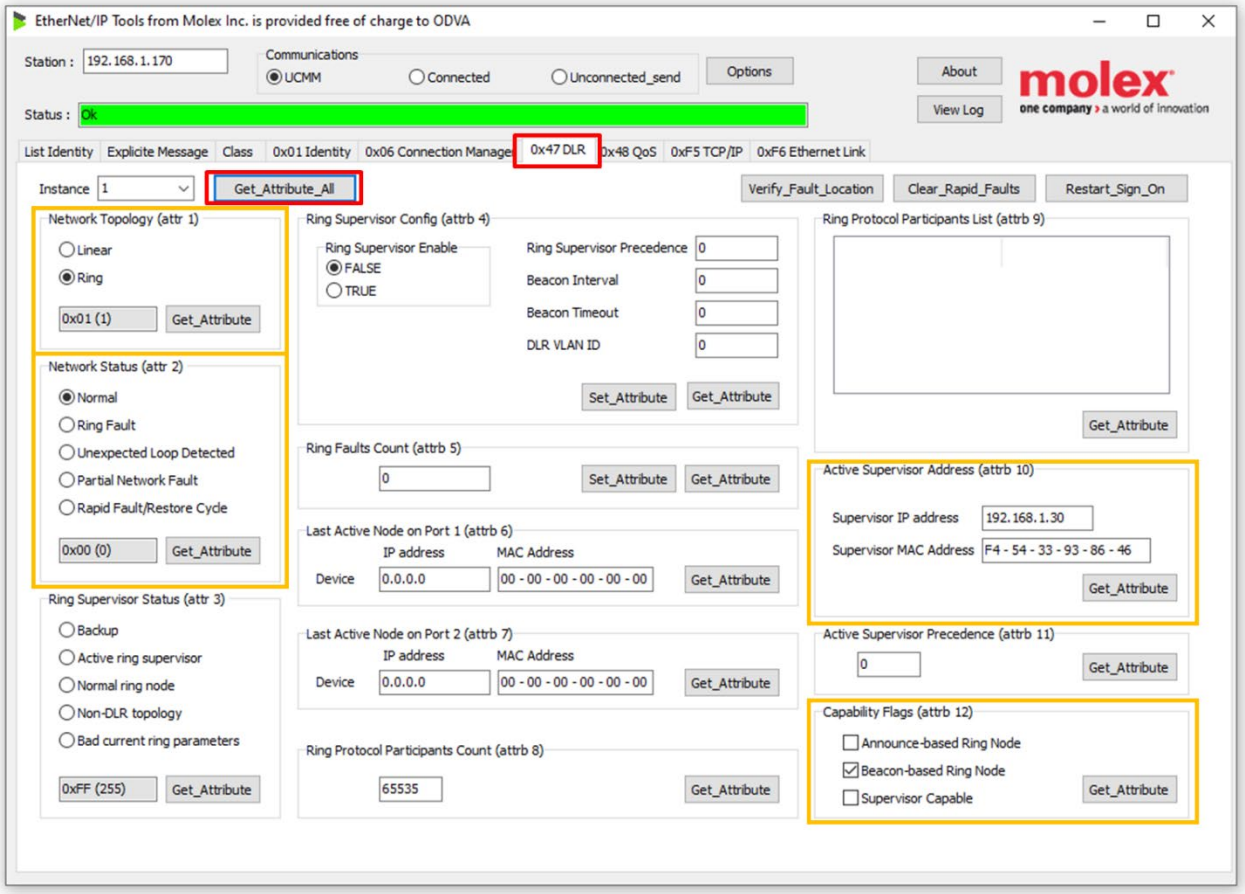


Figure 7-2 Enter the IP address of the target device in EIP Tools

Select the 0x47 DLR tab and click Get_Attributes_All or Get_Attribute_Single. You can see the value of each.



Note: The sample code supports Instance Attribute #1, 2, 10, and 12. (The yellow circled area)

Figure 7-3 Execute Get_Attributes_All in EIP Tools

Check DLR operation by RSLinx and DLR Tool

DLR operation can be checked with the DLR Tool. RSLinx driver settings are required as a preliminary step.

■RSLinx driver settings

Launch RSLinx. If the RSWho window is not open, click RSWho from the Communication tab.

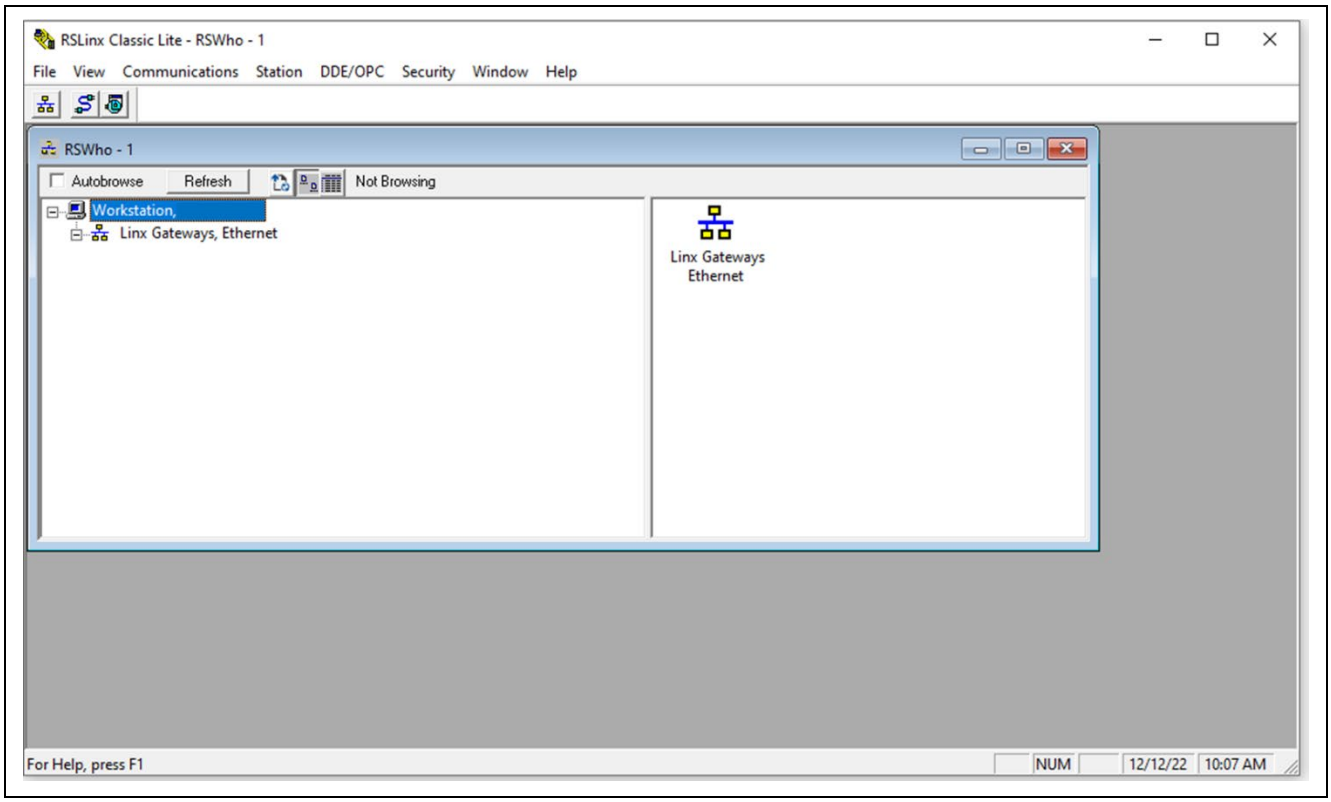


Figure 7-4 Start RSLinx

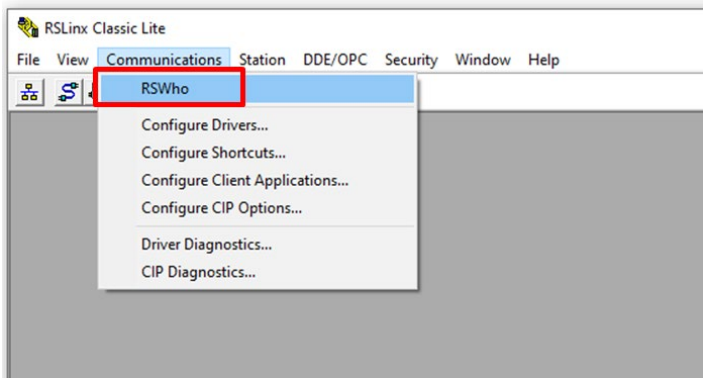


Figure 7-5 Open RSWho window

Create a new driver to monitor the DLR status. Click Configure Driver from the Communication tab.

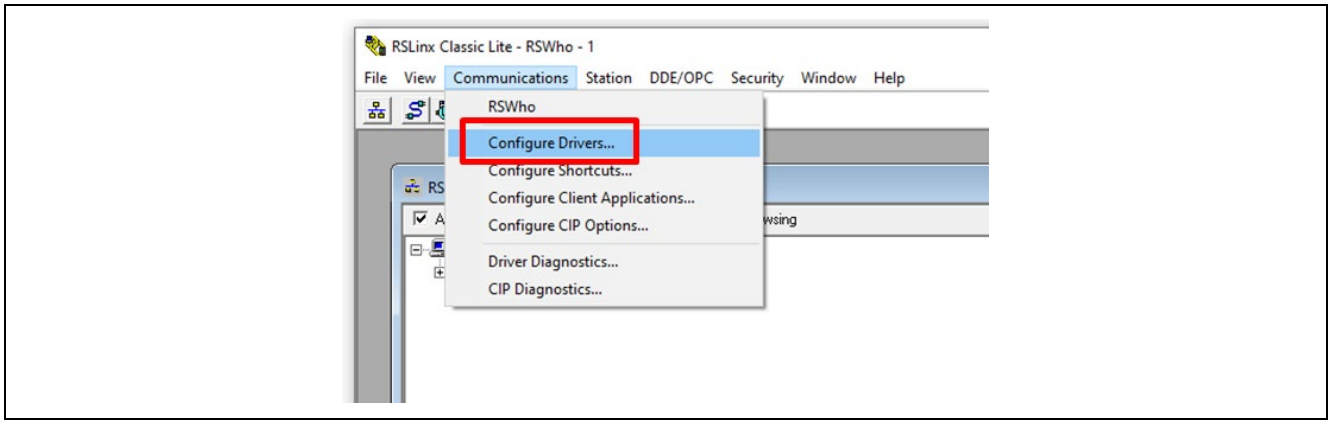


Figure 7-6 Open Configure Drivers window

Select EtherNet/IP Driver from “Available Driver Types” and click “Add New”.

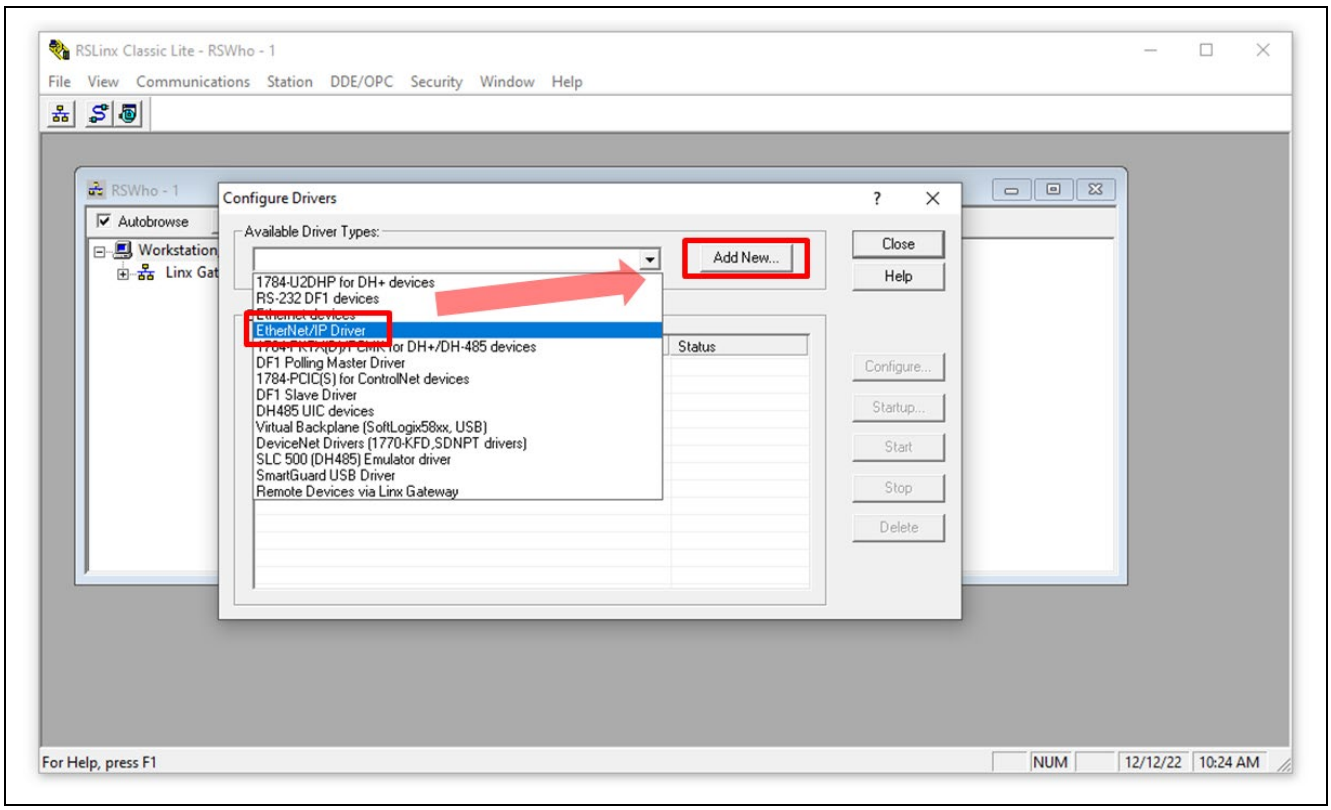


Figure 7-7 Create new EtherNet/IP Driver

Enter any driver name.

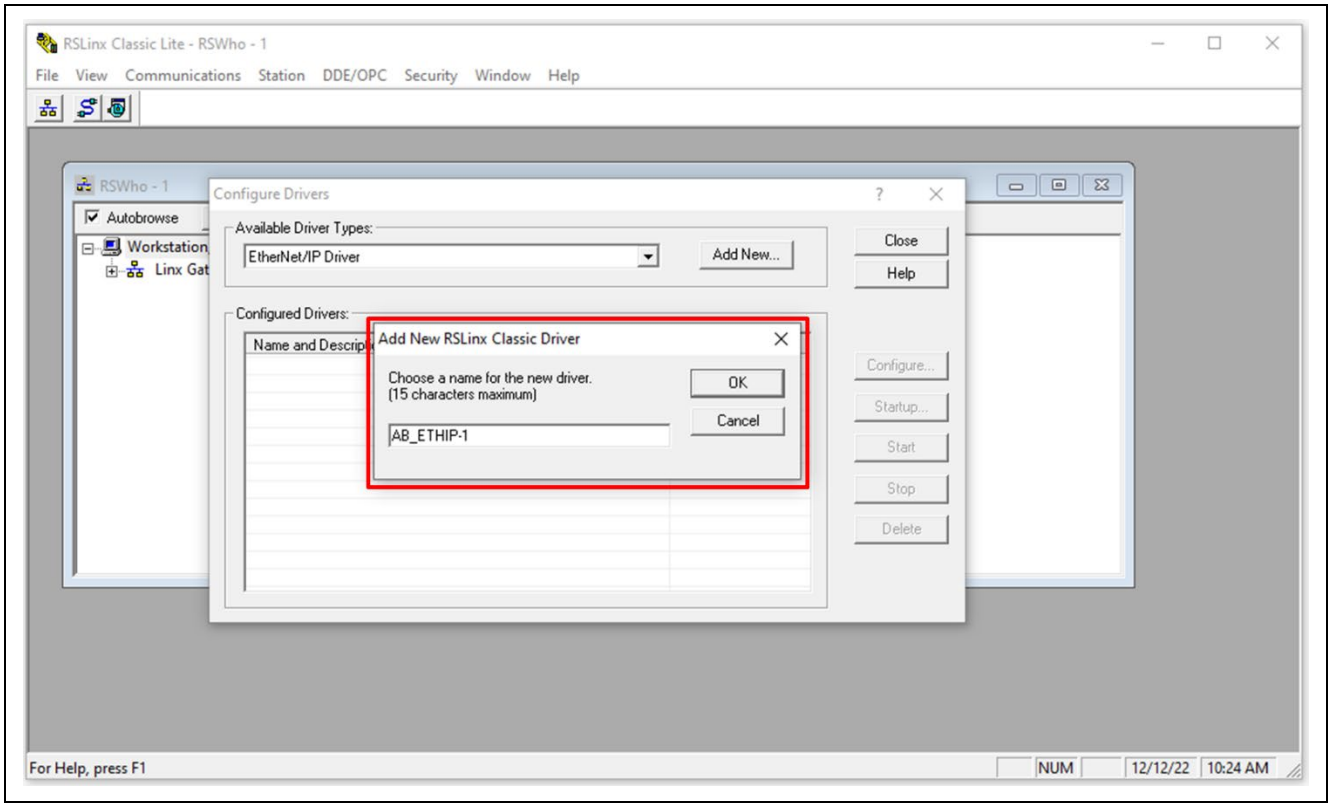


Figure 7-8 Enter new driver name

Select the Ethernet adapter connected to the DLR device, click Apply, and then click OK.

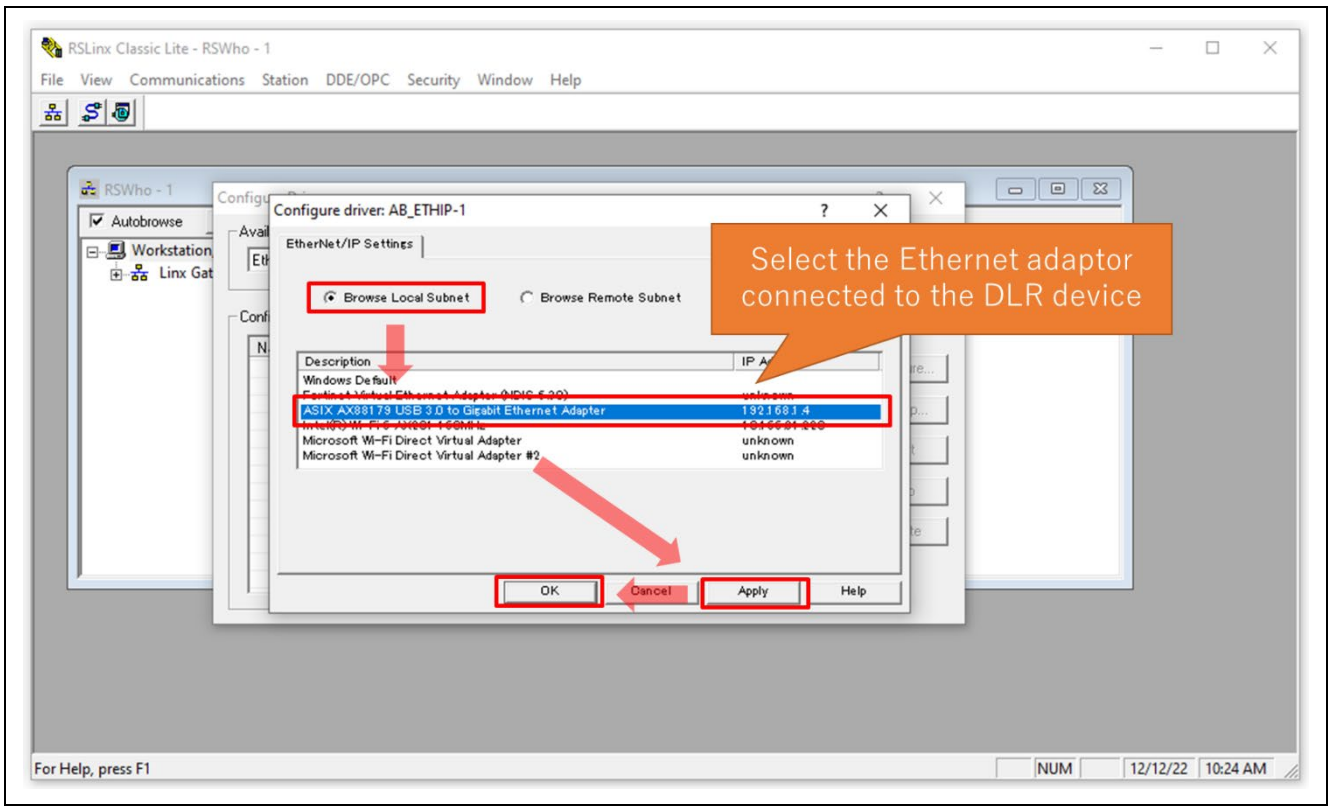


Figure 7-9 Select the Ethernet adaptor connected to the DLR device

Confirm that the driver has been added and Close the Configure Drivers window.

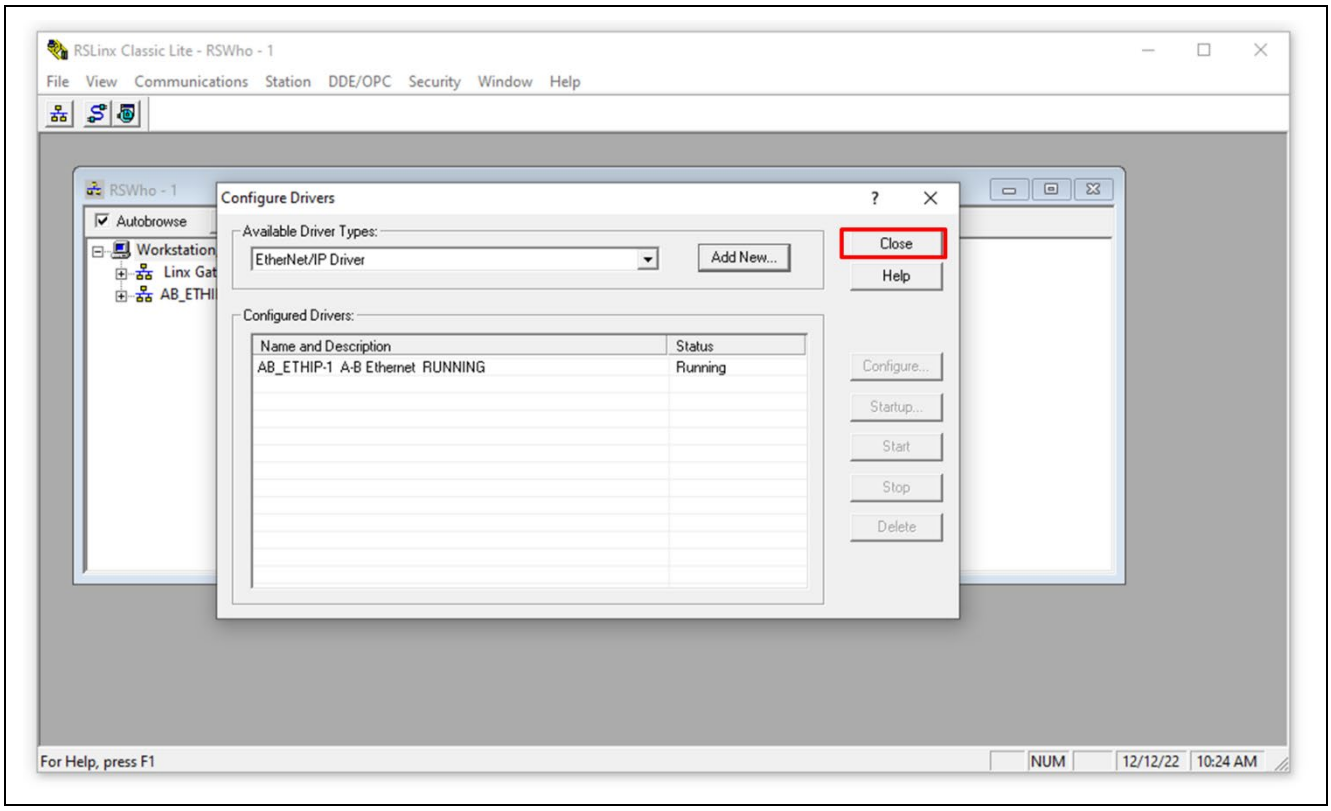


Figure 7-10 Close Configure Drives window

Make sure Autobrowse is enabled and expand the driver you have created. Confirm that the device is recognized as shown in Figure 7-11.

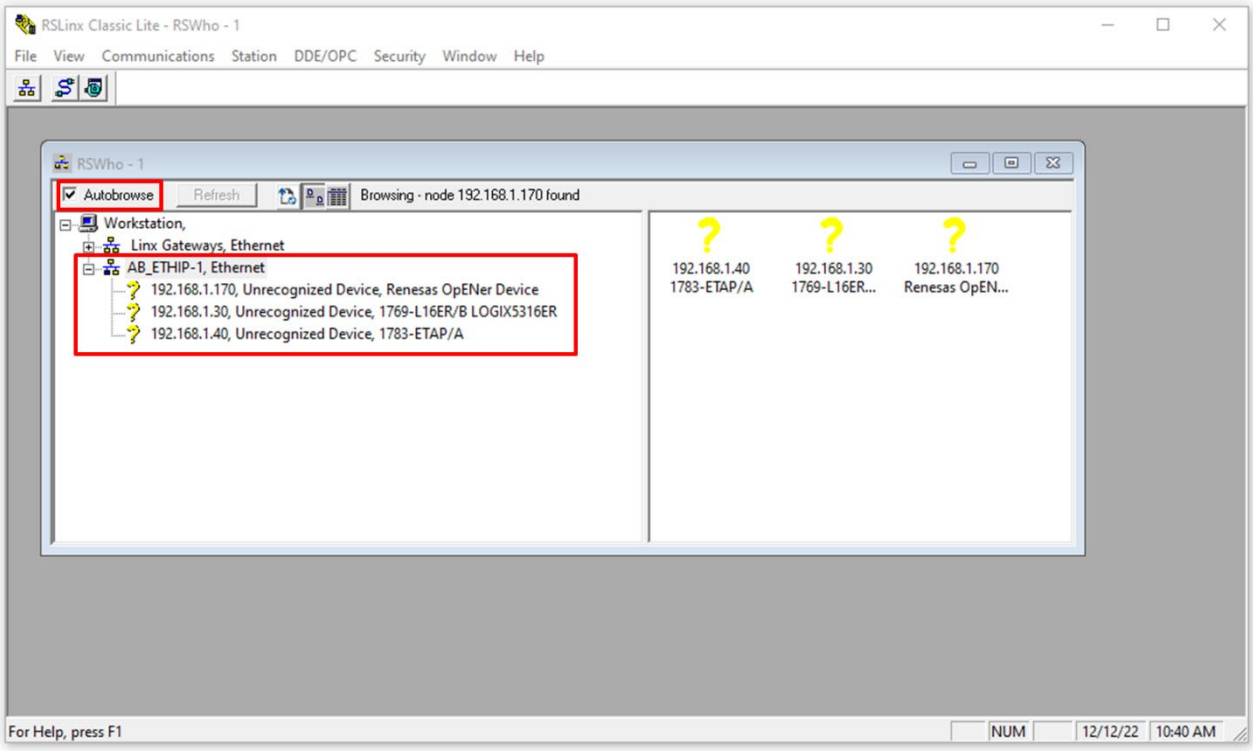


Figure 7-11 Check Autobrowse setting and devices

Note:

Yellow question marks are resolved by registering the EDS files of each device. See "Register EDS files of devices" in RSLinx Classic Help for details.
The EDS file for the sample code is stored in the scanner folder (top level of the sample code zip file directory).

It is now ready to use the DLR Tool.

■Monitor DLR operation with the DLR Tool

Launch the DLR Tool; click the Connect button.

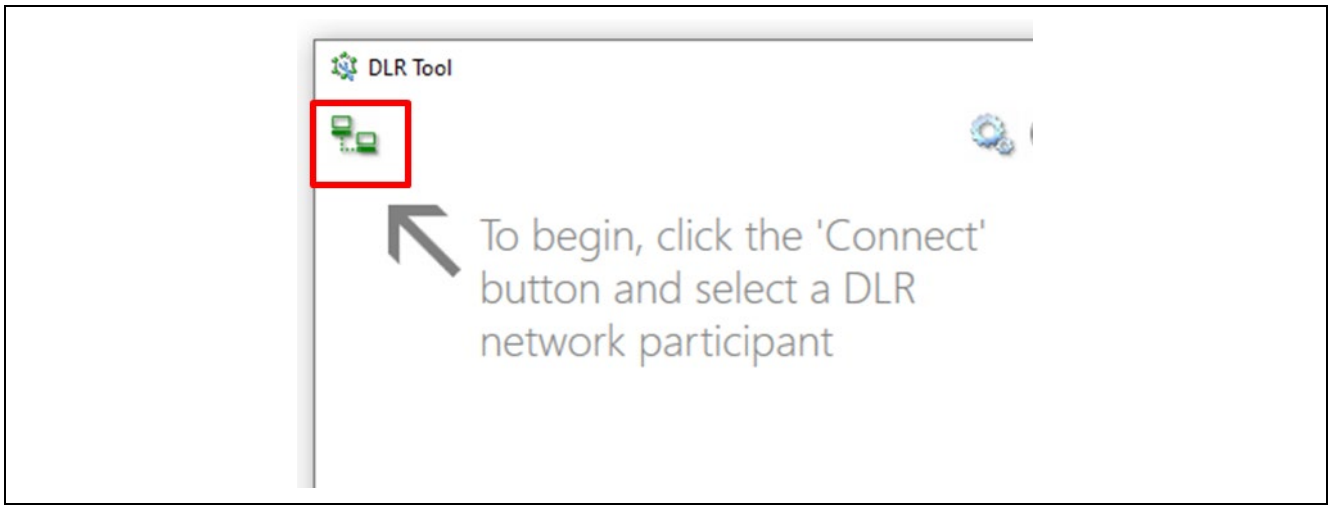


Figure 7-12 Launch DLR Tool and Click Connect button

Expand the added drivers, select one of the devices, and click the Select button.

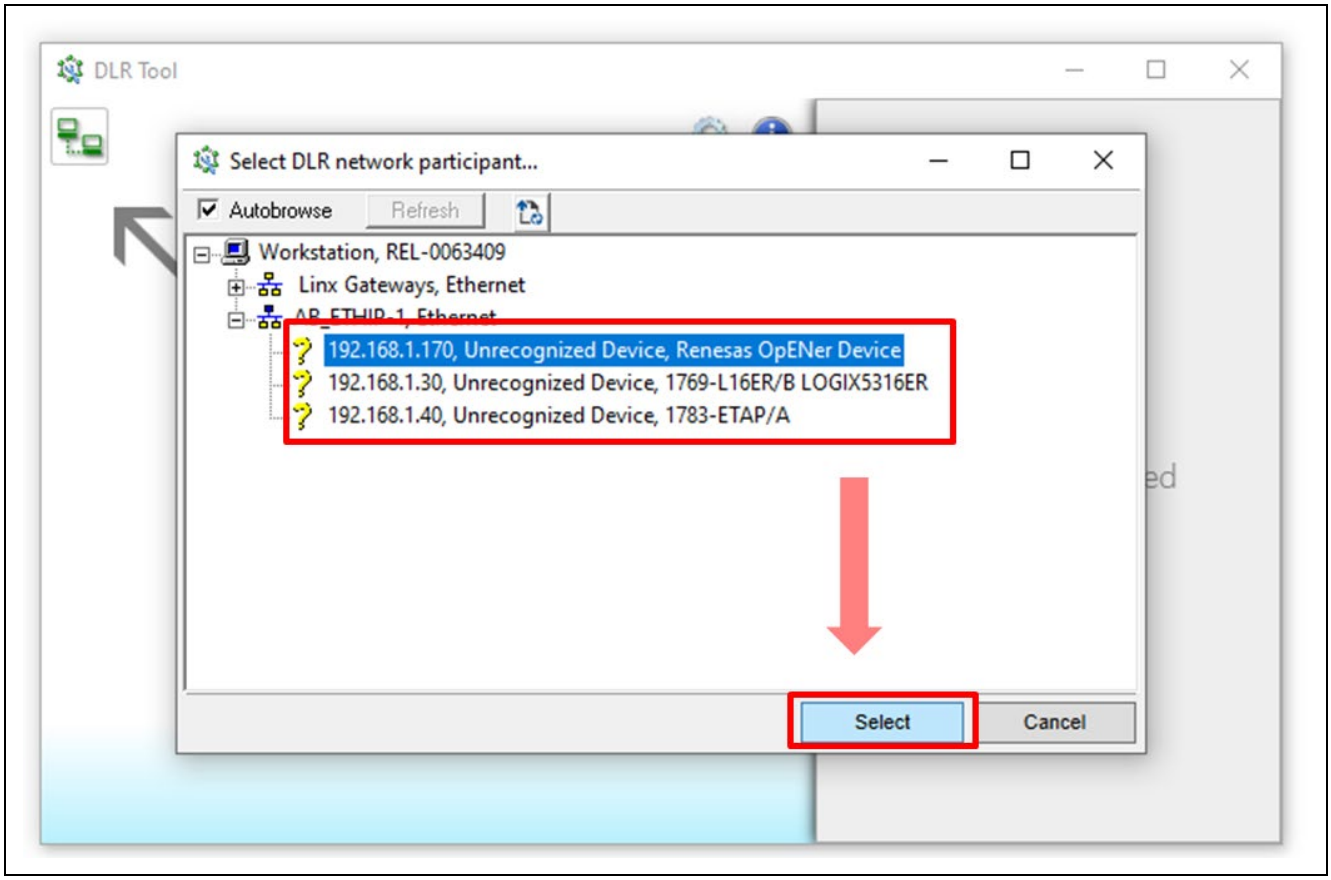


Figure 7-13 Click one of DLR devices and Select button

The status of the DLR operation is graphically displayed and can be monitored.

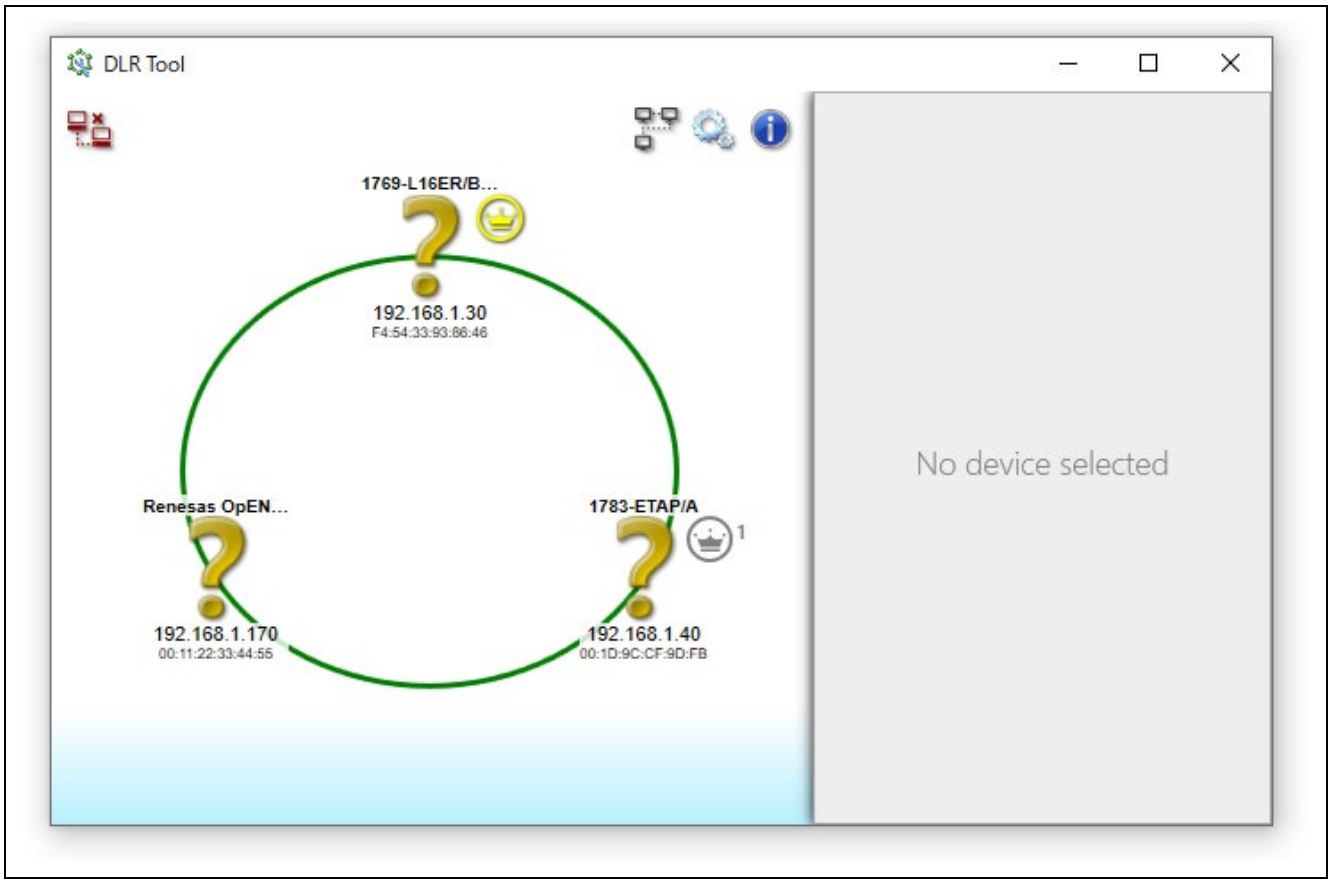


Figure 7-14 DLR operation is graphically displayed on DLR Tool

If any of the topology route is disconnected, the area is highlighted in red. It will be restored when reconnecting.

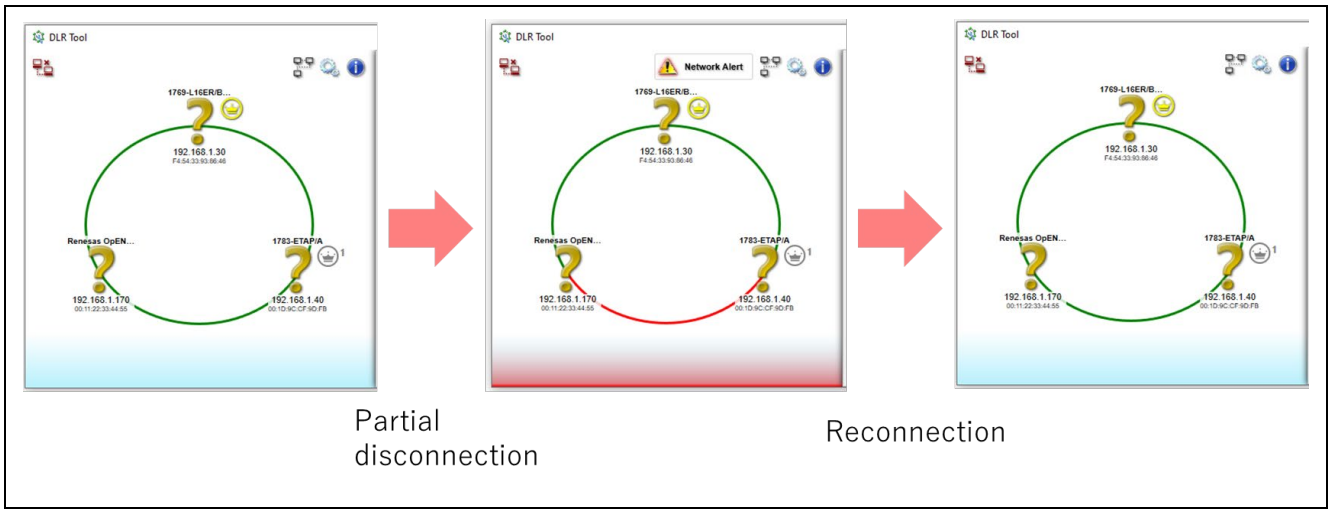


Figure 7-15 Partial disconnection indication and Reconnection

By clicking on a device, information about the device is displayed.

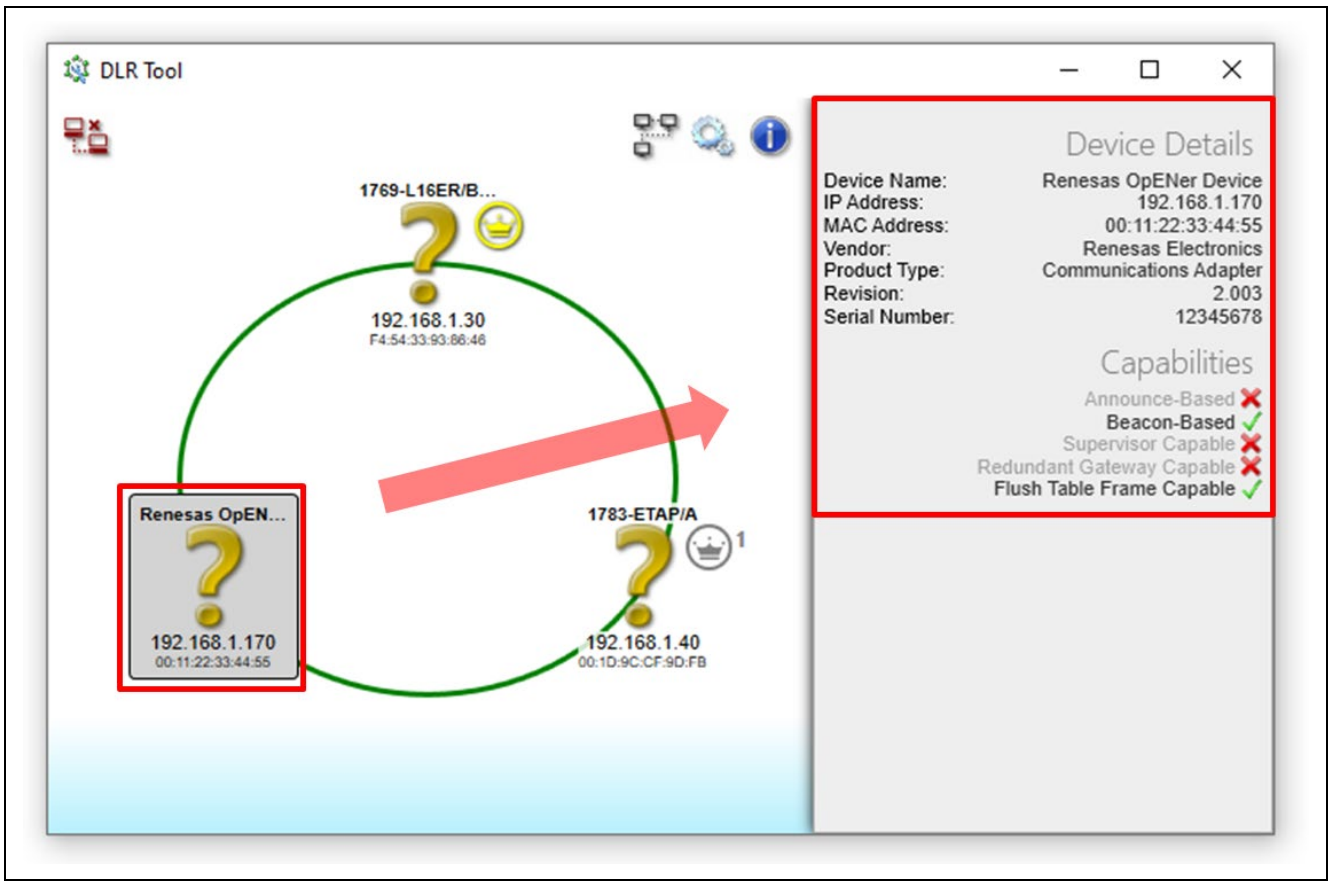


Figure 7-16 Device Details field

Licenses

- OpENer

Regarding the license of OpENer, please see the following file.

```
common\oss\OpENer\license.txt
```

- FreeRTOS

Regarding the license of FreeRTOS, please see the following file.

```
common\oss\amazon-freertos\LICENSE
```

- lwIP

Regarding the license of lwIP, please see the following file.

```
common\oss\lwip\COPYING
```

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2022	-	First issued
1.01	Feb. 10, 2023	All	RZ/T2M supported
		4	Add Limitations and Restrictions
		4	Add 0x47 DLR to Appendix C support CIP Object Class
		50	Create new section Appendix D about DLR.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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