RX Family

Guide for Porting the FIT Project to the Other RX Family

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Introduction

This application note describes porting the FIT project, i.e. the project generated using the FIT module with the smart configurator or the FIT configurator, to the other RX Family.

In this document, the project from which files are ported is called “existing project” and the project to be ported is called “target project”.

Target Devices

Supported devices vary depending on FIT modules.

Supported devices are listed in the Readme.txt file for each FIT module.

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1. Overview

For sample codes or middleware not supported by the FIT, each of them has their independent APIs. In this case, porting between MCUs in different Groups normally requires quite a lot of steps.

However, if they are supported by the FIT, peripheral driver modules or middleware modules can have the common API specifications. Then MCU migration can be done easily.

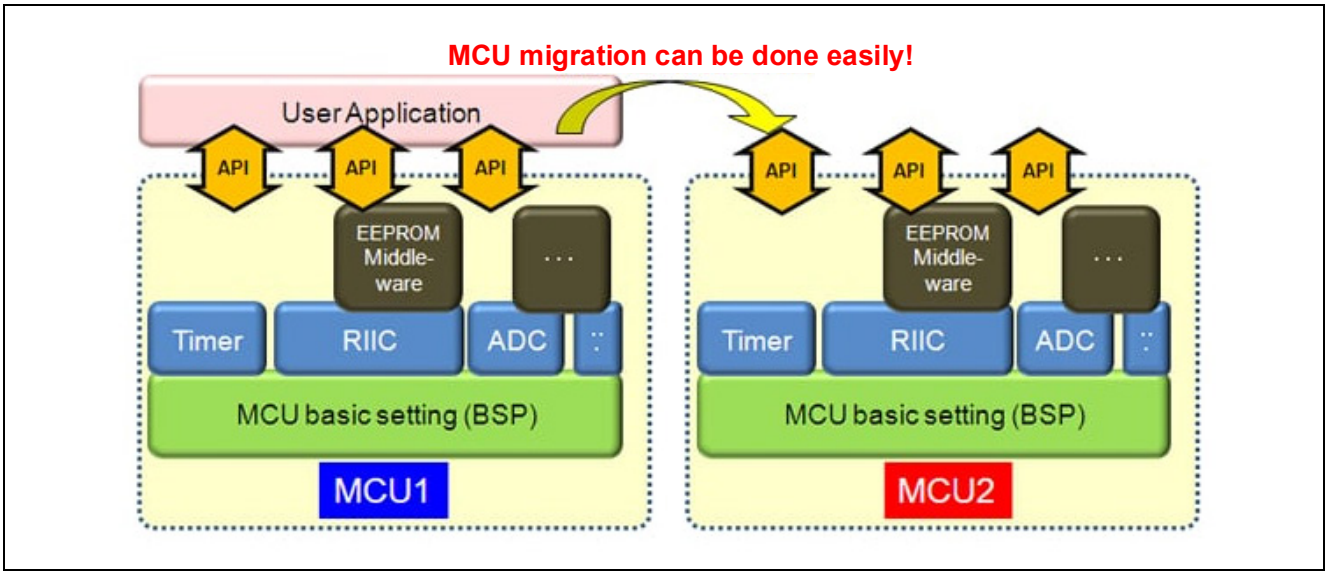


Figure 1.1 Porting Between RX Family MCUs

2. Development Environment of This Application Note

Table 2.1 lists the development environment of this application note.

Table 2.1 Development Environment

Item	Contents
Integrated development environment	Renesas Electronics e^2 studio Version 6.0.0
C compiler	Renesas Electronics C/C++ Compiler Package for RX Family V2.07.00
FIT module	BSP Ver. 3.60 SCI Ver. 1.80 BYTEQ Ver. 1.60

3. Porting

This section describes an example of porting the RX64M FIT project generated by the Smart Configurator to RX65N. If you use the FIT Configurator, translate “Smart Configurator” into “FIT Configurator” in this document. Refer to Adding Firmware Integration Technology Modules to Projects (R01AN1723) for details on the FIT Configurator.

3.1 Before Porting

When using peripheral functions, confirm the following things first. If there are differences in specifications, the procedure introduced in this document may not be used. Please confirm specifications carefully before using this application note.

- Specifications of peripheral modules used by the target MCUs in the existing project and the target project
- Specifications of FIT modules used in the existing project and the target project

3.2 Flowchart of the Porting Procedure

The following shows Flowchart of the Porting Procedure.

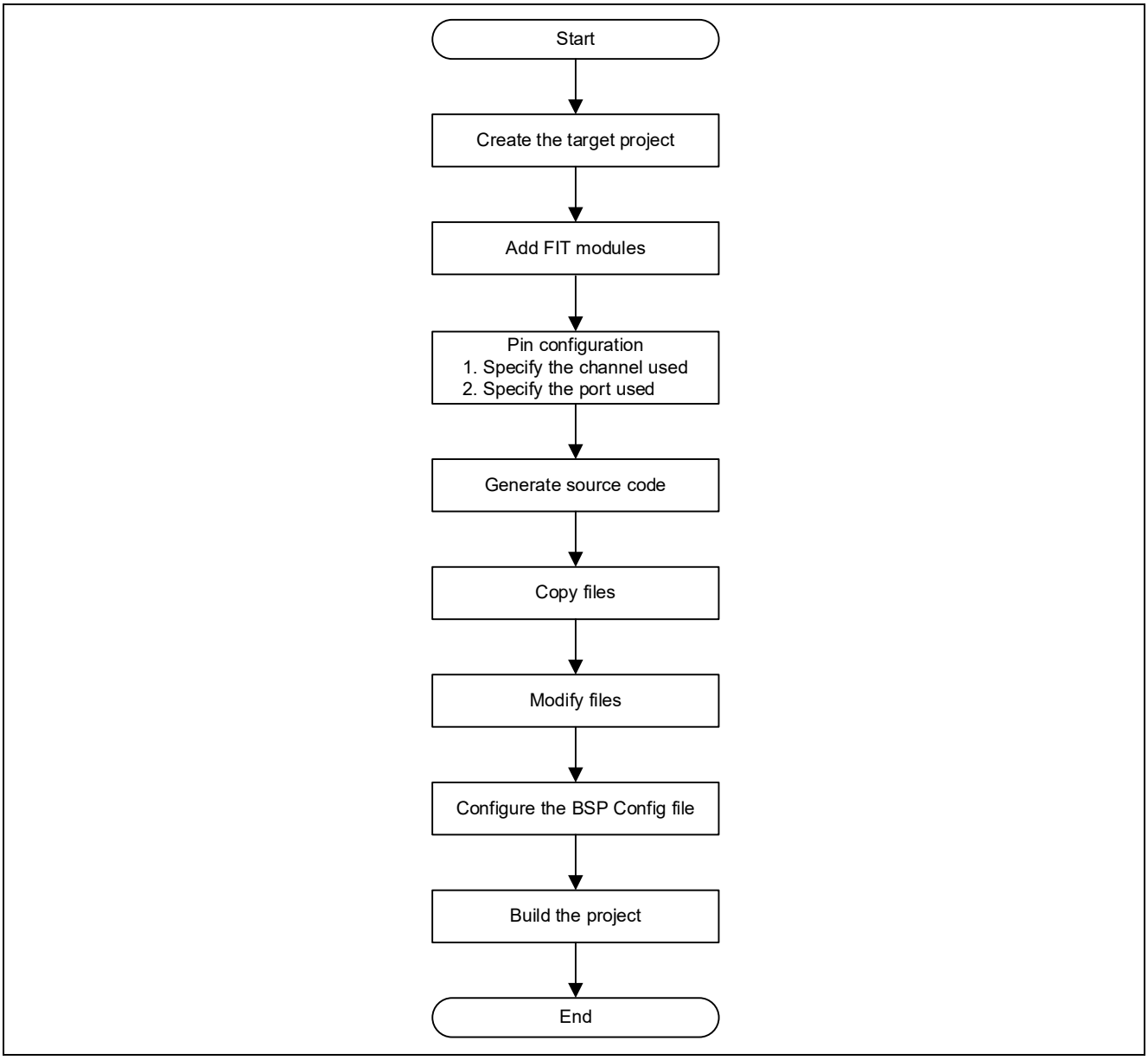


Figure 3.1 Flowchart of the Porting Procedure

3.3 Porting Procedure

3.3.1 Creating the Target Project

Start the e^2 studio and generate the C project using the Smart Configurator. RX65N is used as the target device in this application note.

Refer to 2. Generating a Project in Renesas e^2 studio Smart Configurator User Guide (R20AN0451) for details.

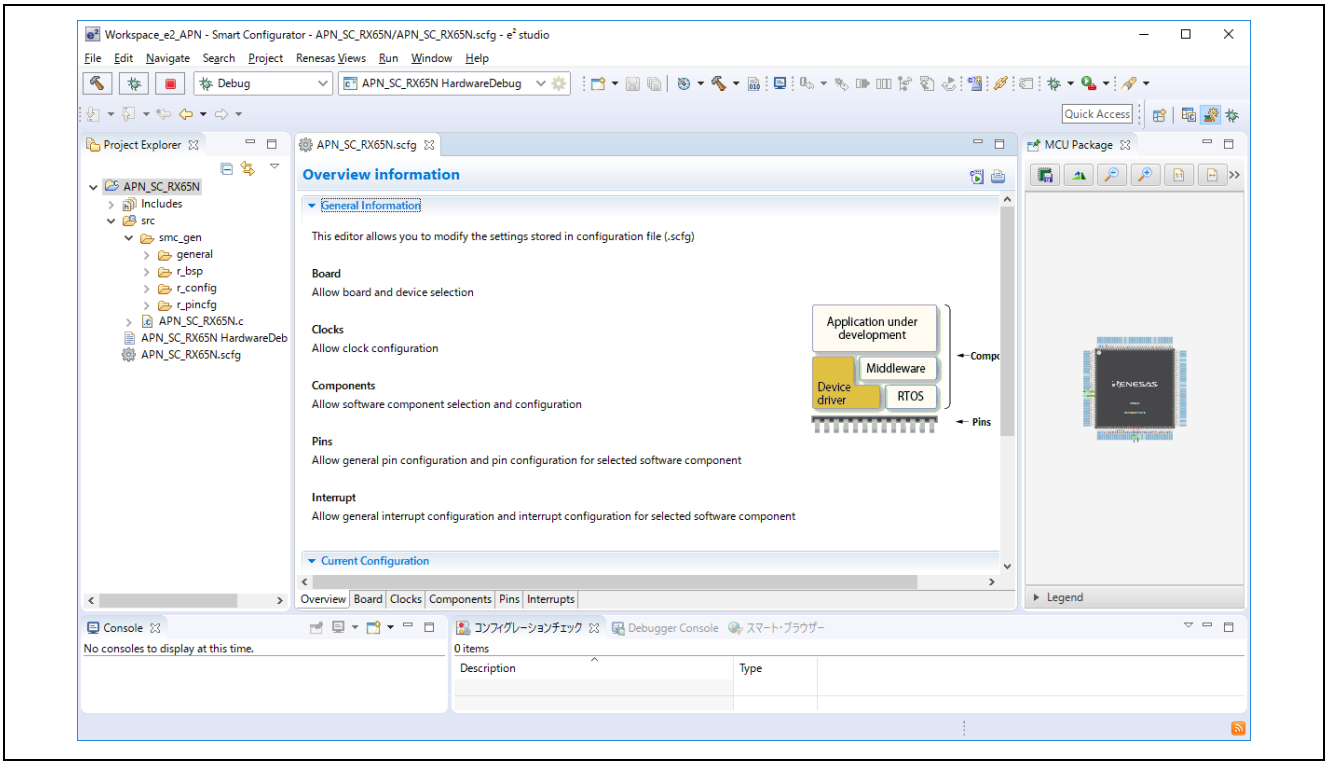


Figure 3.2 Generating the C Project Using the Smart Configurator

3.3.2 Adding the FIT Modules

Add required FIT modules from the Components page of the Smart Configurator Editor. The BSP, SCI, and BYTEQ FIT modules are required in this application note.

The BSP is added as default when using the Smart Configurator. The BYTEQ is added automatically when the SCI is added.

For details, refer to (2) To add a FIT driver or middleware in 3.3.1 Add a software component into the project in Renesas e^2 studio Smart Configurator User Guide (R20AN0451).

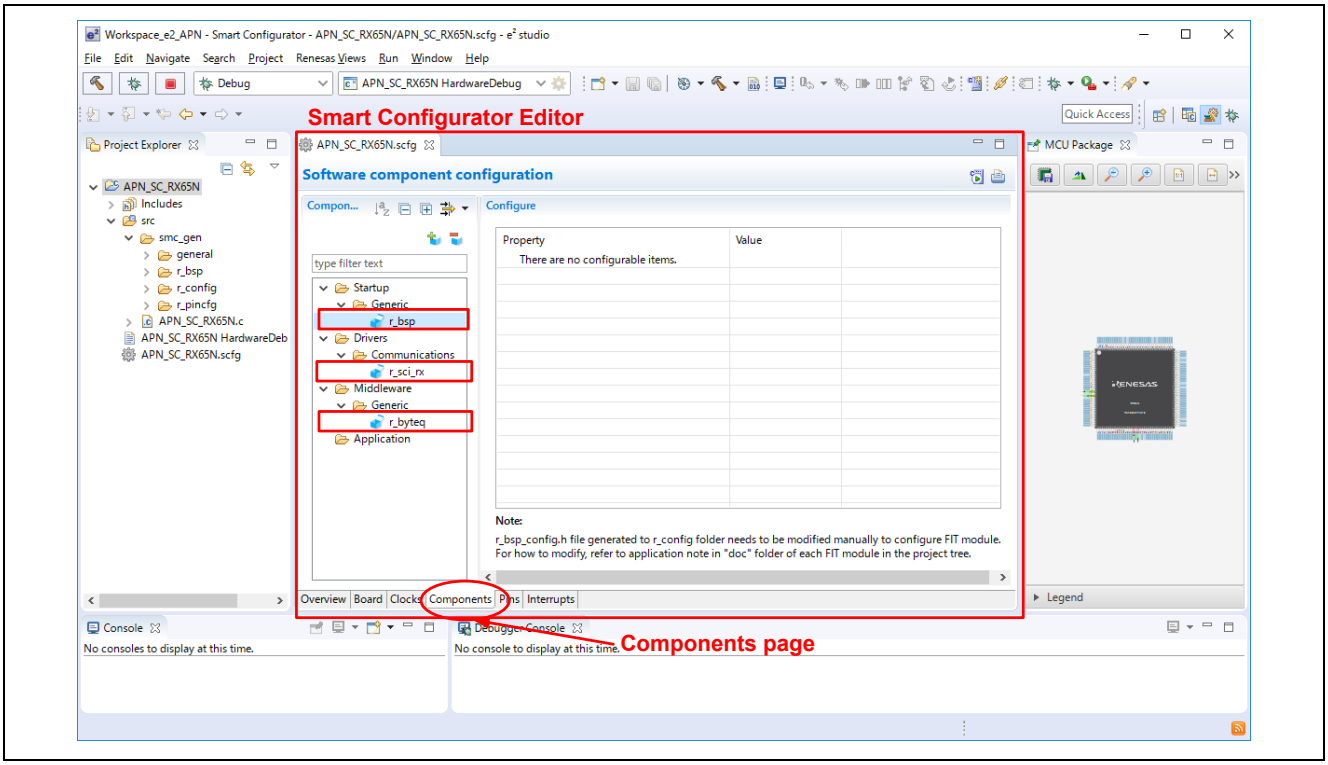


Figure 3.3 Adding the FIT Module

3.3.3 Pin Configuration

1. Specifying the channel

Specify the channel for the FIT module used. Select “r_sci_rx” from the Components page of the Smart Configurator Editor and check to select pins used in the channel.

For details, refer to 3.3.6 Configure a FIT software component in Renesas e^2 studio Smart Configurator User Guide (R20AN0451).

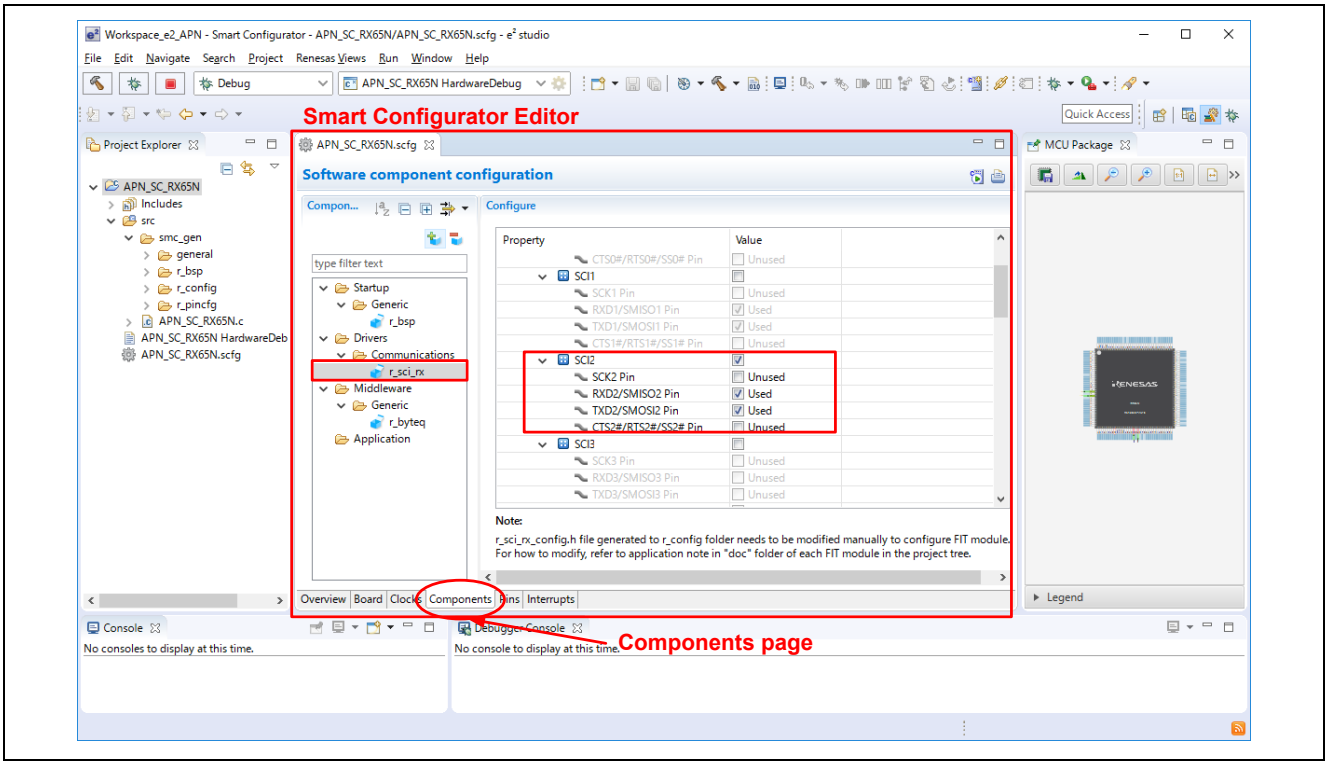


Figure 3.4 Specifying the Channel

2. Specifying the port

Multiple pins may be assigned depending on the function and the channel used. Therefore the port used needs to be specified.

Click in the Pins page of the Smart Configurator Editor and select the FIT module to be modified. When all functions and channels are listed in the Pin Function section, change the pin assignment for the function as necessary.

For details, refer to 3.4.1 Change pin assignment of a software component in Renesas e^2 studio Smart Configurator User Guide (R20AN0451).

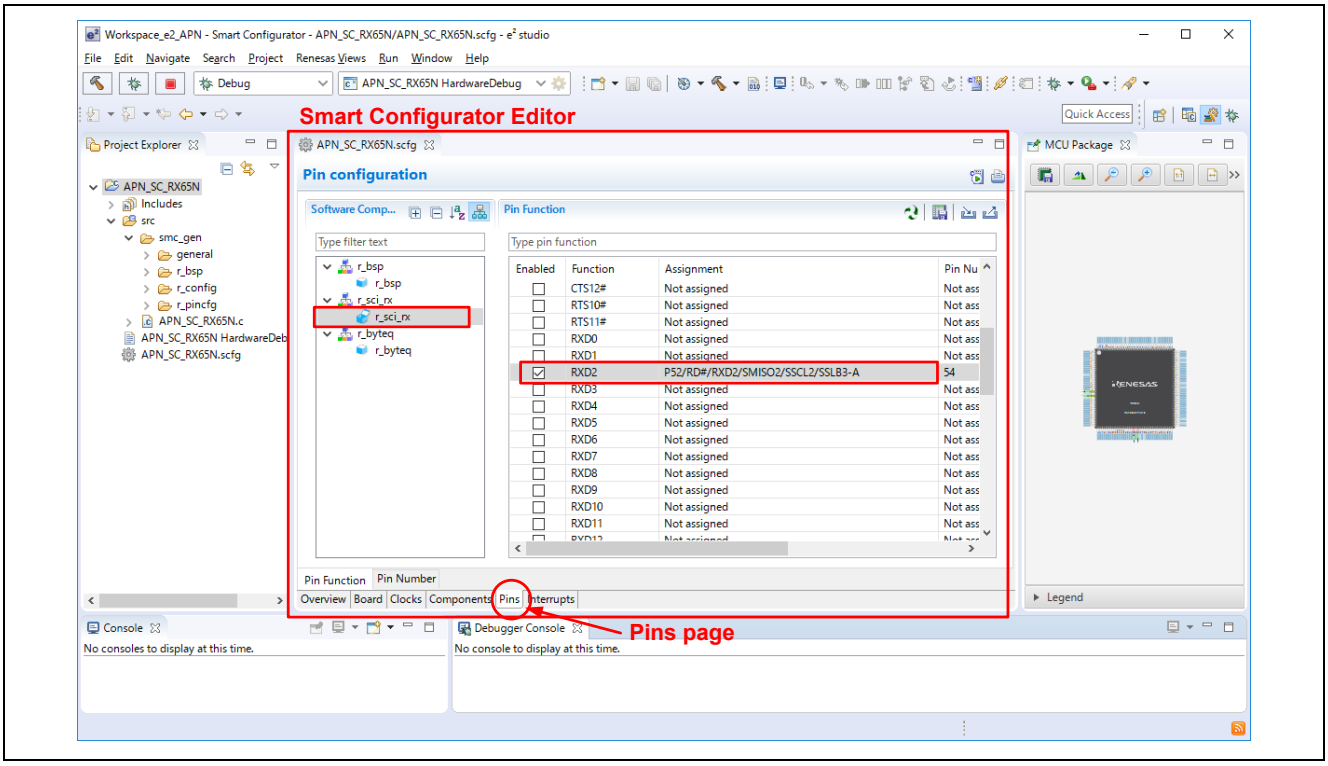


Figure 3.5 Specifying the Port

3.3.4 Generating the Source Code

After the FIT module is added and the pins are configured, generate the code for the FIT module.

Click (Generate Code button) on the Components page of the Smart Configurator Editor to generate the source code. The generated source code appear in the Project Explorer.

For details, refer to 4. Generating source code in Renesas e^2 studio Smart Configurator User Guide (R20AN0451).

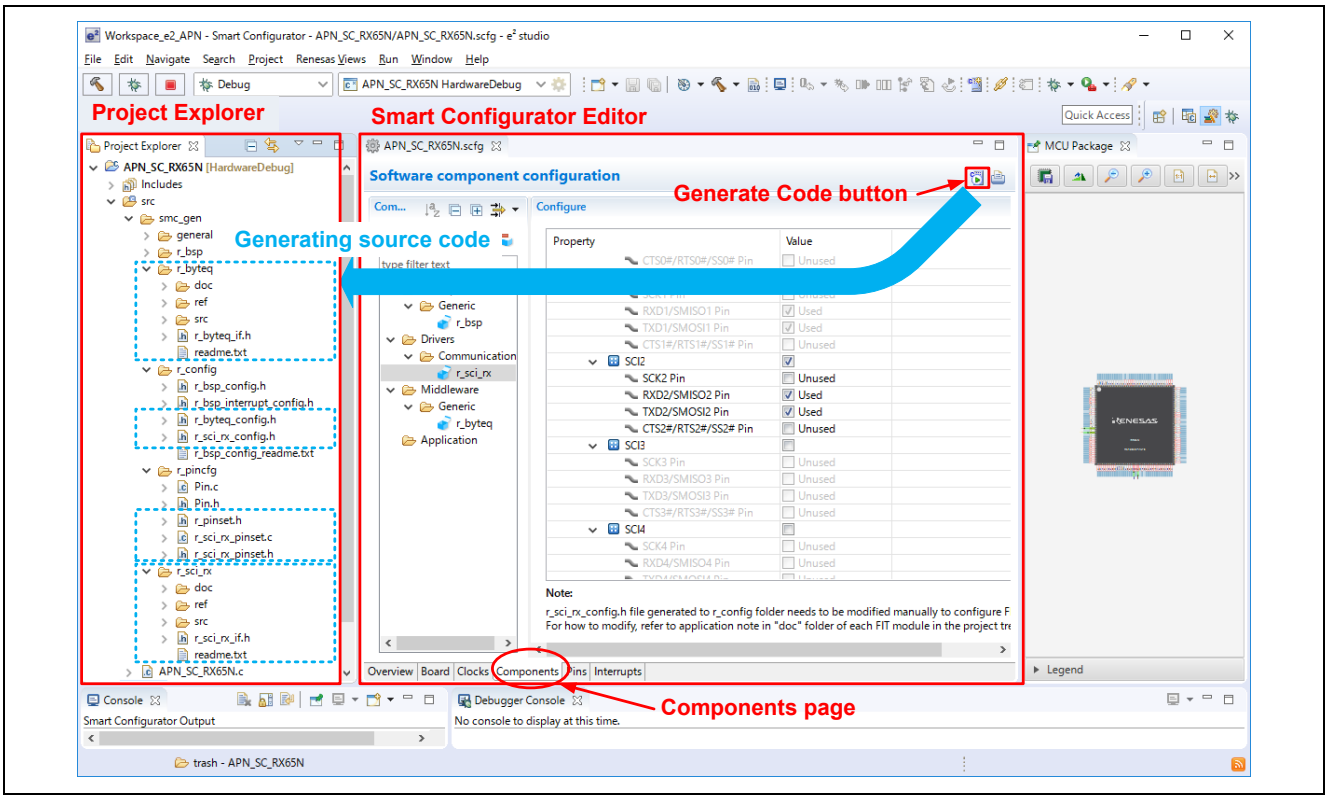


Figure 3.6 Generating the Source Code

3.3.5 Copying Files

Copy the user file and the Config file of each FIT module from the existing FIT project to the target FIT project. The user file here indicates a file which includes the main function or a user developed file.

In this application note, the file which has the main function and the Config files are copied to the target project.

Contents in the Config file may differ depending on the FIT module version. If the contents are different, use the settings of the Config file in the existing project.

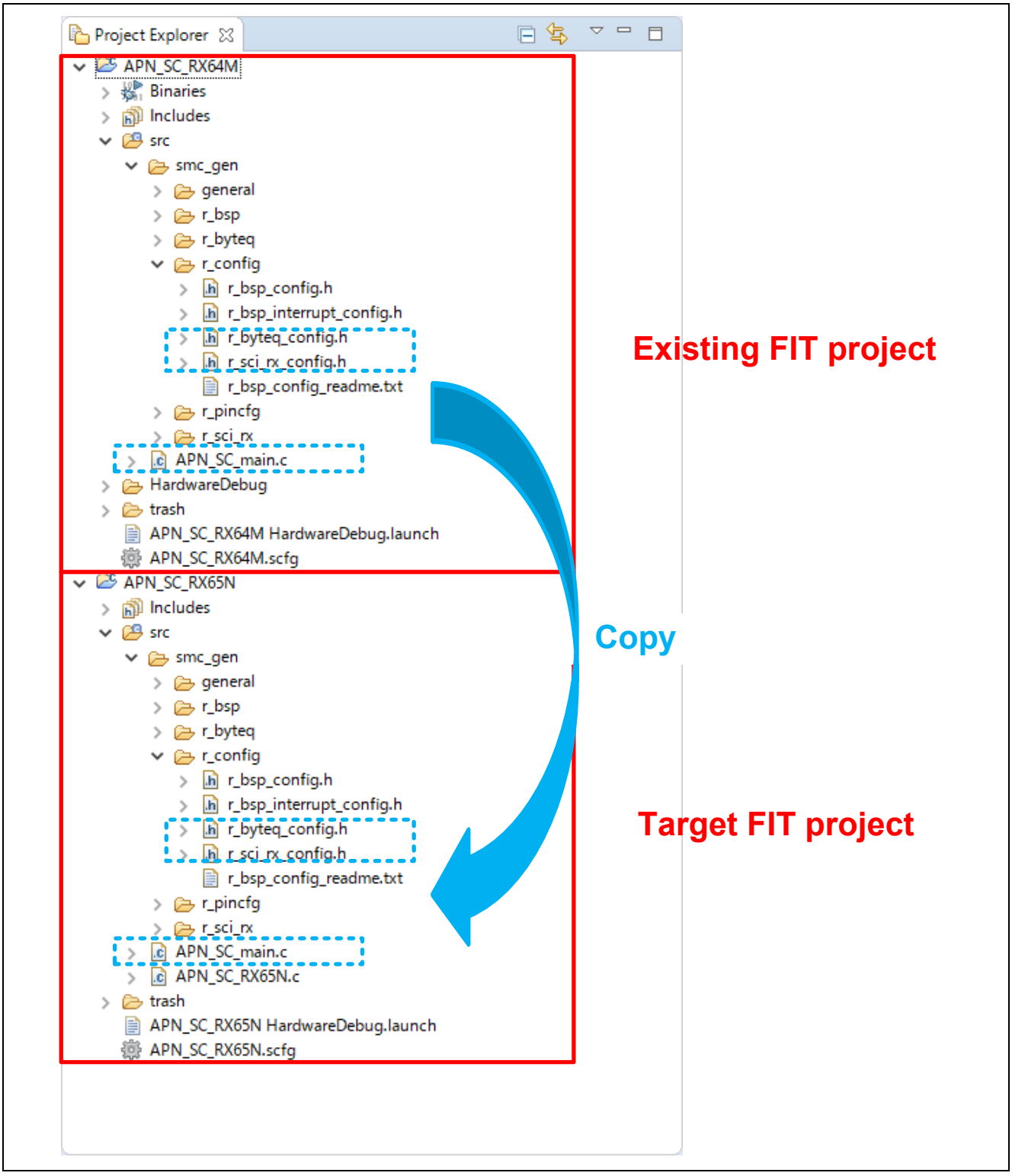


Figure 3.7 Copying the User File

3.3.6 Deleting the File

When a new FIT project is generated, a file which includes the main function is automatically generated. Delete this file since the user file with the main function has been copied from the existing project.

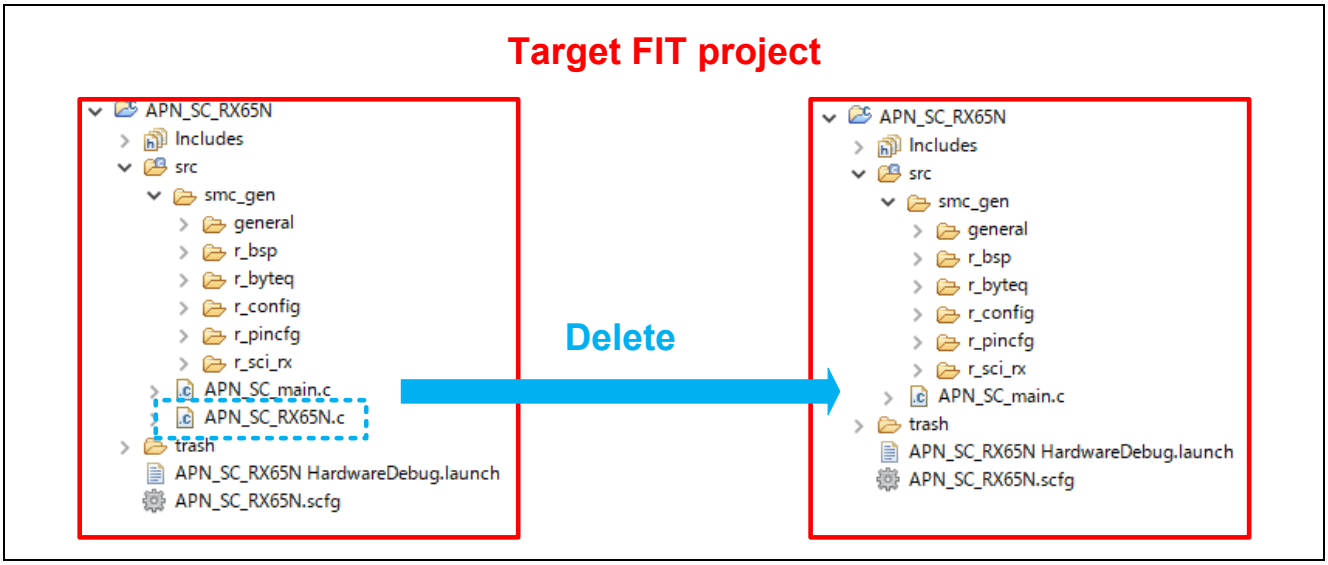


Figure 3.8 Deleting the File

3.3.7 Modifying Files

The user file or other settings may need to be modified due to changes in the target device or depending on the user system. Whether to modify the file or not, or items to be changed is up to the FIT module or the environment used. Please modify an appropriate file when necessary.

The SCI channel is changed in this application note. Accordingly, the user file and the SCI Config file are modified.

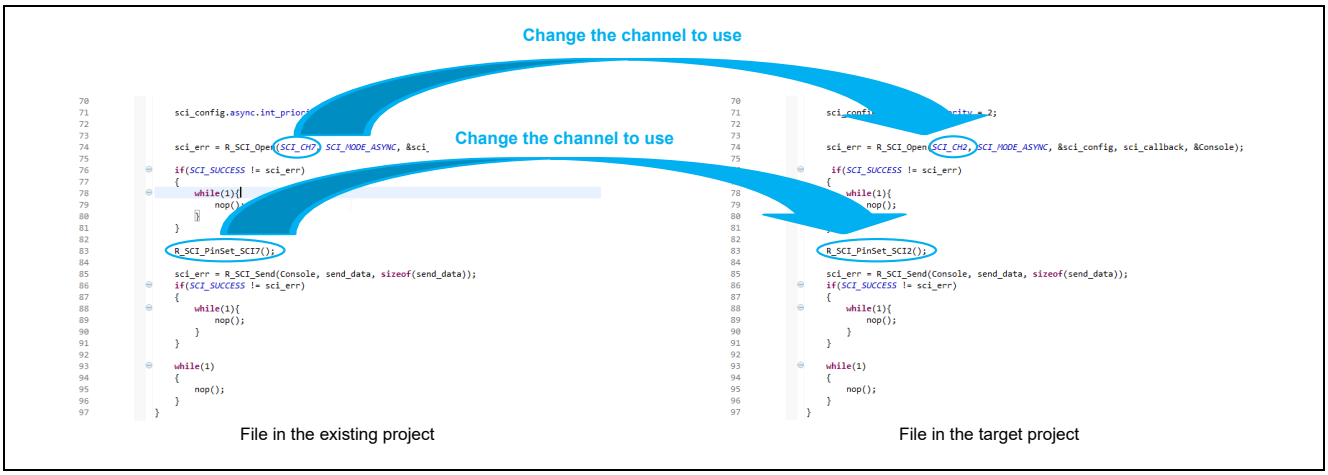


Figure 3.9 Modifying the File (User File)

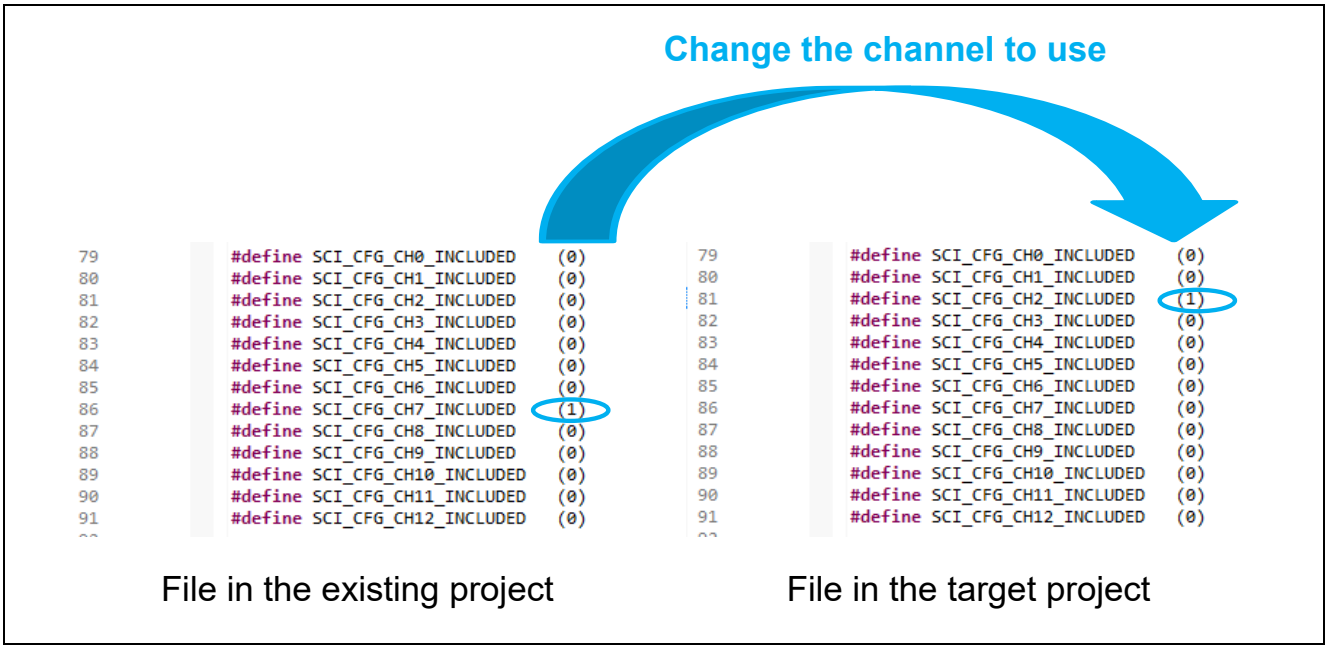


Figure 3.10 Modifying the File (r_sci_rx_config.h)

3.3.8 Configuring the BSP Config File

The system clock setting may need to be changed due to changes in the target device or depending on the user system. When the system clock setting is changed, modify the BSP Config file in the target project.

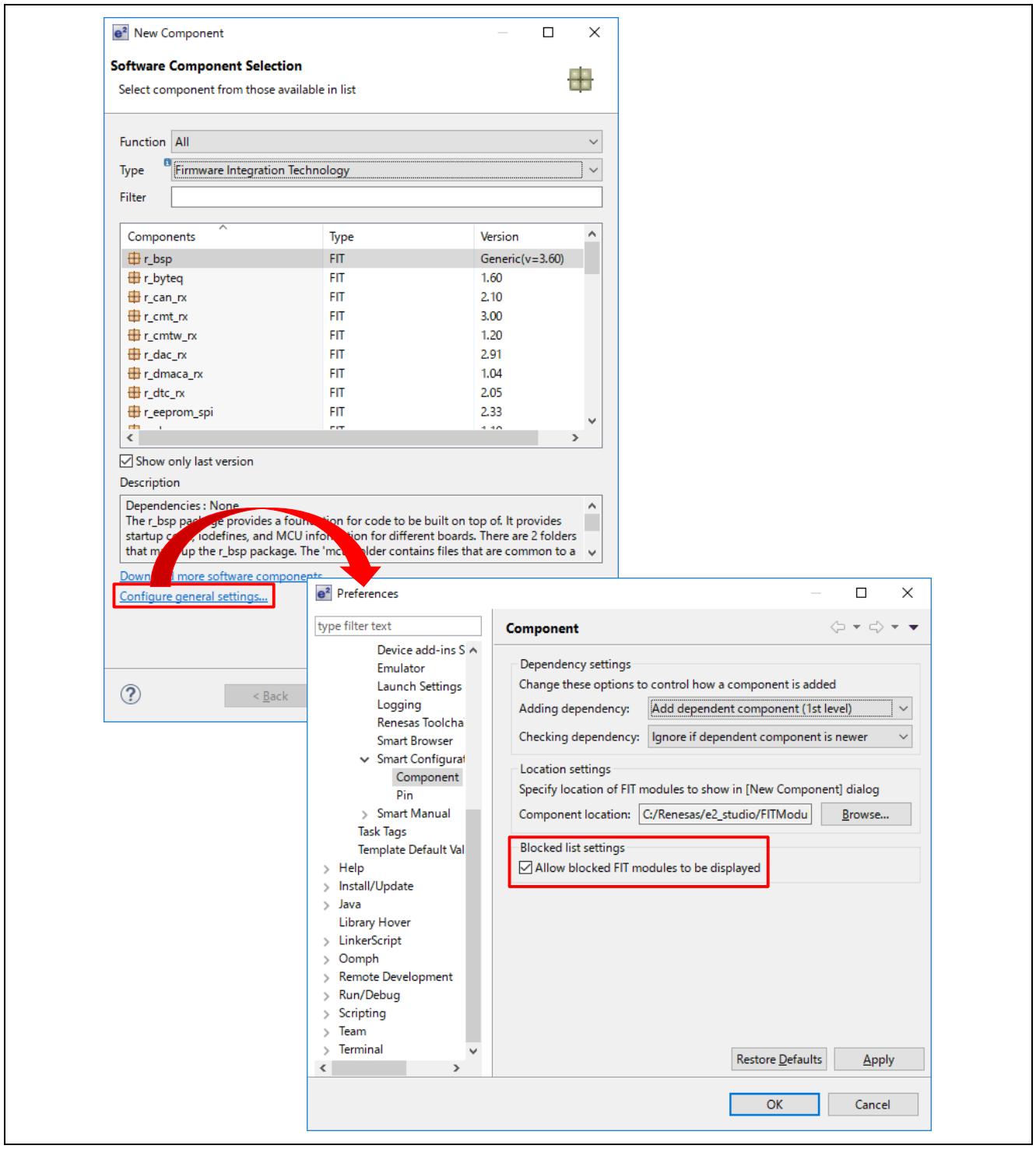
3.3.9 Building the Project

Build the target project.

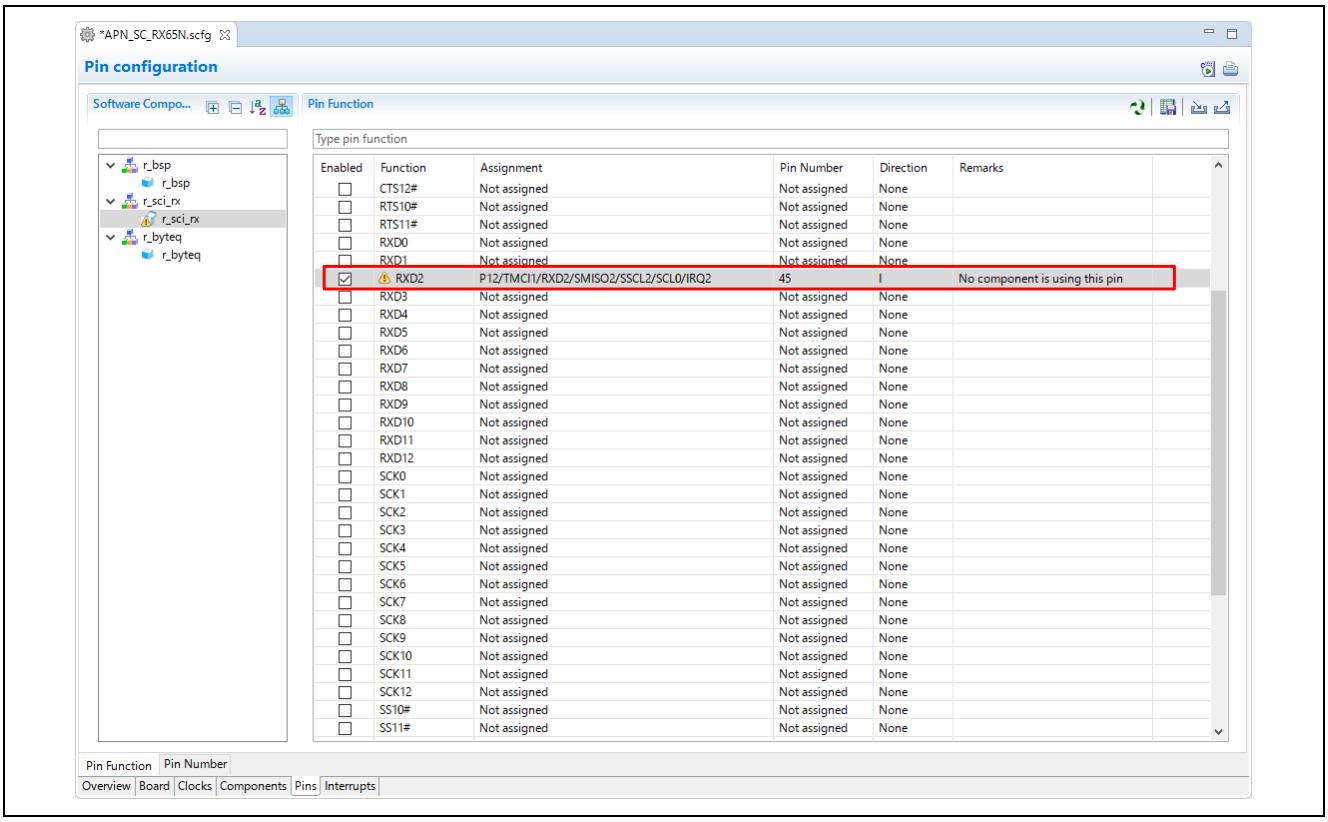
3.4 Troubleshooting

(1) Q: I am trying to add the FIT module to the target project. However, the FIT module I want to add is not displayed.

A: Click “Configure general settings” in the Software Component Selection dialog. When the Component dialog appears, check to select “Allow blocked FIT modules to be displayed” in the Blocked list settings section.



(2) Q: I am trying to perform the pin configuration for the FIT module using the Smart Configurator. When specifying the port to use, the following warning appears.



A: When performing the pin configuration, select the channel and pin to use in the Components page first. Then specify the port to use in the Pins page. Refer to 3.3.3 Pin Configuration for details.

(3) Q: I have followed the application note to copy files from the existing project to the target project and build the project. Then the following error occurred: Duplicate symbol "_main" in ".\src\xxxxx.obj".

A: When generating the target project, the user file which includes the main function is auto-generated. This file may not be deleted from the target project. Refer to 3.3.6 Deleting the File for details.

4. Reference Document

User's manual: Development environment

Renesas e^2 studio Smart Configurator User Guide (R20AN0451)

Application note

RX Family Adding Firmware Integration Technology Modules to Projects (R01AN1723)

* The latest version can be downloaded from the Renesas Electronics website.

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Dec.1.17	—	First edition issued

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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
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   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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