RZ/N2L Group

Quick Start Guide: EtherCAT Slave Software

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Introduction

This document explains Sample Program setup procedures for EtherCAT® slave functionalities with the adapted EtherCAT Stack Code for Renesas RZ/N2L platform. This describes steps to confirm slave behavior and stack features using TwinCAT®Master Configuration tool.

Target Device

RZ/N2L

Contents

1. Overview

This document describes how to run EtherCAT on the RZ/N2L Group. Run the standalone variant using only one core.

EtherCAT(Ethernet for Control Automation Technology) is an Ethernet based fieldbus system, developed by Beckhoff Automation. Development of EtherCAT was to apply Ethernet for automation applications (e.g., for motion control, I/O, sensors) requiring short data update times with low communication jitter and reduced hardware costs.

Tool to generate EtherCAT Slave Stack Code (SSC Tool) is available to the ETG members free of charge. This can be downloaded from the ETG website. SSC tool can be used to generate customized stack, device description files (ESI) and individual source code documentation to suit the developer's own needs.

This document describes the procedure for testing the EtherCAT slave function using EtherCAT stack code compatible with the Renesas RZ/N2L platform. Scope of the documentation is limited to explaining how to use the SSC tool for EtherCAT slave stack code generation and testing its behavior against TwinCAT masters and test applications.

1.1 Abbreviations/Definitions

Table 1. Abbreviations/Definitions

Index	Abbreviations /Definitions	Description
1	CoE	CAN application protocol over EtherCAT
2	EEPROM	Electrically Erasable Programmable Read-Only Memory
3	ESC	EtherCAT Slave Controller
4	ESI	EtherCAT Slave Information
5	FoE	File Access Over EtherCAT
6	I2C	Inter-Integrated Circuit
7	MB	Mailbox
8	PDO	Process Data Object
9	SSC	Slave Stack Code
10	EoE	Ethernet Over EtherCAT

1.2 Reference

Technical information about EtherCAT is available via ETG member site, and information about RZ/N2L is available via Renesas.

Table 2. Technical Inputs

Index	Technical Inputs
1	r20ut4984jg0100-rskrzn2l-usermanual_c.pdf
2	r01uh0955ej0110-rzn2l.pdf

2. Features

EtherCAT slave stack code generated by SSC Tool provides the functionality of EtherCAT slave controller.

Includes the following features:

- ESM (EtherCAT State Machine)
- Mailbox protocols:
  - CoE (CAN application protocol over EtherCAT)
- Synchronization Modes:
  - Free Run
  - Sync Manager Synchronization
  - DC Synchronization
- I/O function:
  - I/O Input DIP SW
  - I/O Output LED

EtherCAT is a registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

3. Project Setup

3.1 Requirements

Table 3. Requirements

Item	Description
Board	Renesas Electronics RZ/N2L RSK Board
IDE	IAR Systems - IAR Embedded Workbench® for ARM Version 9.30.1 Renesas Electronics - e² studio 2022-07 (RZN2L_FSP_Packs_v1.0.0) - FSP Smart Configurator (rznfsp_v1_0_0_e2s_v2022-07) - FSP Smart Configurator (rznfsp_v1_0_0_rzsc_v2022-07)
Emulator	IAR Systems I-jet SEGGER J-Link
SSC Tool	Slave Stack Code (SSC) Tool Version 5.13
Software PLC	Beckhoff Automation TwinCAT3

3.2 Hardware

This document describes the major hardware. Please refer to prototype board user's manual and schematic for more board details.

Device connection between EtherCAT master and slave is shown below.

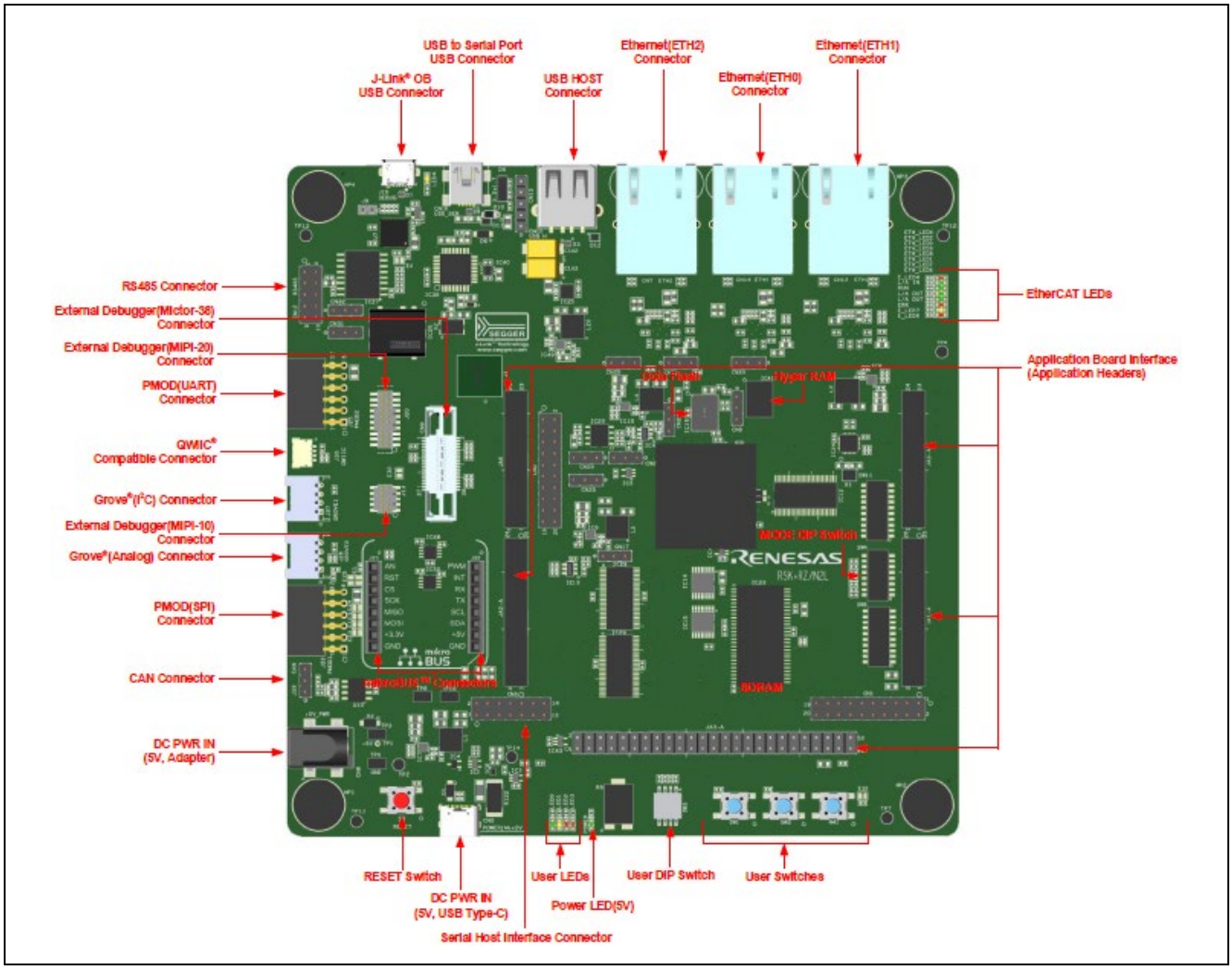


Figure 3.1: RZ/N2L RSK board layout

Table 4. Jumper Pin settings

Reference	Jumper Position	Description
CN8	Short 1-2	Use Octa Flash
	Short 2-3	**Use QSPI Serial Flash**
CN17	Short 1-2	VCC1833_2 Use power supply at 3.3V
	Short 2-3	**VCC1833_2 Use power supply at 1.8V**
CN20	**Short 1-2**	**Use 3 ports in same PHY mode**
	Short 2-3	Use ports 0, 1 in the same PHY mode, use port 2 in different PHY modes
CN21	**Short 1-2**	**Use 3 ports in same PHY mode**
	Short 2-3	Use ports 0, 1 in the same PHY mode, use port 2 in different PHY modes
CN22	**Short 1-2**	**Use 3 ports in same PHY mode**
	Short 2-3	Use ports 0, 1 in the same PHY mode, use port 2 in different PHY modes
CN24	Short 1-2	VCC1833_2 Use power supply at 3.3V
	Short 2-3	**VCC1833_2 Use power supply at 1.8V**

Table 5. Switch4 settings

SW4	Setting	Description
SW4-1	ON	16bit bus boot mode
SW4-2	OFF	
SW4-3	ON	
SW4-4	ON	MDD=0, JTAG Authentication by Hash is disabled.
SW4-5	OFF	MDW=1, ACTM 1 wait, should be set when TCM is used with CPU operating frequencies above 400MHz
SW4-6	OFF	Valid signals other than trace signals
SW4-7	ON	Signals other than the external bus are valid
SW4-8	OFF	SW3 is valid

Table 6. Switch8 settings

SW8	Setting	Description
SW8-1	OFF	Enable the "LED_GREEN" signal.
SW8-2	ON	
SW8-3	OFF	
SW8-4	ON	Enable the "LED5" signal.
SW8-5	OFF	
SW8-6	OFF	RS485_DE & M2_VN Configuration Switch Setting
SW8-7	OFF	
SW8-8	OFF	CAN_TX & IRQ4 & P02_2 Configuration Switch Setting
SW8-9	OFF	
SW8-10	OFF	

Table 7. Switch11 settings

SW11	Setting	Description
SW11-1	ON	Enable the "LED_RED2" signal.
SW11-2	OFF	
SW11-3	OFF	
SW11-4	OFF	RS485_RX & M2_UP Configuration Switch Setting
SW11-5	OFF	
SW11-6	OFF	P21_5 & M2_VP Configuration Switch Setting
SW11-7	OFF	
SW11-8	OFF	CAN_RX & ADTRG & P01_7 Configuration Switch Setting
SW11-9	OFF	
SW11-10	OFF	

Build and run the sample code on the RZ/N2L RSK board by following the steps below.
Both, loading into RAM and flash can be done using IAR Embedded Workbench or e2studio.

1. Connect the decoder to the header "J20" on the RZ/N2L RSK board."

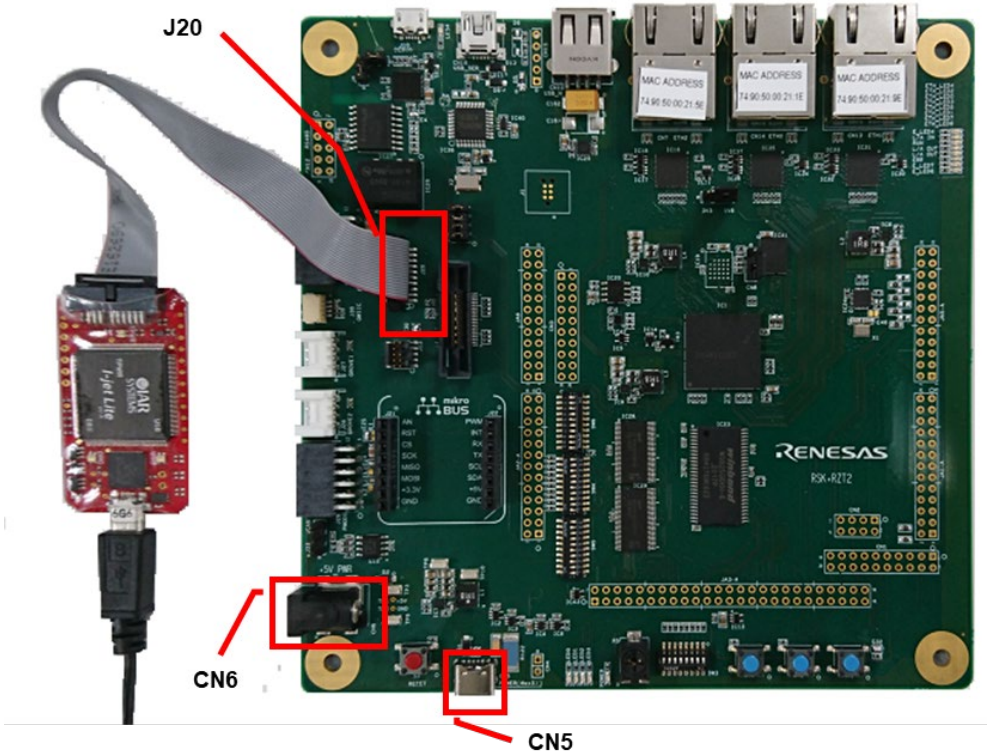


Figure 3.2: RZ/N2L RSK board debug connection diagram

When using J-Link OB, connect the USB cable to the header "J10" and set "J9" to open.

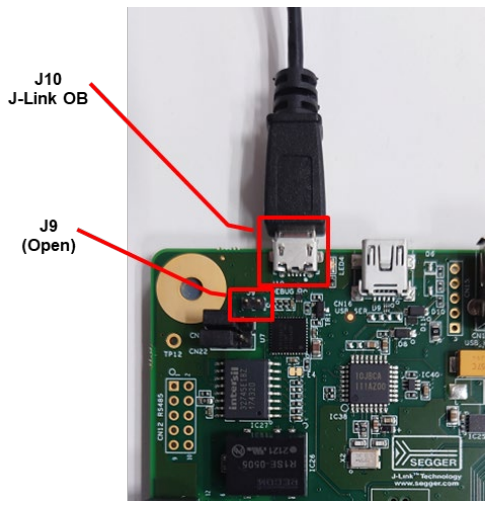


Figure 3.3: RZ/N2L RSK board debug connection diagram (J-Link OB)

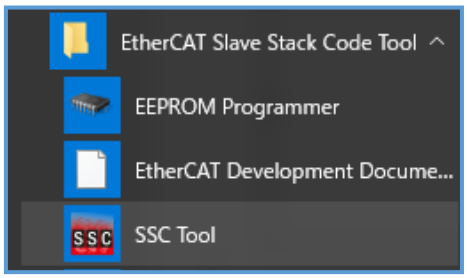
2. Power is supplied using a USB cable (Type-C) or an AC / DC adapter. When using a USB cable (Type-C), connect it to the USB connector "CN5" of the RZ/N2L RSK board. When connecting the AC/DC adapter, connect it to the connector "CN6" of the RZ/N2L RSK board.

3.3 Generating the Slave Stack Code

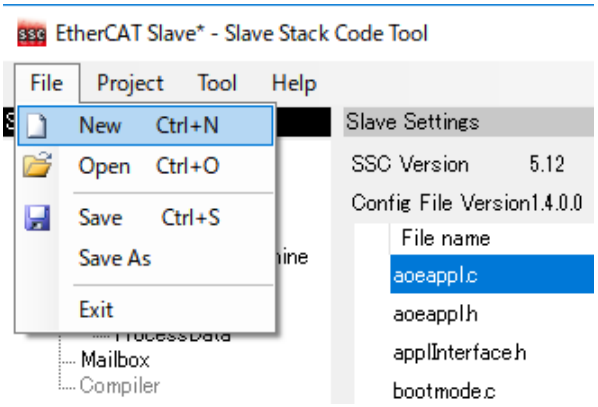
SSC Tool is used for generating the slave stack code.

Note). Replace the folder name in the following description according to the tool to be used.

1. Start the SSC Tool from the Window Start menu.

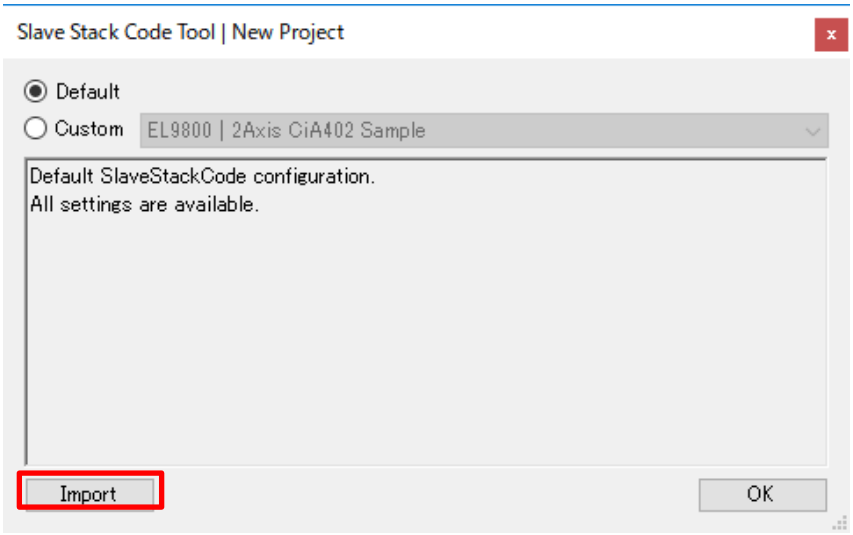


2. Select File > New.

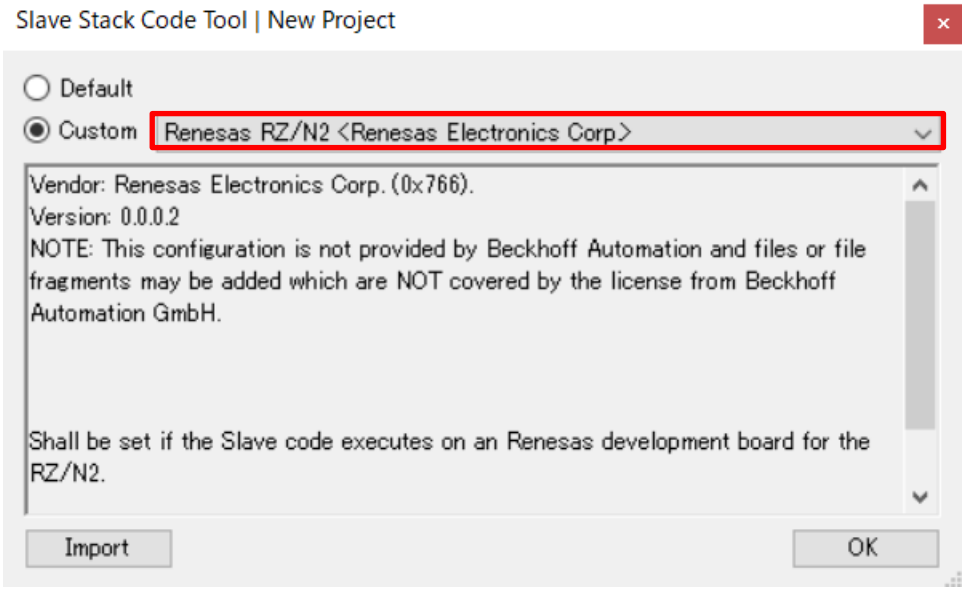


3. Click the [Import] button and select the SSC Tool configuration file at,

"RZN2L_EtherCAT_RSK_rev0100\common\ecat_IO\SSCconfig\Renesas_RZN2_config.xml"

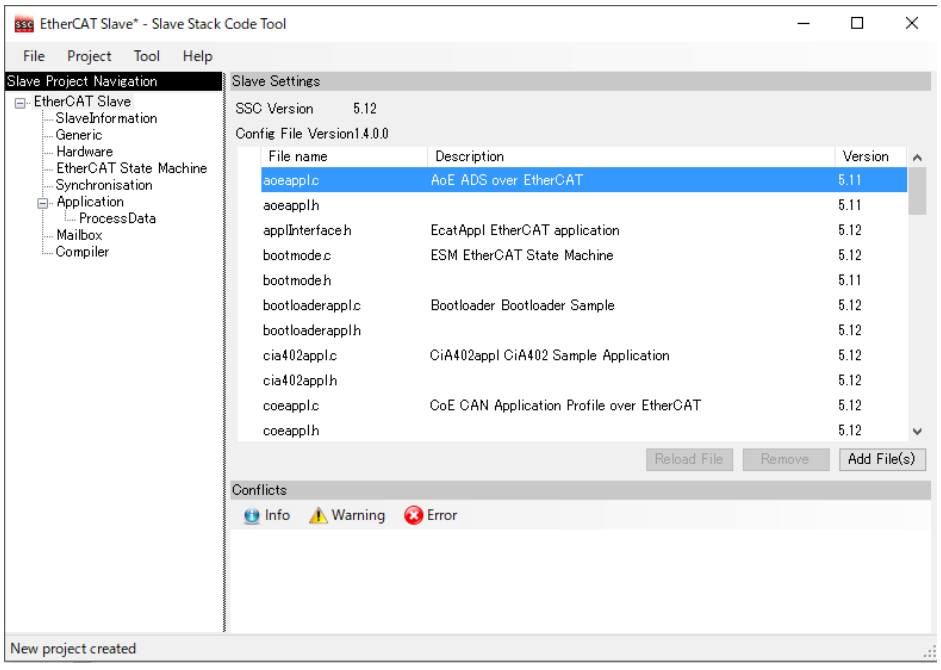


4. After the configuration file is read, the window changes as follows:

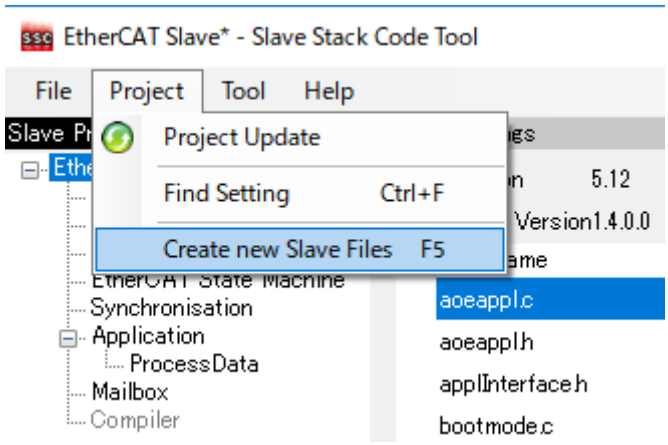


Once the configuration file is read, it is registered in Custom and is selectable from the drop-down list.

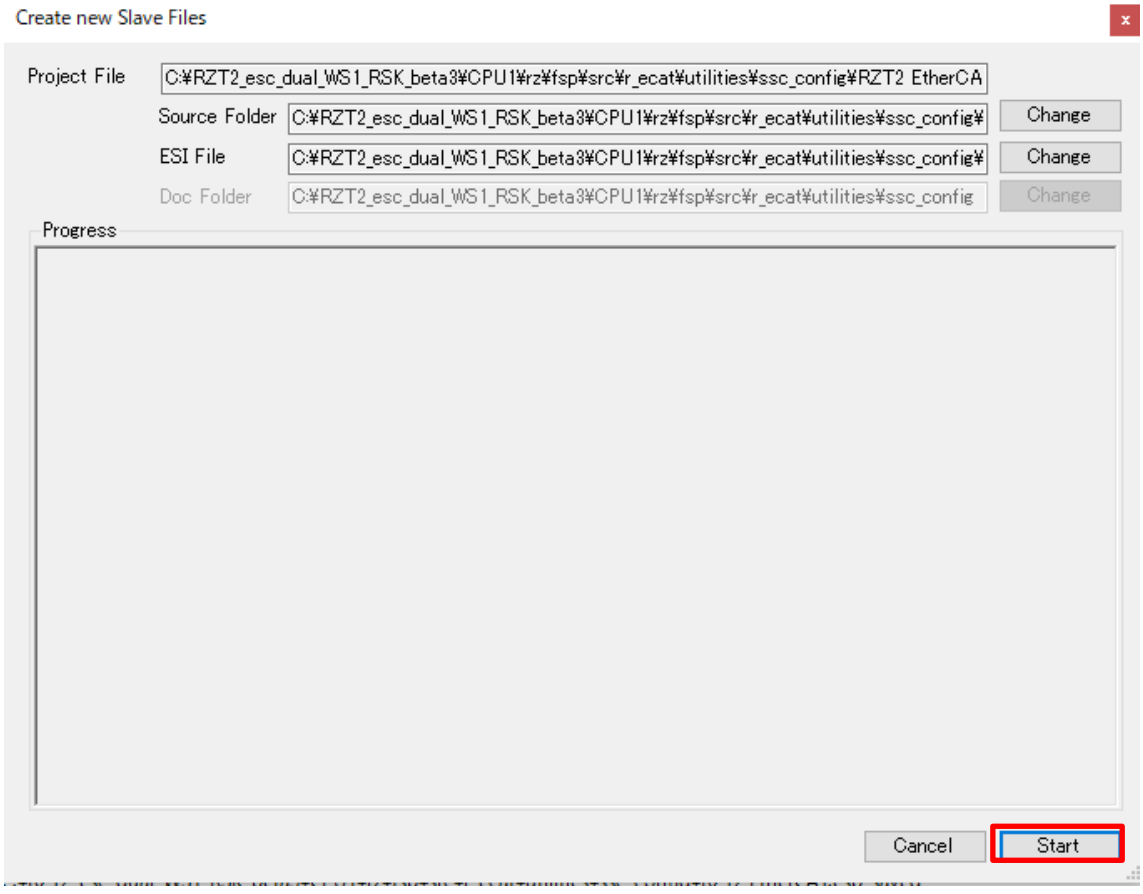
5. After clicking the [OK] button, the following window opens.



6. Select Project > Create new Slave Files.

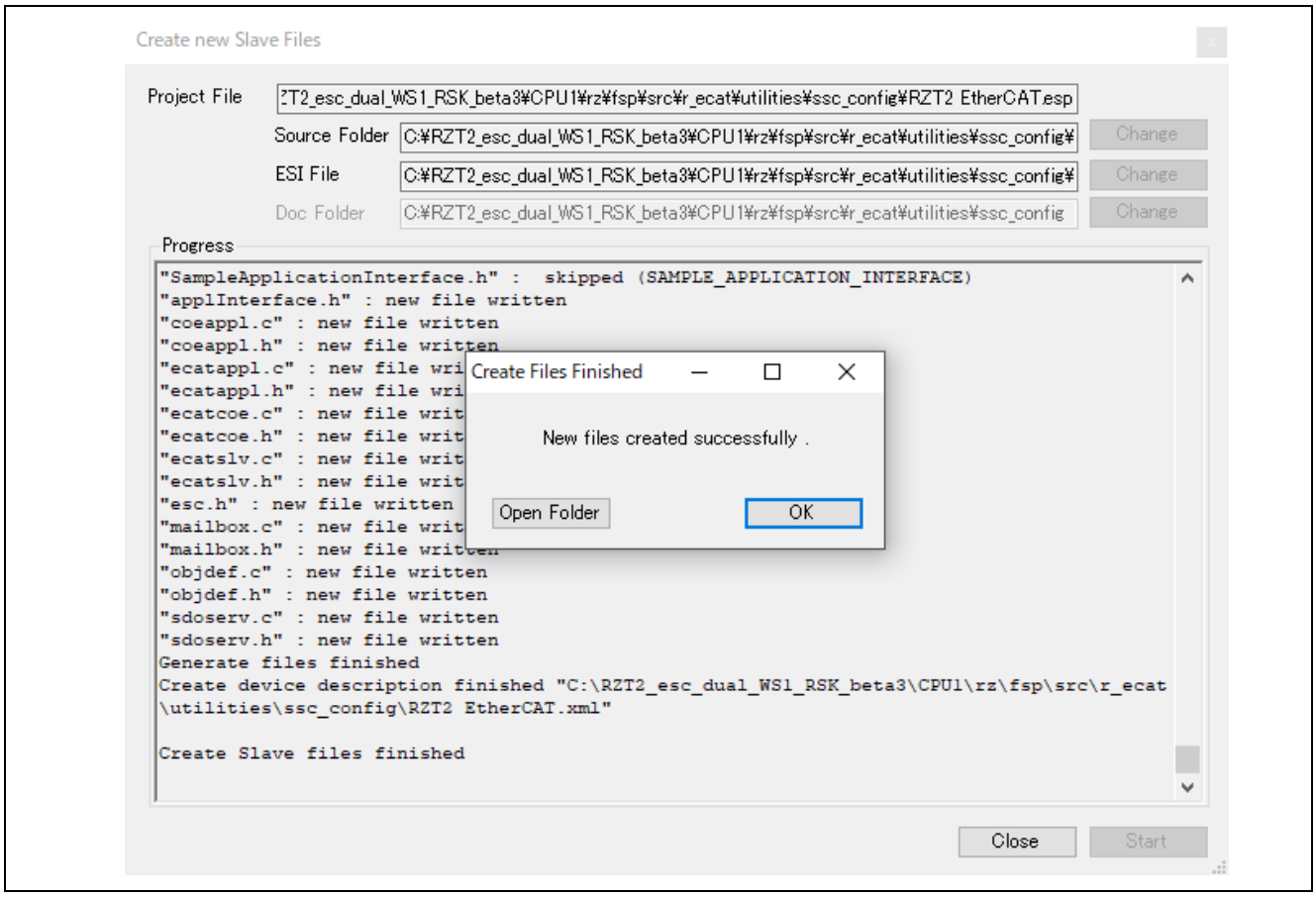


7. Click the [Start] button to start creating the EtherCAT Slave Stack Code.



8. When a message “New file created successfully” appears, the creation processing is completed, and the source files are located in the following folder.

“RZN2L_EtherCAT_RSK_rev0100\common\ecat_IO\SSCconfig\Src”



9. Move the generated EtherCAT slave stack code to the EtherCAT application source folder. The sampleappl.c and sampleappl.h are stored in the destination “\application\ecat” folder. When moving the slave stack code to the application folder, be careful not to delete these files. Remove the original Src code (code generated in the Src folder by SSC) from the folder or exclude the Src code from your build target.

Source folder: (code generated in the Src folder by SSC)
“RZN2L_EtherCAT_RSK_rev0100\common\ecat_IO\SSCconfig\Src”

Move destination folder:
“RZN2L_EtherCAT_RSK_rev0100\project\rzn2l_rsk_rzn2l\ecat_IO\ewarm (e2studio) \src\ ethercat\beckhoff”

4. Setting up a TwinCAT3

4.1 Copying the ESI Files

Before starting TwinCAT, copy the ESI files that are included in the release folder to TwinCAT destination "\TwinCAT\3.x\Config\IO\EtherCAT"

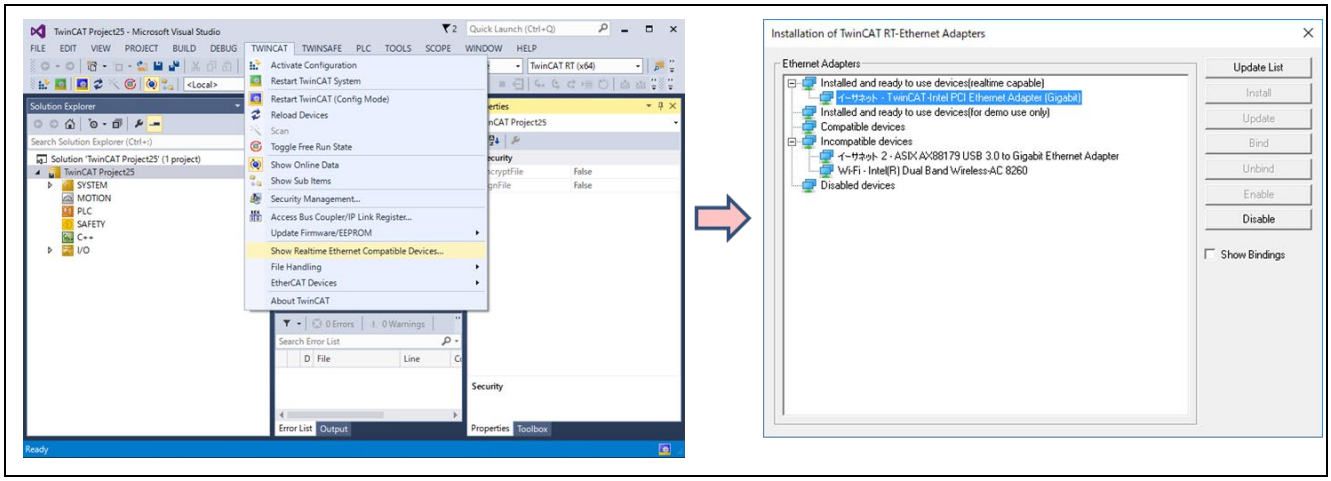
ESI file for current release available at,

"RZN2L_EtherCAT_RSK_rev0100\common\ecat_IO\ESI\Renesas EtherCAT RZN2.xml"

4.2 Add Driver

Add the Ether driver for TwinCAT. (First time only)
From the start menu, select [TwinCAT3] → [Show Realtime Ethernet Compatible Devise].

Select the connected Ether port from the communication ports and install it.



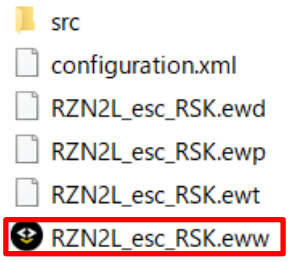
5. Running the sample application

5.1 Build and debug sample code for EWARM

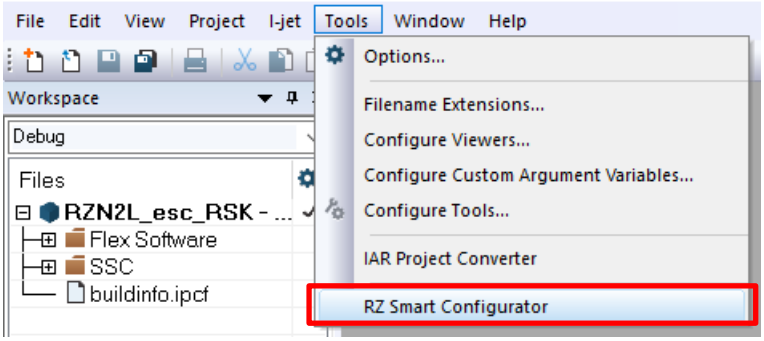
Build the sample code and load it into RAM using IAR Embedded Workbench.

Note). Please install FSP Smart Configurator in advance.
Refer to the latest getting started guide.(R01an6434ejxxxx- rzt2-rzn2.pdf)

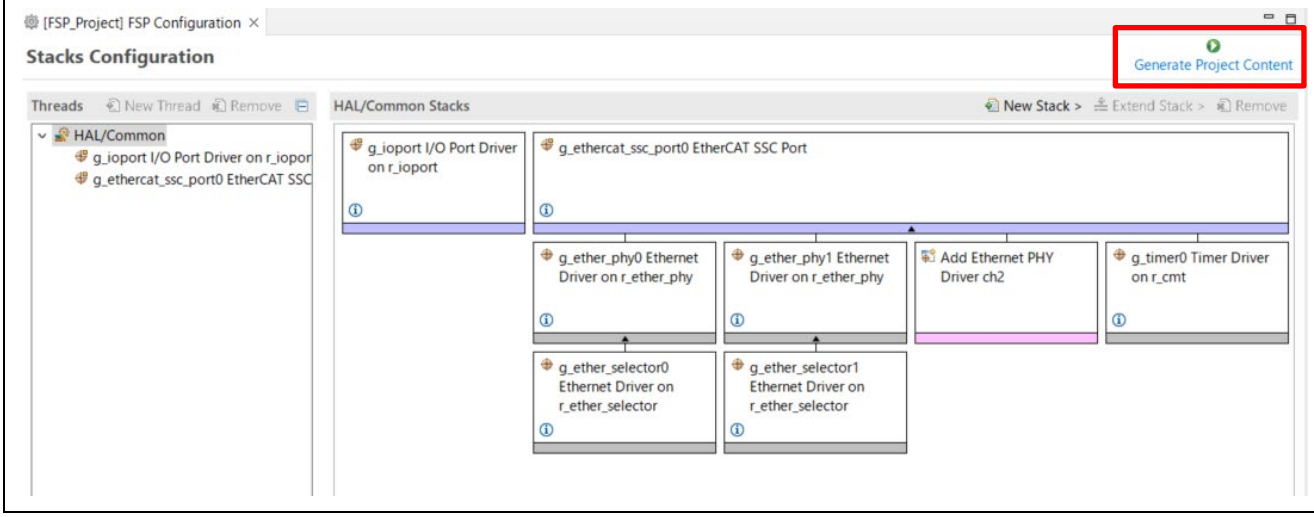
1. Open the sample project.
“RZN2L_EtherCAT_RSK_rev0100\project\rzn2l_rsk_rzn2l\ecat_IO\ewarm\RZN2L_esc_RSK.eww”



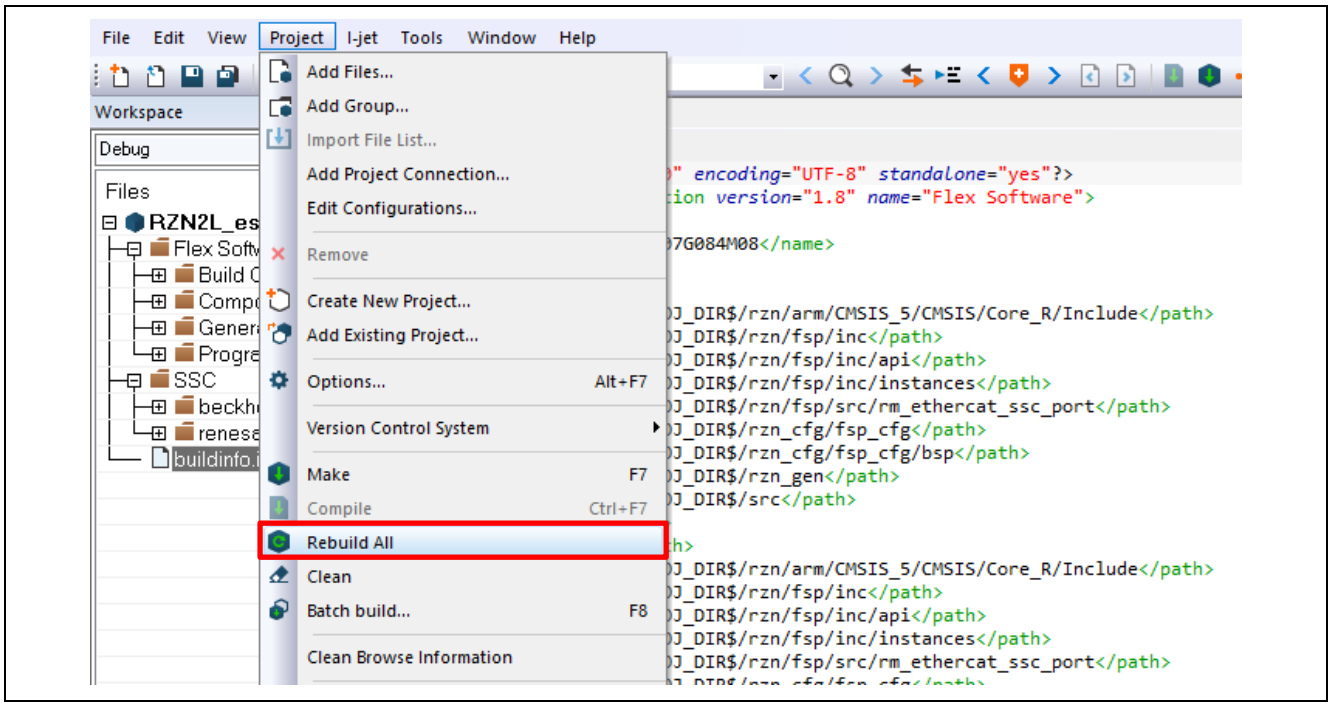
2. Open the “RZ Smart Configurator”



3. Generate the code with "Generate Project Content".

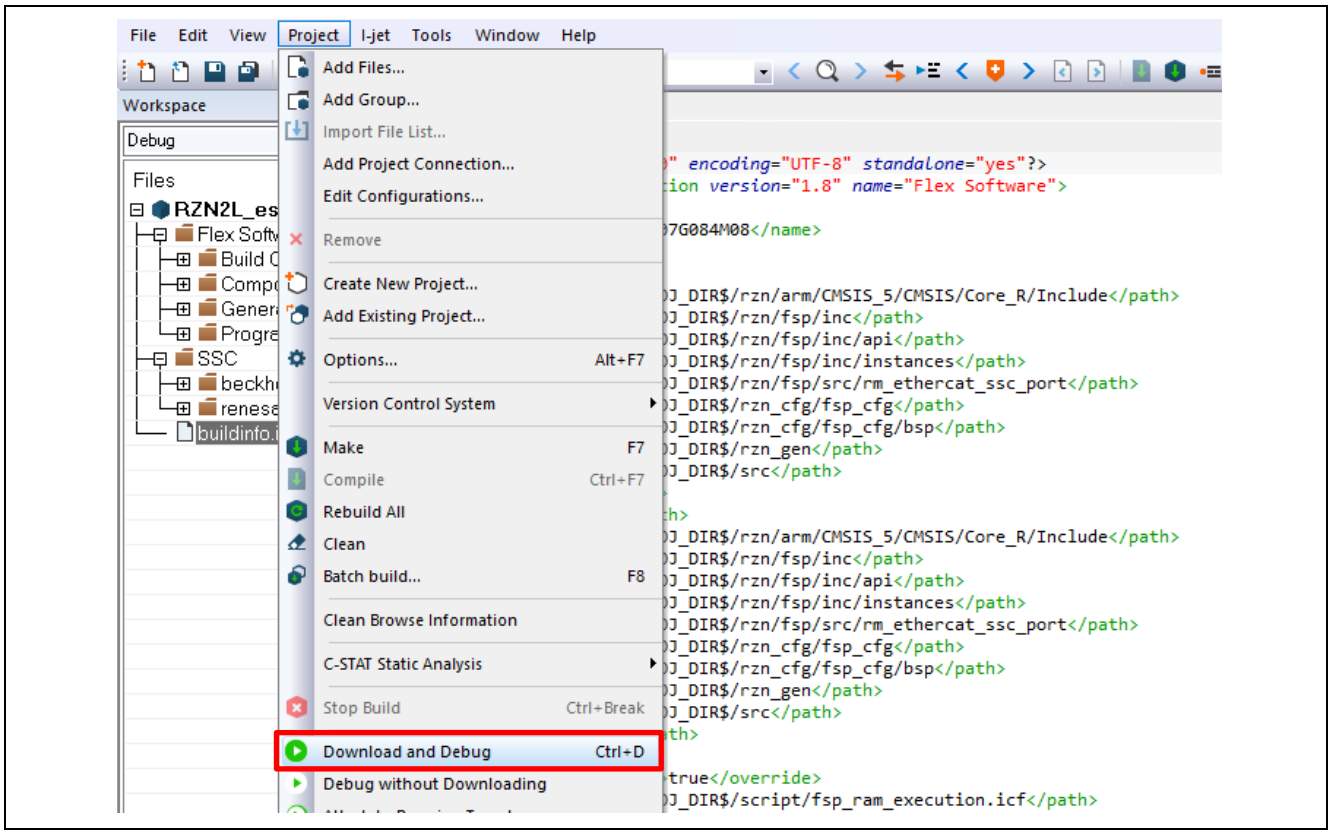


4. Select the “Rebuild All” item from the “Project” menu to rebuild the project.

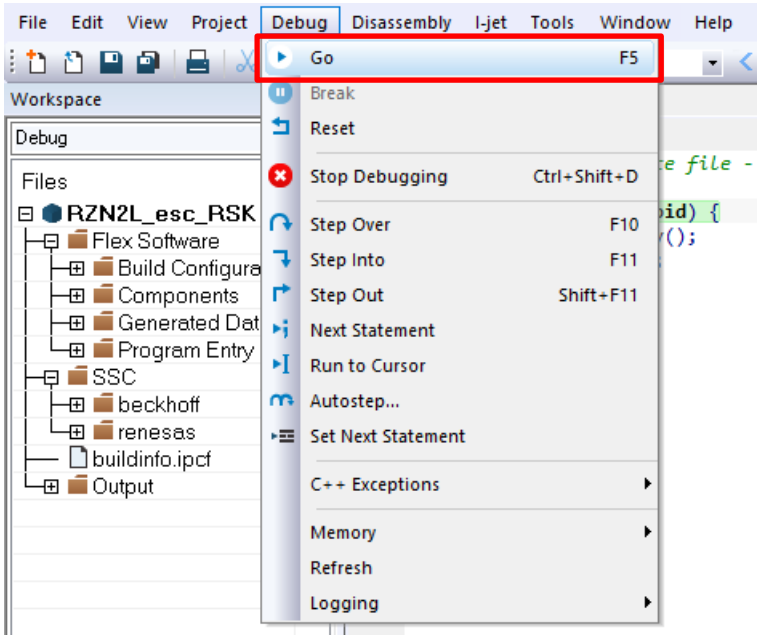


5. Press the “RESET” switch of the RSK + RZN2 prototype board.

6. While the board and I-jet are connected, click on the “Download and debug” button in the “Project” toolbar.



7. Press the "Resume" button for the project. Program is running.

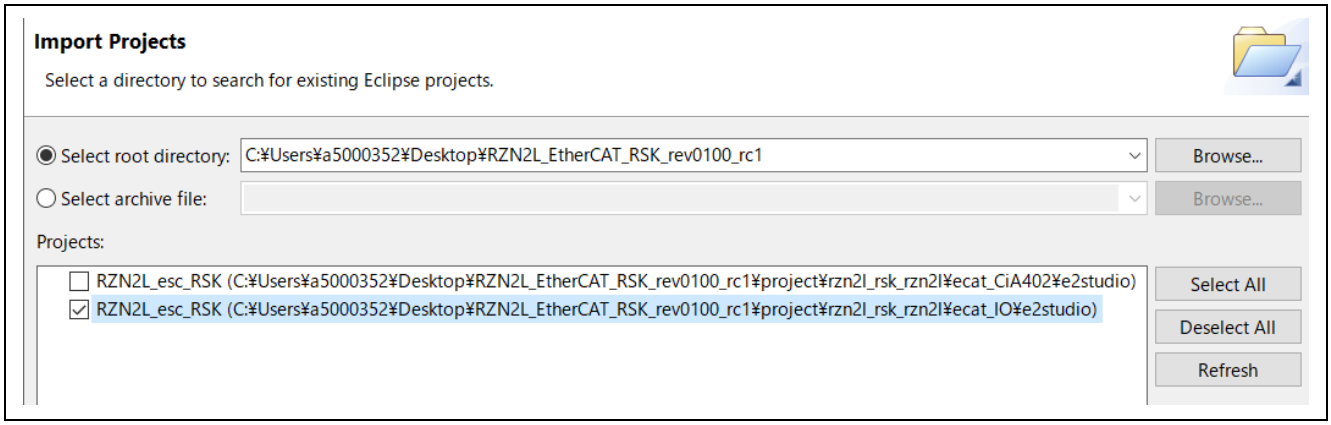


5.2 Setting sample code for GCC

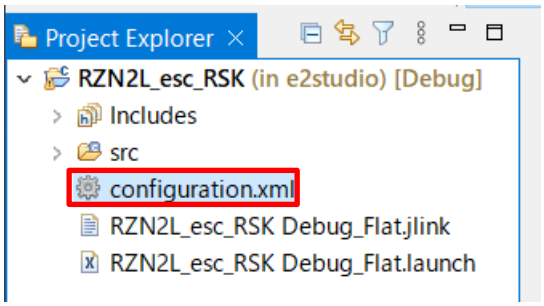
Build the sample code and load it into RAM using Renesas Electronics e² studio.

Note). Please install e2studio and adapt the FSP_Packs_v1.0.0 in advance.
Refer to the latest getting started guide.(R01an6434ejxxxx- rzt2-rzn2.pdf)

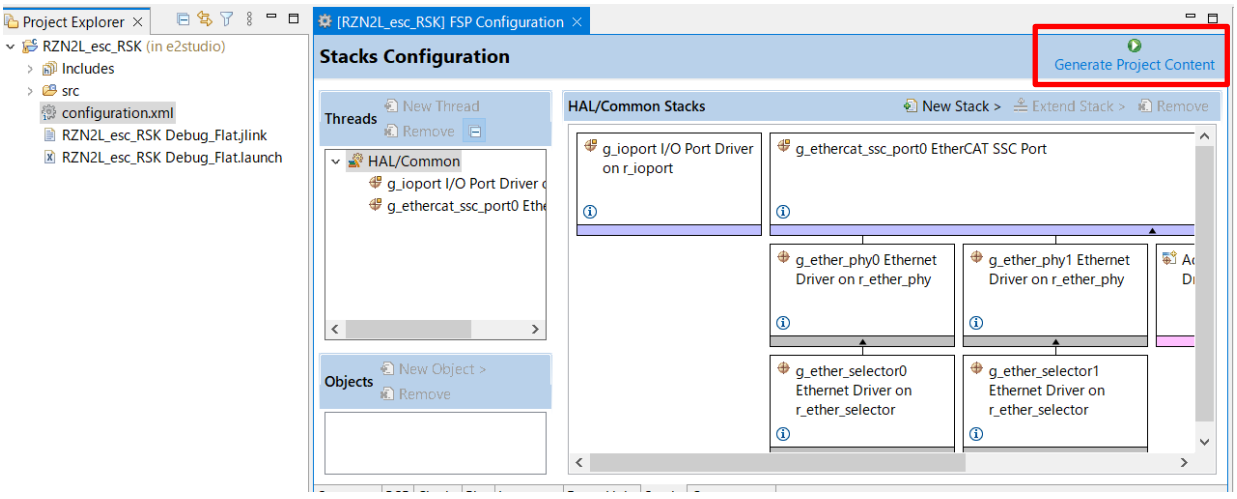
1. Import the sample project. After the program is started, by selecting [File] → [Import] → [Existing Projects into Workspace]. Check the "select root directory" and select “RZN2L_EtherCAT_RSK_rev0100\project\rzn2l_rsk_rzn2l\ecat_IO” folder →[Finish].



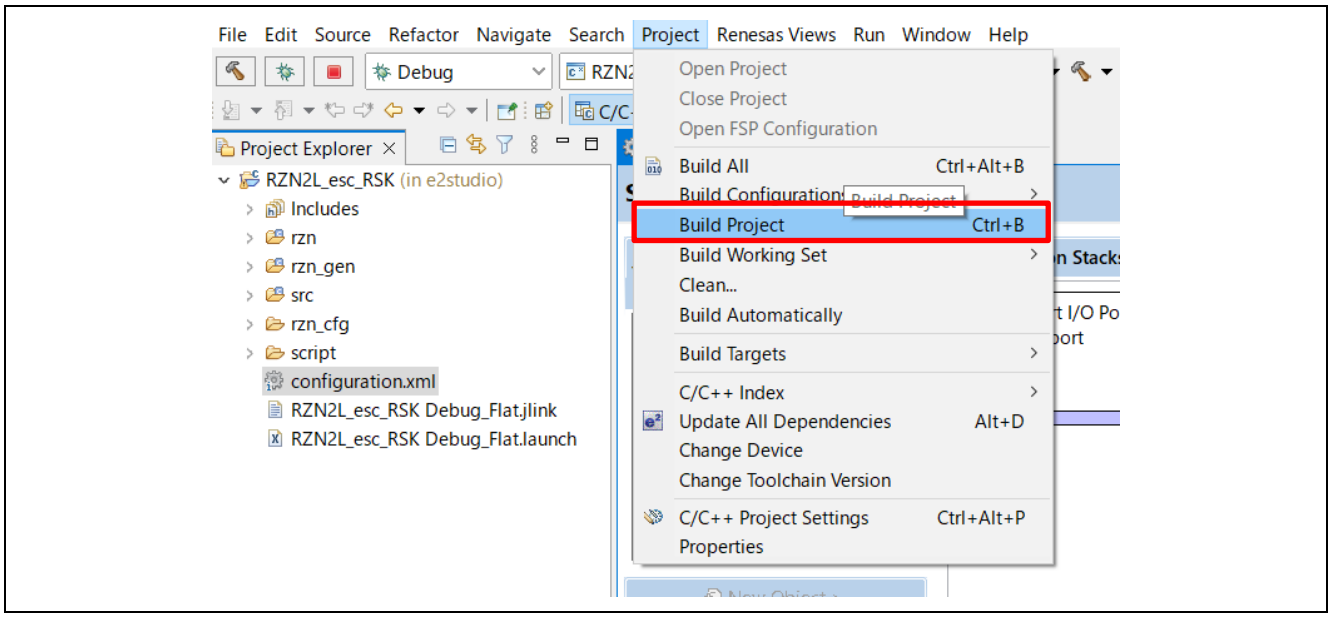
2. Open "cofiguration.xml" in the "RZN2L_esc_RSK " project



3. Generate the code with "Generate Project Content".

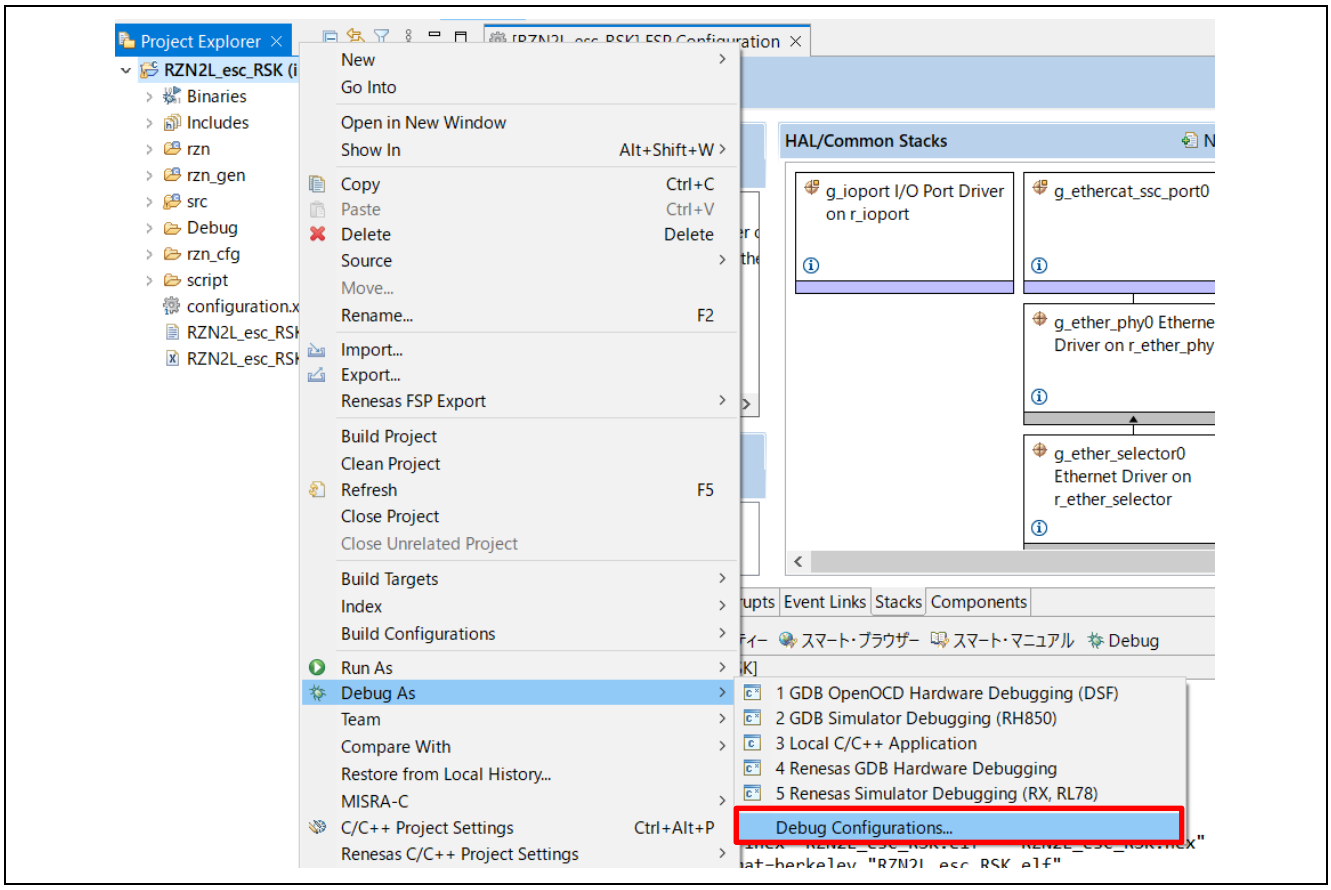


4. Select and build the "RZN2L_EtherCAT_RSK_rev0100" project.

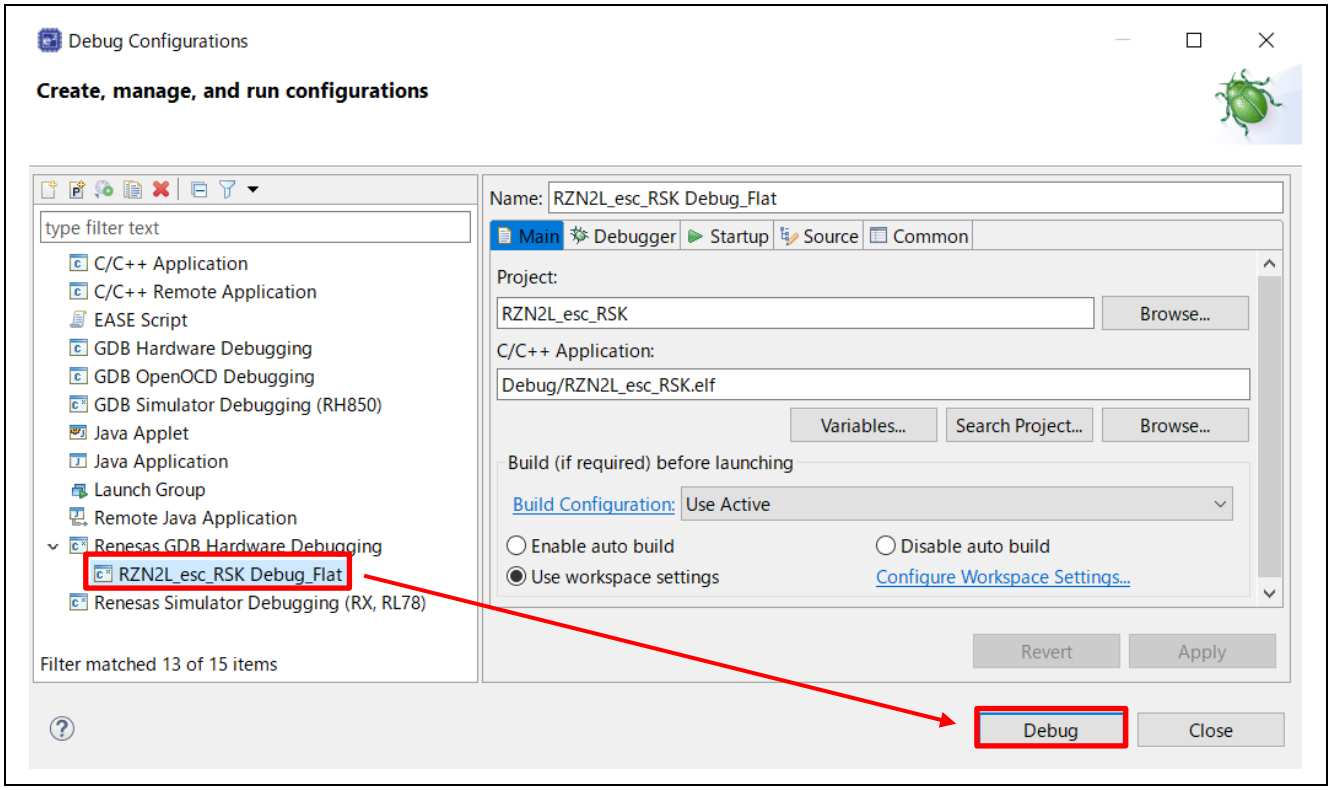


5. Press the “RESET” switch of the RSK + RZN2L board.

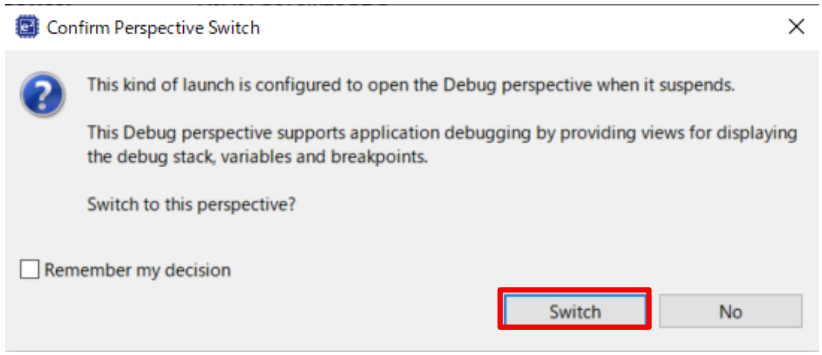
6. Connect J-Link to the RSK board, start debugging in the following procedure.
In [Project Explorer] view, right click the node of project to be debugged and select [Debug As] → [Debug Configurations].



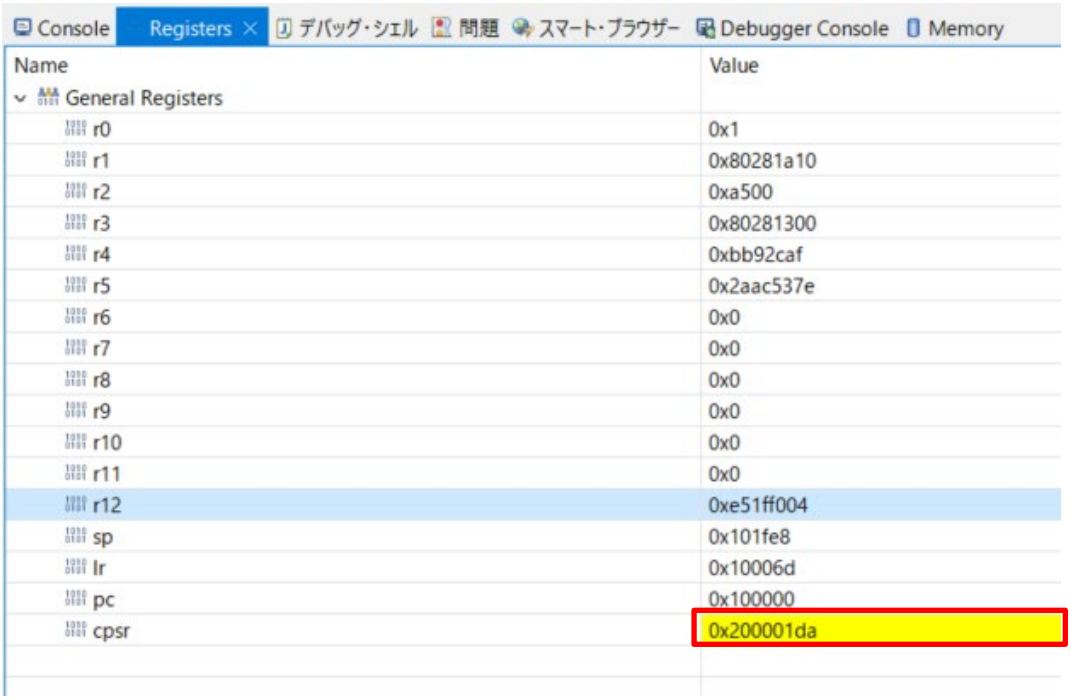
[Renesas DBG Hardware Debugging] → [RZN2L_esc_RSK_Debug_Flat] item,
then press [Debug]



Following dialog will appear, so switch to the debug screen.



7. Before running the loaded program, change the CPSR register of CR52 general register on Registers tabs.
   Change the register value from “0x200001fa” to “0x200001da”.
   If the CPSR register value has not changed, program will stop at Default_Handler () at run time.



8. Press the "Resume" button for the project. Program will stop at hal_entry ().
   Press the "Resume" button again. Program is running.

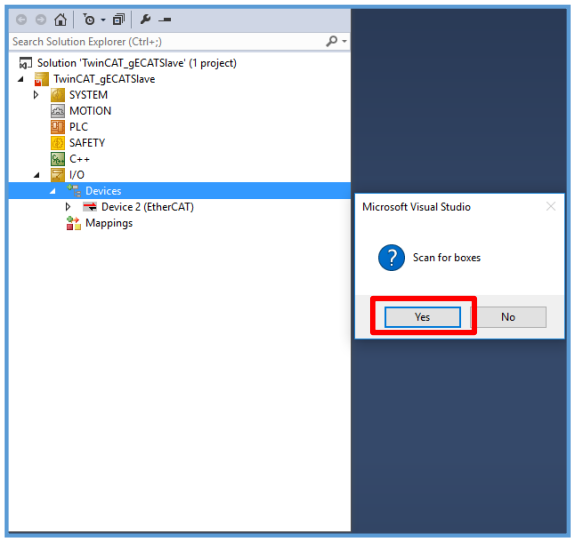
6. Connecting to TwinCAT3

Start TwinCAT3 by using the procedure described below,
From the start menu, select [Beckhoff] → [TwinCAT3] → [TwinCAT XAE (VS2013)].

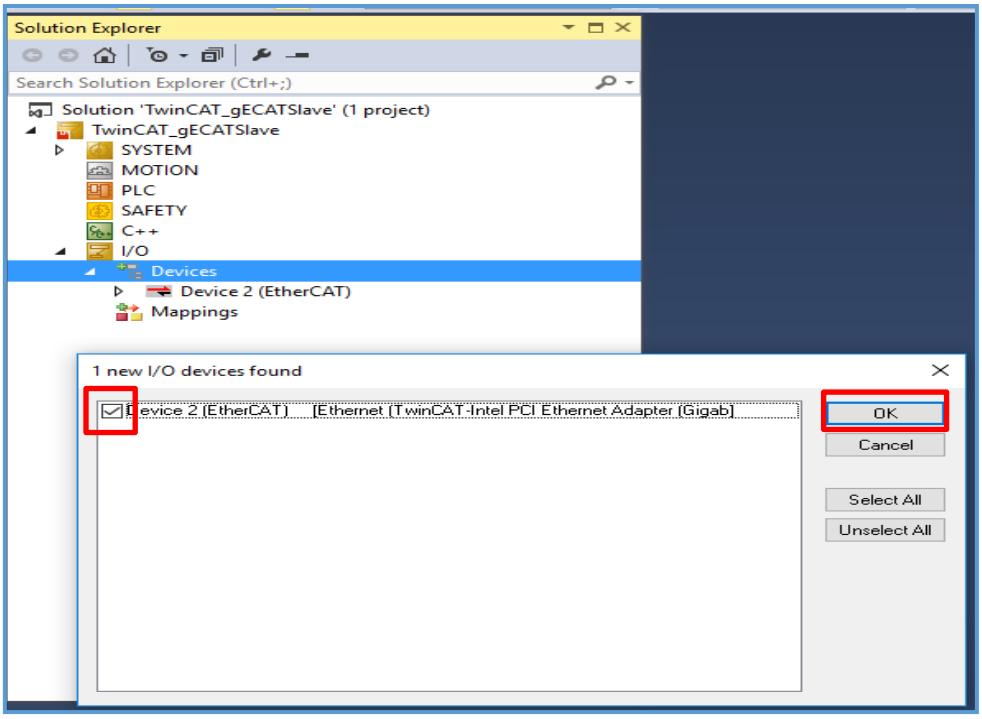
After the program is started, by selecting [File] → [New] → [Project], create a new project of the TwinCAT XAE Project type. The subsequent procedure is described below.

6.1 Scanning I/O Devices

1. (Scan for devices): Under solution explorer -> I/O -> Devices, select 'Scan' as in Figure below

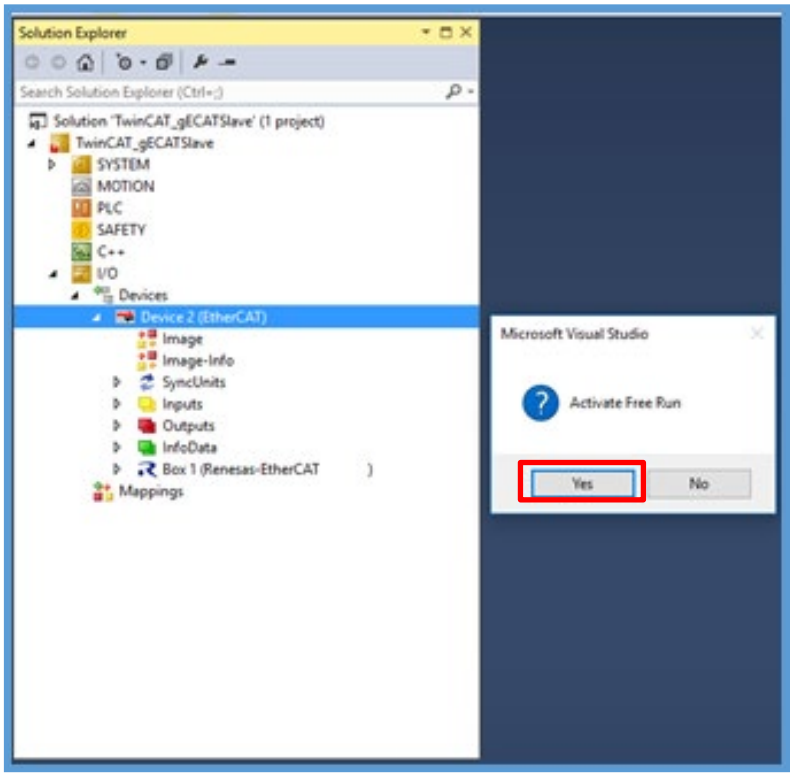


2. (Selecting port): The EtherCAT port will be displayed as below. Select and press OK.



Note). This will list EtherCAT master if a valid slave is present in the network.

3. (Activate slave): The slave is listed in the boxes, in our case “Renesas EtherCAT” in box1 shown in figure below. Press activate free run.



6.2 Updating EEPROM Data

If the data of another application has already been written to the EEPROM, replace the data.
The following shows the procedure for replacing the data on the EEPROM:

1. Double-click [Box 1] to display a panel on the right side of the window.
2. Select the [EtherCAT] tab.
3. Click the [Advanced Setting] button.
4. Select [ESC Access] → [EEPROM] → [Hex Editor].
5. Select [Download from List] → Select ESI File
   "*RZN2L_EtherCAT_RSK_rev0100\common\ecat_IO\ESI\esi\Renesas EtherCAT RZN2.xml*"
6. Select "Renesas EtherCAT RZ/N2 2port" or "Renesas EtherCAT RZ/N2 3port"
7. OK and Download.

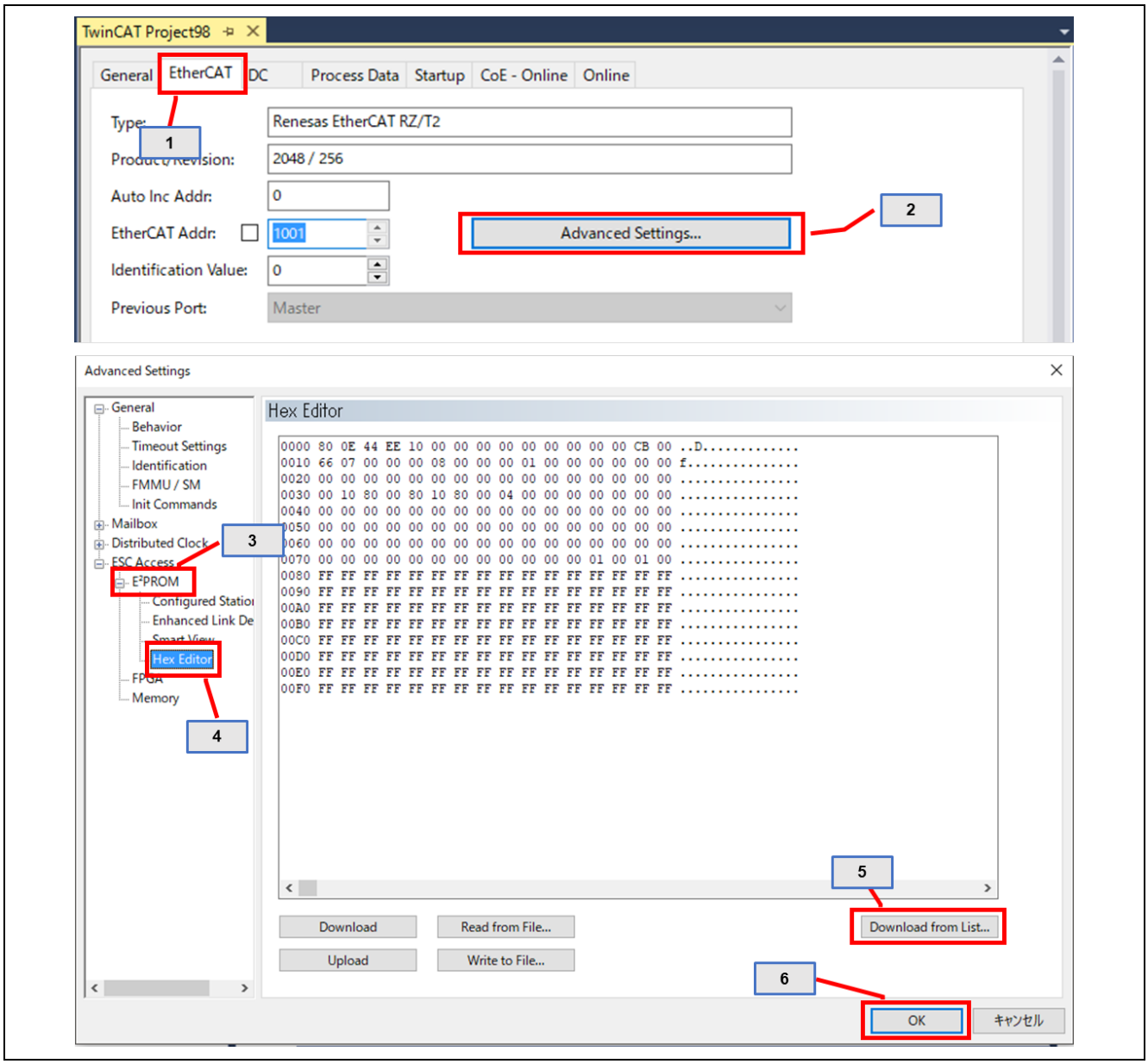


Figure 6.1: EEPROM update

Option A - Create ESI binary file from ESI XML and download.

1. SSC Tool → [Tool] → [EEPROM Programmer].
2. [FILE] → [OPEN] →Browse and select the ESI file.
3. [FILE] → [Save AS] → Select type as binary.
4. A binary file will be generated in the specified folder.
5. [Read from File] Select the ESI binary file → [Download].
6. Confirm the write status using [Upload] option.

After the data is replaced, restart the RZ/N2L (by turning it off and on, or resetting it) so that the new data is applied to the microcomputer. Execute [Restart TwinCAT System].

6.3 Sync Modes

The Slave Stack Code supports different modes of synchronization which are based on three physical signals: (PDI_) IRQ, Sync0 and Sync1.
After setting the synchronous mode, please reflect the setting in [TwinCAT] → [Restart TwinCAT (Config Mode)] → [Reload Devices].

6.3.1 Free Run

In this mode there is no slave application synchronization, AL_EVENT_ENABLED and DC_SUPPORTED disabled.

6.3.2 Sync Manager Synchronization

In this mode the slave application is executed as Sync Manager synchronous. AL_EVENT_ENABLED enabled and DC_SUPPORTED disabled.

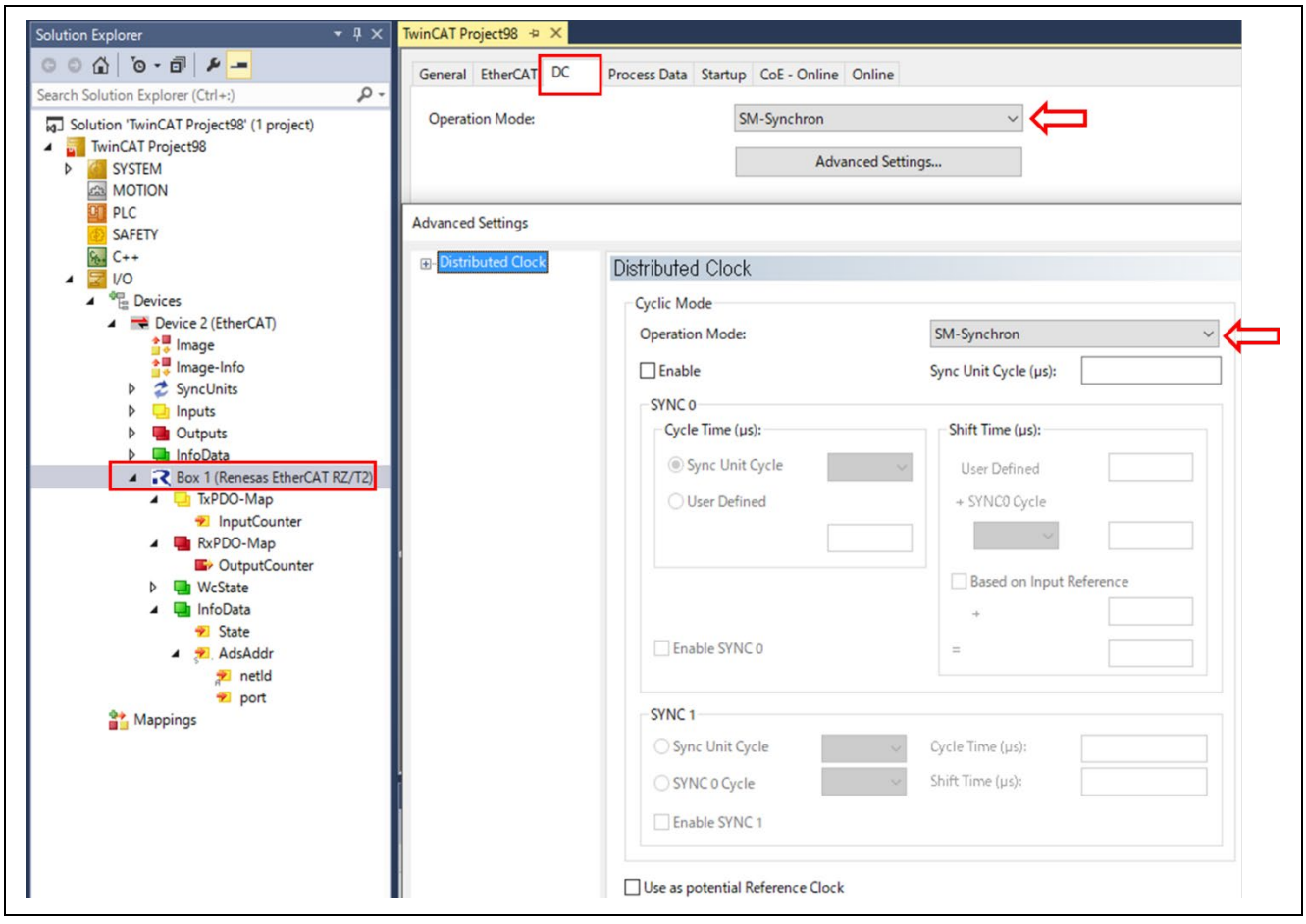


Figure 6.2: SM- Synchronization

6.3.3 DC Synchronization

SyncManager/Sync0 & SyncManager/Sync0/Sync1 synchronous, both AL_EVENT_ENABLED and DC_SUPPORTED are enabled.

1. Master setting for enabling DC synchronization.

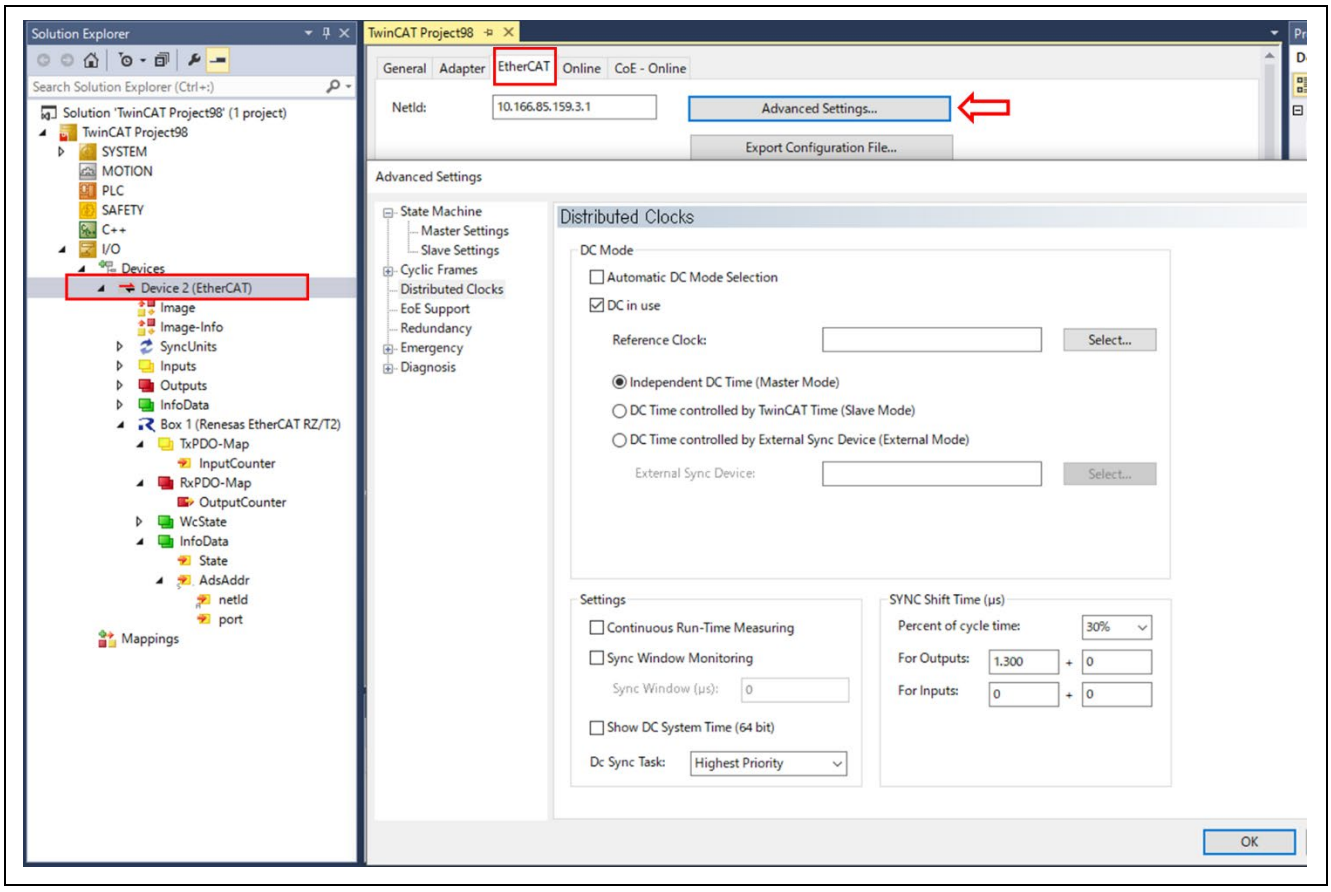


Figure 6.3: DC Setting-Master

2. Slave setting for enabling DC synchronization.

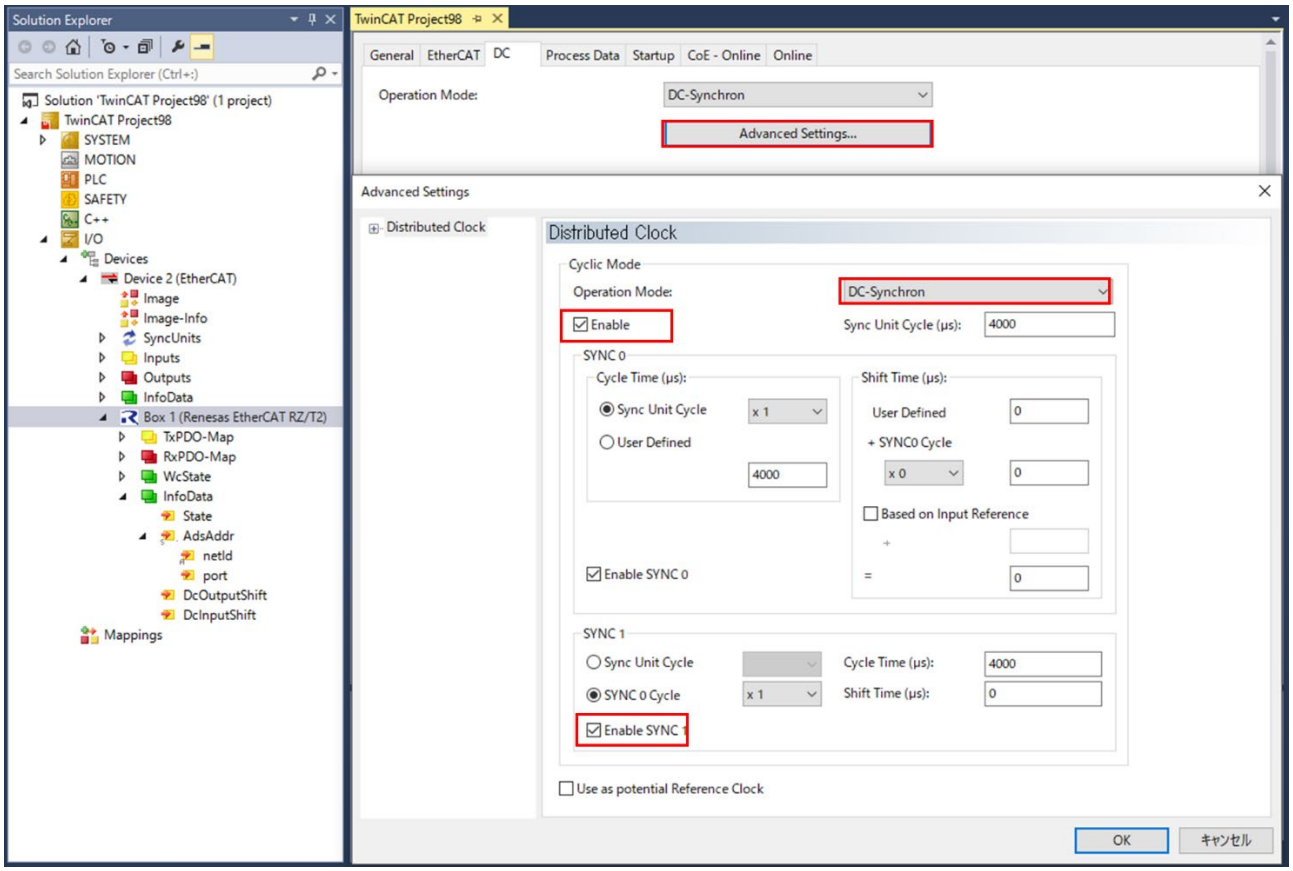


Figure 6.4: DC Setting Slave

Note: SYNC0 and SYNC1 are level triggered interrupt. It can cause synchronization issues due to multiple interrupts in a single pulse. To avoid this issue, pulse width can be reduced by changing the word 2 of EEPROM configuration value in ESI file. It sets the register 0x982 register of EtherCAT slave during power up. Also can be solved by waiting for the line to be low in the interrupt handler by reading the status register 0x98E.

6.4 Testing the I/O Controller

I/O communication can be confirmed by the LED of the RSK board and the DIP SW.

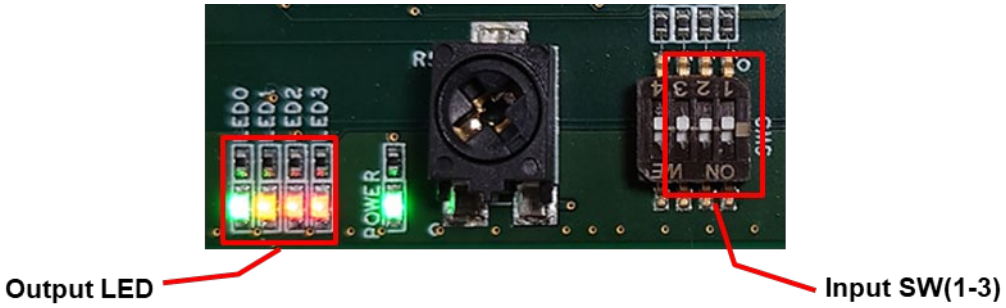


Figure 6.5: LED and DIP SW

To confirm the I/O output, use TwinCAT3 to select [Output Counter] → [Online] →[Write] and enter the desired value.
LED 0 to 3 glow up according to the set value.

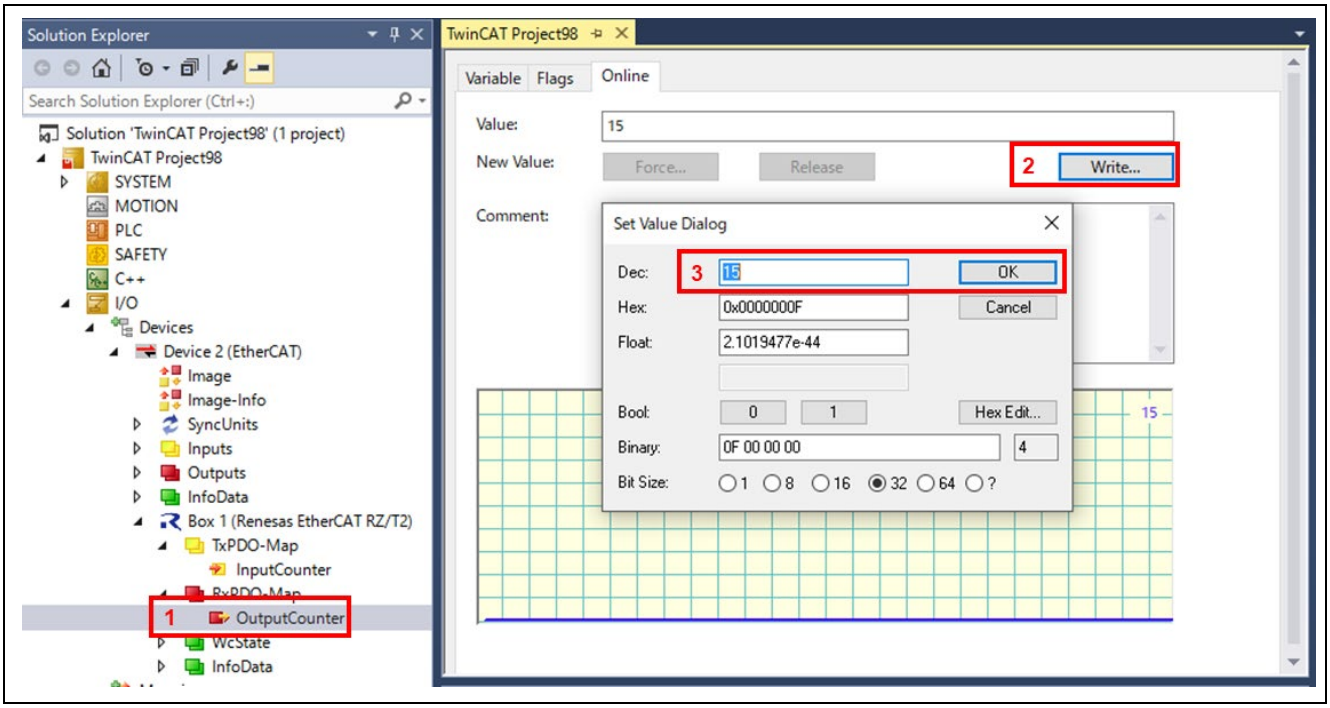


Figure 6.6: I/O Output setting

To confirm the I/O input, use TwinCAT3 to select [Input Counter] → [Online] , 4-bit input value of Dip SW is displayed in Value.

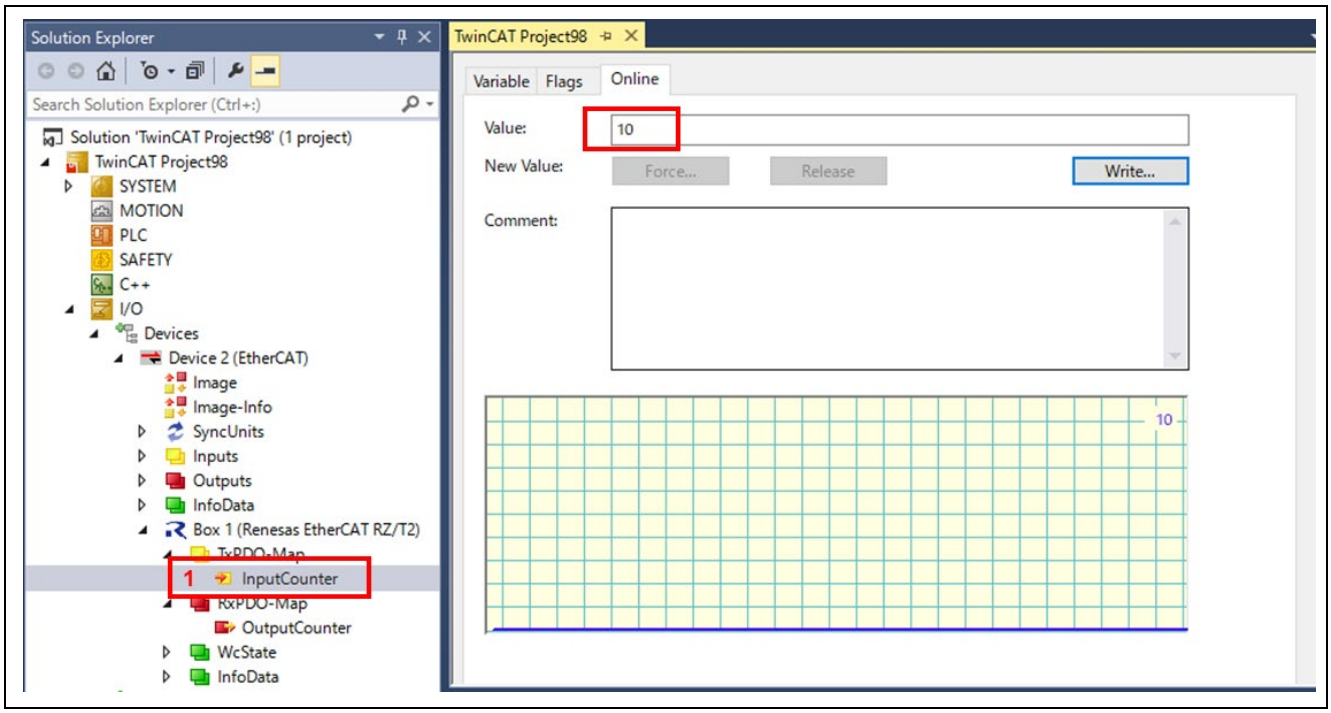


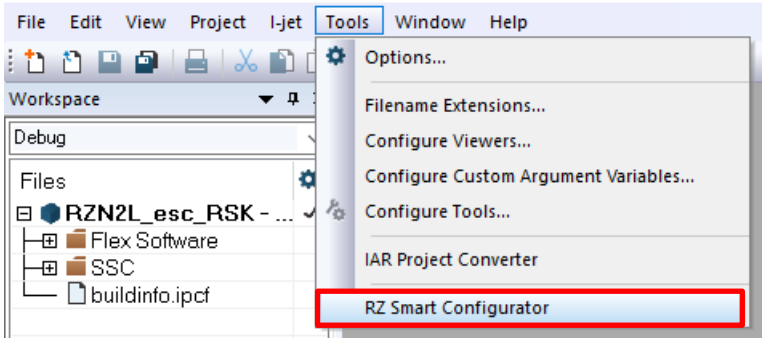
Figure 6.7: I/O Input setting

7. Appendix

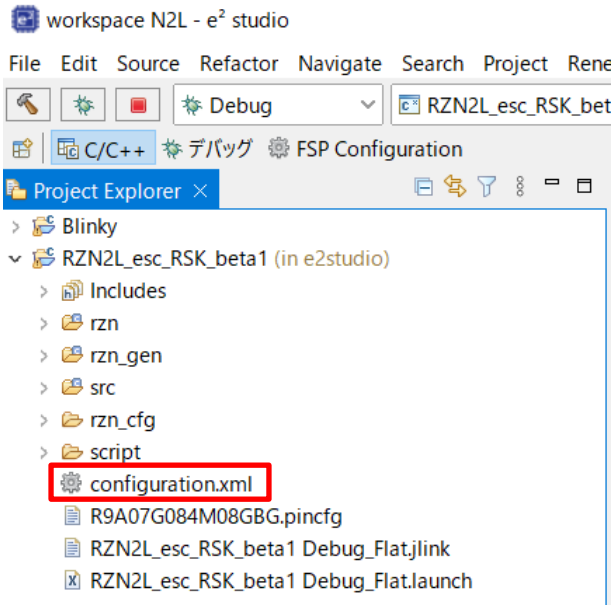
In the FSP1.0.0 compatible sample, it can change the settings from the smart configurator to change the PHY settings and the number of ports.

Method of starting smart configurator depends on the tool.

For EWARM, select [Tool]- [RZ smart configurator] to start smart configurator.



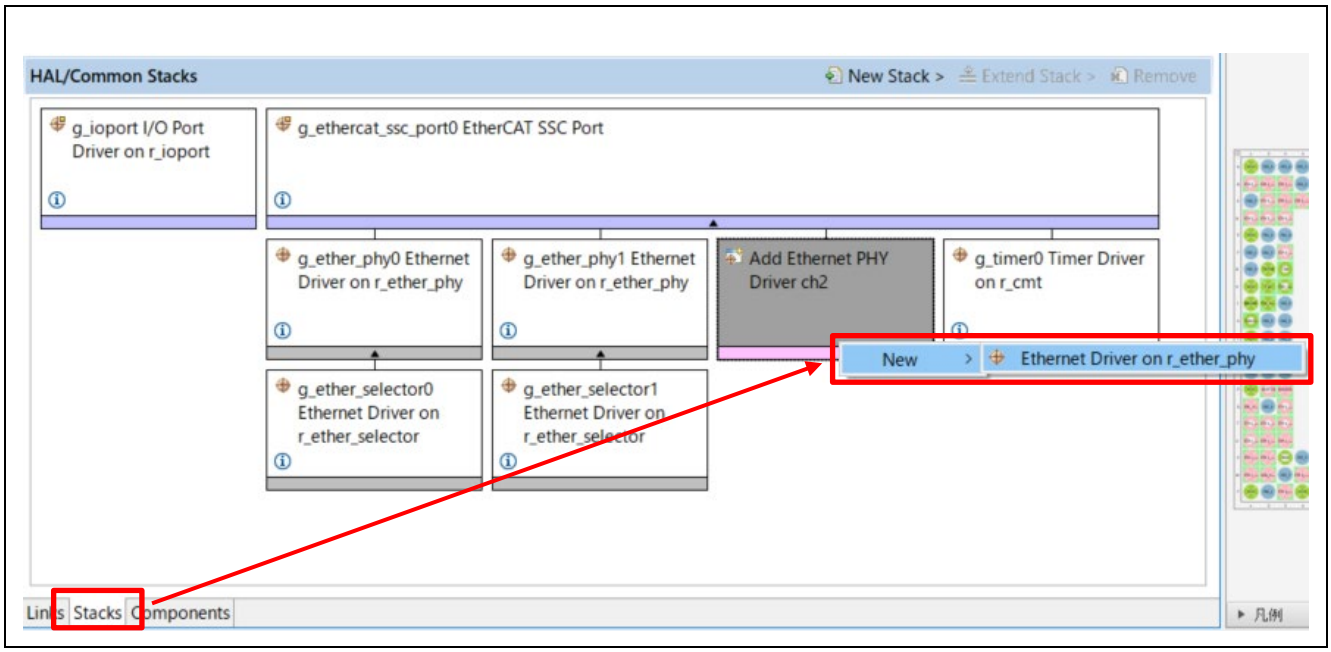
For e2studio, double-click [configuration] on the Project Explorer tab to start smart configurator.



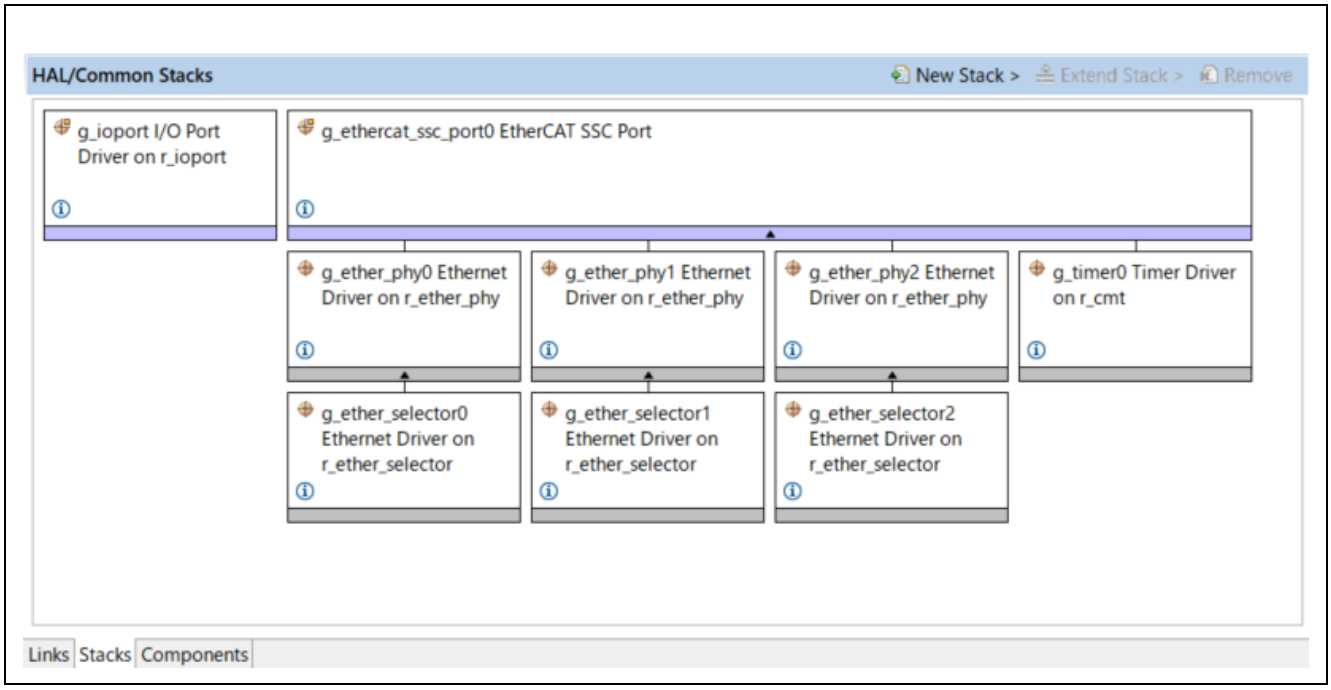
After startup, there is no difference in how to use smart configurator for each tool.

This appendix shows the addition of the 3rd port of EtherCAT.
Display the stack diagram using FSP Configuration. Initially, it is set to 2 ports.

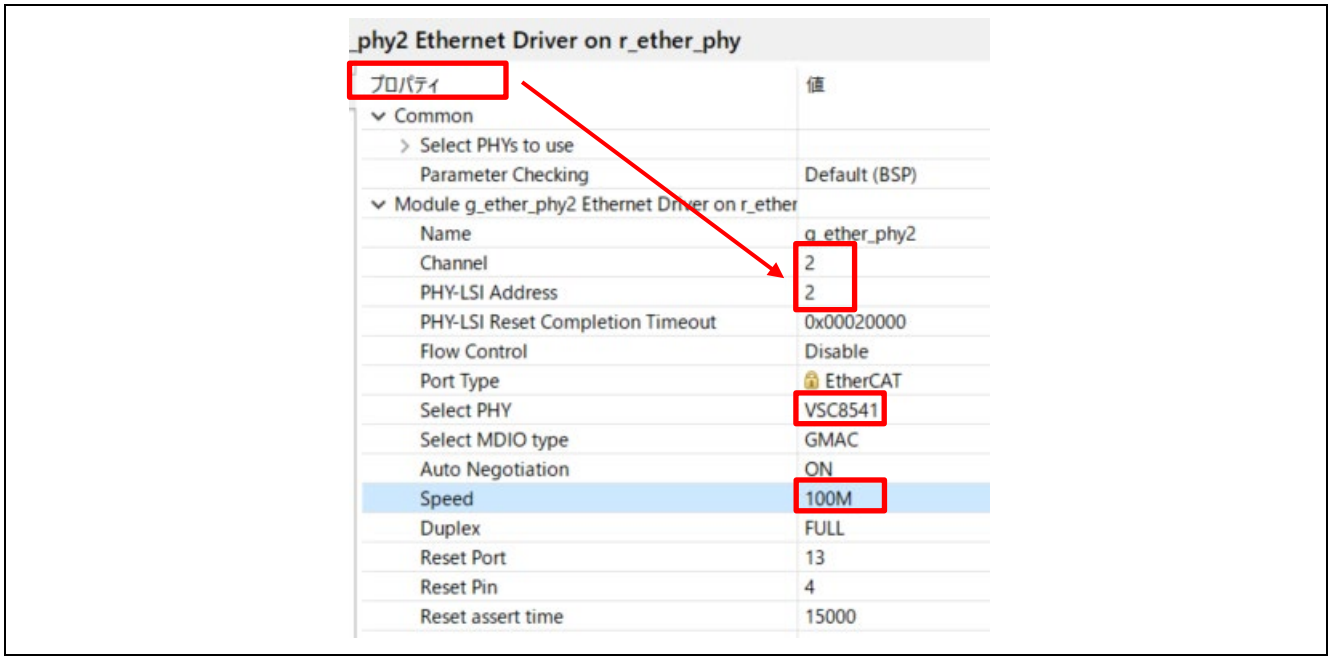
1. Add the 3rd port.
   Add a new ether_PHY. [NEW] →[Ethernet Driver on r_rther_phy]



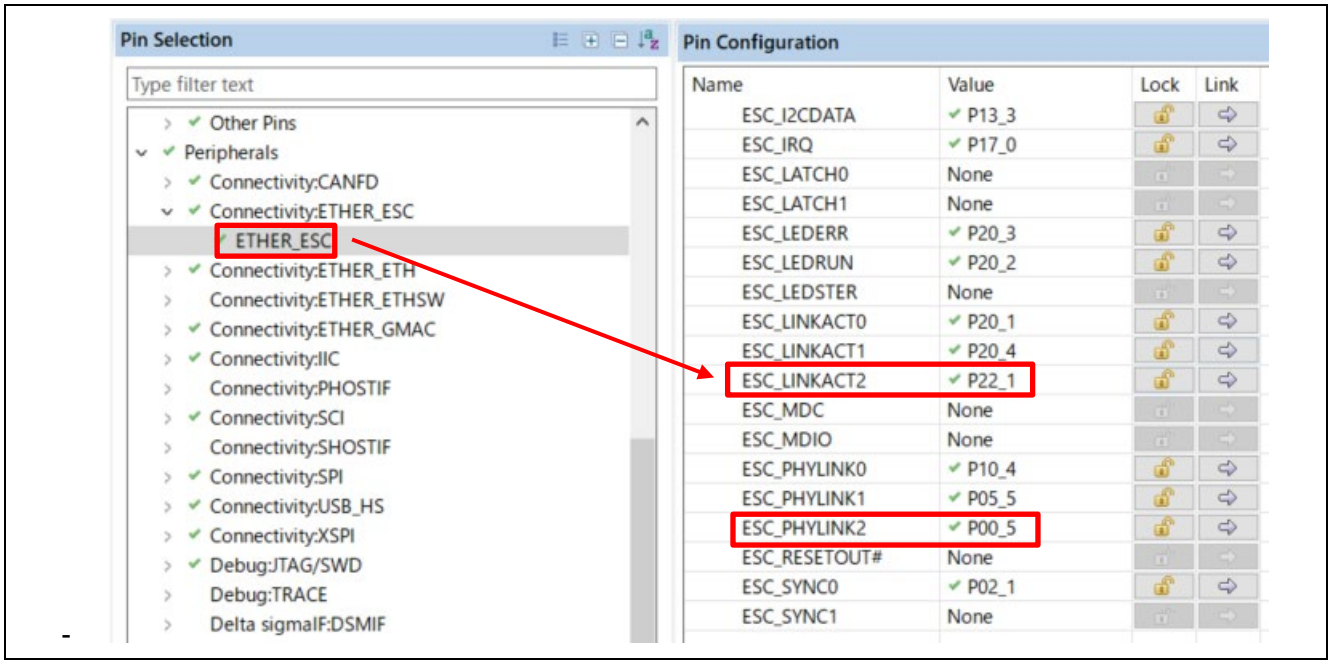
The third port was added.



2. Set the 3rd port PHY
   Set the 3rd port PHY from the PHY properties as follows.
   - Channel:2
   - PHY-LSI Address:2
   - Select PHY:VSC8541
   - Speed:100M

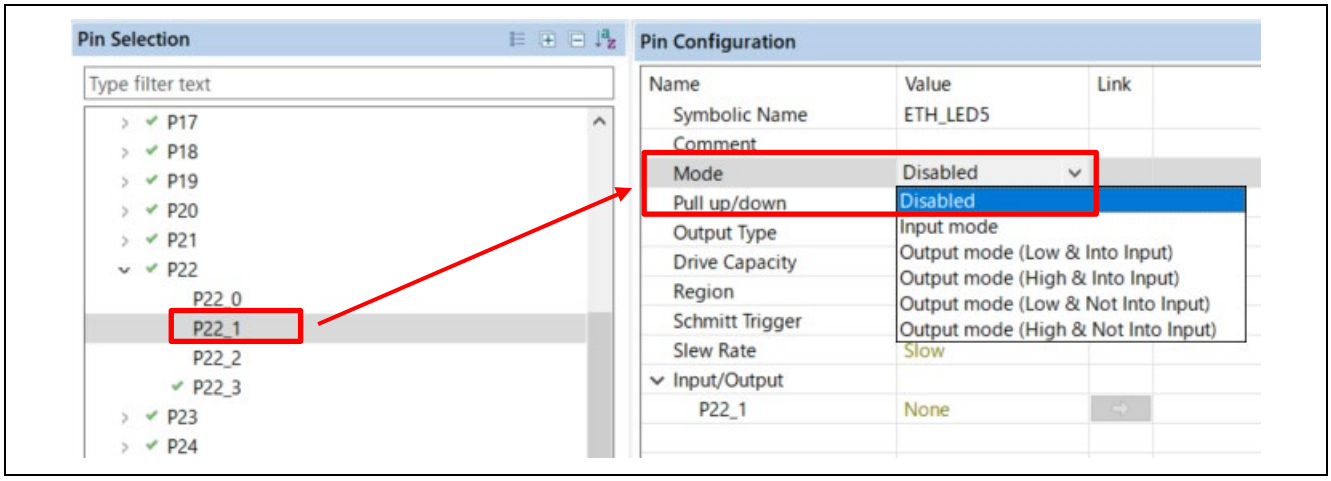


3. Set the ETHER_ESC
   Set the ETHER_ESC from the Pin Selection as follows.
   - ESC_LINKACT2:P22_1
   - ESC_PHYLINK2:P00_5

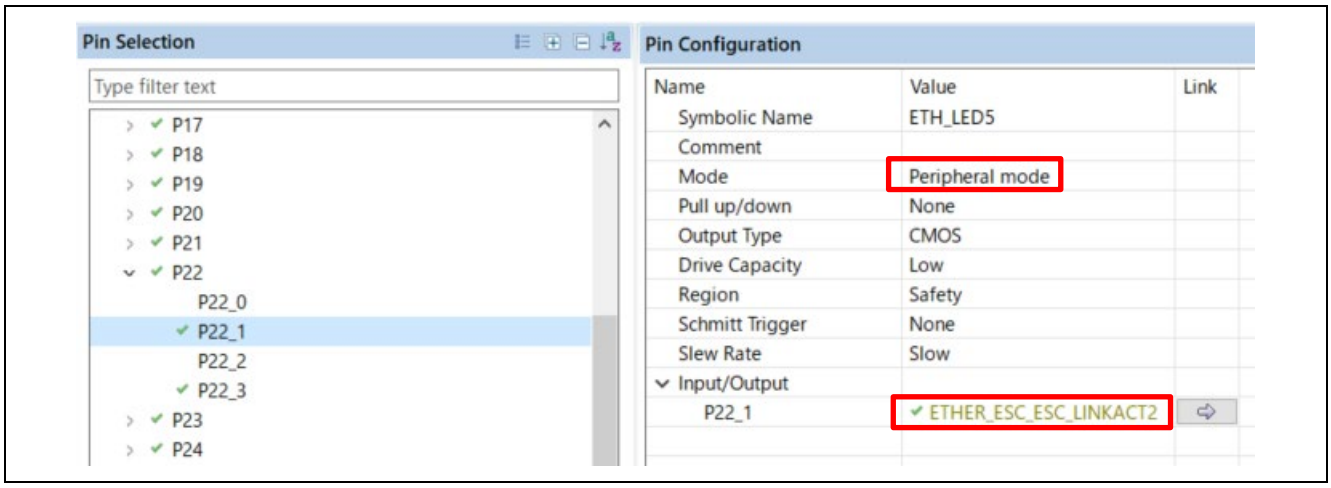


4. Change Pin setting attributes

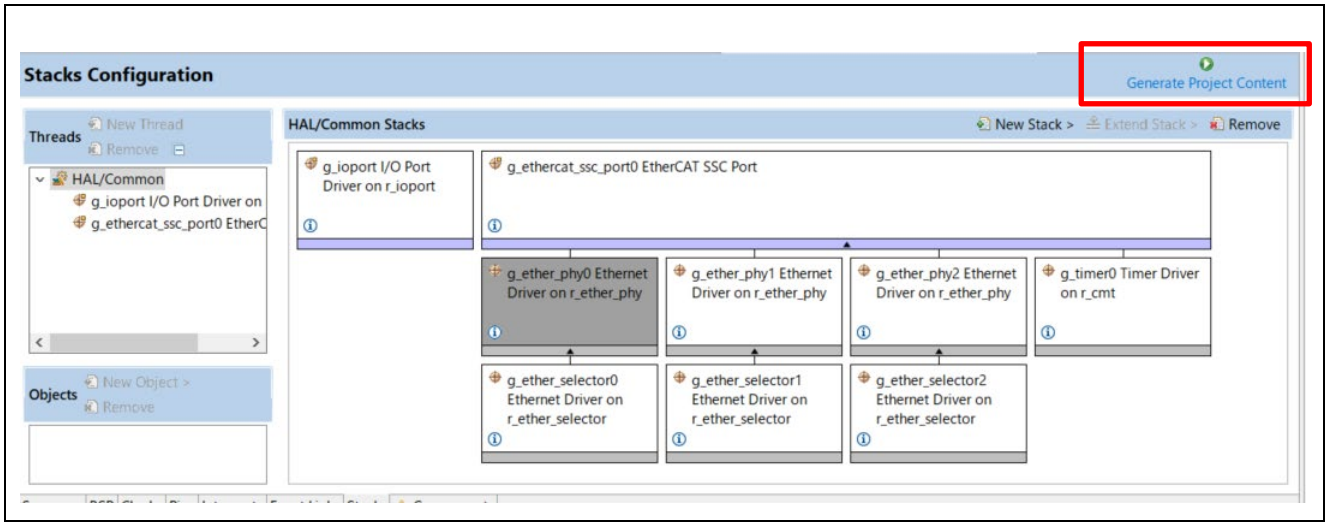
Change the attribute of the Pin set on the 3rd port.
Set the Mode of P22_1 to Disabled.



When the Mode of P22_1 is set to Disabled, it is assigned to [ESC_LINKACT2] and the mode is set to the peripheral mode.



5. After completing all the settings, generate the code with "Generate Project Content".



8. Limitations

1. **This sample program only works in RAM debug mode. Since this sample program executes RAM, it is prohibited to press the "Reset" button during debugging.**

2. **Before running the loaded program, change the CPSR register of CR52 general register on Registers tabs. Change the "T" register bit (bit 5 in CPSR register), which is Thumb execution state bit, from "1" to "0" to switch the instruction mode from "Thumb" to "Arm".**
   For example, when the register value is "0x000001fa", set it to "0x000001da".

3. **When you run the EtherCAT sample program for the first time, be sure to set the number of ports to 2. Write EEPROM data during running in a 2-port configuration. It is not possible to configure 3 ports without writing EEPROM data.**

4. **Program does not start when using xSPI boot mode. So, use the 16bit bus boot mode temporary. Set SW4-2 to OFF.**

5. **DIP SW 3-4 cannot be used.**
   When perform the conformance test, the following sample program needs to be changed.
   RZN2L_EtherCAT_RSK_rev0100\project\rzn2l_rsk_rzn2l\ecat_IO\e2studio\src\ethercat \renesas\sampleappl.c

```
    if (R_BSP_PinRead((bsp_io_port_pin_t)dipsws.p_sws[BSP_DIPSW_0]) == BSP_IO_LEVEL_LOW) u16DipSw |= 0x01;
    if (R_BSP_PinRead((bsp_io_port_pin_t)dipsws.p_sws[BSP_DIPSW_1]) == BSP_IO_LEVEL_LOW) u16DipSw |= 0x02;
    if (R_BSP_PinRead((bsp_io_port_pin_t)dipsws.p_sws[BSP_DIPSW_2]) == BSP_IO_LEVEL_LOW) u16DipSw |= 0x04;

#if 0 // for CTT
    if (R_BSP_PinRead((bsp_io_port_pin_t)dipsws.p_sws[BSP_DIPSW_3]) == BSP_IO_LEVEL_LOW) u16DipSw |= 0x08;
#endif
```

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug 8, 2022	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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